國 立 交 通 大 學

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碩 士 論 文

利用負向主動回授技巧之低壓降穩壓器

A Low-Dropout Regulator with Negative Active-Feedback Frequency Compensation

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A Low-Dropout Regulator with Negative Active-Feedback Frequency Compensation

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摘要

本篇論文詳細討論了利用負向主動回授的補償技巧，來實現低壓降穩壓器(LDO)，文章內容主要可以分成三個部分。

第一部分是探討三級運算放大器的設計。包含利用電流重複使用的技巧，來達到低功率消耗的要求，改善了傳統巢狀米勒補償方式的缺點，此電路以0.35-微米標準金氧半製程製造，在效能與傳統巢狀米勒補償 (NMC) 方式差不多的情形下，所消耗的電流可達到原先的一半；另外一顆放大器則是使用負向主動回授技巧來設計，利用負向主動回授路徑來產生一個左半平面的零點，並藉由此零點所造成的相位增加來補償極點，而順向路徑則可用來得到較佳的頻率與暫態響應，此外，此電路只需要一顆補償電容且相較於巢狀米勒補償並沒有額外電晶體的增加。這個電路是以 0.18-微米標準金氧半製程製造。

第二部分探討參考電壓電路的設計。利用自我偏壓的電路作為主電路電流源的來源，此偏壓電路可用來補償通道長度調變 (channel-length modulation) 所造成電流會隨著電壓源上升而上升的情形，尤其隨著製程的進步，通道長度不斷的縮短，也使得這種影響變的越來越大，此外，藉由電晶體操作在弱反轉區的特性，產生一個不隨溫度變化的參考電壓，我們以 0.35-微米標準金氧半製程設計此一電路。

最後一部分在探討低壓降穩壓器的設計。此電路綜合了負向主動回授的補償技巧以及參考電壓電路，一方面利用負向主動回授路徑所產生的零點，補償系統中過多的極點，使得整個電路能維持穩定，另一方面則藉由參考電壓電路來產生一個不受電壓源及溫度影響的輸入電壓。

Abstract

The thesis describes low-dropout regulator with negative active-feedback frequency compensation. It is divided into three parts.

The first part of this thesis discusses three-stage operational amplifiers. Using current-reused technique fits the demand of low-power dissipation. It improves the shortcoming of the conventional Nested-Miller Compensation (NMC) skill. This circuit has been fabricated by TSMC 0.35-μm N-well CMOS process. Under almost the same performance of CRNMC and NMC amplifiers, the power dissipation is reduced to half of NMC amplifiers. Another three-stage op-amp is proposed by negative active-feedback frequency compensation (NAFFC) techniques. The compensation technique exploits the negative active–feedback path to create a left-half-plane (LHP) zero. By means of the LHP zero adding positive phase, it can cancel out the negative phase-shift pole. At the mean time, a feedforward path is added to the NAFFC amplifier to obtain the better frequency-domain and time-domain performance. Moreover, only one compensation capacitor is needed and no additional transistors are required with comparison to the nested-Miller compensation (NMC) topology. This circuit has been fabricated by TSMC 0.18-μm CMOS process.

The second part of this work discusses how to implement the MOSFET-only voltage reference circuit. The current source of the core circuit mirrors the current coming from a self-biased circuit. This self-biased circuit can compensate the channel-length modulation effect where drain current is increased with supply voltage. Especially in the advanced process, the channel-length modulation effect is becoming more and more prominent when channel length is shorter. Moreover, by means of the characteristics of the subthreshold region, the reference voltage independent of temperature is obtained. This circuit has been implemented in TSMC 0.35-μm N-well CMOS process.

The final part of this work presents the low-dropout (LDO) regulator. The circuit combines the negative active-feedback frequency compensation skill and the voltage reference circuit. In order to make certain the system is stable, using the negative active-feedback path creates a LHP zero to compensate the pole. And the voltage

reference circuit generates the voltage independent of supply voltage and temperature. It is the input voltage of the LDO regulator.

Acknowledgment

I extend my sincere appreciation to my advisor, Professor Chung-Chih Hung, who provides me considerable freedom in my research. Besides, I would like to thank all the members in the Analog Integrated Circuit Laboratory.

I would thank National Chip Implementation Center for providing the TSMC CMOS 0.18 μm and 0.35 μm SPICE model and chip fabrication.

Finally, I would like to express my greatest appreciation to my parents for their without end encouragement and support.

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Chapter 1

Introduction

1.1 INTRODUCTION

The power management is a very important issue today because the mobile electronics are getting more and more popular than ever before. The need for capacity and lifetime of laptop batteries or cell phones are required a lot. However, it isn't suitable to add another battery to our system that is contradictive to the small area demand. Figure 1-1 shows the power management of the mobile phone. It monitors to reduce the standby power consumption and the low-dropout regulator (LDO) is a critical part widely used in it.

There are some reasons to use the LDO circuits. First, because the battery supplies a very noisy voltage leading to the internal circuits suffering the noise influences. It separates the voltage between the battery and the different sub-circuits. Next, it isolates the different subsystems from each other. This is really significant between the analog and digital circuits or in the RF section. Finally, it reduces the sensitivity between the circuitry and the transient voltage changes or ripples of the battery. So in order to provide a low-noise output voltage with high efficiency, it has been widely used like a bridge cascading a switching power supply.

This thesis includes six chapters. Due to the architecture of the LDO regulator consists of the voltage reference circuit and the similar three-stage operational amplifier. First of all we describe two different topologies of op-amp in Chapter 2 and 3. Chapter 2 introduces the Current-Reused NMC (CRNMC) to lower the power of consumption. Chapter 3 demonstrates a negative active-feedback frequency compensation (NAFFC) technique. By means of pole-zero cancellation to obtain the wider bandwidth. Chapter 4 discusses MOSFET-only voltage reference circuit. This circuit consumes less power and provides a high precision reference voltage. The

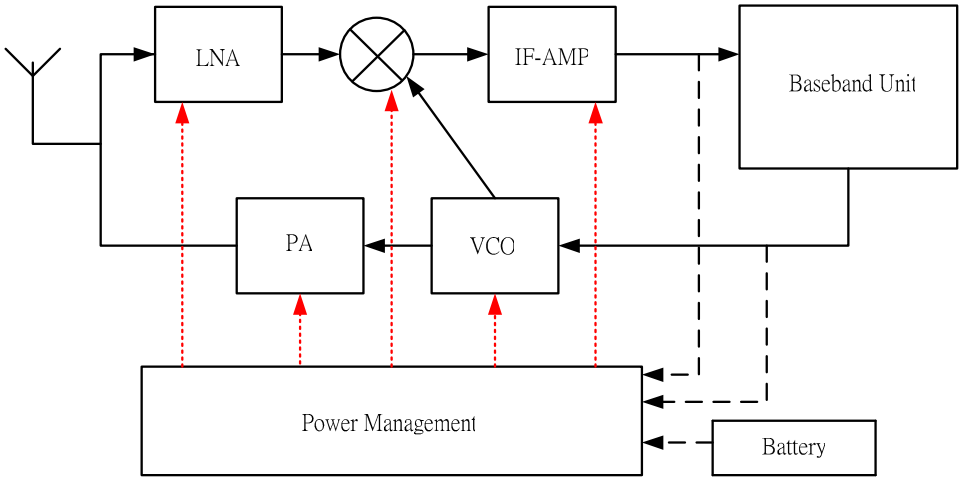


Figure 1-1 Power management of the mobile phone.

LDO circuit which combines the NAFFC amplifier and voltage reference circuit is presented in detail in Chapter 5. Chapter 6 gives a conclusion.

1.2 MULTISTAGE AMPLIFIERS

The increasing demand on very-low-power portable electronic equipment like laptops or mobile phone has pushed analog designer toward the low-voltage researches. In addition, as the feature size of CMOS technology scales down, the supply voltage of digital circuits is also reduced and it is predicted in the ITS roadmap the supply voltage will reach to around 0.6V by 2010 [1]. For analog amplifiers, the conventional approach using vertical-stack (cascode) topology to increase gain is not fitted for low-voltage design. Instead, the more suitable means to enhance gain is to use cascade multiple amplification stages at the low-voltage supply. However, the more complex frequency compensation methods are needed because of additional high impendence nodes causing the low frequency poles [2]-[7]. Fast settling characteristics are another issue that should be paid the attention too. They play important roles in the design of data conversion and switched-capacitor circuits. A longer settling time means the speed of processing analog signals have to be slowed.

Nested-Miller compensation (NMC) amplifier is the most well known topology in the early periods. This configuration is based on the theory of pole-splitting

technique and is not limited to finite stages. However, it sacrifices the bandwidth as increasing the amplification stages to achieve the high dc gain [8]. Another problem is the output stage needs lots of sinking current to maintain the stability leading to be inapplicable in the low-power design.

As such, some recent designs use the feedforward technique to maximize the amplifier bandwidth like multipath nested Miller compensation (MNMC) [2] and nested $G_m - C$ compensation (NGCC) [3] or to remove the Miller capacitors such as no-capacitor feedforward (NCFF) amplifier [9]. The other approaches are recommended to enhance the bandwidth by means of removing the capacitive feedback paths at the output. Without the feedback paths, the novel measures should be provided to make sure an amplifier stable. As a result, damping-factor-control frequency compensation (DFCFC) [10] and dual-loop parallel compensation (DLPC) [11] were reported. A DFCFC amplifier uses damping-factor-control (DFC) block to choose the complex-pole locations and a DLPC amplifier utilizes two parallel paths to propagate high-frequency signals. These two schemes can ensure the stability and achieve the wider bandwidth simultaneously. Moreover, the active-feedback frequency-compensation (AFFC) technique [12] replace passive-capacitive-feedback networks by active-capacitive-feedback ones to reduce the physical size of compensation capacitors and improve the transient responses. Outstanding bandwidth improvement was proposed in single Miller capacitor feedforward frequency (SMCFF) compensation [13]. A SMCFF topology is based on pole splitting and pole-zero cancellation to obtain better small-signal and large-signal performances.

1.3 VOLTAGE REFERENCE CIRCUITS

For the most analog and digital circuits such as low-dropout regulators (LDO), A/D and D/A converters, DRAM and flash memories, a voltage reference is a necessary part. In order to make certain that these circuits could work reliably, the reference voltage should be extremely precise and stable. An ideal voltage reference must be insensitive to the external influences that come from power supply, temperature and process variations. A bandgap voltage reference is usually used. Some researches focus on small-area [17] or low-voltage operation [18] [19], however,

all of them require big-area diodes or parasitic BJT transistors with turn-on voltage as high as 0.6V at room temperature. In the contrast of BJT, the CMOS process is getting more and more prevalent and it has the advantages of smaller area and lower cost. Thus, MOSFET-only voltage reference circuits are presented [20]-[22] and by means of operating MOSFET in the subthreshold region [20] [21] to obtain a low-voltage low-power voltage reference.

1.4 LOW-DROPOUT REGLATORS

As advanced technology is nonstop progressing, the demands for low power and small area are getting stringent. That makes the LDO regulators become the prevalent part of the portable electronic devices. Comparatively speaking, the LDO regulators are easier to integrate in the system-on-chip (SOC) design than switching regulators. Although the latter one achieves the efficiency higher than 80 %, the off-chip inductors and capacitors must be required. Moreover, the LDO regulators produce the stable voltage insensitive to the varying load currents and reduce the voltage ripple. So it's suitable to cascade with a switching regulator to improve the performance and stability of the whole system.

LDO regulators [25]-[29] have been widely used to isolate the different subsystems from each other, especially for SOC design. It separates the analog and digital blocks of the system to prevent the crosstalk problem. In addition, the low quiescent current of LDO regulators increases the battery life of cellular phones, laptops and digital cameras.

Chapter 2

A Low-Power Multistage Operational Amplifier with Current-Reused Technique

2.1 INTRODUCTION

In this chapter, the technique for low-power amplifier design is proposed when still maintaining the same bandwidth of the NMC amplifier. In the following section, a three-stage NMC amplifier is discussed. The low-power design to improve NMC is given in Section 2.3 and then simulation and experimental results are presented in Section 2.4.

2.2 NESTED-MILLER COMPENSATION

The general structure of the NMC op amp is shown in Figure 2-1, where $g_{m1} \sim g_{m3}$ are the transconductances of the amplification stages 1~3, $R_{o1} \sim R_{o3}$ are the output resistances, $C_1 \sim C_2$ and C_L are the parasitic and loading capacitors, respectively, and the compensation capacitors are $C_{m1} \sim C_{m2}$. According to Leung *et al*. [5] and [8], the NMC amplifier in the unity-gain feedback architecture should have the third-order Butterworth frequency response. The dimension of C_{m1} and C_{m2} can be approximated as [8]

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{m3}}\right)C_L \tag{2-1}$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{m3}}\right)C_L \tag{2-2}$$

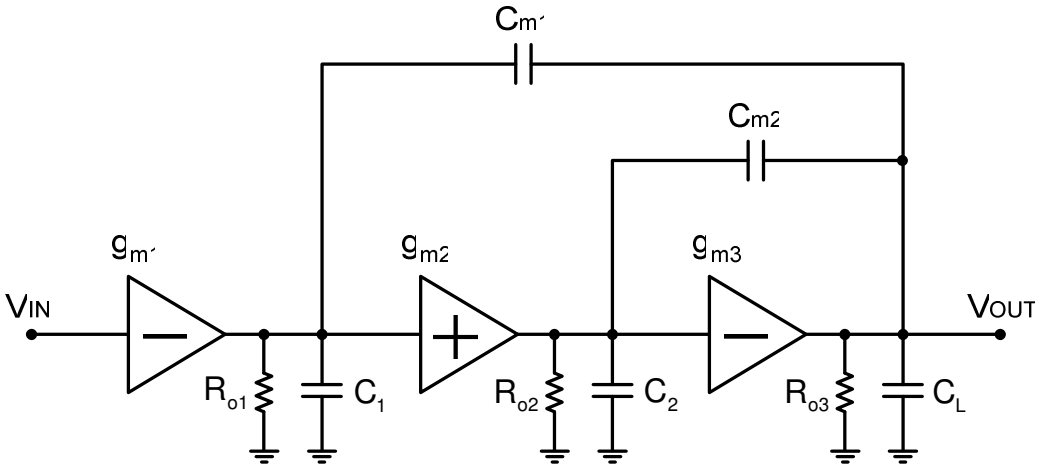


Figure 2-1 Block diagram of the NMC amplifier.

and the gain-bandwidth product (GBW) is given by [8]

$$\text{GBW}=\frac{1}{4}\left(\frac{g_{m3}}{C_L}\right) \tag{2-3}$$

Under the above compensation, the phase margin (PM) is about 60° and the first pole is located at $\omega_{\text{3-dB}}=-1/g_{m2}\,g_{m3}R_{o1}R_{o2}R_{o3}C_{m1}$. The nondominant complex poles are $\omega_{\text{p2, 3}}=-(g_{m3}/2C_L)\pm j(g_{m3}/2C_L)$ and the damping factor of the complex poles is $1/\sqrt{2}$.

The stability analysis is carried out based on the following assumptions:

1). The positions of the zeroes must locate at higher frequency than the poles.

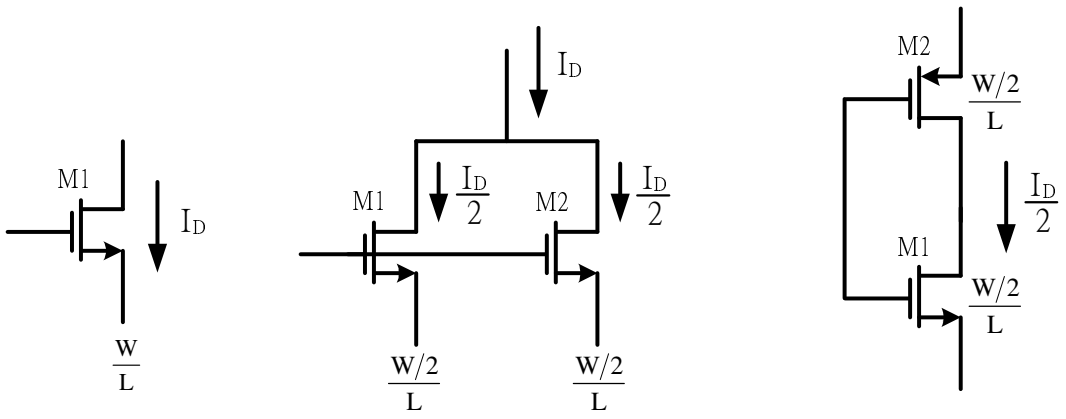
2). The gain of each stage is larger than one.

3). The parasitic capacitances are smaller than the compensation and loading ones.

4). The transconductance of the output stage g_{m3} is much larger than g_{m1} and g_{m2}.

It should be noted that a NMC amplifier is more stable when $g_{m3} >> g_{m1}$ and g_{m2} comes into existence. However, the higher transconductance represents the transistor should sink more current than any other's, so it causes the NMC amplifier hardly achieve the low-power design.

Table 2-1 lists different g_{m3} values with distinct capacitor dimensions, GBW



(a) (b) (c)

Figure 2-2 Illustration of the current-reuse technique.

and current consumption of the output stages according to Equations (2-1)-(2-3). From simulation and process parameters, the third amplification stage of $W/L=160$ and $\mu_n C_{ox} \approx 200\mu A/V$ are proposed. In fact, the current dissipation of the output stage is proportional to g_{m3}, and so is GBW; However, the required compensation capacitance to maintain stability decreases with g_{m3}. The following section provides a technique to maintain large g_{m3}, but at the same time the sinking current reduces almost a half.

TABLE 2-1

NMC AMPLIFIER WITH DIFFERENT g_{m3}

($C_L=100\,pF$, $\mu_n C_{ox} \approx 200\mu A/V$ and $(W/L)_3=160$)

	g_{m1} (μA/V)	g_{m2} (μA/V)	g_{m3} (μA/V)	C_{m1} (pF)	C_{m2} (pF)	GBW (MHz)	Output-stage current (μA)
NMC	100	50	500	80	20	0.2	3.9
			1000	40	10	0.4	15.6
			2000	20	5	0.8	62.5
			3000	13.3	3.3	1.2	140.6

2.3 CURRENT-REUSED NMC

The purpose of the current-reuse technique [16] is to achieve the transconductance of a single device with less current. The derivation is illustrated in

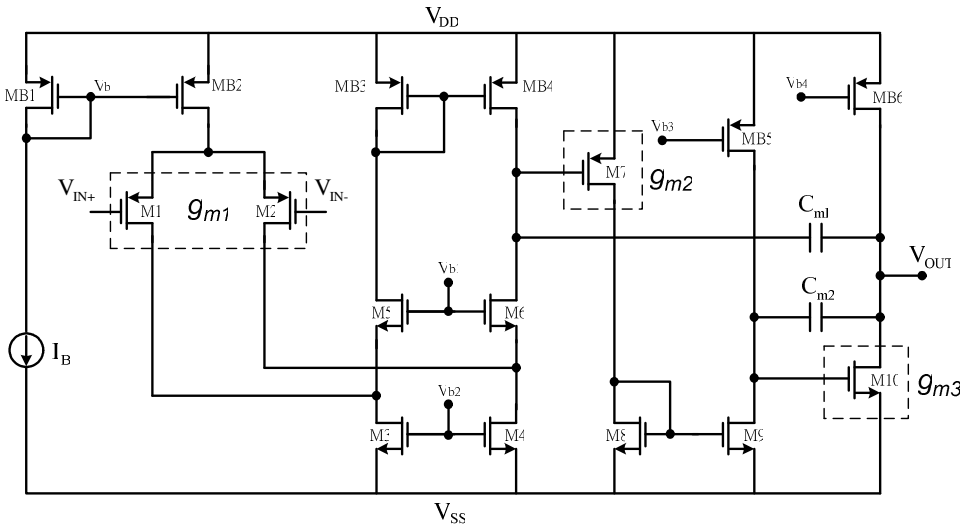


Figure 2-3 Schematic of the NMC amplifier.

Figure 2-2. Figure 2-2(a) shows that a NMOS transistor has a dimension ratio W/L and drain current I_D where $g_{m1} = \sqrt{2I_D\mu_n C_{ox}(W/L)_1}$. To obtain the same g_m, the two NMOS transistors are in parallel with aspect ratio $(1/2)W/L$ and drain current $(1/2)I_D$ in Figure 2-2(b). Thus the equivalent transconductance could be expressed by $g_{m,\text{eq}} = g_{m1} + g_{m2} = 2\sqrt{I_D\mu_n C_{ox}(W/2L)_1} = \sqrt{2I_D\mu_n C_{ox}(W/L)_1}$. Finally, in Figure 2-2(c), a PMOS transistor is folded to substitute for the device M2 in Figure 2-2(b). The above equation is then modified to $g_{m,\text{eq}} = \sqrt{I_D\mu_n C_{ox}(W/2L)_1} + \sqrt{I_D\mu_p C_{ox}(W/2L)_2}$ which is smaller than g_m of single transistor in Figure 2-2(a) because the mobility μ_n of NMOS is nearly three times than μ_p of PMOS. But the current is reduced to half as compared with Figure 2-2(a).

From Table I, if g_{m3} equals to $3000\mu A/V$, the output-stage current is 140.6μA. Using the current-reuse technique, the current can be decreased to 70.3μA. By means of this technique, the power consumption is reduced to half, but still suitable for high GBW application. The detailed circuit structures of NMC and CRNMC are shown in Figure 2-3 and Figure 2-4, respectively. The only difference is the transistor M10 of the NMC amplifier is now substituted by M101 and M102 in the CRNMC amplifier.

2.4 SIMULATION AND EXPERIMEATAL RESULTS

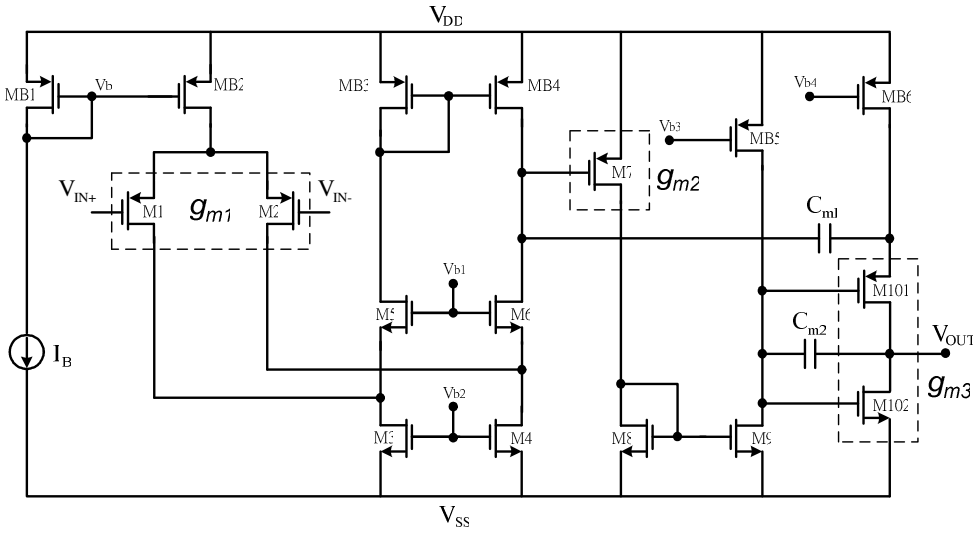


Figure 2-4 Schematic of the CRNMC amplifier.

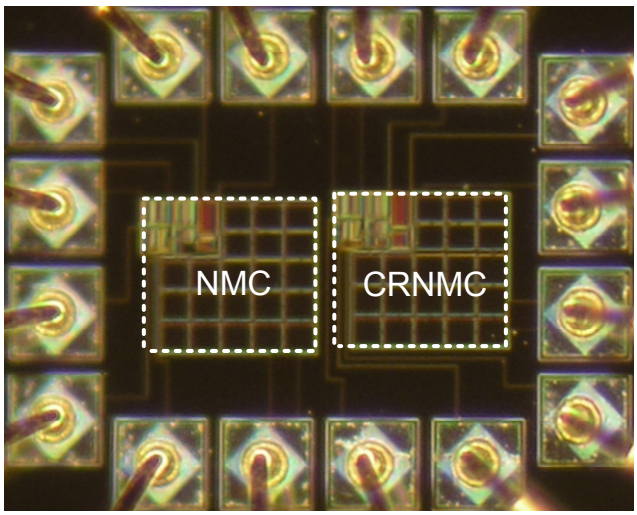


Figure 2-5 Chip photo of the NMC and CRNMC amplifiers.

In order to confirm the proposed technique, the post-layout simulations are presented using the TSMC 0.35μm CMOS technology. The circuit parameters of the NMC amplifier are $g_{m1}=125\mu A/V$, $g_{m2}=80\mu A/V$, $g_{m3}=3260\mu A/V$, $C_{m1}=16pF$, $C_{m2}=4.5pF$ and $C_L=100pF$. The measured power consumption equals to 352 μW which is larger than 155 μW of the CRNMC amplifier. The rest of the performance indexes are nearly the same for the two amplifiers. The chip photo of the NMC and CRNMC amplifiers are shown in Figure 2-5. Figure 2-6 and 2-7 illustrate the frequency response of both amplifiers. Their dc gain are close to 100dB and PM's are both about $60°$.

The step responses and settling time of the amplifiers were simulated by 0.5

Vp-p input steps. The slew rate is about 0.25 V/μs and 1% settling time is nearly to 3.5 μs. Figure 2-8 shows the transient responses of the two amplifiers. The performance of NMC and CRNMC amplifiers are listed in Table 2-2 for comparison.

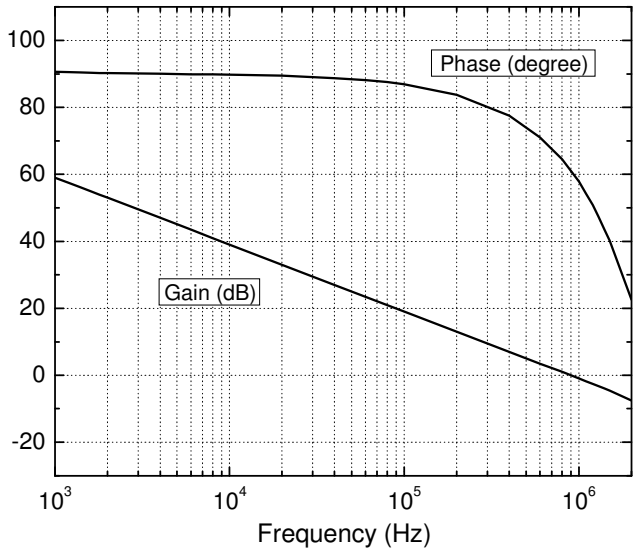


Figure 2-6 The frequency response of the NMC amplifier.

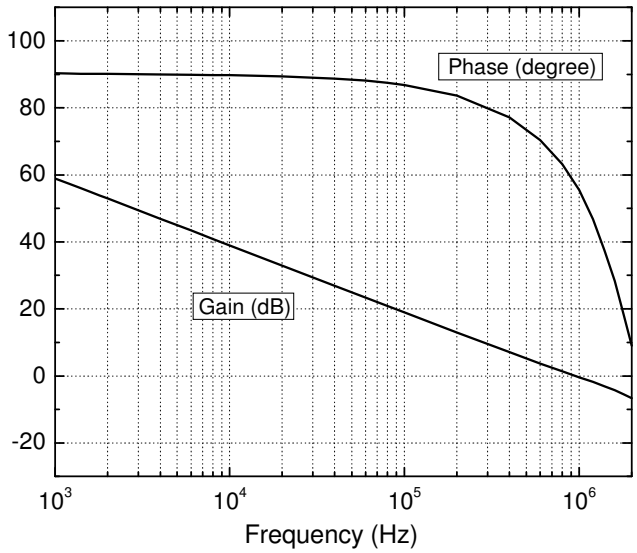
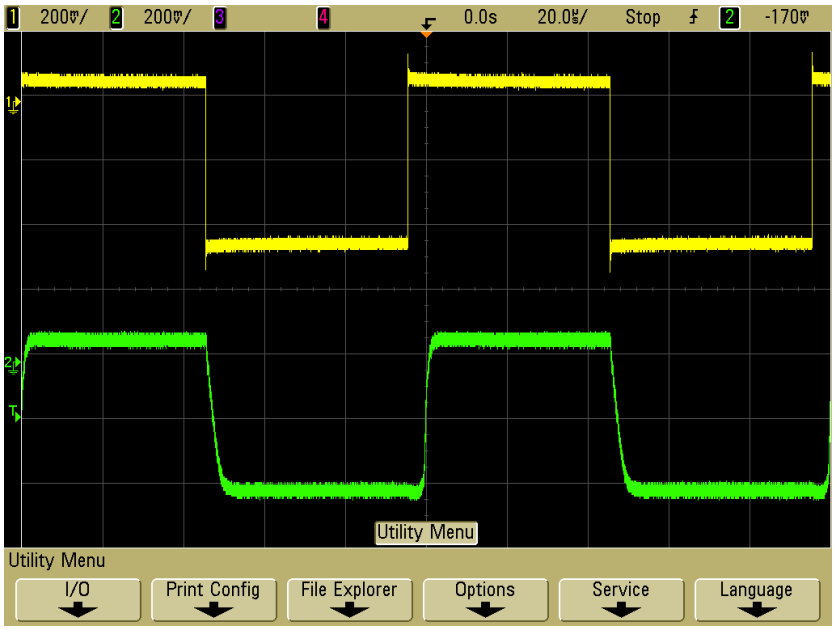
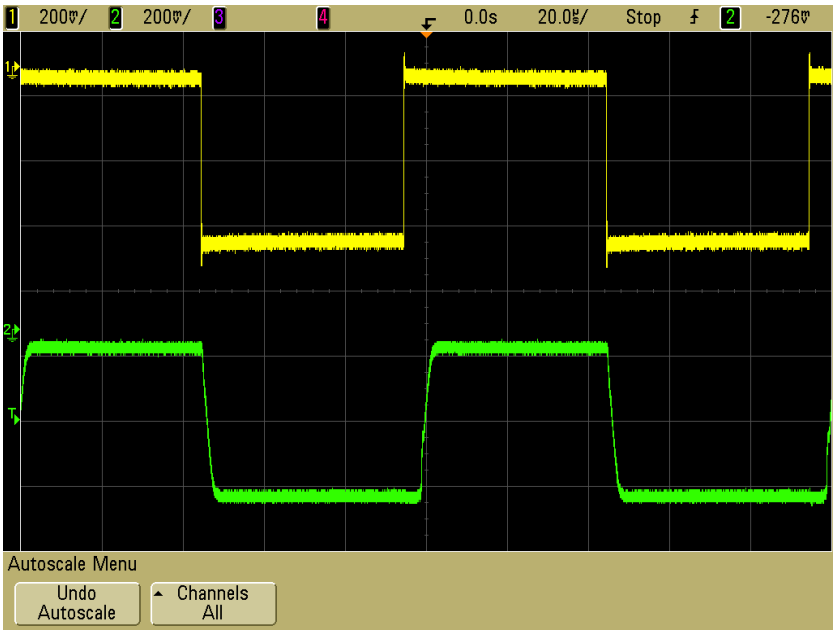


Figure 2-7 The frequency response of the CRNMC amplifier.



(a)



(b)

Figure 2-8 Transient responses of input step and (a) NMC (b) CRNMC.

TABLE 2-2
COMPARISON OF NMC AND CRNMC AMPLIFIERS

Parameter	NMC	CRNMC
Supply voltage	1.5V	
Load	100pF ‖ 25kΩ	
Gain (dB)	98.5	102
PM	61.1°	57.2°
GBW (MHZ)	0.899	0.952
Current consumption (μA)	352	155
SR^+/SR^- (V/μs)	0.333 / -0.133	0.128 / -0.377
T_S^+/T_S^- (μs)	1.54 / 4.61	4.64 / 2.84
Area (mm^2)	0.045	0.045

Chapter 3

Negative Active-Feedback Frequency Compensation Technique for Multistage Amplifiers

3.1 INTRODUCTION

A new topology, the negative active-feedback frequency compensation (NAFFC) scheme, is presented in this chapter. For the purpose of achieving wide bandwidth, it avoids the capacitive feedback paths at the output and using pole-zero cancellation skill. Figure 2-1 shows the conventional NMC amplifier. The compensation capacitor C_{m1} connects the first amplification stage and output stage. According to Miller effect theorem, capacitor C_{m1} creates the dominant pole close to very low frequency because of the high gain. This leads to the low gain-bandwidth product. Moreover, the capacitor C_{m2} which connects the second amplification stage and output stage is short when op-amp is operated at high frequency. Consequently, the feedback path results in the lower high-frequency gain [14]. By means of removing these two capacitors, the wide bandwidth is obtained. At the mean time, the output push-pull stage increases the slew-rate. The following sections will make a detailed description. In Section 3-2, the principle of NAFFC technique is discussed. Section 3-3 addresses the simulation and experimental results.

3.2 PROPOSED NEGATIVE ACTIVE-FEEDBACK FREQUENCY COMPENSATION AMPLIFIER

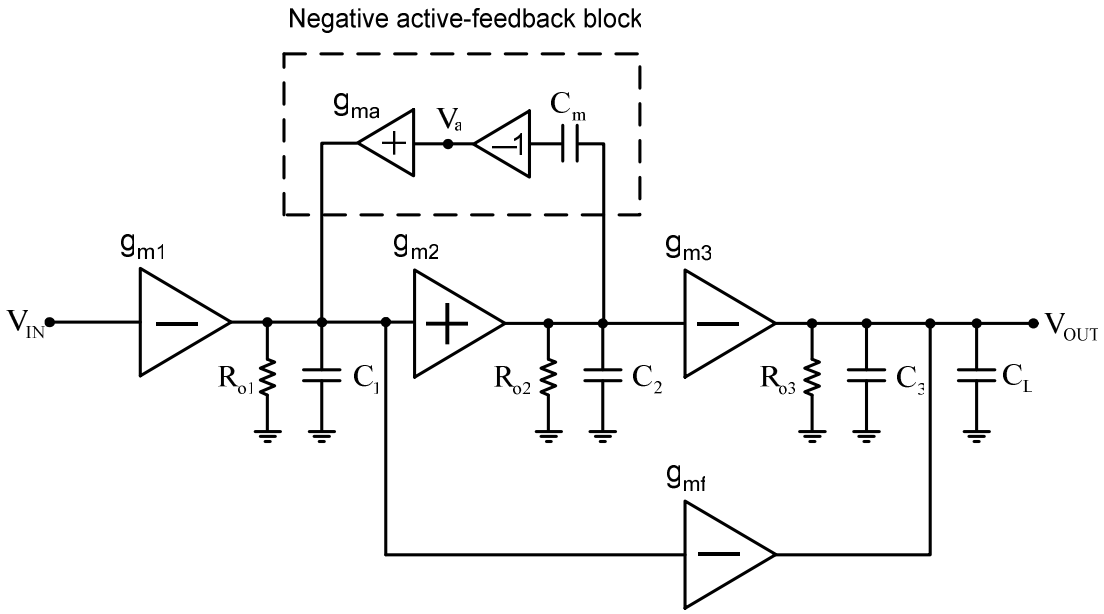


Figure 3-1 Block diagram of the NAFFC amplifier.

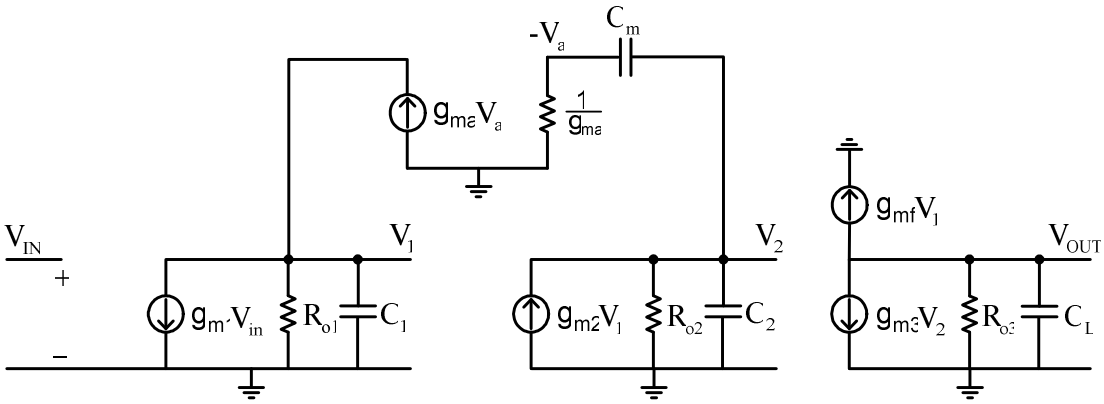


Figure 3-2 Equivalent small-signal circuit of the NAFFC amplifier.

3.2.1 Topology

The proposed topology is shown in Figure 3-1, where only one compensation capacitor is connected between the first and second stage, reducing the feedback capacitive paths at the output so the larger bandwidth can be obtained. However, the second stage providing the positive transconductance results in positive feedback leading the system unstable. For this reason the negative sign should be added to this feedback path and active stage g_{ma} is used to create left-half-plane (LHP) zero. In addition, the feedforward stage g_{mf} not only makes a push-pull stage at the output to improve the transient response but shifts the LHP zero close to low frequency to cancel the second non-dominant pole.

3.2.2 Small-signal analysis

The equivalent small-signal circuit of the NAFFC amplifier is shown in Figure 3-2. In order to simplify the transfer function, the following assumptions should be made. One is that the dc gain of all stage must be greater than one. Another is the parasitic capacitances have to be much smaller than the output load capacitance.

Depending on above assumptions, the transfer function can be expressed by

$$A_v(s) = \frac{A_{dc}\left[1 + sC_m\left(\frac{g_{mf}}{g_{m2}g_{m3}} + \frac{1}{g_{ma}}\right) + s^2\frac{g_{mf}C_mC_2}{g_{ma}g_{m2}g_{m3}}\right]}{\left(1 + \frac{s}{\omega_{-3\text{dB}}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)\left(1 + s\frac{C_1}{g_{m2}} + s^2\frac{C_1C_2}{g_{m2}g_{ma}}\right)}. \tag{3-1}$$

From numerator of (3-1), there are two LHP zeros. One of the zeros is at a much higher frequency which doesn't affect the phase margin of the amplifier due to C_m is greatly larger than C_2. The transfer function can be approximated as a one-zero system

$$A_v(s) \approx \frac{A_{dc}\left[1 + sC_m\left(\frac{g_{mf}}{g_{m2}g_{m3}} + \frac{1}{g_{ma}}\right)\right]}{\left(1 + \frac{s}{\omega_{-3\text{dB}}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)\left(1 + s\frac{C_1}{g_{m2}} + s^2\frac{C_1C_2}{g_{m2}g_{ma}}\right)}. \tag{3-2}$$

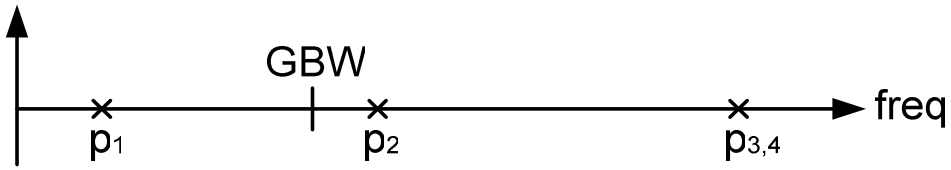
where A_{dc}, $\omega_{-3\text{dB}}$ and ω_{p2} are the dc gain, dominant pole and second non-dominant pole, respectively, which are given by

$$A_{dc} = g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3} \tag{3-3}$$

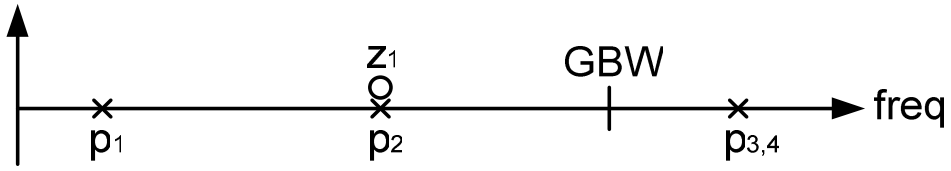
$$\omega_{-3\text{dB}} = -\frac{1}{g_{m2}R_{o2}R_{o1}C_m} \tag{3-4}$$

$$\omega_{p2} = -\frac{1}{R_{o3}C_L}. \tag{3-5}$$

From (3-2), there are a LHP zero, ω_z, to boost the phase margin and a pair of



(a)



(b)

Figure 3-3 The pole and GBW locations (a) without zero (b) with zero.

complex pole $|\omega_{p3,4}|$ with quality factor Q, which are given as

$$\omega_z = -\left[C_m \left(\frac{g_{mf}}{g_{m2} g_{m3}} + \frac{1}{g_{ma}} \right) \right]^{-1} \tag{3-6}$$

$$|\omega_{p3,4}| = \sqrt{\frac{g_{ma} g_{m2}}{C_1 C_2}} \tag{3-7}$$

$$Q = \sqrt{\frac{g_{m2} C_2}{g_{ma} C_1}}. \tag{3-8}$$

3.2.3 Stability issues

Owing to two poles and a pair of complex pole in this system, the gain-bandwidth product (GBW) should be at a low frequency to ensure the stability. However, the LHP zero cancels second non-dominant pole causing the location of GBW moves to a higher frequency. Figure 3-3 shows how to place the pole and zero location to obtain the wide bandwidth.

For simplification, we assume the dimensions of the two parasitic capacitors are almost equal, $C_1 \approx C_2$, and the Q value of the complex pole is $1/\sqrt{2}$ which implies no peaking in the magnitude response. From above assumption and (3-8), the g_{ma} is given as

$$g_{ma} = 2 g_{m2}. \tag{3-9}$$

Moreover, the pole-zero cancellation means

$$\omega_z = \omega_{p2} \Rightarrow \frac{1}{C_m\left(\frac{g_{mf}}{g_{m2}g_{m3}} + \frac{1}{g_{ma}}\right)} = \frac{1}{R_{o3}C_L} \tag{3-10}$$

where $g_{mf} \approx g_{m3}$ and applying (3-9) into (3-10), the C_m is calculated as

$$C_m = \frac{2g_{m2}R_{o3}C_L}{3} = \frac{g_{ma}R_{o3}C_L}{3}. \tag{3-11}$$

From (3-11), the dimension of the compensation capacitor is proportional to the output capacitive and resistive loads. Thus, by choosing the smaller g_{m2} reduces the size of C_m.

After the pole-zero cancellation and from (2-3), (3-3), (3-4) and (3-11), the GBW is given by

$$\begin{aligned} \text{GBW} &= \frac{g_{m1}g_{m3}R_{o3}}{C_m} \\ &= \frac{3g_{m1}g_{m3}}{2g_{m2}C_L} \\ &= \frac{6g_{m1}}{g_{m2}}\text{GBW}_{(\text{NMC})} \end{aligned} . \tag{3-12}$$

As indicated in (3-12), the GBW of the NAFFC amplifier bases on the distinction between g_{m1} and g_{m2}, so in order to maximize the GBW, g_{m1} should be designed much lager than g_{m2}.

Finally, the phase margin (PM) of the NAFFC amplifier is calculated as

$$\begin{aligned} \text{PM} &= 180° - \tan\frac{\text{GBW}}{\omega_{\text{-3dB}}} - 2\tan\frac{\text{GBW}}{\left|\omega_{\text{p3,4}}\right|} \\ &\approx 90° - 2\tan\frac{3g_{m1}g_{m3}C_1}{2\sqrt{2}g_{m2}{}^2C_L} \end{aligned} . \tag{3-13}$$

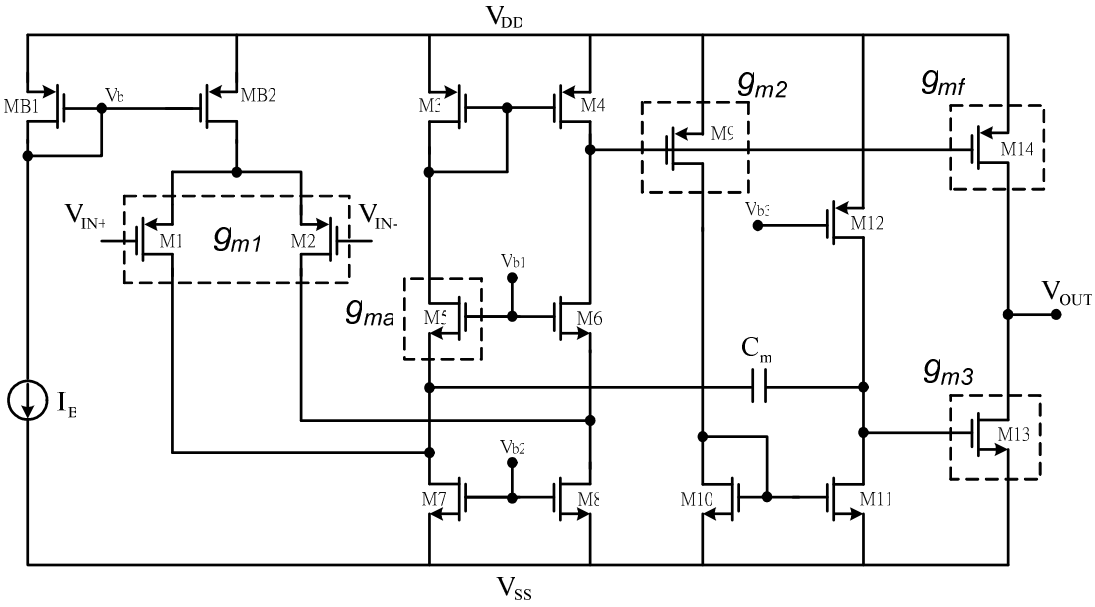


Figure 3-4 Schematic of the NAFFC amplifier.

Owing to the small dimensions of C_1 and C_2, PM is nearly larger than $60°$.

3.2.4 Slew rate and settling time

The feedforward transconductance stage and the third amplification stage form a push-pull output stage which improves the transient response of the NAFFC amplifier. In addition, the feedforward stage also helps to shift a LHP zero to a lower frequency to enhance the driving capability as increasing the value of the loading capacitor. Without this feedforward path, the transfer function is given by

$$A_v(s) = \frac{A_{dc}\left(1 + s\frac{C_m}{g_{ma}}\right)}{\left(1 + \frac{s}{\omega_{-3dB}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)\left(1 + s\frac{C_1}{g_{m2}} + s^2\frac{C_1 C_2}{g_{m2} g_{ma}}\right)} \tag{3-14}$$

where the denominator of (3-14) is the same with (3-2) but the LHP zero is farer.

It should be noted that the pole-zero doublet may degrade the settling time and the effect depends on the pole-zero spacing and its frequency [15]. So the transconductances of each gain stages should be chosen precisely to avoid the imperfect pole-zero cancellation.

3.2.5 Circuit description

The schematic of the NAFFC amplifier is shown in Figure 3-4. The transistors M1-M8 compose of the first folded-cascode stage with a PMOS differential input pair. The second noninverting gain stage consists of transistors M9-M11 and transistor M9 provides the transconductance g_{m2}. At the last gain stage, the transistor M13 generates transconductance of g_{m3} and M14 provides the feedforward path to improve the phase margin. In the negative active-feedback block, the compensation capacitor connects to the source of transistor M5 opposite to M6, the minor sign could be acquired and M5 is the active-feedback transistor. In fact, the architecture of the NAFFC op amp is easy to implement and extra transistors are not needed with a comparison to the NMC topology.

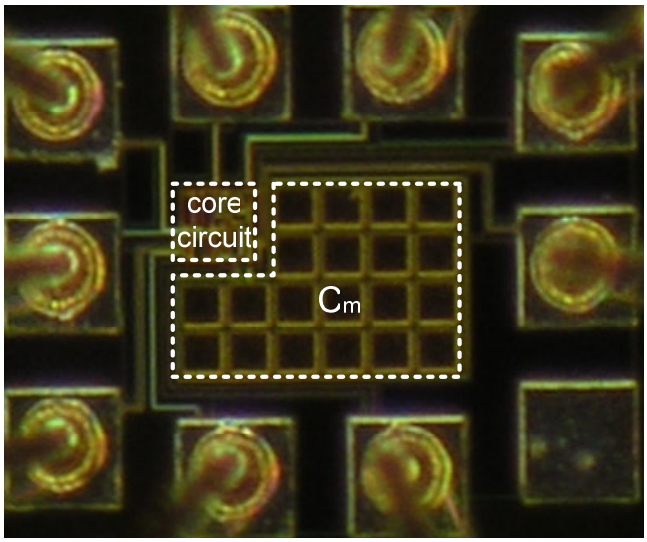


Figure 3-5 Chip photo of the NAFFC amplifier.

3.3 SIMULATION AND EXPERIMENTAL RESULTS

The proposed NAFFC amplifier was fabricated in TSMC 0.18-μm CMOS technology. Figure 3-5 shows the chip photograph of the amplifier. From post-layout simulation, g_{m1} = 161.9 μA/V, g_{m2} = 66.1 μA/V, g_{m3} = 4019.8 μA/V, g_{ma} = 124.8 μA/V, g_{mf} = 4630.3 μA/V, and C_m = 18 pF.

The NAFFC amplifier uses the supply voltage of 1.2-V and has a load of 100 pF connecting in parallel with 25 kΩ. The simulated frequency responses are shown in

Figure 3-6 (a) and (b). The dc gain is larger than 100 dB with phase margin of 64° and GBW of 18.9 MHz. In Figure 3-7, the transient response in unity gain feedback with 0.5-V step input is shown. The average slew rate and 1% settling time are 2 V/μs and 0.985 μs, respectively. Table I summarizes the detailed performance.

In order to precisely compare different amplifiers, two formulas are used to weigh the tradeoff between gain bandwidth product (GBW), slew rate (SR), load capacitance (C_L), and power consumption (PC), which are given by [4] [10]

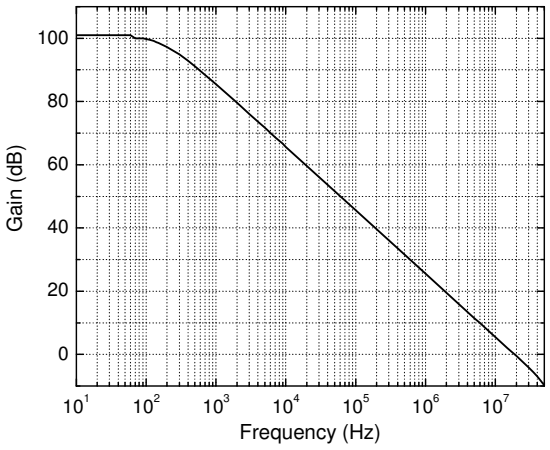
$$\mathrm{FOM_S} = \frac{\mathrm{GBW[MHz]} \cdot C_L\mathrm{[pF]}}{\mathrm{PC[mW]}} \tag{3-15}$$

$$\mathrm{FOM_L} = \frac{\mathrm{SR[V/}\mu s\mathrm{]} \cdot C_L\mathrm{[pF]}}{\mathrm{PC[mW]}}. \tag{3-16}$$

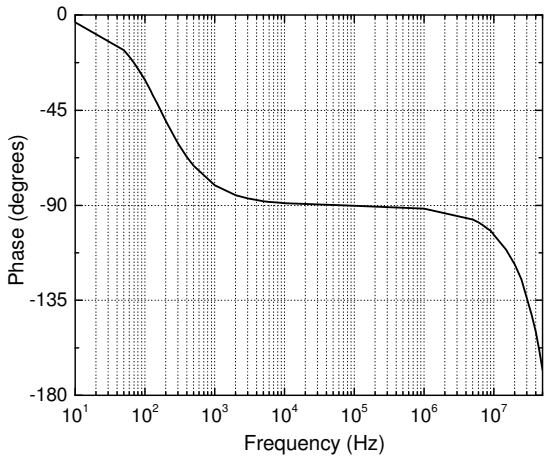
Table II presents the comparison results of different multistage amplifiers. The both formulas are also given. Apparently, the NAFFC amplifier has the most excellent performance.

TABLE 3-1
PERFORMANCE OF NAFFC AMPLIFIER

Technology	0.18-μm CMOS
Voltage supply	± 0.6 V
DC gain	101 dB
Unit-gain frequency	18.9 MHz
Phase margin	64°
Positive slew rate	2.74 V/μs
Negative slew rate	1.34 V/μs
Positive settling time	1.18 μs
Negative settling time	0.79 μs
Power consumption	0.239 μW
Load	100 pF //25 kΩ
Area	0.028 mm^2



(a)



(b)

Figure 3-6 Simulated frequency response of the NAFFC amplifier with 25kΩ//100pF load. (a) Magnitude response (b) Phase response.

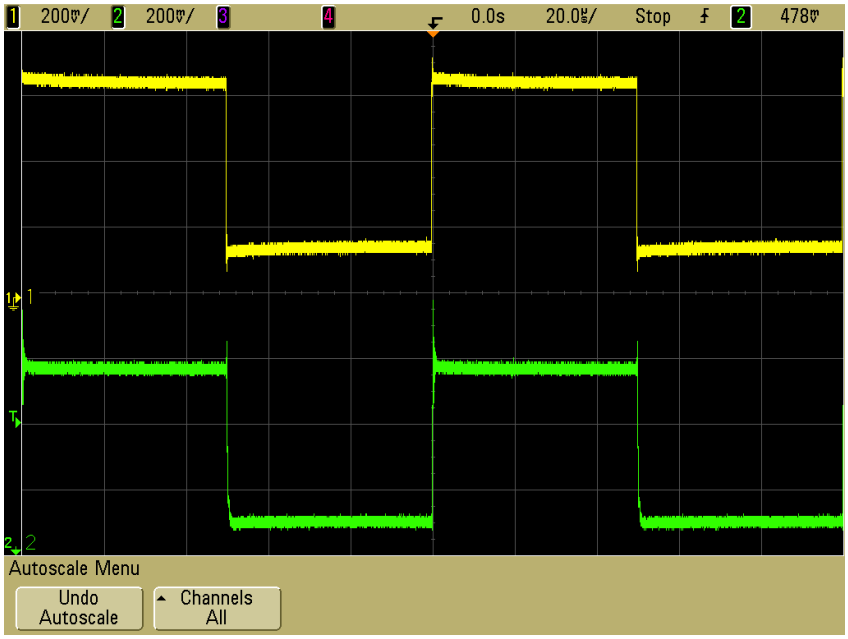


Figure 3-7 Transient Response of the NAFFC amplifier in unit-gain feedback topology with a 0.5-V step input.

TABLE 3-2

COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS

	Gain (dB)	GBW (MHz)	Power (mW@Vdd)	SR^+ / SR^- (V/μs)	$T_S{}^+ / T_S{}^-$ to 1% (μs)	C_L (pF)	FOM_S $\left(\frac{\text{MHz}\cdot\text{pF}}{\text{mW}}\right)$	FOM_L $\left(\frac{\text{V}/\mu\text{s}\cdot\text{pF}}{\text{mW}}\right)$	Technology
Eschauzier [2]	100	100	76@8	35	60	100	131	46	3 GHz f_T BJT
You [3]	100	1	1.4@2	5	--	20	14	71	2μm CMOS
Ng [4]	102	47	6.9@3	89/48	--	40	272	400	0.6μm CMOS
Leung [5]	>100	1.8	0.4@2	0.82/0.75	1.12/1.18	100	450	196	0.8μm CMOS
Ramos [7]	>100	2.7	0.275@1.5	1/1	1.4/1.0	130	1276	473	0.35μm CMOS
Leung [10]	>100	2.6	0.42@2	1.36/1.27	0.96/1.37	100	619	314	0.8μm CMOS
Lee [11]	>100	7	0.33@1.5	2.2/4.4	0.315/0.68	120	2545	1200	0.6μm CMOS
Lee [12]	>100	4.5	0.4@2	2.20/0.78	0.42/0.85	120	1350	447	0.8μm CMOS
Fan [13]	>100	4.6	0.38@2	3.28/1.31	0.53/0.4	120	1453	725	0.5μm CMOS
Fan [13]	>100	9	0.41@2	4.8/2.0	0.58/0.43	120	2634	995	0.5μm CMOS
This work NAFFC	>100	18.9	0.239@1.2	2.74/1.34	1.18/0.79	100	7908	854	0.18μm CMOS

Chapter 4

A Self-Biased CMOS Voltage Reference Based on Weak Inversion Operation

4.1 INTRODUCTION

As the technology scales down, the channel length reduces a lot. This causes that the channel-length modulation effect has a huge impact on CMOS transistors. For the precise and stable voltage reference circuit, the output voltage must be insensitive to the supply voltage and temperature variation. But shorter channel length is, the much output voltage variation will be. However, using the self-biased circuit structure compensates the drain current increasing as supply voltage to reduce this effect. Leading to a reference voltage independent of supple voltage, temperature and process fluctuation.

The following section briefly describes two formulas to qualify the dependence on power supply and temperature. In Section 4.3, the general principle of the bandgap voltage reference is presented to show how to design a reference voltage independent of temperature variation. Section 4.4 discusses the subthreshold characteristics of MOSFET. The new voltage reference circuit structure is shown in Section 4.5. Section 4.6 addresses the simulation and experimental results.

4.2 SENSITIVITY FORMULAS

First of all, we have to qualify the dependence on power supply and temperature [23]. That will let us know the performances of the voltage reference circuits. The concepts of sensitivity and fractional temperature coefficient are presented. V_{REF} stands for the reference voltage and supply voltage is designated as V_{DD}. The

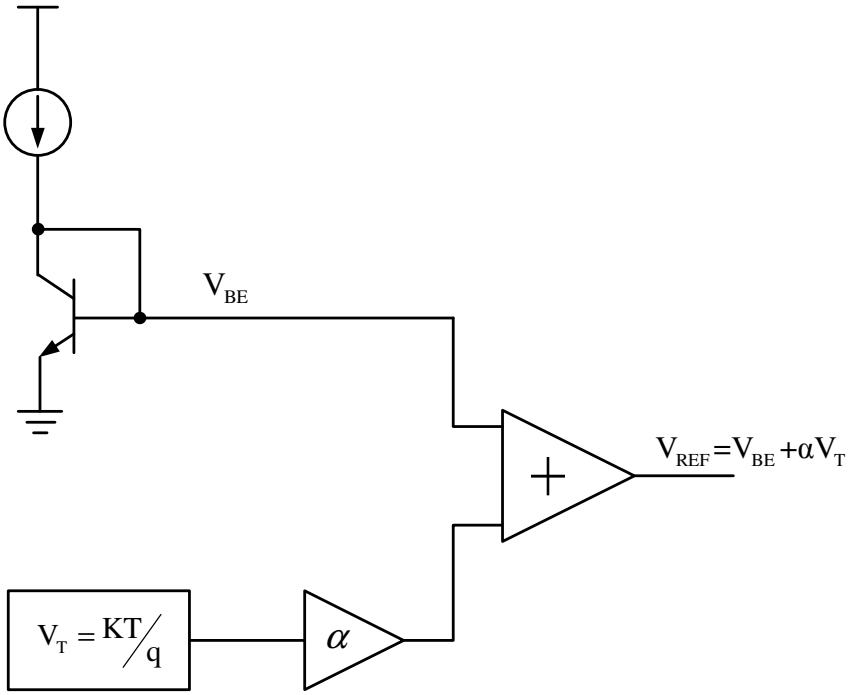


Figure 4-1 General principles of bandgap voltage reference.

sensitivity of V_{REF} versus V_{DD} changing can be written as

$$ST_{V_{DD}}^{V_{REF}} = \lim_{\Delta V_{DD}\to 0} \frac{\Delta V_{REF}/V_{REF}}{\Delta V_{DD}/V_{DD}} = \frac{V_{DD}}{V_{REF}} \frac{\partial V_{REF}}{\partial V_{DD}}. \tag{4-1}$$

From (4-1), for an ideal voltage reference, it is independent of supple voltage. So the term $\partial V_{REF}/\partial V_{DD}$ is equal to zero leading to zero sensitivity. But generally speaking, the practical value of sensitivity is smaller than $1/100$ for voltage reference circuits.

Fractional temperature coefficient (TC_F) is represented for circuits that are dependent of the temperature. It is defined as

$$TC_F(V_{REF}) = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T}. \tag{4-2}$$

As a rule, the fractional temperature coefficient is expressed by ppm/℃. For a stable reference voltage, the TC_F must be less than 50 ppm/℃.

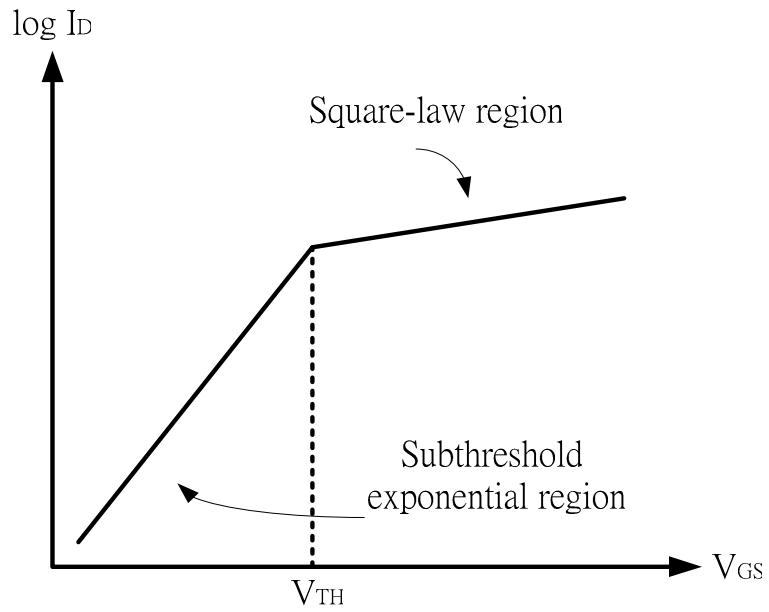


Figure 4-2 MOS subthreshold characteristics. [23]

4.3 GENERAL PRINCIPLES OF BANDGAP VOLTAGE REFERENCE

In order to obtain the reference voltage independent of the temperature variation, using opposite temperature coefficients make up for each other. The general principles are shown in Figure 4-1. The pn-junction diode generates the voltage V_{BE} and at room temperature $\partial V_{BE}/\partial T \approx -1.5$ mV/°K. V_t is the thermal voltage and equal to kT/q whereas $\partial V_t/\partial T \approx +0.087$ mV/°K [23] [24]. By setting the appropriate parameter α, the reference voltage with zero-temperature coefficient can be generated.

4.4 SUBTHRESHOLD CHARACTERISTICS OF MOSFET

Subthreshold region is also known as weak-inversion region. It's for gate-source voltages less than the threshold voltage but high enough to create a depletion region at the silicon surface. The majority of transistors operating in subthreshold region are for low-power applications. First of all, we discuss the relations between the drain current and gate-source voltage in subthreshold region. When $V_{GS} < V_{TH}$, the drain current I_D is quite small and exhibits an exponential dependence on V_{GS}. Figure 4-2 shows the

characteristics and this effect can be formulated for V_{DS} greater than roughly 200 mV as [23] [24]

$$I_D = I_0 \exp \frac{V_{GS}}{\varsigma V_t}, \tag{4-3}$$

where $\varsigma > 1$ is a non-ideal factor and $V_t = KT/q$.

If the MOSFET is in subthreshold region, the relation between V_{GS} and V_{TH} as a function of temperature is [21]

$$V_{GS}(T) = V_{TH}(T) + V_{OFF} + \frac{n(T)}{n(T_0)} \times [V_{GS}(T_0) - V_{TH}(T_0) - V_{OFF}] \frac{T}{T_0}, \tag{4-4}$$

where, $n(T) = 1 + C_d / C_{ox}$ is the subthreshold slope factor and V_{OFF} is a corrective constant term used in BSIM3v3 models. By assuming $n(T)$ only varied slightly with temperature, which means $n(T) \approx n(T_0)$, the threshold voltage can be modeled as $V_{TH}(T) = V_{TH}(T_0) + K_T(T/T_0 - 1)$, where $K_T < 0$. Therefore, V_{GS} can be approximated as

$$V_{GS}(T) \approx V_{GS}(T_0) + K_G\left(\frac{T}{T_0} - 1\right), \tag{4-5}$$

where $K_G \cong K_T + V_{GS}(T_0) - V_{TH}(T_0) - V_{OFF}$. The quantity K_G is negative, so V_{GS} is decreased with the temperature.

4.5 SELF-BIASED VOLTAGE REFERENCE CIRCUIT

The proposed MOSFET-only voltage reference circuit is shown in Figure 4-3. It can be divided into two parts. One is self-biased circuit composing of transistors M1~M4 and resistor R_1. The other is formed by transistors M6~M8 and resistors R_2 and R_3 generating the reference voltage V_{REF}.

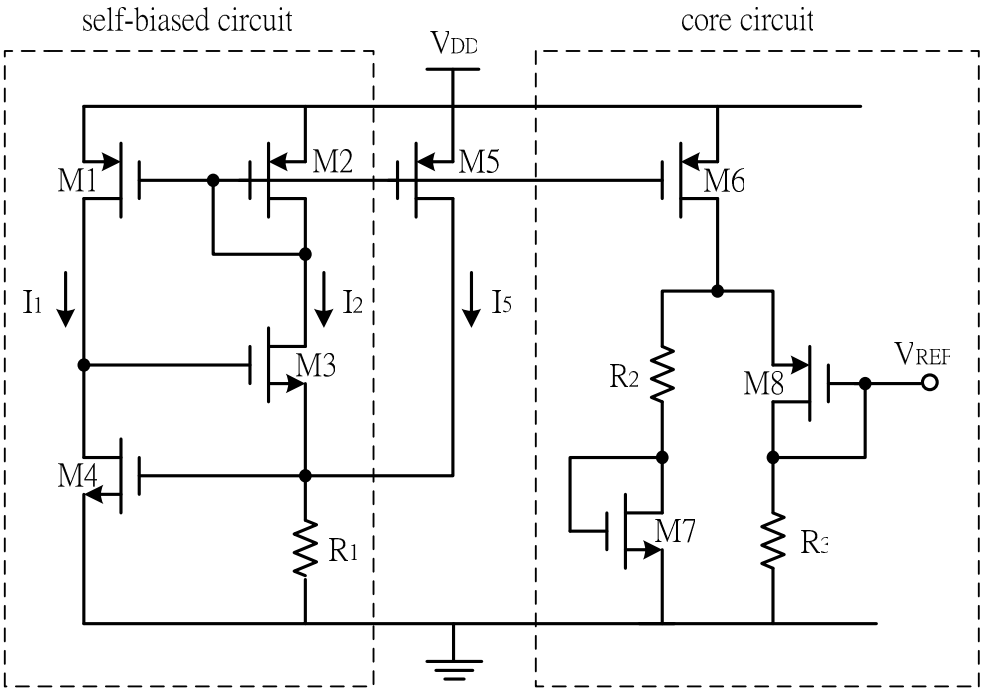


Figure 4-3 The structure of the self-biased CMOS voltage reference.

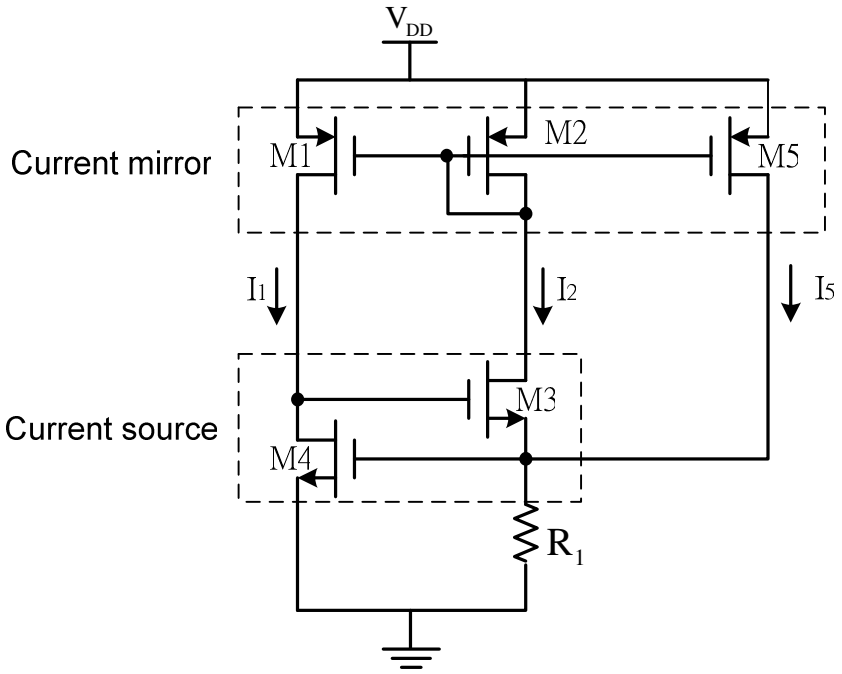


Figure 4-4 Schematic of a self-biased reference.

4.5.1 Self-biased circuit

Figure 4-4 shows the operation of the self-biased circuit [23]. It should be noted that transistor M4 is operated in the subthreshold region. So the current I_1 has an exponential relation to the gate-source voltage V_{GS4} which is produced by

$(I_2 + I_5) \times R_1$. From the standpoint of current mirror block, the current I_1 is proportional to $I_2 + I_5$. The operating point, which is shown in Figure 4-5, is at the intersection of the two characteristics in order to satisfy these two constraints.

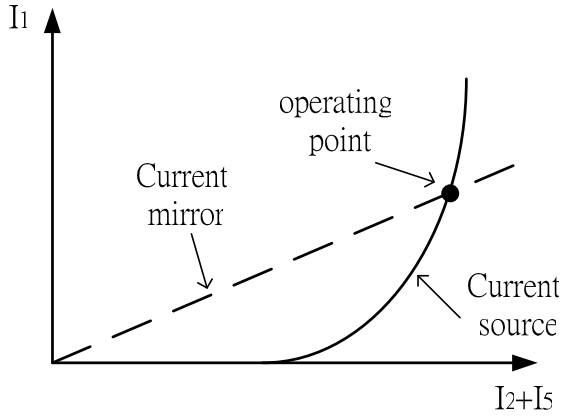


Figure 4-5 Definition of the operating point.

4.5.2 Compensation of channel-length modulation effect

Because the transistor M4 is operated in the subthreshold region, from Section 4.4, we know the relation between I_1 and V_{GS4} are given by

$$I_1 = I_0 \exp \frac{V_{GS4}}{\varsigma V_t}. \tag{4-6}$$

The equation (4-6) also can be expressed as

$$V_{GS4} = \varsigma V_t \ln \frac{I_1}{I_0}. \tag{4-7}$$

From (4-7), we derive V_{GS4} versus supply voltage change

$$\frac{\partial V_{GS4}}{\partial V_{DD}} = \frac{\varsigma V_t}{I_1} \frac{\partial I_1}{\partial V_{DD}}. \tag{4-8}$$

Finally, the current flowing through resistor R_1 is obtained by

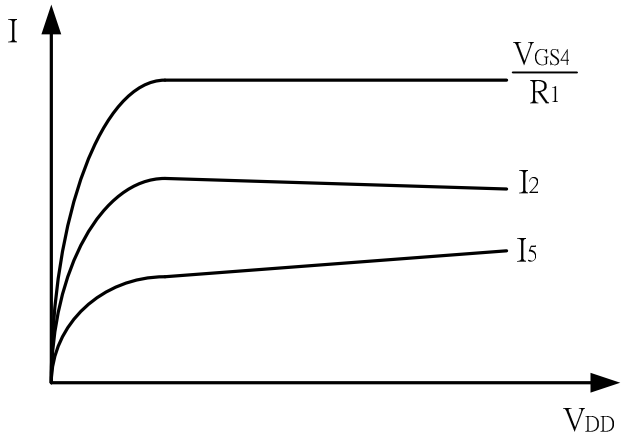


Figure 4-6 Determination of channel-length modulation reduction.

$$\frac{\partial\left(V_{GS4}/R_1\right)}{\partial V_{DD}}=\frac{\varsigma V_t}{I_1 R_1}\frac{\partial I_1}{\partial V_{DD}}. \tag{4-9}$$

If the resistance of R_1 is large, the current V_{GS4}/R_1 is almost independent of supply voltage variation. From simulated parameters, $\partial\left(V_{GS4}/R_1\right)/\partial V_{DD}\approx 0.065\,\partial I_1/\partial V_{DD}$ means this current V_{GS4}/R_1 is insensitive to channel-length modulation effect.

The current flows through R_1 is equal to

$$\frac{V_{GS4}}{R_1}=I_2+I_5. \tag{4-10}$$

Due to design the short length of transistor M5, the current I_5 has a significant channel-length modulation effect. It can be expressed by $I_5=I_5(0)+I_5(\Delta V_{DD})$ where $I_5(0)$ presents the current independent of supply voltage and $I_5(\Delta V_{DD})$ stands for the current increasing as supply voltage. But V_{GS4}/R_1 is stable even when supply voltage changes a lot, then we can obtain the equation $\partial\left(V_{GS4}/R_1\right)/\partial V_{DD}\approx 0$. As a result, the current I_2 must be decreasing as I_5 increasing like equation (4-11). The trend of these two currents is presented in Figure 4-6.

$$\frac{\partial I_2}{\partial V_{DD}}=\frac{\partial V_{GS4}/R_1}{\partial V_{DD}}-\frac{\partial I_5(0)}{\partial V_{DD}}-\frac{\partial I_5(\Delta V_{DD})}{\partial V_{DD}}\approx-\frac{\partial I_5(\Delta V_{DD})}{\partial V_{DD}}. \tag{4-11}$$

4.5.3 Output reference voltage

For simplification, equation (4-10) is modified by

$$\frac{V_{GS4}}{R_1} = I_2 + I_5 = I_2\left(1+\frac{S_5}{S_2}\right), \tag{4-12}$$

where $S=(W/L)$ and we also assume $K=(1+S_5/S_2)^{-1}$. So it can be obtained by

$$I_2 = K\left(V_{GS4}/R_1\right). \tag{4-13}$$

Moreover, the transistor size of M2 and M6 are the same. So the reference voltage is expressed as

$$V_{REF} = \alpha I_2 R_2 + V_{GS7} - |V_{GS8}|, \tag{4-14}$$

where the quantity α represents the percentage of the current flowing through the resistor R_2.

From the standpoint of resistor R_3, the reference voltage is expressed as

$$V_{REF} = (1-\alpha) I_2 R_3 \Rightarrow \alpha = 1 - \frac{V_{REF}}{I_2 R_3}. \tag{4-15}$$

By substituting equation (4-15) into (4-14), we have

$$V_{REF} = I_2 R_2 - \frac{R_2}{R_3} V_{REF} + V_{GS7} - |V_{GS8}|$$

$$\Rightarrow V_{REF} = \left(\frac{1}{1+\frac{R_2}{R_3}}\right)\left(K\frac{R_2}{R_1}V_{GS4} + V_{GS7} - |V_{GS8}|\right). \tag{4-16}$$

From above equation, we know the reference voltage is independent of supply voltage

and process variation. However, note that the transistors M4, M7 and M8 are operated in subthreshold region. They all contain the negative temperature coefficients. The derivative with respect to temperature is

$$\frac{\partial V_{REF}}{\partial T} = \frac{1}{T_0\left(1+R_2/R_3\right)}\left(K_{G4}K\frac{R_2}{R_1}+K_{G7}-K_{G8}\right). \tag{4-17}$$

In order to obtain the reference voltage with zero-temperature coefficient, equation (4-17) must be set to zero by choosing the appropriate parameter $K\,R_2/R_1$.

$$K\frac{R_2}{R_1} = \frac{K_{G8}-K_{G7}}{K_{G4}}. \tag{4-18}$$

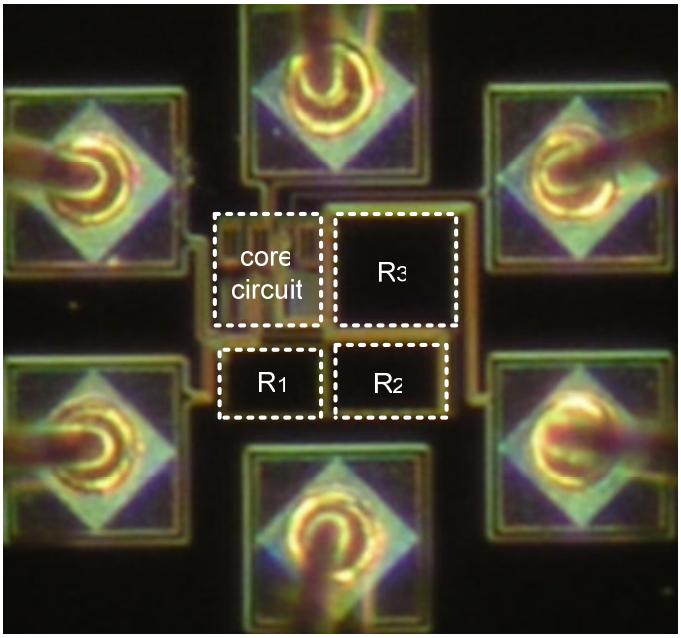


Figure 4-7 Chip photo.

4.6 EXPERIMENTAL RESULTS

The proposed circuit was fabricated by TSMC 0.35μm technology. The chip, whose photo is shown in Figure 4-7, occupies a silicon area of about 0.018 mm^2. The start-up time of voltage reference circuit is shown in Figure 4-8 and nominal reference voltage is 400.3 mV at room temperature. Figure 4-9 shows the steady–state reference

voltage.

Because the proposed voltage reference circuit improves the channel-length modulation effect, the output voltage variation is about 7 mV when supply voltage is changing from 1.5 to 4.0 V. Figure 4-10 shows the reference voltage with and without compensation. The black line comes from the experimental result. The red line stands for the transistor M5 isn't exist and the output voltage variation is 49 mV. A plot of the reference voltage versus supply voltage changing from 0 V to 4 V is shown in Figure 4-11. The minimum supply voltage is 1.3 V and supply current is 7.6 μA. The mean temperature coefficient is 72.4 ppm/ ℃ in the temperature range of -20 ℃ to 80 ℃. The reference voltage versus temperature variation is shown in Figure 4-12.

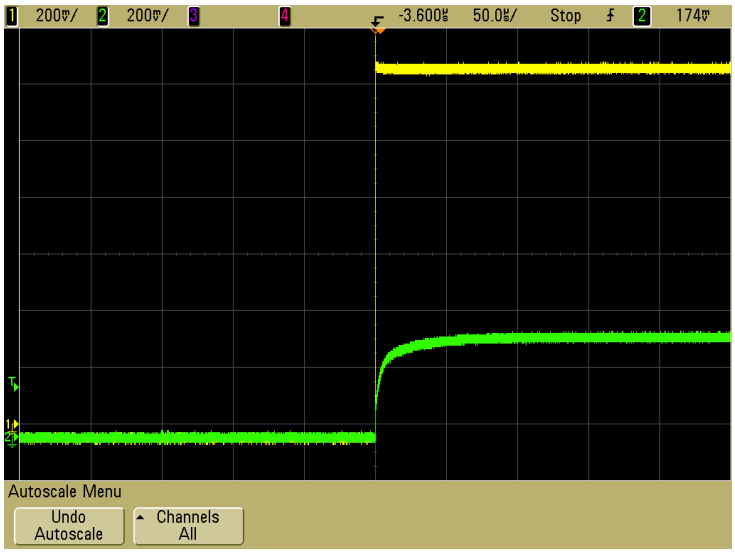


Figure 4-8 Start-up time of voltage reference circuit.

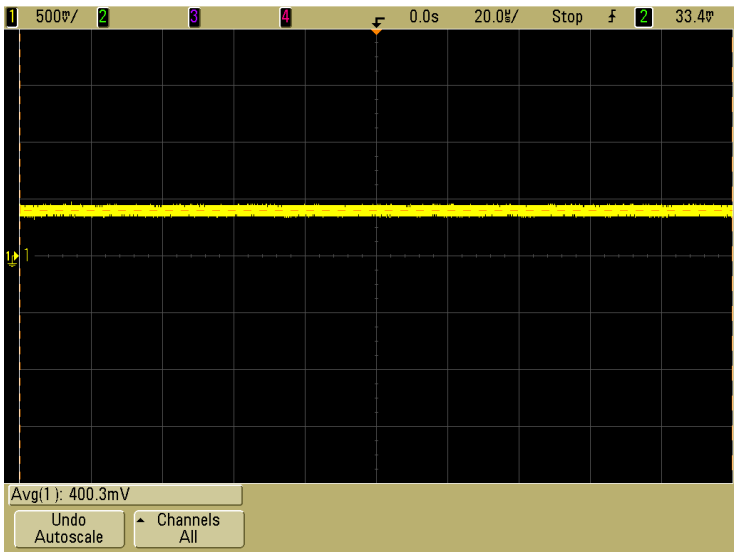


Figure 4-9 The steady-state reference voltage.

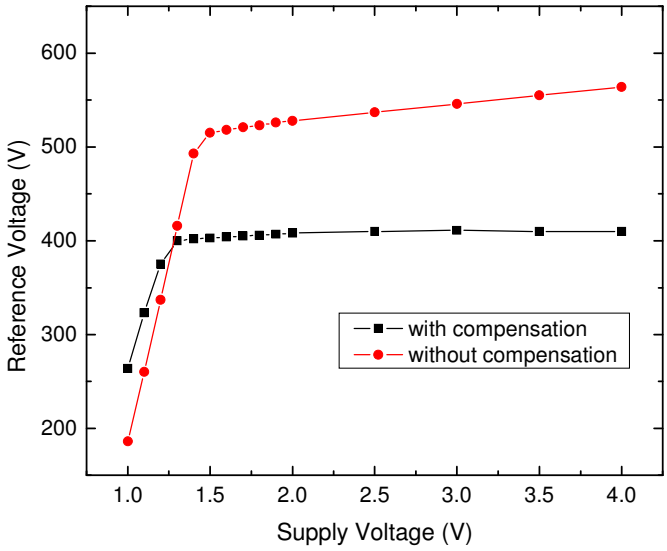


Figure 4-10 Comparison of reference voltage with and without compensation of channel-length modulation effect.

Figure 4-11 Experimental reference voltage versus supply voltage at room temperature.

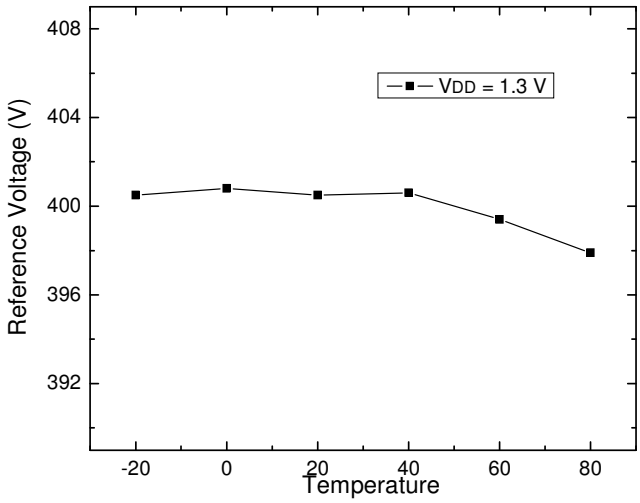


Figure 4-12 Experimental reference voltage versus temperature for V_{DD} = 1.3 V.

TABLE 4-1
PERFORMANCE SUMMARY

Supply voltage	1.3 V to 4.0 V
Supply current	7.6 μA
Reference voltage	400.3 mV
Temperature coefficient (-20 to 80 ℃)	± 1.45 mV 72.4 ppm/ ℃ (mean)
Sensitivity to supply voltage (1.3 to 4 V)	10 mVp-p
Start-up time (V_{DD} = 0 ~ 1.3 V)	4.9 μs
Chip area in 0.35-μm CMOS technology	0.01813 mm^2

Chapter 5

A Low-Dropout Regulator with Negative Active-Feedback Frequency Compensation

5.1 INTRODUCTION

The LDO regulator with negative active-feedback frequency compensation (NAFFC) is presented in this chapter. In order to assure the stability of the system, one compensated capacitor is used. It forms a negative active-feedback path to generate a LHP zero and to solve the unstable issue caused by the large parasitic capacitor of power PMOS. The zero can compensate the frequency response to obtain better phase margin. Section 5.2 shows the brief review of LDO regulators. The proposed circuit is presented in Section 5.3. The circuit descriptions are introduced in Section 5.4. Section 5.5 shows the simulation results.

5.2 BRIEF REVIEW OF LDO REGULATORS

Figure 5-1 illustrates the topology of conventional LDO regulator. It is composed of a power PMOS transistor, an error amplifier and feedback resistors. Moreover, the voltage reference circuit is needed to provide a stable input voltage for the error amplifier. The open-loop system includes at least two low-frequency poles and one zero which are approximated as [26] [28] [29]:

$$\omega_{p1} \approx \frac{1}{r_{dsp} C_{OUT}} \tag{5-1}$$

$$\omega_{p2} \approx \frac{1}{R_{oa} C_{PT}} \tag{5-2}$$

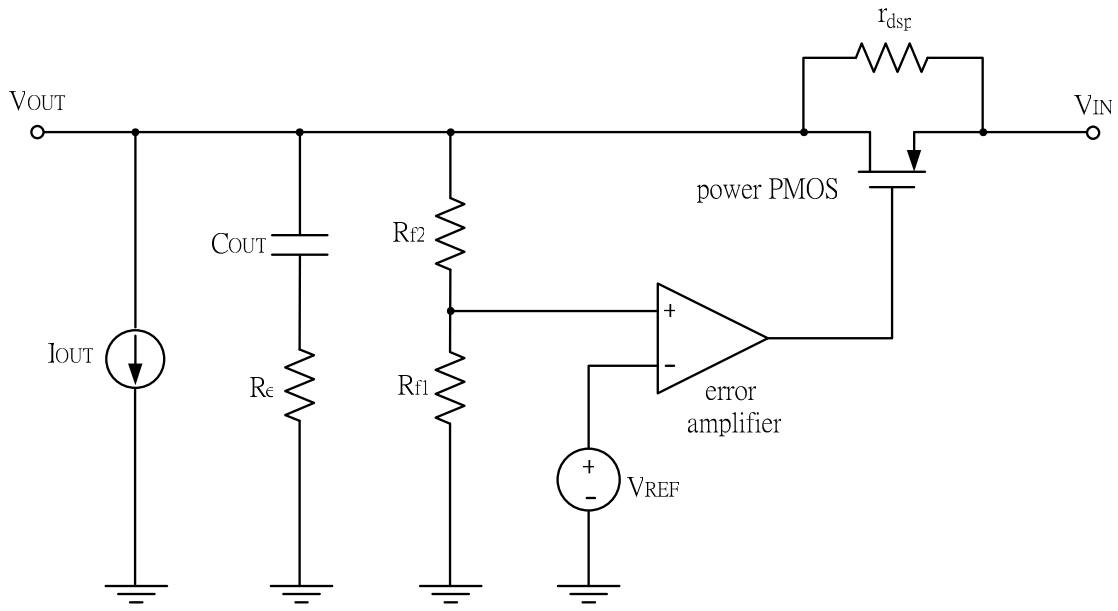


Figure 5-1 Topology of conventional LDO regulator.

$$\omega_{z1} \approx \frac{1}{R_e C_{OUT}} \tag{5-3}$$

, where r_{dsp} is the resistance of power PMOS transistor. R_{oa} and C_{PT} are the output resistance and capacitance of the error amplifier. Due to high impedance of the error amplifier and the large size of power PMOS transistor, the pole ω_{p2} is located at low frequency. The third pole could be introduced by output parasitic or the internal nodes of the error amplifier capacitance. This results in a potentially unstable system of LDO regulator. Besides that, the variable factors of the load, including output current and equivalent series resistance (ESR), makes frequency compensation become a difficult issue.

5.3 THE PROPOSED LDO REGULATORS

In order to make certain the LDO regulator stable, we presented the negative active-feedback frequency compensation (NAFFC) technique. Topology of proposed regulator is shown in Figure 5-2. The error amplifier, high swing stage and power PMOS transistor can be viewed as a three-stage amplifier and the capacitor C_m provides not only the pole-splitting compensation but also the feedback path to create

a LHP zero. The main compensated operations should be divided into two parts which are discussed in the following.

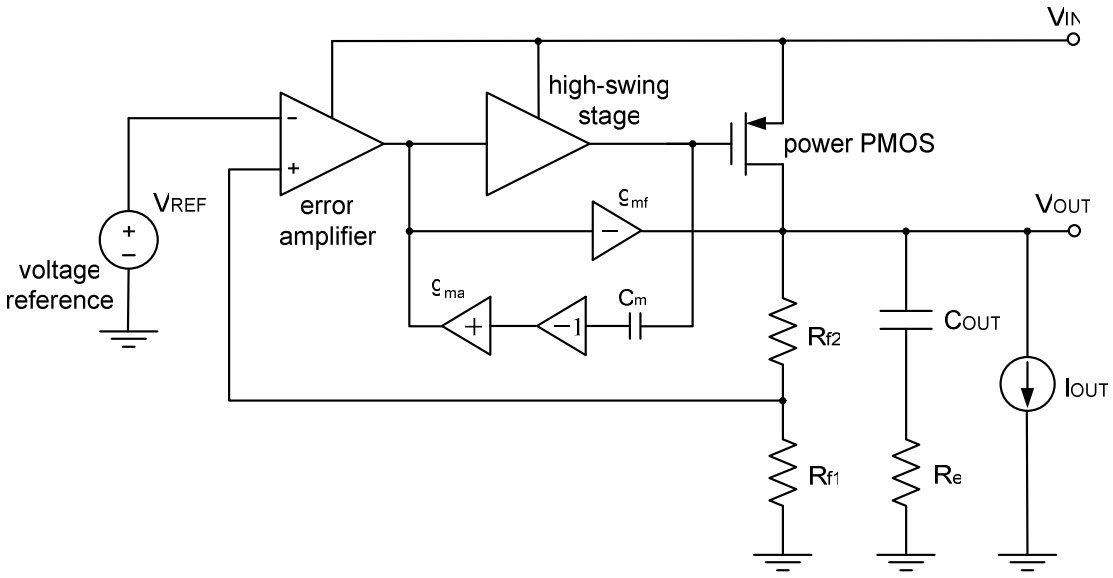


Figure 5-2 Topology of proposed LDO regulator.

5.3.1 **Without off-chip capacitor and ESR**

When off-chip capacitor is moved out, there is still a parasitic capacitor (C_{PAR}) in the output of LDO regulator. The open-loop transfer function is derived as follows:

$$H(s)=\frac{A_0\left(1+s\left(\frac{C_m}{g_{ma}}+\frac{(C_2+C_m)\,g_{mf}}{g_{m2}g_{m\mathrm{PT}}}\right)\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+s\frac{C_1}{g_{m2}}+s^2\frac{C_1C_2}{g_{ma}g_{m2}}\right)}. \tag{5-4}$$

, where A_0 is the dc open-loop gain which is defined in (5-5)

$$A_0=\left(\frac{R_{f1}}{R_{f1}+R_{f2}}\right)g_{m1}g_{m2}g_{m\mathrm{PT}}R_{o1}R_{o2}\left(r_{dsp}\left\|\left(R_{f1}+R_{f2}\right)\right.\right). \tag{5-5}$$

The transconductance g_{m1}, g_{m2}, $g_{m\mathrm{PT}}$ and the output resistance R_{o1}, R_{o2}, r_{dsp} are

provided by error amplifier, high swing stage and power PMOS individually.

From the transfer function (5-4), there are two poles, one complex pole and one zero in the system which are given by

$$\omega_{p1} = \frac{1}{g_{m2} R_{o2} R_{o1} C_m} \tag{5-6}$$

$$\omega_{p2} = \frac{1}{\left(r_{dsp} \left\| \left(R_{f1} + R_{f2} \right) \right. \right) C_{PAR}} \tag{5-7}$$

$$\omega_{p3,4} = \sqrt{\frac{g_{ma} g_{m2}}{C_1 C_2}} \tag{5-8}$$

$$\omega_z = \frac{1}{C_m \left(\frac{1}{g_{ma}} + \frac{\left(1 + C_2 / C_m\right) g_{mf}}{g_{m2} g_{m\mathrm{PT}}} \right)}. \tag{5-9}$$

In order to obtain the maximum flat response, the damping factor (ς) of the second-order function should be set to $1/\sqrt{2}$.

$$\varsigma = \frac{1}{2} \sqrt{\frac{g_{ma} C_1}{g_{m2} C_2}} = \frac{1}{\sqrt{2}} \Rightarrow g_{ma} = 2 g_{m2} \frac{C_2}{C_1} \tag{5-10}$$

, where C_1 and C_2 are the parasitic capacitors in the output of error amplifier and high-swing stage.

Two extreme cases are discussed as follows. When output load current equals to zero, r_{dsp} is maximized and $g_{m\mathrm{PT}}$ is minimized. From (5-7) and (5-9), ω_{p2} and ω_z are located at low frequency and $\omega_{p2} < \omega_z$. In addition, $\omega_{p3,4}$ is located at high frequency due to small parasitic capacitor C_1. The frequency response is shown in Figure 5-3 where solid line illustrates the phase margin is better than $60°$.

When output load current increases a lot, r_{dsp} decreases and $g_{m\mathrm{PT}}$ increases significantly. The open-loop transfer function in the case of $I_{OUT} \neq 0$ is approximated by

$$H(s) \approx \frac{A_0}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+s\frac{C_1}{g_{m2}}+s^2\frac{C_1C_2}{g_{ma}g_{m2}}\right)} \tag{5-11}$$

, where ω_{p2} and ω_z are moved to the high frequency. Because of $\omega_{p3,4} >> \omega_{p1}$, we still obtain the phase margin is larger than $60°$.

5.3.2 **With off-chip capacitor and ESR**

The LDO regulator with off-chip capacitor is also stable. The open-loop transfer function is expressed as

$$H(s) \approx \frac{A_0\left(1+\frac{s}{\omega_{ze}}\right)\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+s\frac{C_1}{g_{m2}}+s^2\frac{C_1C_2}{g_{ma}g_{m2}}\right)} \tag{5-12}$$

, where $\omega_{p3,4}$ and ω_z are defined in (5-8) and (5-9), and ω_{p1}, ω_{p2}, ω_{ze} are given by

$$\omega_{p1} = \frac{1}{\left(r_{dsp} \left\| \left(R_{f1}+R_{f2}\right)\right.\right) C_{OUT}} \tag{5-13}$$

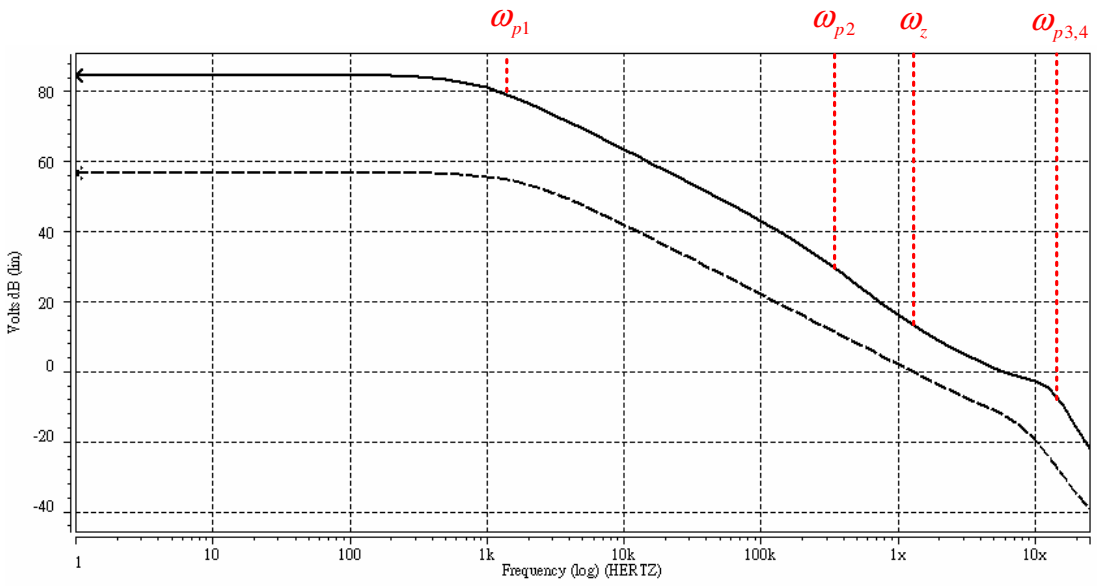
$$\omega_{p2} = \frac{1}{g_{m2}R_{o2}R_{o1}C_m} \tag{5-14}$$

$$\omega_{ze} = \frac{1}{R_e C_{OUT}} \tag{5-15}$$

When $I_{OUT} = 0$, r_{dsp} is maximized and C_{OUT} is large leading to ω_{p1} close to zero frequency. ω_{p2} is generated by the compensated capacitor. Although the system exists four poles, it is still stable by means of two LHP zeros to provide enough phase margin.

When $I_{OUT} \neq 0$, ω_{p1} and ω_z approach the higher frequency. ω_{ze} without a

shift makes the system stable.



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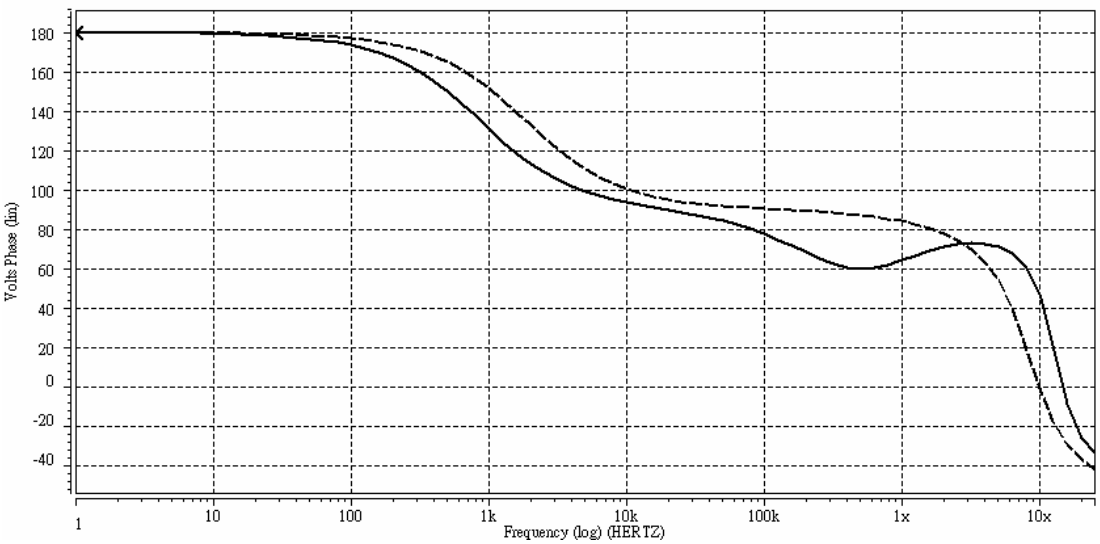
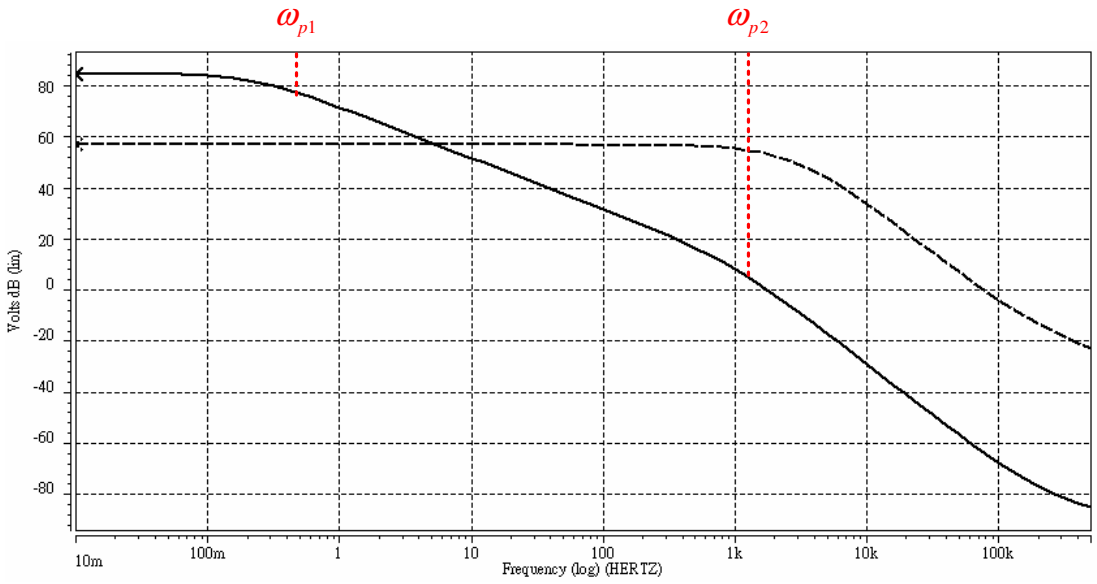
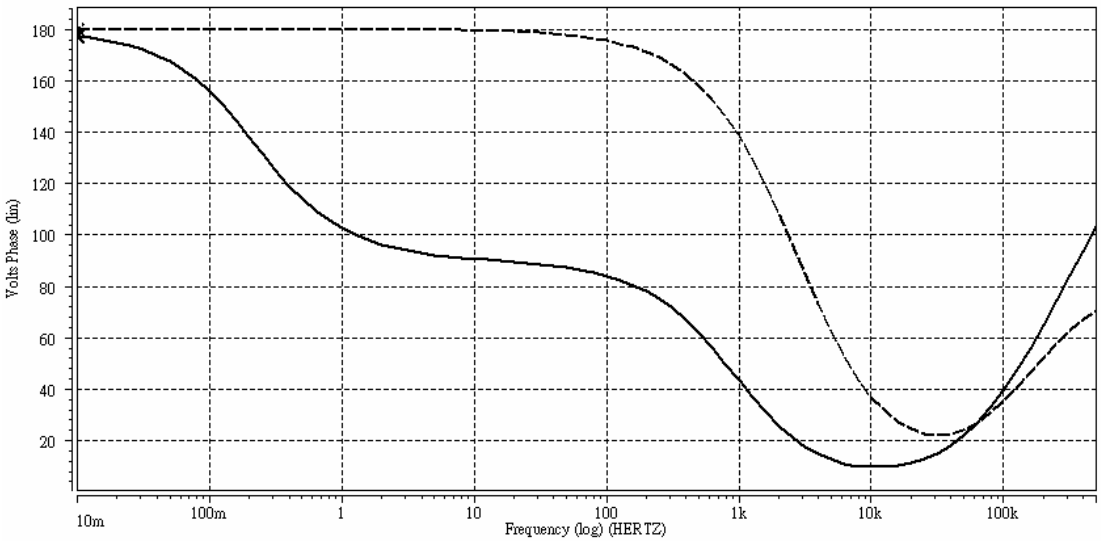


(b)

Figure 5-3 Open-loop gain of LDO regulator without COUT and ESR (a) Magnitude response (b) Phase response. The load current is 0 (solid line) and 80 (dash line) mA.



(a)



(b)

Figure 5-4 Open-loop gain of LDO regulator with C_{OUT} = 10 μF and Re = 0.1Ω (a) Magnitude response (b) Phase response. The load current is 0 (solid line) and 80 (dash line) mA.

5.4 CIRCUIT DESCIPTIONS

The proposed circuit structure is shown in Figure 5-5. In this LDO regulator, it can be viewed as a three-stage amplifier. The first amplification stage is implemented by transistors M11-M18 with a PMOS input differential pair. The second non-inverting amplification stage and third stage are realized by transistors M21-M24 and MPT, respectively. The compensated capacitor C_m connects the high-swing output stage and source of transistor M15 which supply a negative active-feedback path. Transistor MMF can force the LHP zero (ω_z) closing to zero frequency. From (5-9), if MMF doesn't exist, ω_z is changed to $\omega_z' = 1/(C_m/g_{ma})$ which is located at higher frequency than ω_z. It is obvious to obtain the better phase margin if ω_z is closer to ω_{p2}.

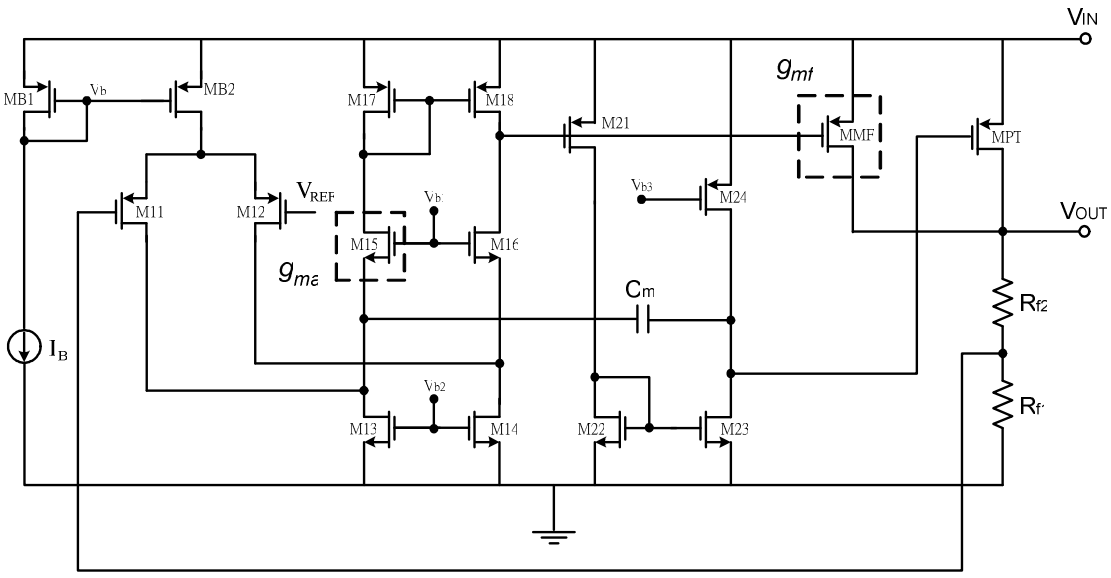


Figure 5-5 The schematic of proposed LDO regulator.

5.5 SIMULATION RESULTS

The chip photo of LDO regulator, implemented by TSMC 0.35 μm technology, is shown in Figure 5-6, and the chip area is occupied by 365 μm × 290 μm. The internal circuit only needs one compensated capacitor C_m=2 pF and it operates in V_{IN} = 1.5 V and consumes 65-μA ground current. The dropout voltage is varied as different load current changed from 0 mA to 100 mA. Figure 5-7 shows the dropout voltage is about 250 mV when load current is lower than 80 mA.

The load transient response for load pulsed currents of 0 mA and 80 mA has been simulated. Two cases without and with off-chip capacitor are taken into consideration. Figure 5-8 and Figure 5-9 show the load transient response, respectively. Moreover, from the simulation results, the larger resistance of ESR is, the faster response time can be achieved. As ESR becomes larger, undershoot and overshoot is increasing at the same time. The influences of ESR are shown in Figure 5-10. Output ripples are 12.5 mVp-p and 2.4 mVp-p produced by supply spikes equaling to 100 mV which shows in Figure 5-11.

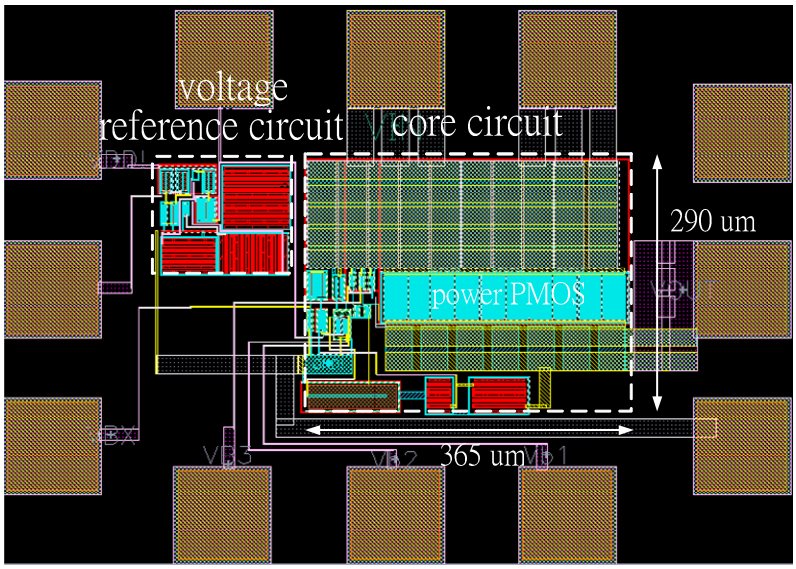


Figure 5-6 Chip photo.

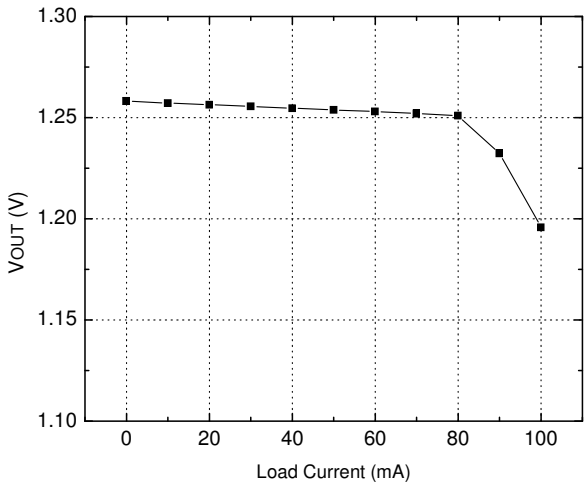


Figure 5-7 Output voltage of LDO regulator vs. load current.

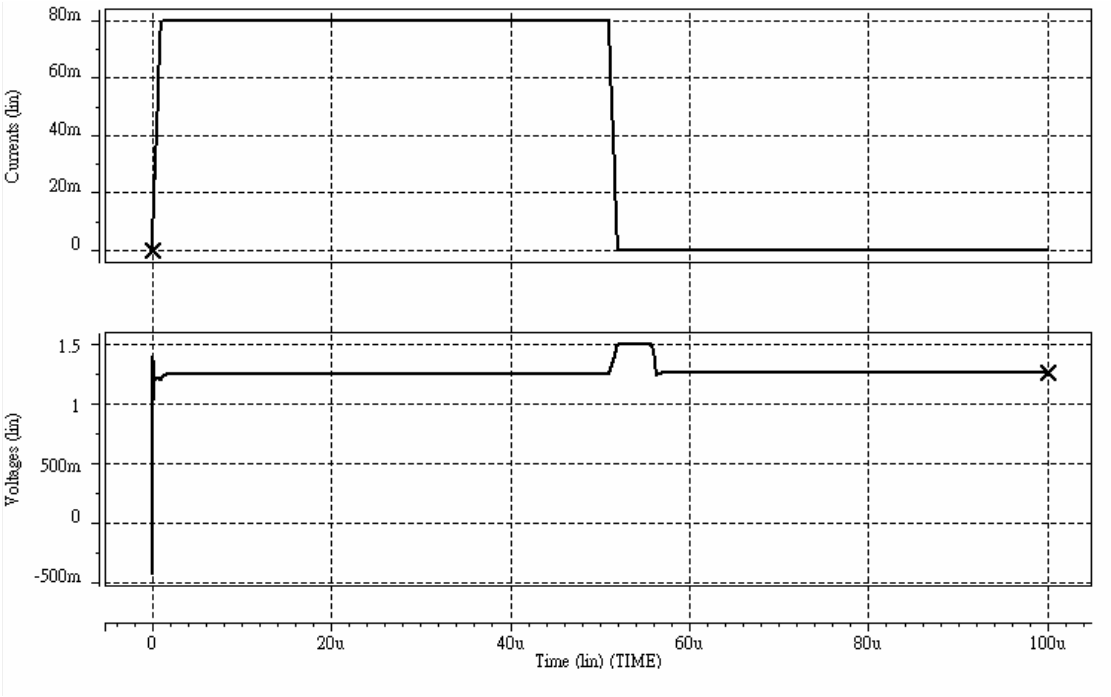


Figure 5-8 Load transient response without off-chip capacitor as load current is varied from 0 to 80 mA.

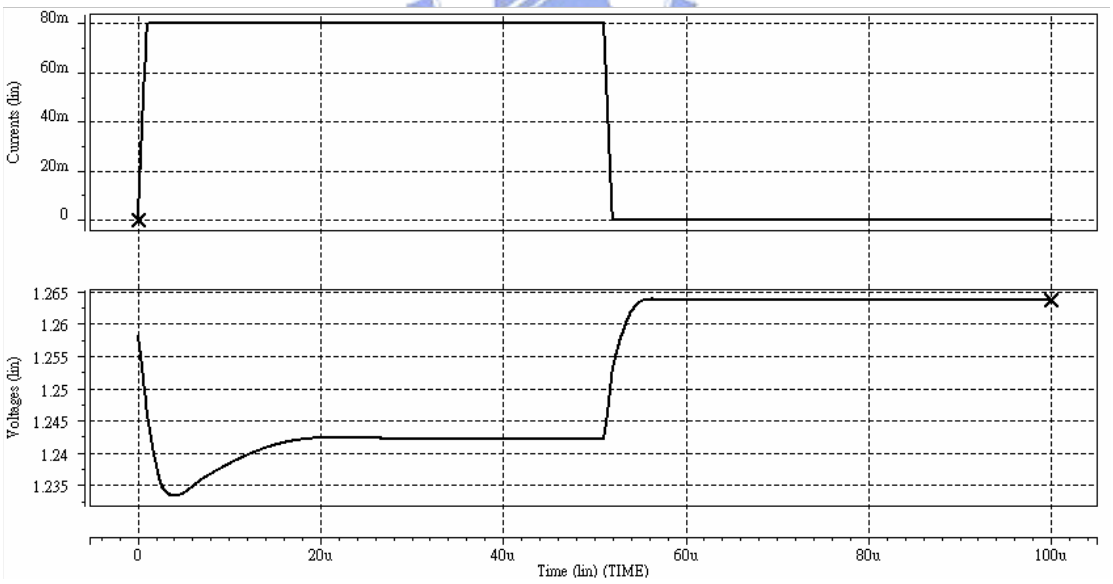
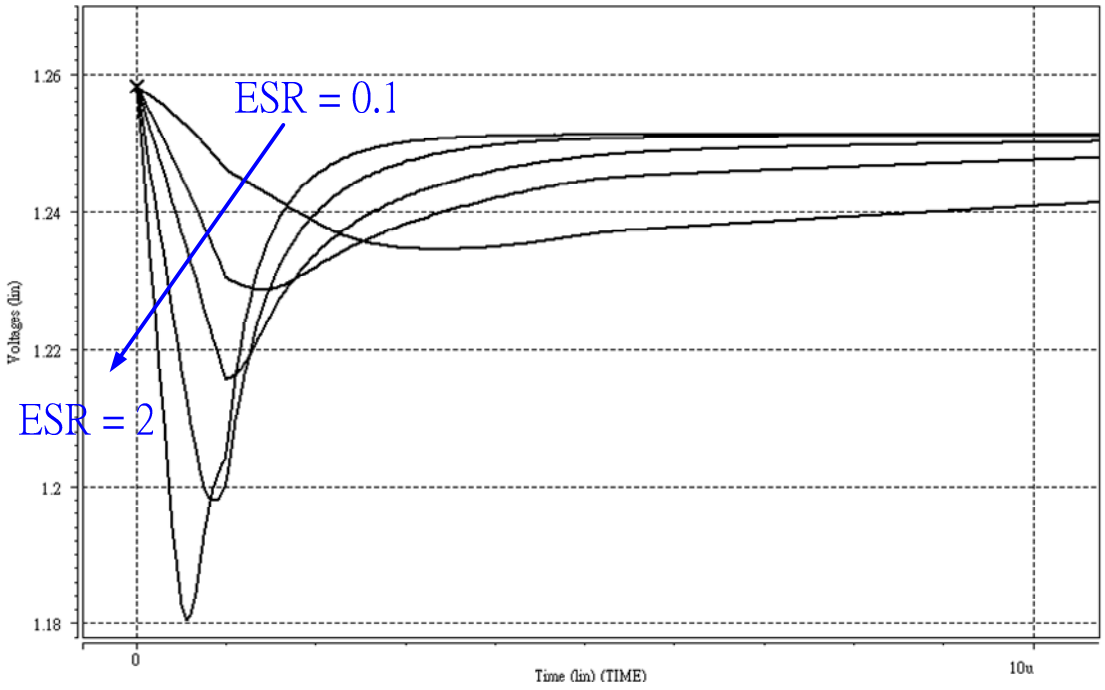


Figure 5-9 Load transient response with C_{OUT} = 10 μF and ESR = 0.1Ω as load current is varied from 0 to 80 mA.



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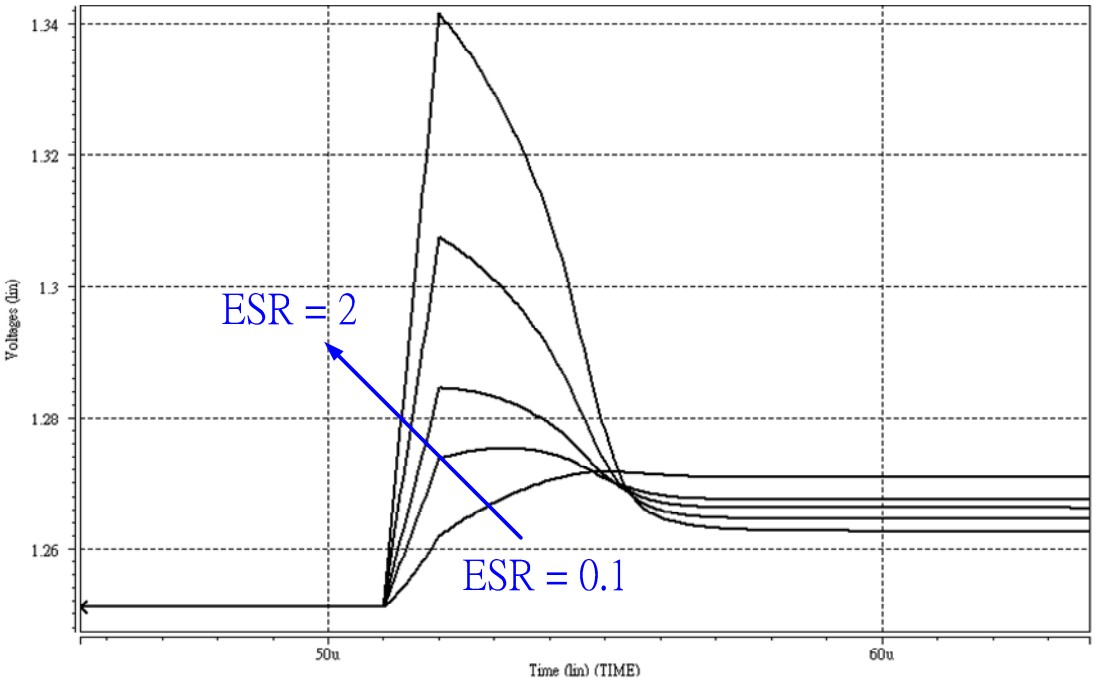
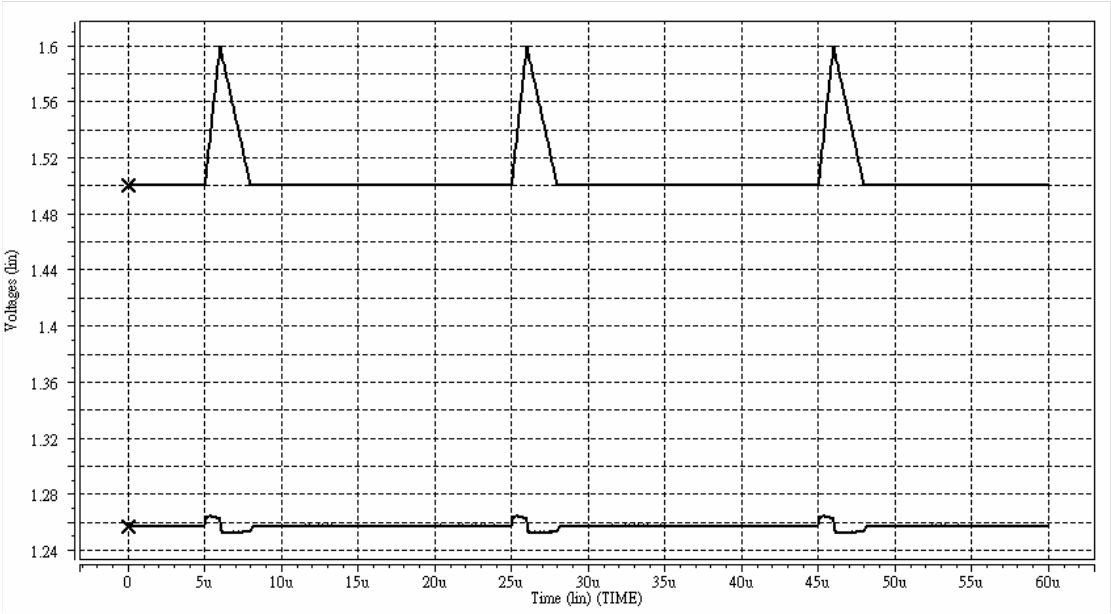
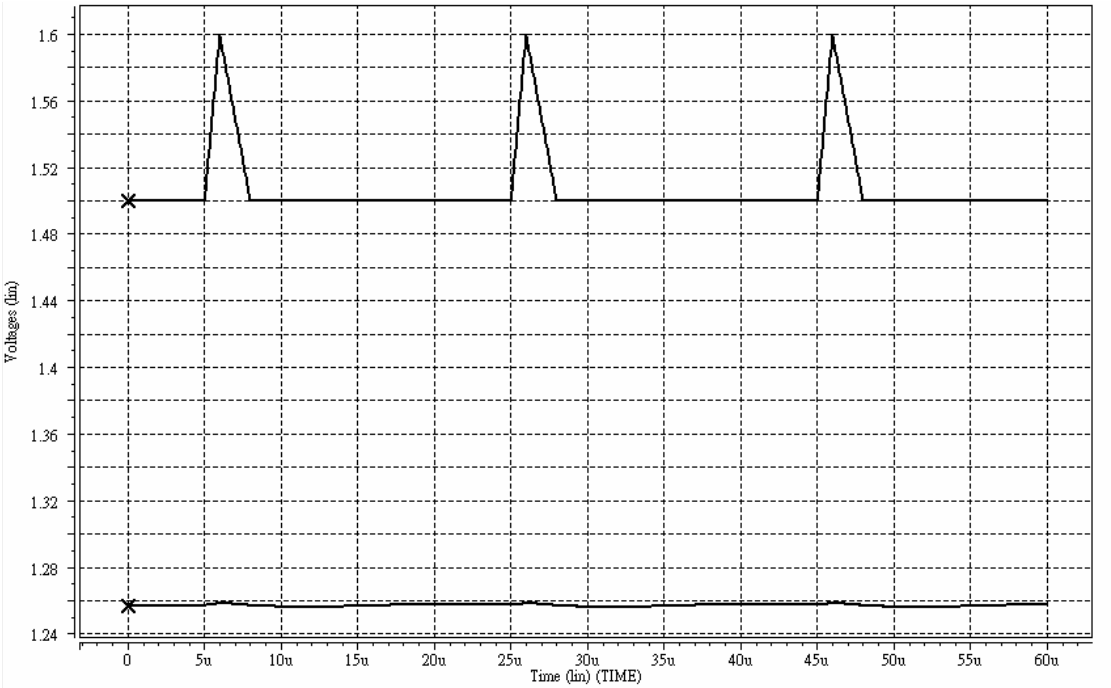


(b)

Figure 5-10 Load transient response with C_{OUT} = 10 μF as output current is varied from 0 to 80 mA. For the ESR, the resistance Re is 0.1, 0.3, 0.5, 1 and 2 Ω.



(a)



(b)

Figure 5-11 Power-supply rejection of the regulator for 10-mA load current (a) without off-chip capacitor (b) with C_{OUT} = 10 μF and Re = 0.1Ω.

Chapter 6

Conclusions

A current-reuse technique for nested Miller compensation amplifier is introduced in Chapter2. It can achieve the low-power design with power consumption reduced to half from the traditional nested Miller compensation amplifier. From the derivation of NMC amplifier, there is a tradeoff between the required compensation capacitance and output-stage sinking current. The CRNMC amplifier can have smaller compensation capacitance and also keep low power dissipation at the same time, so is more suitable for low power, mobile applications. All the simulation results and performance parameters are proved by post-layout simulations using a 0.35-μm CMOS process. The experimental performance and derivation are matched well.

Chapter 3 presents the negative active-feedback frequency compensation (NAFFC) technique. Avoiding the capacitive feedback paths at the output and using the pole-zero cancellation approach improve the gain-bandwidth product obviously. The high slew rate and short settling time of the NAFFC amplifier characteristics make the amplifier suitable for data conversion and switched-capacitor circuits. The experimental results show good frequency and transient responses. Comparison with the other previously published compensation techniques are also presented in this chapter.

A MOSFET-only voltage reference circuit based on subthreshold characteristics has been introduced in Chapter 4. It exploits the self-biased circuit to reduce the channel-length modulation effect and weighted gate-source voltage to achieve nearly zero-PTAT reference voltage. A nominal output voltage is 400.3 mV under the lowest supply voltage = 1.3 V. Experimental results reported the reference voltage having 10-mV variation in the supply range of 1.3 V to 4 V. The temperature coefficient is 72.4 ppm in the range [-20 ℃, 80 ℃].

Chapter 5 presented a novel frequency compensation to assure the LDO regulator

stable. The regulator occupies 0.106 mm^2 of silicon area with 2-pF compensated capacitor and it is suitable for 1.5-1.25 V conversion

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