國 立 交 通 大 學

電信工程學系

碩 士 論 文

語音系統低功率低失真三角積分數位類比轉換器

Low Power Low Distortion Audio Delta-Sigma Digital-to-Analog Converter

研究生：楊 家 泰

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A Thesis

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摘要

近年來因為語音產品的蓬勃發展，如 MP3 隨聲聽等等，使得語音系統數位類比轉換器成為一個重要的目標。而對於用電池運作的語音系統有幾個問題是我們必須注意的。因為功率消耗會影響電池的壽命，所以必須把功率消耗設計的越小越好。另外，為了達到多媒體產品的品質需求，此數位類比轉換器必須達到約 16 位元的高解析度。

三角積分數位類比轉換器(Delta-Sigma D/A converter)是一種廣泛運用的技術，它能夠達到高解析度、降低數位電路部份的操作速度、能夠緩和頻帶外(out-of-band)濾波器的需求以及提高對時脈抖動(clock jitter)的免疫力。使用直接電壓轉換的切換式電容技術可以減少 kT/C 雜訊和元件不匹配的影響而不增加功率消耗，而資料加權平均的演算法可以抑制電容之間的不匹配所造成的非線性度。

在此研究中我們將介紹一個 15 等級量化、三階的三角積分數位類比轉換器，取樣頻率是 44.1 千赫茲，輸入訊號為 18 位元，因為超取樣比率為 64 倍，所以主要時脈操作在 2.8224 百萬赫茲，由晶片中心(CIC)提供的台積電(tsmc)標準 0.18 微米製程中實現。

Low Power Low Distortion Audio Delta-Sigma Digital-to-Analog Converter

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Abstract

Audio digital-to-analog converters (DAC) have played an important role recently with the rapid growth of the minidisc players and portable audio devices. There are some main issues for a battery-operated audio system. Power dissipation affects the battery life, so it must be as low as possible. A high resolution of about 16bits is required for the DAC to meet the quality of the media.

The delta-sigma D/A converters have been used extensively. It can achieve high resolution, reduce digital circuit speed, relax the requirements of the out-of-band filter, and enhance immunity to clock jitter. Using the direct charge transfer switched-capacitor technique in the multi-bit reconstruction DAC can reduce *kT/C* noise and element mismatch without increasing power dissipation. The data weighted averaging algorithm restrains nonlinearity caused by the mismatch of capacitors.

A 15-level quantization, third-order delta-sigma DAC is presented. Its sampling rate is 44.1 kHz with 18-bit input. The main clock is 2.8224 MHz because of the 64X oversampling ratio. This DAC was implemented by TSMC 0.18um CMOS process supported by CIC.

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首先感謝我的指導教授洪崇智老師，在我兩年的研究生活中提供良好的學習環境，以及這段日子來對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間。同時我也要感謝在這碩士班兩年內曾經教過我的每位老師，由於他們熱心的教學，使我在短短的碩士班兩年內，學習如何設計並且製作數位、類比積體電路。還有要感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路得以實現並完成驗證。

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特別要感謝我的父母和家人，感謝他們提供了一個穩定且健全的環境，使我無後顧之憂地完成我的學業。最後要感謝我的女朋友，感謝她一直默默的支持我、鼓勵我，並在這段成長的路上與我相伴。

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楊家泰

國立交通大學
中華民國九十五年十月

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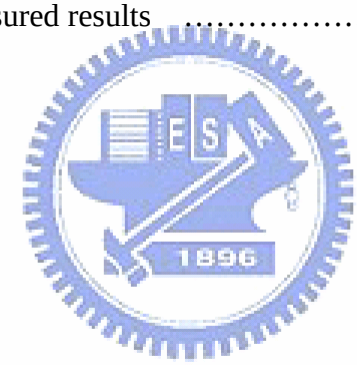


Chapter 1

Introduction

1.1 Motivation

Recently, the demand for an audio digital-to-analog converter has increased because of the development of multimedia systems. The state-of-the-art technique about 120-dB dynamic range is achieved for DAC realization [1], but it has several drawbacks such as large power consumption and limited out-of-band-noise reduction. It is almost impossible to use this type of D/A converters in very complex systems. For example, a complete digital radio system may have four or six delta-sigma DACs embedded. Therefore, low power consumption is crucial to the blocks. In addition, using fully differential or single-ended input/output signals affects the pin count. After considerations of overall factors, the requirements for DACs in these high-end audio systems should meet features of low power consumption [2], dynamic range above 16-bit (i.e., 96dB), performance resistance to the considerable clock jitter, integration of the complete D/A converter channel (implication for no external additional filter), and area reduction and so on.

In this research, a low power and low distortion delta-sigma digital-to-analog converter has been designed with the digital circuit implemented with FPGA and the analog circuit implemented with the standard TSMC 0.18μm CMOS 1P6M process. The parts of interpolator, delta-sigma modulator and switched capacitor filter are emphasized. The decrease in oversampling ratio can decrease the digital circuit speed and then we can achieve the goal of power consumption decrement. A high SNR

(signal-to-noise ratio) is performed in the delta-sigma modulator because of noise shaping function. However, the dynamic range and SNDR (signal-to-noise plus distortion ratio) are decided by noise and distortion caused by the analog circuit. In order to reduce total harmonic distortion, a low distortion switch is designed and applied to the switched capacitor filter.

1.2 Thesis Organization

This thesis is organized into six chapters.

In Chapter 1, this thesis is briefly introduced.

Chapter 2 describes the considerations of the delta-sigma DAC. It includes the architectures of the interpolation filter and the delta-sigma modulator. Finally, the one-bit and the multibit quantizers are compared.

Chapter 3 describes the key circuit blocks used in delta-sigma DAC. Among them are the interpolation filter, the multibit delta-sigma digital modulator, the thermometer encoder, the data weighted averaging encoder, the multibit switched-capacitor DAC, and the RC lowpass filter. The simulation results and the algorithms of each block are also presented.

Chapter 4 introduces the implementation of the delta-sigma DAC in detail. The issues in the design of the digital part circuit are also indicated. Then the bootstrapped switch is implemented to reduce distortion. Finally, the layout of the analog part circuit is presented.

Chapter 5 presents the testing environment, including the component circuits on the DUT (device under test) board and the instruments. Then, the analog circuit of the delta-sigma DAC is fabricated in a standard TSMC 0.18μm CMOS Mixed-Signal process and the pin configuration is listed. The measured results of this chip are also summarized.

Finally, the conclusions of this thesis are summarized in Chapter 6.

Chapter 2

General Design Consideration in Delta-Sigma D/A converter

2.1 Introduction of System Architecture

Delta-sigma DACs are preferred over Nyquist rate DACs in high resolution applications, because they relax the analog filter requirements. A simplified block diagram of an oversampled delta-sigma D/A converter is shown in Fig. 2.1 [3]. A digital signal with N-bit words is sampled with a data rate of f_N. The interpolator achieves a higher rate by inserting 0's between each input word with a rate of $M\ f_N$ and then filtering by a digital lowpass filter.

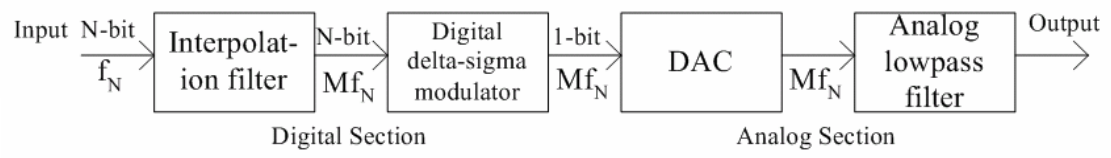


Figure 2.1 Simplified block diagram of a delta-sigma DAC.

The 1-bit output signal of the digital delta-sigma modulator can be converted to an analog signal by switching between two reference voltages. This is followed by an analog lowpass filter to remove the high frequency quantization noise and yields the required analog output signal. The sources of error in the delta-sigma DAC are the device mismatch which causes harmonic distortion, rather than component noise, device nonlinearities, clock jitter sensitivity and inband quantization error from the delta-sigma modulator.

The signal spectra of the input signal and the interpolated signal are shown in the top two figures of Figure 2.2. The output signal of the interpolation filter is passed through a delta-sigma modulator, in which the digital bit stream is truncated into words with less number of bits and keeping the result quantization noise out of the signal band. Finally, the data is transferred into analog signal by a combination of DAC and lowpass filter. The DAC and the first stage of the lowpass filter are implemented by using a switched capacitor filter typically. The switched capacitor filter is followed by a continuous time lowpass filter to attenuate the quantization noise properly. The signal spectra at the input and output of the analog section are shown on the bottom two graphs of Figure 2.2.

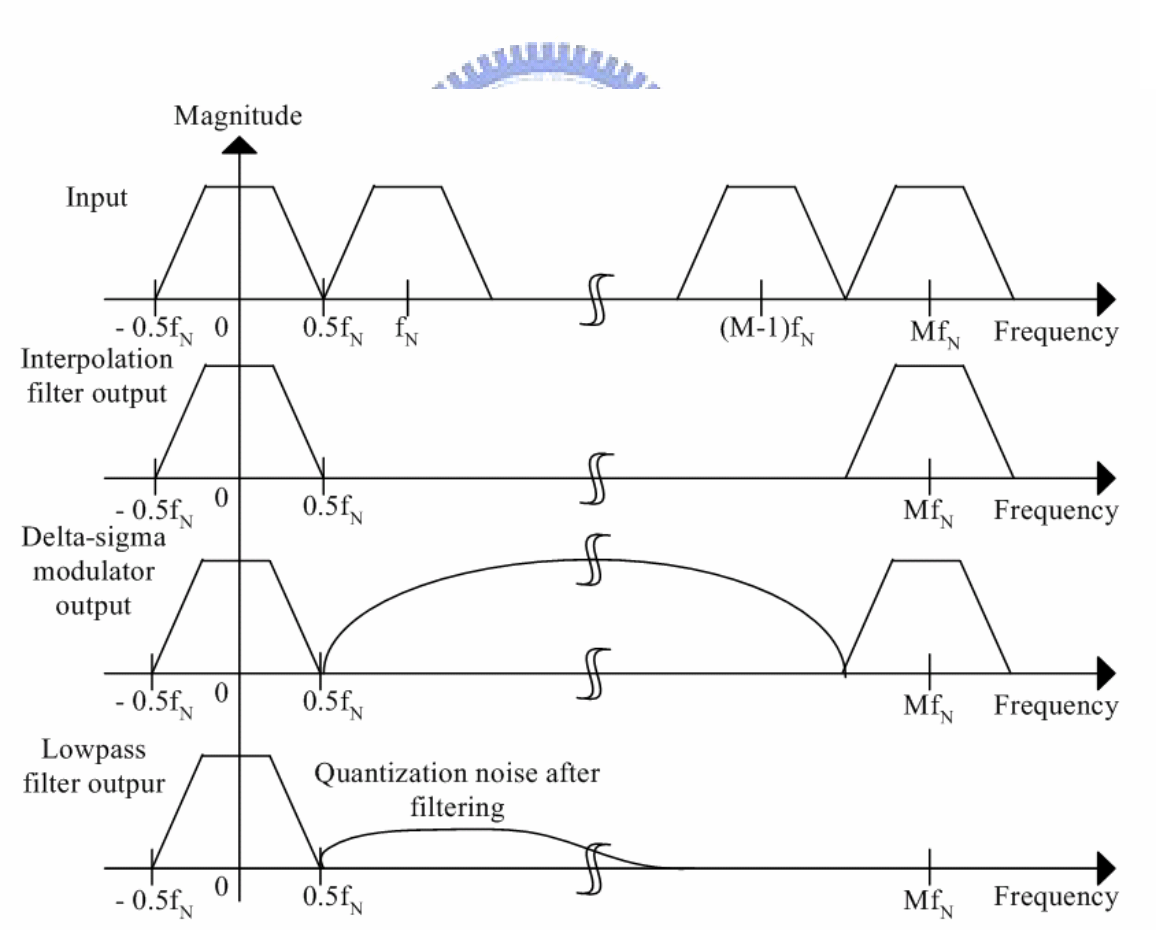


Figure 2.2 Frequency spectra at different points of the delta-sigma DAC

2.2 Interpolation Filter

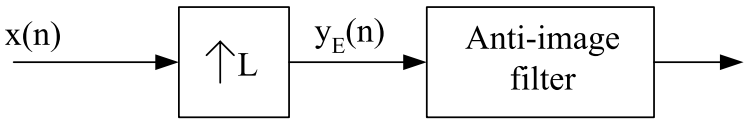


Figure 2.3 Block diagram of interpolator

A simplified block diagram of interpolator is shown in Figure 2.3. The digital input signal x(n) is upsampled to $y_E(n)$ by an oversampling ratio L. If the sampling rate of x(n) is a Nyquist rate f_s, the sampling rate of $y_E(n)$ will be $L f_s$. The Figure 2.4 shows the detail about how to increase sampling rate.

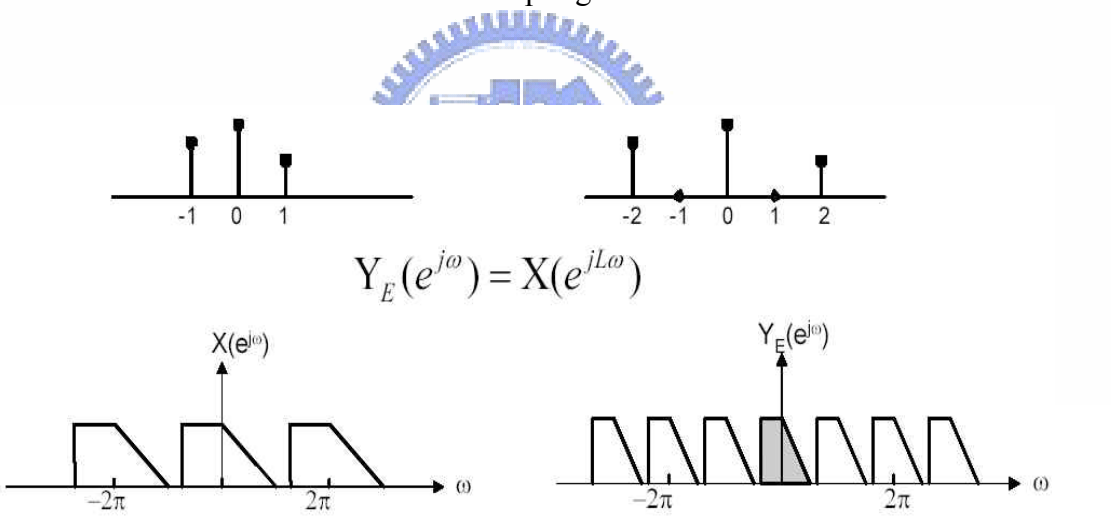


Figure 2.4 Spectra and waveforms of origin and upsampling signals

For example of oversampling ratio L = 2, the signal x(n) is converted into $y_E(n)$ by inserting one 0's into each input signal. The top graph of Figure 2.4 shows the difference between input and output. An anti-image filter is necessary to filter out the undesired image signal shown in the bottom graph of Figure 2.4. The detail of anti-image filter is discussed in the following subsections.

2.2.1 Finite Impulse Response (FIR) Filter

The anti-image filter is used to filter out the undesired image signal caused by upsampling. One of the common realizations of anti-image filter is Finite Impulse Response (FIR) filter. Comparing to Infinite Impulse Response (IIR), the FIR filter is linear phase, stable and easy to implement. However, high order is necessary for a sharp cutoff FIR filter. Figure 2.5 shows the structure of FIR. The number of h[n-1] means n-1 orders or taps.

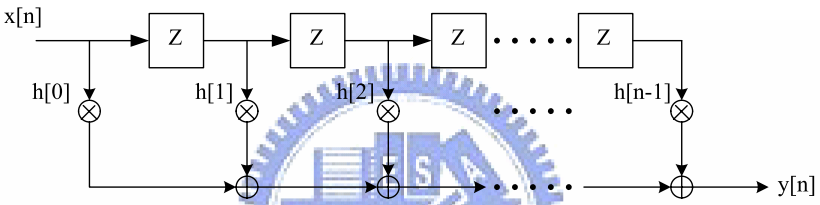


Figure 2.5 FIR structure

2.2.2 FIR Half-Band Filter

The technique of half-band is efficient in reducing the circuit complexity in the design of a sharp cutoff FIR filter [4]. Because about 50 percent of the filter coefficients are zero, half-band filter can cut down the implement cost. First, denote the transfer function H(z) of a linear-phase, FIR half-band filter with order n-1

$$H(z) = \sum_{n=0}^{N-1} h(n) z^{-n}, \qquad h(n) \text{ real.} \qquad (2.1)$$

The filter is restricted the length N-1 is even. A half-band filter design trick is by transforming from a one-band linear-phase FIR filter. To design a one-band filter, the

specifications of ω_p, ω_s, and δ must be given, where ω_p is passband edge, ω_s is stopband edge and $\delta = \delta 1$(passband ripple) + $\delta 2$(stopband ripple). Then we can design a (N-1)/2 order, one-band prototype linear-phase filter G(z) with specifications shown in Figure 2.6.

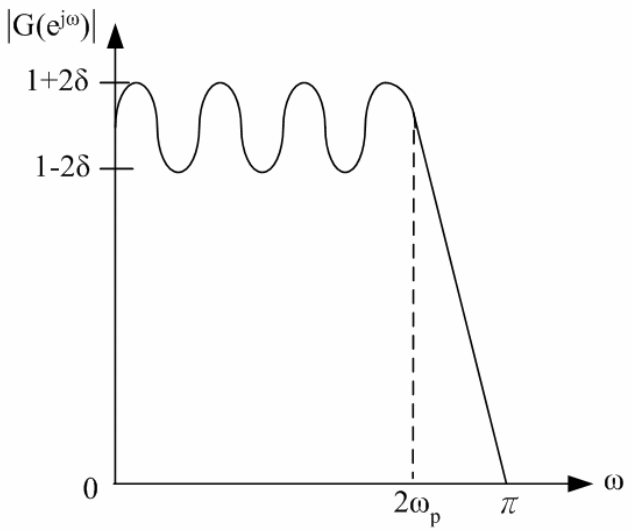


Figure 2.6 Amplitude response of G(z)

Its passband is from 0 to $2\omega_p$ and the transition is from $2\omega_p$ to π. Now we can define

$$H(z) = \frac{G(z^2) + z^{-N-1/2}}{2}, \tag{2.2}$$

then H(z) is a half-band filter with specifications shown in Figure 2.7. The impulse response of H(z) is apparently related to that of G(z) by

$$h(n) = \begin{cases} \frac{1}{2} g(\frac{n}{2}), & n \quad even \\ 0, & n \quad odd \neq \frac{N-1}{2} \\ \frac{1}{2}, & n = \frac{N-1}{2} \end{cases} \tag{2.3}$$

where g(n) is the impulse response of G(z).

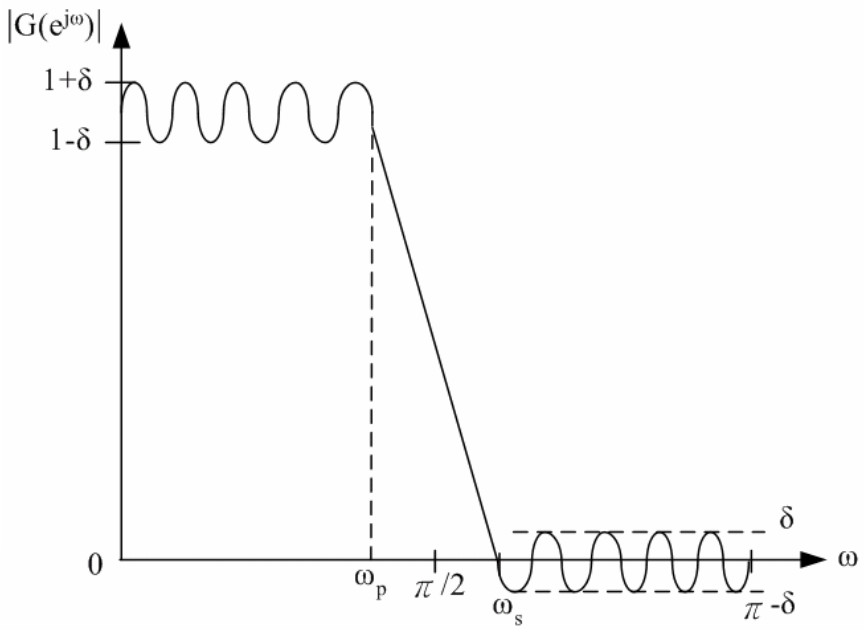


Figure 2.7 Typical amplitude response of a half-band FIR filter

Thus, the passband and stopband limit frequency must be located symmetrically, and the ripples must be the same in the two bands. These restrictions are usually adaptable in the interpolation-by-2 filtering.

2.3 Delta-Sigma Modulator

The delta-sigma modulator shown in Figure 2.8 is a negative feedback system [5]. It is the combination of oversampling technique and noise shaping function. The input bits are N and truncated into M bits by the quantizer in the forward path. However, a large quantization noise results from the truncation process. A high-pass transfer function affects the large quantization noise and shapes it into high frequency band. Thus, most of the noise power resides in the high frequency spectrum outside the

signal band. This is what is called “noise shaping”.

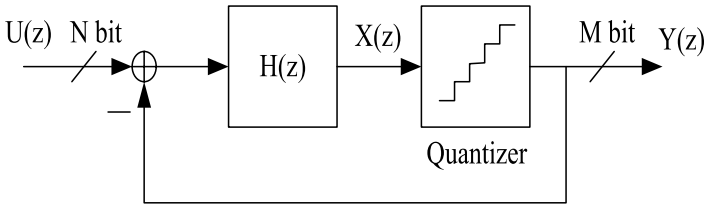


Figure 2.8 The structure of delta-sigma modulator (interpolator structure)

2.3.1 Quantization Noise versus Oversampling

First, modeling a quantizer as adding quantization error e(n), as shown in Figure 2.9. The quantization error is the difference between input x(n) and output y(n). The linear model can be assumed that a uniformly distributed white noise is additive.

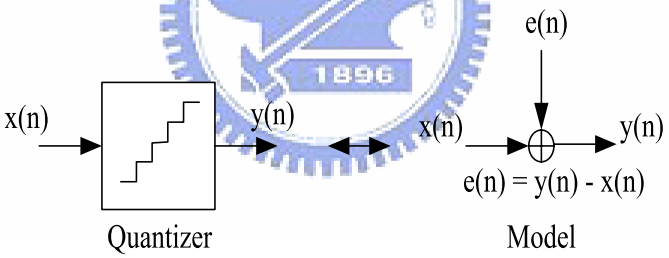


Figure 2.9 Quantizer and its linear model

Under the noise approximation, e(n) can be an independent random number uniformly distributed between $\pm\Delta/2$, where Δ is the difference between two adjacent quantization levels. Thus the quantization noise power equals $\Delta^2/12$ .The spectral density of the quantization noise $S_e(f)$ is shown in Figure 2.10. $S_e(f)$ is white and all its power is within $\pm f_s/2$. With a two-sided definition of power, the total noise power equals the area under $S_e(f)$ within $\pm f_s/2$. As the result of mathematics,

$$\int_{-f_s/2}^{f_s/2} S_e^2(f)df = \int_{-f_s/2}^{f_s/2} k_x^2 df = k_x^2 f_s = \frac{\Delta^2}{12} \tag{2.4}$$

and this relation gives

$$k_x = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}} \tag{2.5}$$

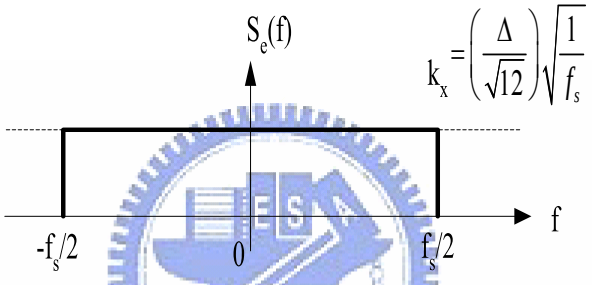


Figure 2.10 Assumed spectral density

If the desired signals are bandlimited to f_0 and the sampling rate of signal is at f_s, then an oversampling ratio (OSR) can be defined as OSR ≡ f_s /2f_0, where $f_s > 2f_0$. Since the signals of interest are all within ±f_0 after quantization, $y_1(n)$ must be filtered by H(f) to create $y_2(n)$, as shown in Figure 2.11. This filter with transfer function H(f) eliminates quantization noise out of f_0. The power within the signal $y_2(n)$ is still the same as the input signal, because we assumed that the signal-band is below f_0. But the quantization noise power is reduced to

$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)\,|H(f)|^2\,df = \int_{-f_o}^{f_o} k_x^2 df = \frac{\Delta^2}{12}\left(\frac{1}{OSR}\right) \tag{2.6}$$

thus, we can decrease 50 percent of the quantization noise power or 3 dB, equivalently 0.5bits, by doubling OSR.

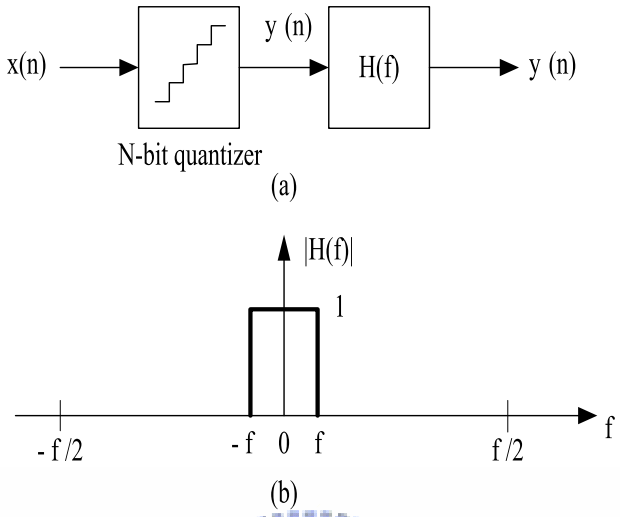


Figure 2.11 (a) A simple oversampling system. (b) The filter with brick-wall response.

Assuming the input signal is a sinusoidal wave, its maximum peak value without clipping is $2^N(\Delta/2)$. For this sinusoidal wave, the signal power, P_s, equals to

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{2.7}$$

then the maximum signal-to-noise ratio (SNR) can be calculated by the ratio of the signal power to the quantization noise power in the signal $y_2(n)$.

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right) = 6.02N + 1.76 + 10\log(OSR) \text{ (dB)} \tag{2.8}$$

The first term is the improvement in SNR by the N-bit quantizer. As discussing before, the straight oversampling provides a SNR enhancement of 3 dB/octave, or equivalently 0.5 bits/octave.

2.3.2 Delta-Sigma Modulator with Noise Shaping

A linear model of a noise-shaped delta-sigma modulator is shown in Figure 2.12. The quantization noise is indicated by E(z). By approximating the linear model as having two independent inputs, a signal transfer function, $S_{TF}(z)$, and a noise transfer function, $N_{TF}(z)$, can be derived.

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.9}$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.10}$$

When H(z) goes to infinity, $N_{TF}(z)$ will go to zero. The output signal can be expressed as the combination of the input signal and the quantization noise. In the frequency domain we can get

$$Y(z) = S_{TF}(z)U(z) + N_{TF}E(z) \tag{2.11}$$

To noise-shape the quantization noise, H(z) must have a large magnitude from 0 to f_0, which is the frequency band of interest. The signal transfer function, $S_{TF}(z)$, approximates unity over the signal-band with the choice of H(z). Furthermore, the noise transfer function, $N_{TF}(z)$, approximates zero over the same band. Thus, the

quantization noise decreases while the signal is almost unaffected.

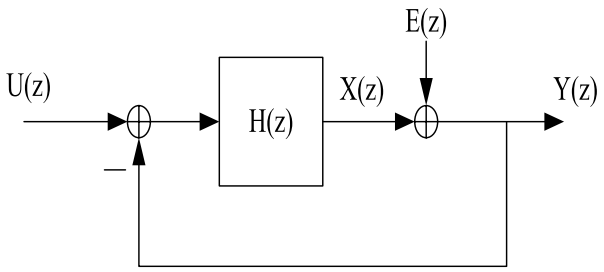


Figure 2.12 Linear model of the modulator

For the common case, the noise transfer function of a delta-sigma modulator must be a highpass function. Because the zeros of $N_{TF}(z)$ are equal the poles of H(z), we can get H(z) = 1/(z-1). Then the signal transfer function is given by

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1} \tag{2.12}$$

We can find that the signal transfer function is simply a delay. If the order of the delta-sigma modulator is L, the noise transfer function is generally in the form of a discrete-time differentiator.

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = (1-z^{-1})^{L} \tag{2.13}$$

The examples of first-order and second-order noise-shaped modulators are shown in Figure 2.13. These modulator structures employ pure differentiation noise transfer functions. The dynamic range of the delta-sigma modulator can be derived with the order of the modulator L, the oversampling ratio R, the number of the quantizer output bit N as

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 R^{2L+1} \tag{2.14}$$

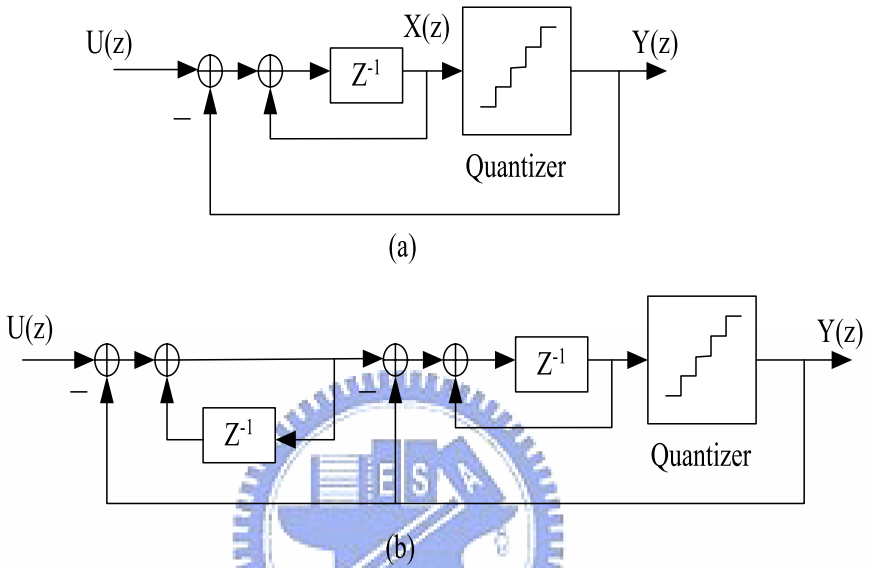


Figure 2.13 Block diagram of pure differentiation modulators, (a) first order, and (b) second order.

Figure 2.14 shows the general shape of zero-order, first-order, and second-order noise-shaping curves. The noise power over the band of interest decreases as the noise-shaping order increases. However, there are some issues about increase of out-of-band noise and stability for the higher-order modulators.

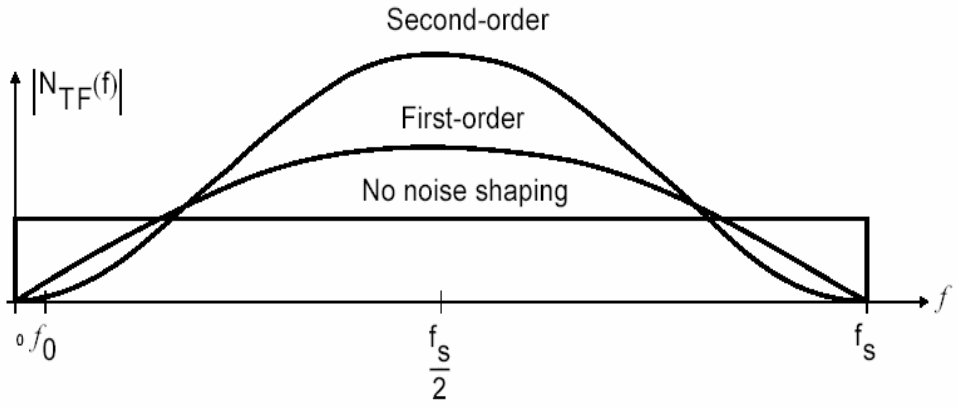


Figure 2.14 Different orders of the noise-shaping transfer functions

2.3.3 High-Order Modulator

In general, an Lth-order noise-shaping modulator improves the signal-to-noise ratio (SNR) by 6L+3 dB/octave, or equivalently L+0.5 bits/octave. There are two approaches - interpolative and MASH - for realizing higher-order noise-shaping modulators. The interpolative structure, as shown in Figure 2.8, is typically a single high-order structure with feedback from the quantized signal. It is more suitable than the error-feedback structure, as shown in Figure 2.15, to analog implementations of modulators due to its reduced sensitivity.

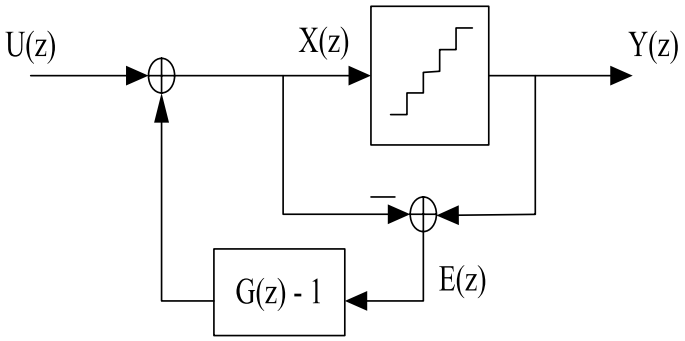


Figure 2.15 The error-feedback structure of a general delta-sigma modulator

One of the first approaches for realizing higher-order interpolative modulators is using a filtering structure similar to a direct-form filter structure. However, a direct-form-type structure is sensitive to component variations, which can cause the zeros of the noise transfer function to move off the unit circle. In order to improve component variations, resonators can be used with a modified interpolative structure, as shown in Figure 2.16. The resonators in this structure are due to the feedback signals associated with f_1 and f_2. They result in the placement of zeros in the noise transfer function located over the frequency-of-interest band. This arrangement provides better dynamic range performance than placing all the zeros at dc. Unfortunately, it is possible for modulators of order two or more to become unstable, especially when large input signals are given. If they go unstable, they may never return to stability even when the large input signals go away.

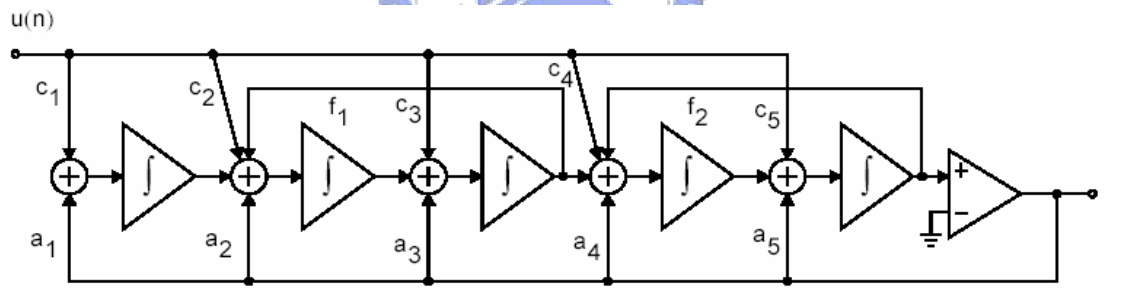


Figure 2.16 A block diagram of a fifth-order modulator

Another approach for realizing modulators, MSAH (Multi-stAge noise SHaping), is to use a cascade-type structure, where the overall higher-order modulator is constructed of using the lower-order ones. The advantage of this approach is that the lower-order modulators are more stable, and then the whole system should remain stable. The arrangement for using two first-order modulators to realize a second-order modulator is shown in Figure 2.17. The first section's quantization error, $e_1(n)$, is

passed to another modulator and the outputs of two modulators are combined. In such a way, the first section's quantization noise is removed. The output is left only with the second section's quantization noise, which has been filtered twice because of two modulators. According to the straightforward linear analysis, we can get

$$Y(z) = z^{-2}U(z) - (1 - z^{-1})^2 E_2(z) \qquad (2.15)$$

Thus, a MASH approach has the advantage that higher-order noise filtering can be achieved by using lower-order modulators. The lower-order modulators are much less sensitive to instability as compared with an interpolative structure having a high order with a single feedback.

However, the MASH approach with a cascade of first-order stages is sensitive to finite opamp gain and mismatch between the analog and digital circuitry. These mismatches cause first-order noise to leak through from the first modulator, and then reduce dynamic range of the system. To improve this problem, the first stage is often chosen to be a higher-order modulator. Its leaking noise does not cause as a serious effect as it would if the first stage was first-order modulator. It is important to minimize errors due to the input-offset voltage caused by clock feedthrough or opamp input-offset voltages. An additional circuit design must be employed to reduce these effects in practical applications. Finally, the MASH approach results in the digital output signal, y(n), as a four-level signal because of the combination of the original two-level output signals. This four-level signal requires a linear four-level D/A converter in a D/A application.

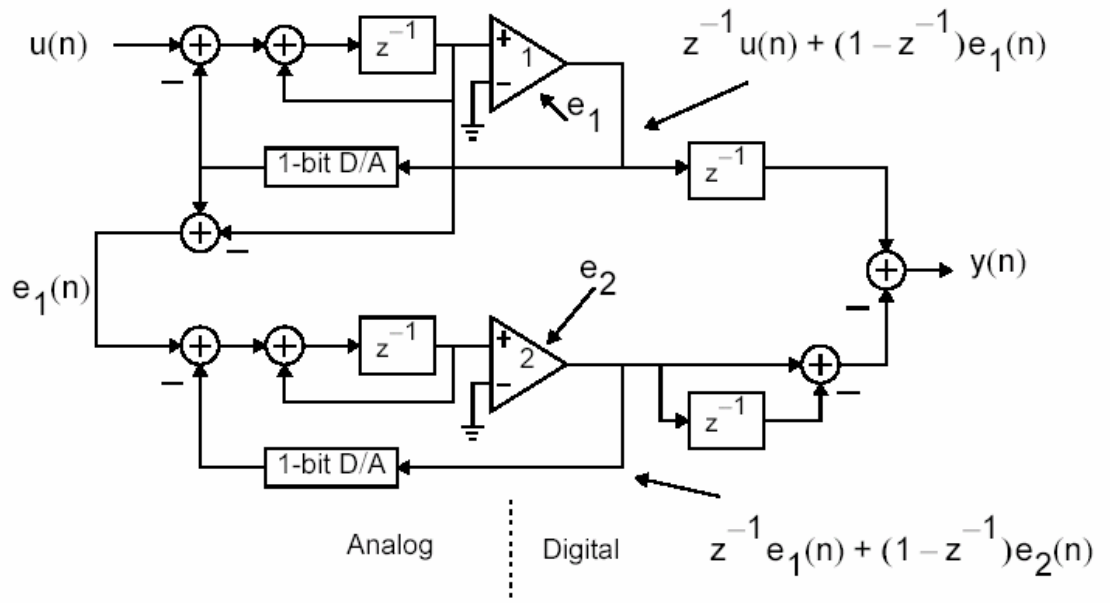


Figure 2.17 A second-order MASH modulator using two first-order modulators

2.4 Comparison of One-bit and Multibit

The comparison of one-bit and multibit modulators is based on oversampling ratio, linearity, stability, and out-of-band quantization noise. The main advantage of one-bit modulator is inherently linear since it only need to produce two output levels and two points can define a straight line. However, the one-bit modulator with higher-order is easy to become unstable. A stable modulator is defined as one in which the input to the quantizer remains bounded and the quantization does not become overloaded. An overloaded quantizer means its input signal is over the quantizer's normal range. It causes the quantization error to be greater than ±Δ/2. According to a general rule, keeping the peak frequency response gain of the noise transfer function, $N_{TF}(z)$, less than the amplitude 1.5. In mathematical terms,

$$| N_{TF}(e^{j\omega}) | \leq 1.5 \qquad \text{for } 0 \leqq \omega \leqq \pi \qquad (2.16)$$

should be satisfied for a one-bit modulator. It often results in a stable modulator with

conforming to this stability criterion. Another disadvantage of one-bit modulator is to result in a large amount of out-of-band quantization noise, which must be significantly reduced by the analog circuit. Such a task requires relatively high-order analog filtering. It increases the difficulty in designing the analog filtering circuit.

A multibit modulator can provide the improvement in SNR. From the formula (2.8), SNR increases 6 dB with increasing one bit in the quantizer output. Therefore, a multibit modulator of a given order can achieve the target of dynamic range with less oversampling ratio than a one-bit modulator of the same order. In the application of higher-order modulators, a multibit modulator is also more stable than a one-bit modulator [6]. Additionally, the use of the multibit modulator can significantly reduce the large amount of out-of-band quantization noise and tolerate relaxed out-of-band filter specifications, but it must take care to ensure the multibit output of the modulator remains linear. The linearity of the multi-level output is limited by the mismatches in the components which are used to generate the analog levels. The diagram of step mismatches in the D/A converter is shown in Figure 2.18.

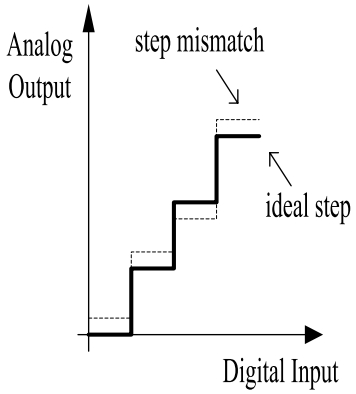


Figure 2.18 Illustration of step mismatch in the D/A converter

These step mismatches caused by component mismatches result in the distortion over the signal band, and then reduce the obtained SNDR (signal-to-noise plus distortion ratio). In order to solve the mismatch problem, various linearization techniques have been proposed, such as trimming and dynamic element matching (DEM). The trimming technique is practical for a D/A converter to enhance the matching property of identical components. It does not require extra circuits to reduce mismatch effect if each component is trimmed individually. However, trimming technique is expensive, time-consuming, and not a one-time process since device aging and temperature variation occurring in the lifetime of a D/A converter reduce the effect of compensating mismatches. The algorithm of DEM will be discussed in the following section.

Chapter 3

Design of Multibit Delta-Sigma D/A Converter

3.1 Multibit Delta-Sigma DAC Architecture

The four main architectural level parameters for a multibit delta-sigma DAC are oversampling ratio, noise-shaping order, quantization level, and reconstruction filter order [7], [8]. The design criteria for selecting these parameters will be discussed later. The overall adopted architecture for the designed multibit delta-sigma DAC is shown in Figure 3.1. The resolution of the input signal is 18 bits. The input sampling rate, fs, is 44.1 kHz. It is interpolated by a 64× OSR (oversampling ratio). The resulting signal with 18 bits is passed through a third-order digital delta-sigma modulator. Here the operating speed is 2.8224 MHz because of the factor 64×. The multibit delta-sigma modulator generates a 15-level output.

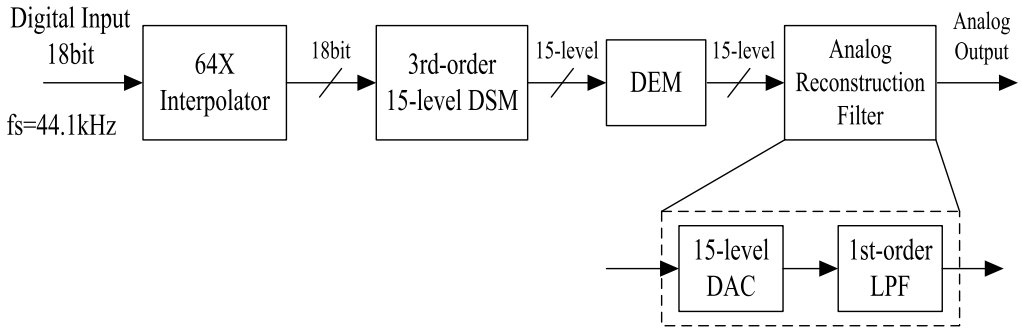


Figure 3.1 Overall architecture of the multibit delta-sigma DAC

The drawback of a multibit delta-sigma modulator is the nonlinearity of the multibit digital-to-analog interface which is realized by a number of components, such as capacitors or resistors. The nonlinearity is due to the mismatch between the components. To improve the nonlinearity of the multibit modulator, a DEM algorithm can be adopted before passing the output of the multibit modulator to the analog reconstruction filter. How many bits used in the quantizer depends on the consideration of designing the analog circuit. The analog reconstruction filter is composed of a 15-level DAC and a first-order RC LPF (low-pass filter). The output signal of the digital circuit is transferred to the analog signal by a 15-level internal DAC, and then filtered by a first-order RC LPF.

3.2 Interpolation Filter

An interpolation filter is used to increase sampling rate of the data. Its purpose is to decrease the quantization noise and relax the out-of-band filtering specifications. The higher OSR (oversampling ratio) is adopted, the better SNR is obtained and the out-of-band filter is easier to design. However, the high OSR increases circuitry speed requirements. It enables digital operation at high voltage and a corresponding increase in digital power consumption. On the contrary, the low OSR results in reduction in power consumption of the digital circuit but causes higher quantization noise. Therefore, how to decide on an OSR is a tradeoff between factors in power dissipation, quantization noise, and requirements of the analog filter.

A block diagram of the whole interpolation filter is shown in Figure 3.2. The interpolation filter is composed of three stages and upsamples the 18-bit input data by 64× and eliminates baseband images around multiplies of sampling rate. The first two

stages of the interpolation filter are implemented by a 48-tap finite impulse response (FIR) filter and a 20-tap FIR filter. The final SINC filter with 8× interpolation is realized by a simple zero order hold register.

Figure 3.2 The block diagram of the interpolation filter

Their cutoff frequencies are half *fs* equally, which means the passband is signal band. The coefficients of the FIR filters are generated by Matlab, which is a functional simulation tool. Although the coefficients can be obtained, the wordlength of the coefficients may be too long to be represented. For the consideration of the hardware design, the wordlength of the coefficients is truncated to a limited bit number, 18 bits. The passband ripple of the FIR filter is about 0.03 dB and the stopband attenuation is about 50 dB, which is sufficient for this application. The frequency responses of the two FIR filters are shown in Figure 3.3 and Figure 3.4, individually [9].

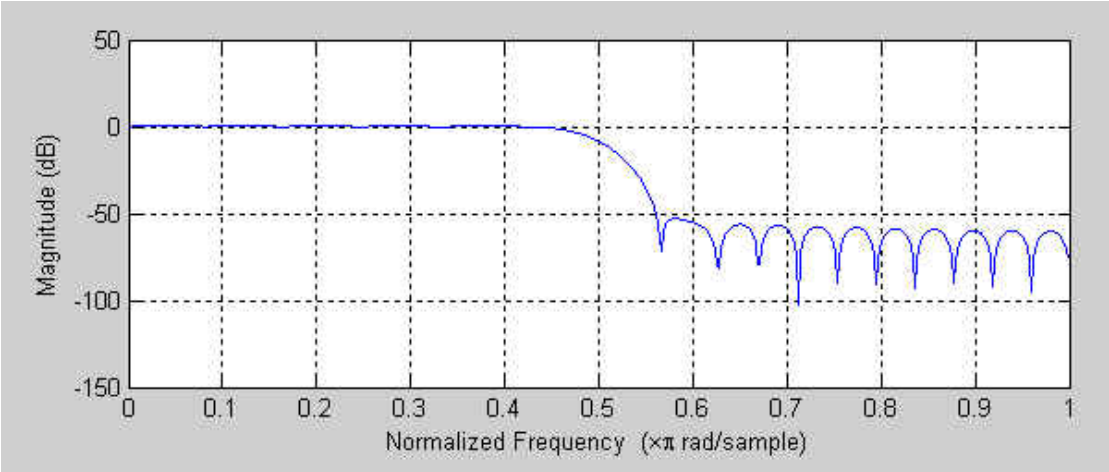


Figure 3.3 The frequency response of the 48-tap FIR filter. Here the frequency is

normalized by *fs*.

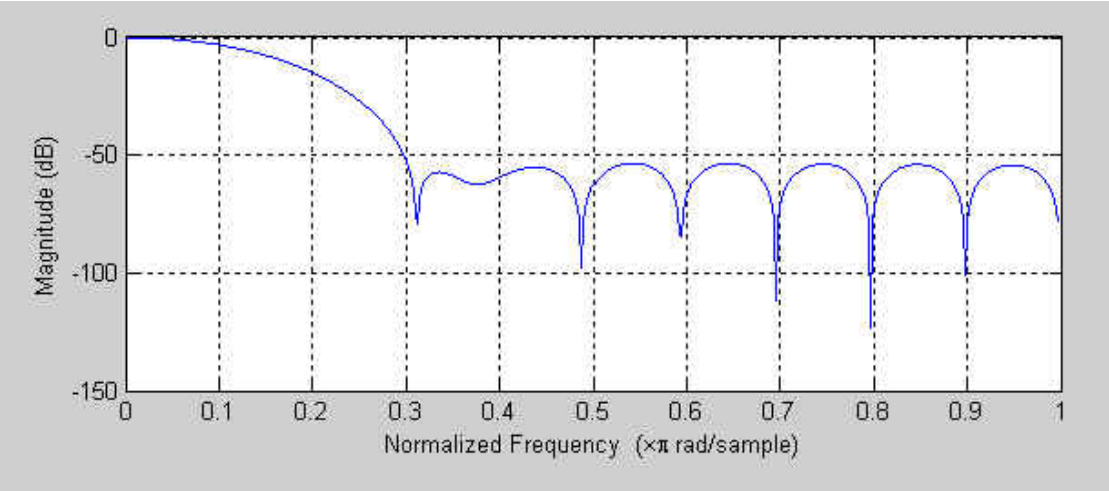


Figure 3.4 The frequency response of the 20-tap FIR filter. Here the frequency is normalized by 4*fs*.

The sinc filter function in time domain is shown in Figure 3.5. It can be expressed mathematically as

$$u[0] = u[1] = \cdots = u[7] = k[0] \tag{3.1}$$

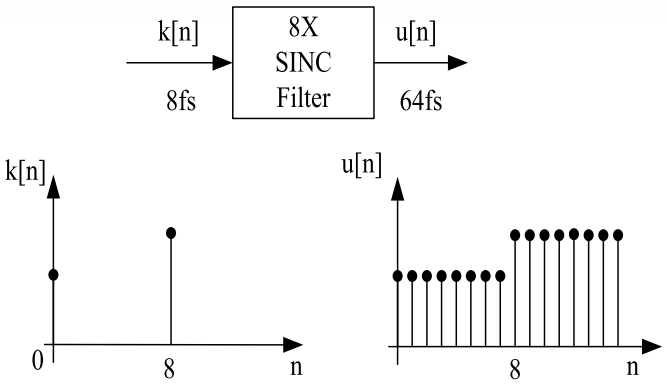


Figure 3.5 Sinc filter function in time domain with upsampling ratio 8

The frequency response of the sinc filter is shown in Figure 3.6. It must be noticed the inband frequency response has gain attenuation. However, the frequency response

of the whole interpolation filter still meets the specification fortunately without any compensating circuit for the sinc effect.

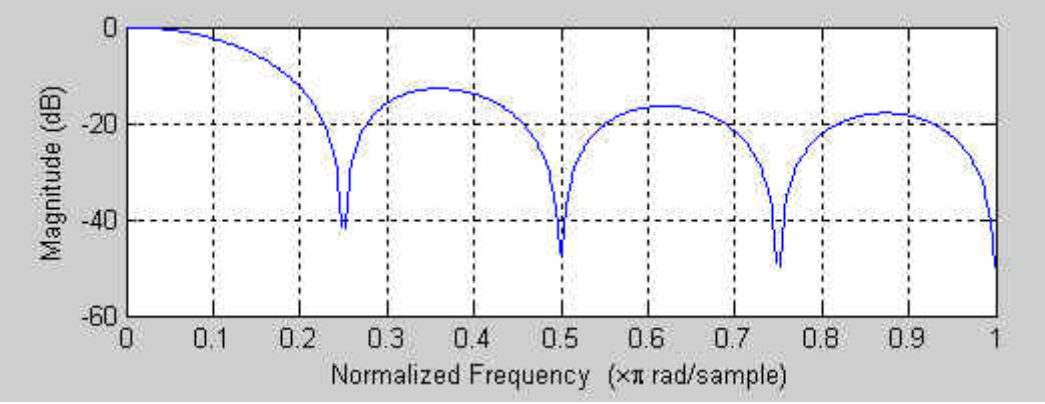


Figure 3.6 The frequency response of the sinc filter. Here the frequency is normalized by 32*fs*.

The frequency response of the overall interpolation filter is shown in Figure 3.7 from dc to 8 *fs*. The input signal is sinc function in time domain and rectangular wave in frequency domain.

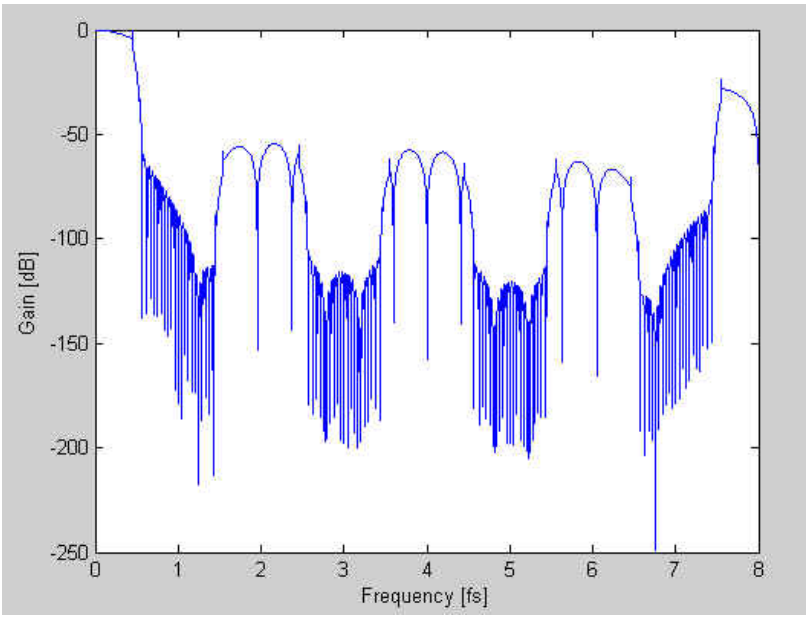


Figure 3.7 The frequency response of the overall interpolation filter

3.3 Multibit Delta-Sigma Digital Modulator

At the output of the interpolation filter, a delta-sigma modulator with third-order, CRFB (cascade-of- resonators, feedback form) structure is adopted [10], [11]. This structure of the delta-sigma modulator is shown in Figure 3.8. It operates with a sampling frequency of 2.8224 MHz, due to oversampling ratio 64×. This data rate is chosen as a trade off between dynamic range achievement, digital part power consumption, and analog filter requirements, as discussed above. A multibit quantizer with 15-level is used in the delta-sigma modulator output.

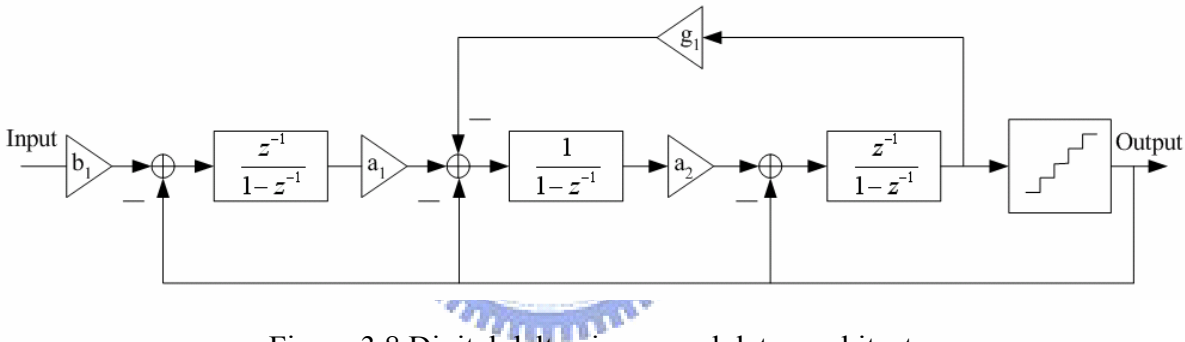


Figure 3.8 Digital delta-sigma modulator architecture

The signal transfer function (STF) and noise transfer function (NTF) of the delta-sigma modulator structure can be expressed with the gain parameters a_1, a_2, b_1, and g_1 indicated in Figure 3.8 as

$$\mathrm{STF} = \frac{a_1 \cdot a_2 \cdot b_1 \cdot z^{-2}}{1 + (g_1 \cdot a_2 - 2 + a_2) \cdot z^{-1} + (1 - g_1 \cdot a_2 + a_1 \cdot a_2 - a_2) \cdot z^{-2}} \qquad (3.2)$$

$$\mathrm{NTF} = \frac{1 + (g_1 \cdot a_2 - 3) \cdot z^{-1} + (3 - g_1 \cdot a_2) \cdot z^{-2} - z^{-3}}{1 + (g_1 \cdot a_2 - 2 + a_2) \cdot z^{-1} + (1 - g_1 \cdot a_2 + a_1 \cdot a_2 - a_2) \cdot z^{-2}} \qquad (3.3)$$

The noise transfer function realizes a highpass transfer function given by the Chebyshev response. In the audio band (20 Hz - 20 kHz), a flat noise floor is obtained by designing the NTF to have the zeros optimally spread in the band, such as one zero at dc and two conjugate zeros at 15 kHz. This placement provides a dynamic range improvement compared to the case in which all zeros are placed at dc [12]. The signal transfer function realizes a lowpass transfer function with a flat response in the audio band and attenuation at high frequency. The values of the coefficients of the delta-sigma modulator structure are referred to the MATLAB model studied for the NTF and STF design. These coefficients are shown in Table 3.1 and have been approximated for the digital implementation. The resulting output waveform and spectrum of the delta-sigma modulator are shown in Figure 3.9 and Figure3.10 respectively. The out-of-band spectrum is shown in Figure 3.11. As expected in delta-sigma modulator, a significant out-of-band noise is presented.

coefficient	approximated value
b_1	$1+2^{-2} = 1.25$
a_1	$2^{-1}+2^{-4} = 0.5625$
a_2	$2^{-1}+2^{-2} = 0.75$
g_1	$2^{-10}+2^{-11} = 0.001468$

Table 3.1 The coefficients in the delta-sigma modulator

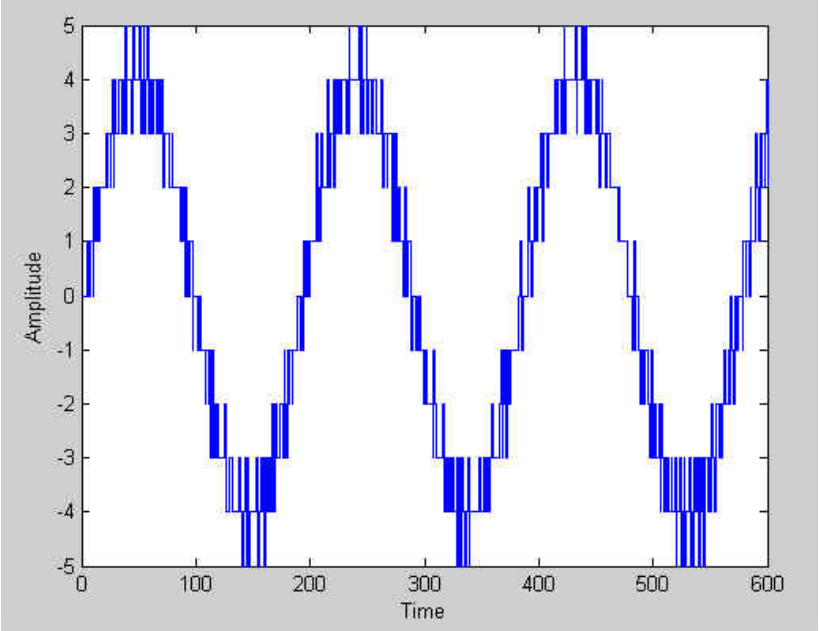


Figure 3.9 The waveform of the delta-sigma modulator output

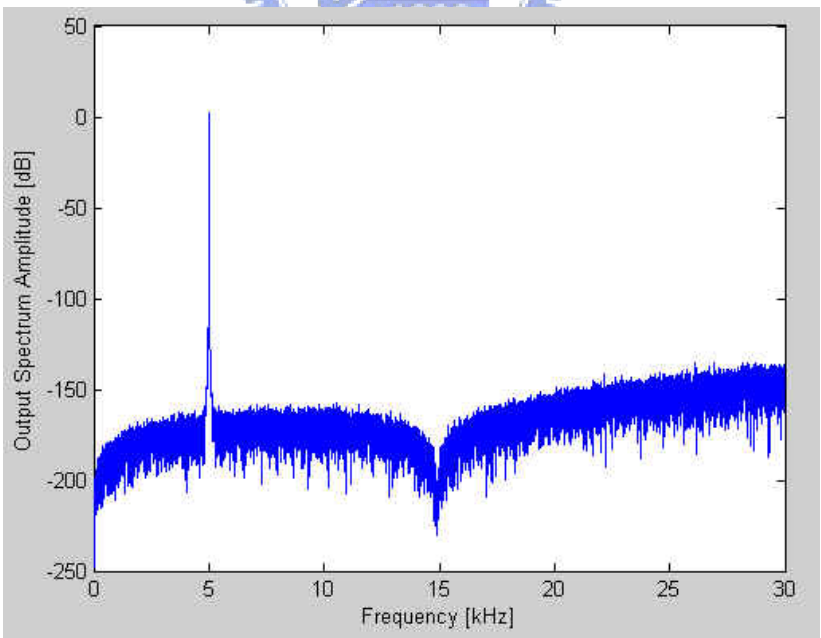


Figure 3.10 The in-band spectrum of the delta-sigma modulator output

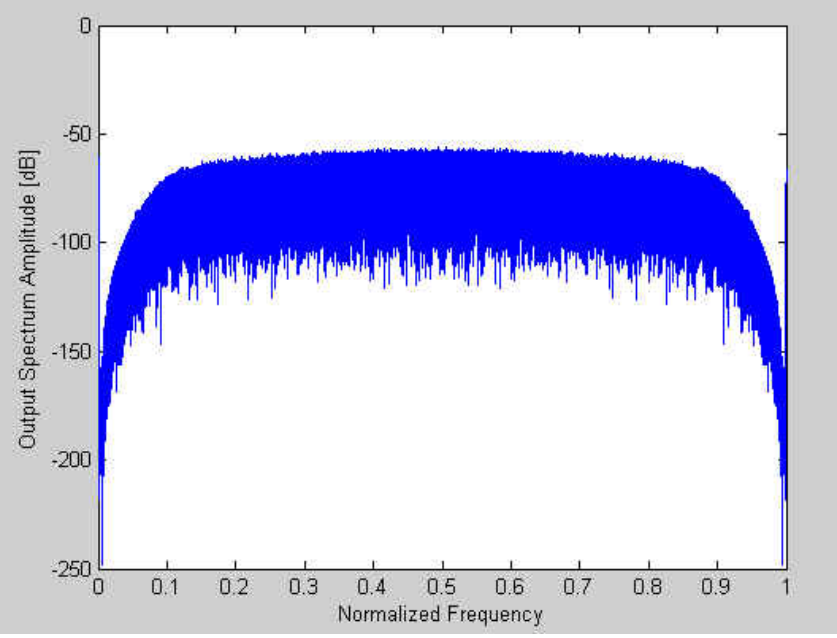


Figure 3.11 The out-of-band spectrum at the delta-sigma modulator output

The use of the multibit quantizer can also make the structure of the delta-sigma modulator more stable. However, the multilevel output requires using a number of unitary components at the digital-to-analog interface (i.e. capacitors), which is equal to the number of the quantizer output levels. The natural mismatches between the analog devices cause signal distortion. This problem can be solved by implementing dynamic element matching (DEM) at the digital-to-analog interface.

3.4 Dynamic Element Matching Block

A DEM algorithm is to execute the randomized selection of the analog elements [13], [14]. It can avoid performance loss in terms of SNR and THD (total harmonic distortion) due to the mismatches between the capacitors, which is used in the input structure of the reconstruction filter. The noise due to distortion may be translated to white noise or shaped in spectrum depending on the used algorithms. For example, it

may be a highpass characteristic. The randomized selecting process is realized in two stages, which are thermometer encoder and DWA (data weighted averaging) encoder [15]. They are shown in Figure 3.12. The 4-bit signal of the delta-sigma modulator output is translated into 15-bit signal by a thermometer encoder. Then this 15-bit signal is randomized by a DWA encoder.

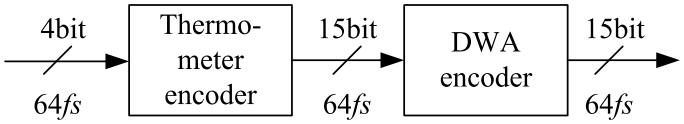


Figure 3.12 The implementation of DEM process

3.4.1 Thermometer Encoder

The operation of thermometer encoder is to convert binary into thermometer code, with the lower ranks producing all ones, and the higher ranks producing all zeros. Then how many capacitors of the digital-to-analog interface must be charged depends on the thermometer code. This thermometer encoder is used to transfer the four signed bits of the delta-sigma modulator output signal. The four signed bits means the levels from -8 to +7. The translation results are listed in Table 3.1.

Quantizer levels	Logic word or Number of selected capacitors	Thermometer word
+7	15	111111111111111
+6	14	011111111111111
…	…	…
1	9	000000111111111
0	8	000000011111111
-1	7	000000001111111
…	…	…
-7	1	000000000000001
-8	0	000000000000000

Table 3.2 Operation of thermometer encoder

Note that no charge has to be injected in the analog reconstruction filter when the 0 logic level is chosen, so no input capacitors are selected.

3.4.2 DWA (data weighted averaging) Encoder

The DWA algorithm uses all the internal DAC components of the analog reconstruction filter at the maximum possible rate while ensuring that each component is used the same number of times. This is realized by selecting components sequentially from an array, and then beginning with the next available unused component. Figure 3.13 illustrates the concept for a 3-bit DAC with an input sequence of 110, 000, 011, and 001. A 3-bit DAC can be translated into 7-bit thermometer code and implemented by seven equally weighted elements. The first two elements of the

DAC are selected when the input sequence, 110, is applied. The next four elements of the DAC are selected when the input sequence, 000, is applied. If the input sequence, 011, is applied, all elements of the DAC are selected. When the next input sequence, 001, is applied, the first four and the last one are selected. The component selection will continue in this manner sequentially as the input data is applied.

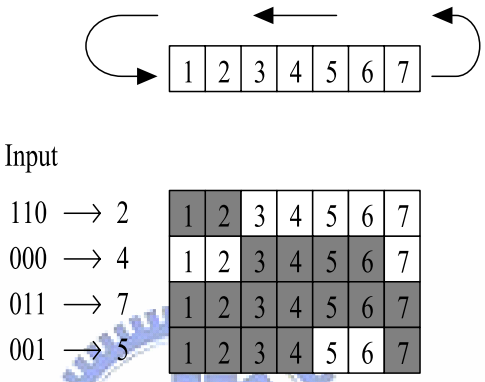


Figure 3.13 DWA operation

As described above, the element averaging is controlled entirely by the input data sequence. Thus, we can refer it to data weighted averaging (DWA) dynamic element matching. This element selection process can use all elements at the maximum possible rate, which ensures that the mismatch errors between components will sum to zero quickly, moving distortion to high frequencies. Another consequence of the cyclic sequencing is that no element of the DAC is selected with an inordinate numbers of times, even in a short time interval. A 15-bit internal DAC is adopted for this design. The input data is 15-bit thermometer code translated from the 4-bit data of the delta-sigma modulator output. The components of the DAC are selected according to the method described above.

3.5 Analog Reconstruction Filter

The function of the analog reconstruction filter is to smooth the digital signal and to reject the out-of-band noise, without compromising the signal purity achieved with the previous digital processing. The main target of the design of this digital-to-analog filter is the minimization of power consumption and area size, while achieving the required DR (dynamic range) and SNR_{out} (out-of-band SNR). These two parameters refer to different aspects. The DR refers to the noise located in the signal band and is dominated by the 1/f and thermal noise of the analog part. The SNR_{out} refers to the residual noise out of the signal band and is dominated by the quantization noise, which depends on the amount of filtering section implemented in the analog part. The two parameters are in tradeoff: a larger amount of out-of-band filtering requires a larger analog filtering section and this causes higher in-band noise, which reduce the DR. For the minimization of the power consumption and area size in addition to the low noise requirement, we realize the analog reconstruction filter with less operational amplifiers.

3.5.1 Low-Power Multibit Switched-Capacitor DAC

The multibit switched-capacitor (SC) technique introduced in this section reduces power dissipation of the internal DAC without sacrifice in noise performance [16]. An SC implementation has advantages over the current steering approach in reducing clock jitter sensitivity and data dependent glitches which can cause distortion. In a conventional SC DAC, an increase of capacitor size in attempt to reduce *kT/C* noise requires a corresponding increase of power consumption. For this design, using the DCT-SC (direct charge transfer switched-capacitor) technique makes its power

dissipation less dependent on capacitor size. The concept of an internal DAC with DCT-SC technique is shown in Figure 3.14. In this figure, the same capacitors are used as the switched input capacitor and the switched feedback capacitor. Since the input capacitor C_{in} directly transmits the charge to the integrating capacitor C_{hold}, the opamp does not need to provide charging current for the capacitors. This technique was originally proposed to realize a robust unity gain amplifier and was later adopted to prevent the problem of opamp slew limiting at the switched-capacitor to continuous-time interface in the analog reconstruction filter of a 1-bit DAC. Slew limiting in the opamp results in a spike in stair step waveform, which causes distortion when it is filtered in continuous-time.

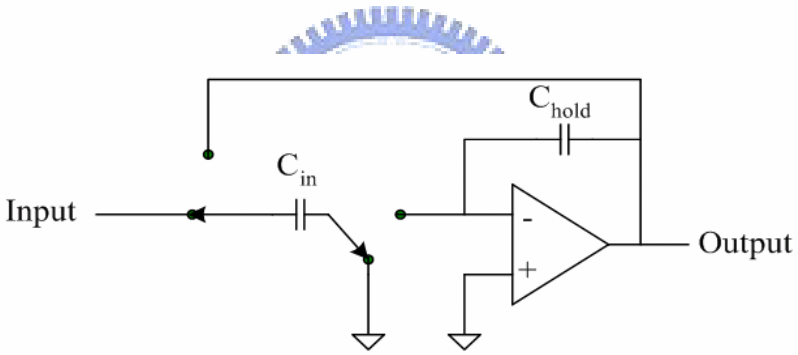


Figure 3.14 Concept of the DCT-SC technique

A 15-level DCT-SC DAC is shown in Figure 3.15. The sampling rate of the DAC is 2.8224 MHz. During the sample phase Φ_1, fifteen equally sized capacitors C_1-C_{15} sample the data D_1-D_{15} of the DWA output. During the hold phase Φ_2, the top of the C_1-C_{15} are all connected to the inverting input of the opamp and the bottom plates are all connected to the opamp output. Then all fifteen capacitors are connected in parallel and in the feedback path. By this operation, the charge sampled at Φ_1 will be distributed averagely by direct charge transfer among the capacitors at Φ_2. Therefore, the analog output level is generated without the support of the opamp.

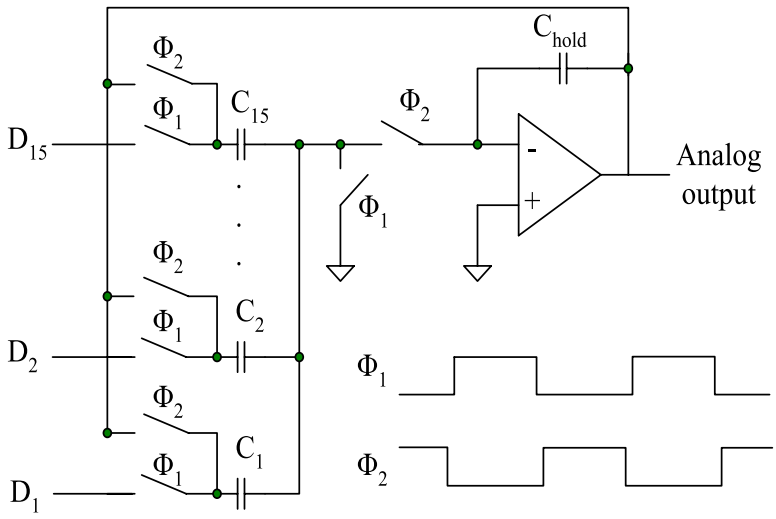


Figure 3.15 The scheme of 15-level DCT-SC DAC

The use of DCT technique makes the slew component of power consumption negligible and independent of capacitor size, because the power required charging the bottom plate parasitic capacitance mostly determines the power consumption. Hence this reason allows use of larger sampling capacitors for resisting noise with small increase of power consumption. At the discrete-to-continuous-time interface, any nonlinearity of the analog output waveform will be converted into noise or distortion in the following lowpass filter. By use of SC technique, clock jitter does not affect the analog levels of the discrete-time sampled points if the settling is adequate. However, when observed in continuous-time, clock jitter appears as a random signal which causes the stair step waveform of the output. The output signal includes high frequency quantization noise, which will be modulated into the signal band. Fortunately, the integrating capacitor C_{hold} provides a first-order lowpass characteristic with a cutoff frequency about 170 kHz in addition to the DAC function. This reduces the high frequency quantization noise and the noise modulated back to the signal band.

3.5.2 RC Lowpass Filter

The RC LPF (lowpass filter) executes out-of-band noise filtering. A general first-order LPF with a single opamp is shown in Figure 3.16. The cutoff frequency of the RC LPF is 496 kHz, which is sufficient to filter out the clock signal presented in DCT-SC DAC. Therefore, a final analog signal of the whole delta-sigma DAC is obtained.

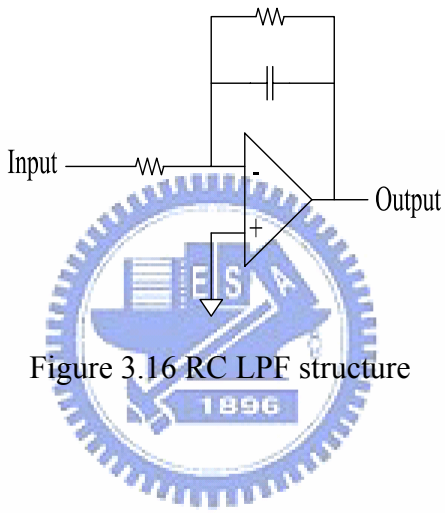


Figure 3.16 RC LPF structure

Chapter 4

Circuit Implementation and Layout

4.1 Introduction

The overall design of the delta-sigma DAC has been presented summarily. In this chapter, we separate the delta-sigma DAC into digital and analog parts. The considerations for the circuit implementation will be introduced in detail in the following sections.

4.2 Digital Part Circuit

The block diagram of the digital part circuit is shown in Figure 4.1, which consists of the 64x interpolation filter, third-order 15-level delta-sigma modulator, thermometer encoder and DWA encoder. The operation of each stage has been introduced in chapter 3. Here we will discuss the consideration for the hardware structure of the digital part circuit.

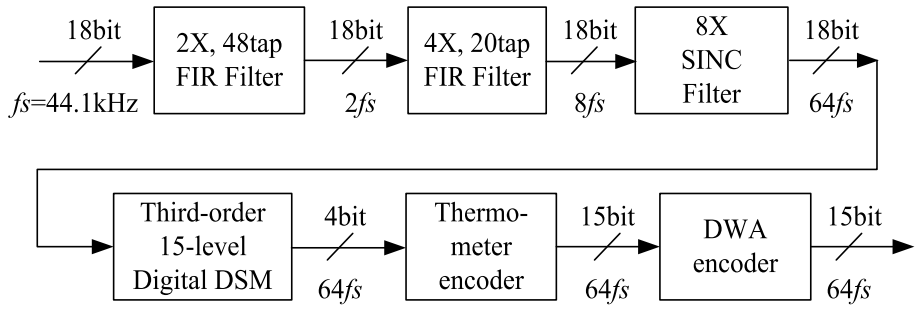


Figure 4.1 The block diagram of the digital part circuit

4.2.1 Interpolation filter

The interpolation filter consists of a 2-fold interpolation filter, a 4-fold interpolation filter and a sinc filter with 8x oversampling ratio. As discussed above, the signal after oversampling needs to pass through a FIR filter for filtering out images. In order to save the hardware cost of the filters, they can be realized by a polyphase algorithm.

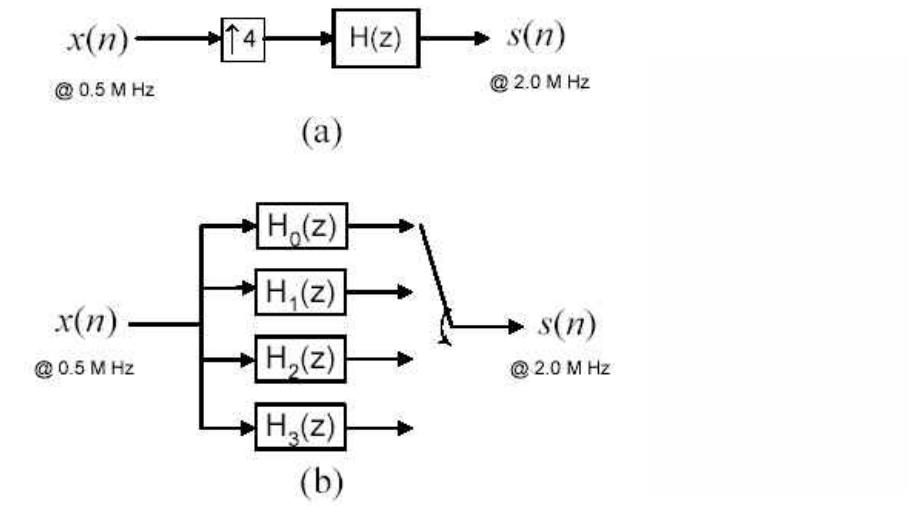


Figure 4.2 (a) 4-fold interpolation filter (b) Scheme of polyphase filter

For example, Figure 4.2 (a) is a 4-fold interpolation filter which upsamples a signal from 0.5 MHz to 2.0 MHz. H(z) is a FIR filter with *N* order. We separate this FIR filter into four subfilters, as shown in Figure 4.2 (b). The operation of ploy phase can be expressed mathematically as

$$s_0(n) = \sum_{k=0}^{N/4-1} h_0(k) \cdot x(n-k) \tag{4.1}$$

$$s_1(n) = \sum_{k=0}^{N/4-1} h_1(k) \cdot x(n-k) \tag{4.2}$$

$$s_2(n) = \sum_{k=0}^{N/4-1} h_2(k) \cdot x(n-k) \tag{4.3}$$

$$s_3(n) = \sum_{k=0}^{N/4-1} h_3(k) \cdot x(n-k) \tag{4.4}$$

$$s(n) = \begin{cases} s_0(m), & n = 4m \\ s_1(m), & n = 4m+1 \\ s_2(m), & n = 4m+2 \\ s_3(m), & n = 4m+3 \end{cases} \tag{4.5}$$

where,

$$h_0(k) = h(4k), 0 \le k \le N/4-1 \tag{4.6}$$

$$h_1(k) = h(4k+1), 0 \le k \le N/4-1 \tag{4.7}$$

$$h_2(k) = h(4k+2), 0 \le k \le N/4-1 \tag{4.8}$$

$$h_3(k) = h(4k+3), 0 \le k \le N/4-1 \tag{4.9}$$

Suppose that N = 128 and system clock is 20 MHz, which means there are 40 clock cycles that we can use between each input. In this condition, only four MAC (Multiplier-Accumulator) are necessary for this example. Each MAC is used in the subfilters respectively. Therefore, the complexity of the digital circuit of interpolation

filters is reduced by realizing this structure.

For the hardware design, the wordlengths of the input data and the coefficients of the filters are 18-bit equally. The coefficients are required to be stored in a ROM (read only memory) and the input data is stored in a RAM (random access memory). For the sinc filter stage, the 8x interpolation can be implemented by a simple zero order hold register to hold the input data.

4.2.2 Third-Order CRFB Delta-Sigma Modulator

The hardware implementation of the delta-sigma modulator with third-order, CRFB (cascade-of- resonators, feedback form) structure and 15-level quantizer as introduced in chapter 2 will be discussed. Because all the coefficients for designing STF and NTF of the delta-sigma modulator are power of 2, it is convenient and useful to replace the multiplier by adders and shifting registers. Therefore, the complexity of the digital circuit is reduced. The 15-level quantizer means that the four MSB (most significant bit) of 18-bit signal are extracted to be the output of the delta-sigma modulator. The transfer functions of the delta-sigma modulator will also be converted into the digital circuits, as shown in Figure 4.3.

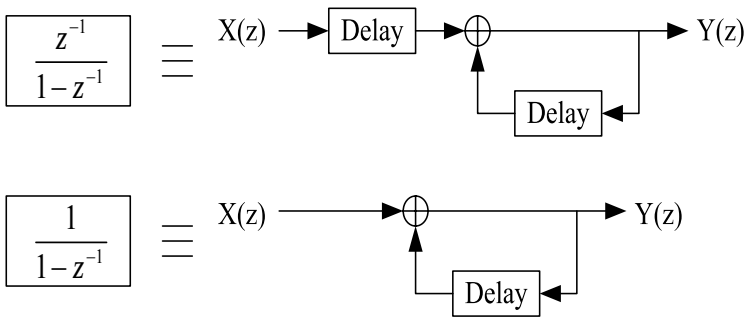


Figure 4.3 Transfer functions in the digital circuit

4.2.3 Wordlength Consideration in Arithmetic Unit

For the FIR filter used in interpolation filter, the arithmetic unit consists of multipliers, adders and accumulators. The delta-sigma modulator consists of adders, substractors and power of 2 shifters mainly. However, the wordlength of arithmetic unit and storage unit is limited, which affects the performance of the delta-sigma DAC directly. Generally, there are two types of error must be considered.

Roundoff error results from the quantizing operation. This type of error is caused by discarding the lower rank bits before storing the result. This condition occurs in multiplications or power of 2 shifters commonly. Arithmetic overflow occurs when the result of adder or substractor exceeds the permissible range of the system wordlength. This condition makes the result different from which we expect. The sign of the result value is changed generally. Therefore, the longer wordlength must be used to prevent the system from overflow in the arithmetic operation units. Then this wordlength will be truncated into the original wordlength, 18-bit.

4.2.4 Implementation with FPGA

The whole digital circuit of the designed delta-sigma DAC will be implemented with FPGA (Field Programmable Gate Array). At the beginning, the functions of digital circuit blocks are coded by Verilog, which is a hardware description language and can verify the functions easily. With using an Altera FPGA device, the Quartus II software is necessary. We must specify the type of device in which the designed circuit will be implemented in the Quartus II. An Altera FPGA device called EP1S40F780C5 is chosen from the device family, Stratix. Then the Quartus II

software is used to synthesis a circuit from the Verilog code and fit the synthesized circuit into the chosen Altera FPGA device. The timing specification can be matched by timing analysis.

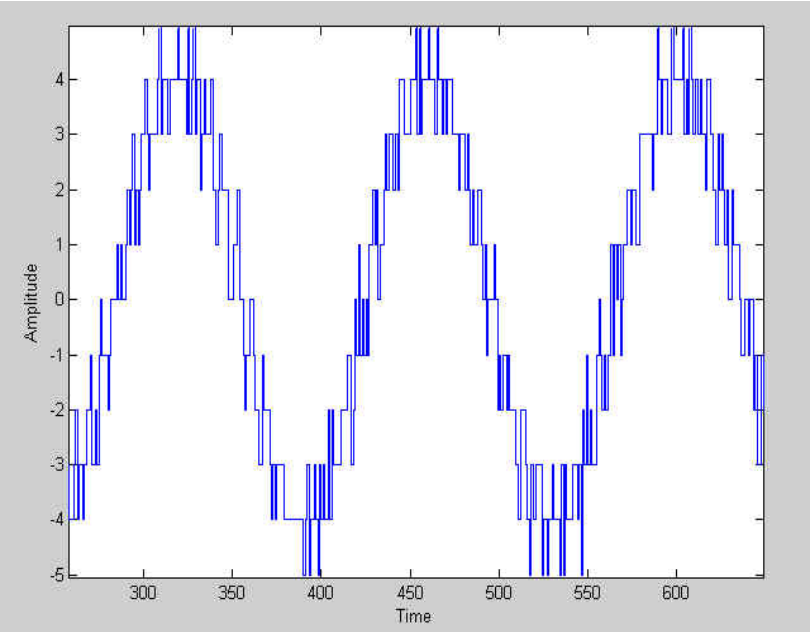


Figure 4.4 Waveform of the simulation result

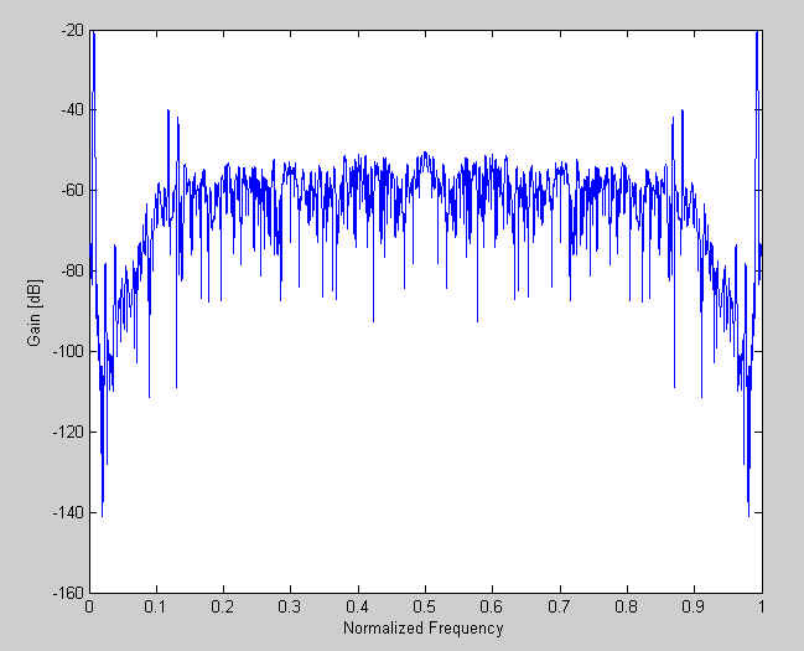


Figure 4.5 Spectrum of the simulation result

After compiling the Verilog code, several input data must be provided for verifying the functions of the designed circuit, such as a pattern of thirty input data. The waveform and the spectrum of the simulation result are shown in Figure 4.4 and Figure 4.5, respectively. We can find that the simulation result is similar to the result simulated by Matlab and the behavior of the Verilog code is verified.

Finally, a Nios development board with Stratix professional edition is adopted, which is shown in Figure 4.6. It includes Stratix EP1S40F780C5 device and JTAG headers compatible with Altera download cables, such as the USB Blaster. We can set the pin assignment of the board by using Quartus II. Then Quartus II programmer enables the FPGA device programming through the ByteBlaster cable. Therefore, the digital circuit of the designed delta-sigma DAC is implemented.

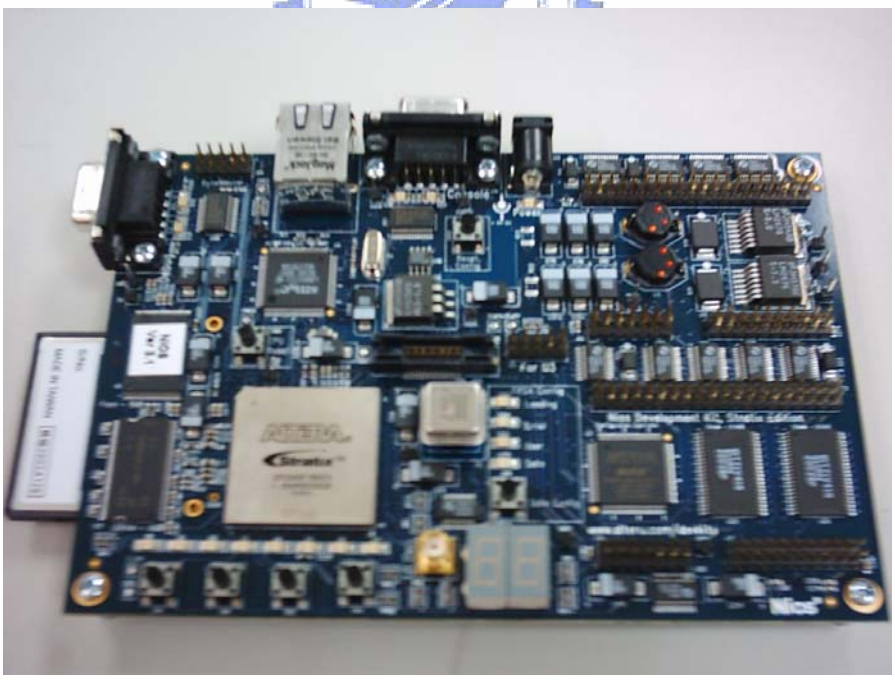


Figure 4.6 Nios development board

4.3 Analog Part Circuit

The block diagram of the analog part circuit is shown in Figure 4.7, which consists of the DCT-SC DAC and the RC lowpass filter. They are introduced in chapter 3 summarily. Here we will describe the bootstrapped switch and the opamp used in the analog circuit of the delta-sigma DAC.

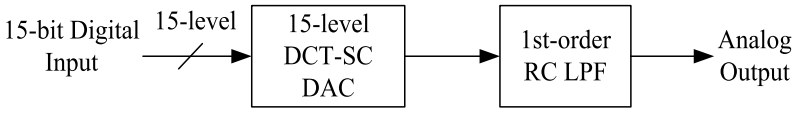


Figure 4.7 The block diagram of the analog part circuit

4.3.1 Bootstrapped Switch

The high SNR and SNDR can be achieved by the DSP (digital signal processing) technique in the digital part circuit. However, the noise and distortion in the analog device are critical for the performance of the overall delta-sigma DAC. As discussed before, we use DCT-SC technique and less analog device to decrease the noise in the analog part. In addition, a bootstrapped switch is adopted to reduce distortion [17], [18].

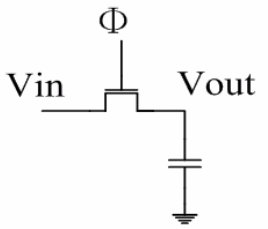


Figure 4.8 A simple sample and hold circuit

Figure 4.8 shows a simple sample and hold circuit. When Φ is high (usually Vdd), the switch is turned on and the capacitor is charged by Vin. In contrast, the switch is turned off and the capacitor will hold the sampled voltage when Φ is low. Its "on" resistance is given by

$$Ron = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{tn})} \tag{4.10}$$

where,

$$V_{tn} = V_{t0} + \gamma\left[\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right] \tag{4.11}$$

In this sampling switch, the output is limited to Vdd – Vt. When Vin > Vdd – Vt, the output voltage will be saturated by Vdd – Vt and the error voltage value will be sampled. It means a full swing range can not be obtained. In addition, the "on" resistance varies with the input signal from equation (4.10). It may cause a large harmonic distortion. The body effect in the MOS also provides nonlinearity, especially at low voltage. Therefore, the bootstrapped switch is proposed to solve the problem of full swing range and variation of the "on" resistance.

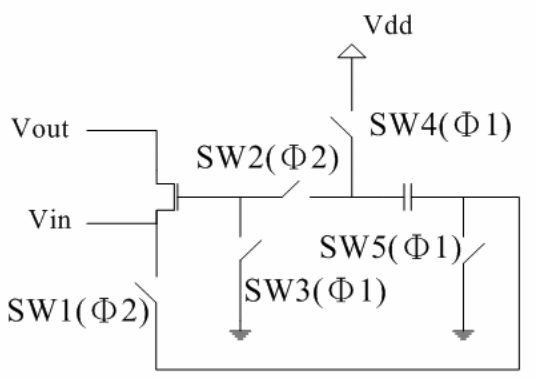


Figure 4.9 The structure of bootstrapped switch

To obtain a constant resistance, the gate to source voltage, Vgs, must be held with constant value during the "on" state. A structure of the bootstrapped switch is shown in Figure 4.9. During Φ1 state (SW3, SW4 and SW5 on), the capacitor is charged to Vdd. It will ideally act as a floating battery to bootstrap the gate voltage during Φ2 state (SW1 and SW2 on). Assuming that the input terminal of the sampling switch is source, the "on" resistance is given by

$$Ron = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{dd} - V_{tn})} \tag{4.12}$$

Clearly, it is independent of input signal to reduce harmonic distortion. Since the MOS switch is bidirectional and symmetric, the drain and source terminals may interchange, which depends on the input signal and the previous sampled voltage. The drain interchanges with the source when the input signal is larger than the previous sampled voltage. In this condition, the voltage of source terminal is previous sampled voltage, not Vin. It means Vgs is not Vdd and we can not keep Vgs constant.

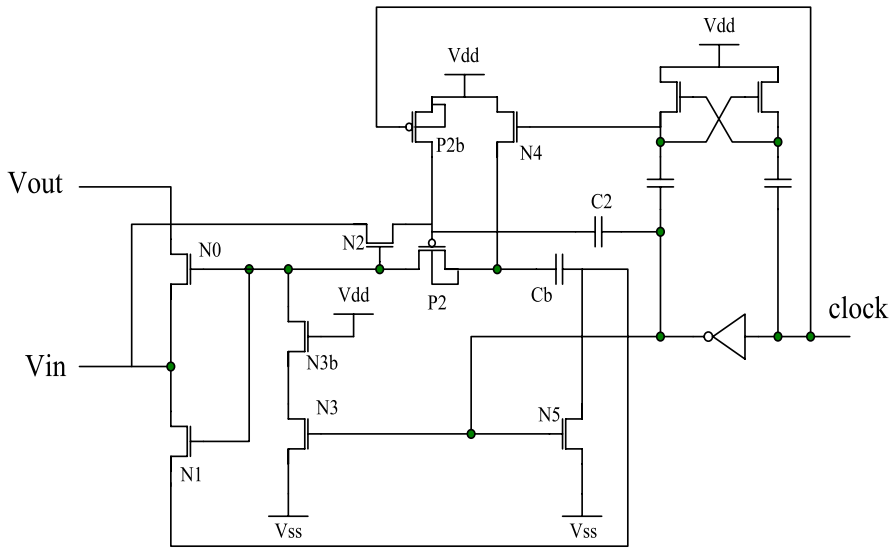


Figure 4.10 Implementation of bootstrapped switch

Figure 4.10 shows an implementation of the bootstrapped switch. The switch SW1 is implemented as a bootstrapped NMOS switch, N1. Switches SW3 and SW5 are trivial switching functions, hence they are realized as simple NMOS switches N3 and N5. However, the switch SW4 can not be implemented as a simple PMOS switch, because it would leak during Φ2 state when the bootstrap capacitor provides a potential over Vdd. Therefore, the switch SW4 is implemented as an NMOS switch N4, which is controlled by a level-shifted clock signal. Assuming Vss = 0, the level-shifted clock signal has levels Vdd and 2Vdd. The switch SW2 is implemented as a simple PMOS switch P2 because the P2's channel potential would exceed Vdd during Φ2 state, and then it is necessary to bias its bulk terminal to a voltage as high as that provided by the bootstrap capacitor at least. The simple option is to connect the bulk terminal to the source terminal, as shown in Figure 4.10.

Because the gate oxide of N3 and P2 is subject to the voltage which exceeds the supply voltage, it may cause error in the foreseeable future. N3 is protected by including the cascode device NMOS N3b. The gate oxide of P2 is protected by operating P2 with a constant overdrive. N2 is included to be a bootstrapped switch which connects Cb between the gate and source terminals of P2, hence P2 is also bootstrapped. By using the small capacitor C2 to initiate the switch's on state Φ2, the two interconnected bootstrap loops would not lock automatically. P2 is turned off and C2 is precharged by the simple PMOS switch P2b.

In the 15-level DCT-SC DAC, the fifteen bootstrapped switches are adopted in the sampling switch for sampling the input voltage from the output of FPGA. All the other switches in the DCT-SC DAC are realized by complementary switches. The effect on the bootstrapped switch can be observed by the comparison between Figure

4.11 and Figure 4.12. The harmonic distortion is decreased about 20 dB by using the bootstrapped switch.

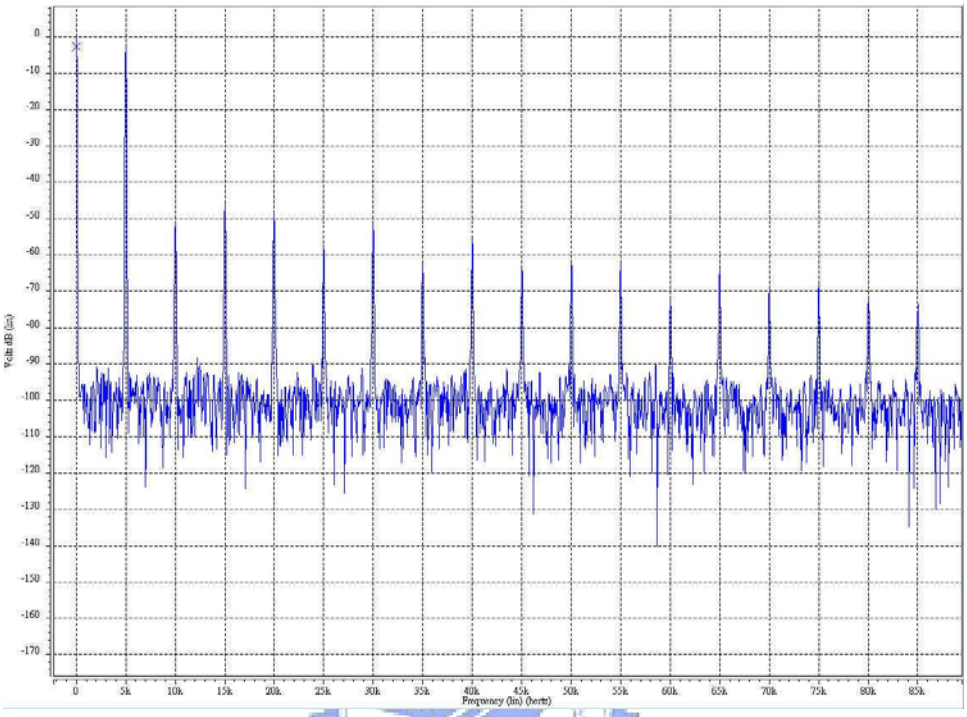


Figure 4.11 Using complementary switches in sampling switch

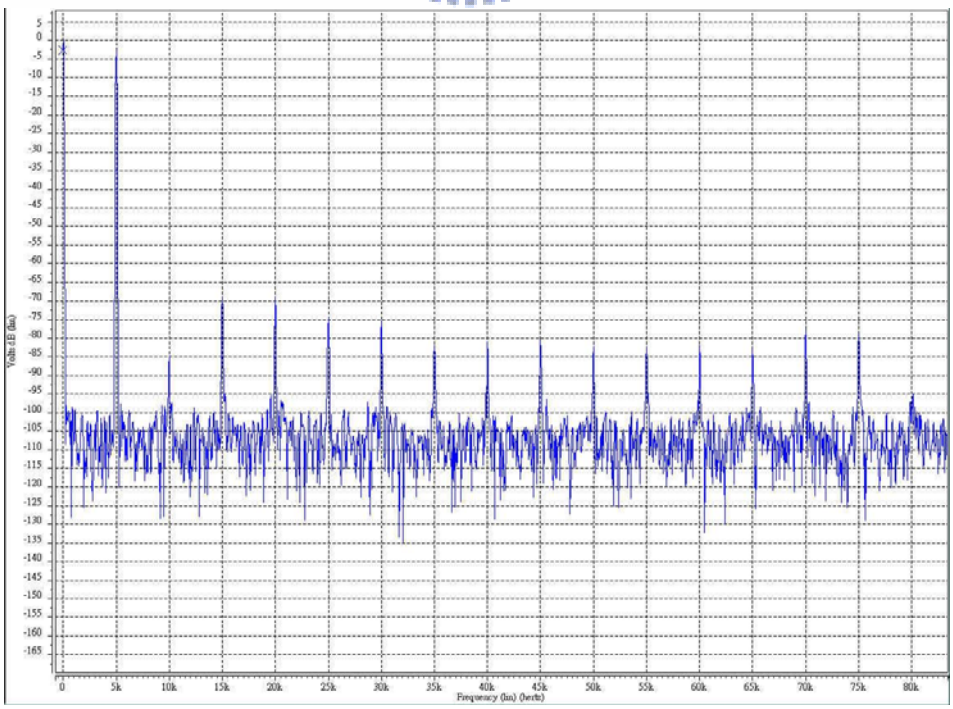


Figure 4.12 Using bootstrapped switches in sampling switch

4.3.2 Opamp Design

A single-ended opamp with two stages is adopted, which is shown in Figure 4.13 [19], [20]. The input stage of the opamp is class-A which allows designing bandwidth and noise properly. A large size of the input device is used to reduce flicker noise. A class-AB output is adopted because it can increase the slew rate. Then the slew-rate-induced distortion is reduced consequently.

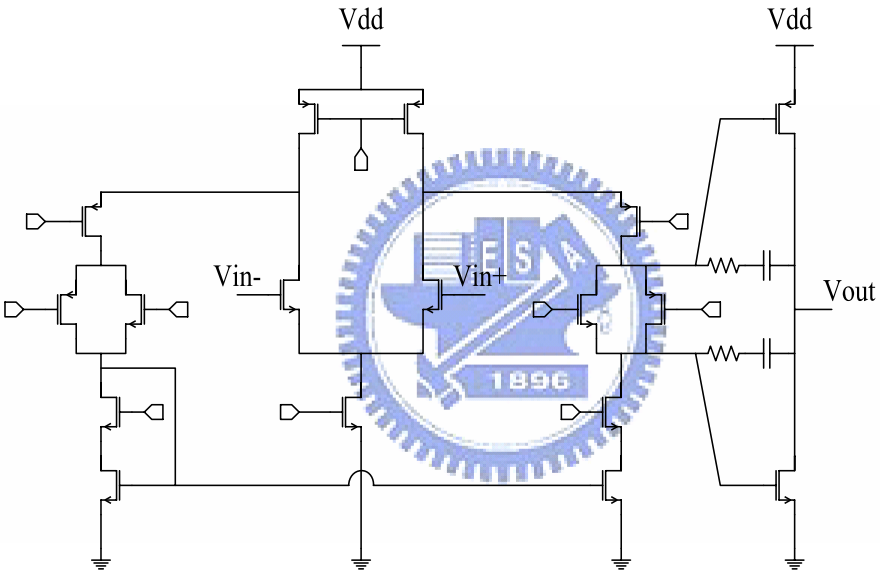


Figure 4.13 Scheme of the two-stage single-ended opamp

The single-ended structure of the SC filter can avoid the CMFB (common-mode feedback) implementation. In a fully differential SC circuit, it must use a CMFB circuit realized with SC technique because of the large output swing. The CMFB circuit may be a critical issue in a fully differential structure, since it requires recharging discharged capacitors at any clock cycle. This will cause spikes and, sometimes, slew rate which increases THD (total harmonic distortion). The opamp is designed symmetrically and the floating battery duplicated in the mirror branch is

necessary for the class-AB output stage. The simulated AC result of the opamp is shown in Figure 4.14 and the specification of the opamp is listed in the Table 4.1.

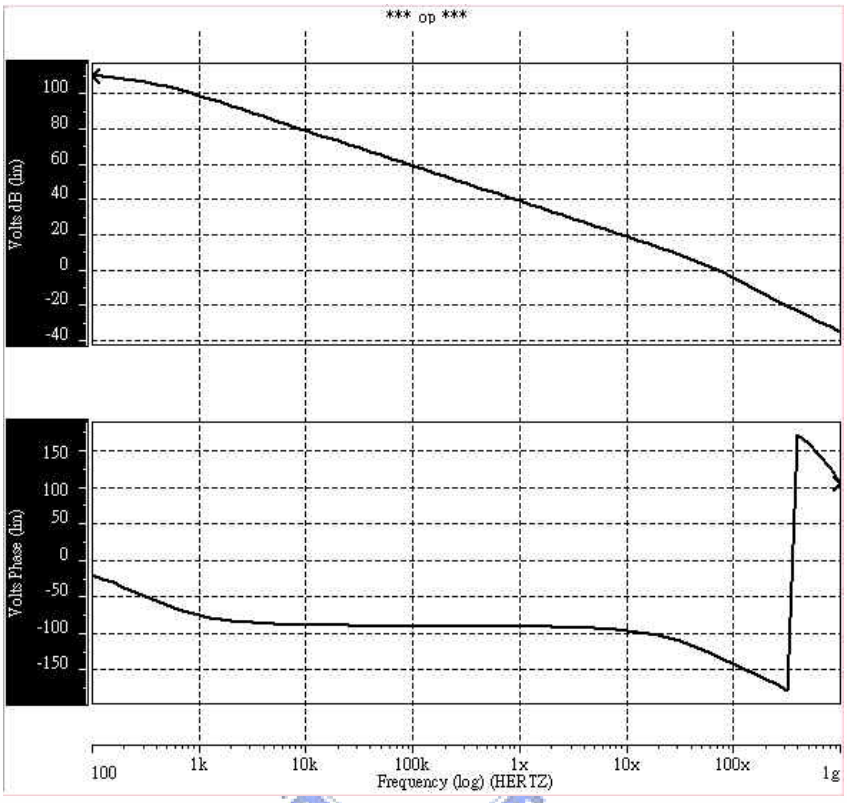


Figure 4.14 Simulated AC result of the opamp

DC Gain	110dB
Phase Margin	47.79°
Unit Gain Bandwidth	71.707MHz
Supply Voltage	1.8V
Power Dissipation	1.8224mW
Process	TSMC 0.18μm 1P6M Process

Table 4.1 Specification of the opamp

The whole analog part circuit is implemented with the standard TSMC 0.18μm CMOS 1P6M process. It is laid out on a 0.92×0.919 mm^2 die that including the pad frame. The layout of the analog part circuit of this designed delta-sigma DAC is shown in Figure 4.15. The core circuits are located at the center of the layout. A guard ring is placed around the circuits, which is connected to ground to absorb the noise in the substrate. The output spectrum of the analog device with a 1 kHz, -60 dB sine-wave input signal is shown in Figure 4.16, which can approximate dynamic range of delta-sigma DAC. The performance of the designed delta-sigma DAC is summarily presented in Table 4.2.

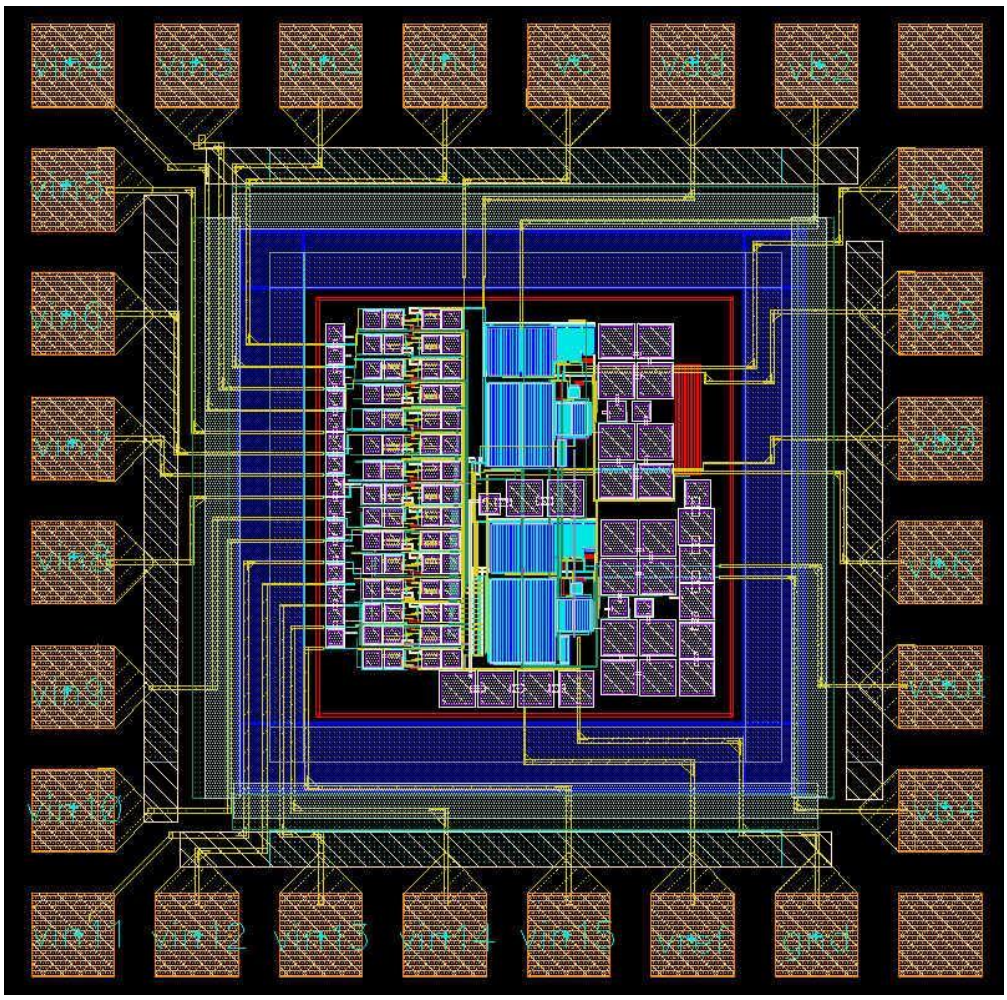


Figure 4.15 Layout of the analog part circuit

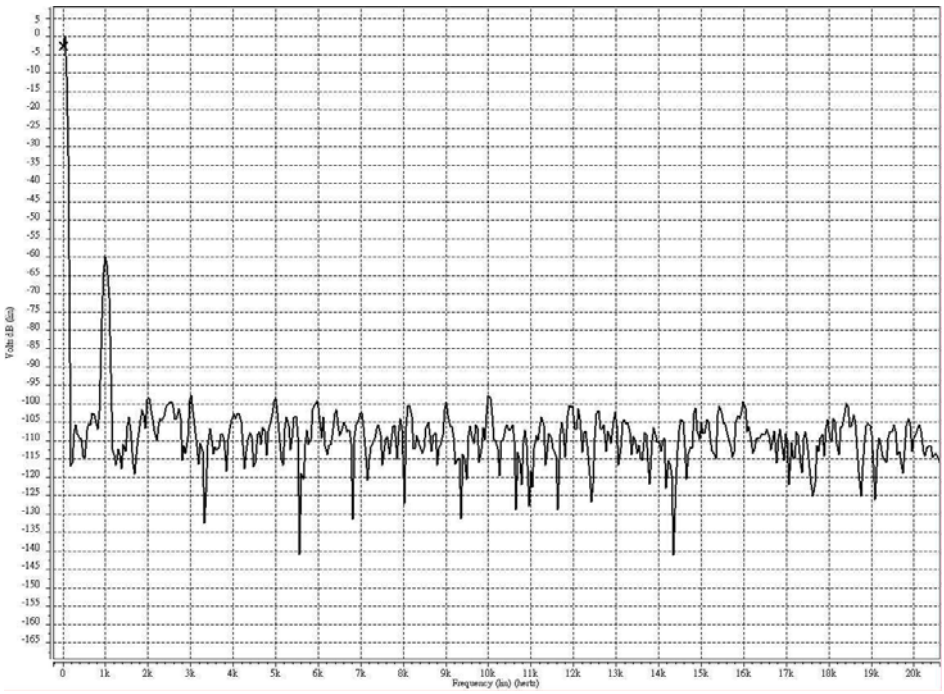


Figure 4.16 Output spectrum with 1 kHz, -60 dB sine-wave input signal

Power Supply	Digital=1.8V Analog=1.8V
Power consumption	Analog=3.145mW
Cell size	Analog=0.846mm^2
Operating Frequency	2.8224 MHz
Output Swing	0.8Vpp
Dynamic range	92dB
Process	TSMC 0.18μm 1P6M

Table 4.2 The performance summary

Chapter 5

Test Setup and Experimental Results

5.1 Introduction

The digital part of the designed delta-sigma DAC is implemented with FPGA. In addition, the analog part is laid out by using the TSMC 0.18μm CMOS process with one poly and six mental. In this chapter, we present a testing environment to combine with the digital and the analog circuits, and then measure the characteristics of the whole delta-sigma DAC. The testing environment includes the component circuits on the DUT (device under test) board and the instruments. Finally, the measured results will also be presented.

5.2 Testing Circuits

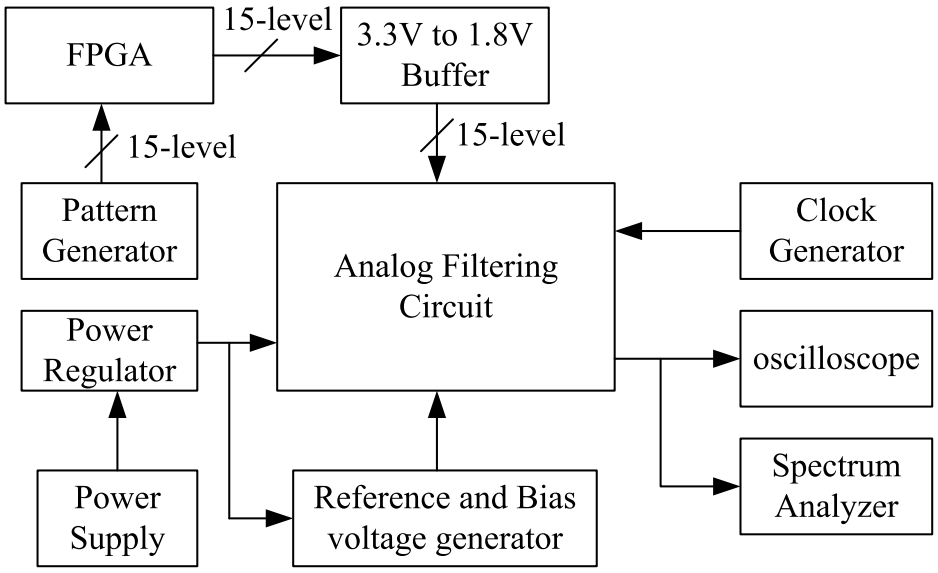


Figure 5.1 Testing setup

The testing setup used to measure the performance of the designed delta-sigma DAC is shown in Figure 5.1. It consists of pattern generator, FPGA, power regulator, clock generator, oscilloscope, and spectrum analyzer. The interface between FPGA and the analog filtering circuit are fifteen buffers – SN74LVC244, which adopted to transfer the digital signal level 3.3V into 1.8V with the supply voltage 1.8V. The reference and bias voltages are all created by voltage division with the combination of fixed resistors, variable resistors, and the voltage generated by power regulator. It is important to make sure that the clock signal of the FPGA and the chip are synchronized.

The input signal to the FPGA is provided by the pattern generator, Agilent 67102B. The photograph of the pattern generator is shown in Figure 5.2. The clock signal of the system is generated with a signal generator, Agilent 33250. The photograph of the clock generators are shown in Figure 5.3. The output signal of the DUT is observed with the oscilloscope, Agilent S4832D and the spectrum analyzer. They are shown in Figure 5.4 and Figure 5.5, respectively.

Figure 5.2 Pattern generator, Agilent 67102B

Figure 5.3 Signal generator, Agilent 33250

Figure 5.4 Oscilloscope, Agilent S4832D

Figure 5.5 Spectrum analyzer

5.2.1 Power Regulator

The analog power supply is generated by the application of the adjustable regulator, LM317, which is shown in Figure 5.5. The resistor R1 is a fixed resistor and resistor R2 is a precise variable resistor. The capacitor C1 is used to improve the ripple rejection and capacitor C2 is the input bypass capacitor. The output voltage of the regulator can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) \cdot I_{ADJ} \cdot R2 \qquad (5.1)$$

where I_{ADJ} is the DC current flowing out of the adjustment terminal ADJ of the regulator. In addition, the resistor R1 can use the low temperature coefficient of the metal film resistor to get the stable output voltage.

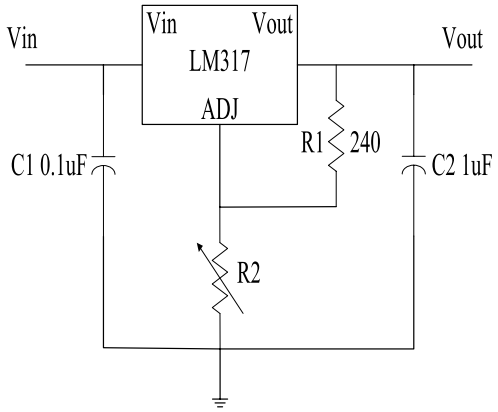


Figure 5.6 Power supply regulator

5.3 The Package and Pin Configuration

Figure 5.7 shows the die photomicrograph of the experimental analog filter of the delta-sigma DAC and Figure 5.8 shows the photograph of the testing DUT board. Figure 5.9 presents the pin configuration and lists the pin assignments of the experimental analog filter of the delta-sigma DAC.

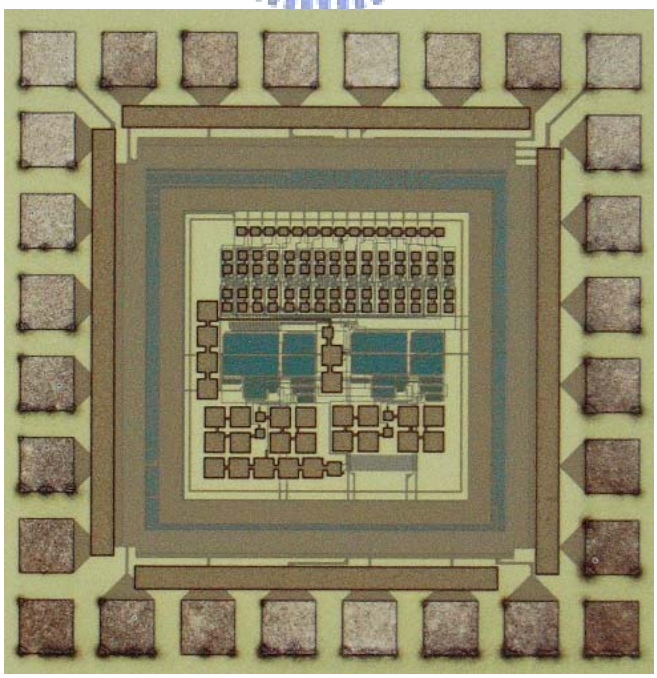


Figure 5.7 Die photomicrograph of the analog filter of the delta-sigma DAC

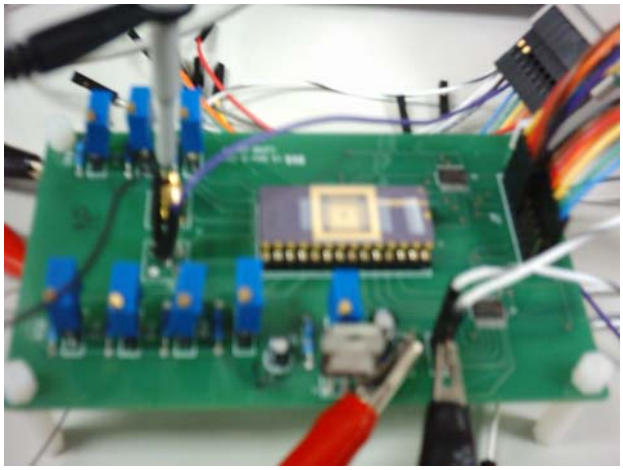
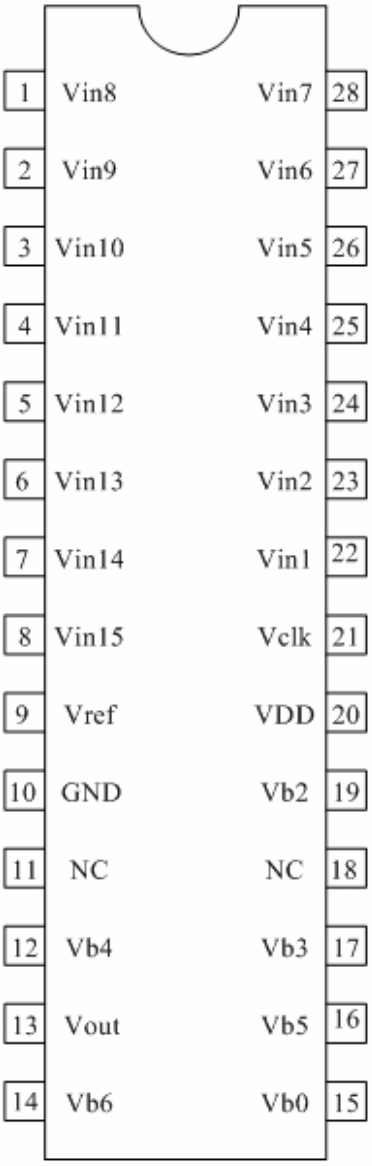


Figure 5.8 The photograph of the testing DUT board



Pin	Name	I/O	Describe
1	Vin8	In	Digital data input
2	Vin9	In	Digital data input
3	Vin10	In	Digital data input
4	Vin11	In	Digital data input
5	Vin12	In	Digital data input
6	Vin13	In	Digital data input
7	Vin14	In	Digital data input
8	Vin15	In	Digital data input
9	Vref	In	Reference voltage
10	GND	In	Ground
11	NC	-	No connection
12	Vb4	In	Bias voltage
13	Vout	out	Analog data output
14	Vb6	In	Bias voltage
15	Vb0	In	Bias voltage
16	Vb5	In	Bias voltage
17	Vb3	In	Bias voltage
18	NC	-	No connection
19	Vb2	In	Bias voltage
20	VDD	In	Power supply
21	Vclk	In	System clock input
22	Vin1	In	Digital data input
23	Vin2	In	Digital data input
24	Vin3	In	Digital data input
25	Vin4	In	Digital data input
26	Vin5	In	Digital data input
27	Vin6	In	Digital data input
28	Vin7	In	Digital data input

Figure 5.9 (a) Pin configuration diagram and (b) Pin assignment

5.4 Experiment Results

The analog filter of the delta-sigma DAC is fabricated in 0.18μm CMOS process. The chip is powered by the 1.8 V supply and connected with the FPGA. A 1 kHz digital sine wave with 18 bits is applied to the FPGA with the sampling rate, 44.1 kHz. The analog output signal of the DUT is observed by the oscilloscope and collected by the spectrum analyzer. The output spectrum with a 0 dB sine wave input is shown in Figure 5.10. This spectrum is dumped from the spectrum analyzer. The graph in this figure indicates the spurious free dynamic range (SFDR) is about -60dB.

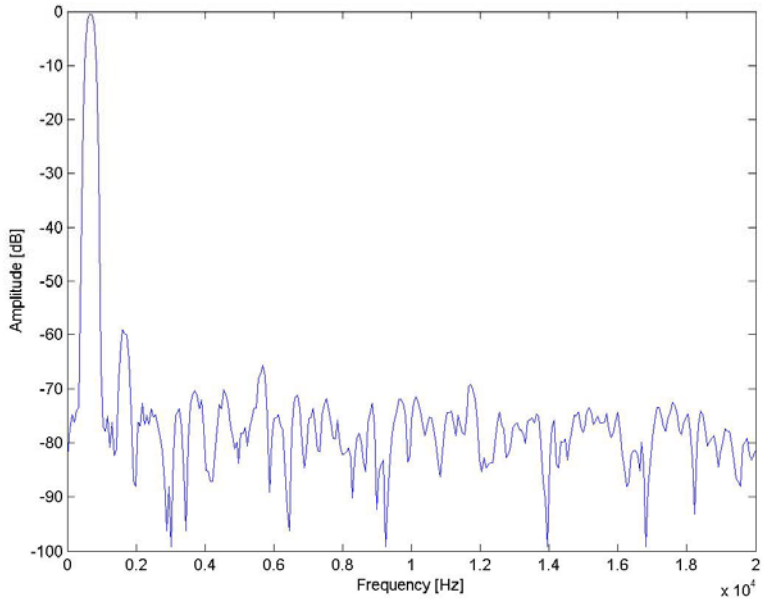


Figure 5.10 Output spectrum for a 1 kHz, 0 dB signal

The measured signal-to-noise plus distortion ratio (SNDR) versus input levels of the design delta-sigma DAC is shown in Figure 5.11. We can obtain the peak SNDR is 75.0927dB and the dynamic is 58.7096dB from this graph. Table 5.1 summaries the measured results of the delta-sigma DAC.

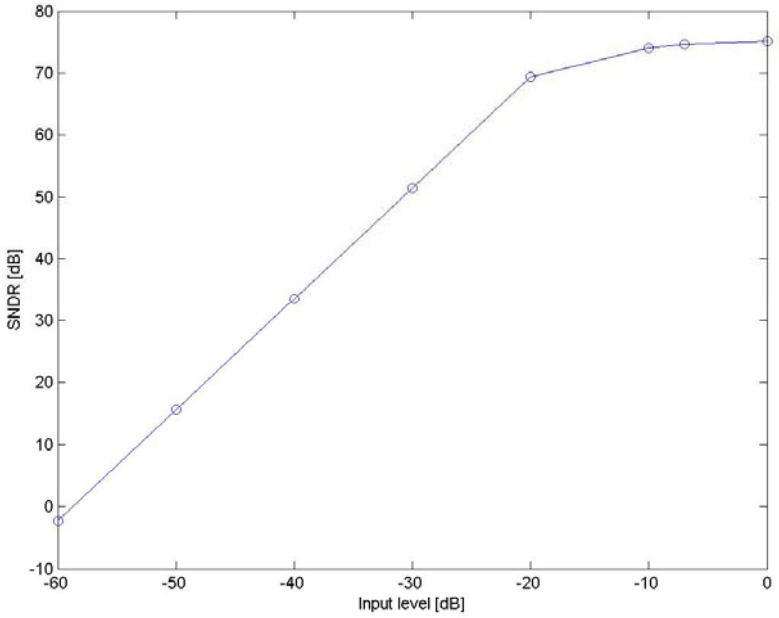


Figure 5.11 The measured SNDR versus input level for a 1 kHz sine wave

Table 5.1 Summary of measured results

Parameters	Measured Results
Supply Voltage	1.8V
Power consumption	Analog=3.145mW
Cell size	Analog=0.846mm^2
Operating Frequency	2.8224 MHz
Output Swing	0.88Vpp
Peak SNDR	75.0927dB @ 0dB
Dynamic range	58.7096dB
Process	TSMC 0.18μm 1P6M

Chapter 6

Conclusions

6.1 Conclusion

In this research, a 1.8V, 18-bit delta-sigma DAC with 44.1 kHz sampling rate is introduced in a standard CMOS technology. For the multi-level quantization, the delta-sigma modulator topology and the DWA implementation are presented. Analog circuit techniques for low-power and low-distortion are also reported. The DCT-SC DAC technique results in the reduction of power dissipation, smaller sensitivity to clock jitter, and reduced distortion. The implementation of the bootstrapped switch can also reduce the harmonic distortion. It is important to achieve the above analog circuit with a single-end output signal, because it does not allow to take advantage of the CMFB structure.

6.2 Future Work

In order to achieve the better performance of the delta-sigma DAC, we should design the analog circuits to reduce the noise, distortion, and power dissipation. It is because the noise and operating voltage of the digital part can be decreased easily. However, the area of the digital circuits in this research is too large to be integrated in a chip. If we continue to research on the same topic, the reduction of the digital part area and the design of the higher dynamic range of the delta-sigma DAC will be the most important purpose for the future work.

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