國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用雙倍取樣技術之10位元200百萬赫茲互補式金氧半導管式類比數位轉換器

10-Bit 200MHz Double-Sampling Pipelined Analog-to-Digital Converter

研究生：何俊達

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中 華 民 國 九十五 年 十 月

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電 信 工 程 學 系 碩 士 班

碩 士 論 文

A Thesis

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應用雙倍取樣技術之 10 位元 200 百萬赫茲互補式金氧半導管式類比數位轉換器

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摘要

導管式類比數位轉換器固有高轉換速度的特性，並且普遍使用在寬頻通訊系統以及影像系統。然而隨著解析度與轉出率的提高，相對的功率消耗以及需要的晶片面積也變得越大。因此，雙倍取樣的技術能夠提供加倍取樣率卻不至於使功率消耗及需要面積倍增的一種方法。

藉由 TSMC 0.18um 1P6M CMOS 製程，我們已經完成一應用雙倍取樣技術之 10 位元 200 百萬赫茲互補式金氧半導管式類比數位轉換器的模擬。此一類比數位轉換器包括前端的取樣保持電路、8 級串接的轉換器（每級 1.5 位元）以及最後一級的 2 位元的快閃式轉換器。所有的類比電路皆以全差動輸入設計，輸入為 2 倍峰對峰的輸入訊號，並且電源供應電壓為 1.8 伏特。在每一級的運算放大器是由兩個操作的路徑共用，並且放大器交互地處理這兩個路徑所獲得的取樣訊號。不但每一級的運算放大器可以在兩個路徑上共用，子類比數位轉換器也能夠在兩個路徑上共同使用。如此一來，可使得取樣更加的有效率並且增加導管式類比數位轉換器的轉換速率。

應用雙倍取樣技術之 10 位元 200 百萬赫茲互補式金氧半導管式類比數位轉換器已經由晶片中心(CIC)提供的 TSMC 0.18um 1P6M CMOS 製程下線。此一導管式類比數位轉換器在時脈為 100 百萬赫茲，取樣頻率為 200 百萬赫茲/取樣數並供以 1.8 伏特的電源電壓，共消耗了 103 毫瓦功率。晶片面積為 1.134*1.380 mm^2。模擬的差動非線性誤差(DNL)以及積分非線性誤差(INL)分別為±0.75 LSB 和

±0.95 LSB。並且當輸入訊號為 1 百萬赫茲弦波時，訊號對雜訊及失真比(SNDR)約為 56dB。

10-Bit 200MHz Double-Sampling Pipelined Analog-to-Digital Converter

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Abstract

Pipelined analog-to-digital converters (ADCs) have intrinsic high-speed characteristics and are commonly used in wideband communication and video systems. However, with the higher resolution and throughput rate the power consumption and the required area are getting larger. Therefore, the double-sampling technique provides a method applied to the pipelined ADC to duplicate the sampling rate without consuming two times of power and area.

The 10-bit 200MS/s double-sampling pipelined analog-to-digital converter was simulated by TSMC 0.18um 1P6M CMOS process. It consists of one front-end SHA, eight cascaded 1.5-bit stages, and a final 2-bit flash converter in the last stage. All analog circuits are fully differential with a 2Vpp input signal and 1.8V power supply. The operation amplifier in each stage is shared between the two paths and active for one of both paths alternately. Not only the operation amplifier in each stage is shared, but sub-ADC is common to both paths. As a result, it makes sampling more efficient and increases the throughput rate of the pipelined ADC.

The 10-bit 200MS/s double-sampling pipelined analog-to-digital converter was finally implemented by TSMC 0.18um 1P6M CMOS process. The pipelined ADC

dissipates 103mW at a 100MHz clock rate and a 200MS/s sampling rate with 1.8V supply voltage. The chip area is 1.134*1.380 mm^2. The simulated differential nonlinearity (DNL) and integral nonlinearity (INL) are ±0.75 LSB and ±0.95 LSB, respectively. And the peak SNDR about 56dB for an input signal of 1MHz sine wave.

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Chapter 1

Introduction

1.1 Motivation for the Thesis

Data converters are dominant in modern data and communication systems where increasingly complex processing of analog signals is performed digitally. To achieve the more effective performance, signal processing trends to digital domain. As the result of low power consumption and cost reduction, digital signal processing (DSP) is becoming more and more important. However, in many applications the input and output signals of the system are inherently analog, but the signal processing in the system is digital. Therefore, analog to digital converters (ADC) and digital to analog converters (DAC) are the necessary interfaces in the system. These interfaces achieve the digitization of the received waveform subject to a sampling rate requirement of the system and transform to analog signal in the output after signal processing. However perfect the digital or analog circuits in the system design, they actually need better data converters to perform much well.

There are many applications for the data converters, such as High-Definition Television (HDTV), Multimedia, Software Radio Receivers, Wireless communications, Radar Systems, and Cable Modems. In order to make the system more accurate, reliable, storable, higher yields, the interface using ADCs has become a key component and plays an important role in the system.

In wireless communication systems the trend to boost data rates is based on

employing wider bandwidths and a higher signal-to-noise ratio. High data rates imply wide bandwidths, while a continuous growing complexity of the modulation schemes and the desire for more flexible receivers push the boundary between analog and digital signal processing closer to the antenna. Because of these trends, there is an urgent need for data converters with increasing conversion rates and resolution. At the same time, the increasing integration level leads to systems with a smaller number of chips, the ultimate goal being a single chip solution, the system on a chip (SoC). Data converters are inherently mixed signal circuits and face the challenges on a small scale.

The main challenges in data converter design are decreasing supply voltage, short channel effects in MOS devices, mixed signal issues, the development of design and simulation tools, and testability. In analog to digital converters, they need to be met at the same time as the requirements for the sampling linearity, conversion rate, resolution, and power consumption are being tougher.

In mixed signal-model ADC interfaces, there is some architecture for several kinds of application. For high speed application, flash and folding ADC architectures are useful. For higher resolution sigma-delta architectures is suitable but it is useful in lower sampling rate, whereas pipeline architecture has been widely employed as it properly manages the trade-off between high conversion rate and resolution.

In this research an attempt has been made to design a 10-bit 200MS/s pipelined ADC with reduced power dissipation by using double sampling technique. The pipelined ADC has been implemented with a standard TSMC 0.18μm CMOS 1P6M process. Here the double sampling technique is used in the front-end of

sample-and-hold amplifier (SHA) and the subsequent stages. Two sets of capacitors are used to sample and hold the signal alternately in two non-overlap phases. Two parallel paths provided by the sets of capacitors introduce parallelism and increases the speed of conversion.

1.2 Thesis Organization

This thesis is organized into six chapters.

Chapter 1 briefly introduces the motivation of the thesis.

Chapter 2 describes the concepts of analog-to-digital conversion and performance parameters used to characterize ADCs. Then, several ADC architectures are introduced and the evolution of the pipelined ADC is presented.

Chapter 3 concentrates on the characteristics of the pipelined ADC. The nonlinearity of components is also need to take into account. Finally, the technique of double sampling is introduced, and it will apply to our design in order to speed the throughput rate of the pipelined ADC.

Chapter 4 illustrates the design and implementation of the double-sampling pipelined ADC. Circuit designs and the behavior model of the key blocks will be introduced in detail. Among them are the operational amplifier, the common mode feedback, the comparator, the bootstrapped switch, the sample-and-hold amplifier (SHA), the 1.5-bit architecture, and the 2-bit flash converter. Then, the transistor level simulated results of each circuit are presented. Finally, the simulation of the whole

pipelined ADC and its layout and floor plan are presented.

Chapter 5 presents the testing environment, including the component circuits on the DUT (device under test) board and the instruments. Then, the double-sampling pipelined ADC described in Chapter 4 is fabricated in a standard TSMC 0.18μm CMOS Mixed-Signal process and the measured results of this chip are summarized.

Finally, Chapter 6 is the conclusions of this work. Some suggestions and improved recommendations are proposed for the future work.

Chapter 2

Fundamentals of Analog-to-Digital Converter

2.1 Introduction

An analog-to-digital converter quantizes an analog signal into digital code at discrete time points. The performance of A/D converters depends on static specifications and dynamic specifications. This chapter first introduces the concept of the analog-to-digital converters and presents the static and dynamic performance parameters for A/D converters. Second, some of the prominent ADC architectures are introduced and the characteristics of these ADCs are described. Third, the technique of double sampling is discussed and the behavior model of the pipelined A/D converter with the double sampling technique is established by simulink.

2.2 The Concept and Performance of A/D Converters

An analog to digital converter (ADC) is a device converting analog signals into digital codes to link the real world and the digital systems. Figure 2.1 shows a block diagram of a traditional A/D converter at Nyquist rate. A low pass filter called an anti-aliasing filter is necessary to avoid the aliasing of higher frequency signals back into the baseband of ADC. The low pass filter is followed by a sample-and-hold amplifier (SHA) that maintains the signal in discrete time. The conversion is accomplished by a quantizer that segments the reference into subranges. Typically,

there are 2^N subranges, where N is the number of digital output codes. Finally, the digital encoder is allowed to encode the corresponding digital bits according to the reference of subranges.

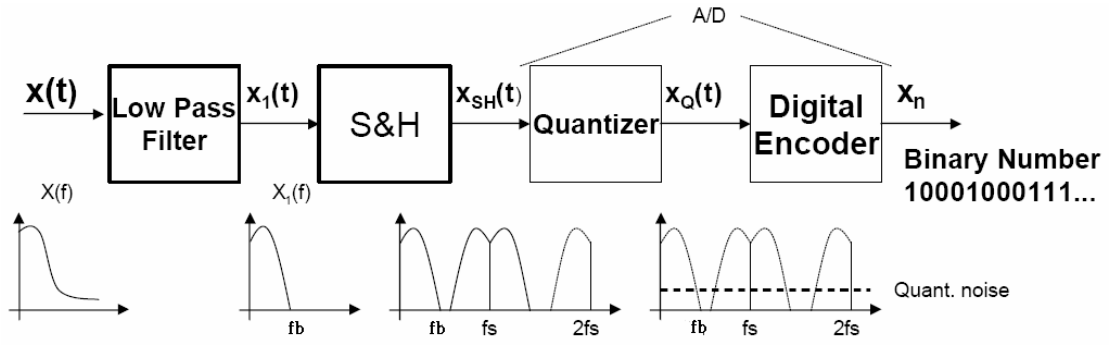


Figure 2.1 block diagram of an ADC

The frequency response of the ADC is also illustrated in Figure 2.1. At first we define the bandwidth of the signal, fb, and the sampling frequency, fs. The spectrum of the input signal is aliased at the sampling frequency. If the bandwidth of the signal, fb, is above 1/2fs, the spectrum of the signal will overlap with that of its image. It will result in the unrecoverable area around the frequency 1/2fs. This concept is formalized in the Nyquist rate, which states that the sampling frequency must be at least twice the bandwidth of the signal in order for the signal to be recovered from the samples. The types of ADCs operate in the concept of the Nyquist rate are called Nyquist analog-to-digital converters. [01]

Figure 2.2 illustrates the ideal conversion characteristic of a 4-bit ADC. The transition voltage can be written as

$$V_{tn} = \frac{V_{ref}}{2^N} \cdot n, \quad n \in \left\{0,1,2,...,2^N - 1\right\}, \tag{2.1}$$

where N and V_{ref} represent the bit numbers and the applied reference voltage respectively. The quantization step (V_{LSB}) is the difference of two transition voltages and it can be written as

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.2}$$

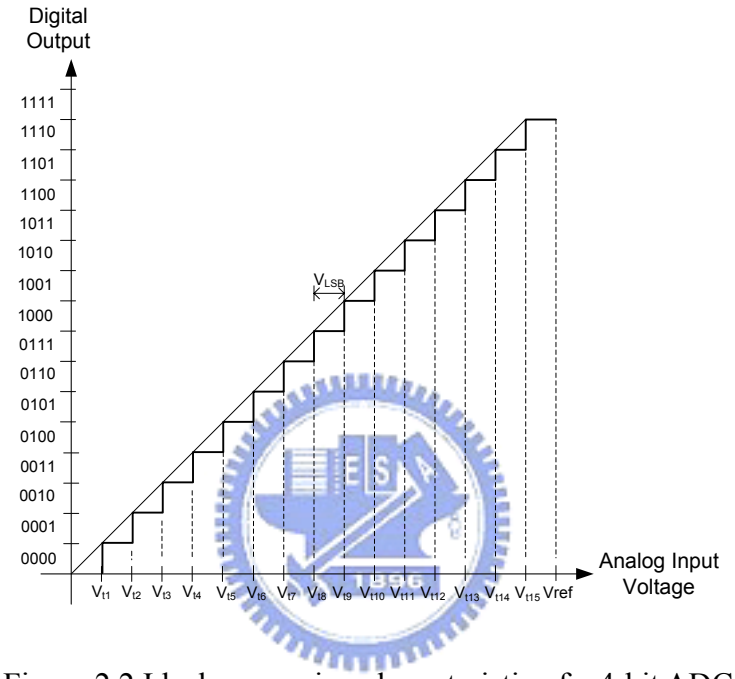


Figure 2.2 Ideal conversion characteristic of a 4-bit ADC

2.2.1 Static Specifications

The static error of an A/D converter is based on the input-output characteristics shown below. Static parameters are directly related with a comparison between the ideal and the expected conversion characteristics. These static characteristics that define the static performance of A/D converters are offset error, gain error, integral nonlinearity (INL), and differential nonlinearity (DNL). These errors will cause inaccuracy output digital codes converted by the ADC. As in most applications these errors really impact the performance of ADC, some of calibration techniques have

been proposed. We will discuss some calibration methods applying in the A/D converter later.

2.2.1.1 Offset Error

The offset error is the deviation between the ideal transition voltage and the actual transition voltage relatively to the quantization step, V_{LSB}. For an ADC with offset error, the ideal characteristic line is shifted horizontally. Offset error is illustrated in Figure 2.3.

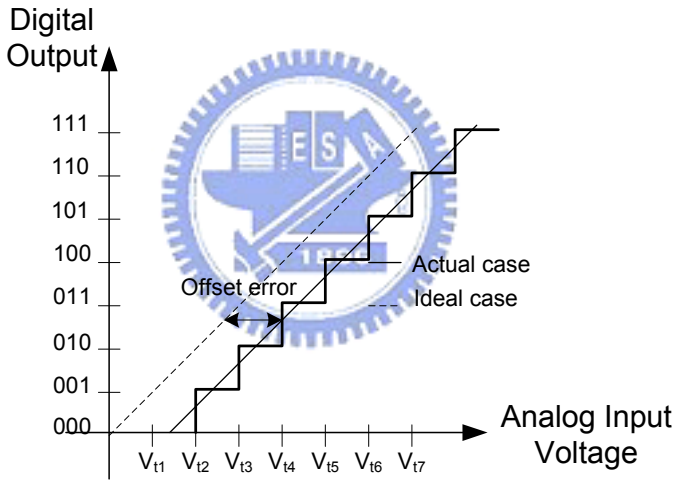


Figure 2.3 illustrates Offset Error.

2.2.1.2 Gain Error

The gain error can be defined as the ratio between the slopes of the actual and other the ideal straight lines defined using the two endpoints of both conversion characteristics. Gain error can be measured as the horizontal difference in LSBs between actual and ideal finite resolution characteristics at highest digital code. Gain

error is illustrated in Figure 2.4. [02]

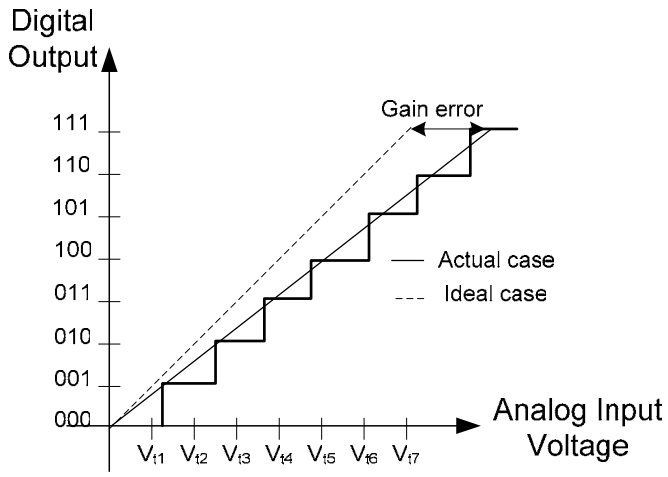


Figure 2.4 Illustrates Gain Error

2.2.1.3 Differential Non-Linearity Error (DNL)

Differential non-linearity error is defined as the difference between two adjacent analog signal values compared to the step size of converter generated by transitions between adjacent pairs of digital code numbers over the whole range of the converter. In other words, DNL is the value compared the actual step size with the ideal step size voltage ($1LSB = \frac{V_{ref}}{2^N}$). To achieve a maximum DNL error of ± 0.5 LSB defined at the resolution level of the ADC (N-bit) , the transition voltages should be within 0.5 to 1.5 LSB at N-bit level.

If the maximum DNL error is larger than -1 LSB at N-bit level, it is guaranteed that the ADC is monotonic, which means that the digital output always increases or is kept constant as the input increases. If DNL error is larger or equal to 1 LSB, it guarantees a non-monotonic transfer function with more missing codes.

DNL error is defined as follows:

$$DNL(n) = \frac{V_{t(n+1),actual} - V_{t(n),actual} - 1LSB}{1LSB}. \quad (2.3)$$

2.2.1.4 Integral Non-Linearity Error (INL)

INL error is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset. The integral non-linearity error (INL) should not deviate more than ±1/2 LSB of the straight line drawn. INL is also specified after the static gain error has been removed. It is defined as follows:

$$INL(n) = \frac{V_{t(n),actual} - V_{t(n),ideal}}{1LSB}. \quad (2.4)$$

Figure 2.5 displays examples of DNL and INL errors in 3-bit ADC . [02] [03]

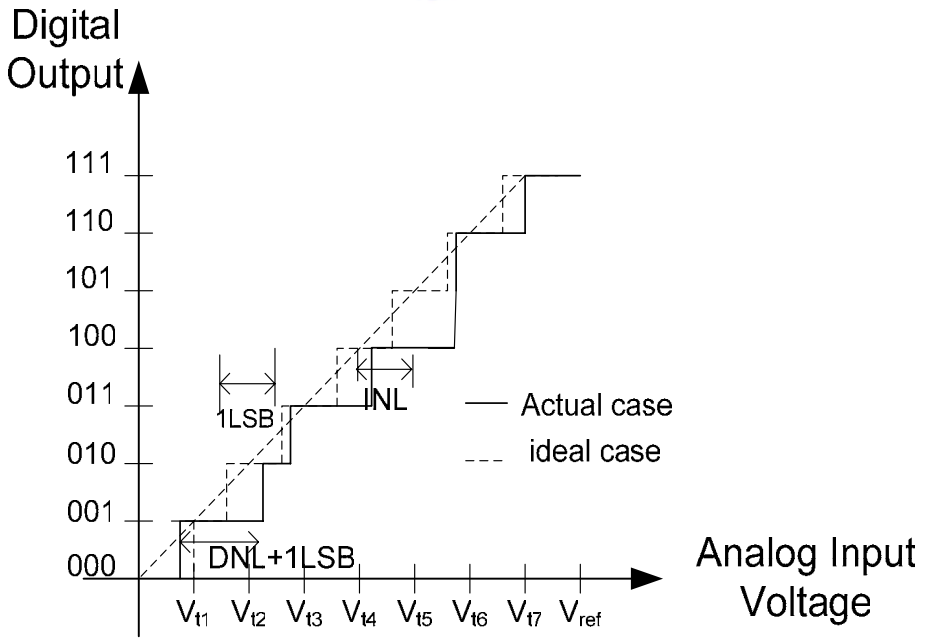


Figure 2.5 DNL and INL errors in a 3-bit ADC

2.2.2 Dynamic Specifications

Dynamic performance parameters depend on the resolution, the sampling frequency and the input signal frequency of an A/D converter and include information about dynamic linearity, distortion, sampling time uncertainty, noise and settling time errors. The most commonly analysis are related to the spectrum of the output signal. With the input of full-scale sine wave, the resulting spectral analysis is rich in information about the dynamic behavior of the ADC.

2.2.2.1 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the signal power, corresponding to the maximum amplitude of the signal component, and the noise power present at the output of ADC. The SNR includes the quantization noise and other circuits noise excluding any harmonic component of the input signal.

Assuming that the quantization error of an ADC is evenly distributed, the rms value of the generated noise signal, $V_{Q(rms)}$,is given by

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.5}$$

where V_{LSB} is the quantization step, and N is the resolution of the ADC. Assuming V_{in} is a sinusoidal waveform between 0 and V_{ref} , and considering only the ac power of the signal, the SNR is given by

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(\sqrt{\frac{3}{2}}2^N\right) \qquad (2.6)$$

$$= 6.02N + 1.76 \text{ dB}$$

2.2.2.2 Signal-to-Noise and Distortion Ratio (SNDR)

Signal-to-Noise and Distortion Ratio is defined as the ratio of the signal power to the total noise power including all spurs and harmonics of the ADC. SNDR is measured for a sinusoidal input and is normally represented as a function of the frequency of the input signal. [04]

2.2.2.3 Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range is defined as the ratio between the maximum rms amplitude of the signal and the rms value of the largest distortion component in a specified frequency range. SFDR indicates the usable dynamic range of an ADC, beyond which a spectral analysis poses special detection and thresholding problems.

To get much more understanding between SNR, SNDR, and SFDR, we can realize the difference between these parameters by the power spectrum illustrated in Figure. 2.6, where S is the fundamental of the input tones, D is the harmonic distortion component, and N is the noise floor. The Spurious Free Dynamic Range (SFDR) is depicted in Figure 2.6. SNR and SNDR are defined as

$$SNR = \frac{S}{N} \qquad SNDR = \frac{S}{N+D} \qquad (2.7)$$

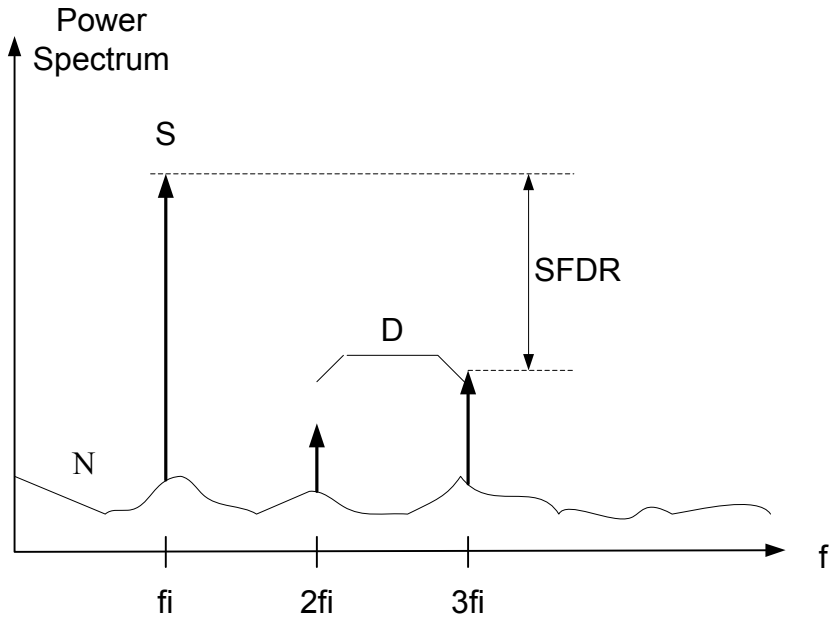


Figure 2.6 the power spectrum with the fundamental and noise[05]

2.2.2.4 Effective Number of Bits (ENOB)

For actual ADCs, a specification often used in place of the SNR or SNDR is ENOB, which is a global indication of ADC accuracy at a specific input frequency and sampling rate. ENOB can be defined as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad bits . \tag{2.8}$$

2.2.2.5 Dynamic Range (DR)

Dynamic range (DR) is the input power range for which the signal-to-noise ratio of the ADC is greater than 0 dB. The dynamic range of a converter is usually specified as the ratio of the rms value of the maximum amplitude input sinusoidal signal to the rms SNR measured when the same sinusoid is present at the output. The dynamic range can be obtained by measuring the SNR as a function of the input power.

2.2.2.6 Sampling-Time Uncertainty (Aperture jitter)

The aperture jitter comes from the fact that there is a random variation between the clock signal and the effective holding time. For a sinusoidal waveform, the sampling time uncertainty is less of a problem near the peak values. However, the sampling time uncertainty will cause severe errors at the zero crossing where the maximum rate of change occurs.

A ADC with a full-scale sinusoidal input is illustrated in Figure 2.7.

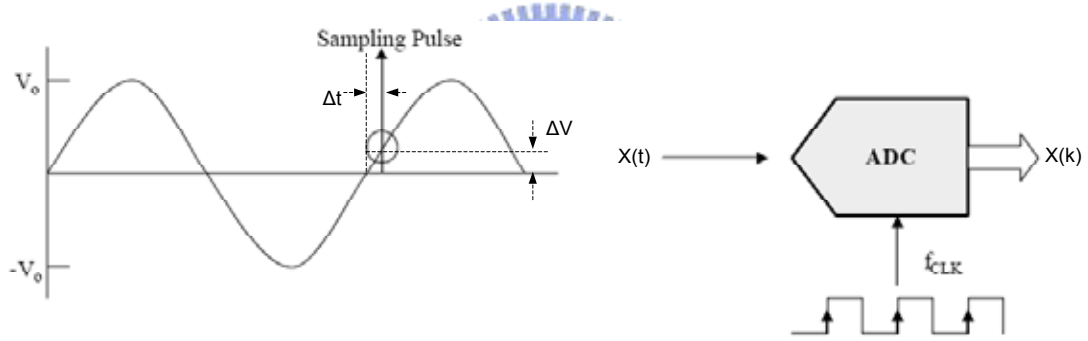


Figure 2.7 the aperture jitter for full-scale sinusoidal input

For the continuous-time input X(t), the discrete-time output is generated through the ADC which is controlled by the clock f_{clk}. Taking account of the aperture jitter Δt, we can get

$$X(k) = X(kT_s + \Delta t) \qquad T_s = \frac{1}{f_{CLK}} \tag{2.9}$$

For a full-scale sinusoidal input with the frequency f_{in}, we can find that

$$X(t) = \frac{1}{2} A_{FS} \sin(2\pi f_{in} t) \qquad A_{FS} = 2^N LSB \tag{2.10}$$

At the zero corssing, we find that the aperture error voltage ΔV must be less than 1 LSB

$$\Delta V \approx \frac{dX}{dt} \times \Delta t < A_{FS} \times \pi f_{in} \times \Delta t < 1\ LSB \tag{2.11}$$

In consequence, we get the limit of the aperture jitter Δt for the N bit ADC as follows,

$$\Delta t < \frac{1}{2^N \pi f_{in}} \tag{2.12}$$

In the other way, the signal-to-noise ratio (SNR) is limited by the aperture jitter. Let $X(t) = \frac{1}{2} A_{FS} \sin(2\pi f_{in} t)$ and Δt be a random variable, then

$$\begin{aligned} X(k) = X(kT_s + \Delta t) &\approx \frac{1}{2} A_{FS} \sin(2\pi f_{in} kT_s) + \frac{dX(t)}{dt}|_{t=kTs} \times \Delta t \\ &\approx \frac{1}{2} A_{FS} \sin(2\pi f_{in} kT_s) + A_{FS} \pi f_{in} \cos(2\pi f_{in} kT_s) \times \Delta t \end{aligned} \tag{2.13}$$

The total signal power and noise power can be calculated to be

$$\overline{X^2(k)} = \frac{1}{8} A_{FS}^2 + \frac{1}{2} A_{FS}^2 \pi^2 f_{in}^2 \times \overline{\Delta t^2} = P_s + P_n \tag{2.14}$$

By the equation (2.14), the signal-to-noise ratio of X(k) is

$$SNR = \frac{P_s}{P_n} = -20 \log(2\pi f_{in} \Delta t_{rms})\ dB \tag{2.15}$$

From the equation (2.15), it can be seen that SNR is independent of signal amplitude and that it decrease as the signal frequency f_{in} and the rms value jitter Δt_{rms} increases. [01][06]

2.3 ADC Architectures Overview

Architectures for realizing analog-to-digital converters can be divided into three categories shown in Table 2.1 --- low-to-medium speed, medium speed, and high speed. These different types of A/D converts are designed for several kinds of applications, such as video systems, communication systems, and audio system, etc. In this section, we will discuss some of the prominent A/D converters. In many applications, it is necessary to have a smaller conversion time. Therefore, it has led to the development of high-speed ADCs that use parallel techniques to achieve short conversion times or increase the speed of the individual components in ADCs. However, the high speed ADCs usually cannot be design for very high resolution, like 14-bit resolution or even more. The speed and resolution of A/D converter is a trade off and it is difficult to design ADCs satisfying both demands at the same time. Generally, the oversampling architecture of the ADC is adopted for high resolution design.

Low-to-Medium Speed, High Resolution	**Medium Speed, Medium Resolution**	**High Speed, Low-to-Medium Resolution**
Integrating Oversampling	Successive approximation Algorithmic	Flash Two-step Interpolating Folding Pipelined Time-interleaved

Table 2.1 Different A/D converter architectures [04]

2.3.1 Flash ADC

Flash ADCs are the very-high-speed converters. The input signal in a flash is fed to 2^{N-1} comparators in parallel, as shown in Figure 2.8. For a N-bit flash converter, It performs 2^N-1 level quantization by dividing the full-scale reference voltage into 2^N segments. The reference voltages of the comparators are generated by using a resistor ladder which is connected between the positive and the negative reference voltage: +Vref and –Vref respectively. Each comparator is also connected to a different node of a resistor string. Any comparator connected to a resistor string node where the reference of each comparator is larger than the input signal will have a 1 output, while those connected to nodes with less reference voltages than the input voltage will have 0 outputs. The set of 2^N-1 comparator outputs is often referred to as thermometer code and is converted to N-bit binary word with a logic circuit. The input signal of the flash ADC is directly connected to the inputs of the comparators, and all comparators compare the input signal with the reference voltages in the resistor string simultaneously. Thus the speed of the flash ADC is very fast and the speed is only limited by the speed of the comparators. Therefore the flash ADC is capable of high speed.

The flash ADCs are fast but they require a large number of comparators, which typically take up a large area and consume much power. Both area and power become isseues in the parallel ADC as the resolution increases. Therefore the flash ADC is not suitable for high resolution application; typical resolutions are seven bits or below.

Besides, the bubble error is a serious problem. The outputs of the comparators should be a thermometer code with a single transition. However, sometimes a lone 1

will occur within the strings of 0s due to comparator metastability, noise, cross talk, limited bandwidth, etc. To combat the bubble noise, one can widen the input of the 1-of-2^N detector. For example, use three-input OR gate to detect the 011 transition in the thermometer input. [04]

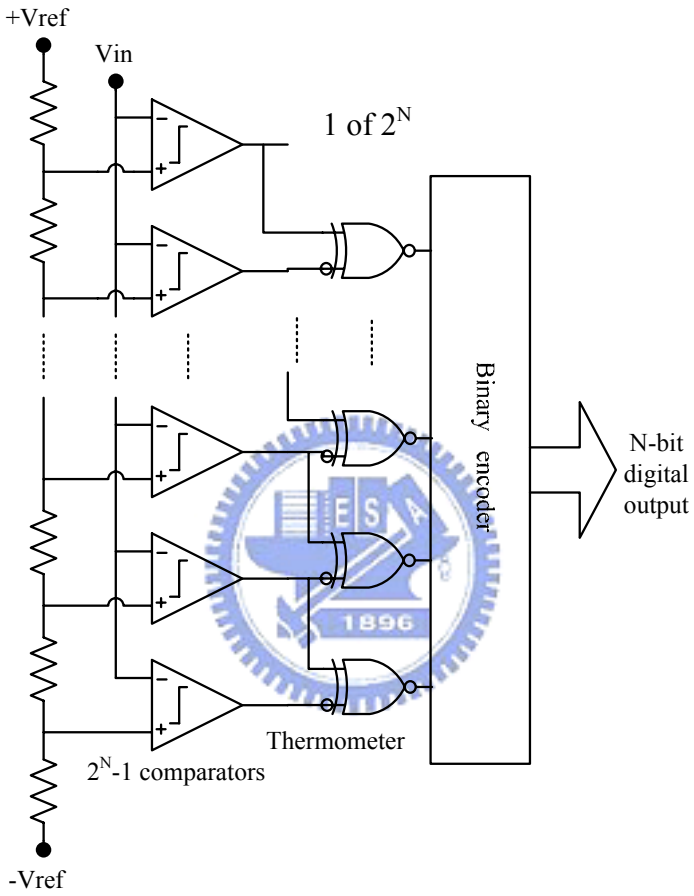


Figure 2.8 N-bit Flash ADC

2.3.2 Two-Step ADC (or Subranging ADC)

In high speed applications, it is difficult to realize high-resolution flash ADCs which have the exponential growth of size and power. In order to overcome these drawbacks, two-step ADC has been proposed. The two-step ADC is demonstrated by separating coarse and fine converters into two paths, as shown in Figure 2.9.

The two-step ADC consists of an S/H circuit, a coarse flash ADC, a DAC, and a fine ADC. The conversion takes two steps. First, the S/H circuit samples the input signal and the M-bit MSB are generated through the coarse flash ADC. These M-bits will correspond to output voltage of the DAC. Second, the output voltage is subtracted from the former analog input voltage. The residue voltage is determined by the fine flash ADC to get the N-bit LSB. Therefore, the M+N bits resolution is reached by combining M-bit MSB and N-bit LSB.

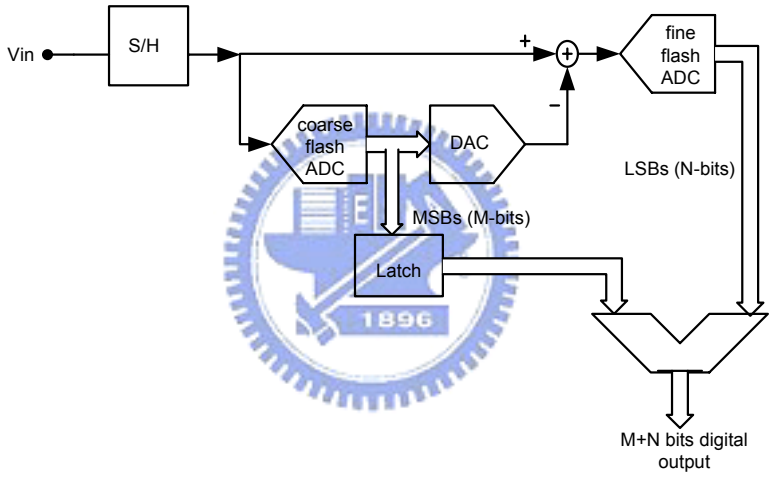


Figure 2.9 Two-step ADC

Compared with the flash ADC, the number of the comparators for the architecture of the two-step ADC is reduced from 2^{M+N}-1 to 2^{M}-1+2^{N}-1. For example, to achieve 10-bit resolution, we can reduce the number of comparators from 1023 (in flash architecture) to 62 (in two-step architecture). The area and power consumption is also reduced greatly.

However, the two-step converter has a longer latency delay than the flash

converter but it can allow for higher resolutions than the flash converter because of reducing the number of comparators.

2.3.3 Pipelined ADC

In a pipeline A/D converter, the quantization is distributed along a pipelined signal chain resulting in an effective architecture for high-resolution high-speed ADCs. By the idea of the two-step architecture, it is spread to a multi-stage architecture to construct the pipelined ADC. It has features that improve the throughput rate and tolerance to comparator offsets. The block diagram of the pipelined ADC is shown in Figure 2.10. It consists of M low-resolution stages and each stage generates k bit output codes. Finally, the last pipelined stage is followed by a flash ADC providing p bits. [07]

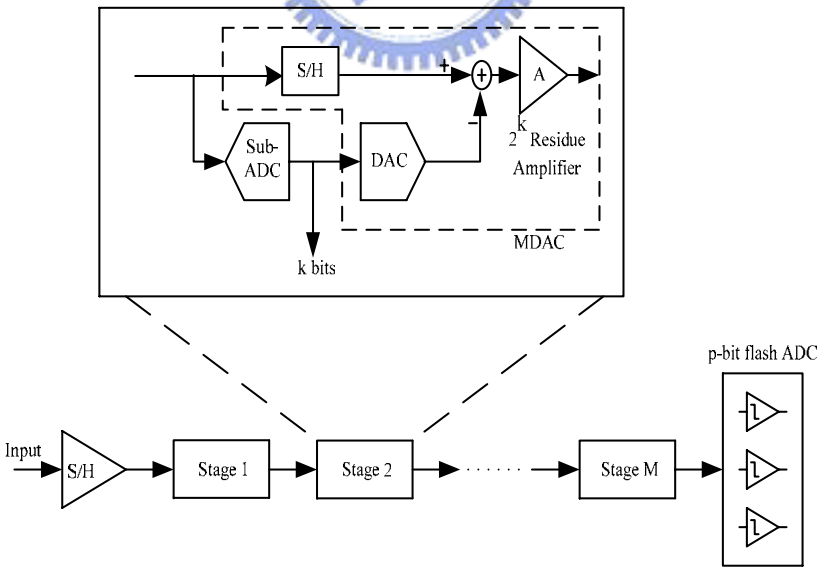


Figure 2.10 m-bit/stage pipelined ADC

The input signal is first sampled by the front-end S/H circuit and then the output is delivered to Stage 1. For each stage, the input signal is the output of the previous

stage except for the last stage. Each stage comprises a low-resolution sub-analog-to digital converter (sub-ADC) and an arithmetic unit called the multiplying digital-to-analog converter (MDAC) that performs a sample-and-hold (S/H) operation, coarse D/A conversion, subtraction, and amplification. In operation, each stage performs an A/D conversion of k bits, converts the digital output back to analog and subtracts it from the sampled and held analog input. The resulting residue voltage is amplified by 2^k.

The architecture of pipelined ADC is the good compromise between area and speed. However, the major limitation on the accuracy in pipelined ADC is the gain amplifier, especially in the first few stages, where accuracy requirements are most stringent. The bandwidth of the gain amplifiers will decide the total throughput rate of the pipelined ADC. And the gain of gain amplifiers influences the total resolution greatly. Therefore, the gain amplifier plays the most important role in the pipelined ADC.

2.3.4 Cyclic ADC

A cyclic ADC is based on a pipelined ADC, as shown in Figure 2.11. It has only one stage but uses the stage repeatedly in a cycle. A cyclic ADC consisted of a single pipeline stage with the output fed back to the input. The delay from the input sample to complete digital output is the same as the pipelined ADC. The cyclic ADC completes N bits by reusing the stage multiple times thus it uses very little chip area and dissipates very low power. However, the throughput rate of the cyclic ADC is much less than the pipelined ADC. For N bit resolution, the cyclic ADC samples the single input signal every (N*clock cycle), and thus the throughput rate of the cyclic

ADC is only 1/N times compared with the pipelined ADC. [08]

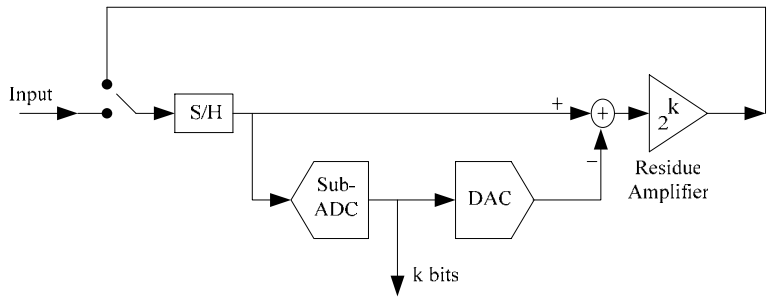


Figure 2.11 Cyclic ADC

2.3.5 Time-Interleaved ADC

Figure 2.12 shows the block diagram of an architecture in which four ADCs are used on parallel to achieve four times the sampling rate of a single converter. This method is often known as time-interleaved architecture . The sample-and-hold circuits consecutively sample and apply the input analog signal to their respective ADCs. The digital outputs of the channels are combined with a multiplexer to a single bit-stream. [02] [06]

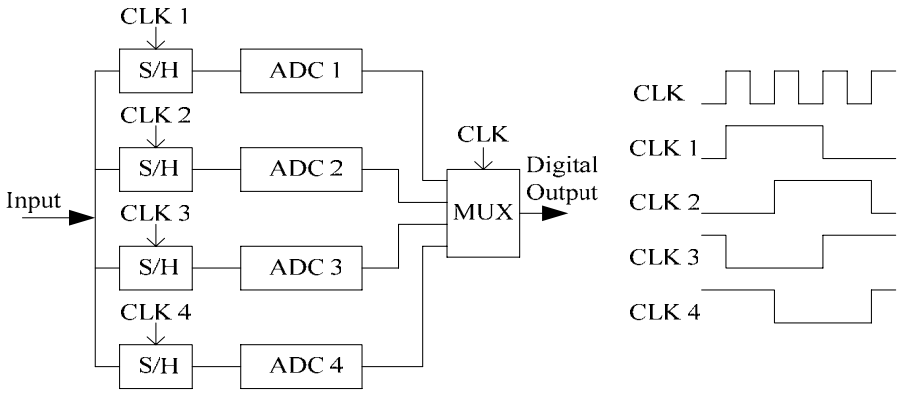


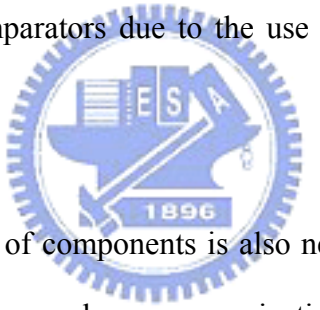
Figure 2.12 Four-channel time-interleaved ADC and its clock signals

Chapter 3

The System of Pipelined Analog-to-Digital Converters and the Double-Sampling Technique

3.1 Introduction

In this chapter we will concentrate on the pipelined ADC. We will discuss the pipelined architecture in more detail. As we know, the pipelined ADC has large tolerance to the offset of comparators due to the use of the redundancy and digital correction algorithm.



However, the nonlinearity of components is also need to take into account. With the rapid growth in applications, such as communication systems and video systems, the demands for the resolution and throughput rate of the ADC are getting higher. As a result, the accuracy for high-resolution pipelined ADCs is actually a tough challenge. Thus some calibration algorithms are developed to improve the accuracy. We will discuss in later section. Finally, the technique of double sampling is introduced, and it will be applied to our design in order to speed the throughput rate of the pipelined ADC.

3.2 Conventional Pipelined ADC

A conventional pipelined ADC consists of N cascaded stages, each resolving k bits as shown in Figure 3.1. Each stage consists of an S/H circuit, a sub-ADC, a DAC and a gain amplifier, as mentioned before. Digital correction logic is often employed in order to relax the specifications of each stage.

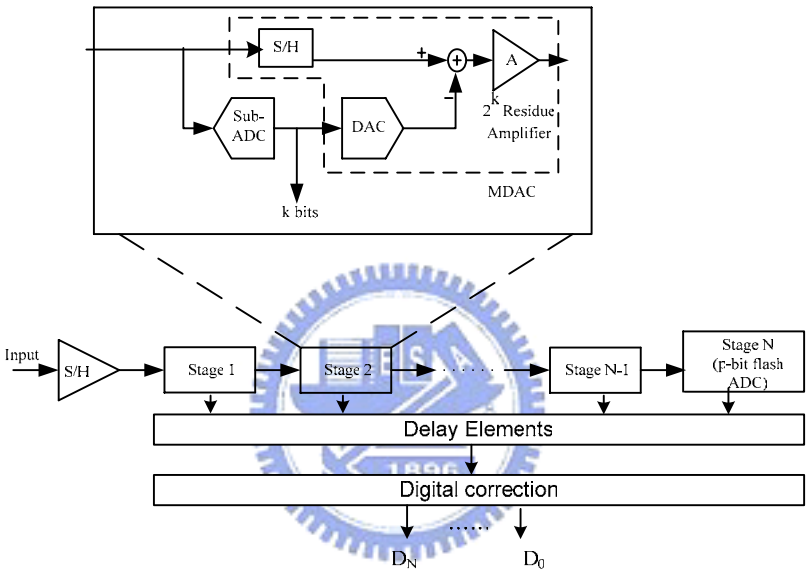


Figure 3.1 Block diagram of N-stage pipelined ADC

The pipelined ADC needs two phase clock phases per conversion. One clock phase is used for sampling the input signal, and the other is employed for holding and delivering the residue voltage. Consecutive stages operate in opposite clock phase and as a result one sample traverses two stages in one clock cycle. Thus the latency in clock cycles is half the number of stages plus one. The complete cycle for processing a given input sample ends when the last stage of the pipeline quantizes the amplified residue provided by the previous stage. Meanwhile, from the beginning of processing a given sample, N/2 new samples are already sampled and being processed inside the

chain. The timming analysis is illustrated in Figure 3.2. For example, the lantency time for the 10-bit pipelined ADC is 5 clock cycles, and the corresponding digitized codes are available at the output after 5 clock cycles of operation. [02]

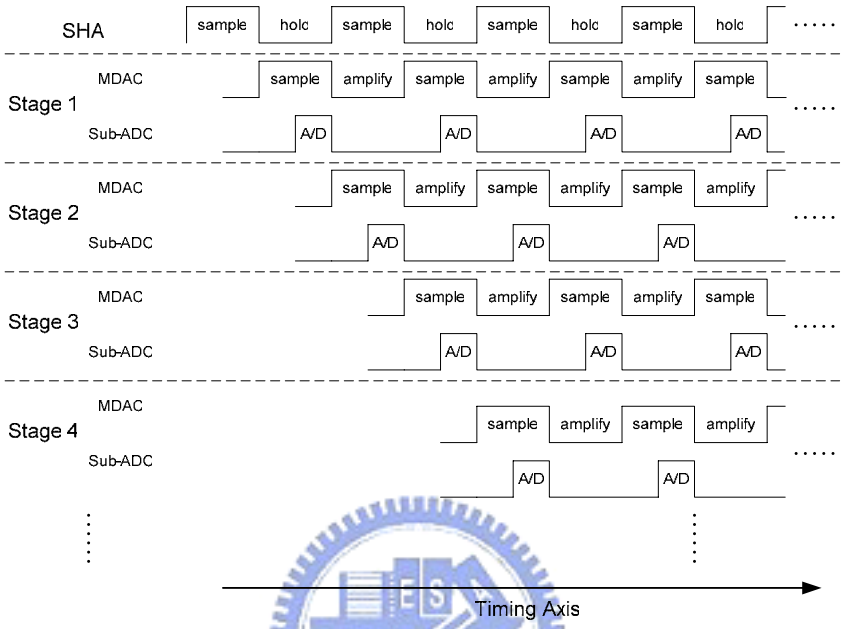
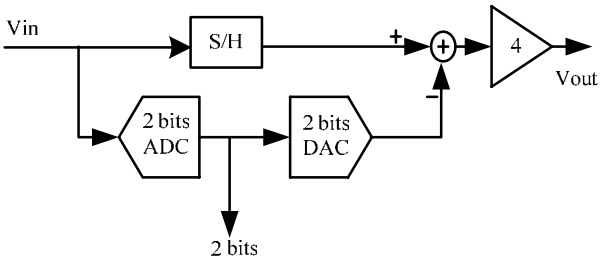


Figure 3.2 Timing diagram of the pipelined ADC

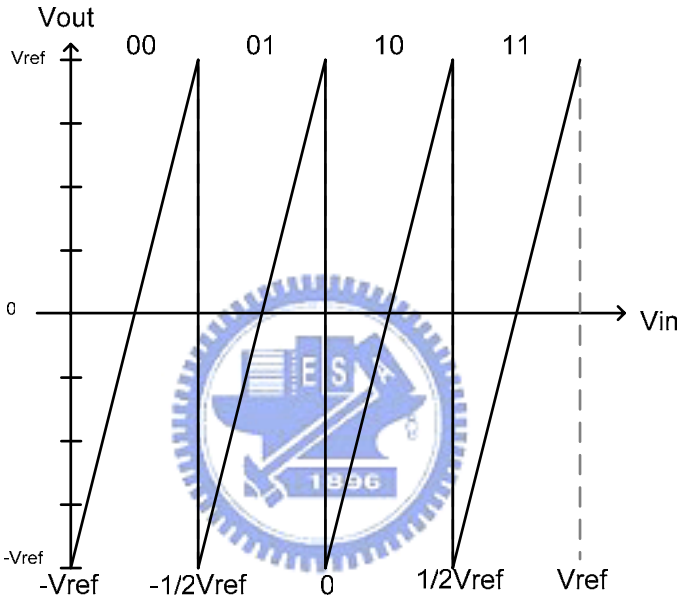
An example for the ideal 2-bit per stage is shown in Figure 3.3(a). The resolution for this stage is 2 bit, and the full scale input range is divided into four subranges, each one corresponding to a given input digital code among the possible combinations. After subtracting the DAC value from the input signal, the residue is yielded by the gain amplifier, whose gain is 4. So the analog residue is

$$V_{out} = 4\left(V_{in} - V_{DAC}\right) \tag{3.1}$$

As shown in Figure 3.3(b), the residue plot is the shape of sawtooth with the full scale range between Vref and –Vref. [09]



(a)



(b)

Figure 3.3 (a) Block diagram for 2-bit/stage (b) ideal residue plot

3.3 Nonidealities and Error Sources in Pipeline ADCs

In the pipelined ADC, designs of each stage and components are not ideal, and some error sources need to be considered while designing the circuit. The primary error sources presented in a pipelined ADC are offset errors in the S/H circuits and amplifiers, gain errors in the S/H circuits and amplifiers, sub-ADC nonlinearity, DAC nonlinearity, and opamp settling-time errors.

For an example of ideal 2-bit pipelined stage, the residue plot and conversion characteristic are shown in Figure 3.4. Ideally, the 2-bit stage transistion voltages are 0, -1/2 Vref, 1/2 Vref, where Vref is the reference voltage. The residue amplification characteristic has four segments according to the input voltage. And the conversion characteristic for 2-bit stage is linear. [10]

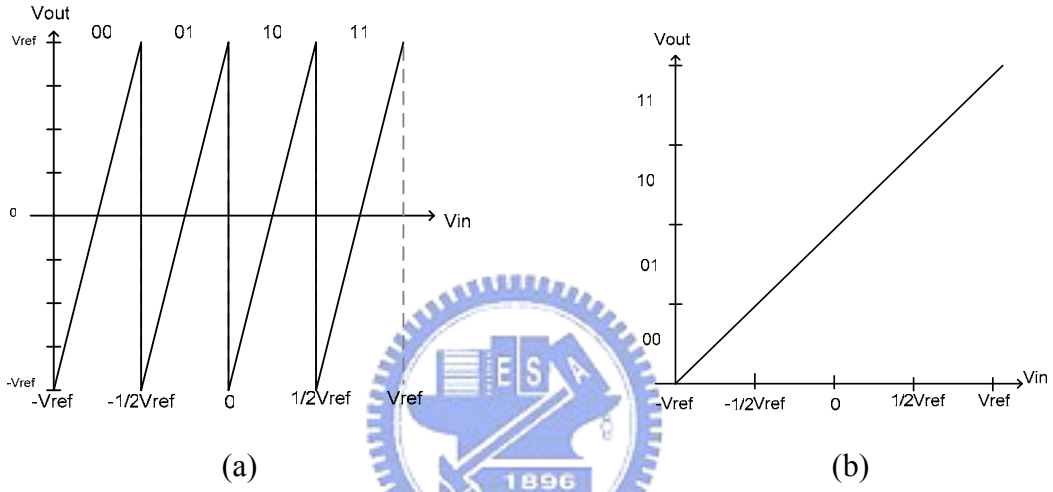
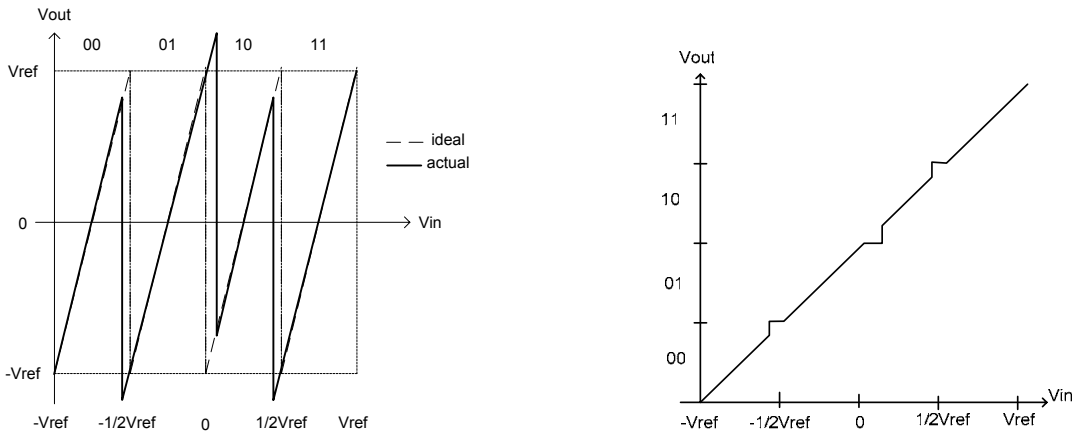


Figure 3.4 Ideal 2-bit stage (a) residue plot (b) conversion characteristic

3.3.1 Nonidealities in the Sub-ADC

For the comparators in the sub-ADC, limited accuracy and offset in the decision levels of the comparators produce wrong 2-bit output codes and, consequently, originate deviations in the transition voltages between subranges of the residue characteristic. If the deviations in the residue characteristic exceed the full range scale, the residue propagated to the next stage exceeds the conversion range of the next stage, resulting in saturation which cannot be corrected. So some codes will be missing, as shown in Figure 3.5. The offset error can be resolved by the digital error correction technique, discussed later.



(a) (b)

Figure 3.5 2-bit stage with comparator offset (a) residue plot (b) conversion characteristic

3.3.2 Residue Amplification Gain Error in the MDACs

For a given pipelined stage, a gain error in the residue amplification can cause the residue range to be smaller or larger than the conversion range of the following stage. As a result, missing codes is also apparent to see. Figure 3.6 illustrates these errors where the residue amplification characteristic of the MDAC exhibits different segment-slopes from the ideal ones. Gain errors result from two aspects. On one hand, the residue amplification gain error is basically due to mismatches between the sampling capacitors and the feedback capacitors. On the other hand, the limited DC gain of the operational amplifier contributes to the gain error of the residue. [11] To overcome gain errors, analog or digital self-calibration techniques are employed and they also improve the DNL of the conversion characteristic.

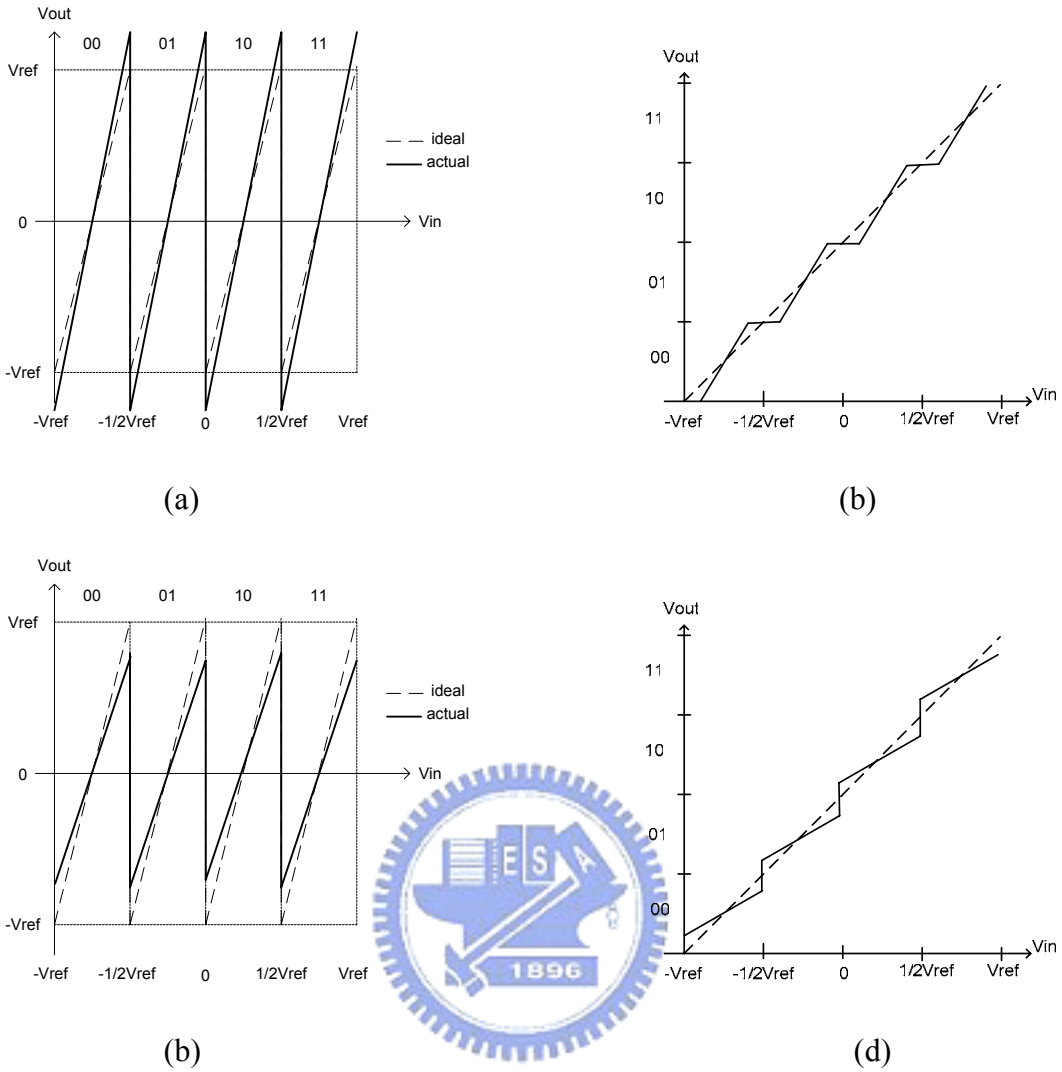
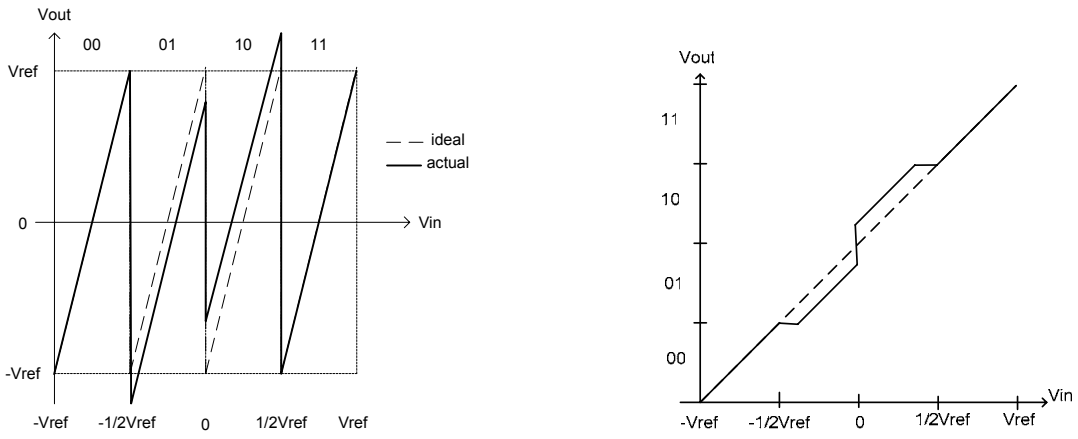


Figure 3.6 Residue plot and conversion characteristic of 2-bit stage considering a gain error (a) (b) larger and (c) (d) smaller than 4

3.3.3 Nonlinearity in the MDACs

Mismatch errors in the capacitor-array of the MDAC and nonlinearity in the operational amplifier produce differences in the transition magnitudes of the residue. Figure 3.7 illustrates nonlinearity in MDACs and it results in different width for each digital code corresponding to the input voltage. The nonlinearity errors in the MDACs can produce a large number of missing code in the overall conversion characteristic.



(a) (b)

Figure 3.7 2-bit stage with nonlinearity in MDAC (a) residue plot (b) conversion characteristic

3.4 Digital Error Correction Technique and Redundancy

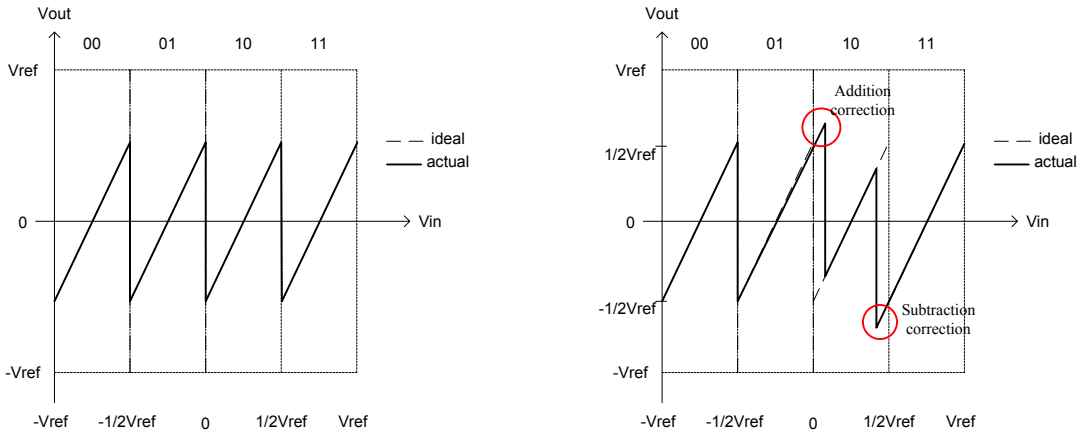
Digital error correction and redundancy are used to eliminate the nonlinearity of sub-ADC and inter stage offset on the overall linearity. With the digital error correction, the pipelined ADC has a large tolerance of the comparator offset. Without the digital error correction, the comparator offset must be no more than one LSB of the pipelined ADC. This technique is attractive because it allows the use of simplified comparators for each stage. Thus, it can reduce the total area and power consumption.

As we mention in 3.3, the comparator offset and gain error may lead the residue to the next stage to exceed the conversion range and make codes missing. In the pipelined ADC, it needs the same input and output signal range for each stage due to the cascade implementation. The output signal for each stage is produced by the gain amplifier which has gain of 2^N, N is the resolution for each stage. The amplified

residue must still within the conversion range for the next stage. However, it is difficult to avoid code missing with the inter stage gain as much as 2^N. In order to overcome this problem, the inter stage gain is reduced to 2^{N-1} so that the amplified residue can remain within the conversion range of the next stage.

In many previous implementations, digital error correction technique has used both addition and subtraction to correct errors. When the offset error occurs in the first stage, the next stage can calibrate the digital codes of the first stage by the digital error correction. The correction logic has three options at each stage (to add, subtract, or do nothing) according to the residue of the previous stage.

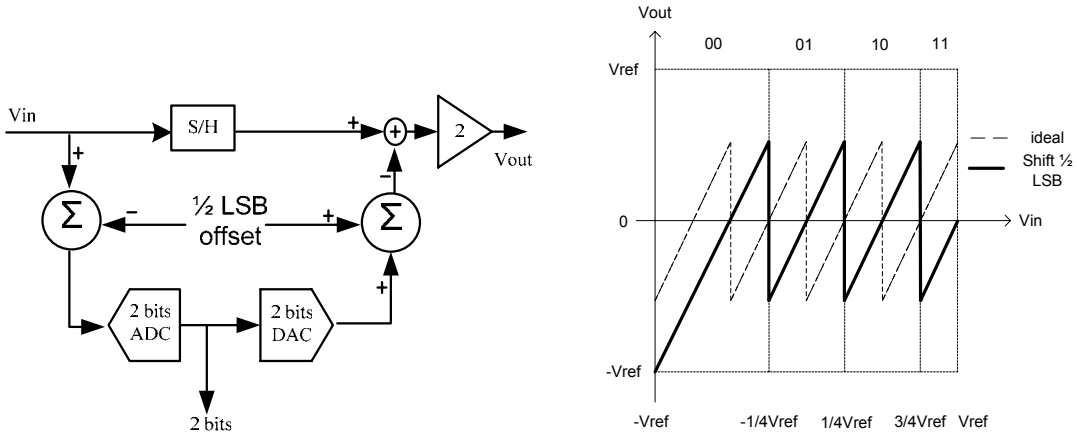
To illustrate digital error correction technique in more detail, we take a 2-bit/stage pipelined ADC for example. When the inter stage gain is reduced to 2, the residue range is compressed between 1/2 Vref and -1/2 Vref, illustrated in Fig 3.8 (a). Even if the comparator offset occurs, the residue is still within Vref and –Verf. And then the following stage will correct the output codes by adding or subtracting correction, as shown in Figure 3.8 (b). When one of the decision level of the sub-ADC has an offset, the output of the first stage will exceeds 1/2 Vref. The second stage, sensing the overhanging, will add the output by 1 LSB. In the same way, when the output of the first stage drops below -1/2 Vref, the second stage will subtract 1 LSB. It allows the comparator offset to be as large as 1/4 Vref and the output is still in the input range of the following stage. Digital error correction simply utilizes the extra bit to correct the overhanging section from the previous stage.



(a) (b)

Figure 3.8 the residue plot with inter stage gain of 2 (a) without offsets (b) with offsets

Since subtraction is equivalent to addition with offset, the required correction logic can be simplified by eliminating the need for the correction logic to do subtraction. So subtraction can be eliminated by intentionally adding a 1/2 LSB offset to both sub-ADC and DAC, as shown in Figure 3.9. After shifting 1/2 LSB offset in

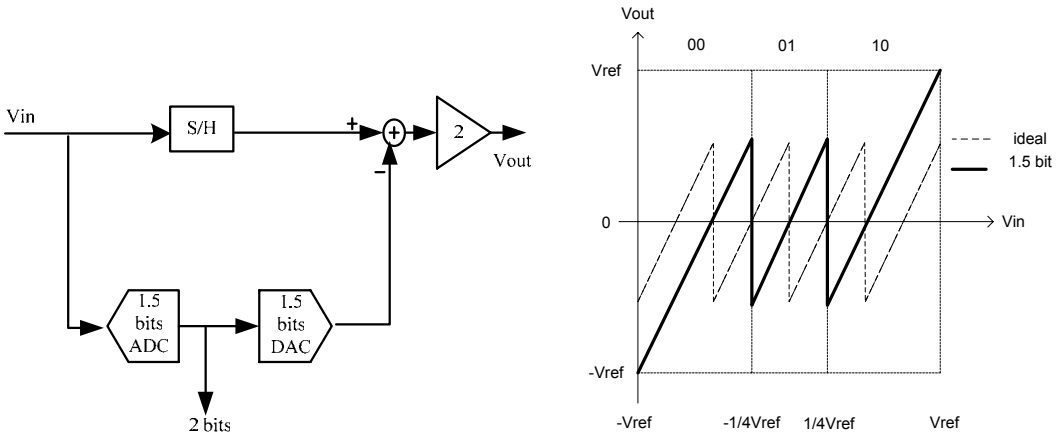


(a) (b)

Figure 3.9 (a) Block diagram of one stage with offset in ADC and DAC (b) ideal residue versus held input with 1/2 LSB offset

the decision level, the subranges are separated in different width. The section of "00" is enlarged and that of "11" is reduced. Because the interstage gain is 2, the amplified residue remains within the conversion range of the next stage when the offset of comparators are between 1/2 LSB. Under these conditions, errors caused by the sub-ADC nonlinearity can be corrected, and the correction requires no change and addition.

Since the top-most decision level is 1/2 LSB below the maximum stage input, we can assume that the decision level of the top comparator has an offset of 1/2 LSB adding and it is shifted to the upper bound of the conversion range, as shown in Figure 3.10(b). So the digital output code 11 is eliminated. However, the output code 11 can be recovered by the digital error correction of the next stage and the output residue is still within the conversion range. According to this assumption, removal of the top-most comparator does not change the correction range because the decision can still move by up to ±1/2 LSB before saturating the next stage. [09] [12]



(a) (b)

Figure 3.10 (a) Block diagram of 1.5 bit output per stage(b) ideal residue versus held input without top comparator

The final block diagram is shown in Figure 3.10(a). The comparator thresholds are at 1/4 Vref and -1/4Vref and the DAC level are at -1/2Vref, 0, 1/2Vref. In each stage, only 2 comparators are needed, which means that the resolution per stage here is 1.5 bits. Reconstruction of the redundant sign digit coded digital stage outputs is performed by adding up the properly delayed stage outputs with one-bit overlap, as indicated in Figure 3.11. [07] [09]

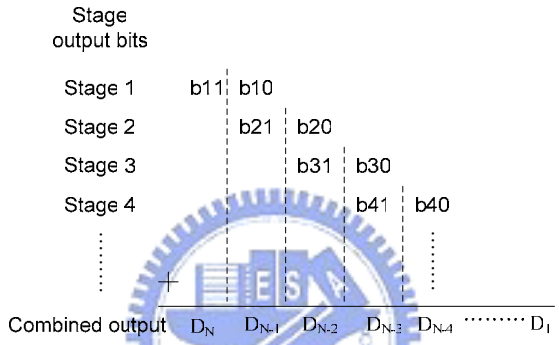


Figure 3.11 RSD correction in digital domain

3.5 1.5 Bit / Stage Architecture

As we know, the 1.5 bit/stage pipeline architecture is characteristic of only 3 digital output codes, 00, 01, and 10. If we would like to realize a pipelined ADC with 10 bits resolution, 1.5 bit/stage architecture can be adopted with 9 stages and each stage resolves two bits with a sub-ADC, as shown in Figure 3.12. The 1.5 bit/stage pipeline architecture is employed in the first 8 stage, and the last stage is composed of 2 bit flash qunatizer. According to the input range of signal, from –Vref to -1/4Vref, -1/4Vref to 1/4Vref, and 1/4Vref to Vref, the output residue transfer function can be derived as follows :

$$V_{out} = \begin{cases} 2V_{in} + V_{ref}, if\ -V_{ref} < V_{in} < \dfrac{-V_{ref}}{4} \Leftrightarrow D = (00)_2 \\ 2V_{in}\qquad , if\ \dfrac{-V_{ref}}{4} < V_{in} < \dfrac{+V_{ref}}{4} \Leftrightarrow D = (01)_2 \\ 2V_{in} - V_{ref}, if\ \dfrac{+V_{ref}}{4} < V_{in} < +V_{ref} \Leftrightarrow D = (10)_2 \end{cases} \tag{3.2}$$

D is the output code for each stage. The transfer function of 1.5-bit/stage is shown in Figure 3.10(b). Because of using the digital error correction technology, the 1.5-bit/stage has lower (2 instead of 4) inter-stage gain than the 2-bit/stage, but it requires more stages (9 stages instead of 5 stages for 10bits ADC) than the 2-bit/stage. By reducing the inter-stage gain, the accuracy requirements on the sub-ADCs are greatly reduced. In this research, a maximum offset voltage of Vref/4 can be tolerated before the bit errors occur.

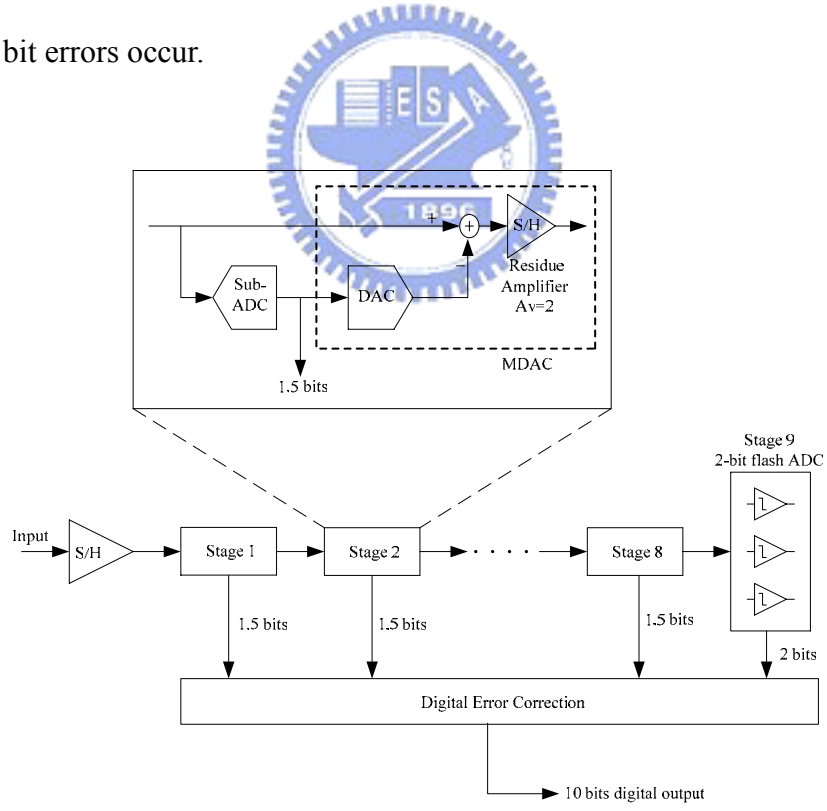


Figure 3.12 Pipelined ADC with 1.5-bit/stage architecture

For implementation of a pipeline stage, Figure 3.13 is illustrated to understand

how the 1.5 bit/stage architecture works. For simplicity, a single-ended configuration is used. A common, switched-capacitor implementation is chosen which operates on a two-phase clock. During the first phase, the input signal V_i is applied to the input of the sub-ADC, which has thresholds at Vref/4 and –Vref/4. The input signal ranges from –Vref to Vref. Concurrently, V_i is applied to sampling capacitors C_s and C_f. At the end of the first clock phase, V_i is sampled across C_s and C_f, and the output of the sub-ADC is latched. During the second phase, C_f closes a negative feedback loop around the opamp, while the top plate of C_s is switched to the DAC output. The stage residue V_o is generated by this configuration. The output of the sub-ADC is used to select the DAC output voltage, V_{dac}, through an analog multiplexor. V_{dac} is capacitively subtracted from the residue such that :

$$V_o = \begin{cases} (1+\frac{C_s}{C_f})V_i - \frac{C_s}{C_f}V_{ref} & \text{if } V_i > \frac{V_{ref}}{4} \\ (1+\frac{C_s}{C_f})V_i & \text{if } -\frac{V_{ref}}{4} < V_i < \frac{V_{ref}}{4} \\ (1+\frac{C_s}{C_f})V_i + \frac{C_s}{C_f}V_{ref} & \text{if } V_i < -\frac{V_{ref}}{4} \end{cases} \quad (3.3)$$

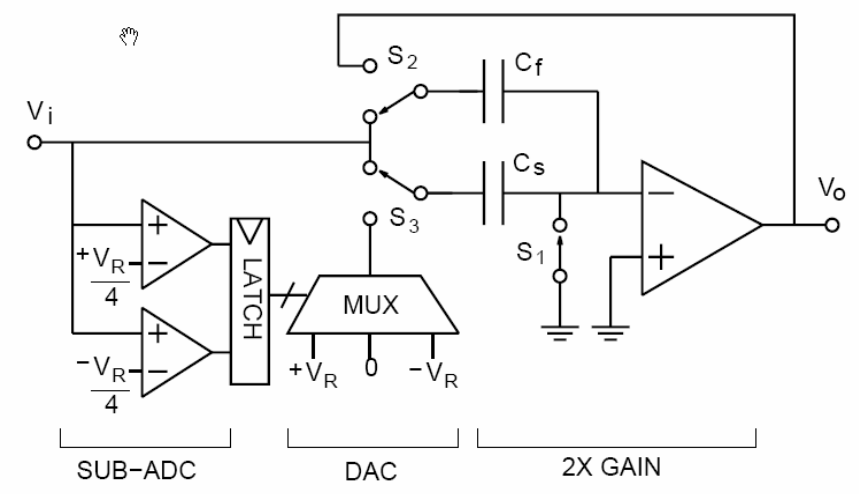


Figure 3.13 Switched-capacitor implemention of each pipeline stage

In the 1.5 bit/stage architecture Cs=Cf is chosen to give a gain of two in the transfer function. In the 1.5 bit/stage architecture Cs=Cf is chosen to give a gain of two in the transfer function. The opamp gain msut be large (>60dB for 10 bit pipelined ADC) enough to reach the specifications of the resolution. Moreover, the opamp must settle to better than 0.1% accuracy in one clock phase (one half cycle). The settling time limits the overall pipelined throughtput. [13]

3.6 Calibration Techniques for Pipelined A/D Converter

A number of calibration Techniques have been developed to make high resolution analog to digital conversion possible in spite of the sources of error mentioned earlier in the chapter. Some of the techniques are based on adding circuit enhancements to reduce the error to a tolerable level. Other techniques do not attempt to fix the error but instead are based on design changes that make the error more tolerable. The basic idea in the calibration methods is to minimize or correct the steps causing nonidealities in the stage transfer functions. These calibration techniques have resulted in an improvement of the resolution capability of pipelined ADCs. This improvement has made it possible to design pipelined ADCs with high resolutions that are limited by thermal noise rather than matching constrains. Because the mismatch and error attached to each step can either be average out, or their magnitude can be measured and corrected.

3.6.1 Capacitor Error Averaging

Capacitor error averaging is the technique for achieving a precise gain of two in the residue amplifier for each stage of the pipelined ADC. The basic idea in the

capacitor error averaging is, rather than fix the sampling and feedback capacitors in the MDAC, to swap their roles. The residue is amplified twice and each time a different feedback capacitor is be used. But an extra clock phase and one additional amplifier are needed in each stage. By adding an extra clock phase, the gain error resulting from the mismatch between the two different feedback loops is compensated during different feedback capacitors interchanging.

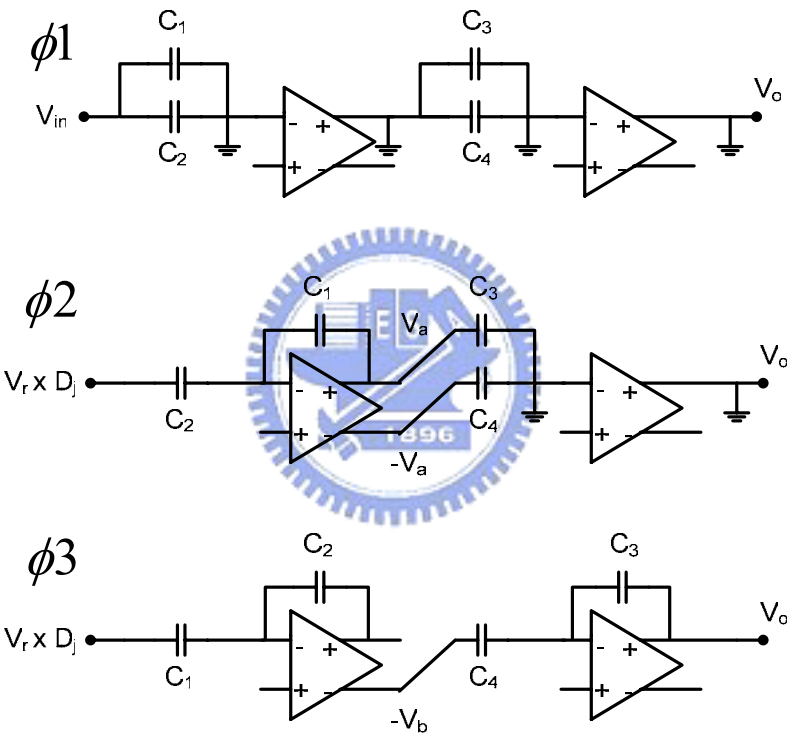


Figure 3.14 Capacitor error averaging technique: $\phi 1$: sampling phase

$\phi 2$:amplification phase $\phi 3$:averaging phase

Figure 3.14 shows how the capacitor error averaging technique works during each phase. During $\phi 1$ the input signal V_{in} is sampled onto capacitors C_1 and C_2. These two capacitors have mismatch capacitances. As a result, interstage gain is different while using either capacitor as the feedback capacitor. To average gain error, it needs

two amplification phases, one where C_1 is used for feedback and the other where C_2 is used for feedback. During the amplification phase $\phi 2$, C1 is used for feedback, and the positive output of the first amplifier V_a is sampled onto capacitor C_3 while the negative output of the first amplifier $-V_a$ is sampled onto capacitor C_4. During the averaging phase $\phi 3$, C_2 is used for feedback, and the negative output $-V_b$ is connected to C_4

In order to analyze the output voltage as a function of the input voltage, we have to assume these capacitors are not match perfectly. So let's assume that

$$C_1=C_a, \quad C_2=(1+\alpha)C_a, \quad C_3=2C_b, \quad C_4=(1+\beta)C_b$$

$$\text{where} \quad |\alpha| \ll 1, \quad |\beta| \ll 1$$

During the sampling phase $\phi 1$ and the amplification phase $\phi 2$, the following expression is obtained.

$$V_a = V_{in} + \frac{C_2}{C_1}(V_{in} - V_r \times D_j) = (2V_{in} - V_r \times D_j) + \alpha(V_{in} - V_r \times D_j) \tag{3.4}$$

During the averaging phase $\phi 3$, we can get as follows,

$$V_b = V_r \times D_j + \frac{C_1}{C_2}(V_a - V_r \times D_j) \approx (2V_{in} - V_r \times D_j) - \alpha(V_{in} - V_r \times D_j) \tag{3.5}$$

Finally, the output function with gain error averaging is derived by combining equations (3.4) and (3.5).

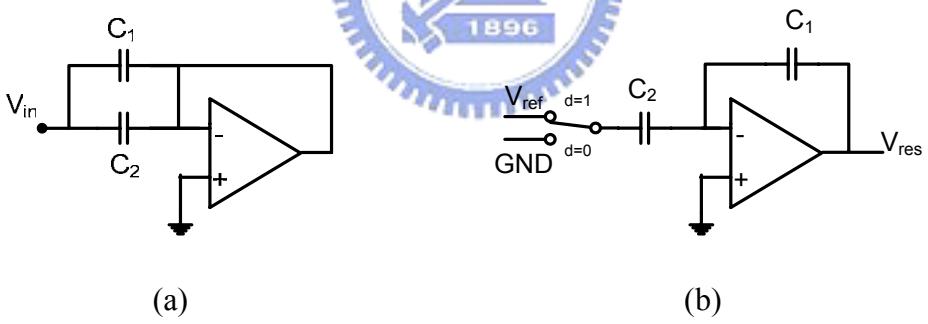
$$\begin{aligned} V_o &= V_a + \frac{C_4}{C_3}(-V_a + V_b) = V_a + \frac{1+\beta}{2}(-V_a + V_b) \\ &\approx (2V_{in} - V_r \times D_j) - \alpha\beta(V_{in} - V_r \times D_j) \end{aligned} \tag{3.6}$$

From the equation (3.6), the oupt voltage can be divided into two parts, which are the ideal residue and the mismatch error. With the capacitor error averaging technique

applying, the mismatch error is actually reduced greatly. [14]

3.6.2 Commutated Feedback-Capacitor Switching Technique (CFCS)

The commuted feedback-capacitor switching technique (CFCS) is motivated by the fact that in many imaging applications, high resolution but medium accuracy are reauired. Therefore, the commutated feedback-capacitor switching technique (CFCS) relaxes the capacitor matching requirement to the point that it is easy to satisfy in most modern process technologies. [15] As a result, the technique allows the capacitors to be scaled down to the kT/C noise limit. With a reduced capacitive load, opamp power consumption is also reduced.



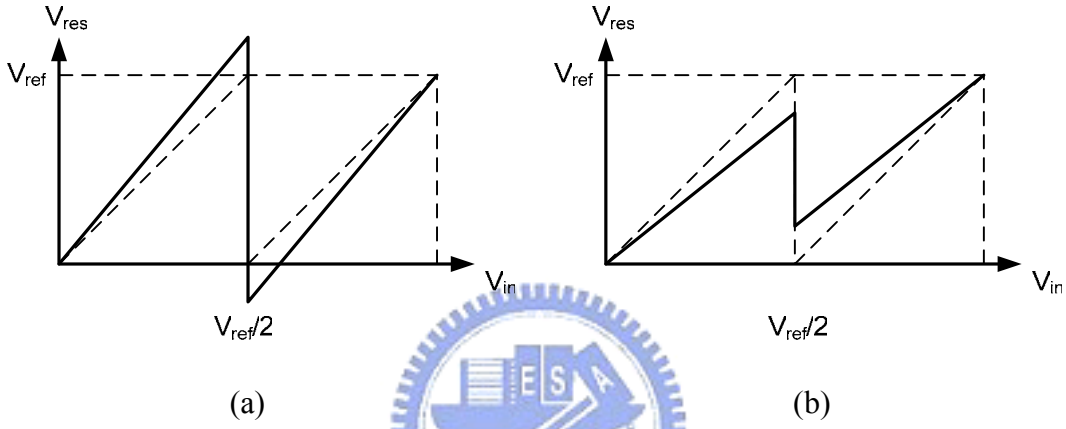
(a) (b)

Figure 3.15 The conventional MDAC operation (a) sampling phase (b) amplifying phase

To compare the CFCS technique with the conventional architecture, we examine the effect of the capacitor mismatch in these two styles. For simplicity, we consider the case of a single-ended 1-b/stage pipelined ADC, which has a capacitor mismatch. For the fixed feedback capacitor stage is illustrate in Figure 3.15. During the sampling phase, the input is sampled on both C_1 and C_2. During the amplifying phase, C_1 is

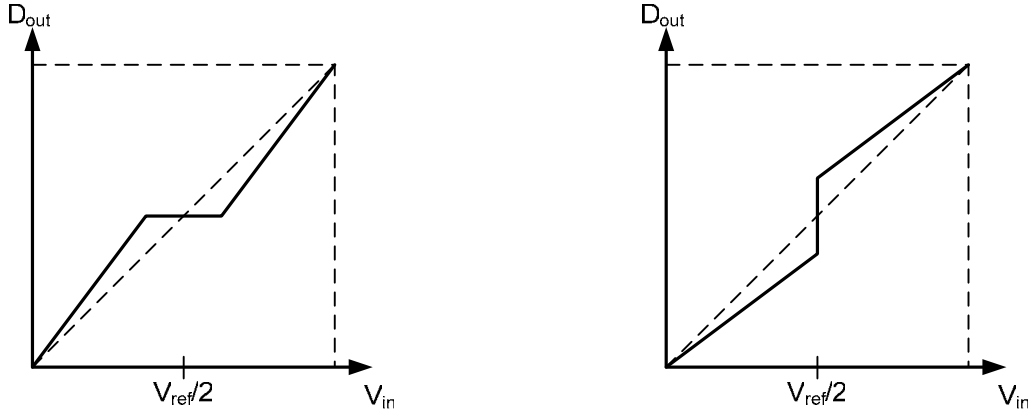
fixed as the feedback capacitor. The residue of the conventional architecture is derived as follows, depending on the input voltage large than Vref/2 (d=1) or less than Vref/2 (d=0)

$$V_{RES} = \begin{cases} (\frac{C_1 + C_2}{C_1})V_{in} & d = 0 \\ (\frac{C_1 + C_2}{C_1})V_{in} - (\frac{C_2}{C_1})V_{ref}, & d = 1 \end{cases} \tag{3.7}$$



(a) (b)

Figure 3.16 Residue plot of the conventional stage (a) for C1>C2 (b) for C1<C2



(a) (b)

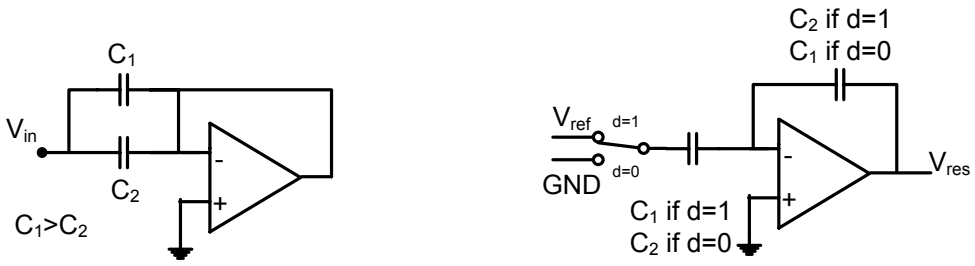
Figure 3.17 Transfer curve of the conventional stage (a) for C_1>C_2 (b) for C_1<C_2

The residue plot of the conventional stage and the transfer curve of the conventional stage are illustrated in Figure 3.16 and Figure 3.17 individually. If C_1<C_2,

the interstage gain is less than 2 and the transfer curve will result in a missing codes error at the boundary of Vref/2. If C_1>C_2, the interstage gain is larger than 2 and exceeds the conversion range. It will results in a wide code error.

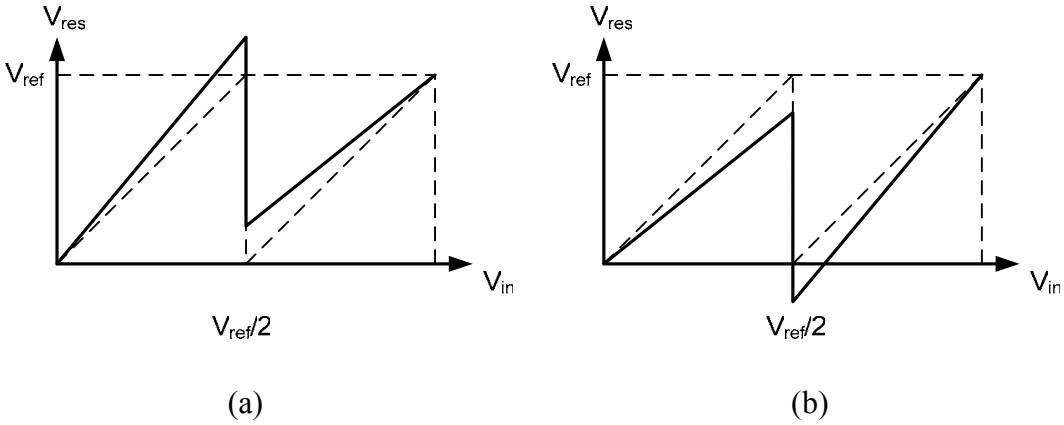
The commuted feedback-capacitor switching technique (CFCS) is shown in Figure 3.18. During the sampling phase, the input is sampled on both C1 and C2 as in the conventional case. During the amplifying case, when the comparator decision d=0 (Vin <Vref/2), C1 is selected as the feedback capacitor. On the other hand, when d=1 (Vin >Vref/2), C2 is selected as the feedback capacitor. The residue plot is shown in Figure 3.19. By interchanging the feedback capacitor depending on the digital code, the residue drop is matched to Vref, the full scale of the next stage. Figure 3.20 illustrates the transfer curve of the stage with the CFCS technique. Although capacitors are mismatch, the problem of missing code error and wide code error at the boundary of Vref/2 are eliminated in Figure 3.20. We can get the residue transfer function as follows

$$V_{RES} = \begin{cases} (\frac{C_1 + C_2}{C_1})V_{in} & d = 0 \\ (\frac{C_1 + C_2}{C_2})V_{in} - (\frac{C_1}{C_2})V_{ref}, & d = 1 \end{cases} \tag{3.8}$$



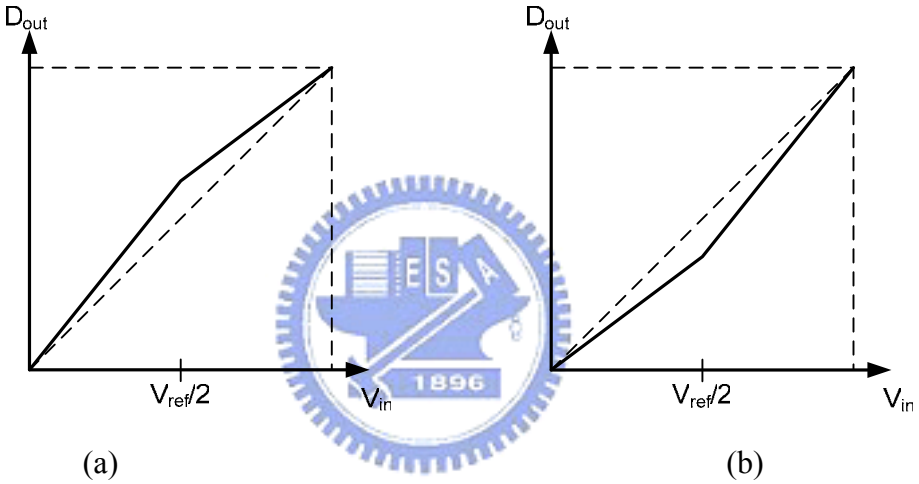
(a) (b)

Figure 3.18 The CFCS's MDAC operation (a) sampling phase (b) amplifying phase



(a) (b)

Figure 3.19 Residue plot with CFCS technique (a) for C1>C2 (b) for C1<C2



(a) (b)

Figure 3.20 Transfer curve with CFCS technique (a) for C_1>C_2 (b) for C_1<C_2

3.7 Double Sampling Technique

The clock rate of the switched capacitor circuits is limited by the bandwidth of the opamp. In order to achieve a high throughput rate, it is essential to exploit the opamp efficiently. This technique is used to double the sampling rate of the switched capacitor circuits without a need to increase the speed of the opamp. A method of increasing the sampling frequency is to use the opamp during both phases of clock. This technique, called double-sampling, was proposed in [16]. It has been applied in

various SC circuits such as filters, ΔΣ-modulators, pipelined ADCs, and sample and hold circuits.

3.7.1 A Double Sampled Switched Capacitor Delay Cell

An SC circuit can be divided into blocks, each comprising an opamp and a set of switches and capacitors. It operates in two phases. In the first phase the circuit samples its input. In the second phase the output is delivered by holding the former sampled value. [17]

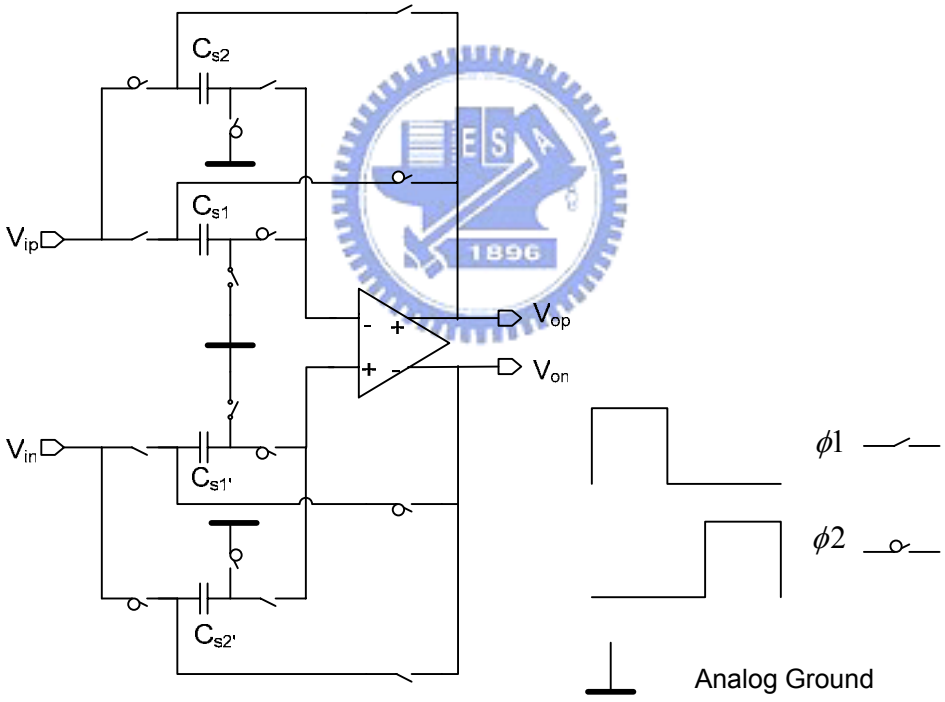


Figure 3.21 A double-sampled SC delay circuit

Since the opamp is not used in the sampling phase, it is more efficient to exploit the opamp's idle phase by duplicating the sampling circuitry and operate the two sampling circuits in opposite clock phases. Based on the architecture of the opamp in one-capacitor sample-and-hold circuit, this circuit utilizes an extra set of capacitors to

increase the sampling frequency by a factor of two without increasing the clock rate or requiring a faster opamp, shown in Figure 3.21. There is only a minor increase in power consumption because it is dominated by the opamp, which consumes power also when idle.

In Figure 3.21 the input signal is sampled every half clock period ($T_s/2$) and appears at the output with a half-clock period delay. Assuming the gain of the opamp A is infinite and other elements in the circuit are all ideal, the transfer function of the circuit is derived as follows

$$\frac{V_{od}(\hat{z})}{V_{id}(\hat{z})} = \hat{z}^{-1} \tag{3.9}$$

where $\hat{z} = e^{j\omega(\frac{T_s}{2})}$

Although the factor-of-two improvement in the speed of the double-sampled SC delay cell is achieved, the mismatch between the two paths actually results in image error in return. Therefore, finite opamp gain and opamp input capacitance need to be taken into account while analyzing the operation of the double-sampled SC delay cell because they are related to both gain and phase error in transfer function of the double-sampled SC delay circuit.

Figure 3.22 shows a single-ended equivalent circuit of the double-sampled delay circuit during $\phi 1$ and $\phi 2$. Charge conversation on capacitors Cs1 and Cin before $\phi 2$ (the non-overlapping phase) and after $\phi 2$ yields the following difference equation :

$$C_{s1}\left[v_i(n) - \left(v_o(n+1) + \frac{v_o(n+1)}{A}\right)\right] = C_{in}\left[-\frac{v_0(n)}{A} + \frac{v_o(n+1)}{A}\right] \tag{3.10}$$

Rewriting the equation (3.10) in z-transform as follows :

$$C_{s1}\left[v_i(z)-\left(v_o(z)\cdot z+\frac{v_o(z)}{A}\cdot z\right)\right]=C_{in}\left[-\frac{v_0(z)}{A}+\frac{v_o(z)}{A}\cdot z\right] \qquad (3.11)$$

If capacitors Cs1=Cs2=Cs, a similar difference equation would be obtained for the $\phi 1$ phase and we can finally find that the transfer function, H(z), to be given by

$$\frac{v_o(z)}{v_i(z)}=H(z)=\frac{1}{1+\frac{1}{A}(\frac{C_s+C_{in}}{C_s})-\frac{C_{in}}{C_s}\cdot\frac{1}{A}z^{-1}}z^{-1} \qquad (3.12)$$

where $\hat{z}=e^{j\omega(\frac{T_s}{2})}$

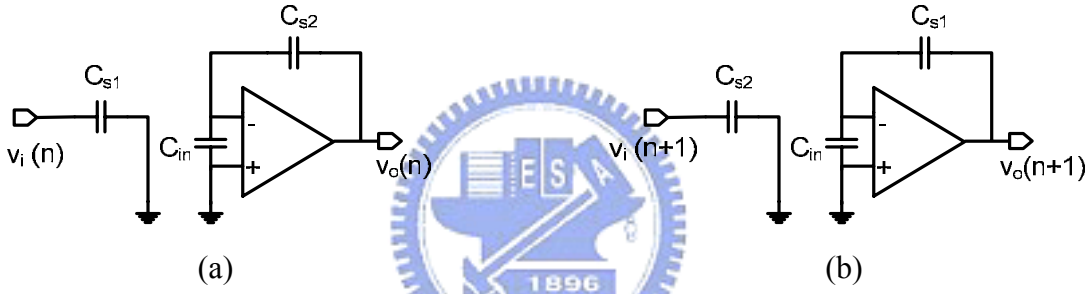


Figure 3.22 A single-ended equivalent circuit of Figure 3.21 during (a) $\phi 1$ (b) $\phi 2$

Therefore, finite opamp gain and non-zero input capacitance modify the transfer function of the double sampled delay cell by damped integrator term from its ideal response. This change of the transfer function causes both gain and phase error in the response of the delay circuit. The actual transfer function becomes

$$H(z)=[m\cdot e^{j\theta}]\cdot z^{-1} \qquad (3.13)$$

where m and θ are magnitude and phase of the error term in the double-sampled delay circuit. Assuming A>>1, the magnitude and phase error are given by

$$m\approx 1-\frac{1}{A\beta}+\frac{\cos\omega T}{A}(\frac{C_{in}}{C_s}) \qquad (3.14)$$

$$\theta \approx -\frac{\sin \omega T}{A}\left(\frac{C_{in}}{C_s}\right) \tag{3.15}$$

3.7.2 Nonidealities in the Double Sampling Circuits

In the double sampling architecture, the use of parallelism in the analog domain introduces limitations that are related to the finite opamp gain and the settling time. These errors mostly arise from the offset, gain and timming mismatches between the two parallel paths. The influence of these errors to the double-sampled SC circuit is discussed below. [18]

3.7.2.1 Memory Effect

Due to the finite gain of the opamp a fraction of the previous sample remains stored in the parasitic capacitance in the input of the amplifier. So in order to consider the analysis more completely, the finite opamp gain and the parasitic capacitance need to be taken into account. The z-transform of the voltage gain in the double-sampled SC delay circuit can be rewritten as

$$\frac{v_o(z)}{v_i(z)} = H(z) = \frac{1}{1+\frac{1}{A}\left(\frac{C_s+C_{in}}{C_s}\right)-\frac{C_{in}}{C_s}\cdot\frac{1}{A}z^{-1}}z^{-1} \tag{3.16}$$

Where A is the DC gain of the opamp, Cs is the sampling capacitor, Cin is the opamp input capacitance, and Cp is the parasitic capacitance in the sampling capacitor. From the equation (3.16), it is a delaying S/H circuit, which has a delay time half of the clock cycle. Besides, the equation shows that double-sampling adds a low-pass

filtering effect. In the worst case the additional error is equal to the error caused by the opamp input capacitance.

3.7.2.2 Offset

Channel offset is caused by operational amplifier and charge injection mismatches across the two paths. Channel offset can be modeled as a voltage source connected in series with path 1, as shown in Figure 3.23.

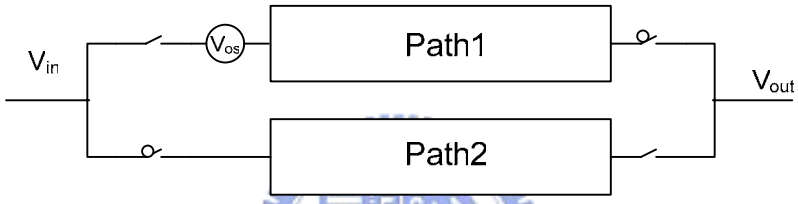


Figure 3.23 Channel offset in the double sampling model

For simpilty, a static offset between the two singal paths can be considered as a constant value added to every other sample. In the time domain it can be written as

$$y(t) = \sum_{n=-\infty}^{\infty} x(t) \cdot \delta(t - nT) + \sum_{n=-\infty}^{\infty} V_{os} \cdot \delta[t - (2n+1)T] \quad n = 0,1,2... \qquad (3.17)$$

where Vos is the offset error between these two paths, and offset always occurs in odd sampling. The frequency domain representation can be obtained with Fourier transform, which results in

$$Y(f) = \sum_{n=-\infty}^{\infty} X(f) \cdot \delta(f - nf_s) - \sum_{n=-\infty}^{\infty} (-1)^n V_{os} \cdot \delta[f - \frac{n}{2} f_s] \quad n = 0,1,2... \quad (3.18)$$

The frequency spectrum is shown in Figure 3.24, where f_s is the sampling frequency. This is manifested in the frequency domain as tones at multiples of $f_s/2$. The effect of

offset is additive and independent from the input signal level and frequency.

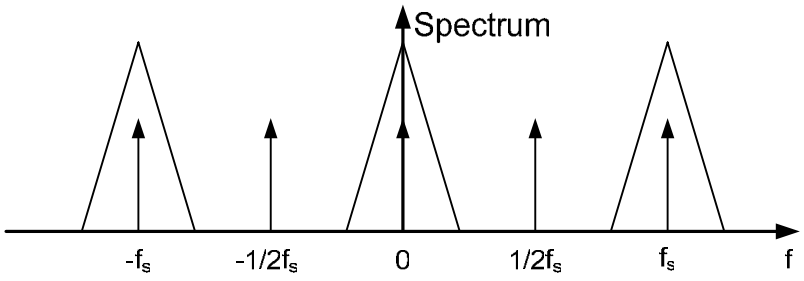


Figure 3.24 the spectrum of the double-sampled SC circuit with channel offsets

3.7.2.3 Gain Mismatch

Gain mismatch is caused by non-symmetry between two paths. It will cause an in-band image of the signal. A diagram of a two-path circuit and its corresponding clock phase is shown in Figure 3.25.

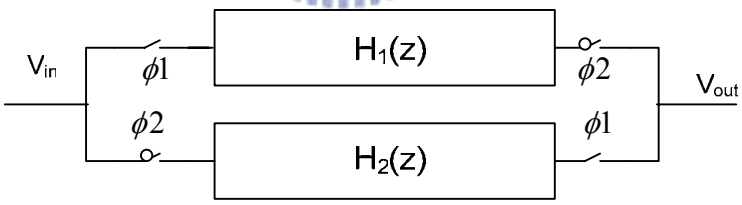


Figure 3.25 gain mismatch in the double sampling model

The nonoverlapping clock has a frequency of f_{clock} and the effective sampling frequency (f_s) of a double-sampled SC circuit is $f_s=2f_{clock}$. The sampling sequences can be divided into odd sampling (during $\phi 1$) and even sampling (during $\phi 2$). The odd and even sequences have a sampling frequency of $f_{clock} = f_s/2$. The input sequence vin can be represented by the sum of odd (v_{in}^o) and even (v_{in}^e) sequences in the

z-domain : [19]

$$V_{in}(z) = v_{in}^{o}(z) + v_{in}^{e}(z) \tag{3.19}$$

Similarly, the output sequence is expressed as

$$V_{out}(z) = v_{out}^{o}(z) + v_{out}^{e}(z) \tag{3.20}$$

where odd and even sequences are related by

$$v_{out}^{o}(z) = H_1(z)v_{in}^{o}(z) \qquad v_{out}^{o}(z) = H_2(z)v_{in}^{e}(z) \tag{3.21}$$

If the two paths are symmetric, we can get $H_1(z)=H_2(z)=H(z)$. If not, there is a gain mismatch of δ between them, the input-output relation is

$$V_{out}(z) = (1+\delta)H(z)v_{in}^{o}(z) + H(z)v_{in}^{e}(z) \tag{3.22}$$

Equation (3.22) can be rewritten as

$$V_{out}(z) = H(z)[V_{in}(z) + \delta v_{in}^{o}(z)] \tag{3.23}$$

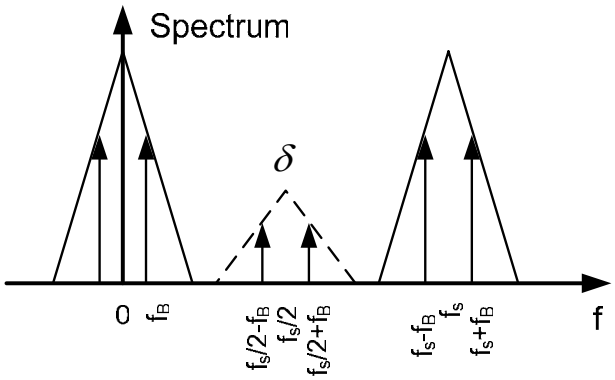
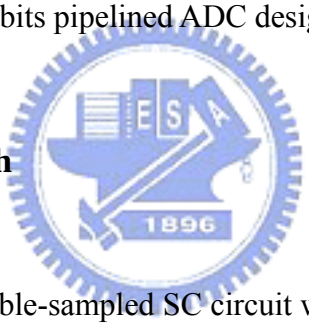


Figure 3.26 Spectrum of the input signal v_{in} (solid line) and the attenuated odd samples of the input signal (dotted line)

In the frequency domain, a sampled input signal V_{in} with a frequency f_B will have a periodic spectrum with the signal appearing at $nf_s \pm f_B$. However, the gain mismatch path samples the input signal at a rate of $f_s/2$ causing the input spectrum to be repeated periodically at intervals of $f_s/2$, as shown in Figure 3.26. Figure 3.26 shows the periodic spectrum of the input signals V_{in} and δv_{in}^{o}.

If the signal bandwidth exceeds fs/4, the sidebands alias to the signal band degrading the signal-to-noise ratio. Gain mismatch comes from capacitor mismatch in the double-sampled SC circuits. With careful sizing and layout, capacitor matching can be sufficient for the 10-12 bits pipelined ADC design.



3.7.2.4 Timming Mismatch

Clock generation for a double-sampled SC circuit with timming mismatch leads to nonuniform sampling. Besides, random sampling jitter or sampling time aperture uncertainty also results in nonuniform sampling.

The random sampling jitter is potentially an issue for single-sampled SC circuit as well as for double-sampled SC circuit. Because of its random nature the aperture uncertainty does not cause any fixed pattern tones in the output spectrum but degrades the signal-to-noise ratio.

The fixed sample time mismatches between two paths, contrary to the random sampling jitter, cause fixed side bands in the output spectrum. Assuming the path 1

deviates by ΔT from the path 2, shown in Figure 3.27, the output signal spectrum can be represented as follows:

$$Y(f)=\frac{1}{2T}\sum_{n=-\infty}^{\infty}X(f-\frac{n}{2T})\cdot\left[1+e^{-jn\pi}\cdot e^{j2\pi\Delta T(f-n/2T)}\right] \tag{3.24}$$

Comparing the output spectrum with timing mismatch and the output spectrum with gain mismatch it can be seen that both cause side bands around multiples of $f_s/2$. However, in the timming mismatch case, the magnitude of the side bands is frequency-dependant, seen from Eq (3.24). [20]

Figure 3.27 Timming mismatch in the double sampling model

Chapter 4

Design of Double-Sampling Pipelined Analog-to-Digital Converter

4.1 Introduction

The increasing range of wide-band wireless communication standards will evolve to high data rate applications within the next few years. At the same time, the boundary between analog and digital signal processing is moving closer to the antenna, following the trend toward software-defined radio. Therefore, high resolution and very high sampling rate analog-to-digital converters are required.

Traditional designs of high-speed CMOS analog-to-digital converters have used time-interleaved pipelined architectures to satisfy high resolution and very high sampling rate at the same time. While time-interleaved pipelined architectures usually yield the highest throughput rate, they trend to require four pipelined channels or even more to sample the input signal. If M channels are employed in the ADC and each channel has the sampling rate f_s, the highest throughput for the time-interleaved pipelined ADC can get up to M x f_s . However, large silicon area because of the more numbers of channels is required.

The double sampling technique has been introduced in 3.7. Employing double sampling technique in the pipelined ADC, a very competitive power and area consumption can be obtained. The double sampling pipelined ADC architecture has

been adopted in my design. With the double sampling technique, the architecture of the ADC is still based on the pipeline but an extra set of switches and comparators are required. It obvious that double sampling raises the conversion rate and lowers the slew rate and bandwidth requirements of the amplifier in a switched-capacitor gain stage.

4.2 Pipeline Stage Accuracy Requirements

To achieve the desired resolution, linearity, and signal-to-noise ratio, each stage must be designed such that non-ideal effects do not excessively degrade the overall performance. Capacitor matching, opamp gain, opamp bandwidth, opamp settling, and thermal noise are all critical to pipelined ADC performance. [21]

4.2.1 Opamp Requirements

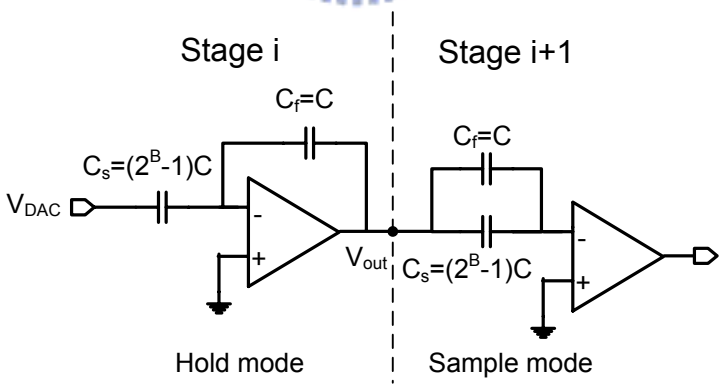


Figure 4.1 operation of pipeline stages implemented with identical stages

In the pipelined ADC, the accuracy requirement on each stage can be decreased by stages. For an N bit ADC with the effective per stage resolution of B-bit/stage, the first stage has to reach N bits accuracy requirement. And the accuracy requirements

for the following stages are reduced B bit per stage. Therefore, the lower stage constrains can be relaxed more.

In Figure 4.1, adjacent pipeline stages are illustrated that stage i is in the holding mode and stage i+1 is in the sampling mode. For a given total resolution of N bits, the per stage resolution of B, and finite opamp gain A, the resolutionship between the output and input of an interstage gain-amplifier can be written as :

$$V_{out} = G \cdot (V_{in} - V_{DAC}) \tag{4.1}$$

where
$$G = (1 + \frac{C_s}{C_F}) \cdot (1 - \varepsilon_{rr}) = (1 + \frac{C_s}{C_F}) \cdot \left(\frac{1}{1 + \frac{1}{Af}} \right) \tag{4.2}$$

$$f = \frac{C_f}{C_f + C_s + C_{opamp}} \tag{4.3}$$

$$\varepsilon_{rr} = \frac{1}{A} \cdot \frac{C_f + C_s + C_{opamp}}{C_f} \tag{4.4}$$

In Equation (4.2) and (4.3), ε_{rr} is gain error factor, f is feedback factor, and C_{opamp} is the input capacitance of the opamp. Because the i-th stage resolve B bit, the gain G_i of the i-th stage can be represented as

$$G_i = 1 + \frac{C_s}{C_f} = 2^B \tag{4.5}$$

In order to reach N-bit linearity, the gain error parameter in the interstage amplification should be less than $1/2^{N-B}$ of the full scale input range where N-B is the resolution of the next stage. Therefore, we can get

$$\varepsilon_{rr} < \frac{1}{2^{N-B}} \tag{4.6}$$

Substituting gain error factor ε_{rr} from Equation (4.4), the limit of finite opamp gain is yielded as follows

$$A > 2^{N-B} \times \frac{C_f + C_s + C_{opamp}}{C_f} = 2^{N-B} \times (2^B + \frac{C_{opamp}}{C_f}) = 2^N \cdot (1 + \frac{1}{2^B} \cdot \frac{C_{opamp}}{C_f}) \tag{4.7}$$

This is the minimum requirement on A. In practice, the opamp gain should be much large than this value, since error caused by other sources such as capacitor mismatches and incomplete amplifier settling are not taken into account.

The opamp finite bandwidth determines the maximum usable sampling rate in a pipelined ADC. Ignoring the slewing behavior, the MDAC settling time constant can be written as

$$\tau = \frac{1}{2\pi \cdot GBW} \cdot \frac{1}{f} \tag{4.8}$$

Since the settling error of a single-pole system has to be within $1/2^N$, the required number of time constants can be found as

$$e^{\frac{-T_{settle}}{\tau}} < \frac{1}{2^N} \tag{4.9}$$

$$T_{settle} > N \cdot \ln 2 \cdot \tau \tag{4.10}$$

For pipelined ADCs, the allowed settling time is a little less than 1/2 of a clock period. Then the minimum value for GBW of the amplifier is given by substituting τ from Equation (4.8)

$$GBW > \frac{N \cdot \ln 2}{2\pi \cdot f} \cdot \frac{1}{T_{settle}} \approx \frac{N \cdot \ln 2}{\pi \cdot f} \cdot F_s \tag{4.11}$$

where f is the feedback factor, and F_s is the sampling frequency. From the Equation (4.11), we can realize that the more resolutions and sampling rate of ADC is required, the larger gain-bandwidth product (GBW) is required to maintain the throughput rate of the pipelined ADC. [21]

4.2.2 Capacitor Requirements

In the pipelined ADCs, the sampling and feedback capacitors are related to the gain amplifiers and DACs, so capacitor matching is an important issue when choosing the capacitor size. If the capacitors C_s and C_f are not equal, gain error will be generated in the residue output and affects the accuracy of the pipelined ADC.

For an N bit ADC with the effective per stage resolution of B-bit/stage, the residue output is found as

$$V_{out} = (1 + \frac{C_s}{C_f})V_{in} \pm (\frac{C_s}{C_f})V_{DAC} \tag{4.12}$$

Assuming the capacitors deviate by ΔC and C_s=C+ΔC/2 C_f=C-ΔC/2, the residue output is given by

$$V_{out} = (2 + \frac{\Delta C}{C})V_{in} \pm (1 + \frac{\Delta C}{C})V_{DAC} \tag{4.13}$$

From Equation (4.13), the requirement on the DAC of each stage, and ΔC/C of each capacitor must be less than $1/2^N$ to ensure that ΔV_{DAC} is less than 1 LSB. Smaller capacitors tend to have worse matching, so the thermal noise kT/C limits the capacitor

size.[13]

As we know, the thermal noise is a major source of error in a pipelined ADC. The way to reduce thermal noise is to increase the size of the sampling capacitor Cs. But at the same time the power consumption of the ADC also increases. Therefore, there exists a tradeoff when choosing the capacitor size. In ADCs a common requirement is that thermal noise power is smaller than the power of the quantization noise, which can be shown to be $LSB^2/12$. This sets the lowest limit for capacitor value Cs as follows

$$C_s > \frac{kT \cdot 12}{LSB^2} = \frac{kT \cdot 12}{(2V_{FS})^2} \cdot 2^{2N} \tag{4.14}$$

where N is the number of in the ADC, which has full scale input signal V_{FS} and sampling capacitor size C_s. And the SNR of the ADC when considering thermal noise and quantization noise can be calculated as

$$SNR = 10\log\left(\frac{V_{FS}^2/2}{\frac{LSB^2}{12}+\sigma^2}\right) = 10\log\left(\frac{V_{FS}^2/2}{\frac{(2V_{FS}/2^N)^2}{12}+\frac{kT}{C_s}}\right) \tag{4.15}$$

4.3 Behavior Model of the Double-Sampling Pipelined ADC

In order to understand the operation of the double-sampling pipelined ADC in detail, the behavior model of a 10-bit double-sampling pipelined ADC with 1.5-bit/stage architecture is established with Simulink in Matlab. The sample rate of the 10-bit double-sampling pipelined ADC is set in 100MHz for each path. With the double sampling technique, the total throughput rate can be doubled toward 200MHz.

For simplicity, the single ended configuration is adopted. We describe each block including SHA circuit, sub-ADC, MDAC, final stage 2-bit flash ADC, and digital error correction. With ideal mathematical analysis, each block of the ADC is constructed with some nonideal properties. [22]

4.3.1 SHA Circuit

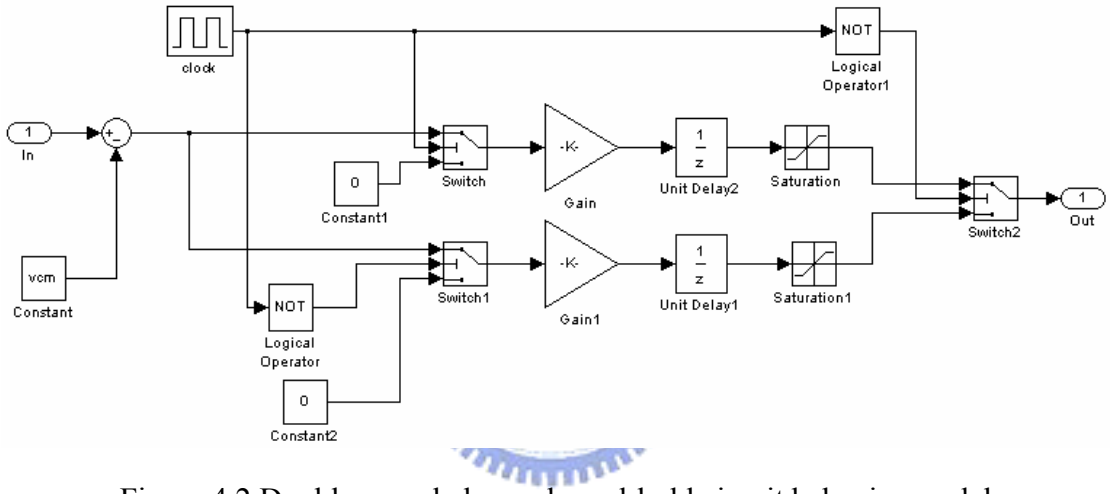


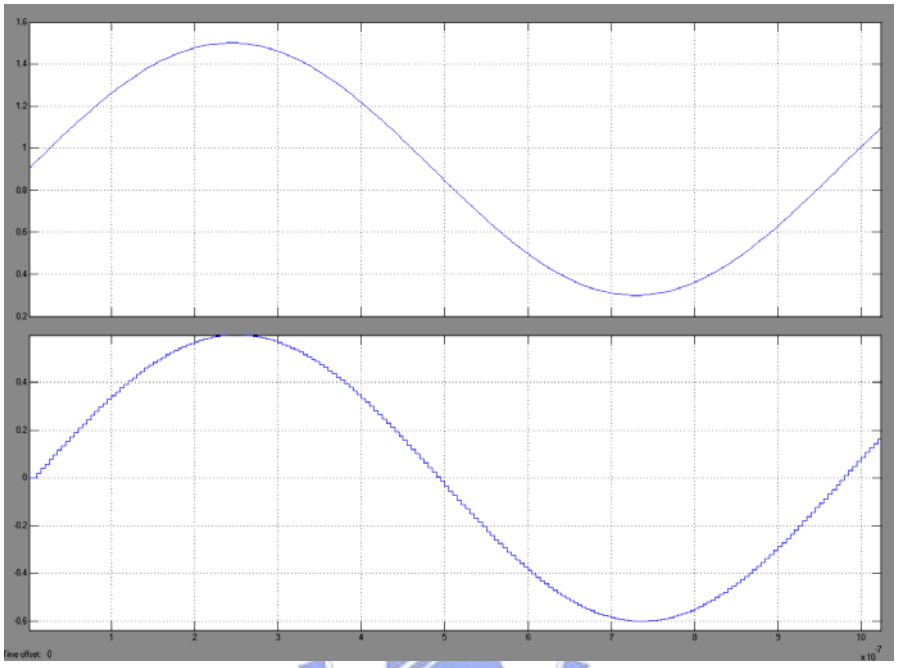
Figure 4.2 Double-sampled sample-and-hold circuit behavior model

With the application of double sampling technique, the sample-and-hold (SHA) circuit behavior model is illustrated in Figure 4.2. The behavior model is constructed according to the transfer function and characteristic of SHA. The mathematical equation is shown in Equation (4.16).

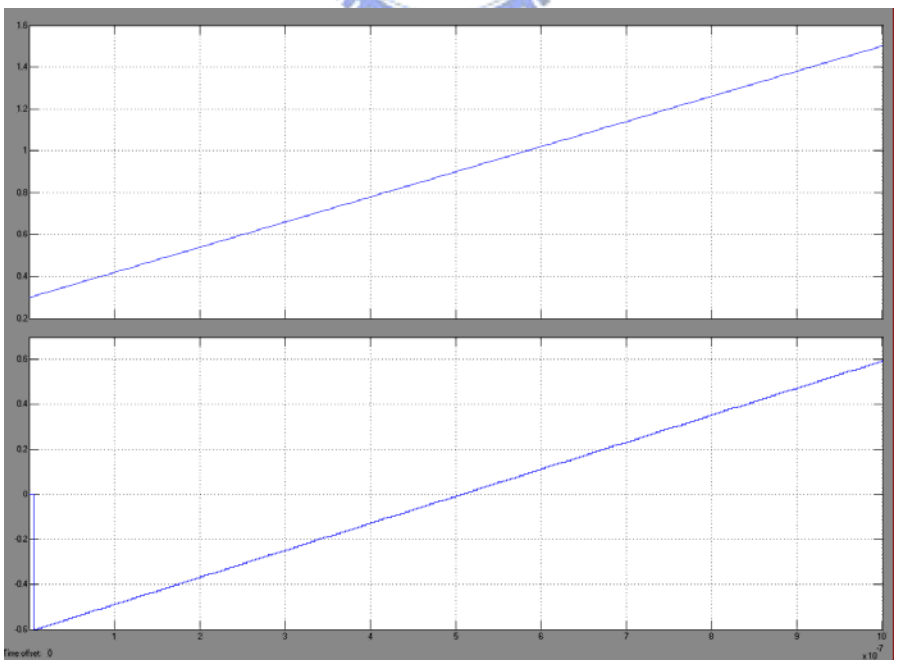
$$V_{out} = \frac{1}{1+\frac{1}{A}(1+\frac{C_{in}}{C_s})} V_{in} Z^{-1} \tag{4.16}$$

where Cs is sampling capacitor and it is in the feedback loop when in then holding phase. A is the finite opamp gain and Cin is the input capacitor of the amplifier. The

input signal is sampled by two paths in turn depending on the nonoverlapping clolck phases, 100MHz. The simulated results are illustrated in Figure 4.3 (a)(b), which show the transfer curve of the input signal of the sine wave and ramp respectively.



(a)



(b)

Figure 4.3 the transfer curve for the input signal of (a) 1M sine wave (b) ramp

4.3.2 Sub-ADC

Figure 4.4 shows the behavior model of sub-ADC. It consists of two comparators with ±1/4Vref threshold voltage and offset. D1 and D0 are MSB and LSB of the sub-ADC respectively. VDAC is the voltage to control the MDAC operation. Figure shows the digital output codes of MSB and LSB for the input signal of sine wave and ramp.

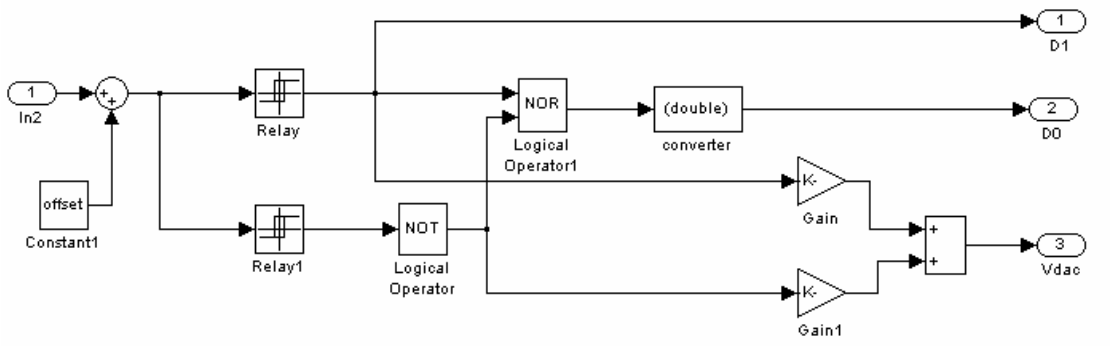
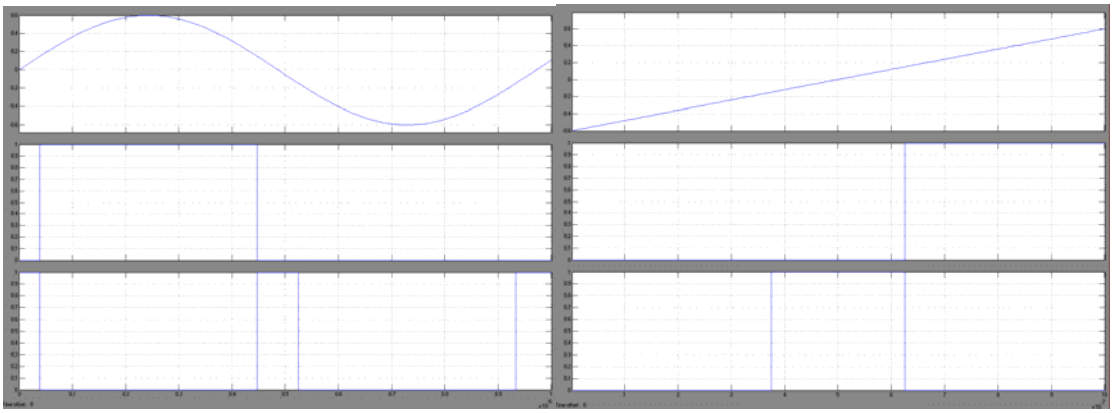


Figure 4.4 Sub-ADC behavior model



(a) (b)

Figure 4.5 the input signal of (a) 1M sine wave (b) ramp versus digital output codes of MSB and LSB

4.3.3 MDAC

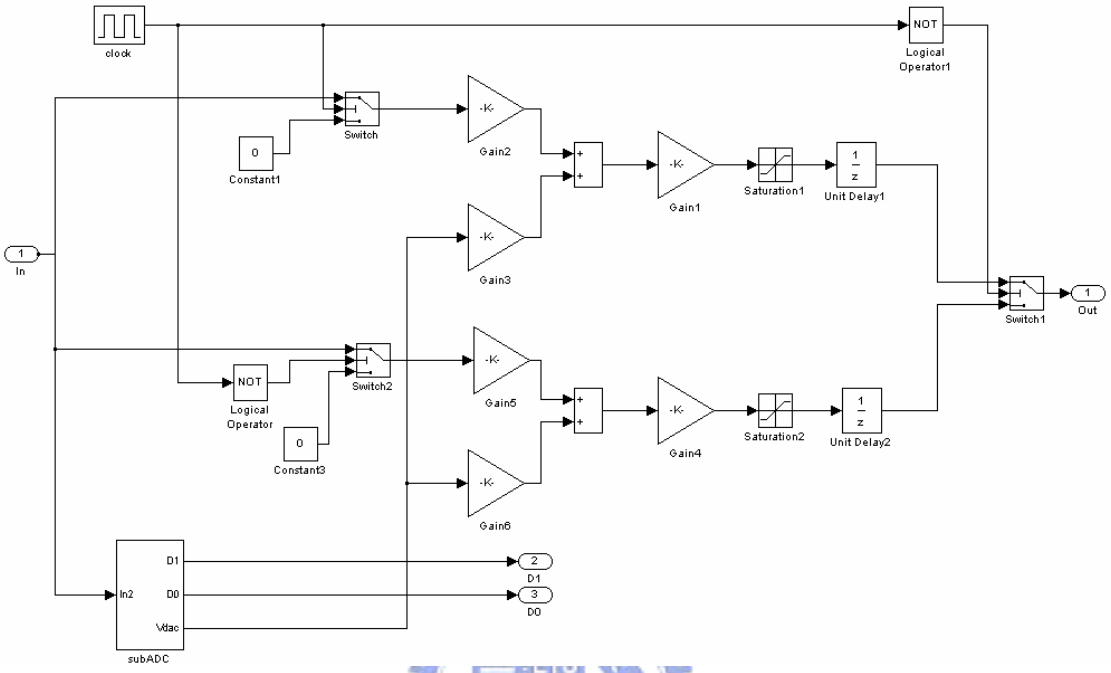
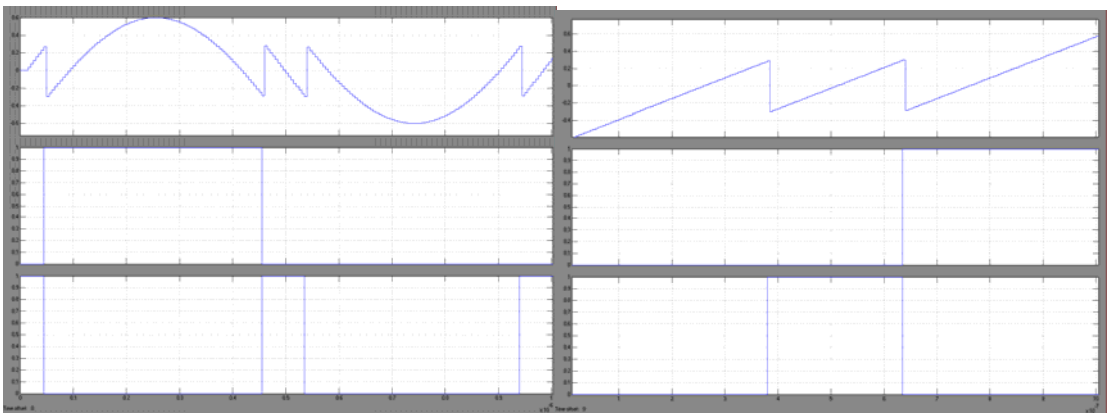


Figure 4.6 MDAC behavior model

The MDAC of double sampling pipelined ADC is modeled in the Figure 4.6. It is modeled in two paths, as in the SHA, according to the transfer function and characteristic of MDAC. The mathematical equation is shown in Equation (4.17).

$$V_{out} = \frac{\left[(C_s + C_f)V_{in} + C_s V_{DAC}\right]}{C_f + \frac{C_s + C_f}{A}} Z^{-1} \qquad (4.17)$$

where Cs is the sampling capacitor, Cf is the feedback capacitor, and A is the finite gain of the amplifier. The simulated results are illustrated in Figure 4.7 (a)(b), which show the transfer curve of the input signal of the sine wave and ramp respectively.



(a) (b)

Figure 4.7 the output residue and ital output codes of MSB and LSB for the input signal of (a) 1M sine wave (b) ramp

4.3.4 2-Bit Flash

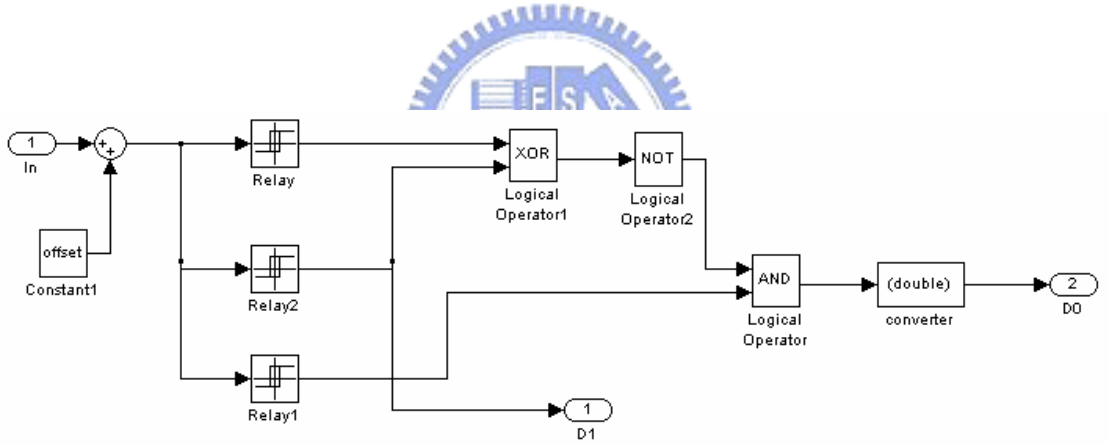


Figure 4.8 2-bit flash behavior model

The final stage of the double sampling pipelined ADC is the 2-bit flash. The MSB and LSB is yielded in this stage without the need of the digital error correction. Figure 4.8 illustrates the 2-bit flash behavior model. The transfer curve of the MSB and LSB is shown in Figure 4.9.

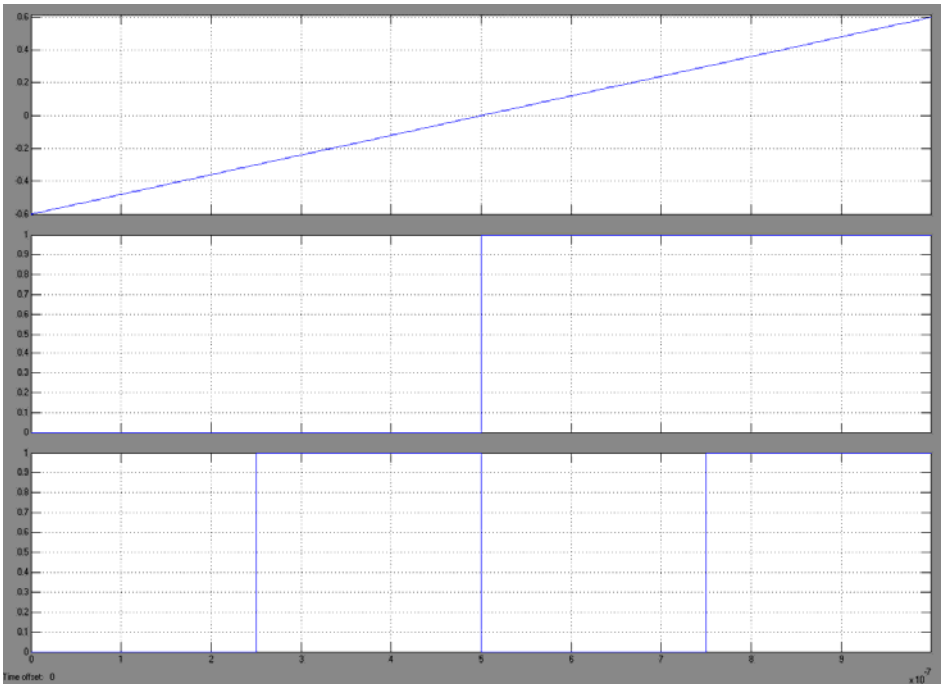


Figure 4.9 Transfer curve of the MSB and LSB versus the input voltage

4.3.5 10-Bit Double-Sampling Pipelined ADC

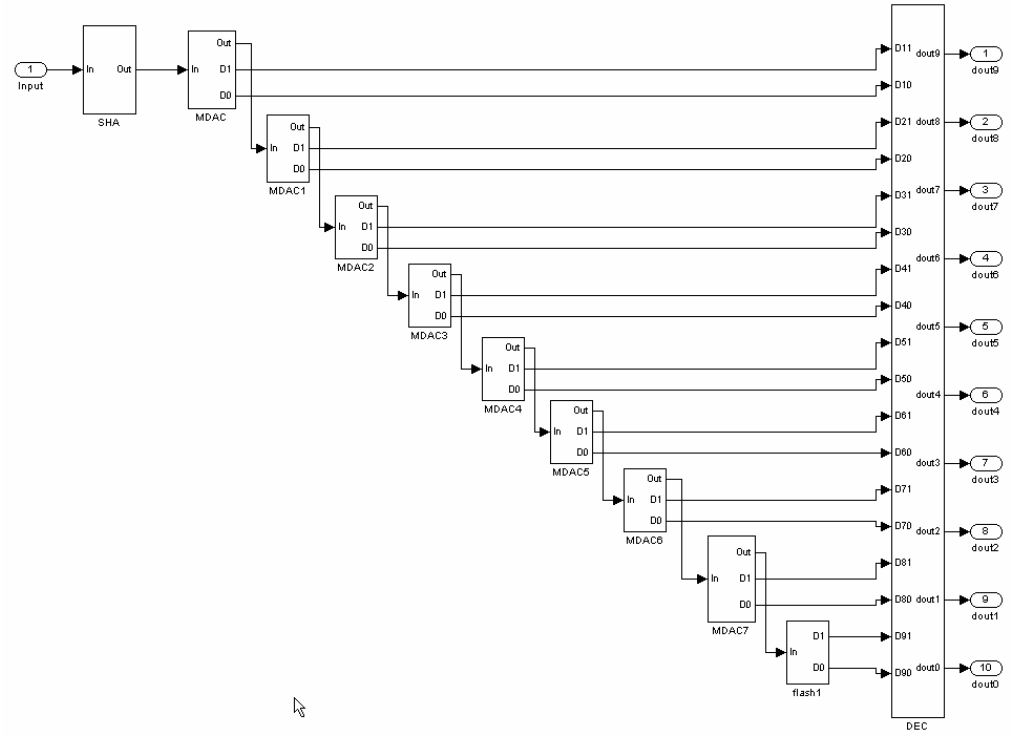


Figure 4.10 10 bit double-sampling pipelined ADC behavior model

Figure 4.10 shows the behavior model of the 10 bit double-sampling pipelined ADC, which is made up of a SHA, 8 MDACs, a 2-bit flash, and a digital error correction logics.

4.3.6 Ideal DAC Reconstructed Waveform

Figure 4.11 shows the behavior model ideal DAC which is used to reconstructed the input signal of the pipelined ADC. The digital output code of the pipelined ADC can be transformed into the analog result in binary weighting by the ideal ADC.

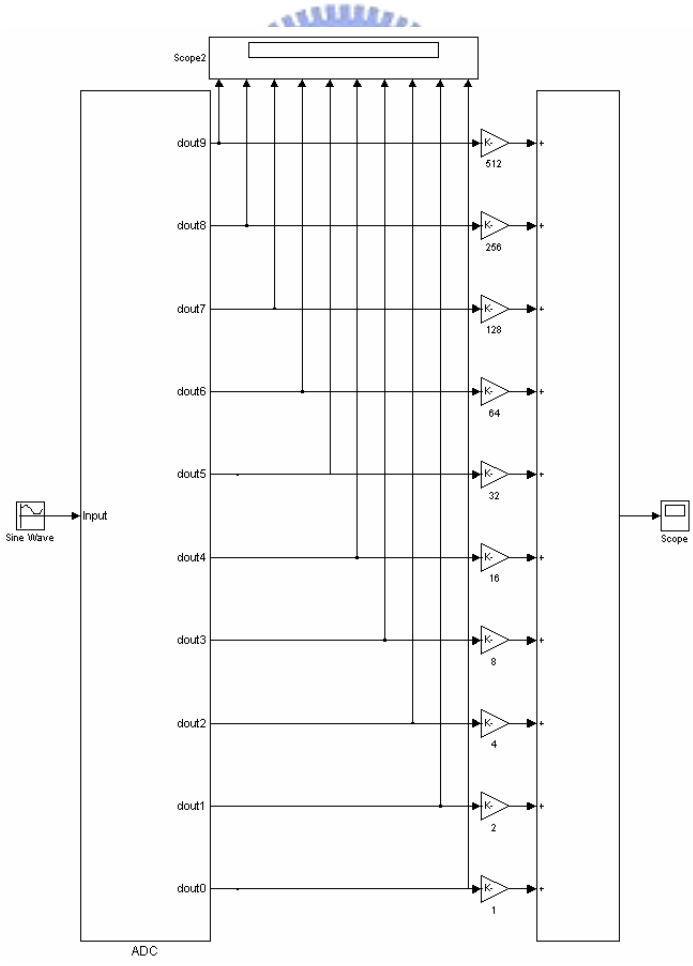
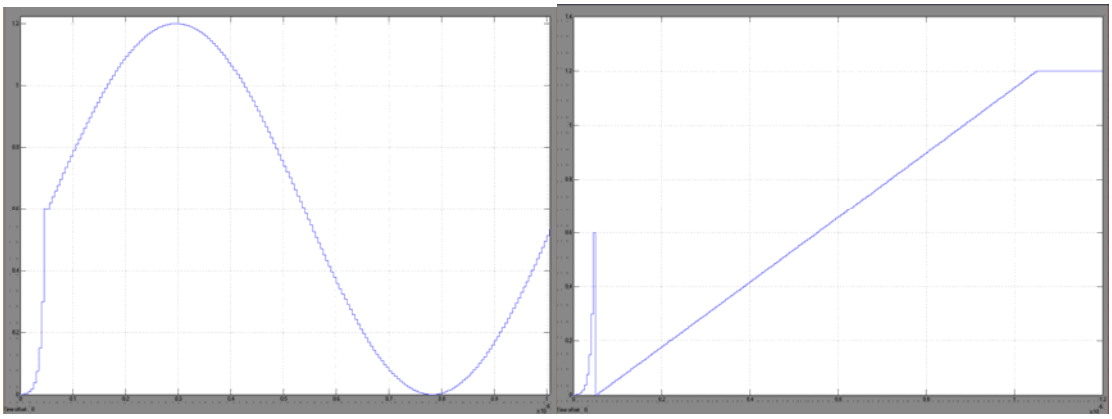


Figure 4.11 The reconstructed behavior model by a ideal DAC



(a) (b)

Figure 4.12 The reconstructed waveform of (a) sine wave (b) ramp

Figure 4.12 (a)(b) show the constructed waveform of the sine wave and ramp respectively. By the ideal ADC, the performance of the pipelined ADC can be determined by comparing the input signal with the reconstructed waveform and analyzing the spectrum of the output signal.

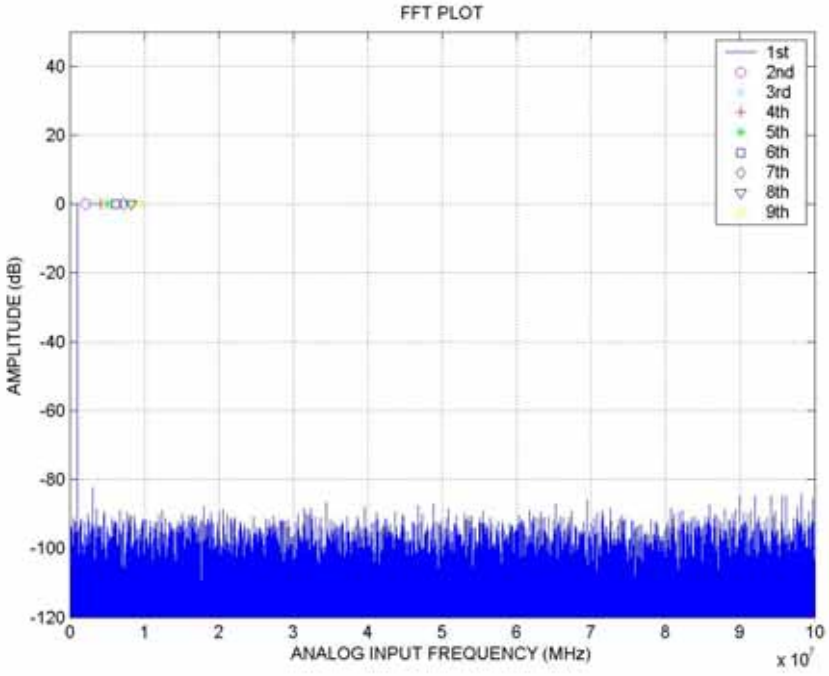


Figure 4.13 The output spectrum of the sine wave

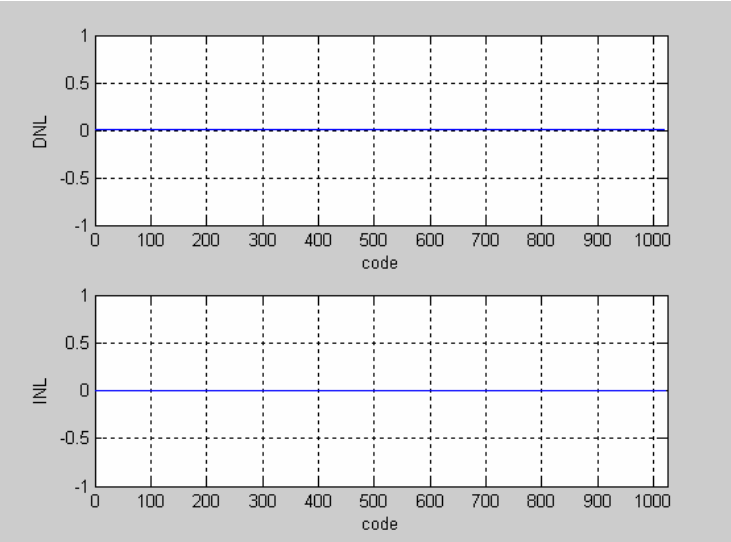
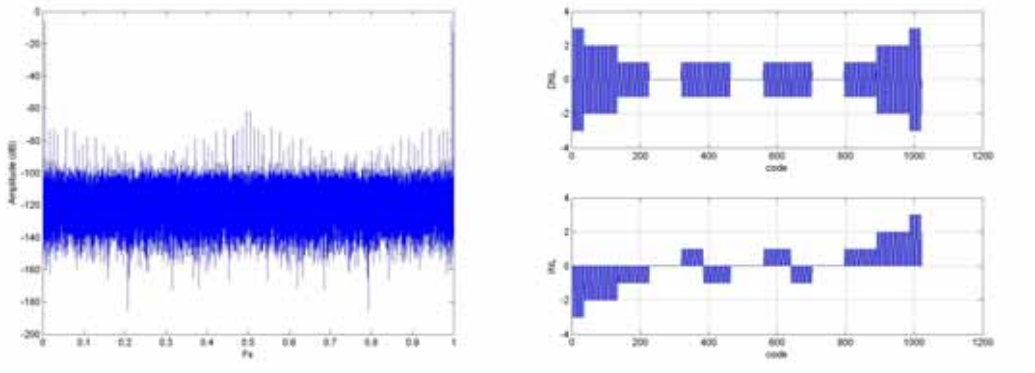


Figure 4.14 DNL and INL versus code

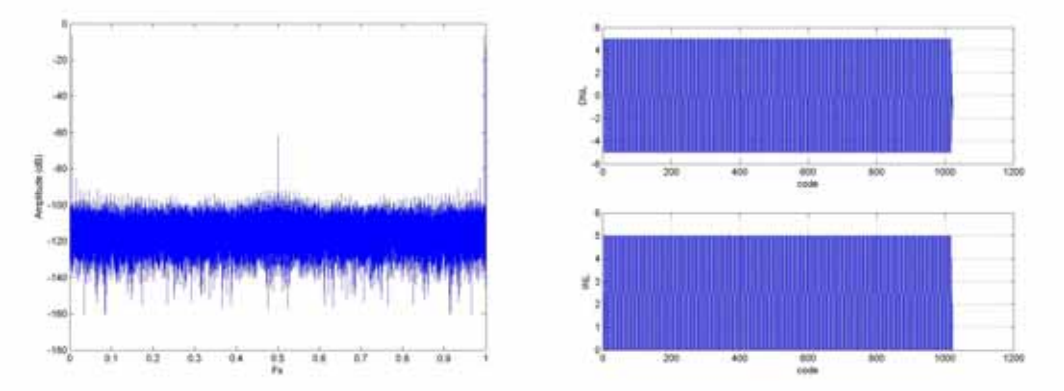
Figure 4.13 shows the output spectrum of the sine wave with the frequency of 1.028MHz. With the finite opamp gain 60dB, it shows the SNDR is 61dB. Figure 4.14 illustrates the DNL and INL which are almost 0 LSB while no offset is added.

4.3.7 Mismatch Considerations



(a) (b)

Figure 4.15 Gain mismatch (1%) (a) FFT spectrum (b) DNL & INL



(a) (b)

Figure 4.16 Offset mismatch (1%) (a) FFT spectrum (b) DNL & INL

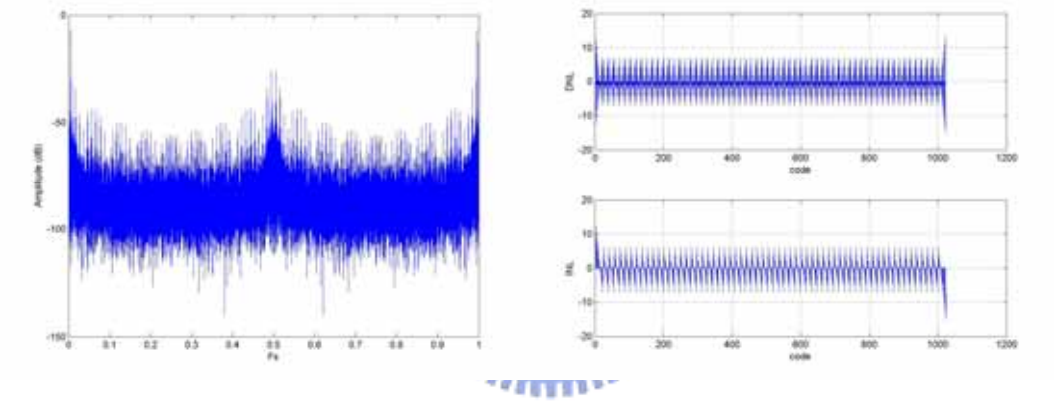


Figure 4.17 Timming mismatch (1%) (a) FFT spectrum (b) DNL & INL

Considering the mismatches between the two paths, the FFT spectrum and DNL&INL plot are illustrated in Figure 4.15, Figure 4.16, and Figure 4.17, respectively. [18] [20] [29]

4.4 The Implementation of 10-Bit Double-Sampling Pipelined ADC

Having determined the optimal double-sampling pipelined A/D architecture, the implementation of this architecture is described in this section. The prototype of a 10-bit 200MSPS double-sampling pipelined ADC has been implemented on the

TSMC 0.18um CMOS 1P6M process technology. The digital power supply and analog power supply are 1.8V.

The double-sampling pipelined ADC is composed of the front-end SHA, 8 MDACs in stages, final 2-bit flash, and digital error correction logics. And operational amplifiers are applied in the SHA and MDACs of eight stages. All analog circuits are fully differential. The advantages of the fully-differential circuit are that it can reduce even-order harmonic distortion, substrate noise, and common-mode disturbances. It also improves the power supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR). One drawback in the fully-differential circuit is that it needs the common-mode feedback circuit and it will be illustrated in the following sections.

4.4.1 Operational Amplifier

The opamp is the most important element in the SHA and every stage of the pipelined ADC. However, many limitations such as finite gain, bandwidth, stability, and linearity have to be considered when designing the opamp. To speed the converting rate of the pipelined ADC, the frequency bandwidth of the op-amp need to be increased. To improve the resolutions of the pipelined ADC, we have to increase the dc gain of the op-amp. Therefore, the specifications of the opamp require high gain and wide bandwidth so as to reach the demands of the high resolution and high throughput rate. Through it is a tradeoff between the opamp gain and bandwidth.

A two-stage opamp may achieve higher DC gain than a single-stage amplifier. However, the optimal design can be achieved by using single-stage amplifier topology, because it has higher bandwidth and smaller power consumption. Therefore, the

opamp is implemented as a fully differential folded cascade amplifier, a close relative of the telescopic with a slightly better output swing. It allows the DC level of the output signal to be the same as the DC level of the input signal.

The folded cascode op-amp is shown in Figure 4.18. For the requirement of higher resolution accuracy, it is necessary to use the op-amp open-loop gain enhancement technique to increase the dc gain of the op-amp. This method is called gain-boosting, and the theory will be illustrated as follows. [23] [24] [25]

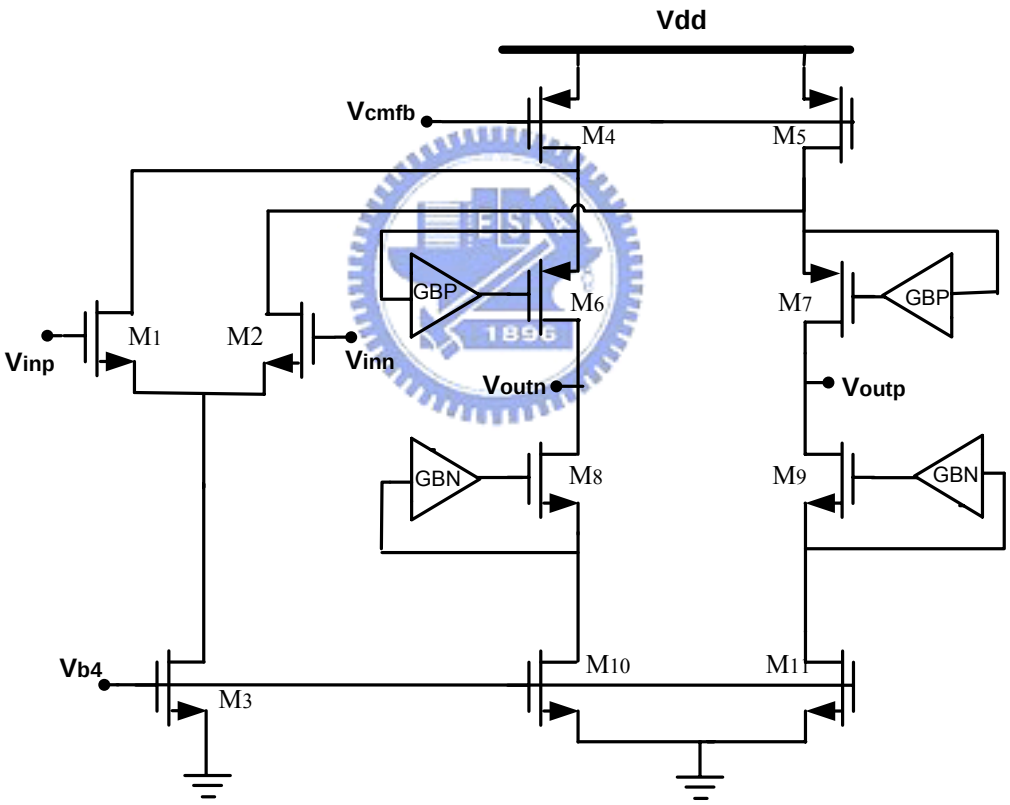


Figure 4.18 Fully-differential folded cascode op-amp with gain boosting

The dc gain of the fully-differential folded cascode op-amp without gain boosting can be written as

$$|A_v| = G_m \times R_{out} . \qquad (4.18)$$

$$R_{out} = \left[\left(g_{m9} + g_{mb9} \right) r_{o11} r_{o9} \right] \| \left[\left(g_{m7} + g_{mb7} \right) r_{o7} \left(r_{o2} \| r_{o5} \right) \right]. \quad (4.19)$$

The transconductance G_m is approximately equal to g_{m2}. Substituting equation (4.19) into equation (4.18), we obtain

$$\left| A_v \right| = g_{m2} \left\{ \left[\left(g_{m9} + g_{mb9} \right) r_{o11} r_{o9} \right] \| \left[\left(g_{m7} + g_{mb7} \right) r_{o7} \left(r_{o2} \| r_{o5} \right) \right] \right\}. \quad (4.20)$$

With the application of gain boosting the output impedance of the folded-cascode opamp is further increased without adding more cascade devices. Assuming that the GBP and GBN have the feedback loops, and they are the gain boosting amplifiers of PMOS and NMOS respectively. We can derive the output impedance enhanced by gain boosting amplifiers as

$$R_{out} = \left[A_{GBN} \left(g_{m9} + g_{mb9} \right) r_{o11} r_{o9} \right] \| \left[A_{GBP} \left(g_{m7} + g_{mb7} \right) r_{o7} \left(r_{o2} \| r_{o5} \right) \right] \quad (4.21)$$

And the dc gain can be rewritten as

$$\left| A_v \right| = g_{m2} \left\{ \left[A_{GBN} \left(g_{m9} + g_{mb9} \right) r_{o11} r_{o9} \right] \| \left[A_{GBP} \left(g_{m7} + g_{mb7} \right) r_{o7} \left(r_{o2} \| r_{o5} \right) \right] \right\} \quad (4.22)$$

Because of the single-stage topology, the second pole is far away from the unity-gain frequency. Assuming the output capacitance and resistance are C_L and R_{out}, the frequency response of the folded-cascode opamp is derived by

$$A(s) = \frac{g_{m2} R_{out}}{1 + s R_{out} C_L} \quad (4.23)$$

For the high frequency response, because of $sR_{out}C_L >> 1$ we can get the transfer function as follows

$$A(s) = \frac{g_{m2}}{sC_L} \tag{4.24}$$

The unity-gain frequency is given by

$$|A(s)| = \left|\frac{g_{m2}}{sC_L}\right| = 1 \tag{4.25}$$

$$\omega_u = \frac{g_{m2}}{C_L} \tag{4.26}$$

Since the folded-cascode opamp is adopted in fully-differential, it is therefore necessary to add additional circuitry to determine the output common-mode voltage and to control it to be equal to some specified voltage, usually about halfway between the power-supply voltages. This circuitry, referred to as the common-mode feedback (CMFB) circuitry, takes an important role in the feedback loop of the opamp.

To avoid the signal swing limit, a switched-capacitor common-mode feedback (SC-CMFB) circuit is applied into the folded-cascode opamp. A switched-capacitor common-mode feedback (SC-CMFB) circuit offer very wide input dynamic range, high linearity, and inherent stability with no power consumption. [26]

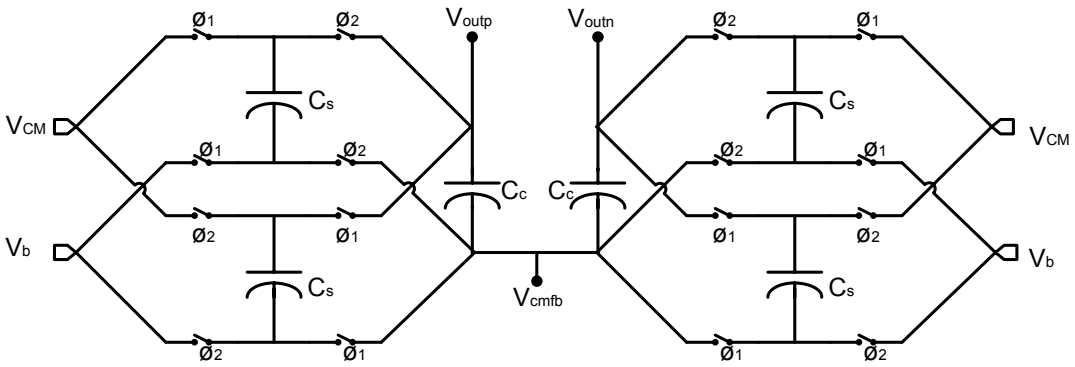


Figure 4.19 Dual-phase switched-capacitor CMFB circuit

The main advantages of SC-CMFB are that they impose no limits on the maximum allowable differential input signals, have no additional parasitic poles in the CM loop, and are highly linear. However, SC-CMFB injects nonlinear clock-feedthrough noise into the op-amp output nodes and increases the load capacitance that needs to be driven by the op-amp. Hence, SC-CMFB is typically only used in switched-capacitor applications such as sample-and-hold amplifier and SC-filter. The dual-phase switched-capacitor common-mode feedback (SC-CMFB) circuit is shown in Figure 4.19.

In Figure 4.19 it duplicates the sampling capacitors Cs, and interchanges its driving switch clocks. This scheme continuously refreshes capacitor Cc during both clock phases, and assures the same loading and same CM feedback factor. Capacitors Cc generate the average of the output voltages, which is used to create control voltages for the opamp current sources. The dc voltage across Cc is determined by capacitors Cs, which are switched between bias voltages and between being in parallel with Cc. The bias voltages are designed to be equal to the difference between the desired common-mode voltage and the desired control voltage used for the opamp current sources.

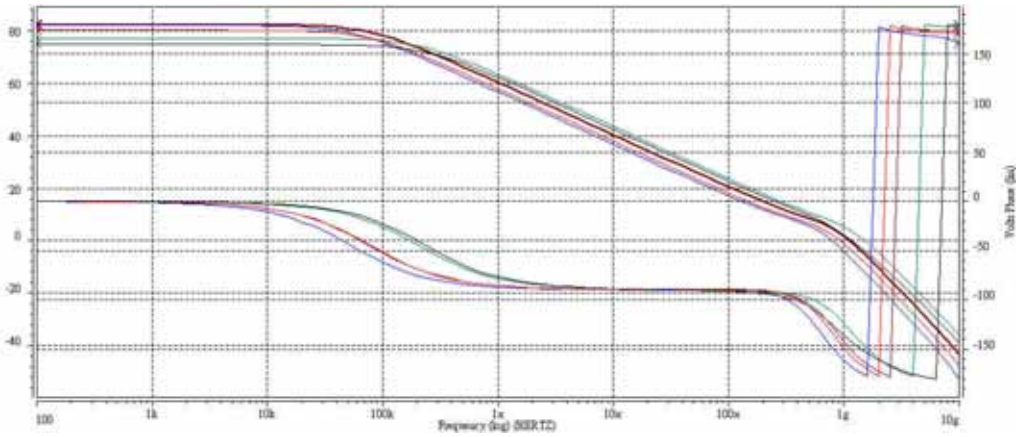


Figure 4.20 Simulated AC results of the op-amp

Figure 4.20 shows the AC simulation results including the gain and phase margin of five process corners (TT, FF, FS, SF, SS), which are summarized in Table 4.1. The simulated performance of the fully-differential folded cascode op-amp is summarized in Table 4.2.

	TT	SS	SF	FS	FF
Gain (dB)	82.38	83.24	79.65	83.33	78.87
Phase (deg)	65.25	67.75	65.13	66.57	64.32
Unity GB(MHz)	721.5	678.7	698.5	742.5	785.4

Table 4.1 Simultated performance of opamp in five process corners

Folded-Cascode Op-amp(TT process corner)		
DC Gain		82.38dB
Phase Margin		65.25°
Unity Gain Bandwidth		721.5MHz
Load Capacitor		2pF
Common Mode Input Range		0.3V~1.4V
Output Swing		0.35V~1.45V
Slew Rate	Rise	302V/μs
	Fall	311V/μs
Settling Time		4.12ns
Power Dissipation		8.43mW
Process		TSMC 0.18μm 1P6M Process

Table 4.2 Summary of the simulation results of the op-amp

4.4.2 Bootstrapped Switches

The decreasing maximum supply voltage of integrated circuits has made the driving of an MOS transistor switch with sufficient over-drive difficult. A widely used method to improve the linearity is to bootstrap the switch transistor gate voltage to reduce the on-resistance signal dependency. Figure 4.21 shows the well known gate-source bootstrapping technique. During the clock phase $ø_2$ when the transistor is non-conductive the capacitor C is precharged to V_{DD}-V_{SS}. To turn the switch on, the capacitor is switched between the input voltage and the transistor gate. This advantage is that the constant R_{ON} due to the fixed V_{GS} makes the time constant $\tau=R_{ON}\times C$ independent of the input signal. This will decrease the harmonic distortion. The fixed V_{GS} also eliminates the high gate oxide voltage when the input signal is low. Switch S5 fixes the gate voltage of MNSW to V_{SS} during $ø_2$ to make sure that the transistor is in the OFF state. [27]

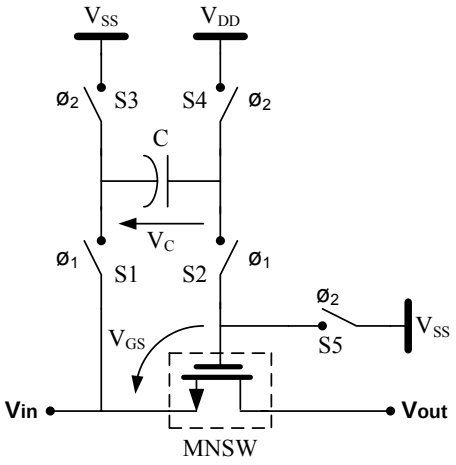


Figure 4.21 Basic circuit of the bootstrapped switch

Figure 4.22 shows the transistor-level implementation of the bootstrapped-switch

circuit shown in Figure 4.21. The offset voltage is realized with the capacitor C, which is precharged to Vdd during the main switch off-period. To turn on the switch MS, the precharged capacitor is connected between its source and gate via the series switches M1 and M4. Turning off MS is performed by disconnection the capacitor C and pulling down the gate with M6. The transistor M5 is needed to prevent the gate-source voltage of M6 from exceeding Vdd. The gate of PMOS transistor M3 is tied to the gate of MS. The simulated result is illustrated in Figure 4.23 for an input signal of sine wave.

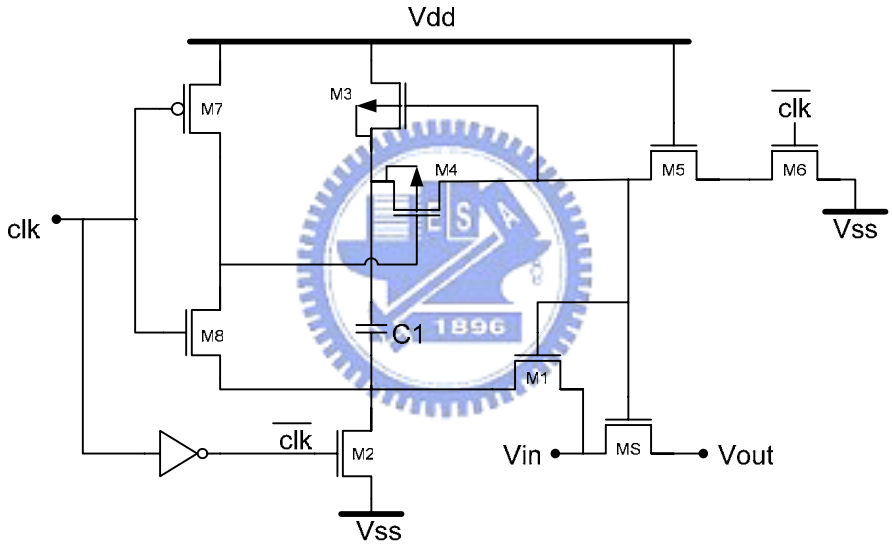


Figure 4.22 Transistor-level implementation of the bootstrapped switch

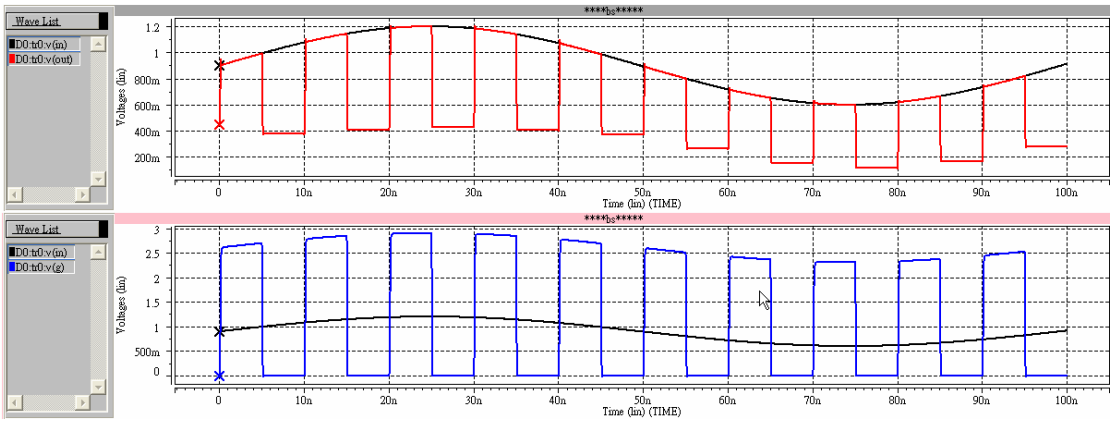


Figure 4.23 The simulated result of the bootstrapped switch

4.4.3 Double-Sampled Sample and Hold Amplifier

The accuracy and speed of ADC critically depends on the performance of front-end sample and hold amplifier. The sample-and-hold amplifier needs to acquire a wideband input signal, and drive the large load capacitance of the next stage with low distortion. Also with the double-sampling technique skew in the timming of the signals controlling the switches may deteriorate the circuit performance. To overcome the timming skew problem a modification circuit, which makes the double-sampled circuits insensitive to the timming errors, is applied in the double-sampled sample-and-hold circuit. [28] [29] [30]

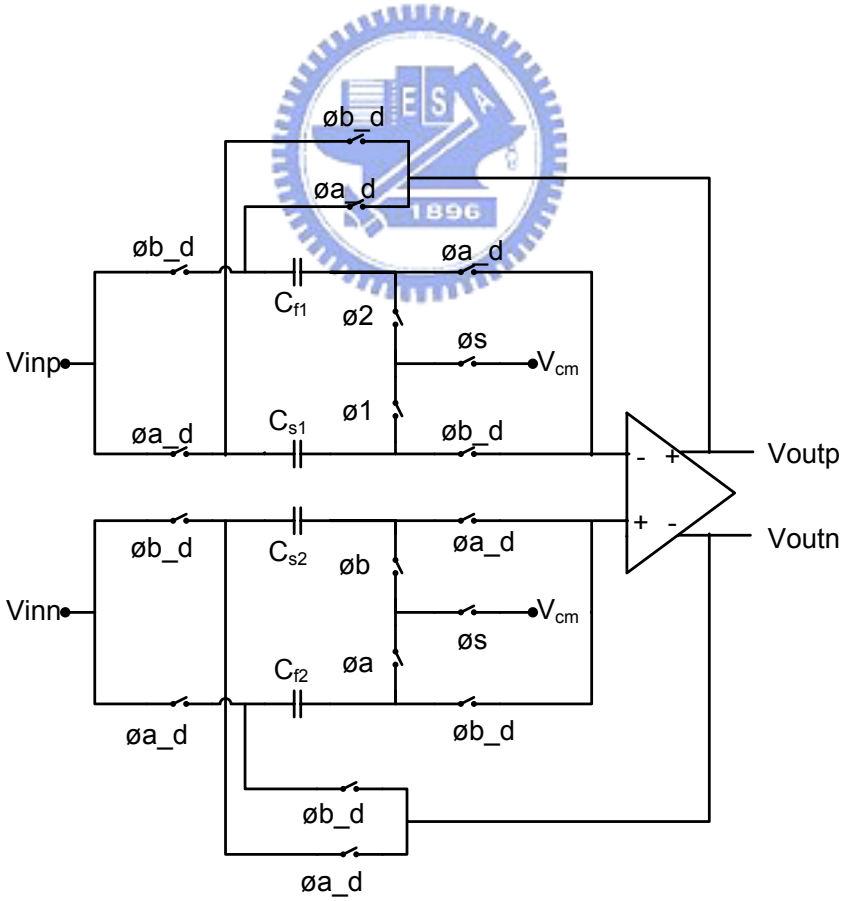


Figure 4.24 Timming skew-insensitive double-sampled S/H circuit

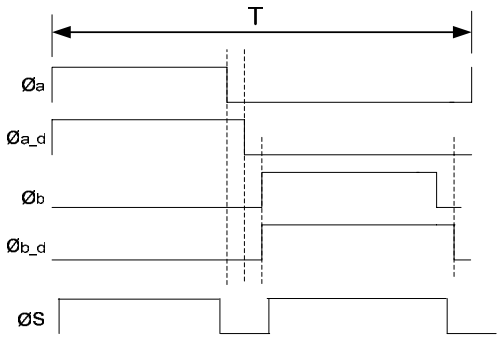


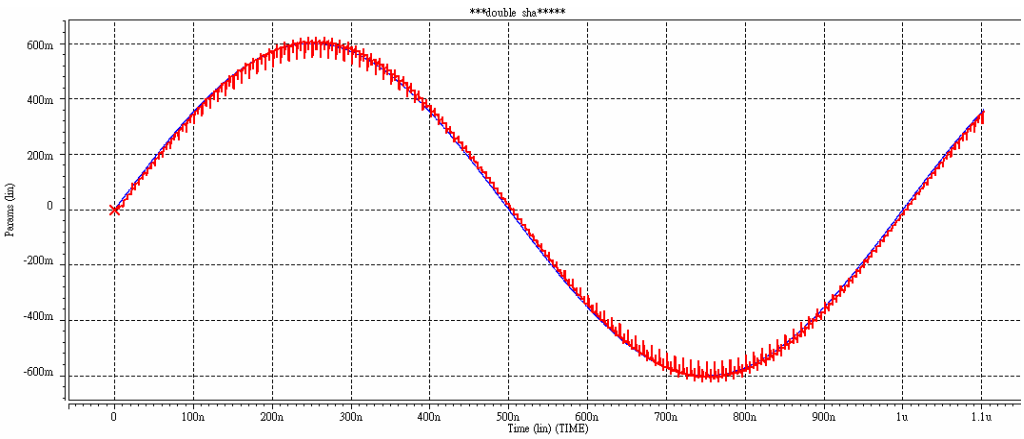
Figure 4.25 Timming diagram of the S/H circuit

The front-end double-sampled sample-and-hold circuit is designed fully-differentially and shown in Figure 4.24. The main idea in the double-sampling is to make the utilization of the opamp more efficient. This is done by sharing the opamp with two parallel circuits, which is possible because the opamp is needed only during one half of the clock cycle. While the input signal is sampled into one set of the capacitors, the other is holding the previous sample being connected in feedback around the amplifier. In the next cycle the roles of the capacitors are changed.

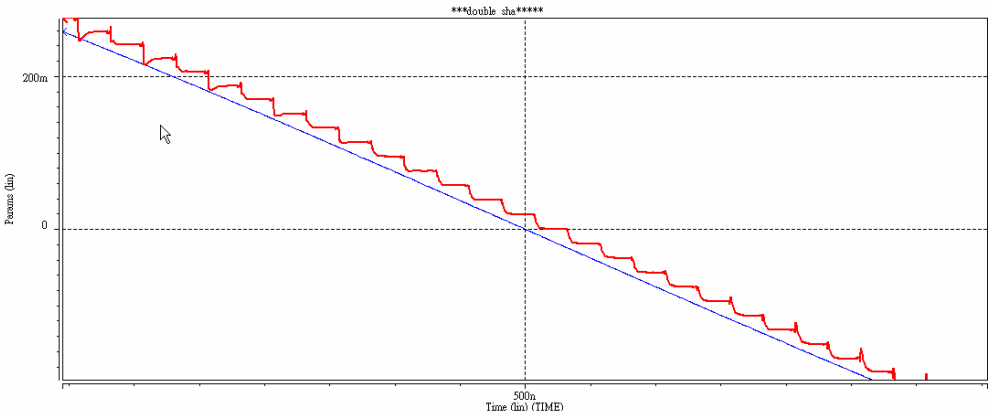
In order to remove timming skew errors in double-sampled circuit, the separate sampling switches of the parallel sampling circuits are replaced with a single switch, which is common for both the sampling circuits. And two additional switches, which act as a multiplexer, and a clock phase $ø_s$ are added. The sample is taken by applying a short zero pulse to the sampling switches as shown in Figure 4.25. Each sampling pulse is generated with the same edge of a full speed clock signal and thus any systematic timming error between the channels is avoided. The load capacitance of the S/H circuit is minimized by allowing only one component ADC to be connected in the S/H output at a time. The price is the need for extra clock signals in the frond-end S/H circuit.

Since the sampling capacitor in the double-sampled SHA is the same with the feedback capacitor, the gain error will not result from the capacitance mismatch. Bootstrapped switches are used in the S/H circuit to reduce harmonic distortions and improve the SFDR of the ADC.

Figure 4.26 shows the simulation result of the SHA when applying the sine-wave input of 1MHz (frequency) with the amplitude of ±600mV. Figure 4.26(b) is the zoom-in result of Figure 4.22(a).



(a)



(b)

Figure 4.26 Simulated result of the S/H sampling the input sine-wave

4.4.4 Sub-ADC

4.4.4.1 Comparators

In many ADC designs, dynamic comparators using low-powered, cross-coupled inverter latches have a drawback of intolerable offset voltages and mismatches due to process variations, but in the 1.5 bits-per-stage pipline, a ±Vref/4 of comparator offset can be corrected using the digital correction logics. Thus a dynamic latch may be used in the system of pipelined ADC.

In order to make a dynamic comparator against mismatch and process variations all transistors should be in saturation straight after the latching signal. The comparator, based on two cross coupled differential pairs and switchable current sources, has a small power and area dissipation and it is shown to be very insensitive to transistor mismatch. A fully-differential CMOS dynamic comparator for pipelined ADC with a low stage resolution is implemented in Figure 4.27. [31] [32] [33]

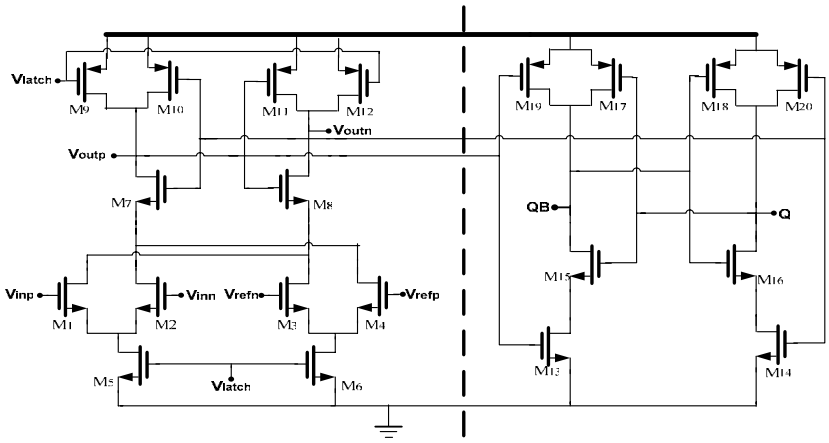


Figure 4.27 Schematic diagram of comparator circuit

The comparator consists of two cross coupled differential pairs M_1~M_4, the current source transistors M_5 and M_6, and latches M_7~M_{12}. The operation of the comparator is as follows:

When V_{latch}=0V, transistors M5 and M6 are inactive and no current path between the supply voltages exists. Simultaneously the switch transistors M_9 and M_{12} reset the outputs by shorting them to V_{dd}. The transistors M_7 and M_8 of the latch conduct and force the drains of all the input transistors M_1~M_4 to V_{dd}.

When the V_{latch}=V_{dd}, the outputs are disconnected from the positive supply and the switching current sources M_5 and M_6 enter saturation and begin to conduct. The two cross-coupled differential pairs M1~M4 start to compare the threshold with the input voltage. When the transistors M7 and M8 are active and amplify the difference of the source voltage in the cross-coupled differential pair. The transistors M5 and M6 determine the bias currents of the two differential pairs M_1 - M_2 and M_3 - M_4, respectively. Therefore, the threshold voltage of the comparator is determined by the current division in the differential pairs and between the cross coupled branches.

The output of the comparator has only two conditions. One condition is M7 and M11 is active but M8 and M10 is inactive. The other is M8 and M10 is active but M7 and M11 is inactive. Thus the comparator is free of static power consumption. The determination of the switching point of the comparator can be modeled with the simplification of Figure 4.28 for the two cross coupled differential pairs. Using the symbols indicated in the figure and having W1=W2, W3=W4 the transistors M1-M4 follow the large signal current equations:

$$I_{D1} - I_{D2} = \beta_1 V_{in} \sqrt{\frac{2I_{D5}}{\beta_1} - V_{in}^2} \tag{4.27}$$

$$I_{D4} - I_{D3} = \beta_3 V_{ref} \sqrt{\frac{2I_{D6}}{\beta_1} - V_{ref}^2} \tag{4.28}$$

where $\beta_i = (1/2)K'(W_i/L) = (1/2)\mu_0 C_{ox}(W_i/L)$, $V_{in}=V_{in}^{+}-V_{in}^{-}$ and $V_{ref}=V_{ref}^{+}-V_{ref}^{-}$. The comparator changes its stage when the currents I_{o1} and I_{o2} of the both output branches are equal. Assuming the relation of the source coupled pair bias currents to be I_{D5}=d I_{D6} and by making the threshold point with parameter e so that V_{in}=e V_{ref}, this results in a condition from (4.27) and (4.28):

$$2de^2 I_{D6}\frac{W_1}{L} - K'e^4 V_{ref}^2 (\frac{W_1}{L})^2 = 2I_{D6}\frac{W_3}{L} - K'V_{ref}^2 (\frac{W_3}{L})^2 \tag{4.29}$$

From Eq(4.29) the threshold and transistor sizes of the comparators can be decided. The right-side of the Figure 4.27 is a SR-latch, which is used to stretch the output of the comparator to the full period because of only half-period lasting result in the output of the comparator. Figure 4.29 shows the simulation result of the output signal when applying the sine-wave input into the comparator.

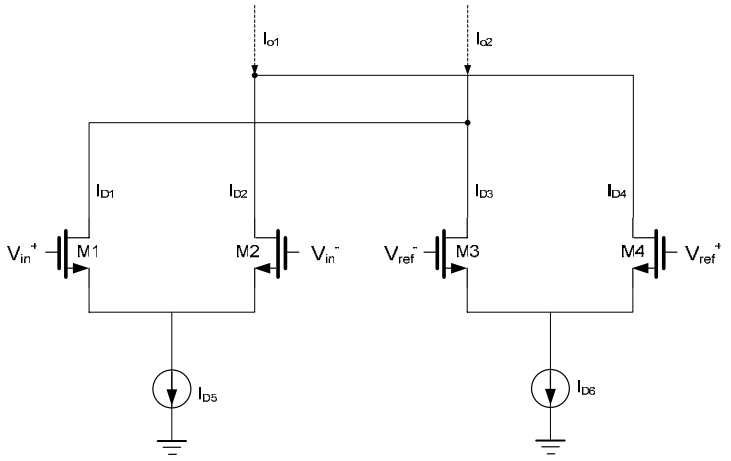
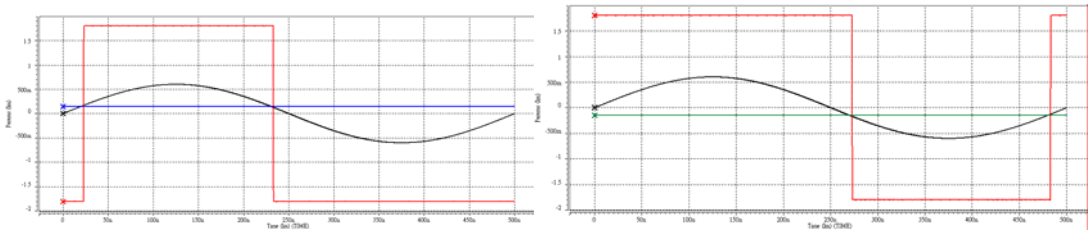


Figure 4.28 Simplified model of the differential pair comparator



(a) (b)

Figure 4.29 Simulated result of the comparator for a threshold of (a) Vref/4 (b) –Vref/4

4.4.4.2 1.5-Bit Sub-ADC (Flash Quantizer)

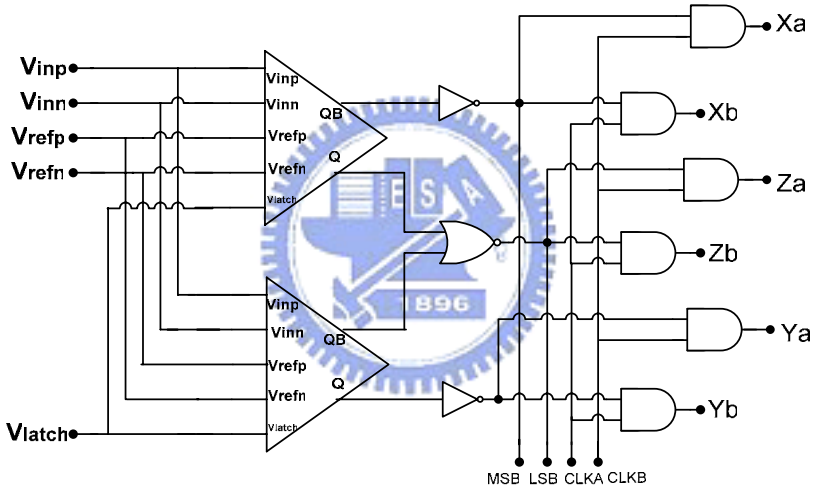


Figure 4.30 Schematic of the 1.5-bit Sub-ADC

The 1.5-bit Sub-ADC consists of two differential comparators and some simple logic as shown in Figure4.30. The threshold voltages of the comparator are in Vref/4 and –Vref/4. A comparator offset voltage up to ±Vref/4 can be tolerated through digital error correction technology. The sub-ADC compares the differential input signal with two decision levels and generates one of three different digital outputs 00,01 or 10. The MSB and LSB are the digital output codes of the 1.5-bit sub-ADC. Because the double sampling technique is applied in the pipelined ADC, not only

opamp is shared in two paths of each stage, but the sub-ADC is also shared. Therefore, the Xa, Ya, Za and Xb, Yb, Zb, corresponding to clka and clkb respectively, are the controlled signals which will be applied to the MDAC, which is also implemented with double-sampling technique.

Table 4.3 summaries the digital output codes of MSB and LSB and the controlled signals of X, Y, and Z for different values of the differential input voltage. Figure 4.31 shows the simulated result of the 1.5-bit sub-ADC, where the ±Vref are set equal to ±600mV.

Differential Input Voltage (V_{in})	Digital Output Codes (MSB, LSB)	Controlled Signals (X, Y, Z)
$-V_{ref} < V_{in} < \frac{-V_{ref}}{4}$	00	010
$\frac{-V_{ref}}{4} < V_{in} < \frac{+V_{ref}}{4}$	01	001
$\frac{+V_{ref}}{4} < V_{in} < +V_{ref}$	10	100

Table 4.3 Digital output codes and controlled signals of 1.5-bit sub-ADC

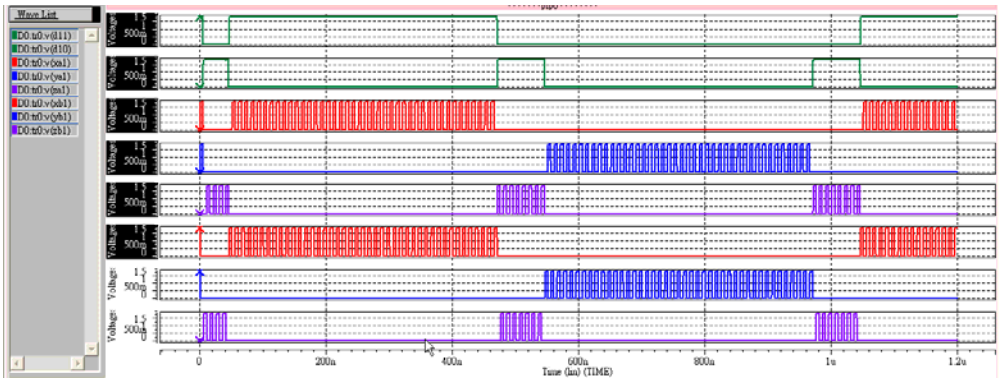


Figure 4.31 Simulated result of MSB, LSB, Xa, Ya, Za, Xb, Yb, Zb for an input signal of sine wave

4.4.5 1.5-Bit MDAC

The performance of pipelined ADC critically depends on the 1.5-bit multiplying-digital-to-analog converter (MDAC). Figure 4.32 shows the schematic of the double-sampling 1.5-bit MDAC configuration. As the configuration of the SHA, the MDAC is designed for two parallel sets of sampling capacitors and feedback capacitors to increase the throughput rate in each stage. The two parallel paths are controlled by opposite non-overlapping phase clocks $ø_a$ and $ø_a$. The phase $ø_{a\_d}$ and $ø_{b\_d}$ are delayed version of phase $ø_a$ and $ø_b$. [34] [35] [36]

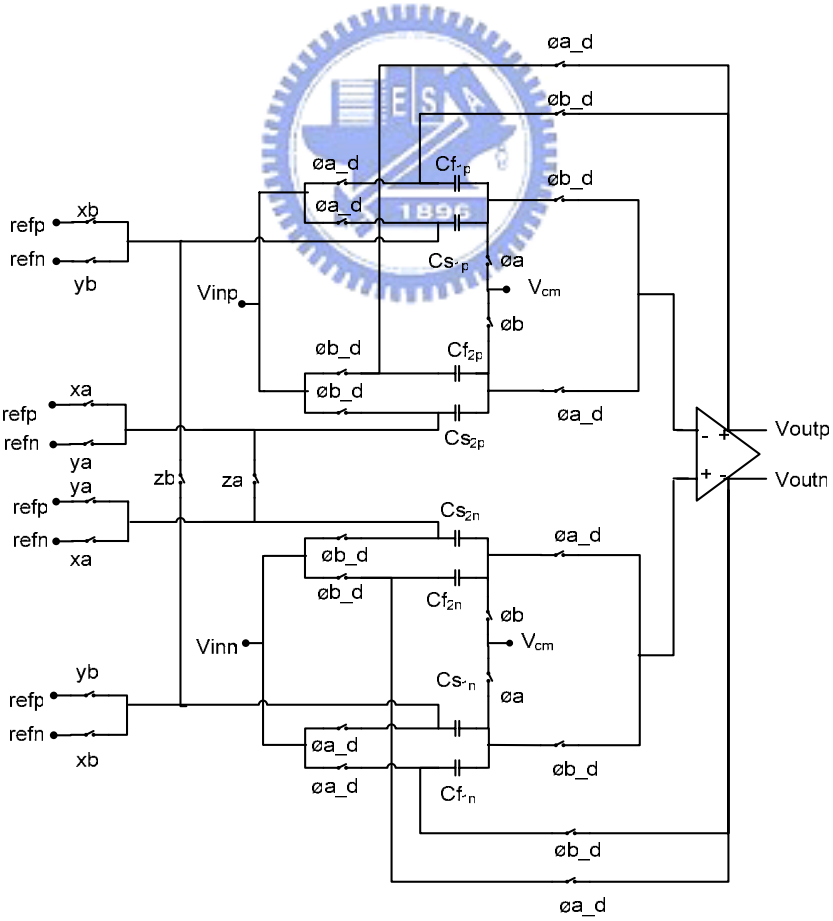


Figure 4.32 Schematic of the double-sampling 1.5-bit MDAC

During the first phase $ø_a$, one set of capacitors Cs_{1p}, Cf_{1p}, Cs_{1n} and Cf_{1n} sample the differential input voltage Vinp and Vinn .Concurrently the other set of capacitors Cf_{2p} and Cf_{2n} are connected in feedback, and capacitors Cs_{2p} and Cs_{2n} are connected to a proper reference voltage, Vrefp or Vrefn, which is controlled by the controlled signals Xa, Ya, and Za generated from the sub-ADC. The amplifier performs the analog reconstruction of the digital code resulting from the sub-ADC, subtracts it from the analog sampled voltage, Vin, and multiplies the resulting residue by 2.

During the second phase $ø_b$, the roles of the capacitors are exchanged. Capacitors Cs_{2p}, Cf_{2p}, Cs_{2n} and Cf_{2n} are employed as sampling capacitors. And capacitors Cf_{2p} and Cf_{2n} form the feedback loop of the opamp while the capacitors Cs_{2p} and Cs_{2n} are connected to the positive reference voltage (Vrefp), or to the negative reference voltage (Vrefn) depending on the state of controlled signals Xb, Yb, and Zb.

Assuming Cs=Cf=C and the a non-ideal op-amp with finite DC gain, the value of the amplified residue to be processed by the next stage of the pipeline is given approximately by

$$V_{out} = \begin{cases} \dfrac{2V_{in} + V_{ref}}{1+\dfrac{2}{A}}, if\ -V_{ref} < V_{in} < \dfrac{-V_{ref}}{4} \Leftrightarrow Y = 1 \\ \dfrac{2V_{in}}{1+\dfrac{2}{A}}, if\ \dfrac{-V_{ref}}{4} < V_{in} < \dfrac{+V_{ref}}{4} \Leftrightarrow Z = 1 \\ \dfrac{2V_{in} - V_{ref}}{1+\dfrac{2}{A}}, if\ \dfrac{+V_{ref}}{4} < V_{in} < +V_{ref} \Leftrightarrow X = 1 \end{cases} \quad (4.30)$$

yielding for very large A

$$V_{out} \cong 2 \cdot V_{in} - X \cdot V_{ref} + Y \cdot V_{ref} \quad (4.31)$$

where X, Y, and Z are the encoded digital outputs provided by the 1.5-bit sub-ADC. Figure 4.33 shows the simulation output waveform of the MDAC circuits in the first stage .

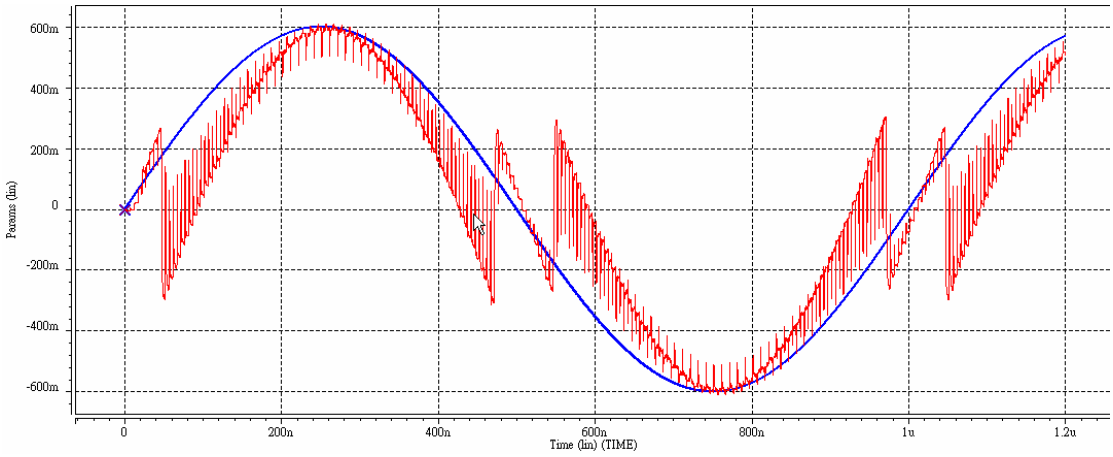


Figure 4.33 Simulated result of the 1.5-bit MDAC

4.4.6 The 2-Bit Flash ADC

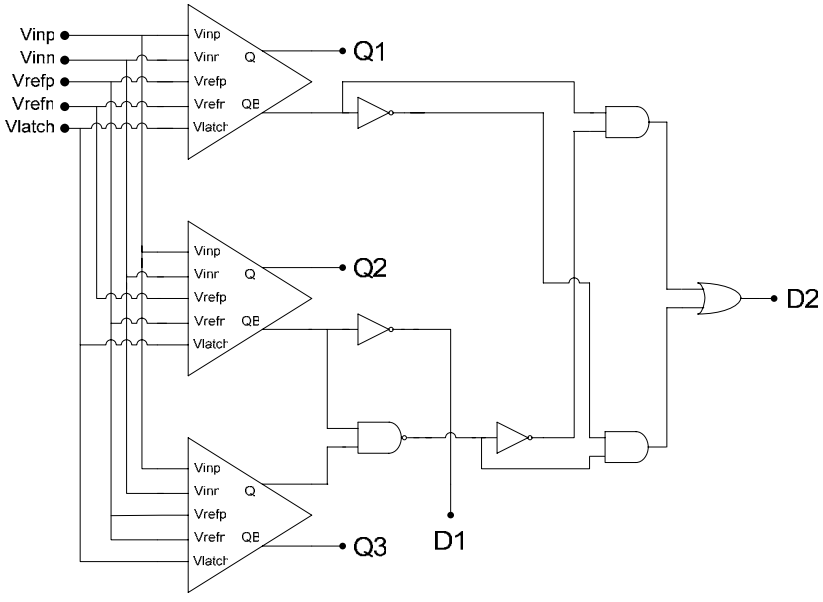


Figure 4.34 Schematic of the 2-bit Flash ADC

The final stage of 2-bit flash ADC is shown Figure 4.34. The simulated results are illustrated in Figure 4.35. The output digital codes are 00, 01, 10, 11 depending on the threshold voltages, Vrefp and Vrefn.

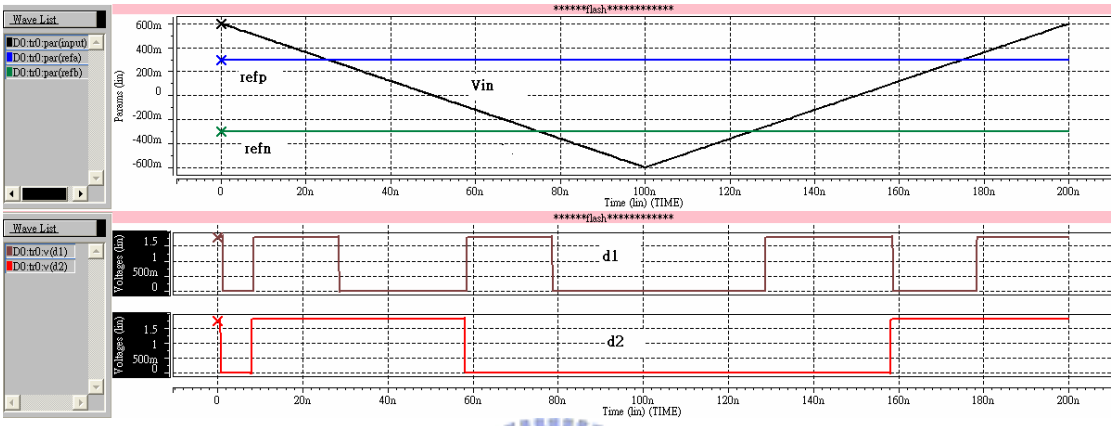


Figure 4.35 Simulated result of the 2-bit Flash ADC

4.4.7 Clock Generator

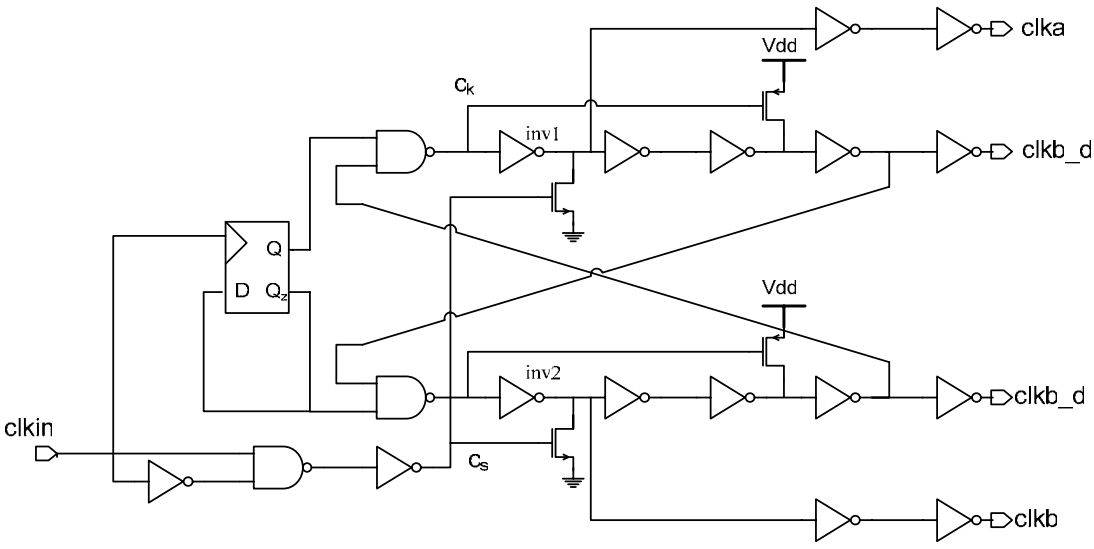


Figure 4.36 Two-phase clock generator for double-sampling pipelined ADC

The two-phase clock generator for the double-sampling pipelined ADC is

illustrated in Figure 4.36. The input clock ,clkin, is inserted off-chip in the frequency of 200MHz. Two non-overlapping phases, shown in Figure 4.37, are delivered for proper operation of switched capacitor circuits in the frequency of 100MHz respectively. The characteristic of this scheme is the adoption of the short pulse Cs of the width Δ and frequency 200MHz, which changes from 0 to 1 on the rising edge of clkin, illustrated in Figure 4.38. The short pulse Cs cause a high-to-low transition at the output of the inv1, which has its output at logic level one. Therefore, the falling edges of the clka and clkb can be controlled uniformly by the short pulse Cs. [37]

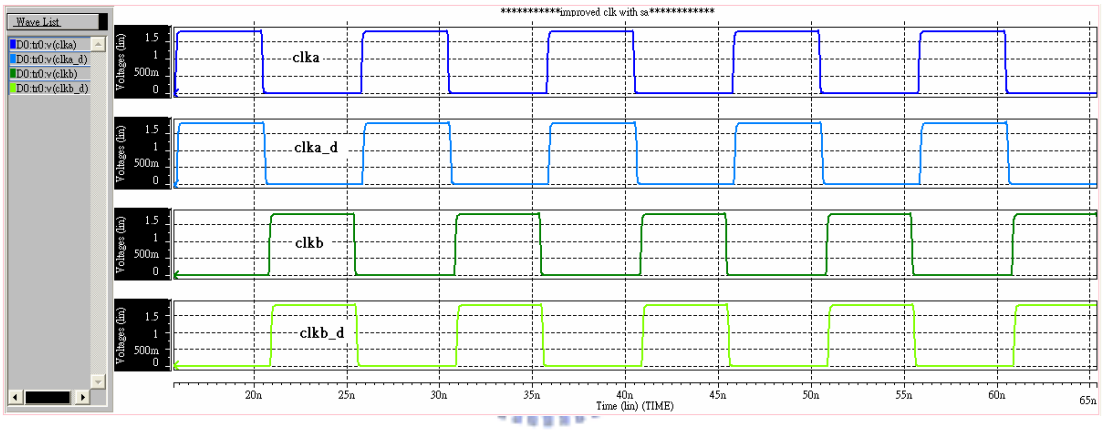


Figure 4.37 Simulated results of the non-overlapping clocks

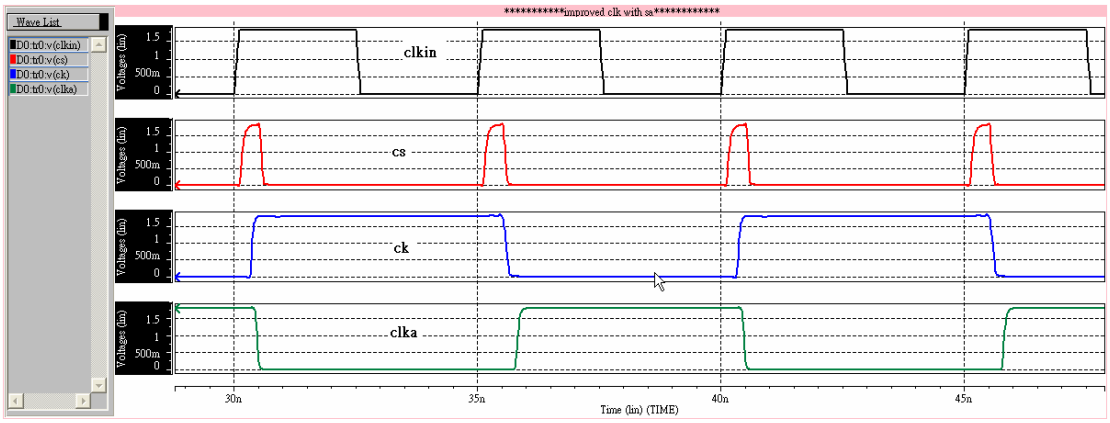


Figure 4.38 Timing diagram of the clock generator

As a result, uniform sampling clocks can be reached to minimize time-skew

problems in the double-sampling pipelined ADC. A possible disadvantage of this circuit will be that a short time makes the pmos of inv1 and M1, or, the pmos of inv2 and M2 simultaneously on. It will increase the power dissipation a little, but it can be negligible in the overall power consumption.

4.4.8 Registers and Digital Error Correction Logics

The registers are used to make the output codes from 9 stages synchronous and the final 10-bit codes are stored in registers after processing by digital error correction logics. Positive edge-triggered true single-phase clocked D-flips are adopted in the design of the registers, as shown in Figure 4.39. Only one clock phase is needed in the register and the complexity of the register arrays can be reduced.

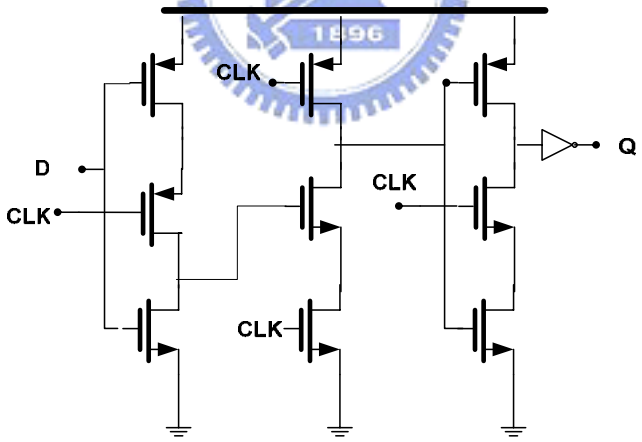


Figure 4.39 Positive edge-triggered true single-phase clocked D-flip

The digital output codes in each stage must be calibrated by the digital correction logics. It recombined the nine 1.5-bit codes by overlapping adding operation. Combining the register array and digital correction logics implement the backend design of the ADC shown in Figure 4.40.

Figure 4.40 Shift register arrays and digital error correction logics

4.4.9 Simulated Results of Pipelined ADC

The 10-bit, 200MS/s double-sampling pipelined A/D converter with the 1.8V supply voltage is implemented. With the ideal DAC, the 10-bit output digital codes are converter to analog signal. Figure 4.41 shows the simulated result of the pipelined ADC when applying the 1 MHz sine-wave to the inputs. The spectrum of the reconstructed 0.98 MHz sine wave is shown in Figure 4.42 and the SNDR is about 56.14 dB.

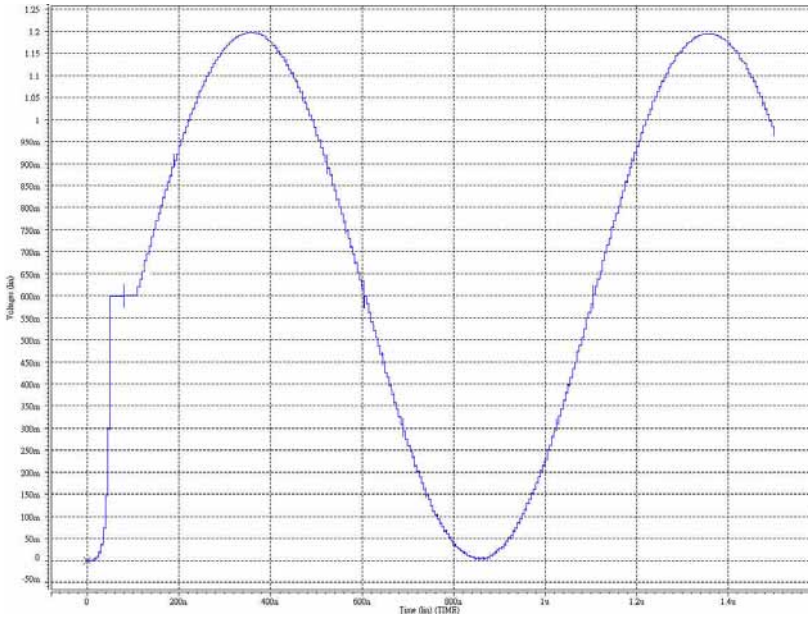


Figure 4.41 Simulated result of the pipelined ADC with the sine-wave input signal

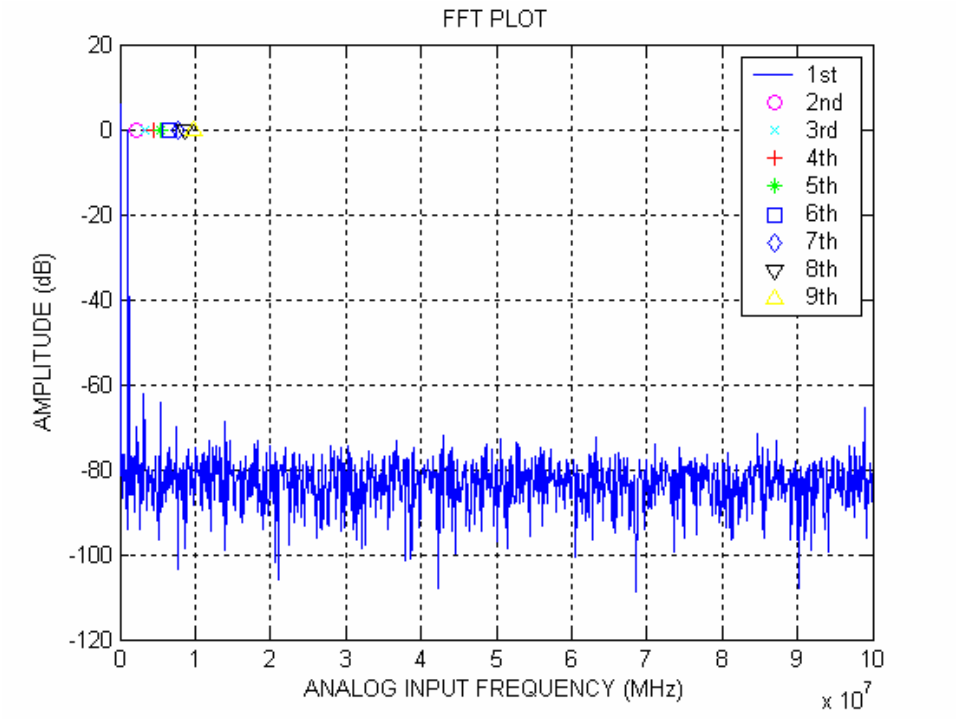


Figure 4.42 The spectrum of the 0.98 MHz sine wave

Figure 4.43 shows the simulated results through the ideal DAC when applying the ramp signal to input.

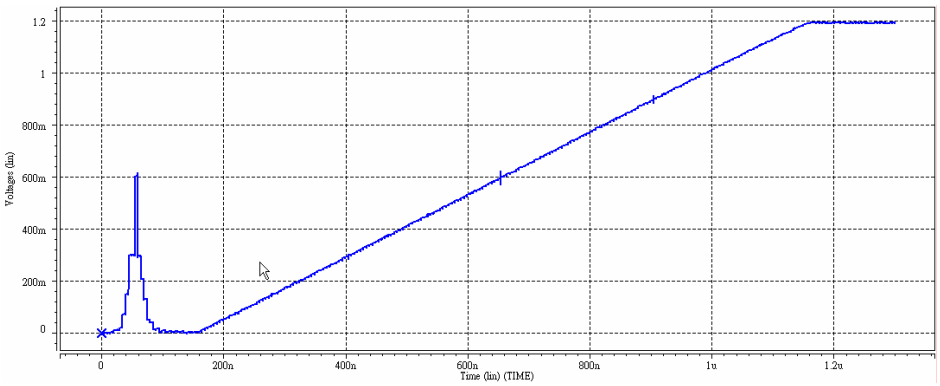


Figure 4.43 Simulated result of the pipelined ADC with the ramp input signal

Then the results are analyzed for characterizing the linearity of the ADC. However, the linearity of the ADC could be realized by analyzing the parameters of the DNL and INL. The simulated results of the DNL and INL of the pipelined ADC are shown in Figure 4.44. The maximum DNL and INL are ±0.75 LSB and ±0.95 LSB.

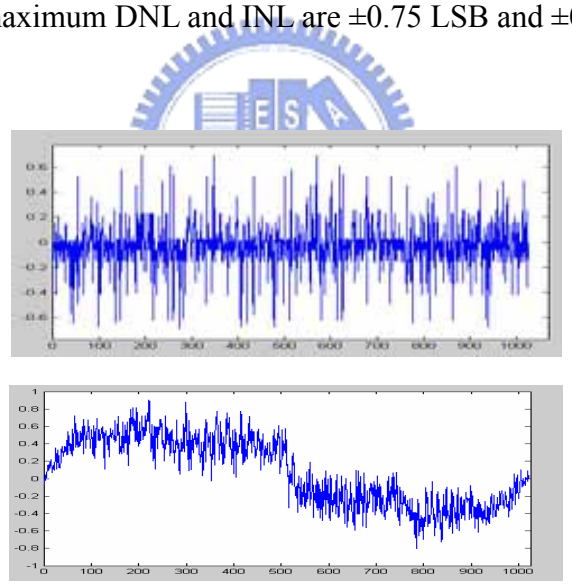


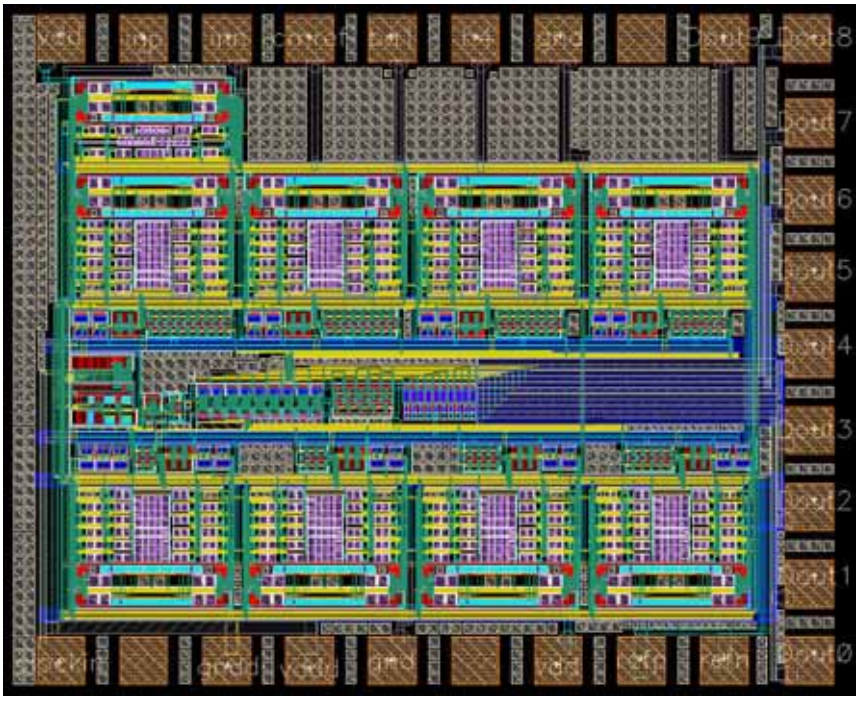
Figure 4.44 Simulated results of DNL and INL

Table 4.4 summaries the simulated results of the pipelined ADC. Layout and floor plan of the experimental prototype chip are shown in Figure 4.45. This pipelined ADC was laid out on a 1.380×1.134 mm^2 die that including digital circuits and the pad frame. In the layout, we use the mirror symmetry to enhance the rejection of common mode noises in the fully differential circuits. In this research, the analog circuit is

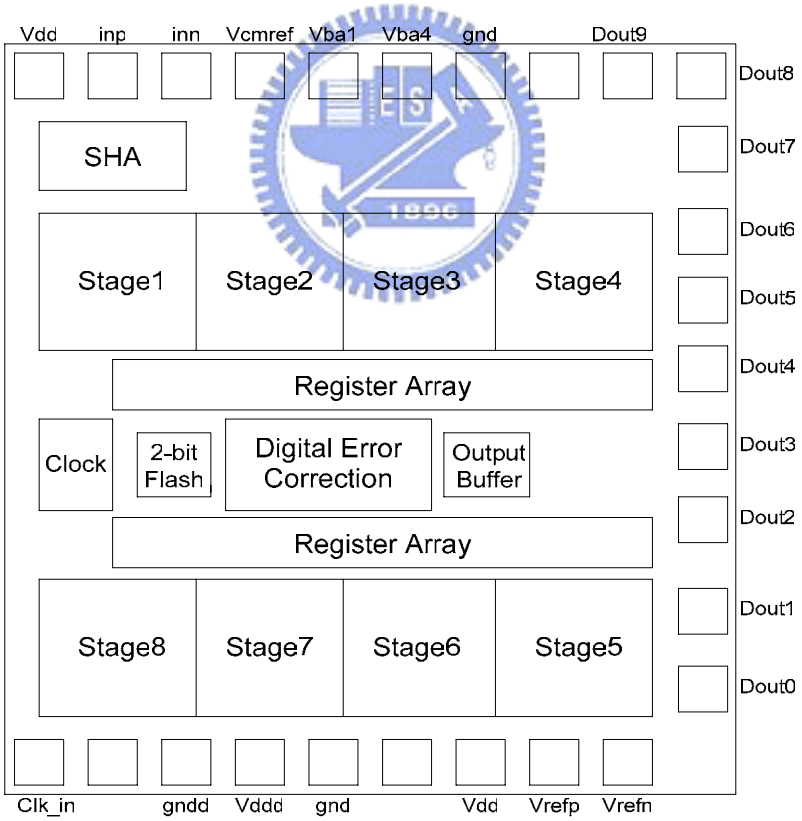
separated from the digital circuit and is powered from a separated power supply.

Parameters	Simulated Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.8 V
Input Range	±0.6V Fully differential
Resolution	10 bits
Operation Frequency	200 MHz
INL/DNL	±0.95 LSB /±0.75 LSB
ENOB(Fin=0.98MHz)	9.03 bits
SNDR (Fin=0.98MHz)	56.14 dB
Power Dissipation	103.28 mW
Chip Size	1.380mm×1.134mm

Table 4.4 Summary of simulated results of the double-sampling pipelined ADC



(a) Layout



(b) Floor plan

Figure 4.45 (a) Layout and (b) floor plan of the pipelined ADC

Chapter 5

Test Setup and Experimental Results

5.1 Introduction

The double-sampling pipelined ADC has been implemented by TSMC 0.18um 1P6M CMOS Mixed-Signal process. In this chapter, the testing environment, the printed circuit board (PCB) circuits and required instrument for testing are introduction. Finally, the experimental results are summarized.

5.2 Test Setup

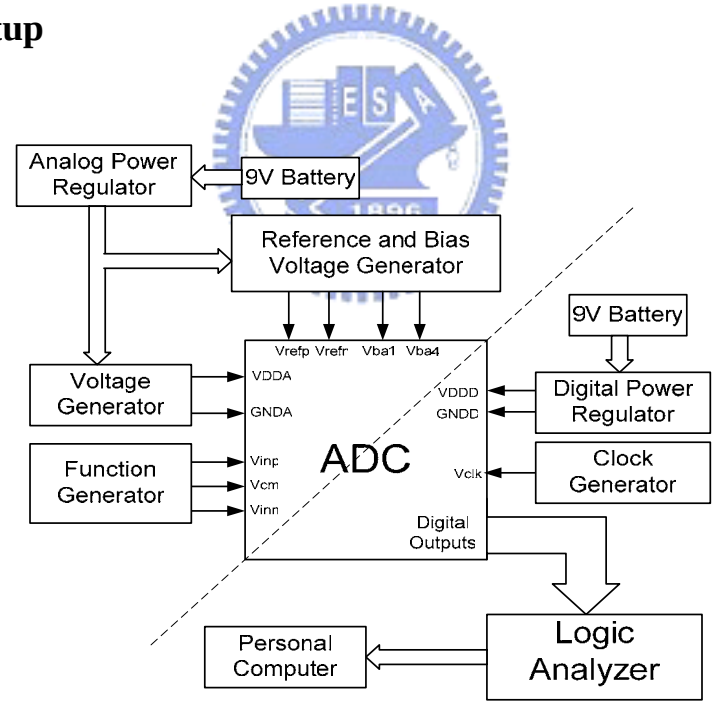


Figure 5.1 Testing setup

A schematic of the measurement setup used to evaluate the double-sampling pipelined ADC performance is presented in Figure 5.1. Figure 5.2 shows a photograph of the PC board used in the experimental evaluations. In Figure 5.1 it consists of the

analog power regulator, the digital power regulator, the function generator, the clock generator, the reference and bias voltage generator, and the logic analyzer.

Figure 5.2 The photograph of the experimental pipelined ADC DUT board

5.2.1 Power Supply Regulators

The power supply is divided into two main parts to support the analog voltage VDDA and digital VDDD to avoid noise coupling between analog and digital circuit. Therefore, these two powers have their own regulator and the output voltage, and the analog ground and digital ground are isolated to each other.

The analog and digital power supplies are generated by the application of the LM317 adjustable regulators shown in Figure 5.3. The input voltage of the regulator circuit is connected to a 9V battery, and the output voltage is specified in 1.8V. The regulator circuit requires two resistors to define the output voltage. [38] The output

voltage of the Figure 5.3can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) \cdot I_{ADJ} \cdot R2\,, \tag{5.1}$$

where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator.

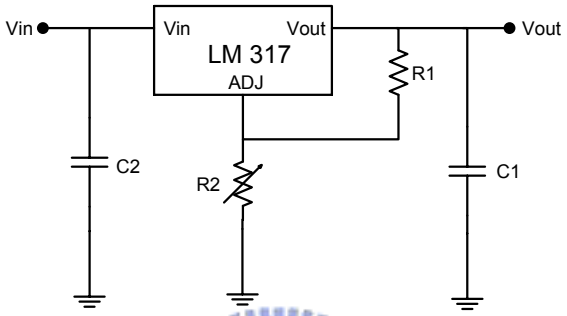


Figure 5.3 Power supply regulator

The outputs of the regulators are bypassed on the PCB with the filter tank. The bypassed filter network is combined by 10uF, 1uF, 0.1uF, and 0.01uF capacitors as shown in Figure 5.4. The capacitor arrangement in Figure 5.4 provides decoupling of both low frequency noise with large amplitude and high frequency noise with small amplitude.

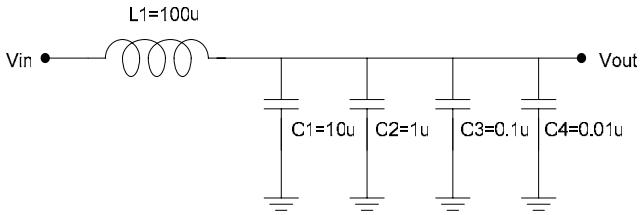


Figure 5.4 Bypass filter at the output of the regulator

5.2.2 Input Termination Circuit

The applied input signal to the DUT is buffered and converted to balanced differential forms by the circuit shown in Figure 5.5. By using the configuration of an inverting opamp and a non-inverting opamp, the differential signals are generated and delivered to the AC coupled circuit. [22] [39] [40] [41]

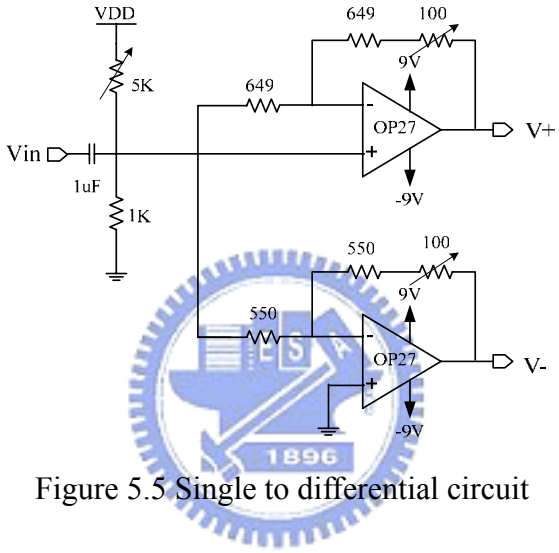


Figure 5.5 Single to differential circuit

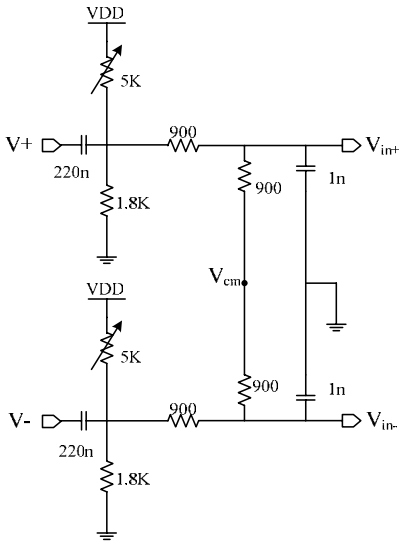


Figure 5.6 AC coupled circuit

The AC couple circuit is illustrated in Figure 5.6. The outputs of the AC coupled circuits are terminated on the DUT with one pole low pass filters as shown in Figure 5.6. With the AC coupled circuit, we can prevent the aliasing of high frequency noise components into the baseband and attenuate charge kickback from the sampling switches in the DUT into the input source.

5.2.3 Measured Instruments

The input signal to the DUT is provided by the signal generator, Agilent E4438C, shown in Figure 5.7. The clock signal is generated by a pulse/pattern generator Agilient 81130A, shown in Figure 5.8. The output bit streams of the DUT are fed to the logic analyzer, HP 16702B, shown in Figure 5.9. The 10-bit output data was primarily captured and stored in the logic analyzer. By transferring the digital data from the logic analyzer, the converter outputs were processed and analyzed using MATLAB in the personal computer.

Figure 5.7 Signal Generator Agilent E4438C

Figure 5.8 Pulse/pattern generator Agilient 81130A

Figure 5.9 Logic analyzer HP 16702B

5.3 The Package and Pin Configuration

Figure 5.10 shows the die photomicrograph of the experimental double-sampling pipelined ADC. Figure 5.11 presents the pin configuration and lists the pin assignments of the experimental pipelined ADC.

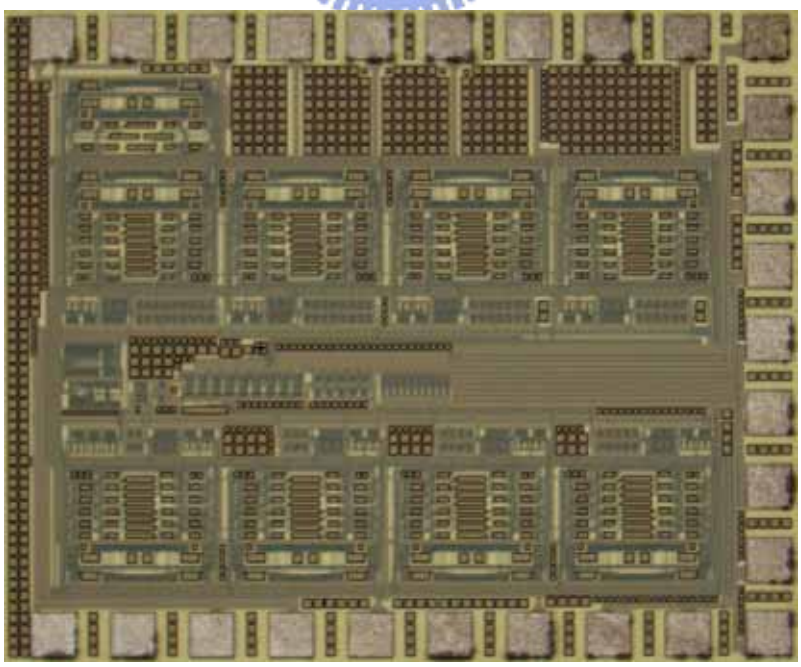
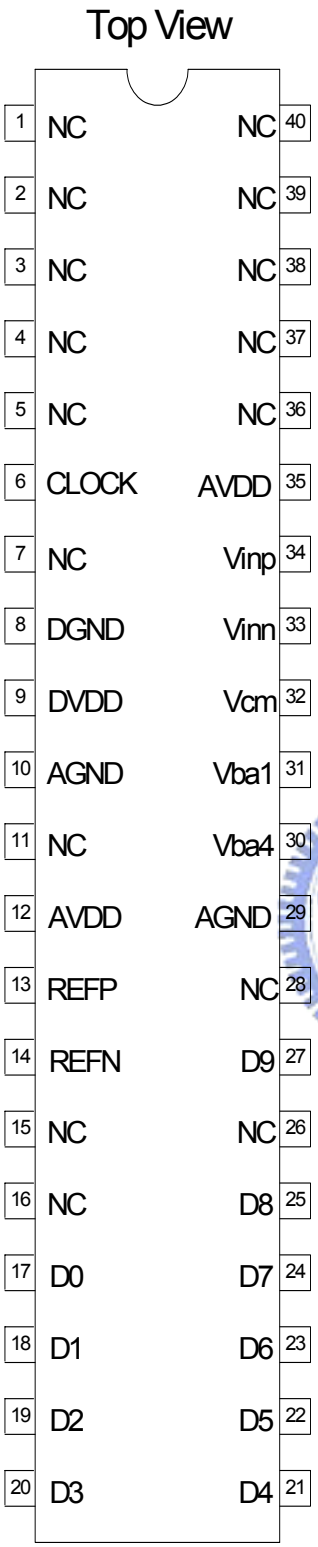


Figure 5.10 Die photomicrograph of the pipelined ADC

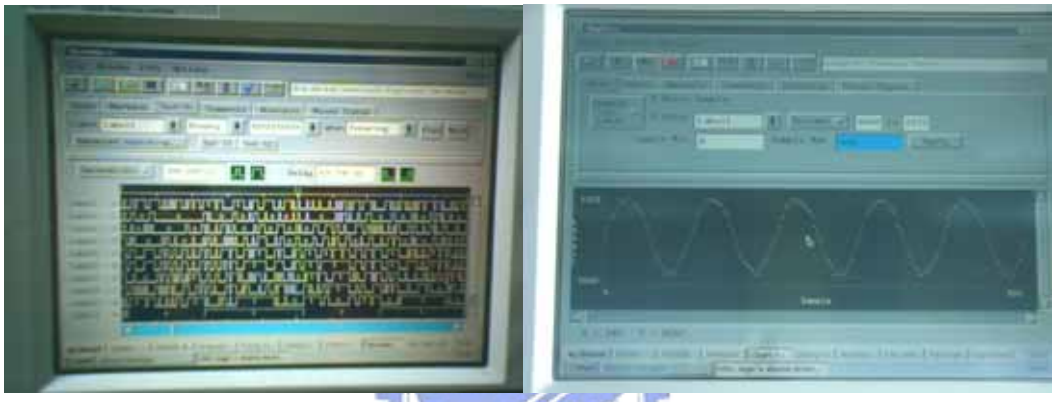


Pin	Name	I/O	Describe
1	NC	-	No connection
2	NC	-	No connection
3	NC	-	No connection
4	NC	-	No connection
5	NC	-	No connection
6	CLOCK	In	System clock input
7	NC	-	No connection
8	DGND	In	Digital ground
9	DVDD	In	Digital power supply
10	AGND	In	Analog ground
11	NC	-	No connection
12	AVDD	In	Analog power supply
13	REFP	In	Reference voltage＞Vcm
14	REFN	In	Reference voltage＜Vcm
15	NC	-	No connection
16	NC	-	No connection
17	D0	Out	Digital data output
18	D1	Out	Digital data output
19	D2	Out	Digital data output
20	D3	Out	Digital data output
21	D4	Out	Digital data output
22	D5	Out	Digital data output
23	D6	Out	Digital data output
24	D7	Out	Digital data output
25	D8	Out	Digital data output
26	NC	-	No connection
27	D9	Out	Digital data output
28	NC	-	No connection
29	AGND	In	Analog ground
30	Vba4	In	Bias voltage
31	Vba1	In	Bias voltage
32	Vcm	In	Common mode voltage
33	Vinn	In	Input signal (180°)
34	Vinp	In	Input signal (0°)
35	AVDD	In	Analog power supply
36	NC	-	No connection
37	NC	-	No connection
38	NC	-	No connection
39	NC	-	No connection
40	NC	-	No connection

Figure 5.11 (a) Pin configuration diagram and (b) Pin assignment

5.4 Experiment Results of Pipelined ADC

The pipelined ADC has fabricated in 0.18μm CMOS process. The chip was powered by the 1.8 V analog and digital circuits supply. A 1 MHz sine wave is applied to the ADC and operates at the 100 Msample/s and 150 Msample/s conversion rate, respectively. The output 10-bit streams of the DUT collected by the logic analyzer and the plot chart are shown in Figure 5.12 and 5.13.

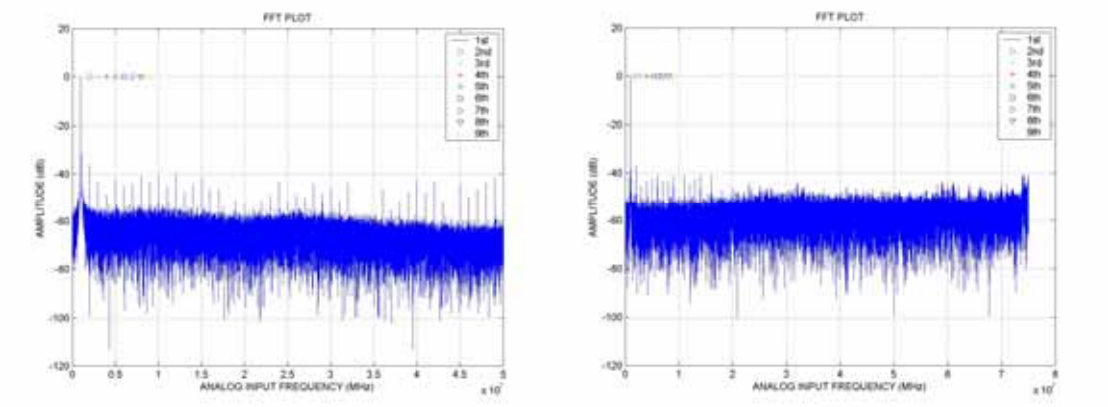


(a) (b)

Figure 5.12 Measured results for 100 Msample/s conversion rate (a)Output bit streams (b) Plot chart

Figure 5.13 Measured results for 150 Msample/s conversion rate (a)Output bit streams (b) Plot chart

From the measured results shown in Figure 5.12 and 5.13, the signal to noise ratio is calculated by collecting 65536 samples of the input signal and performing a 65536 point fast Fourier transform shown in Figure 5.14. This result shows that SNDR are about 32.14 dB and 30.78 dB for 100 and 150 Msample/s conversion rate respectively.



(a) (b)

Figure 5.14 65536 points FFT at 1MHz input frequency for (a) 100 MHz sampling frequency (b) 150 MHz

These harmonic distortions are caused by the nonlinear of the op-amp and mismatch of the two sampling paths. The worst reason is that the DC gain of the op-amp at the highest output swing is no longer large enough to meet the required specification. Furthermore, the charge injection and common mode drift issues both are the possible reasons. In addition, when the sampling rate is large than 150 Msample/s, the plot chart of the ADC doesn't show the similar sine-wave. Probably the input signal and the sampling rate are coupled each other, thus the input signal is influenced and clipped. Figure 5.15 shows the SNDR for different sampling rate. Table 5.1 summaries the measured results of the pipelined ADC.

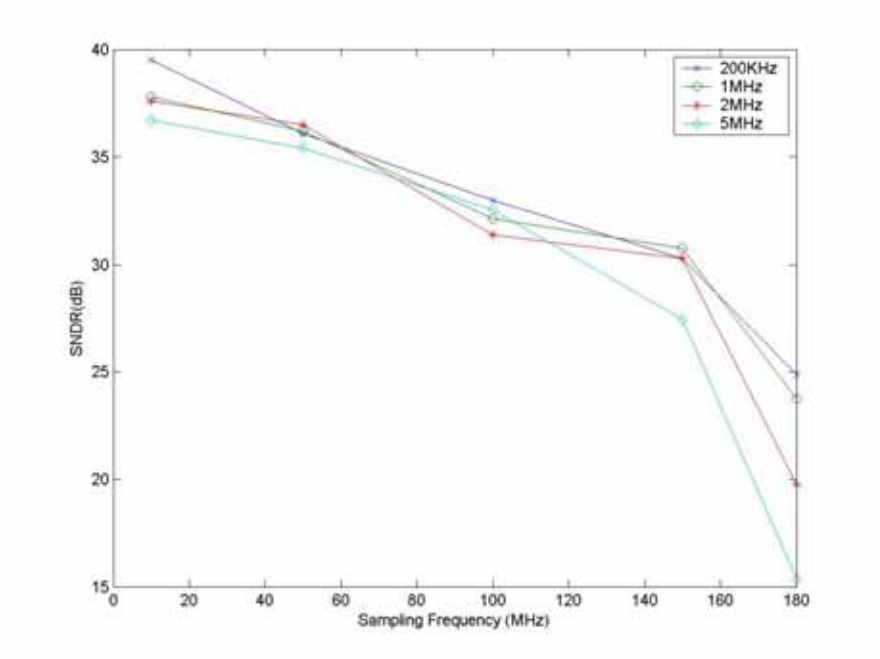


Figure 5.15 The SNDR against the sampling rate

Parameters	Measured Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.8 V
Input Range	±0.6V Fully differential
Operation Frequency	150 MHz
SNDR for a 1 MHz input	30.78 dB
ENOB	4.82bits
DNL/INL	5.43/18.62 LSB
Power Dissipation	103 mW
Chip Size	1.380mm×1.134mm

Table 5.1 Summary of measured results of the pipelined ADC

Chapter 6

Conclusions

6.1 Conclusion

In thesis, a double-sampling pipelined ADC has been designed, laid-out, fabricated, and tested. With the technique of double-sampling, the specifications of the operational amplifier can be relaxed and the conversion rate of the pipelined ADC is duplicated compared with the single-sampling ADC.

Although the technique of double-sampling can increase the conversion rate, some non-idealities also comes along in the double-sampling pipelined ADC. Besides the non-idealities in the single-sampling pipelined ADC, such as the charge injection error, offset error, and gain error, the mismatches between the two paths have to be considered. We have discussed these problems in chapter 3.

The chip was fabricated by TSMC 0.18um 1P6M CMOS process. The measured results are 32.14dB in the 100MHz conversion rate. The maximum conversion rate in the measurement is worse than the simulation, because the design of the opamp is not good enough and settling error increases. Therefore, the output residue of each stage can not be settled properly when increasing the sampling frequency. On the other hand, there are many extra parasitic capacitors that the post-layout extraction didn't extract out, and the measuring skills are not good enough, and any other reasons like the instrument issue and the high frequency effects that need to discover and study.

6.2 Future Work

As the mismatches between the paths result in severe distortions in the spectrum, the performance of the measurement is not satisfied. Therefore, it is an important issue to reduce the gain mismatch, offset mismatch, and timming mismatch. If we continue to research on the same topic, we will try to add some calibration methods to correct the nonidealities in the double-sampling pipelined ADC. As time goes by, a wide variety of calibration techniques has been proposed. Digital or analog calibration methods may be applied to the design for the double-sampling pipelined ADC. Based on the architecture of double-sampling pipelined ADC, the time-interleaved ADC can be established by combining more channels of double-sampling pipelined ADC. As a result, the sampling rate can be increased much greatly.

On the other hand, low voltage low-power design is the other topic to study for the future work. With the reduced supply voltage, we have to do efforts to improve the performance of the opamp to reach the accuracy of the ADC. And in order to reduce the power consumption, scaling down the sampling capacitors stage by stage will be necessary.

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