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單晶片溫度感測器的高線性度參考電壓之設計與製作

The Design and Implementation of High Linear Voltage References for System-on-Chip Temperature Sensors

研究生：蔡佐昇

指導教授：闕河鳴　博士

西元二００六年七月

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研 究 生：蔡佐昇　　Student：Joseph Tzuo-sheng Tsai

指導教授：闕河鳴　博士　　Advisor：Dr. Herming Chiueh

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摘要

高線性度電壓參考電路以 TSMC 0.13μm 及 TSMC 0.18μm 複合式金氧矽製程來設計及實現。先前研究已經提出在傳統上正比絕對溫度的電路裡，金氧矽電晶體操作在弱反轉區可以用來取代雙極性裝置。然而這樣的方法，在現今深次微米及奈米複合式金氧矽技術下，常因元件的漏電流效應，使得在高溫時會有線性度之問題。本論文所提出的電路，利用溫度補償技術用在正比絕對溫度及與絕對無度無關這兩個參考電壓下，來加強線性度並產生一個較為穩定的無關溫度之參考電壓。模擬結果中，在 55°C 到 170°C 的溫度範圍下，R-quares 都可達到 0.999 以上。此論文設計了一個溫度範圍廣的溫度感測器，並且能夠容易整合於現今的系統晶片設計之中。

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National Chiao Tung University

Hsinchu, Taiwan 30050

Abstract

High linear voltage references circuitry is designed and implemented in TSMC 0.13μm and 0.18μm CMOS technology. Previous research has proposed the use of MOS transistors operating in the weak inversion region to replace the bipolar devices in conventional PTAT(proportional to absolute temperature) circuits. However such solutions often have linearity problem in high temperature region due to the current leaking devices in modern deep sub micron and nano-scale CMOS technology. The proposed circuit utilized temperature complementation technique on two voltage references, PTAT and IOAT (independent of absolute temperature) references, to enhance the linearity and produce a more stable IOAT voltage reference. Base on the simulation results, the R-squares of both circuitries are better than 0.999 in a considerable wider temperature range from -55°C to 170°C. Thus, a fully integrated temperature sensor with wider temperature range is designed and easily to integrate to modern system-on-chip designs with minimal efforts.

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CHAPTER 1

Introduction

1.1 Motivation

Increases in circuit density and clock speed in modern VLSI systems have brought thermal issues into the spotlight of high-speed VLSI design. Large gate-count and high operating frequency in modern system-on-chip integration escalate the problem. Previous research has indicated that the thermal problem can cause significant performance decay [1] as well as reducing of circuitry reliability [2]-[5]. In order to avoid thermal damages, early detection of overheating and properly handling such event are necessary. For these reasons, temperature sensors are widely used in modern VLSI systems.

Recent research has indicated that the best candidate for a fully-integrated temperature sensor is the proportional-to-absolute temperature (PTAT) circuit [6] and independent-of-absolute-temperature (IOAT) circuit with the sigma-delta modulator and digital filter. Figure 1.1 shows the block diagram of this on-chip thermal aware system. In such design, the PTAT sources are usually implemented using parasitic vertical BJTs in any standard CMOS technology [7], [8]. These circuits require resistors which may vary from different technology. Also, the power consumption of the BJT based references is relatively high for low power applications. However, in deep sub micron CMOS technology, the characteristic of vertical BJT is getting worse. So, the design of temperature sensor has become a major challenge in deep sub micron technology.

The PTAT generator of Vittoz and Fellrath [9] takes advantage of MOS transistors operating in the weak inversion region; the power consumption is minimal due to the

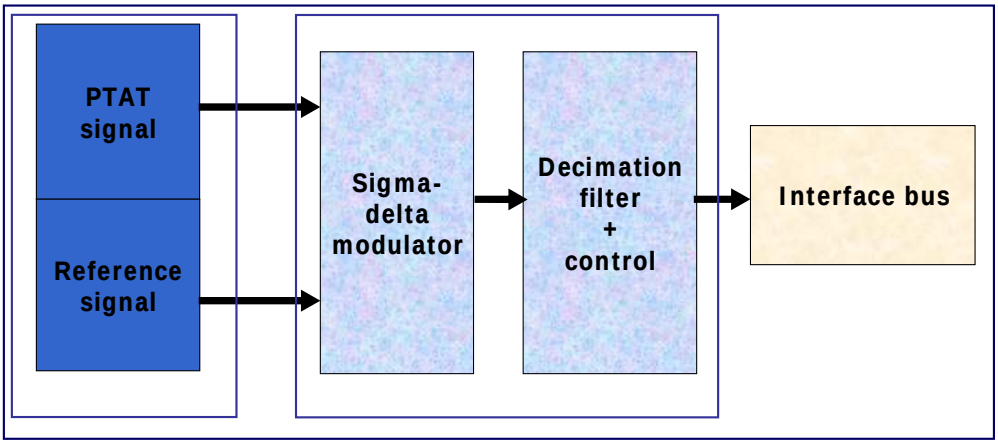


Figure 1.1 Block diagram of a thermal aware system.

inherently low currents in that region. However, this circuit does not allow strong supply voltage scaling.

Serra-Graells and Huertas [10] introduce an all-MOS implementation exhibiting enough low-voltage capabilities by the use of MOS sub-threshold techniques. However, in this circuit, the current leaking device in modern deep sub-micron CMOS technology has cause the linearity problem of the PTAT and IOAT signals in high temperature range.

These nonlinearity behaviors are crucial effect to implement a complete thermal management system within a digital circuit since such circuitries require more efforts and costs for after process calibration. Thus, linearity and power issues are the key factors for design a fully integrated temperature sensor in the deep sub micron CMOS technology.

In this thesis, both PTAT and IOAT voltage references are redesigned by utilizing sub-threshold MOSFETs and temperature complementation technique to enhance the linearity and produce a more stable output. The propose design has extend the linear temperature rage of on-chip temperature sensor to -55°C to 170°C which provides a practical solution for modern system-on-chip's thermal management systems.

1.2 Organization

Chapter 2 begins with the review of the temperature sensing, from mercury-in-glass thermometers to very low power and low cost smart temperature sensors. Then the temperature sensing methods both with bipolar transistors and subthreshold MOSFETs are described. For the low-power consideration, subthreshold MOSFETs

are more suitable than bipolar transistors. We also demonstrated the nMOS is better than pMOS for the design.

Chapter 3, first, introduces the MOS PTAT reference circuitry architecture which has been proposed in [11]. Then the new PTAT and IOAT reference circuitry architectures have been proposed. The first version is resistor-based reference circuitry architecture. For the area consideration, the second version, all-MOS reference circuitry architecture, has been proposed. The all-MOS reference circuitry architecture also enhances the compensative mechanism. All the detail design concepts will be described in this Chapter.

In Chapter 4, the simulation and experiment results are introduced. First, the resistor-based reference circuitry architecture has been simulated in TSMC 0.18μm 1P6M CMOS technology. Then, the simulation results of all-MOS version which are simulated with both TSMC 0.18μm and 0.13μm CMOS technology have been shown. All-MOS version's layout consideration is also described. Finally, the experiment results and discussion are discussed.

The conclusions and future works of this thesis are given in Chapter 5.

CHAPTER 2

Temperature Sensing

This Chapter begins with the introduce of smart temperature sensors. Following the brief introduce, the methods of temperature sensing both with bipolar transistors and subthreshold MOSFETs are described. For the low power applications, the n-type subthreshold MOSFETs are more suitable than p-type, this result is demonstrated on a deep-submicron technology. A brief conclusion is made in the end of the Chapter.

2.1 CMOS Smart Temperature Sensors

As time goes by, due to the remarkable market growth portable systems nowadays, the demand for very low power and low cost but high performance temperature sensors is becoming much stronger than ever. To reduce the cost of a system that consists of both a temperature sensor and a computer interface, integration of the temperature sensor and the analog-to-digital converter was attempted. This new system family was called integrated smart temperature sensors. Figure 2.1 shows this system.

The important nowadays applications of smart temperature sensors include: 1) the power consumption control in VLSI chips; 2) the thermal compensation in single-chip systems and micro systems with built-in sensors; 3) the environment temperature monitor in automatic fabrication factories; and 4) the temperature control of consumer electronics. However, temperature sensing with bipolar transistor do not exhibit enough low-power capabilities [12]-[14]. This disadvantage is a very fatal reason for the low power portable applications. Nowadays researches have some solutions for this problem, such as temperature sensing with subthreshold MOSFETs and time-to-digital-converter-based CMOS smart temperature sensors [15].

Smart temperature sensors are needed because the systems in which they are being

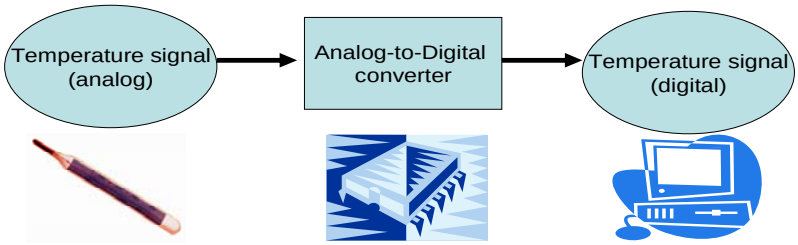


Figure 2.1 Communication between a temperature sensor and a computer.

applied are getting more and more complex. The future trend for smart temperature sensors will be low power and low cost. Cheaper temperature sensors will also increase the number of applications.

Figure 2.2 shows the block diagram of conventional smart temperature sensor. In the figure, we know the temperature is sensed by two voltage references, PTAT and reference signal (such as bandgap reference or independent-of-absolute-temperature reference). So to improve the linearity of PTAT or to reduce the variance of bandgap reference (or independent-of-absolute-temperature reference) will make the sensor produce a more accurate temperature output. This thesis will force on the topic of how to improve these reference signals.

In order to attain our goal, knowing the principle of PTAT and bandgap reference will be necessary. In the next session, we will introduce how to produce both positive and negative temperature coefficients with bipolar transistors and MOSFETs. Then to combine pTC and nTC, we will get independent-of-absolute-temperature reference. some improvements will be presented in the following chapters.

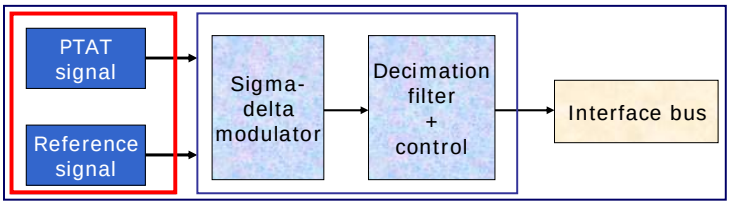


Figure 2.2 The block diagram of conventional smart temperature sensor.

2.2 Temperature sensing

In this section, the temperature sensing method with both bipolar transistor and subthreshold MOSFETs will be described. In order to convert temperature to a digital value, both a well-defined temperature dependent signal and a temperature independent reference signal are required. There are two voltage that we interesting, one requires a positive temperature coefficient (pTC), and another requires a negative

temperature coefficient (nTC). A quantity which requires a positive temperature coefficient is used to measure the temperature. If two quantities having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a temperature-independent quantity which requires a zero TC. As follow, the two interesting quantities, one requires a negative temperature coefficient and another requires a positive one, are discussed.

(A) Bipolar transistor

(i) Negative temperature coefficient (nTC)

The base-emitter voltage of bipolar transistors exhibits a negative TC. For a bipolar device,

$$I_C = I_S \cdot EXP(\frac{V_{BE}}{V_T}) \tag{2.1}$$

Where U_T = k T /q and I_S is the saturation current of the transistor which is temperature dependent. Rewrite Equation (2.1), we can get:

$$V_{BE}(I_C) = \frac{kT}{q} \cdot \ln(\frac{I_C}{I_S}) \tag{2.2}$$

Where k is Boltzmann's constant ($1.3807 \cdot 10^{-23}$ J/K), T the absolute temperature (in Kelvin), and q the electron charge ($1.6022 \cdot 10^{-19}$ C). Because we want to know the TC of the base-emitter voltage, we take the derivative of V_{BE} with respect to T. We can get:

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \cdot \ln(\frac{I_C}{I_S}) - \frac{kT}{q}\frac{1}{I_S}\frac{\partial I_S}{\partial T} \tag{2.3}$$

The saturation current is I_S is proportional to $(u \cdot k \cdot T \cdot n_i^2)$, where u is the mobility of minority carries and n_i is the intrinsic minority carries concentration of silicon. The temperature dependence of these quantities is represented as $u \propto u_0 \cdot T^m$, where m is a constant about -3/2, and $n_i^2 \propto T^3 \cdot \exp[-V_g / kT]$, where V_g is the bandgap energy of silicon. Thus we

can write I_S as follows:

$$I_S = \beta \cdot T^{4+m} \cdot \exp\frac{-V_g}{kT} \tag{2.4}$$

β is a proportionality factor. We take the derivative of I_S with respect to T to know its temperature characteristic. We can get:

$$\frac{\partial I_S}{\partial T} = \beta \cdot (4+m) \cdot T^{3+m} \cdot \exp\frac{-V_g}{kT} + \beta \cdot T^{2+m} \cdot \frac{V_g}{k} \cdot \exp\frac{-V_g}{kT} \tag{2.5}$$

With the aid of (2.3) and (2.4), we can write

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \cdot \ln(\frac{I_C}{I_S}) - \frac{k}{q} \cdot (4+m) - \frac{V_g}{qT} \tag{2.6}$$

$$= \frac{V_{BE} - (4+m)U_T - V_g/q}{T} \tag{2.7}$$

From Equation (2.7), the temperature coefficient of the base-emitter voltage at a given temperature T is gotten and it is clear negative. For example, with $V_{BE} \approx 750mV$ and $T = 300^o K$, $\partial V_{BE} / \partial T \approx -1.5mV/^o K$.

(ii) Positive temperature coefficient (pTC)

When two bipolar transistors operate at two different collector currents I_1 and I_2, the difference between their base-emitter voltage will be a proportional to absolute temperature quantity. Figure 2.2 is illustrates this idea. As follows, we describe in detail.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{2.8}$$

$$= U_T \ln\frac{I_1}{I_S} - U_T \ln\frac{I_2}{I_S} \tag{2.9}$$

$$= U_T \ln\frac{I_1}{I_2} \tag{2.10}$$

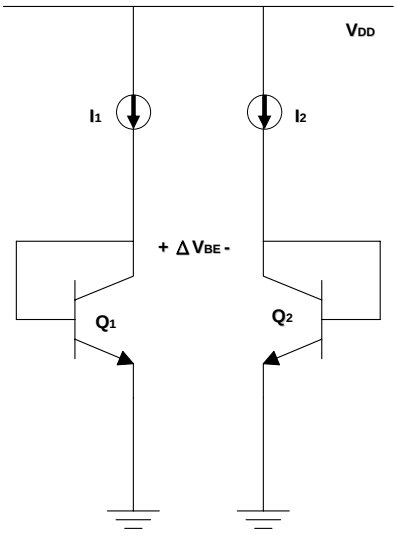


Figure 2.3 Generation of PTAT voltage with bipolar transistors.

If the two collector currents have this relation, $I_1 = pI_2$, where p is a constant. From Equation (2.10), we get:

$$\Delta V_{BE} = \frac{kT}{q} \cdot \ln(p) \tag{2.11}$$

Taking the derivative of Equation (2.11) with respect to T, we get:

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \cdot \ln(p) \tag{2.12}$$

According to Equation (2.12), we know clear the difference of the base-emitter voltage operated in different collector currents is a PTAT quantity.

(B) Subthreshold MOSFETs

(i) Negative temperature coefficient (nTC)

Previous research [16] has shown the gate-source voltage of an nMOS which operated in weak inversion has a negative temperature coefficient (nTC) and can be modeled as:

$$V_{GSn}(T) \approx V_{GSn}(T_0) + K_{Gn} \cdot (T/T_0 - 1) \tag{2.13}$$

Where

$$K_{Gn} \cong K_{Tn} + V_{GSn}(T_0) - V_{THn}(T_0) - V_{OFFn} \tag{2.14}$$

Where K_{Tn} is the temperature coefficient for nMOS threshold voltage and T_0 is room temperature (=300 K). The gate-source voltage of a pMOS transistor can also been modeled as:

$$\left|V_{GSp}(T)\right| \approx \left|V_{GSp}(T_0)\right| + K_{Gp} \cdot (T/T_0 - 1) \tag{2.15}$$

Where

$$K_{Gp} \cong K_{Tp} + \left|V_{GSp}(T_0)\right| - \left|V_{THp}(T_0)\right| - V_{OFFp} \tag{2.16}$$

In order to verify the linearity of V_{GS} operated in deep sub micron simulations based on both TSMC 0.13μm and 0.18μm technology are conduced, the gate-source voltage of an nMOS diode-connected transistor biased with a 100-nA current and the diode aspect ratio was set to 50/2 are simulated. The same simulations are also done with a pMOS diode-connected transistor. Figure 2.3 shows the simulation prototypes. The results are shown in Figure 2.4 and Figure 2.5. Basing on the results shown in Figure 2.4 and Figure 2.5, we can know that the linearity of nMOS gate-source voltage is better than pMOS source-gate voltage in both TSMC 0.18μm and 0.13μm CMOS technology. Table 2.1 shows the summary. So, if we want to get much better linearity in wider range, for the case, [-55, +170] ^0C, the gate-source voltage of an nMOS transistor is the best choice.

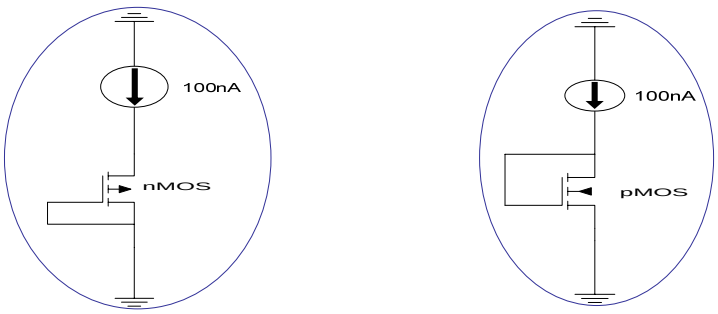


Figure 2.4 The simulation prototypes.

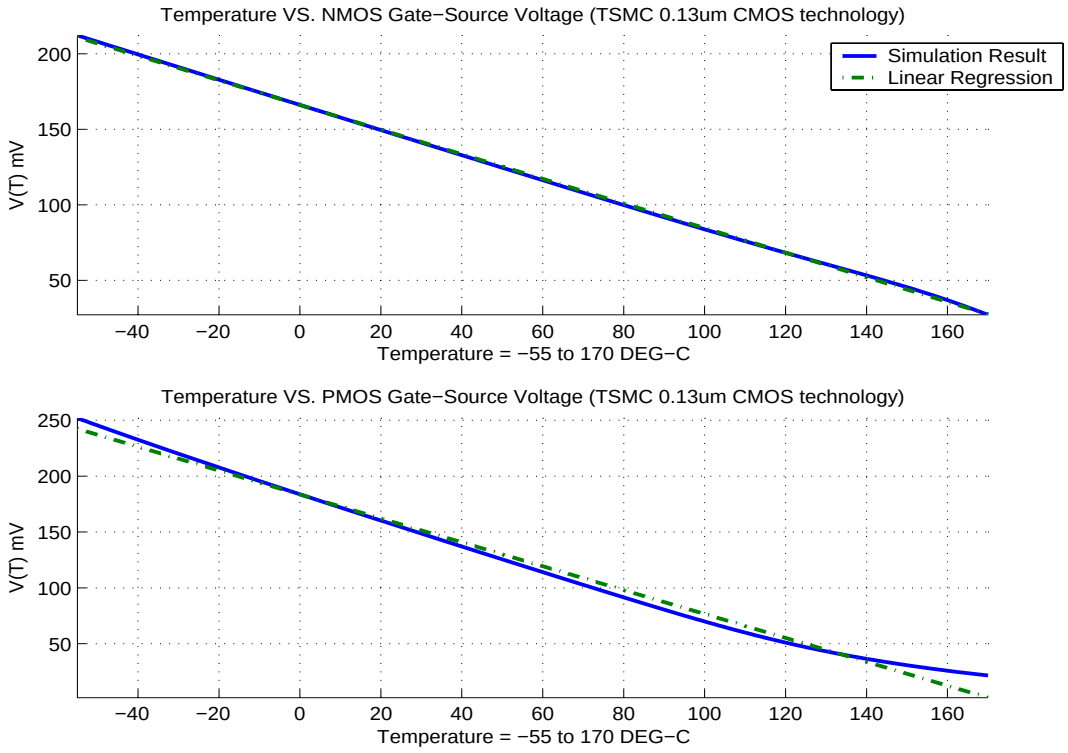


Figure 2.5 The simulation results done in TSMC 0.13μm CMOS technology.

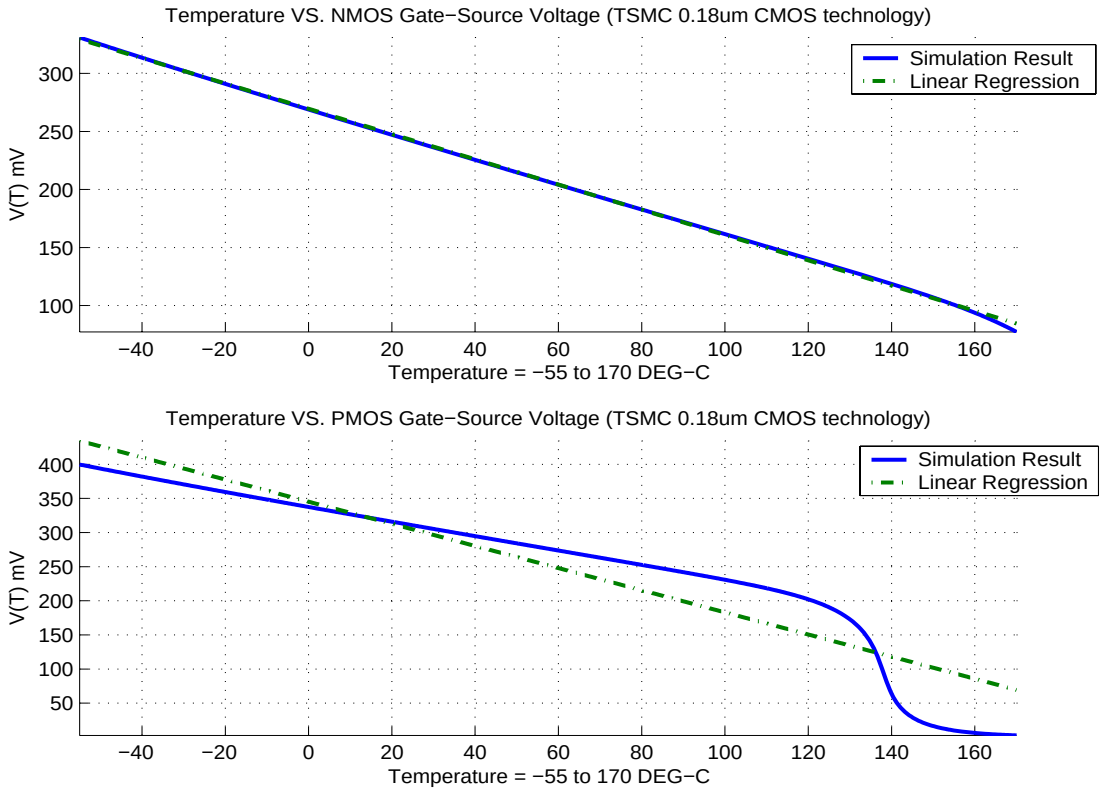


Figure 2.6 The simulation results done in TSMC 0.18μm CMOS technology.

Table 2.1 The linearity summary of V_{GS}.

R-square	NMOS	PMOS
TSMC 0.13μm CMOS technology	0.99976	0.99214
TSMC 0.18μm CMOS technology	0.99971	0.87315

Above all, a linear negative temperature coefficient voltage based on subthreshold MOSFETs has been presented.

(ii) Positive temperature coefficient (pTC)

The positive temperature coefficient quantity can be gotten in several kinds of MOS PTAT generators. The idea of MOS PTAT generators is like the bipolar transistor PTAT generators. When two MOSFETs operate at two different collector currents I_1 and I_2, the difference between their gate-source voltage will be a proportional to absolute temperature quantity. Figure 2.5 is illustrates this idea. As follows, we describe in detail.

According to the references [11] and [17], the drain currents of M1 and M2 are given by

$$I_{D1} = K_{w1} \cdot \beta_1 \cdot U_T^2 \cdot e^{\frac{V_{G1} - V_{t0,1} - (n_1 - 1) \cdot V_S}{n_1 \cdot U_T}} \tag{2.17}$$

$$I_{D2} = K_{w2} \cdot \beta_2 \cdot U_T^2 \cdot e^{\frac{V_{G2} - V_{t0,2} - (n_2 - 1) \cdot V_S}{n_2 \cdot U_T}} \tag{2.18}$$

Where n is the slope factor, ϕ_f is the substrate Fermi potent, and

$$\phi_0 = 2\phi_f + several \cdot U_T \tag{2.19}$$

$$K_w = (n-1) \cdot e^{\frac{\phi_0 - 2\phi_f}{U_T}} \tag{2.20}$$

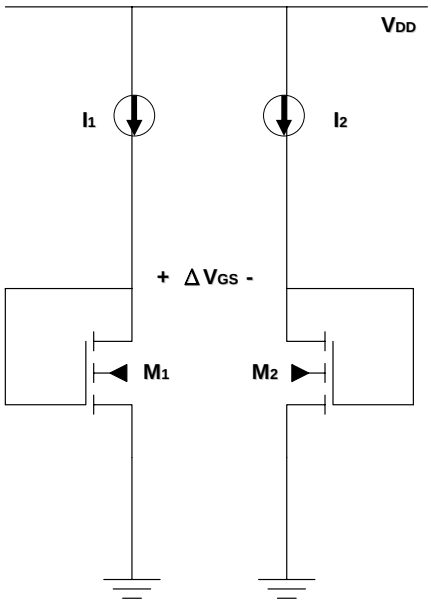


Figure 2.7 Generation of PTAT voltage with subthreshold MOSFETs.

$$\beta_{1,2} = u_{n,1,2} \cdot C'_{ox,1,2} \cdot \frac{W_{1,2}}{L_{1,2}} \tag{2.21}$$

$$V_{t0,1,2} = V_{FB} + \phi_0 + \gamma \cdot \sqrt{\phi_0} \tag{2.22}$$

Where V_{FB} is the flat-band voltage.

Because the source is connected to ground, Equations (2.17) and (2.18) can be derived to

$$V_{G1} = V_{t0,1} + n_1 \cdot U_T \cdot \ln(\frac{I_{D1}}{C_1}) \tag{2.23}$$

$$V_{G2} = V_{t0,2} + n_2 \cdot U_T \cdot \ln(\frac{I_{D2}}{C_2}) \tag{2.24}$$

Where

$$C_{1,2} = K_{w1,2} \cdot \beta_{1,2} \cdot U_T^2 \tag{2.25}$$

If M1 and M2 are matched, the PTAT voltage can be obtained from the difference in V_{G1} and V_{G2}:

$$\Delta V_{GS} = V_{G1} - V_{G2} = n \cdot U_T \cdot \ln(\frac{I_{D1}}{I_{D2}} \cdot \frac{S_2}{S_1}) \tag{2.26}$$

Where S_1 and S_2 are the W/L ratios of M1 and M2 respectively. Taking the derivative of Equation (2.26) with respect to T, we get:

$$\frac{\partial \Delta V_{GS}}{\partial T} = n \cdot \frac{k}{q} \cdot \ln(\frac{I_{D1}}{I_{D2}} \cdot \frac{S_2}{S_1}) \tag{2.27}$$

If the drain currents have the relation, $I_{D1} = p \cdot I_{D2}$, and $S_2 = r \cdot S_1$, where p and q are constants, we get:

$$\frac{\partial \Delta V_{GS}}{\partial T} = n \cdot \frac{k}{q} \cdot \ln(p \cdot r) \tag{2.28}$$

According to Equation (2.28), we know clear the difference of the gate-source voltage operated in different drain currents is a PTAT quantity.

2.3 Summary

In this Chapter, the history of the temperature sensing is introduced. And we also describe the smart temperature sensor. As time goes by, much cheaper, low power, and high performance temperature sensors will be demanded for many applications. In the section 2.3, we describe how to generate two voltage references which one has a negative temperature coefficient and another is a proportional-to-absolute-temperature with both bipolar transistors and subthreshold MOSFETs. However, for the low power consideration, the bipolar transistor is more difficult to implement. Because the MOSFETs operated in the weak inversion region will have minimal power consumption, subthreshold MOSFETs are more suitable for the low power design. But when we use subthreshold MOSFETs, we still have many challenges, such as [7]:

- The behaviors are more complicated for designers.
- Linearity is worse as process scaling down, particularly in high temperature.

- The performance is significantly affected by the variations of manufacture process.

These problems affect the performance significantly. Leakage current has become a serious problem in modern VLSI. It also affects the linearity of PTAT. As to smart temperature sensors, many dynamic offset-cancellation techniques can be used to enhance the performance, such as autozero techniques, chopper techniques, and nested chopper technique. However, for the linearity of PTAT or the variation of the independent-to-absolute-temperature (IOAT), we still can do more efforts to improve their performance.

In next Chapter, PTAT and IOAT of our design will be proposed. Some compensation methods to improve the linearity of PTAT and the variation of IOAT are presented. All the details will be described later. Based in this Chapter's backgrounds, it is useful for us to get guidelines in our proposed design.

CHAPTER 3

CMOS Voltage References

In this Chapter, both proportional-to-absolute-temperature (PTAT) and independent-of-absolute-temperature (IOAT) voltage references are redesigned by utilizing sub-threshold MOSFETs and temperature complementation technique to enhance the linearity and produce a more stable output. The propose design has extend the linear temperature rage of on-chip temperature sensor to -55°C to 170°C which provides a practical solution for modern system-on-chip's thermal management systems. The design concept of proposed circuit will be described in this Chapter, and the experimental results are presented in Chapter 4.

3.1 Introduction

Various on-chip PTAT and IOAT references have been extensively implemented using parasite BJTs because of the ease of design. In some CMOS process, however, obtaining reliable BJTs is very costly and desirable performance from these parasitic devices is hard to expect. Also, the power consumption of the BJT based references is relatively high and an alternative approach is preferred, especially in low power applications.

Several PTAT and IOAT references based on the subthreshold MOSFETs have been studied and applied in low power low voltage design. As we mention in the Chapter 2, these circuits take the advantages of the MOS transistors operated in weak inversion region in the respects: the power consumption is made minimum due to the inherent low currents in this region. The power issues are overcome by taking the advantage of the MOS transistors operated in weak inversion region. Another issue is the accuracy. For the PTAT references, linearity is the most important performance index we concern about. For the IOAT references, various must be as low as possible. Some temperature compensation techniques are applied to enhance the circuit performance.

Our design concepts are described in detail as follow. And some design issues are also described in following sections.

3.2 CMOS Voltage References

In the Chapter 2, we know the gate-source voltage of an nMOS transistor operated in the weak inversion region has a linear negative temperature coefficient (nTC) and is suit for the design. So if we put PTAT core and the gate-source voltage which operated in weak inversion region (V_{GS}) together, the IOAT voltage reference will be achieved by sum up both out. According to previous researches [8], a PTAT voltage reference circuit based on subthreshold MOSFETs has been developed. Figure 3.1 and figure 3.2 illustrate the condensed scheme of two low-voltage CMOS PTAT references [11]. In these circuits, M1 and M2 operate in weak inversion region, while transistors M3-M8 ensure the current ratio of M1-M2 pair. The transistor Mc which operated in weak inversion region compensates the leakage current to enhance the linearity of PTAT reference. Above all, the PTAT references will be written as:

$$V_{PTAT} = U_T \ln P \tag{3.1}$$

Where U_T = k T /q and P is the aspect ratio of M6 to M3.

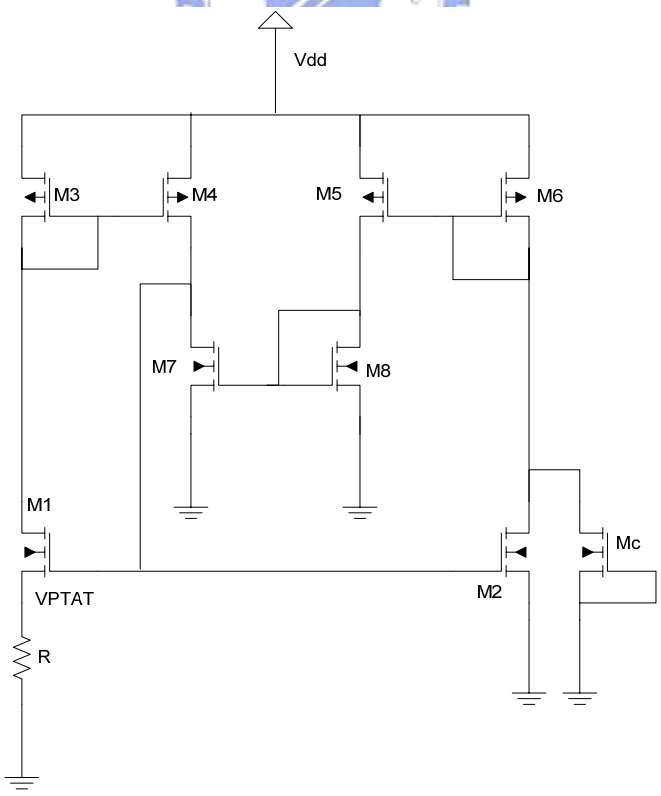


Figure 3.1 Low-voltage CMOS PTAT references (resistor-based).

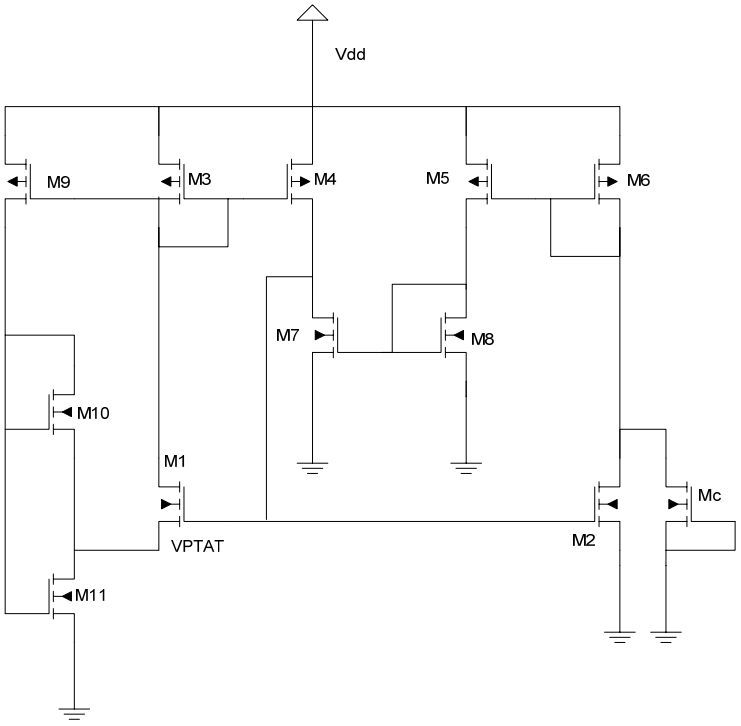


Figure 3.2 Low-voltage CMOS PTAT references (all-MOS-based).

The proposed circuitry architectures are shown in Fig. 3.3. The design concept is that using current mirror combines positive and negative temperature coefficients.

The first part circuit, M1-M8, Mc, and R1, will produce a PTAT voltage reference. The slope of PTAT reference is determined by the aspect ratio of M6 and M3. And function of Mc is to compensate the leakage current. The quantity of the PTAT reference is as the same as equation (3.1). The second part of this circuit is made up of M9, R2, and a diode-connected transistor, Mn. A negative temperature coefficient will be produced in the gate-source voltage of Mn. The target of our design is to make two different temperature coefficient sum up, so we use a current mirror to make them sun up in current type. In this architecture, the IOAT voltage can be expressed as:

$$V_{IOAT} = V_{PTAT} \cdot \frac{R_2}{R_1} \cdot \frac{S_9}{S_3} + V_{GSn} \tag{3.2}$$

Where S_3 and S_9 are the aspect ratios of M3 to M9.

In order to get a zero temperature coefficient, we take the derivative of equation (3.2) with respect to temperature (T).

$$\frac{\partial V_{PTAT}}{\partial T} \cdot \frac{R_2}{R_1} \cdot \frac{S_9}{S_3} + \frac{\partial V_{GSn}}{\partial T} = 0 \tag{3.3}$$

According to equations (3.1), (2.13), and (2.14), we can get:

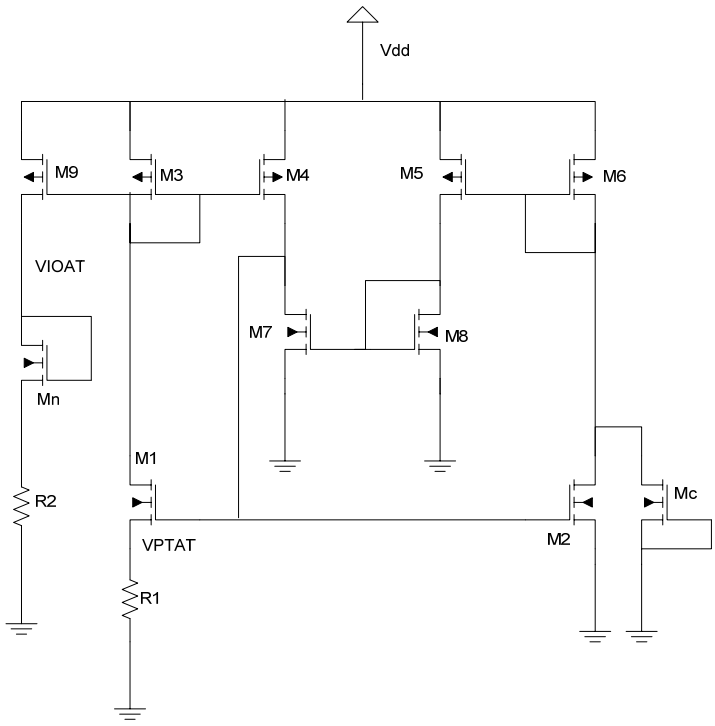


Figure 3.3 Resistor-based CMOS PTAT and IOAT references.

$$\frac{R_2}{R_1}\cdot\frac{S_9}{S_3}\cdot\frac{k}{q}\cdot\ln p+\frac{1}{T_0}[K_{Tn}+V_{GS}(T_0)-V_{THn}(T_0)-V_{OFFn}]=0 \qquad (3.4)$$

Where K_{Tn} is the temperature coefficient for nMOS threshold voltage and T_0 is room temperature (=300 K). We rewrite equation as:

$$\frac{R_2}{R_1}\cdot\frac{S_9}{S_3}=\frac{q}{k\cdot T_0\cdot\ln p}[V_{THn}(T_0)+V_{OFFn}-K_{Tn}-V_{GSn}(T_0)] \qquad (3.5)$$

Because the right side of equation (3.5) is constant, the ration $\frac{R_2}{R_1}\cdot\frac{S_9}{S_3}$ is determined.

For the area consideration, we also develop all-MOS PTAT and IOAT voltage reference. Figure 3.4 shows the all-MOS architecture. R1 exchanges with M9, M10, and M11. R2 is exchanges with M14, M15, and M16. Both M11 and M12 are operated in strong inversion conduction region. In order to ensure each current ratio, we add another feedback path M17, M18, M19, and M20. Following equations (3.6), (3.7), (3.8), and (3.9), the details are described:

$$I_D=\beta\cdot[V_{GB}-V_{TO}-\frac{n}{2}(V_{DB}+V_{SB})]\cdot(V_{DB}-V_{SB}) \qquad \text{s.i.cond. (3.6)}$$

$$I_D=\frac{\beta}{2n}\cdot(V_{GB}-V_{TO}-nV_{SB})^2 \qquad \text{s.i.sat. (3.7)}$$

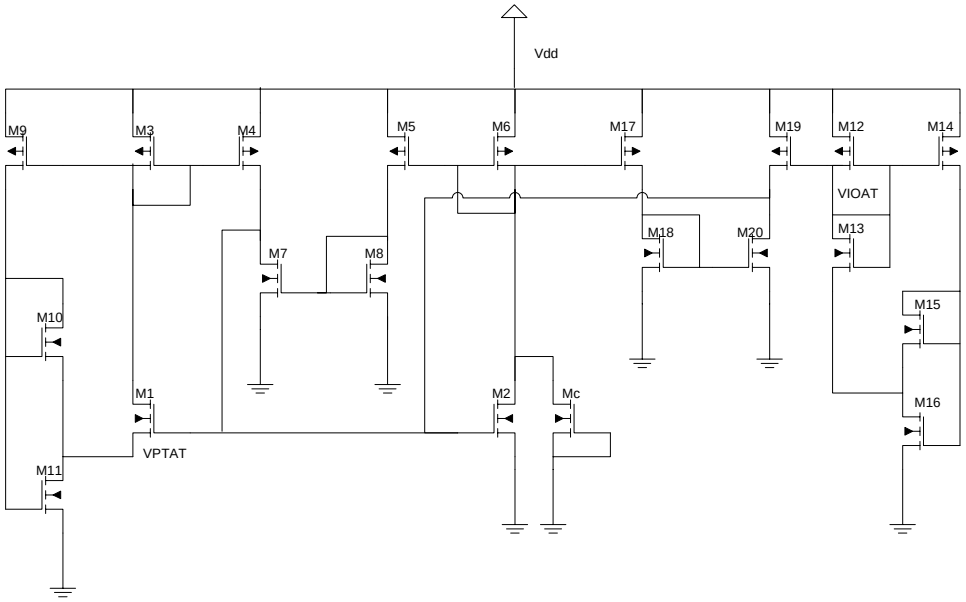


Figure 3.4 All-MOS CMOS PTAT and IOAT references.

$$I_D = I_S \cdot e^{(V_{GB}-V_{TO})/nU_T} \cdot e^{-V_{SB}/U_T} \quad \text{w.i.sat.} \tag{3.8}$$

$$I_S = 2 \cdot n \cdot \beta \cdot U_T{}^2 \tag{3.9}$$

Where V_{TO}, β, n, and I_S stand for the threshold voltage, current factor, subthreshold slope, and specific current, respectively, as defined in the EKV model [17]. We assume that there is no current the path 1 as shown as follow:

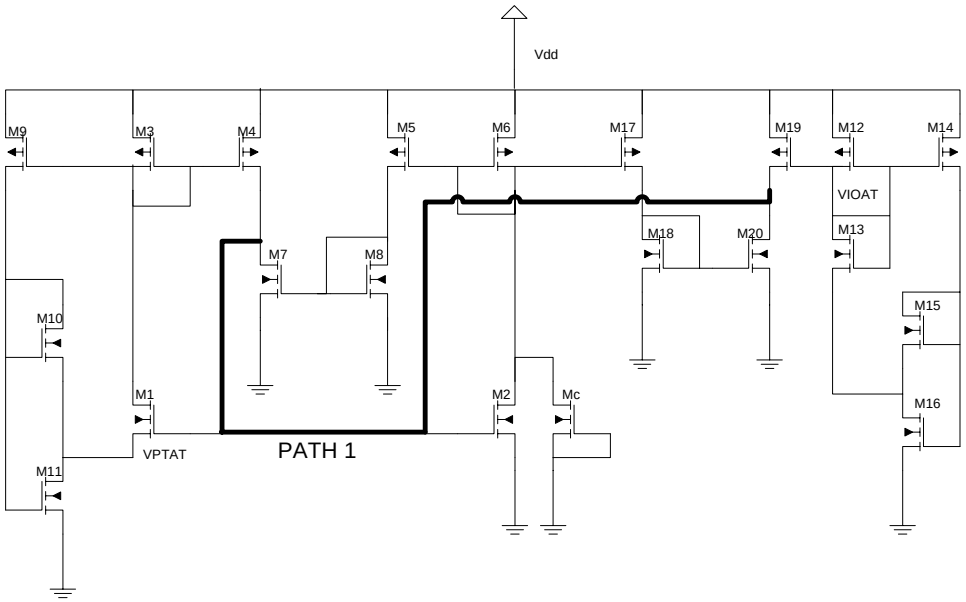


Figure 3.5 Path 1.

Table 3.1 Ratio List

NMOS					PMOS				
M7	M8	M10	M11		M3	M4	M5	M6	M9
1	1	N	1		1	1	1	P	M
M15	M16	M18	M20		M12	M14	M17	M19	
S	1	1	1		1	Q	1	1	

The ratios of transistors are shown in Table 3.1and Table 3.2. According to the equations (3.6) to (3.9), we can write:

$$I_{D10} = N \cdot \frac{\beta_{10}}{2n}(V_{GB10} - V_{TO} - nV_{PTAT})^2 = M \cdot I_{D12} \tag{3.10}$$

$$I_{D11} = \beta_{11} \cdot [(V_{GB11} - V_{TO}) - \frac{n}{2}V_{PTAT}] \cdot V_{PTAT} = (M+1) \cdot I_{D12} \tag{3.11}$$

Set the bodies of M10 and M11 connect to ground. Because the gates of M10 and M11 are connected together, we can get:

$$I_{D12} = \frac{2n\beta_{11}{V_{PTAT}}^2}{4 \cdot (M+1)^2} \cdot \frac{M}{N} \cdot (1 + \sqrt{1 + N + \frac{N}{M}})^2 \tag{3.12}$$

The same idea is applied in the right side of this circuitry.

$$I_{D15} = S \cdot \frac{\beta_{15}}{2n}(V_{GB15} - V_{TO} - nV_X)^2 = Q \cdot I_{D12} \tag{3.13}$$

$$I_{D16} = \beta_{16} \cdot [(V_{GB16} - V_{TO}) - \frac{n}{2}V_X] \cdot V_X = (Q+1) \cdot I_{D12} \tag{3.14}$$

Where $V_X = V_{D16} = V_{S15} = V_{S13}$. Set the bodies of M15 and M16 connect to ground. Because the gates of M15 and M16 are connected together, we can get:

$$I_{D12} = \frac{2n\beta_{16}{V_X}^2}{4 \cdot (Q+1)^2} \cdot \frac{Q}{S} \cdot (1 + \sqrt{1 + S + \frac{S}{Q}})^2 \tag{3.15}$$

If all transistors are matched, equation (3.12) and (3.15) can be combined as:

$$\frac{V_{PTAT}^{\ 2}}{(M+1)^2}\cdot\frac{M}{N}\cdot(1+\sqrt{1+N+\frac{N}{M}})^2=\frac{V_x^{\ 2}}{(Q+1)^2}\cdot\frac{Q}{S}\cdot(1+\sqrt{1+S+\frac{S}{Q}})^2 \tag{3.16}$$

Simplify equation (3.16), we can get:

$$V_X=\frac{Q+1}{M+1}\cdot\frac{1+\sqrt{1+N+\frac{N}{M}}}{1+\sqrt{1+S+\frac{S}{Q}}}\cdot\sqrt{\frac{M}{N}\cdot\frac{S}{Q}}\cdot V_{PTAT} \tag{3.17}$$

From equation (3.17), the V_{IOAT} can be written as:

$$V_{IOAT}=V_{GSn13}+K\cdot V_{PTAT}$$
(3.18)

Where

$$K=\frac{Q+1}{M+1}\cdot\frac{1+\sqrt{1+N+\frac{N}{M}}}{1+\sqrt{1+S+\frac{S}{Q}}}\cdot\sqrt{\frac{M}{N}\cdot\frac{S}{Q}} \tag{3.19}$$

K is a design parameter which composed of transistor ratios. Because M, N, S, and Q are ratios, they will make K more accurate when the manufacturing process varies.

In order to get a zero temperature coefficient, we take the derivative of equation (3.18) with respect to temperature (T).

$$\frac{\partial V_{GSn13}}{\partial T}+K\cdot\frac{k}{q}\cdot\ln p=0 \tag{3.20}$$

According to equation (2.13) and (2.14), we can rewrite equation (3.20) as:

$$K\cdot\frac{k}{q}\cdot\ln p+\frac{1}{T_0}[K_{Tn}+V_{GS}(T_0)-V_{THn}(T_0)-V_{OFFn}]=0 \tag{3.21}$$

From equation (3.21), we can get the design constant K will be:

$$K=\frac{q}{k\cdot T_0\cdot\ln p}[V_{THn}(T_0)+V_{OFFn}-K_{Tn}-V_{GSn}(T_0)] \tag{3.22}$$

Above all, two PTAT and IOAT reference circuitry architectures are designed. The linearity of PTAT reference is compensated by the transistor, Mc. This compensation technique has been proposed before. Our design is to add a well-defined IOAT

reference and an efficient current compensation circuit. This Chapter has described the design concepts of two proposed circuits, one is resistor-based PTAT and IOAT reference circuitry architecture and another one is all-MOS-based PTAT and IOAT reference circuitry architecture.

Next session we will discuss the power-supply rejection ratio (PSRR) issue.

3.3 Power Supply Rejection Ratio (PSRR)

From section 3.2, we proposed two PTAT and IOAT reference circuitry architectures and some compensation technique. However, the power supply rejection ratio (PSRR) of these circuits deteriorates sharply in deep-submicro technology. So the analysis of PSRR is necessary for a reference circuit. The PSRR of PTAT reference has been discussed in previous research [18].

The small signal DC gain v_{ptat}/v_{dd} of this circuit can be derived from the low frequency small signal model shown in Fig. 3.6. Assume $g_o << g_m$ for all transistors, then

$$A_{ptat} \approx \frac{v_{ptat}}{v_{dd}} \approx \frac{R \cdot g_{m7} \cdot g_{m5} \cdot g_{m3} \cdot (g_{m2} \cdot g_{o1} - g_{m1} \cdot g_{o2})}{g_{m2} \cdot g_{m7} \cdot g_{m5} \cdot g_{m3} \cdot (1 + g_{m1} \cdot R) - g_{m1} \cdot g_{m4} \cdot g_{m6} \cdot g_{m8}} \tag{3.23}$$

If $g_{m4} = g_{m5}$ and $g_{m7} = g_{m8}$, the above equation can be written as

$$A_{ptat} \approx \frac{v_{ptat}}{v_{dd}} \approx \frac{R \cdot g_{m3} \cdot (g_{m2} \cdot g_{o1} - g_{m1} \cdot g_{o2})}{g_{m2} \cdot g_{m3} \cdot (1 + g_{m1} \cdot R) - g_{m1} \cdot g_{m6}} \tag{3.24}$$

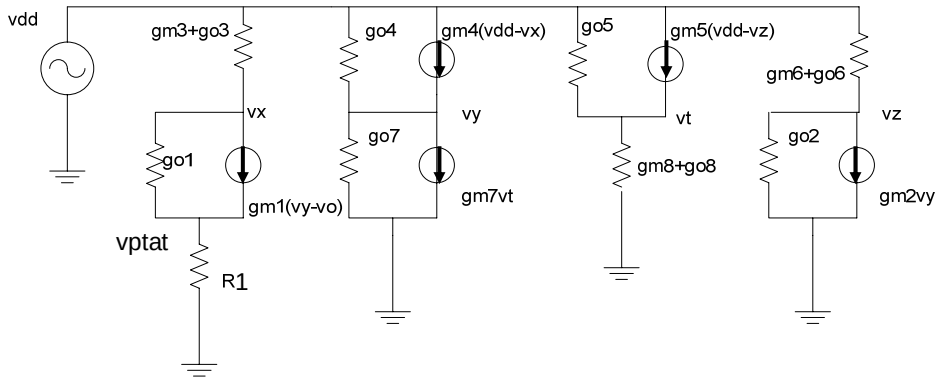


Figure 3.6 Low-frequency small-signal model of the resistor-based PTAT reference shown in Fig. 3.3.

According to above result, we can know that $g_{m2} \cdot g_{o1} = g_{m1} \cdot g_{o2}$ and $PSRR^{+} \to \infty$ for low frequency response.

After finishing the PSRR analysis of PTAT reference, we continue to discuss the PSRR analysis of IOAT reference in this circuit.

The small signal DC gain v_{ioat}/v_{dd} of this circuit can be derived from the low frequency small signal model shown in Fig. 3.7. Assume $g_o << g_m$ for all transistors, then

$$v_{ioat} = (v_{dd} - v_{ioat}) \cdot g_{o9} + g_{m9} \cdot (v_{dd} - v_x) \cdot (R_2 + \frac{1}{g_{mn} + g_{on}}) \tag{3.25}$$

And the voltage of node x can be derived as:

$$(v_{dd} - v_x) \cdot (g_{m8} + g_{o8}) = {v_{ptat}}/{R_1} \tag{3.26}$$

$$v_x = v_{dd} - \cdot \frac{v_{ptat}}{R_1 \cdot (g_{m8} + g_{o8})} \tag{3.27}$$

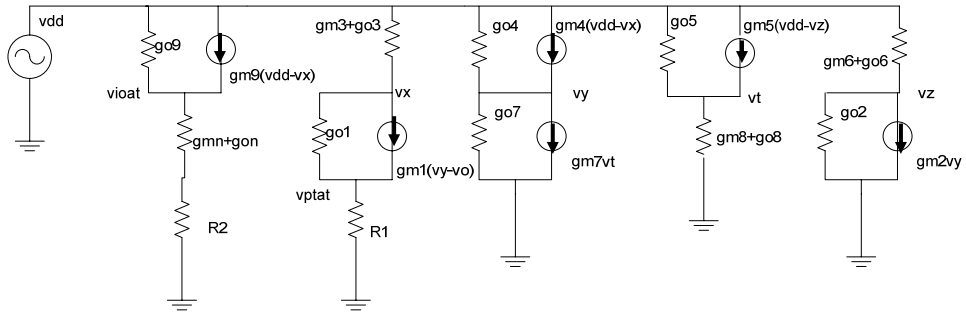


Figure 3.7 Low-frequency small-signal model of the resistor-based IOAT reference shown in Fig. 3.3.

Take equation (3.36) into equation (3.34), we can get the gain of V_{ioat}, A_{ioat} as

$$\frac{v_{ioat}}{v_{dd}} \approx \frac{1}{1 + g_{o9}} \cdot [g_{o9} + A_{ptat} \cdot (\frac{R_2}{R_1} \cdot \frac{g_{m9}}{g_{m8} + g_{o8}} + \frac{g_{m9}}{R_1 \cdot (g_{m8} + g_{o8}) \cdot (g_{mn} + g_{on})})] \tag{3.28}$$

Where A_{ptat} is shown in equation (3.23) and (3.24)

According to above result, if $g_{m2} \cdot g_{o1} = g_{m1} \cdot g_{o2}$, the PSRR of PTAT reference will become infinite, and the gain of the IOAT reference will be

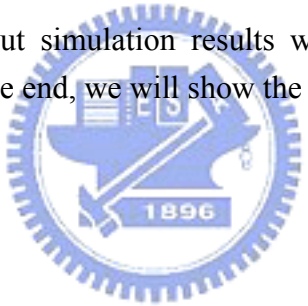
$$A_{ioat} \approx \frac{g_{o9}}{1+g_{o9}} \tag{3.29}$$

If $g_{o9} >> 1$, the gain of IOAT reference will be unity. So we can know the power supply rejection ratio (PSRR) of IOAT is dependent on the power supply rejection ratio (PSRR) of PTAT, and the gain of IOAT reference will been unity.

3.4 Summary

In this Chapter, we proposed two kinds of PTAT and IOAT reference circuitry architectures, which one is resistor-based and another one is all-MOS-based. The design concepts are well described in this Chapter. After we describe the circuits, the issue of power supply rejection ratio (PSRR) is also discussed. According to the results, we know the PSRR of PTAT can achieve to infinite. When this happened, the gain of IOAT reference will be unity. The much well the PSRR of PTAT, the much well the PSRR of IOAT is.

Next Chapter, the pre-layout simulation results will be shown. And the layout concept is also discussed. In the end, we will show the post-layout simulation results.



CHAPTER 4

Simulation and Experimental Results

In this Chapter, the both pre-layout simulation and post-layout simulation are presented. We simulate the both resistor-based and all-MOS-based circuitry architectures with TSMC 0.18μm CMOS technology. Moreover, all-MOS-based circuitry architecture is further simulated with TSMC 0.13μm CMOS technology. Then, the layout with TSMC 0.18μm CMOS technology is shown. Post-layout simulation is shown in the end of this Chapter.

4.1 Pre-layout Simulation

In Chapter 3, we proposed two new circuitry architectures, resistor-based and all–MOS based voltage generators and have been complete described. First, we simulate both the circuitry architectures with TSMC 0.18μm CMOS technology. The simulation results are shown in figure 4.1 and 4.2.

Figure 4.1 shows the PTAT voltage versus temperature for all-MOS-based and resistor-based PTAT references simulated in TSMC 0.18μm 1P6M standard CMOS technology. The simulation range is from -55°C to 170°C temperature range conduced for each circuit. The R-squares of resistor-based and all-MOS-based circuits are 0.99963 and 0.99968 respectively.

Figure 4.2 shows the PTAT voltage versus temperature for all-MOS-based IOAT reference simulated in TSMC 0.18μm 1P6M standard CMOS technology. The simulation range is from -55°C to 170°C for each circuit. The means of resistor-based and all-MOS-based circuits are 578.75mV and 514.94mV respectively. The variation

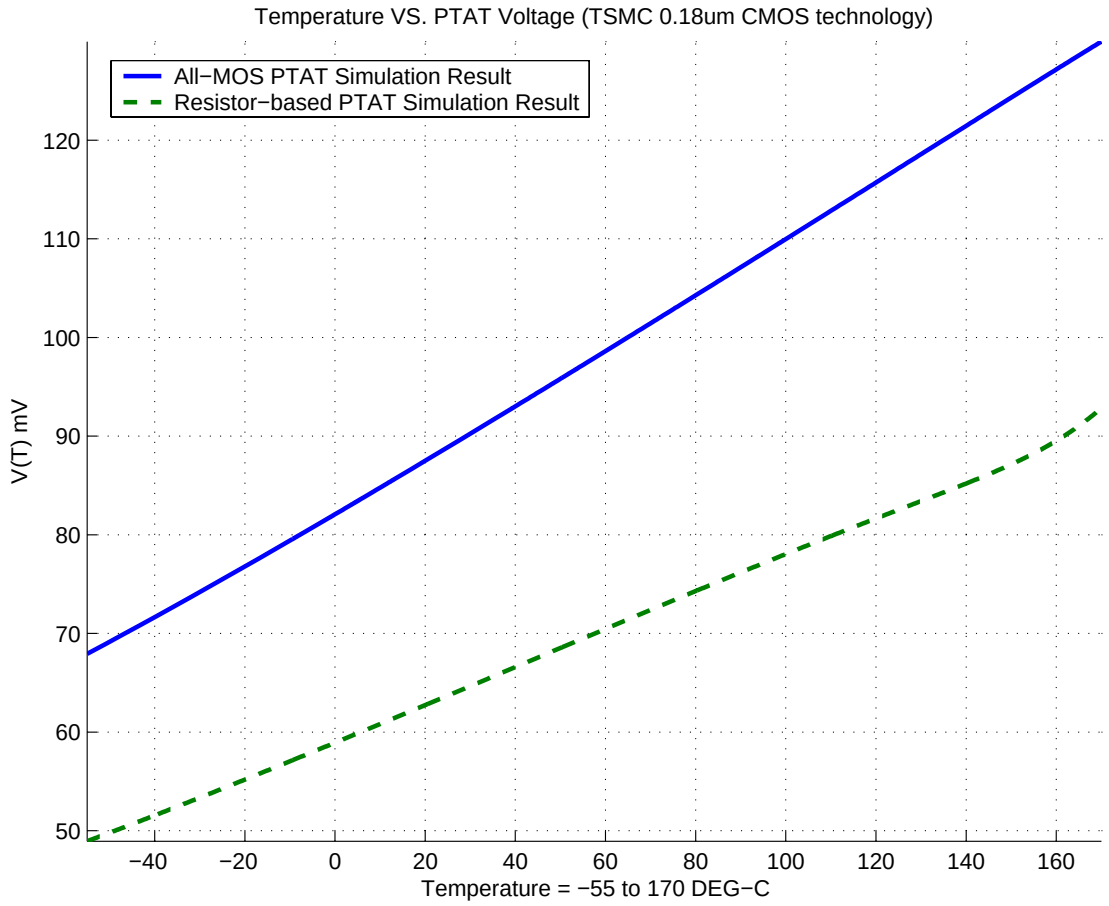


Figure 4.1 The simulation result of PTAT references simulated in TSMC 0.18μm CMOS technology.

of the resistor-based circuit is about ±5mV. For the all-MOS-based circuit, the variation is about ±8mV.

The performance is summarized in Table 4.1. All the transistors aspects are shown in Table 4.2 and Table 4.3. According to the simulation results, we know the performance of resistor-based circuit is not better than the performance of all-MOS-based circuit. Moreover, for the area consideration, resistor-based circuit requires more area. This means the resistor-based circuitry architecture is not suited for the market demand. For the low cost consideration, we give up this architecture, and force on all-MOS-based circuitry architecture. The further simulation of all-MOS-based circuitry architecture is done with TSMC 0.13μm CMOS technology.

Table 4.1 Summary of TSMC 0.18μm CMOS technology simulation results

TSMC 0.18μm	**PTAT Temperature Coefficient (mV / °C)**	**PTAT R-square**	**IOAT Mean (mV)**
R-based	**0.206**	**0.99963**	**514.94**
All-MOS-based	**0.276**	**0.99968**	**578.75**

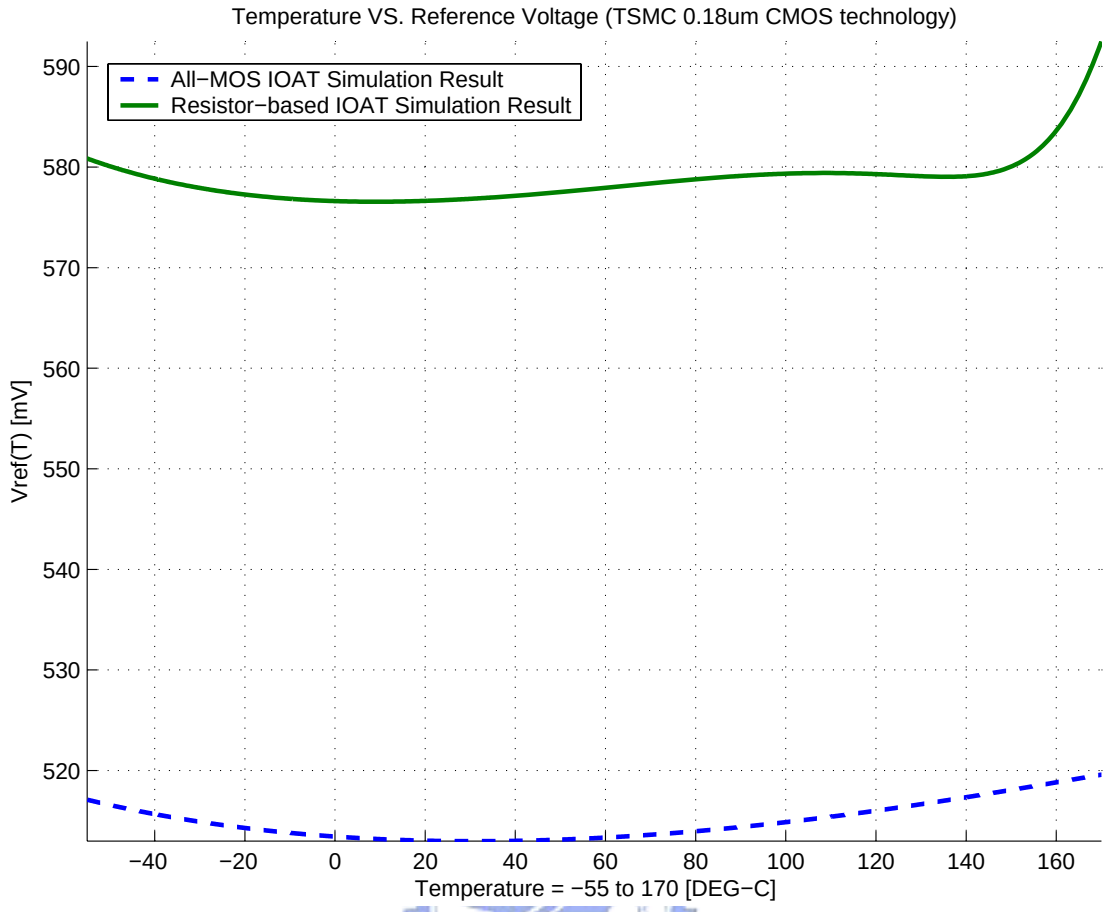


Figure 4.2 The simulation result of IOAT references simulated in TSMC 0.18μm CMOS technology.

Table 4.2 Sizing of resistor-based circuit in TSMC 0.18μm CMOS technology

TSMC 0.18μm CMOS technology	Model Name	Aspect (W/L)
M1,M2,Mn	NCH	1.2/0.36 m=40
M3,M4	PCH	0.6/2.8
M5	PCH	0.64/0.6 m=10
M6,M7,M8,M9	PCH	0.64/0.6
Mc	NCH	1.2/0.36 m=150
X1	Rppo1rpo	2/3050
X2	Rppo1rpo	2/12800

Table 4.3 Aspect of all-MOS-based circuit in TSMC 0.18μm CMOS technology

TSMC 0.18μm CMOS technology	Model Name	Aspect (W/L)
M1,M2,M13	NCH	1.2/0.36 m=20
M3,M4,M5,M9,M12,M14,M17,M19	PCH	0.44/0.6
M6	PCH	0.44/0.6 m=10
M7,M8,M10,M11,M15,M16,M18,M20	NCH	0.3/1.4
Mc	NCH	0.3/1.4 m=132

Figure 4.3 shows the PTAT voltage versus temperature for all-MOS-based PTAT reference simulated in TSMC 0.13μm 1P8M standard CMOS technology. The simulation range is from -55°C to 170°C temperature range conduced for each circuit. The R-squares of all-MOS-based circuits are 0.99969 and 0.99968.

Figure 4.4 shows the PTAT voltage versus temperature for all-MOS-based IOAT reference simulated in TSMC 0.13μm 1P8M standard CMOS technology. The simulation range is from -55°C to 170°C for each circuit. The means of all-MOS-based circuit is 417.26mV. Table 4.4 summarized this simulation. All the transistors aspects are shown in Table 4.5.

Table 4.4 Summary of TSMC 0.13μm CMOS technology simulation result

	PTAT Temperature Coefficient (mV / °C)	**PTAT R-square**	**IOAT Mean (mV)**
All-MOS (0.13μm)	**0.267**	**0.99969**	**417.26**

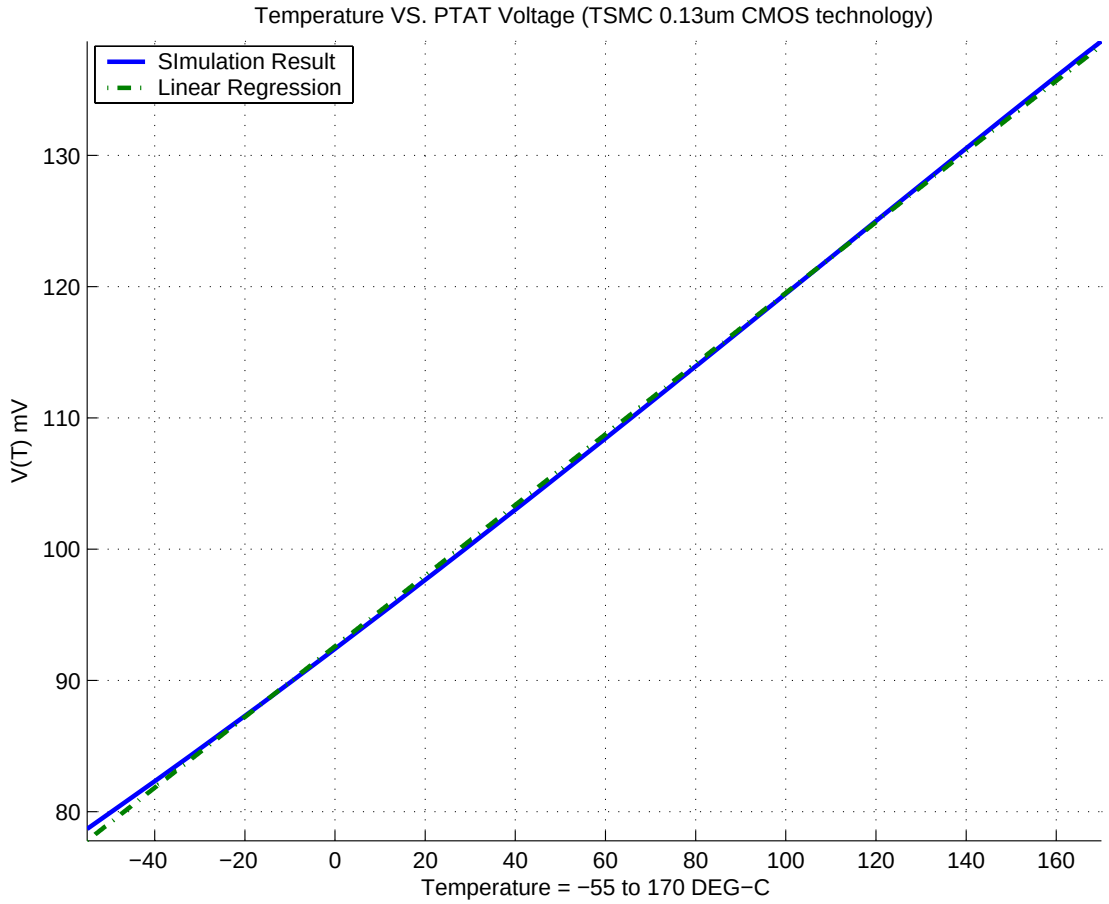


Figure 4.3 The simulation result of PTAT reference simulated in TSMC 0.13μm CMOS technology.

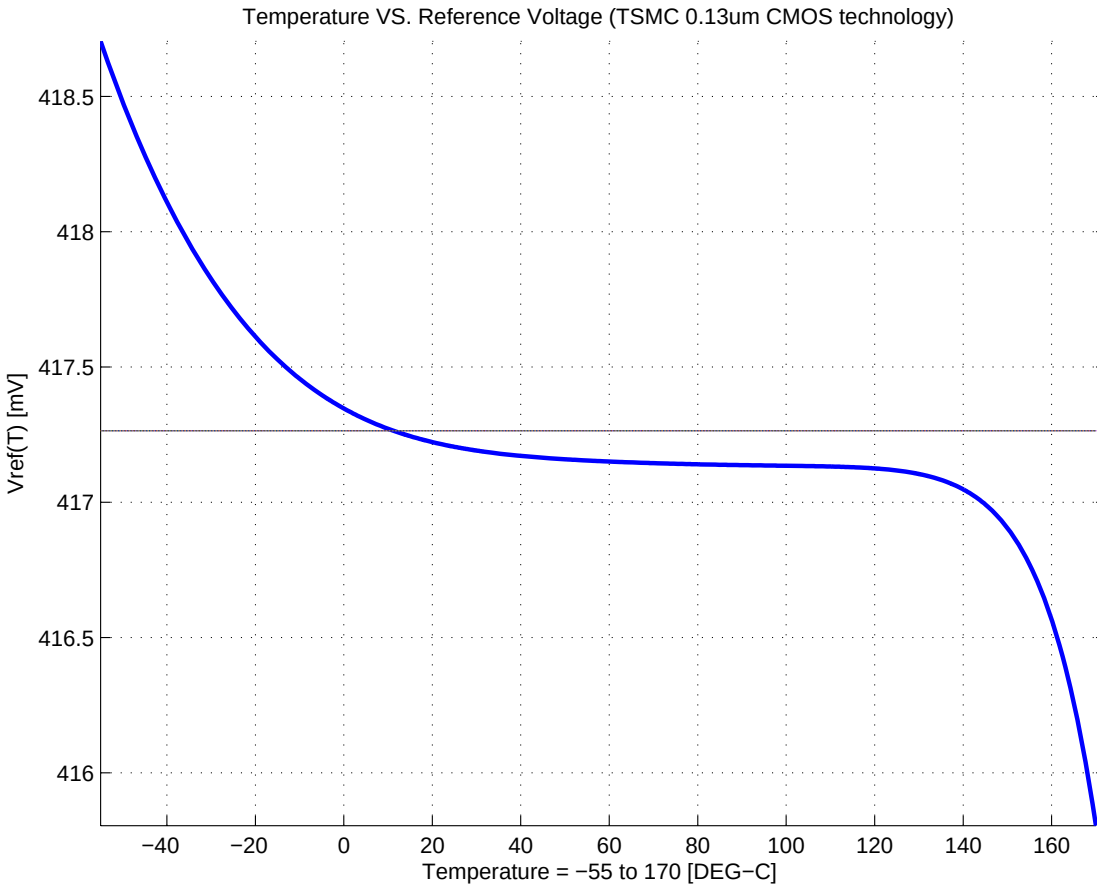


Figure 4.4 The simulation result of IOAT reference simulated in TSMC 0.13μm CMOS technology.

Table 4.5 Aspect of all-MOS-based circuit in TSMC 0.13μm CMOS technology

TSMC 0.13μm CMOS technology	Model Name	Aspect (W/L)
M1,M2,M13	N	0.6/0.2 m=20
M3,M4,M5,M9,M12,M14,M17,M19	P	0.2/0.3
M6	P	0.2/0.3 m=10
M7,M8,M10,M11,M16,M18,M20	N	0.2/0.7
Mc	N	0.6/0.18 m=132
M15	N	0.2/0.6

Above all, we know that all-MOS-based circuitry architecture takes advantage of both area and performance. Figure 4.5 shows both PTAT and IOAT voltage references together. The simulation results done with TSMC 0.18μm and 0.13μm CMOS technology have shown all-MOS-based circuit is well-work in this two kinds of technology. In next session, the layout in TSMC 0.18μm CMOS technology is presented. The layout concept is also described. The post-layout simulation is shown in the end of next session.

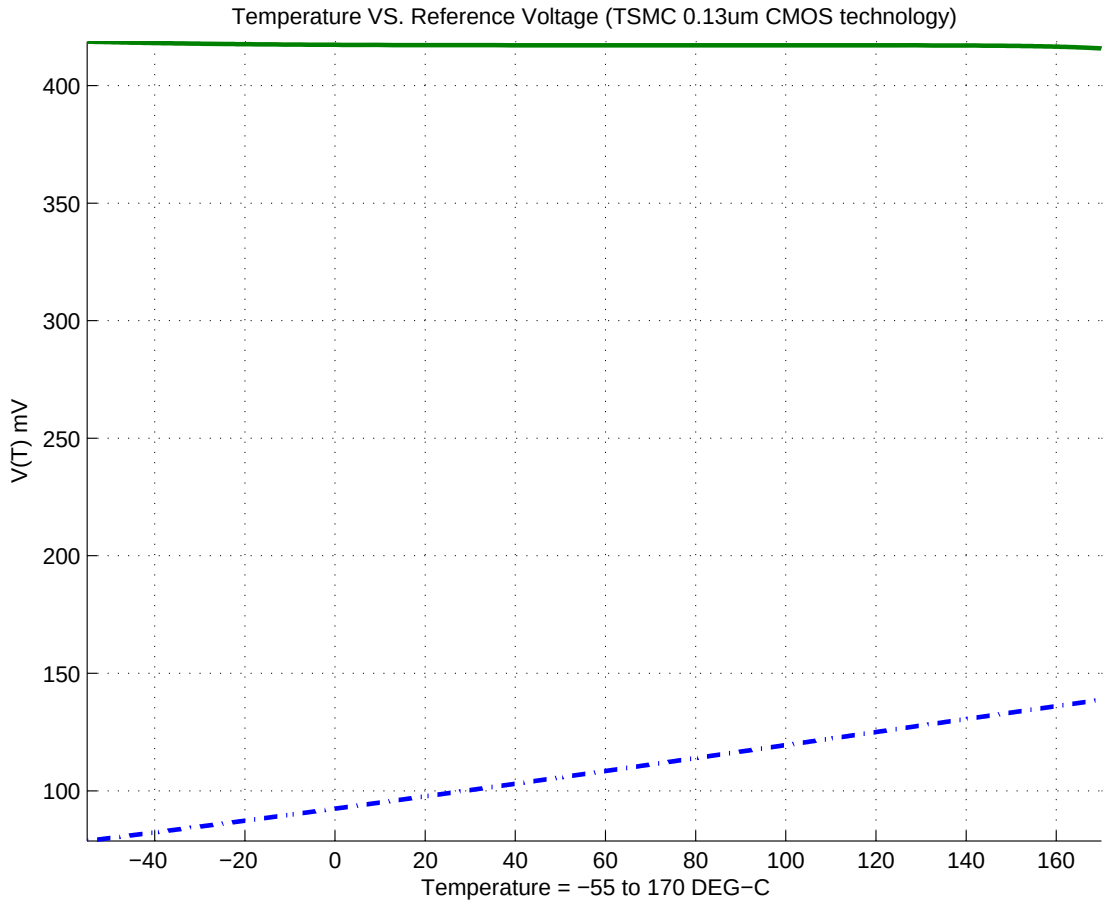


Figure 4.5 The simulation results of both PTAT and IOAT references simulated in TSMC 0.13μm CMOS technology.

4.2 Layout Consideration and Post-layout Simulation

Before we start the layout implementation, the fine tuning concept has to be considered. The positive and negative temperature coefficients will be changed due to the change of current ratio after LPE (PEX). So the constant K which we introduce in Chapter 3 has to be modified after LPE (PEX). Our design flow is shown in figure 4.6. Figure 4.7 shows the layout of all-MOS-based circuit which is designed with TSMC 0.18μm 1P6M CMOS technology. Because of fine tuning consideration, the length of M15 is designed to be easily changed in the layout. The supply voltage is 1.2v and area is about $42um \times 31um$ ($1260um^2$). Figure 4.8 and 4.9 show the post-layout simulation of PTAT and IOAT references before fine tuning. Figure 4.10 and 4.11 show the post-layout simulation of PTAT and IOAT references after fine tuning. The post-layout simulation results compared with pre-layout simulation result are summarized in Table 4.6. In next session, we have a discussion on these simulation results and some considerations for applying our circuit in smart temperature sensors.

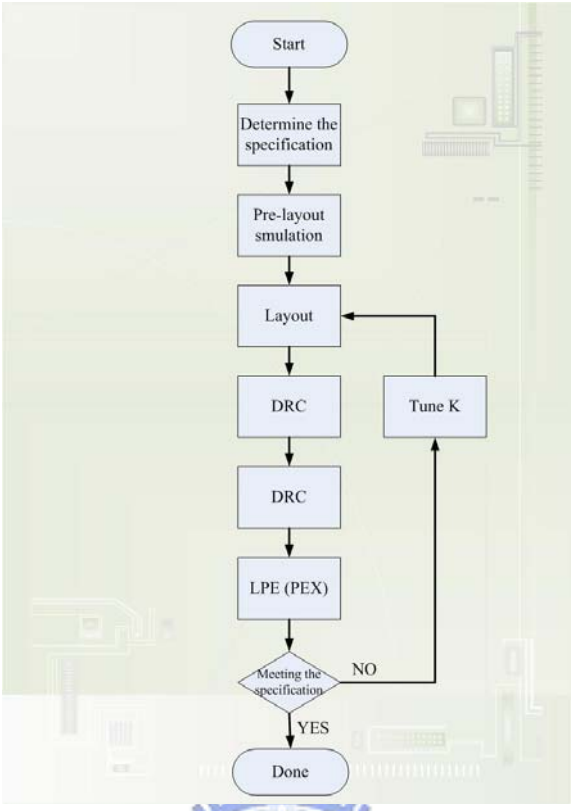


Figure 4.6 The block diagram of our design flow.

Figure 4.7 The all-MOS-based layout of TSMC 0.18μm 1P6M CMOS technology.

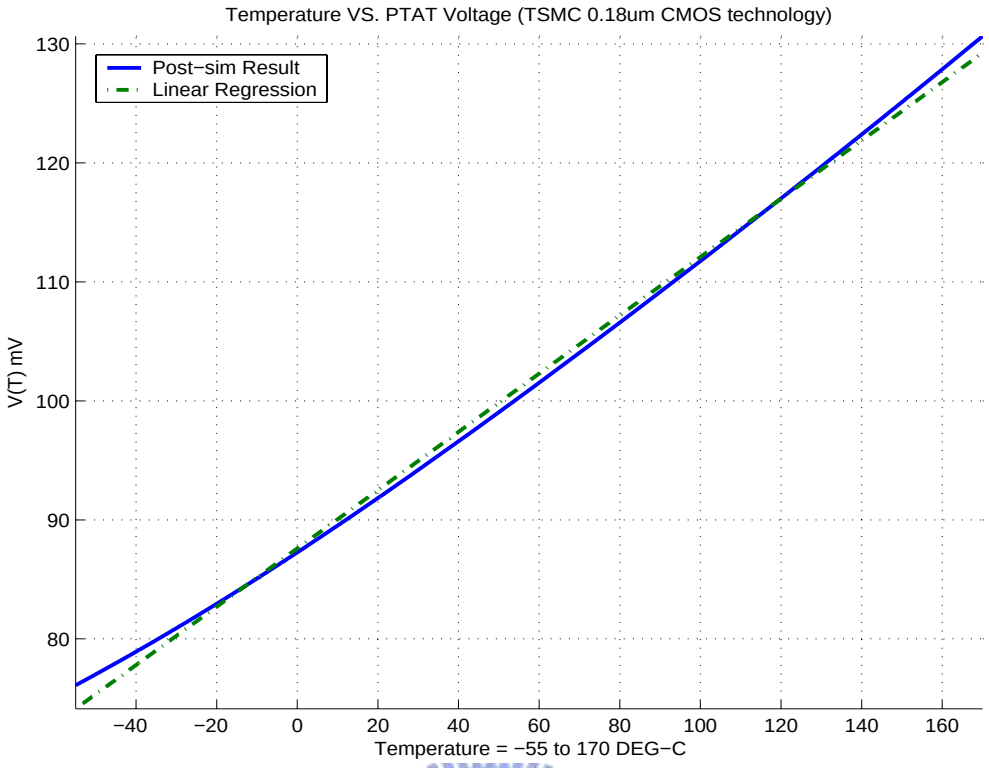


Figure 4.8 Post-layout simulation of PTAT reference before tuning.

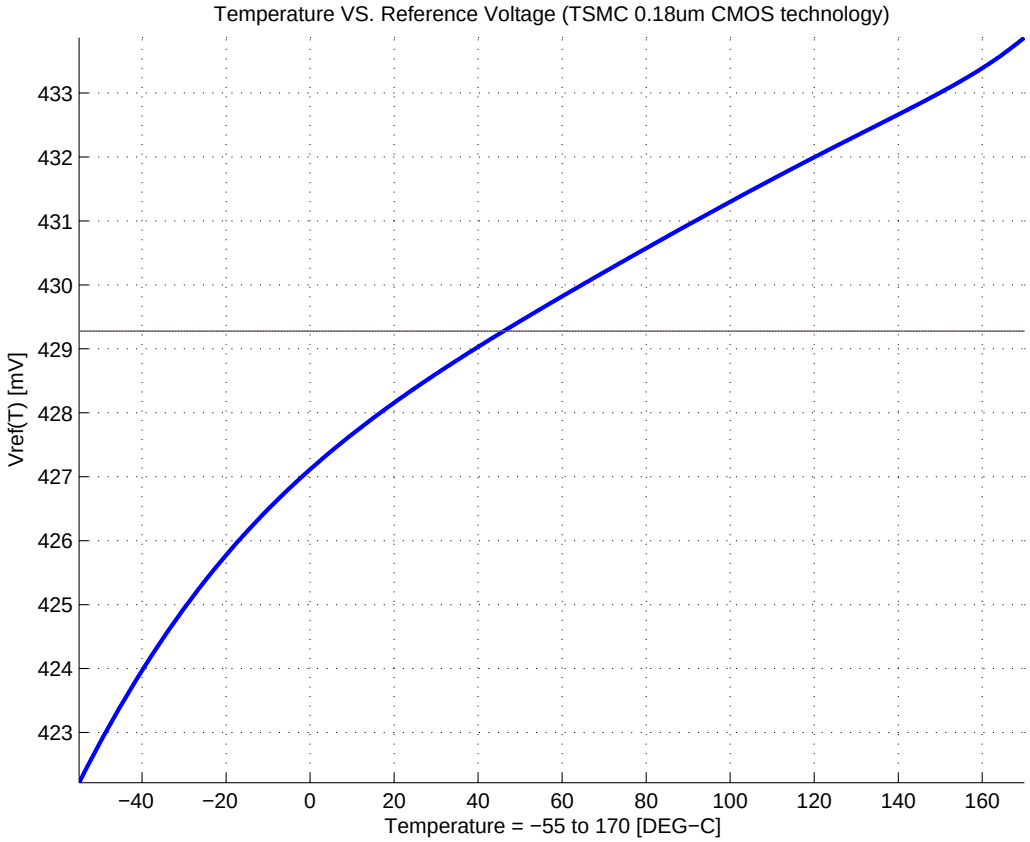


Figure 4.9 Post-layout simulation of IOAT reference before tuning.

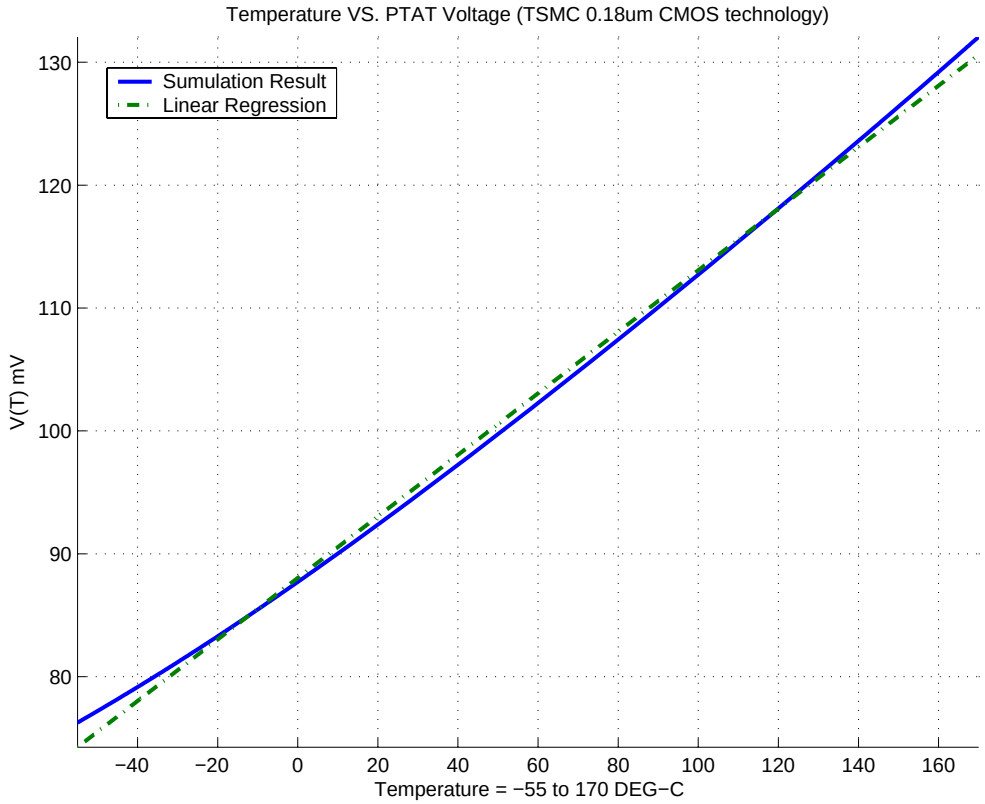


Figure 4.10 Post-layout simulation of PTAT reference after tuning.

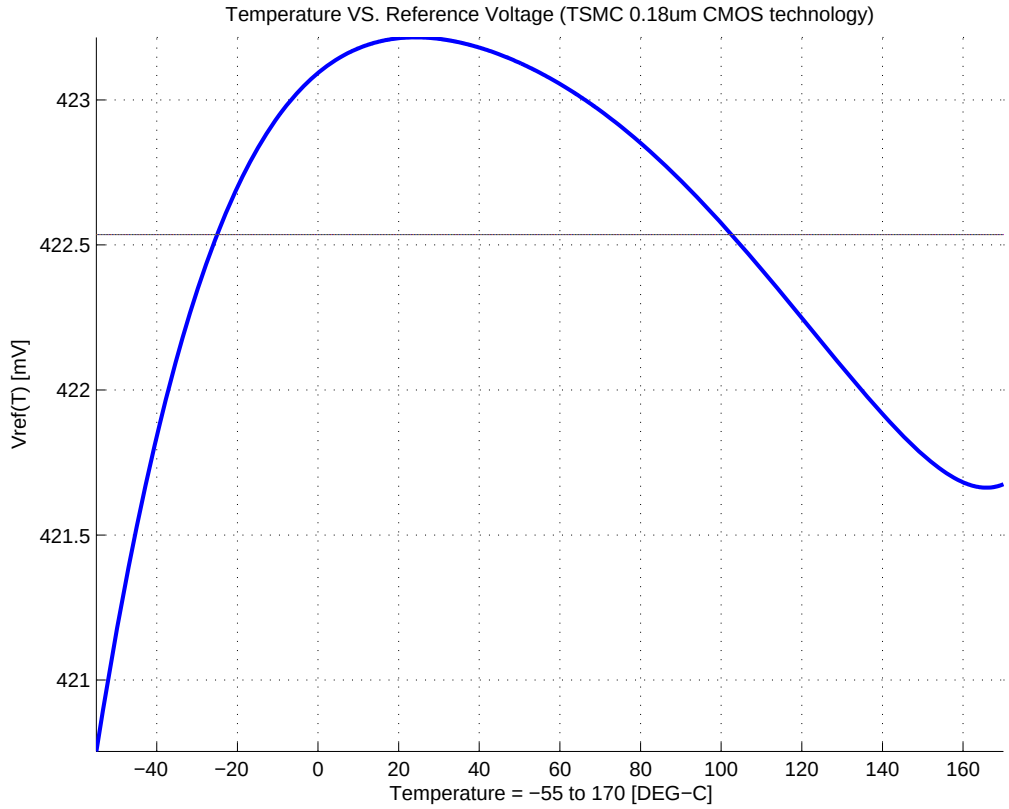


Figure 4.11 Post-layout simulation of IOAT reference after tuning.

Table 4.6 Simulation summary of all-MOS-based circuitry architecture

All-MOS-based (0.18μm)	Power (μW)	PTAT TC (mV / °C)	PTAT R-square	IOAT Variance* (mV)
Pre-sim	**18.4773**	**0.276**	**0.99968**	**87.12**
Post-sim	**27.8820**	**0.257**	**0.99787**	**142.49**
Post-sim (after tuning)	**28.5227**	**0.264**	**0.99788**	**28.46**

$*Variance = [\sum (y(i) - mean)^2]^{1/2}$

4.3 Discussion

According to the post-layout simulation results, we know that the linearity of PTAT is almost the same with pre-layout simulation results. It means the compensation circuit (M17-M20, and Mc) is efficient. But the variation of IOAT is dependent on the process variance. In this work, we run the design flow to get the optimization of IOAT in the simulation level. The results also prove the improvement of IOAT by fine tuning.

In order to apply our work in smart temperature sensors, the level shift circuit has to design. When we take PTAT and IOAT as temperature signals, the first thing we have to do is to shift PTAT and IOAT in order to produce a cross point. The cross point will be defined as reference voltage at certain temperature. And if we subtract PTAT from this cross point, the difference will be taken as temperature difference signal. After the process of A/D converter, the digital value of temperature will be presented.

Above all, we can know how to improve the variation of IOAT and some design concepts for using this proposed circuit and some considerations for applying our circuit in smart temperature sensors. The conclusions and future works are discussed in next Chapter.

CHAPTER 5

Conclusions and Future Works

In the previous Chapter, simulation and experimental results have been shown. Basing on those results, we make some conclusions of proposed design. Section 5.1 describes the conclusions of this thesis. The long term future works are also discussed in Section 5.2.

5.1 Conclusions

At the beginning, we review the temperature sensing methods, from mercury-in-glass thermometer to very low power and low cost smart temperature sensors. Then we discuss the advantages and disadvantages of both bipolar transistors and subthreshold MOSFETs for the low power design. Finally, we proposed new PTAT and IOAT reference circuitry architectures and show the simulation and experimental results.

In this thesis, $-55^{o}C$ to $170^{o}C$ high linear voltage references circuitry for fully integrated temperature sensor is designed and implemented in TSMC 0.13μm and 0.18μm CMOS technology. The proposed circuit utilized temperature complementation technique on PTAT and IOAT references. Base on the simulation results, the R-squares of both circuitries are better than 0.999 in a considerable wider temperature range from $-55^{o}C$ to $170^{o}C$ as shown in the Chapter 4. Thus, a fully integrated temperature sensor with wider temperature range is designed and easily to integrate to modern system-on-chip designs with minimal efforts. In a world, we can make three points to conclude the thesis.

1. Propose the architecture based on subthreshold MOSFETS that produce both VPTAT and VREF. And the circuitry is working in both TSMC 0.18μm and 0.13μm CMOS technology.
2. Compensate the leakage current to get good linearity in high temperature.

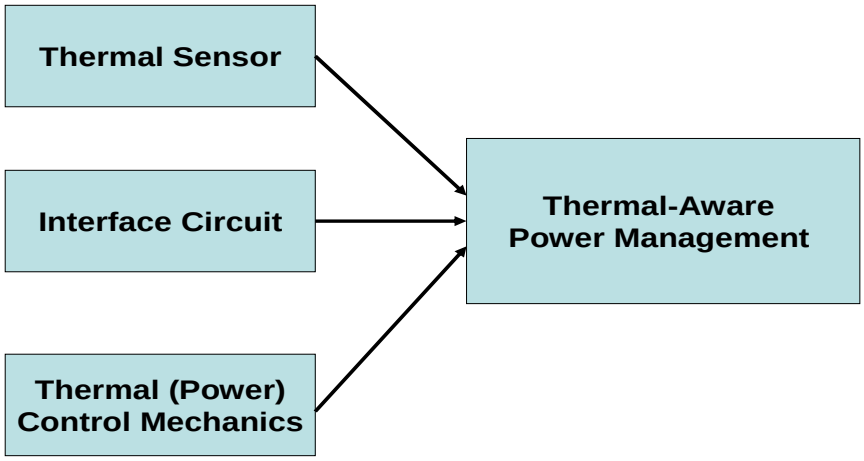


Figure 5.1 The block diagram of the thermal-aware power management system.

3. A fully integrated temperature sensor with wider temperature range (-55~170 ^{o}C) is designed and easily to integrate to modern SOC designs with minimal efforts.

5.2 Future Works

Our long term goal is to implement the thermal-aware power management. The mid term goal is to structure a very low power and high performance smart temperature sensor. After this thesis' work, the next step will be to research how to efficiently combine this PTAT and IOAT reference circuitry architecture with A/D converter. However, some dynamic offset-cancellation techniques should be applied in order to maintain or even improve the performance. Finally, integrate with digital interface bus to get the digital output for the thermal-aware power management. Figure 5.1 shows the block diagram of this system.

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