國 立 交 通 大 學

電信工程研究所

博 士 論 文

超寬頻射頻關鍵積體電路之設計與分析

Design and Analysis of Key Radio Frequency Integrated Circuits for Ultra-Wideband Communication Systems

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摘要

本篇論文提出了數種適用於超寬頻通訊系統的 0.18 微米互補式金氧半製程關鍵積體電路元件的架構、分析與設計。其中包含了 (1)兩個高線性度之寬頻降頻器的分析與設計；(2)應用於超寬頻系統的全頻帶頻率合成器的設計；(3)具溫度補償效應的主動式電感電壓控制震盪器；(4)利用電流再利用技術的半動態除三電路。

首先談到的是第一種寬頻高線性度降頻器。此混頻器使用摺疊疊接式的吉伯特混頻器架構，此摺疊疊接式混頻器包含高線性度的轉導級搭配寬頻切換級，除了可以增加輸出訊號的擺幅之外，亦針對此混頻器的線性度做了理論及實務上的設計與分析。利用諧波平衡理論分析推導電路的轉導結構，推導出抑制三階諧波的條件進而達成線性度的提升。量測結果顯示，此寬頻降頻器於使用頻段範圍內的轉換增益為 3.3 ± 1.5 dB，等效輸入端之增益 1-dB 壓縮點(IP_{1dB})為−2.8 dBm，等效輸入端之三階互調失真點(IIP_3)為 6.9 dBm。此寬頻降頻器的工作電壓為 1.8 伏特，共消耗功率 14.4 mW。 此降頻器的晶片面積為 0.7 × 0.58 平方毫米。基於第一種提出的降頻器的成果，第二種寬頻的降頻器再搭配上整合於晶片內的寬頻主動式巴倫電路。在此提出的寬頻主動式巴倫電路的目的為於單端輸

入訊號的情況之下，可以用來產生寬頻的雙端平衡輸出。利用寬頻主動式巴倫的小訊號模型推導出了精確的相位差關係式，進而推知此主動式巴倫於 2 GHz 到 13 GHz 的使用頻段範圍內可達到只有 2 dB 的增益差異及 4 度的相位差異。由量測結果顯示，此具有寬頻巴倫的寬頻降頻器的轉換增益為 6.9 ± 1.5 dB，等效輸入端之增益 1-dB 壓縮點(IP_{1dB})為-3.5 dBm，等效輸入端之三階互調失真點(IIP_3)為 6.5 dBm，此寬頻降頻器的工作電壓為 1.8 伏特時，總共消耗 25.7 mW。此降頻器的晶片面積為 0.85 × 0.57 平方毫米。

其次，本論文提出了一個應用於 IEEE 802.15.3a 協定之超寬頻頻率合成器。此應用多頻帶正交頻率多工技術的超寬頻頻率合成器主要由兩組鎖相迴路，一個半動態除七電路，以及一個鏡像抑制混波器所構成。模擬結果顯示此頻率合成器全頻帶的頻率切換時間均小於 2 ns，諧波抑制能力為 25 dBc 以上，工作電壓 1.3 伏特時共消耗 111 mW。此頻率合成器的晶片面積為 2.29 × 2.51 平方毫米。

再其次，本論文提出一個應用具溫度補償效應的主動式電感之電壓控制震盪器。利用具溫度補償效應的主動式電感，可降低環境溫度對主動式電感所造成因電流改變而影響感值的效應。量測結果顯示，此震盪器在外界溫度由-20℃ 到 60℃ 的條件之下，震盪頻率的變異度只有 0.99%。當中心頻率操作於 2.4GHz 時，離載波頻率 1MHz 的相位雜訊為-91 dBc/Hz。當中心頻率為 2.25GHz 時，頻率操作範圍可達 48.89%。此震盪器的晶片面積為 0.19 × 0.195 平方毫米。

最後，本論文提出了一個可應用於 60-GHz 超寬頻系統的半動態除三電路。此除頻器主要由一組吉伯特混頻器，一級靜態除頻器，以及輸入端的主動式巴倫所組成。其中混頻器的切換級亦同時為除頻器的電流源，進而達成電流再利用的共同結構。由實驗的結果分析得知，在 1.5 伏特的工作電壓操作時，功率消耗為 12 mW。當輸入訊號功率為 0 dBm 時，除頻範圍為 1080MHz。

Design and Analysis of Key Radio Frequency Integrated Circuits for Ultra-Wideband Communication Systems

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ABSTRACT

In this dissertation, the design methodologies and implementations of key radio frequency integrated circuits (RFICs) for ultra-wideband (UWB) communication systems are proposed. There are four parts in this thesis, including: (1) the analysis and design of two wideband high-linearity down conversion mixers, (2) the design of full-band synthesizer for UWB applications, (3) the design of active inductor based proportional to absolute temperature (PTAT) voltage-controlled oscillator (VCO), and (4) the design of current-reused divide-by-3 semi-dynamic frequency divider (SDFD).

Firstly, a 2.4 to 10.7 GHz high-linearity CMOS down conversion mixer using 0.18-μm CMOS technology is demonstrated. The mixer employs a folded cascode Gilbert cell topology. The folded cascode approach is adopted to increase the output swing, and the linearity is enhanced by a harmonic distortion canceling technique

derived from the harmonic balance analysis. The proposed configuration shows the highest IIP_3 and IP_{1dB}, and exhibits more compact size than most of published works. This wideband mixer has the conversion gain of 3.3 ± 1.5 dB, input 1-dB compression point (IP_{1dB}) of -2.8 dBm, and third-order input intercept point (IIP_3) of 6.9 dBm under the power consumption of 14.4 mW from a 1.8 V power supply. The chip area is 0.7 × 0.58 mm^2. The second wideband high-linearity mixer is operated from 2 to 11 GHz with wideband active baluns using 0.18-μm CMOS technology. The mixer employs a folded cascode Gilbert cell topology and on-chip broadband active baluns. The broadband active balun is used to generate wideband differential signals, together with the derivation of a closed-form expression for the phase imbalance. This single-ended wideband high-linearity mixer has the conversion gain of 6.9 ± 1.5 dB, IP_{1dB} of −3.5 dBm, and IIP_3 of 6.5 dBm under the power consumption of 25.7 mW from a 1.8 V power supply. The chip area is 0.85 × 0.57 mm^2.

Secondly, an UWB CMOS frequency synthesizer architecture is proposed and to be realized by TSMC 0.18-μm process technology. It can produce 14 bands for multi-band orthogonal frequency division multiplexing (MB-OFDM) system with characteristics of low power consumption and short switching time. The proposed architecture is composed of two PLLs, one divide-by-7 divider, and one SSB quadrature mixer. The simulation result shows that the synthesizer produces the full 14 bands with output frequencies ranging from 3.432 GHz to 10.296 GHz, and is with less than 2 ns hopping time, less than −25 dBc spurious, and 111 mW power consumption from a 1.3 V power supply. The total area including pads is 2.29 × 2.51 mm^2.

Thirdly, an LC-tank voltage-controlled oscillator (VCO) with temperature compensation active inductors using 0.18-μm 1P6M CMOS technology is demonstrated. A cascode-grounded active inductor circuit topology with the PTAT current sources was adopted, which is used to improve the temperature effect on the inductance of the active inductor. The measured variation of the oscillating frequency is within 0.99 % while the temperature varies from –20 to +60°C. The measured phase noise is –91 dBc/Hz at 1MHz offset when the oscillating frequency is at 2.4 GHz. The proposed circuit provides an oscillating frequency from 1.7 GHz to 2.8 GHz, exhibiting a 48% tunable frequency ranges. The active LC-tank VCO occupies a small active area of 190 × 195 μm^2 due to the absence of passive inductors.

Finally, a divide-by-3 SDFD with active balun is presented using the current-reused technique. The proposed SDFD is composed of a Gilbert cell mixer, one stage of static divider, and an active balun. The local oscillator (LO) switching stage of Gilbert cell mixer is also the current sources of the static frequency divider to construct the current-reused architecture. At the incident power of 0 dBm, this frequency divider operates the maximum bandwidth of 1080 MHz from 21.48 to 22.56 GHz. The power consumption of the divider core fabricated in TSMC 0.18-μm CMOS process is 12 mW from 1.5 V supply.

誌謝

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CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The wireless communication is becoming more and more significant because of the convenience for human-being life and accelerating the transmission of the information in the last two decades. The landscape of the wireless communication systems is shown in Fig. 1.1, the higher bandwidth of these radio bands, such as global system for mobile (GSM), general packet radio service (GPRS), wideband code division multiple access (W-CDMA), wireless local area network (WLAN), ultra-wideband (UWB) significantly enables the higher data rate applications. The growing request for high data rate promotes the development of UWB system. Examples of possible applications include wireless USB 3.0 and high-definition multimedia interface (HDMI) for high-definition television (HDTV) video stream. The Federal Communications Commission (FCC) groups of IEEE 802.15.3a and IEEE 802.15.3c are both working toward the standard development of the UWB wireless communication systems.

For the IEEE 802.15.3a group, the multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB system uses the unlicensed UWB spectrum from 3.1 GHz to 10.6 GHz with a regulated frequency-power emission below –41.3 dBm to provide data communication capabilities up to 480 Mbps. The 7.5 GHz bandwidth is divided into 4 groups of 14 bands in total as shown in Fig. 1.2. Therefore, the occupied spectrum for each OFDM signal is 528 MHz. The UWB system adopted frequency hopping approach to reduce degradation caused by narrowband interferers.

An example can be found in Fig. 1.3. The figure shows that each OFDM symbol is transmitted in the order of band #1, band #2, and band #3 with a setting time within 9.47 ns.

On the other hand, IEEE 802.15.3c group established the standard for the unlicensed band from 57 to 66 GHz with the data communication capabilities up to multi-Gbps. As shown in Fig. 1.4, the available unlicensed frequency bands around the world are 57.05–64 GHz in USA, 59.4–62.9 GHz in Australia, 57–66 GHz in Europe, and 59–66 GHz in Japan, etc. The 60-GHz band UWB system has fewer interference and higher transmission power than the UWB system at 3.1–10.6 GHz band with almost the same amount of spectrum.

In this thesis, the main research focus is on key components for UWB communication systems. It includes wideband down conversion mixers, a full-band frequency synthesizer, a proportional to absolute temperature (PTAT) active inductor based voltage-controlled oscillator (VCO), and divide-by-3 frequency divider. The research motivation will be depicted in the following subsection.

1.2 RESEARCH MOTIVATION

Motivated by the issues arise from the increasing demand for data communication capabilities, the study on exploring new different circuit topologies and design techniques of the key RFIC components in UWB communication systems is proposed.

Mixer is responsible for frequency conversion in RF transceiver, and the nonlinearity will cause many problems such as cross modulation, desensitization, harmonic generation, and gain compression. The differential architecture can be used

to reduce the even-order nonlinearity, but it is difficult to suppress the odd-order nonlinearity. In order to analyze the nonlinear effects, the harmonic balance analysis started from the derivation of the output current of the transconductor stage.

The frequency synthesizer is utilized to be the local oscillator (LO) of the UWB transceiver. As to the frequency plan for UWB system, the IEEE 802.15.3a group proposed the MB-OFDM based UWB system separating the whole 7.5 GHz bandwidth (from 3.1 GHz to 10.6 GHz) into 14 sub-bands, each with 528 MHz bandwidth. And the guard interval duration should be less than 9.47 ns for fast frequency hopping. The new UWB frequency synthesizer, which can generate full bands with a fast switching time, is designed.

However, in order to cancel the temperature effects on the active devices and decrease the area consumption of the synthesizer, the active inductor based VCO with temperature compensation is proposed. The lower resonant frequency of the oscillator often gets better phase noise. Therefore, the proposed VCO can be applied in the synthesizer after the multiplier.

With the growing request for the high data communication capabilities, the 60 GHz UWB system is developed for new consumer applications. The frequency divider is a key component of the phase locked loop (PLL) and frequency synthesizer. The divide-by-3 frequency divider is proposed to make the PLL architecture more compact.

The aim of this dissertation is to develop key components for UWB communication systems including wideband down conversion mixer, a PTAT VCO, a UWB frequency synthesizer, and a divide-by-3 frequency divider. The main results will be depicted below.

1.3 THESIS ORGANIZATION

It is the aim of this thesis to analyze and design key RFICs for UWB applications. The thesis includes the design and analysis of the wideband down conversion mixer, the design of full-band synthesizer for UWB applications, the design of active inductor based PTAT VCO for UWB synthesizer, and a divide-by-3 frequency divider for 60-GHz PLL.

Chapter 1 introduces the background, and describes the research motivation.

Chapter 2 begins with the analysis on feedforward compensated differential transconductor of the wideband mixer. The odd-order harmonics are the dominant parts of the nonlinearity for differential architecture. The third-order distortion can be eliminated by designing the resistors and the transconductance parameters of the transconductor properly. A closed form of phase imbalance for the wideband active balun is given with small signal analysis.

In chapter 3, a frequency synthesizer with the semi-dynamic frequency divider (SDFD) for UWB communication system is proposed and designed. The synthesizer consists of: 1) two PLLs for frequency generation; 2) an SDFD to generate necessary frequencies for mixer; and 3) wideband single-side band (SSB) mixer with capacitor switches. The proposed SDFD circuit is introduced to divide the frequency by seven and co-designed with the PLL as a prescaler.

In chapter 4, an LC-tank VCO with temperature compensation active inductors in TSMC 0.18-μm CMOS technology is presented. The adopted active inductors are composed of MOSFETs in CMOS technology. The threshold voltage V_{THN} and mobility μ_n of these MOSFETs will be affected by the temperature variation, which in turn results in the inductance variation of the active inductors with temperature. The

active inductor with temperature compensation current source is proposed in this chapter to solve the problems.

In chapter 5, a current-reused divide-by-3 SDFD with active balun is presented. The divide-by-3 frequency divider can be used to simplify the PLL design with more flexibility. Current-reused technique has advantages of less DC power consumption and compact structure for the designed circuit. This technique is realized by taking the LO switching stage of Gilbert cell mixer as the current sources of static frequency divider.

In chapter 6, conclusions and future work are given.

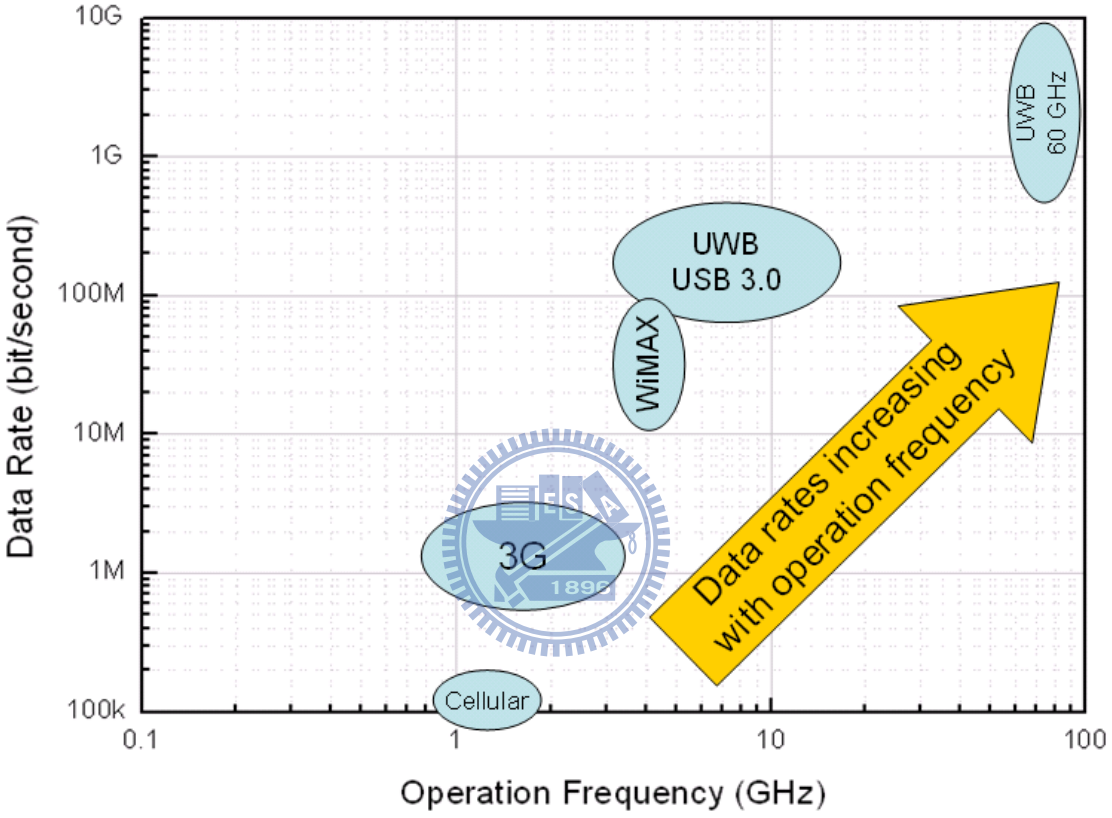


Fig. 1.1 The landscape of wireless communication systems.

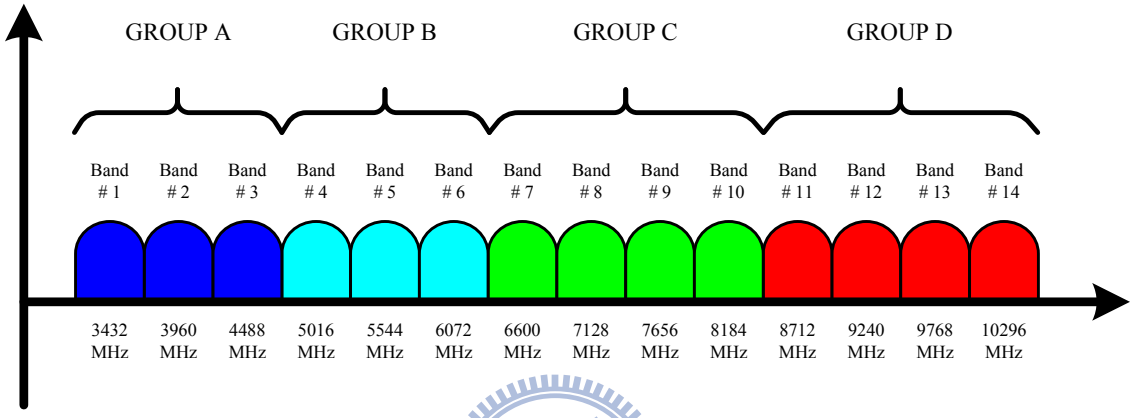


Fig. 1.2 The band group plans of the MB-OFDM UWB system (3.1 GHz ~ 10.6 GHz).

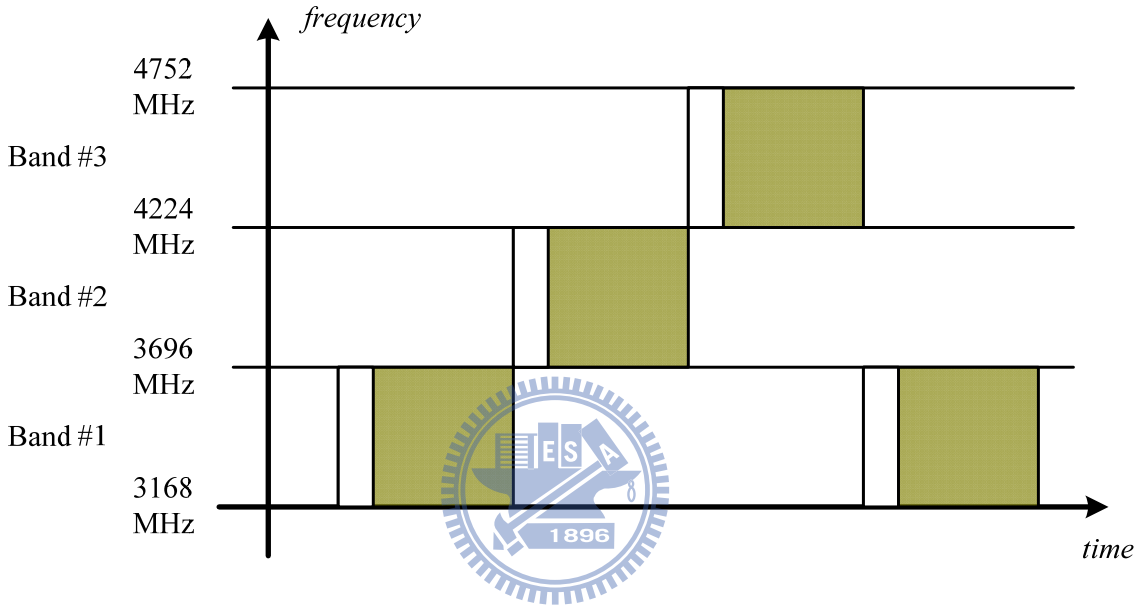


Fig. 1.3 The example of band transmission in band group A.

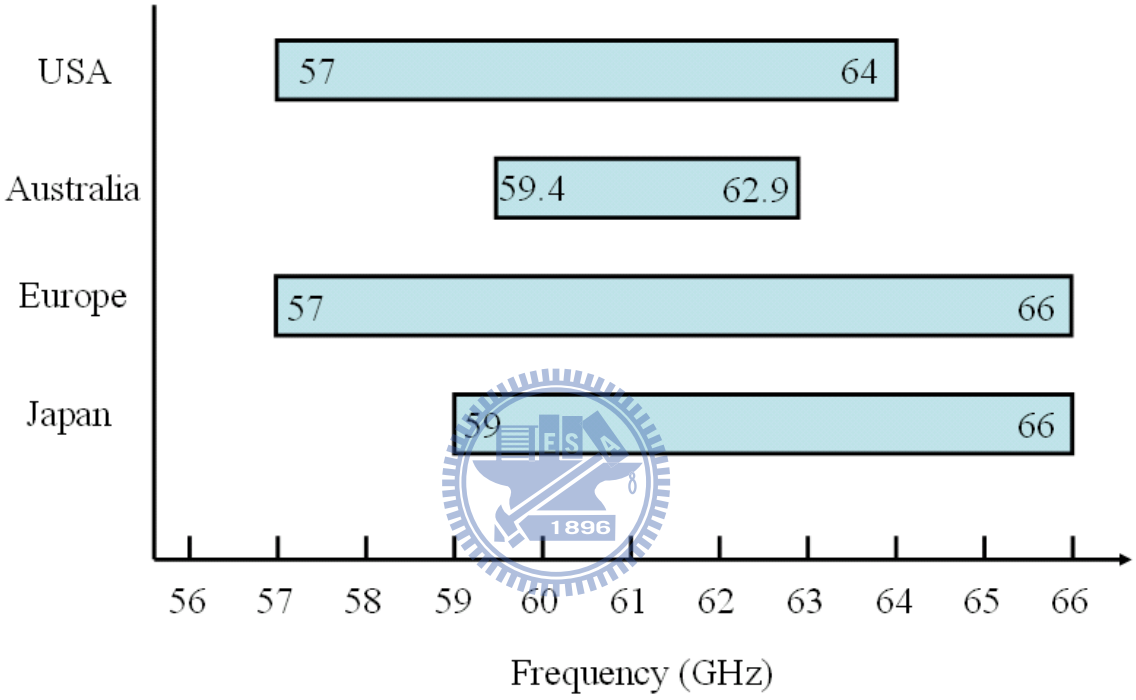


Fig. 1.4 The unlicensed bandwidth for 60–GHz UWB system.

CHAPTER 2

DESIGN OF THE WIDEBAND DOWN CONVERSION MIXER

It is the aim of this chapter to introduce new wideband down conversion mixers. The mixer, which is responsible for frequency conversion, is an essential building block of transceivers. It is also an important component associated with the linearity of the front-end receivers. Direct conversion and low-IF wireless receiver architectures have attracted more attention in the past few years due to simplicity, easy integration with baseband, low power and potential low manufacturing costs [1]-[5]. However, LO leakage, DC offsets, and flick noise are the critical design issues of the direct conversion and low-IF receivers, which need not be considered in heterodyne receiver. Fig. 2.1 shows the conventional heterodyne conversion receiver architecture. The first stage of mixer must have high linearity to handle the large input signals from LNA without significant intermodulation [6].

Nonlinearity will cause many problems, such as cross modulation, desensitization, harmonic generation, and gain compression [7]. The differential architecture can be used to reduce the even-order nonlinearity, but it is difficult to suppress the odd-order one, especially for the third-order intermodulation distortion (IMD3), which is the dominant part of the odd-order nonlinearity.

Gilbert cell is a typical type of active mixers. The Gilbert mixer consists of three stages: transconductor stage, switching stage, and load stage. The linearity of Gilbert mixer will be dominated by the transconductor stage if the switching stage is ideal.

In order to get higher conversion gain, good isolation, and better dynamic and static offsets, and help improve the second and third order intermodulation rejection,

the double balanced Gilbert mixer with differential RF, LO, and IF signals are commonly used for optimum operation [8]–[9].

In Section 2.1, the nonlinearity cancellation of third-order distortion is derived. The wideband down conversion mixer with active balun is described in Section 2.2. Finally, the summary is given in Section 2.3. And this work has been published in [10] and [11].

2.1 WIDEBAND DOWN CONVERSION MIXER

2.1.1 Analysis on Feedforward Compensated Differential Transconductor

Comparing passive mixers and active mixers, active mixers have better gain and isolation, but worse linearity. Passive mixers have superior linearity than active mixers. Third-order input intercept point (IIP_3), second-order input intercept point (IIP_2), and input 1-dB compression point (IP_{1dB}) are the principal parameters of linearity. IIP_3 and IIP_2 are the effects of intermodulation terms in nonlinear circuits, and IP_{1dB} is the ceiling of the input power. In order to improve the linearity of Gilbert mixer, many methods have been used, such as adding source degeneration resistors below the gain stage [12], using bisymmetric Class-AB input stage [6] and multiple gated transistor [7], and employing common-source and common-emitter RF transconductors [13].

The feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The transconductor, as shown in Fig. 2.2, consists of two degenerate common-source transistors ($M1$, $M3$) and two degenerate common-gate transistors ($M2$, $M4$), which is used to be the input stage and achieve feed-forward distortion linearization [14]. This feedforward

compensated differential transconductor has the function of providing accurate input impedance and high intermodulation intercepts, and has less distortion than Class-AB [15], multi-tanh [16], degenerated differential pair, and cascode compensation [17]. R_1 and R_2, as will be described below, are used for suppressing the excited harmonics, and thus the nonlinearity, in the circuit. R_2 also serves for input matching purpose. Without input matching active baluns, a wideband mixer with feedforward compensated differential transconductor in CMOS 0.18-μm technology was previously presented by the authors [13]. Although good linearity was achieved, neither theoretical study nor design formula was given there.

In order to analyze the nonlinear effects generated by the transconductor stage, the harmonic balance analysis started from the derivation of the output current. The output currents, I_{out1} and I_{out2}, of the differential transconductor stage characterize a nonlinear relationship with the input voltages $V_{in1} = V_{dc} + V_m \cos\omega t$ and $V_{in2} = V_{dc} - V_m \cos\omega t$, where V_{dc} is the DC bias voltage of the input signals. The differential output current I_{od} can be written as

$$I_{od} = I_{out1} - I_{out2} = (I_1 + I_2) - (I_3 + I_4) \tag{2.1}$$

where I_1 to I_4 are the currents for transistors M_1 to M_4. In this study, the third-order harmonic distortion canceling technique is adopted for achieving high linearity. To this end, the cancellation criterion for wideband applications is first derived based on the harmonic balance analysis.

Assume that all the FETs in Fig. 2.2 are operated in saturation region with channel length modulation parameter $\lambda = 0$. The currents I_1 and I_2 can be expressed as

$$I_1 = \frac{1}{2} K_1 \left[V_{dc} - V_m \cos \omega t - \left(I_1 R_1 + V_x \right) - V_{TH} \right]^2 \tag{2.2}$$

and

$$I_2 = \frac{1}{2} K_2 \left[V_b - \left(I_2 R_2 + V_{dc} + V_m \cos \omega t \right) - V_{TH} \right]^2 \tag{2.3}$$

where V_{TH} and V_b are the threshold voltage and bias voltage, respectively. And the transconductance parameter K (= K_1 or K_2) is given as

$$K = \mu_n C_{ox} \frac{W}{L} \tag{2.4}$$

Reforming (2.2) and (2.3), one obtains

$$\begin{aligned} I_1 = & \left(\frac{2}{R_1^2 K_1} - \frac{K_1 {V_{P1}}^2}{2} + \frac{1}{2} R_1 K_1^2 {V_{P1}}^3 + \frac{2V_{P1}}{R_1} - \frac{1}{4} K_1 V_m^2 + \frac{3}{4} R_1 K_1^2 V_{P1} V_m^2 \right) \\ & + \left(-\frac{3}{2} R_1 K_1^2 {V_{P1}}^2 V_m - \frac{3}{8} R_1 K_1^2 V_m^3 + K_1 V_m V_{P1} - \frac{2V_m}{R_1} \right) \cos \omega t \\ & + \left(-\frac{1}{4} K_1 V_m^2 + \frac{3}{4} R_1 K_1^2 V_{P1} V_m^2 \right) \cos 2\omega t - \frac{1}{8} R_1 K_1^2 V_m^3 \cos 3\omega t \ . \end{aligned} \tag{2.5}$$

and

$$\begin{aligned} I_2 = & \left(\frac{K_2 V_{P2}^2}{2} - \frac{1}{2} R_2 K_2^2 V_{P2}^3 + \frac{1}{4} K_2 V_m^2 - \frac{3}{4} R_2 K_2^2 V_{P2} V_m^2 \right) \\ & + \left(\frac{3}{2} R_2 K_2^2 V_m V_{P2}^2 + \frac{3}{8} R_2 K_2^2 V_m^3 - K_2 V_m V_{P2} \right) \cos \omega t \\ & + \left(\frac{1}{4} K_2 V_m^2 - \frac{3}{4} R_2 K_2^2 V_{P2} V_m^2 \right) \cos 2\omega t + \frac{1}{8} R_2 K_2^2 V_m^3 \cos 3\omega t \ . \end{aligned} \tag{2.6}$$

where $V_{P1} = V_{dc} - V_{TH} - V_x$ and $V_{P2} = V_b - V_{TH} - V_{dc}$.

Similarly, the currents I_3 and I_4 for $M3$ and $M4$, respectively, can be derived as

$$\begin{aligned} I_3 = & \left(\frac{2}{R_1^2 K_1} - \frac{K_1 V_{P1}^{\ 2}}{2} + \frac{1}{2} R_1 K_1^2 V_{P1}^3 + \frac{2V_{P1}}{R_1} - \frac{1}{4} K_1 V_m^2 + \frac{3}{4} R_1 K_1^2 V_{P1} V_m^2 \right) \\ & - \left(-\frac{3}{2} R_1 K_1^2 V_{P1}^{\ 2} V_m - \frac{3}{8} R_1 K_1^2 V_m^3 + K_1 V_{P1} V_m - \frac{2V_m}{R_1} \right) \cos \omega t \\ & + \left(-\frac{1}{4} K_1 V_m^2 + \frac{3}{4} R_1 K_1^2 V_{P1} V_m^2 \right) \cos 2\omega t + \frac{1}{8} R_1 K_1^2 V_m^3 \cos 3\omega t \quad . \end{aligned} \tag{2.7}$$

and

$$\begin{aligned} I_4 = & \left(\frac{K_2 V_{P2}^2}{2} - \frac{1}{2} R_2 K_2^2 V_{P2}^3 + \frac{1}{4} K_2 V_m^2 - \frac{3}{4} R_2 K_2^2 V_{P2} V_m^2 \right) \\ & - \left(\frac{3}{2} R_2 K_2^2 V_m V_{P2}^2 + \frac{3}{8} R_2 K_2^2 V_m^3 - K_2 V_m V_{P2} \right) \cos \omega t \\ & + \left(\frac{1}{4} K_2 V_m^2 - \frac{3}{4} R_2 K_2^2 V_{P2} V_m^2 \right) \cos 2\omega t - \frac{1}{8} R_2 K_2^2 V_m^3 \cos 3\omega t \quad . \end{aligned} \tag{2.8}$$

Substituting (2.5)–(2.8) into (2.1), the differential output current I_{od} turns out to be

$$\begin{aligned} I_{od} &= I_{out1} - I_{out2} = (I_1 + I_2) - (I_3 + I_4) \\ &= A_F \cos \omega t + A_{HD3} \cos 3\omega t. \end{aligned} \tag{2.9}$$

where A_F and A_{HD3} represent the amplitudes of the fundamental and third-order harmonics, respectively. A_F and A_{HD3} can be found as

$$A_F = \frac{V_m}{4} \left[\begin{array}{l} 8(K_1 V_{P1} - K_2 V_{P2}) + 3V_m^2 (-R_1 K_1^2 + R_2 K_2^2) \\ +12 \left(-R_1 K_1^2 V_{P1}^{\ 2} + R_2 K_2^2 V_{P2}^{\ 2} \right) - \dfrac{16}{R_1} \end{array} \right] \tag{2.10}$$

and

$$A_{HD3} = \frac{V_m^3}{4}\left(-R_1K_1^2 + R_2K_2^2\right) \tag{2.11}$$

The even order harmonic distortion is canceled due to the differential architecture. The third-order distortion is the dominant part of the nonlinearity, and it may induce problems like intermodulation, cross-modulation, desensitization, and gain compression. All these higher-order distortion deteriorate the circuit linearity. The DC and second-order harmonics in (2.5)–(2.8) are canceled due to the differential architecture. It is seen from (2.11) that, the amplitudes of the third-order harmonic, A_{HD3}, becomes null if it follows that

$$R_1K_1^2 = R_2K_2^2 \tag{2.12}$$

This means that the third-order distortion, which is the dominant part of the nonlinearity, can be eliminated if one designs the resistances R_1, R_2 and the transconductance parameters K_1, K_2 properly according to (2.12). The formula is proposed to provide design guidance for obtaining better linearity by canceling the third-order distortion. Based on the above criteria, the third-order harmonic of the differential output current becomes null. And the fundamental amplitude can be rewritten as follow

$$A_F = \frac{V_m}{4}\left[8\left(K_1V_{P1} - K_2V_{P2}\right) + 12\left(-R_1K_1^2{V_{P1}}^2 + R_2K_2^2{V_{P2}}^2\right) - \frac{16}{R_1}\right] \tag{2.13}$$

The formula (2.13) shows that the fundamental amplitude will enlarge when the resistor R_2 increases. However, with the unchanged transconductor parameter K, the

formula (2.12) indicates that R_1 should be increased at the same time to meet the criteria if R_2 is increased. Meanwhile, the formula (2.13) shows that the increased R_1 will lessen the fundamental amplitude due to the term $(-R_1K_1^2V_{P1}^2)$ though the term $(-16/R_1)$ is enlarged. The method of increasing mixer gain at the same IP_3 point is to find out the maximum R_2 under the consideration of R_1 in formula (2.13). Hence, in an attempt to find out the maximum mixer gain, R_1 and R_2 should be well chosen and trade-off.

2.1.2 RLC Folded Cascode Stage

The mixer gain is proportional to the transconductance g_m, and higher overdrive voltage will get higher gain. Furthermore, the level of the supply voltage for the feedforward compensated differential transconductor is critical to keep the driver FETs always operated in the saturation region. To overcome this problem, the RLC folded cascode circuit is used as the load to get larger output voltage headroom [7], [12], [18], [19]. Since the inductor is short-circuited at DC operation, this modified LC folded load can still provide more voltage headroom for the output signal. An LC folded cascode mixer with an added resistance is shown in Fig. 2.3. The addition of the resistance in the LC tank helps to reduce the quality factor and thus increase the bandwidth of the mixer.

In function, the differential signal get into the feedforward compensated differential transconductor for amplification first. The small-signal voltage is converted to a small-signal current at this stage. Then, the current signal is down-converted by the switching pair. Finally, the RLC tank provides loading to the preceding stages and converts the current signals back to the voltage signals.

2.1.3 Circuit Design

Fig. 2.4 shows the proposed mixer, which is composed of an LC folded cascode mixer and a feedforward compensated differential transconductor. Functionally, the input differential signal fed into the feed-forward compensated differential transconductor to amplify the input signal firstly. The small-signal voltage is converted to a small-signal current at this stage. The current signal is down-converted by the switching pair. Then the load stage provides loading to preceding stages and converts the current signals back to voltage signals. Finally, common sources are used as output buffers for testing and matching purposes.

2.1.4 Simulation and Experimental Results

In this section, we show the measurement setups and results of the proposed mixer. The measurements were performed with the chip directly mounted on a 28 × 28 mm^2 and thickness of 20 mil RO4003 microwave substrate with SMA connectors. Fig. 2.5 shows the test board with die mounted on it. The chip microphotograph is shown in Fig. 2.6. The die size is 0.7 × 0.58 mm^2 including pads. The connectors and lines both result in loss in measurement.

The mixer is designed using TSMC 0.18-μm CMOS technology. All measurements were done at 1.8 V and 1.2 V supply voltage and the power consumption is 14.4 mW including the output buffer. Fig. 2.7 illustrates the conversion gain versus the RF frequency with both RF and LO ports swept in frequency from 2 to 12 GHz, a fixed IF frequency of 50 MHz, RF power of −30 dBm, and LO power of −5 dBm. The conversion gain is 3.3 ± 1.5dB with a bandwidth of 2.4 to 10.7 GHz, The measured RF and IF return loss is better than 10 dB as shown in

Fig. 2.8. The measured RF–to–IF, LO–to–IF and RF–to–LO isolation shown in Fig. 2.9 are better than 20 dB. Fig. 2.10 shows the linearity of the mixer as a function of frequency. The measured IIP_3 is from 4 to 6.9 dBm and IP_{1dB} is from −2.8 to −5.8 dBm in the bandwidth of 2.4 to 10.7 GHz.

Finally, the comparison of the proposed mixer against recently reported CMOS mixer is shown in Table 2.1 named as Mixer1, it indicates that the proposed mixer provides better linearity, more compact chip size, and acceptable conversion gain and power consumption.

2.2 WIDEBAND DOWN CONVERSION MIXER WITH ACTIVE BALUN

In this section, we proposed a high linearity down conversion mixer with wideband active baluns, by using the standard 0.18-μm CMOS process. Detailed design information is presented. The adopted cascode CG and CS active balun is improved from the common-gate cascaded with common-source structure for better performance at high frequency and wideband applications. A closed form of phase imbalance for the wideband active balun is given with small signal analysis. Furthermore, the experimented results of the fabricated chip designed on the basis of the circuit simulations are presented and compared to other wideband mixers using the similar technology.

2.2.1 Wideband Active Balun

2.2.1.1 Fundamental of Active Balun

Differential balun (or phase splitter) circuits play an important role in generating differential output signals which characterize balanced amplitude and phase. Here are two distinct types of baluns, i.e., passive and active baluns. In general, the passive baluns have the advantage of consuming no DC power. And they are often implemented in the forms of LC networks or microstrip line transformers. The LC network baluns can be used in narrow band and the microstrip line transformers in wideband applications. However, both of them are lossy and expansive for larger physical size at frequencies below X-band, which limit the practicability of the passive baluns in monolithic microwave integrated circuit (MMIC) designs. Oppositely, the active baluns have the characteristics of more acceptable gain imbalance and phase imbalance in a wideband range. Also, the compact size makes the active baluns more suitable than passive baluns in integrated circuit designs.

Several types of active balun topologies have been proposed in the literature. Three configurations are commonly used: single FET circuits, common-gate cascaded with common-source (CGCS) circuits, and differential amplifier circuits. The challenge of the active balun design is to maintain an 180^{o} phase difference and limit gain imbalance between the two output ports in a wide frequency range. The common-source single–FET type is the simplest configuration of active baluns as shown in Fig. 2.11. When signals enter the gate, ideally the output signals at the drain and source will be out of phase by 180 degrees and have equal amplitude. However, the parasitic capacitance of the FET makes the common-source FET difficult to achieve the required phase difference for wideband and high frequency application. Examples can be found in [20] and [21], with operation frequency lower than 2 GHz.

As for the second configuration, the CGCS circuit as shown in Fig. 2.12, its characteristics are low power consumption and adequate isolation. However it does not have low phase error performance in broadband applications due to the parasitic effects. An active phase splitter proposed in [22] adopted the common base/common emitter structure using the InGaP HBT foundry process, which exhibited a maximum amplitude error and a phase error up to 1.3 dB and 8 °, respectively, at the personal communication system (PCS) frequency band (1850–1910 MHz).

For the third configuration, the differential amplifier balun circuit as shown in Fig. 2.13, the output signals are usually poor in equal amplitude and out–of–phase since the current source becomes an imperfect open circuit at the high frequency. The leakage signal to the current source will cause the phase and gain imbalances. Also the over driven voltage of the differential amplifier will decrease the headroom of the output signals. Viallon and the coworkers [23] utilized this configuration to implement an active balun with a very wide frequency range from 0.2 to 22 GHz. The drawback of their design is the large power consumption up to 166 mW.

2.2.1.2 Design of Broadband Active Balun

In this subsection, the adopted cascode CG and CS active balun is analyzed and compared to the conventional CGCS one. As shown in Fig. 2.12, a conventional CGCS balun consists of common-gate and common-source stages, whose advantages are low power consumption and adequate isolation. However, it gets too much phase error for broadband application.

To meet the bandwidth requirement in this study, the active balun as illustrated in Fig. 2.14 is used, which is modified from the CGCS circuit by replacing the CG

stage into a cascode CG stage to improve the phase error of differential output. The resistance R_{in} is utilized for input matching to save the die area.

To demonstrate the superiority of the cascode CG and CS structure in wideband phase balance, the transmission phase $\angle S_{21}|_{CGCG}$ (i.e., the phase of V_{out} /V_{in}) of the cascode CG structure is derived by using the small-signal equivalent circuit shown in Fig. 2.15. The transmission phases $\angle S_{21}|_{CS}$ and $\angle S_{21}|_{CG}$ for the conventional CS and CG stages are then derived from the corresponding small-signal circuits [24]. The results are shown in (2.14), (2.15), and (2.16), respectively.

$$\angle S_{21}\big|_{CS} = \tan^{-1}\left\{\frac{\omega\left[C_{gd}(\frac{1}{r_o}+\frac{1}{Z_0})+g_m(C_{gd}+C_{db})\right]-\omega Z_0\left[(1+g_m r_o)C_{gd}+C_{gs}\right]\left[\omega^2 C_{gd}(C_{gd}+C_{db})-g_m(\frac{1}{r_o}+\frac{1}{Z_0})\right]}{\left[\omega^2 C_{gd}(C_{gd}+C_{db})-g_m(\frac{1}{r_o}+\frac{1}{Z_0})\right]+\omega^2 Z_0\left[(1+g_m r_o)C_{gd}+C_{gs}\right]\left[C_{gd}(\frac{1}{r_o}+\frac{1}{Z_0})+g_m(C_{gd}+C_{db})\right]}\right\} \quad (2.14)$$

$$\angle S_{21}\big|_{CG} = \tan^{-1}\left\{\frac{-\omega\left[C_{gs}Z_0(1+\frac{r_o}{Z_0})+r_o(1+g_m Z_0)(C_{gd}+C_{db})\right]}{(1+g_m Z_0)(1+\frac{r_o}{Z_0})-\omega^2 C_{gs}Z_0\left[r_o(C_{gd}+C_{db})\right]}\right\} \quad (2.15)$$

$$\angle S_{21}\big|_{CGCG} = \tan^{-1}\left(\omega\frac{AD-BC}{AC+\omega^2 BD}\right)$$

where

$$A=\left\{1+r_o(1+K)Z_0^{-1}+(1+g_m r_o)K-\omega^2 C_{gs}r_o\left[C_{gs}(Z_0+r_o)+Z_0C_{gd}(2+g_m r_o)\right]\right\}\left(g_m{}^2+\omega^2 C_{gs}{}^2\right)$$

$$B=\left\{\begin{array}{c}(1+g_m r_o)\left[C_{gs}Z_0+Z_0C_{gd}(1+g_m r_o)+C_{gs}r_o\right]+\\ C_{gs}\left[Z_0+r_o(1+K)\right]+r_o\left(C_{gs}+C_{gs}r_oZ_0^{-1}+2C_{gd}+g_m r_oC_{gd}\right)\end{array}\right\}\left(g_m{}^2+\omega^2 C_{gs}{}^2\right) \quad (2.16)$$

$$C=2g_m^3Z_0+2r_og_m^3(1+K)+2\omega^2C_{gs}r_og_m^2\left(2Z_0C_{gd}+Z_0C_{gd}g_m r_o+C_{gs}Z_0+C_{gs}r_o\right)$$

$$D=2g_m^2\left[g_m r_o\left(2Z_0C_{gd}+Z_0C_{gd}g_m r_o+C_{gs}Z_0+C_{gs}r_o\right)-Z_0C_{gs}-r_oC_{gs}(1+K)\right]$$

$$K=1+g_m r_o-\omega^2C_{gs}C_{gd}r_oZ_0$$

From the derived transmission phases, the phase imbalances for the conventional CGCS balun and the cascode CG & CS balun are obtained:

$$\begin{aligned} &\textit{Phase imbalance of conventional CGCS balun} \\ &= \pi - \left| \angle S_{21} \big|_{CS} - \angle S_{21} \big|_{CG} \right| \ , \end{aligned} \tag{2.17}$$

and

$$\begin{aligned} &\textit{Phase imbalance of cascode CG \& CS balun} \\ &= \pi - \left| \angle S_{21} \big|_{CS} - \angle S_{21} \big|_{CGCG} \right| \ . \end{aligned} \tag{2.18}$$

Fig. 2.16 depicts the calculation results for the two circuits. Here the process parameters given by TSMC with 0.18-μm CMOS technology are used (W/L=18.15/0.18, g_m=8.9ms, C_{gs}=18.4fF, C_{gd}=6.02fF, r_o=301.5Ω). It is seen that, in the frequency range from 0 to 13 GHz, the phase imbalance of the conventional CGCS balun is varied between 0° and −10°, while that of the cascode CG & CS balun is between 0° and −2.2°. Obviously, the latter has better performance than the former.

Table 2.2 summaries the performances of reported active baluns and this work. It is seen that the cascode CG and CS active balun in this work has higher upper frequency bound than others except [16]. The balun in [16] adopted the differential amplifier topology and has a wideband range performance from 0.2 GHz to 22 GHz. However, it consumed a very large power which is 92 times of the power used in the present work. The main difference between the cascode CG and CS active balun and conventional one is the cascode common-gate stage. The common source stage characterizes high resistance with the reactance composed of parasitic capacitance C_{gs} and C_{gd} in transmission process. The large resistance and parasitic capacitance will lead to higher RC delay. Therefore, larger phase delay will be generated. As to the

common gate stage, the resistance in transmission process is approximate to $1/g_m$ with the reactance composed of parasitic capacitance of C_{gs}. Hence, its RC delay effect is less than common source stage especially for wide band application. The cascode common gate stage is used to add phase delay to approach the tendency toward the phase variation of the common source stage when frequency varies. The cascode common-gate configuration is adopted to increase the phase delay to attain the bandwidth extension in the less phase error condition.

The simulated gain imbalance and phase imbalance of the cascode CG and CS active balun combined with the mixer core, presented in the previous subsection, are shown in Fig. 2.17. The Agilent Advanced Design System (ADS) simulated data show that in the bandwidth from 2 GHz to 13 GHz, the gain imbalance is less than 2 dB (0.7 dB to 1.9 dB) and the phase imbalance is within $\pm$ 2^{o}.

2.2.2 Design of Wideband Mixer with Active Balun

Fig. 2.18 illustrates the block diagram of the proposed mixer. It includes the mixer core (double balanced mixer), two active baluns (modified CGCS baluns) for RF and LO ports, and an output buffer for IF port. The mixer core uses the LC folded cascode topology with differential transconductor to improve the linearity. And the active baluns adopts the improved common-gate that cascaded with common-source baluns to generate balanced RF and LO signals. The output buffer is a differential common-source amplifier for testing and matching purposes. All input/output ports are single-ended so that the proposed mixer circuit can be directly combined with single-ended front-end and back-end circuits.

The completed circuit schematic of the high linearity mixer is shown in Fig. 2.19 The proposed mixer is based on a Gilbert cell mixer, which is composed of an LO

switching stage ($M5$–$M8$), an RF transconductor stage ($M1$–$M4$), current mirrors, and IF buffer amplifiers.

2.2.3 Simulation and Experimental Results

The proposed cascode Gilbert cell mixer with wideband active baluns was designed and fabricated using the TSMC 0.18-μm CMOS process. The die photo of the proposed circuit is depicted in Fig. 2.20 with a chip size of 0.85 × 0.57 mm^2, where the active region occupies an area of 0.44 × 0.48 mm^2.

The measurements were performed with the chip directly mounted on a 20 mil RO4003 high frequency microwave substrate and tested through SMA connectors, as shown in Fig. 2.21.

The effects of the chip pads, bond wires, and transmission lines in the circuit board are taken into consideration in the simulation process of the whole circuitry. All measurements were done at 1.8 V supply voltage and the total power consumption is 25.7 mW, including that (14.5 mW) consumed by the output buffer. The conversion gain of the proposed mixer was measured for an IF frequency of 50 MHz with both RF and LO ports swept in frequency up to 12 GHz. The RF and LO signal power were set to be −30 dBm and −5 dBm, respectively. The simulated and measured power conversion gain versus the RF frequency is shown in Fig. 2.22. The mixer achieved a conversion gain of better than 4.4 dB over a wideband frequency from 2 GHz to 12 GHz. Also, the conversion gain exhibited a 3−dB variation across the RF frequency of 2 GHz to 11 GHz with an average conversion gain of 6.9 dB and maximum gain of 8.4 dB. The measured return loss for the RF signal is also shown in Fig. 2.22, which illustrates that the proposed mixer possesses a return loss better than 10 dB from 2 GHz to 12 GHz. Although not shown, the measured LO and IF return

losses are also larger than 10 dB. The port to port isolations of the proposed mixer were measured and are presented in Fig. 2.23. The LO–to–RF and RF–to–IF isolations of the mixer are both better than 25 dB, and the LO–to–IF isolation is above 20 dB over the whole measurement frequencies.

The simulated and measured power conversion gain versus RF input power is illustrated in Fig. 2.24 for RF frequency of 8 GHz and LO frequency of 7.95 GHz. The LO power is fixed at −5 dBm.

In Fig. 2.24, it is seen that the RF input 1−dB compression point (IP_{1dB}) of −7 dBm is obtained. Fig. 2.25 depicts the main signal power and third-order inter-modulation power as functions of the RF input power. There are two signals fed to the RF input port for IIP_3 measurement, one at 8GHz and the other at 8.001GHz. The LO signal has a frequency of 7.9505 GHz and power level of −5 dBm. The proposed mixer exhibited an IIP_3 of 3.5 dBm at the RF frequency of 8 GHz.

Finally, the IP_{1dB} and IIP_3 were measured for various RF frequencies ranging from 2 GHz to 12 GHz. The results are shown in Fig. 2.26. In the measurement, the LO power was set as −5 dBm and the IF frequency was fixed at 50 MHz. The measured SSB noise figure is 15.5 dB, and the overall measured results are shown in Fig. 2.27. The proposed mixer works well from 2 to 11 GHz, with maximum IP_{1dB} and IIP_3 of −3.5 dBm and 6.5 dBm, respectively. The proposed mixer is compared with the published Gilbert cell mixers in Table 2.1, and the proposed mixer with active balun is named as Mixer2.

It shows that the proposed mixer provides better linearity, more compact chip size, and acceptable conversion gain and power consumption than other works. The proposed configuration shows the better IIP_3 and IP_{1dB}, and exhibits more compact size than most of the published works.

2.3 SUMMARY

In this chapter, a wideband mixer using LC folded cascode mixer topology and a modified feedforward compensated differential transconductor in TSMC 0.18-μm CMOS technology is presented in the first section. The LC folded cascode method is used to get more voltage headroom, and the feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The linearity is enhanced by a harmonic distortion canceling technique derived from the harmonic balance analysis. The finished mixer core occupies an area of only 0.7×0.58 mm^2 with a consumed power of 14.4 mW.

For the second section, a wideband down conversion mixer with active balun is proposed. The cascode CG and CS active balun structure exhibits a broadband performance, which provides balance signals for mixer core from single input. The finished mixer core and active baluns possess good linearity, wide bandwidth, and occupy an area of only 0.85×0.57 mm^2 with a consumed power of 25.7 mW under 1.8 V supply voltage, which is suitable for application in various wireless communication systems.

Table 2.1

Performance comparison between the present work and other wideband mixers

Reference	Mexer1	Mexer2	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]	[34]
Technology	0.18μm CMOS	0.18μm CMOS	GaAs HBT	GaAs HBT	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.35μm BiCMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	GaAs HBT
Freq. (GHz)	2.4 ~ 10.7	2 ~ 11	DC ~ 9	DC ~ 8	0.3 ~ 25	3.1 ~ 8.7	1~1.6	3.5~14.5	0.2~16	3~7	0.5~7.5	1.5~14
CG (dB)	3.3 ± 1.5	6.9 ± 1.5	10.5 ± 1.5	9.5 ± 1.5	11 ± 1.5	3.75 ± 1.25	5.9	15	>5.3	5.3~8.2	5.7	20
IIP_3 (dBm)	6.9	6.5	2	-7	---	5	4.1	-7	---	-3.2~-0.3	-5.7	-3
IP_{1dB} (dBm)	-2.8	-3.5	-4	-17	-5	---	---	-19	-10 (OP_{1dB})	---	-16	-17
LO Power (dBm)	-5	-5	-8	-2	-1	9	0	6	-2	450 mV_{pp}	5	---
Pdis. (mW)	14.4	25.7	25	---	71	10.4	20.7	60	15	2.5~5.8	0.48	16.32
Supply Voltage (V)	1.8	1.8	5	5	5	1.8	1.8	5	1.8	0.8~1.2	0.77	2.4
Die Area (mm^2)	0.7 × 0.58	0.85 × 0.57	---	---	0.8 × 1	1.4 × 1.16	0.43 × 0.36 (core)	1 × 1	0.68 × 0.65	0.36 × 0.38 (core)	0.86 × 0.72	1 × 1
Balun Type	w/o	Active (Cascode CG & CS)	Active (CBCE)	Active (CBCE)	w/o	w/o	w/o	Passive (Marchand)	w/o	w/o	w/o	Passive (Transformer)

Table 2.2

Comparison of Active Baluns.

Ref.	this work*	[16]	[24]	[35]	[36]	[37]
Frequency (GHz)	2~13	0.2~22	0.5~10	0~8	1.7~5.8	5.1~5.9
Gain imbalance (dB)	2	0.5	0.5	2.7	2	0.02
Phase imbalance	4°	4°	5°	4.2°	2°	0.58°
$P_{dis.}$ (mW)	1.8	166	---	1.44	11.4	9.17

* For the simulation result of this work in Table 2.2, the active balun is connected with the mixer core.

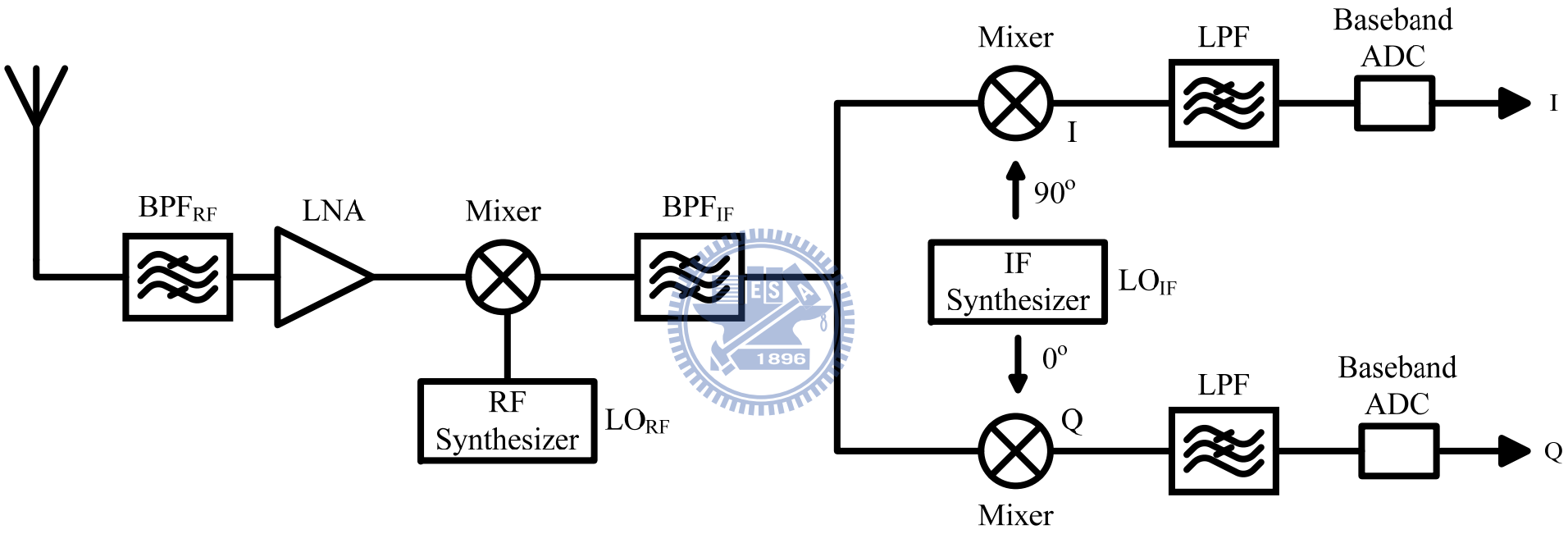


Fig. 2.1 Block diagram of the heterodyne receiver.

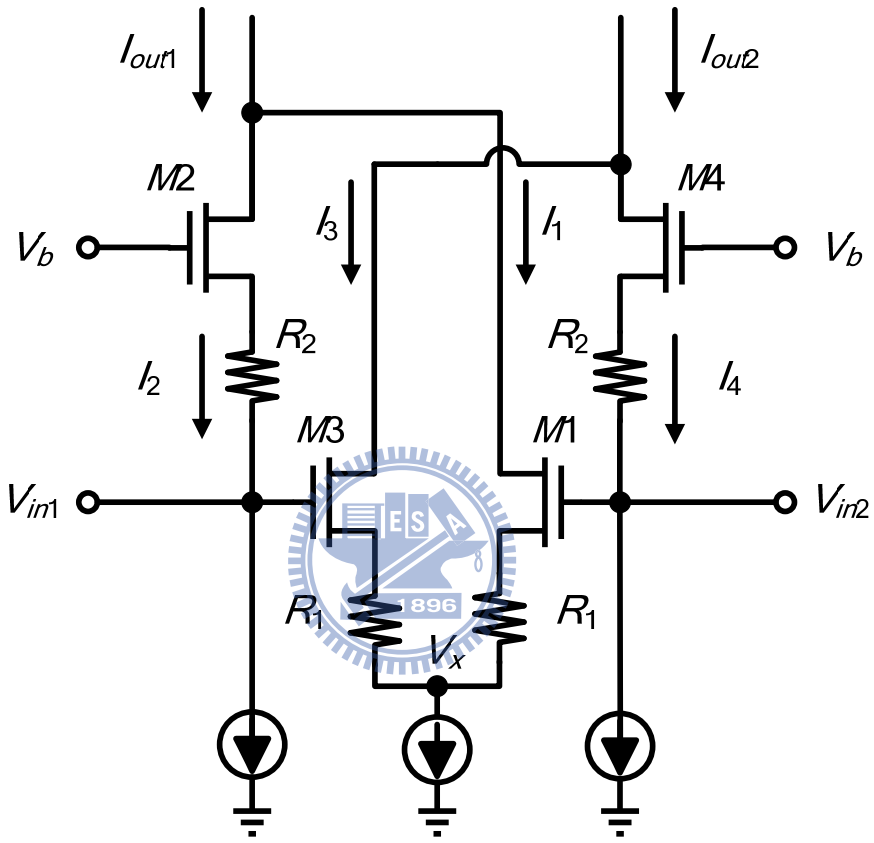


Fig. 2.2 Differential transconductor stage of the proposed mixer.

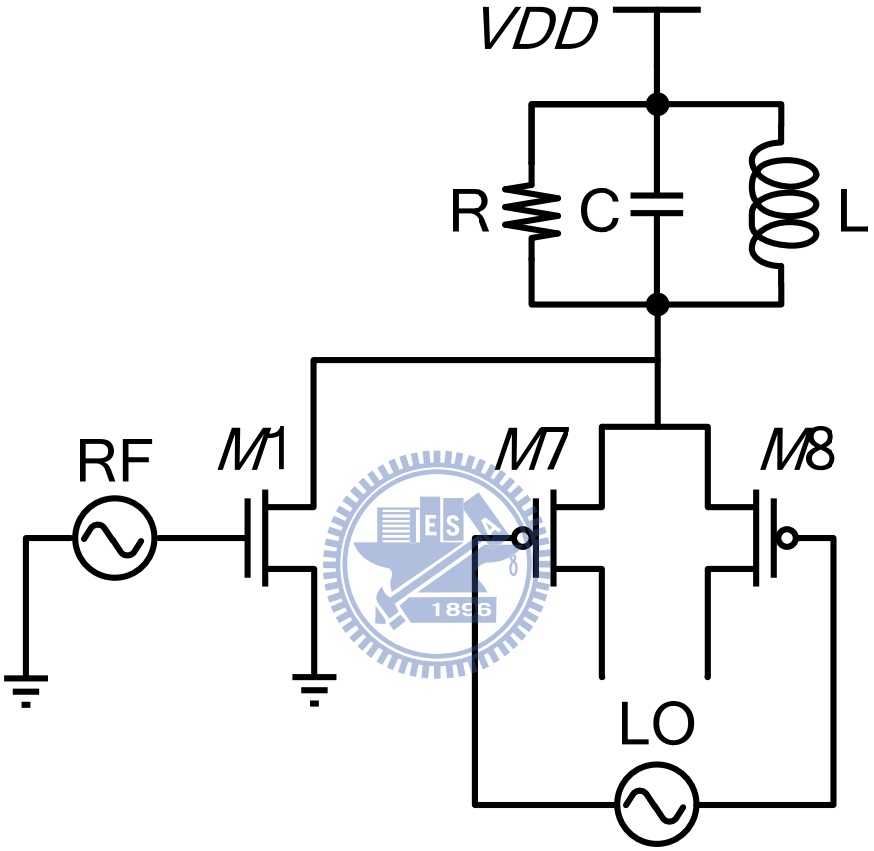


Fig. 2.3 LC folded cascade mixer with an added resistance.

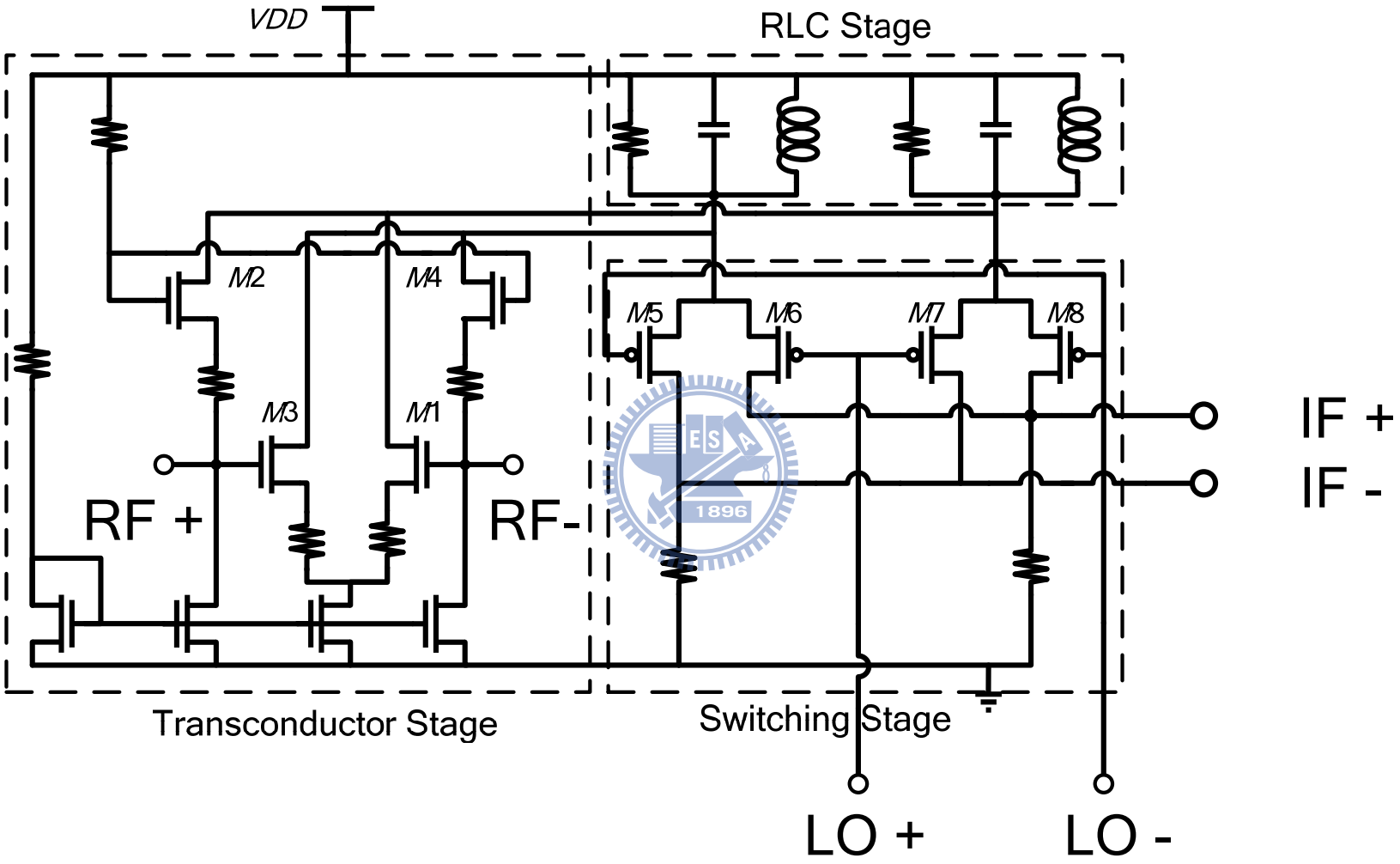


Fig. 2.19 Completed circuit schematic of the proposed mixer with wideband active baluns.

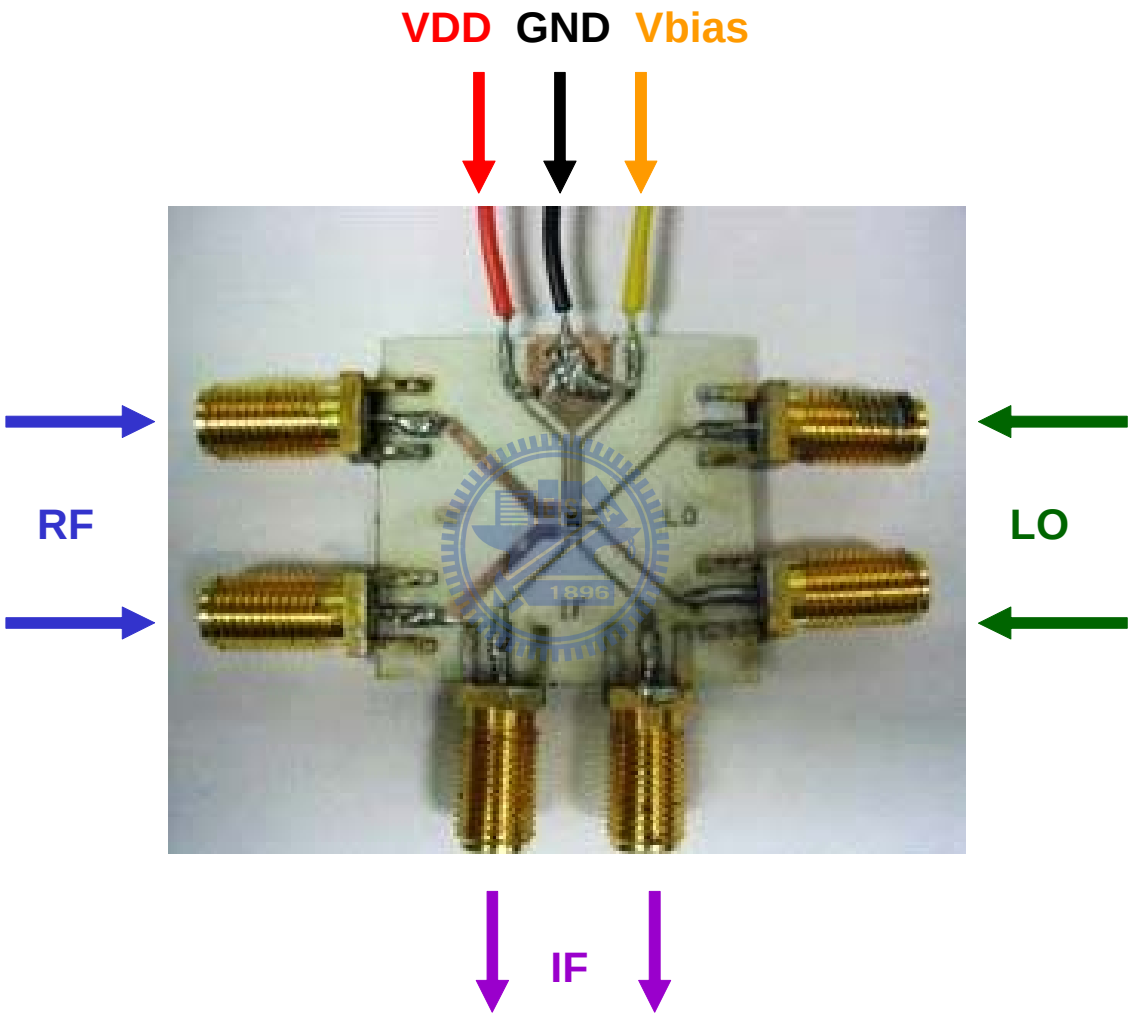


Fig. 2.5 The test board with die mounted on PCB.

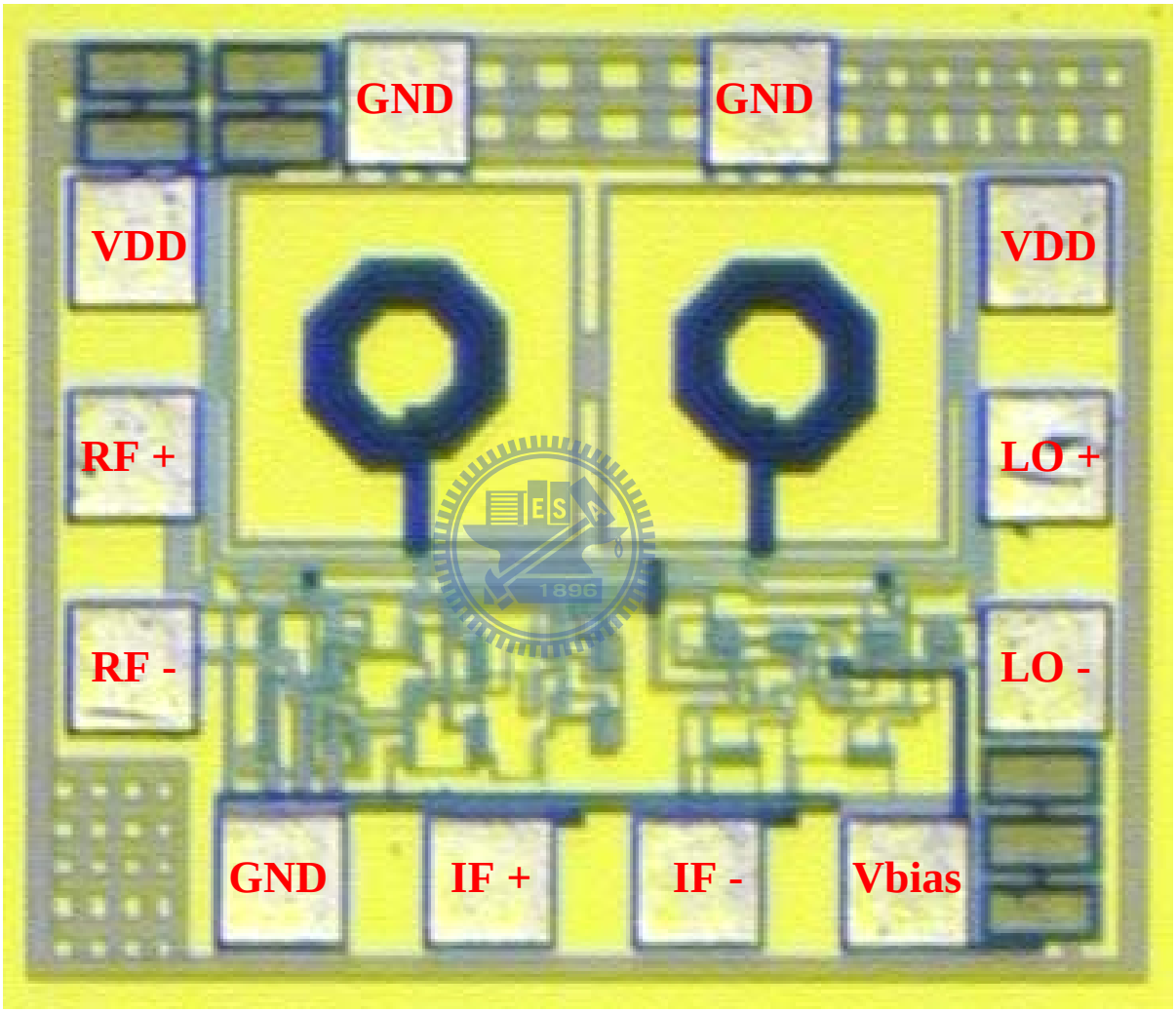


Fig. 2.6 Microphotograph of the proposed mixer (0.7×0.58 mm^2).

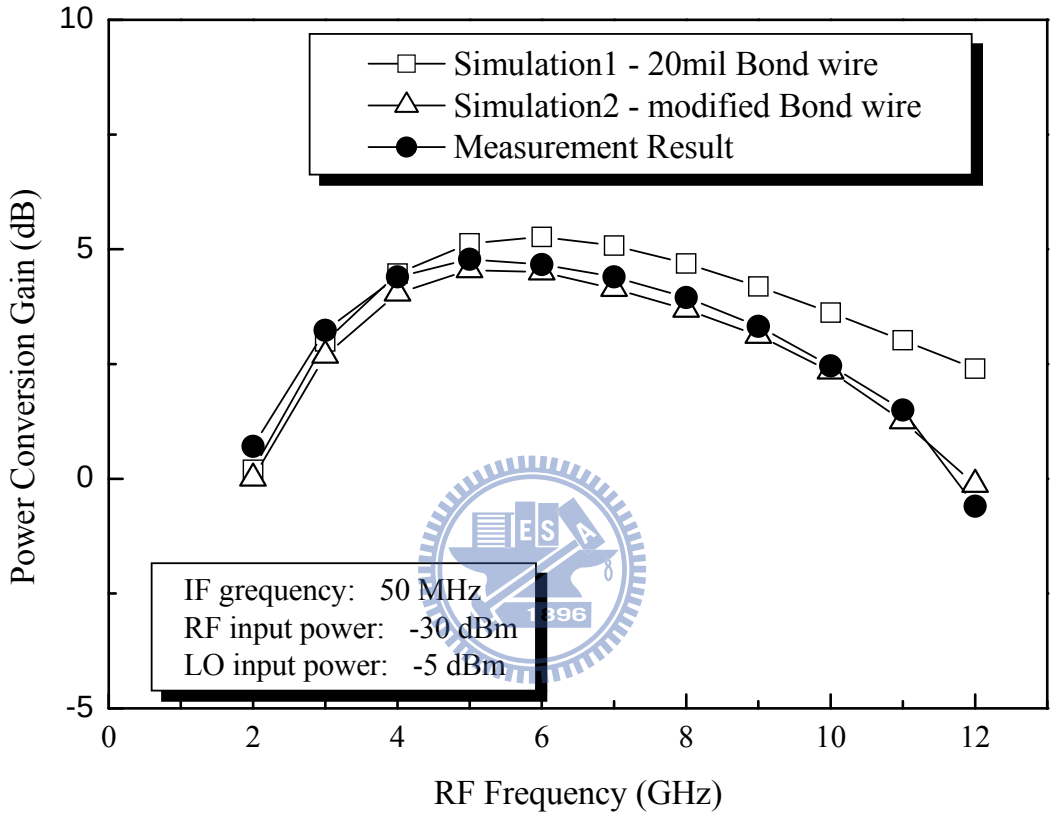
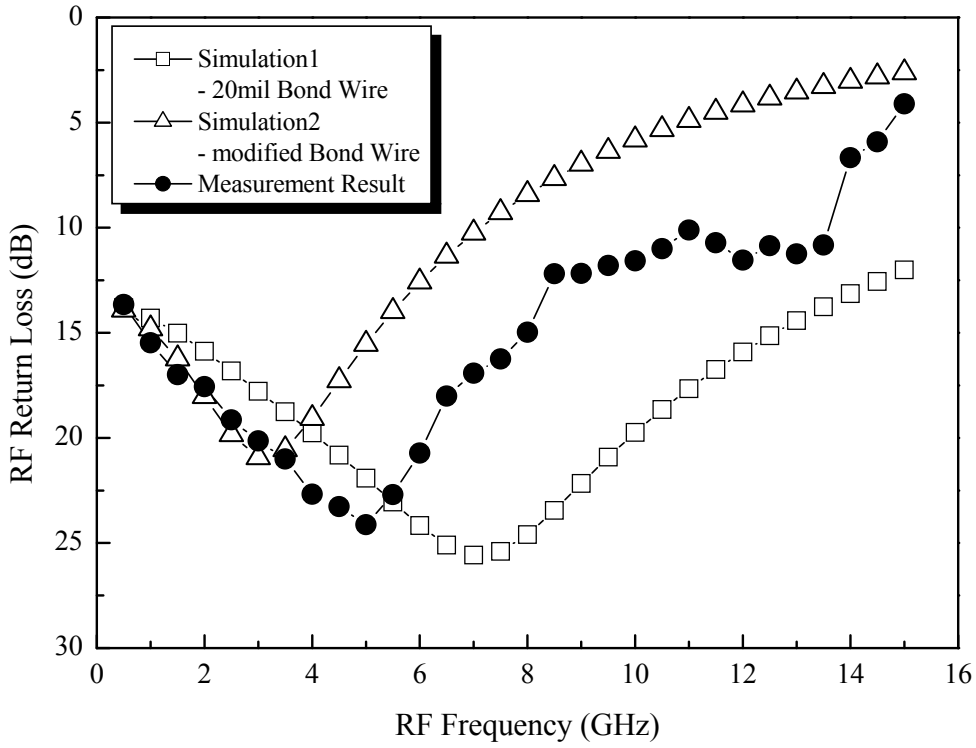
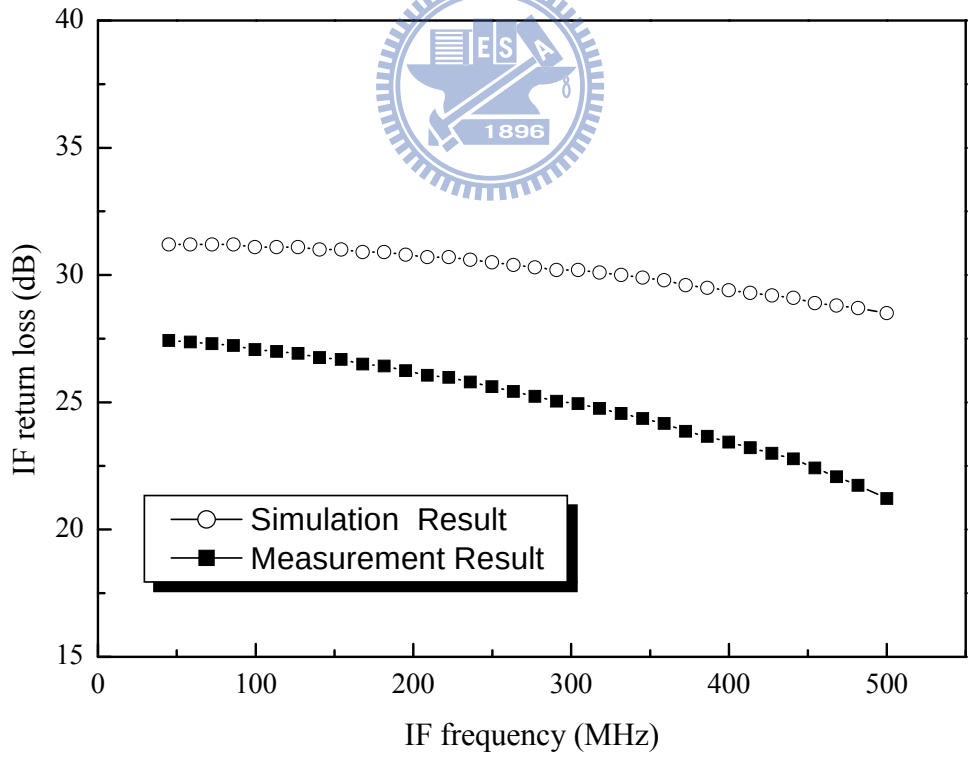


Fig. 2.7 Power conversion gain versus RF frequency with the IF frequency is 50 MHz, RF power is –30 dBm, and LO power is –5 dBm.



(a)



(b)

Fig. 2.8 Simulated and Measured (a) RF return loss versus RF frequency (b) IF return loss versus IF frequency.

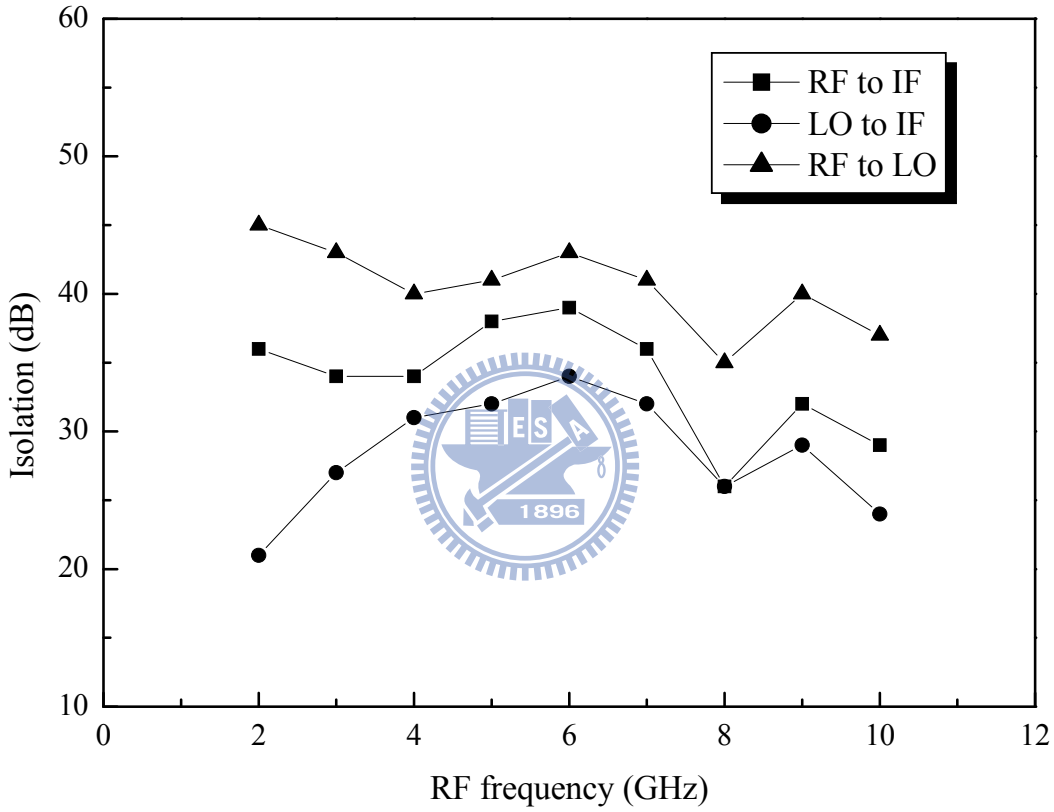
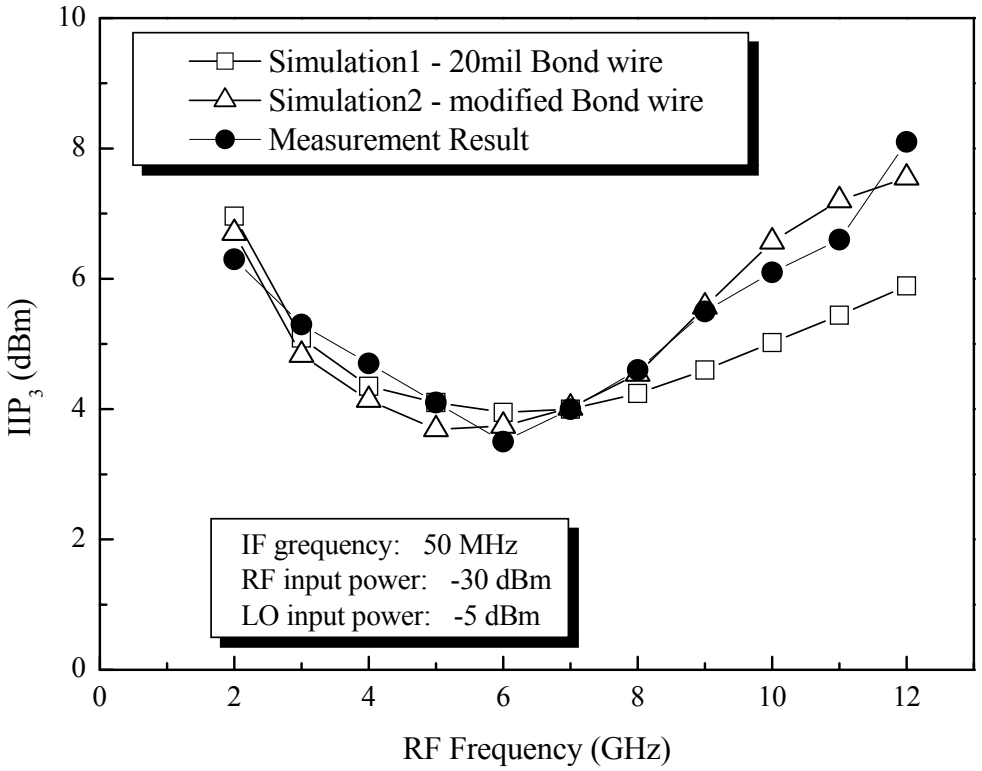
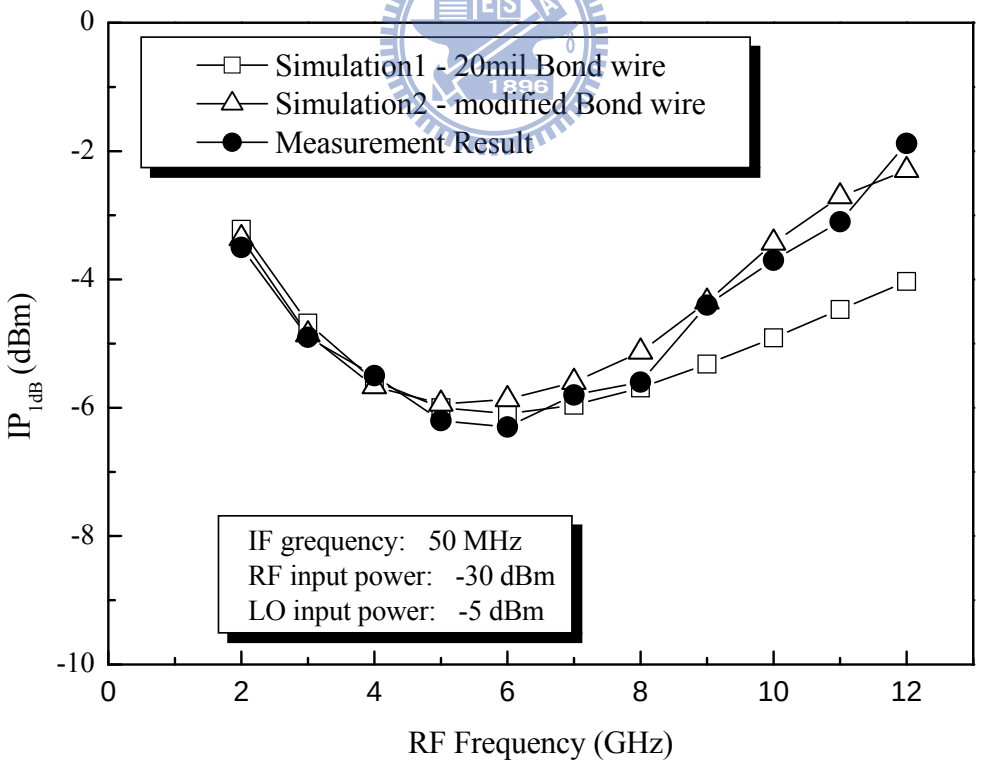


Fig. 2.9 Measured Isolation versus RF frequency.



(a)



(b)

Fig. 2.10 Simulated and Measured (a) IIP_3 and (b)IP_{1dB} versus RF frequency.

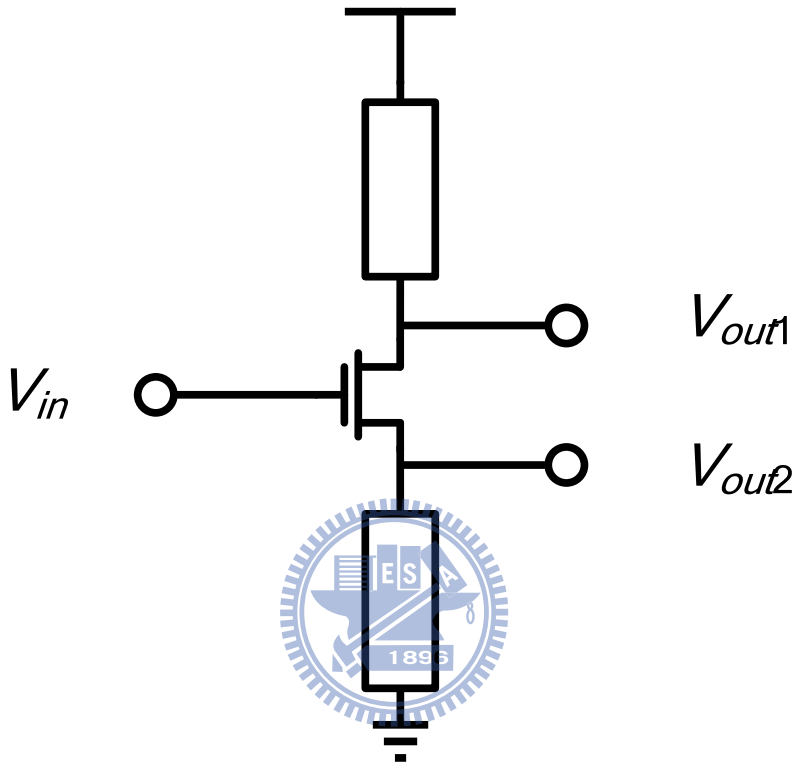


Fig. 2.11 Common-source single-FET active balun.

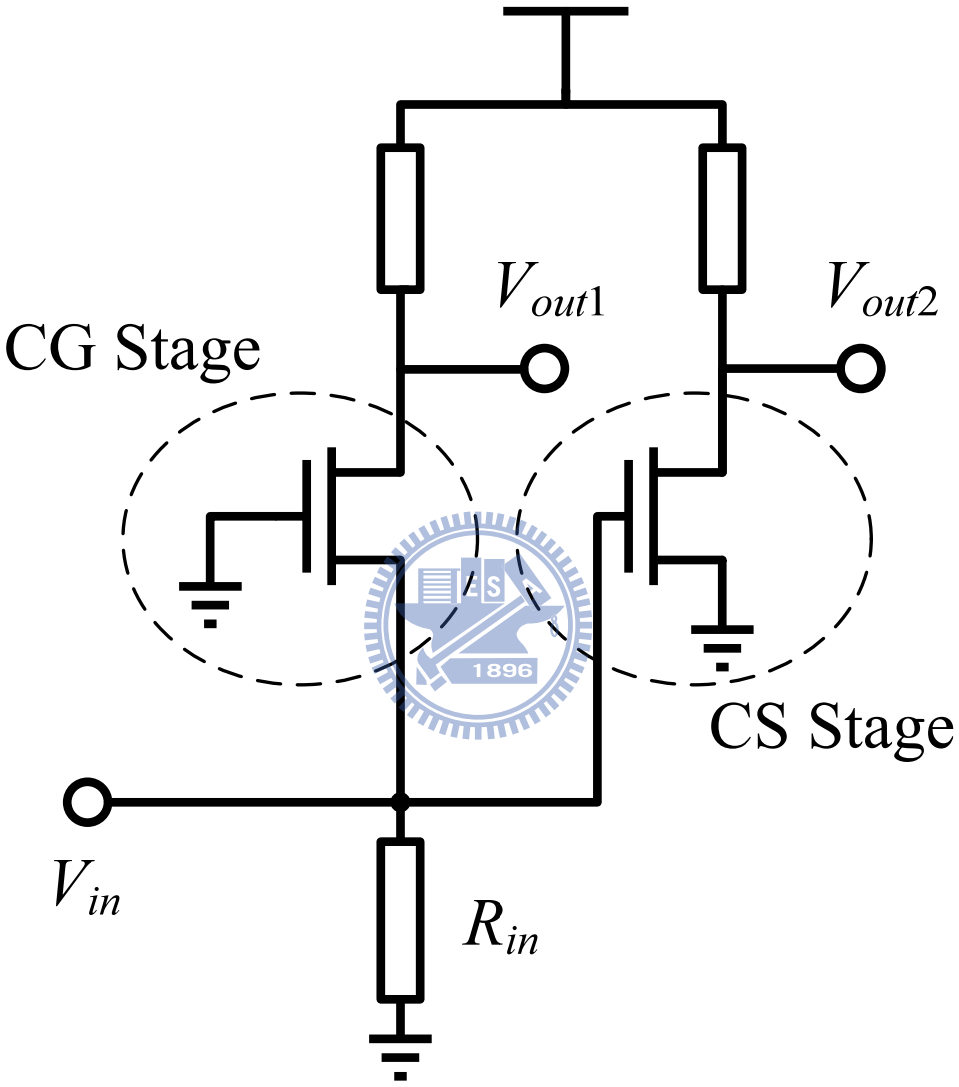


Fig. 2.12 CGCS active balun.

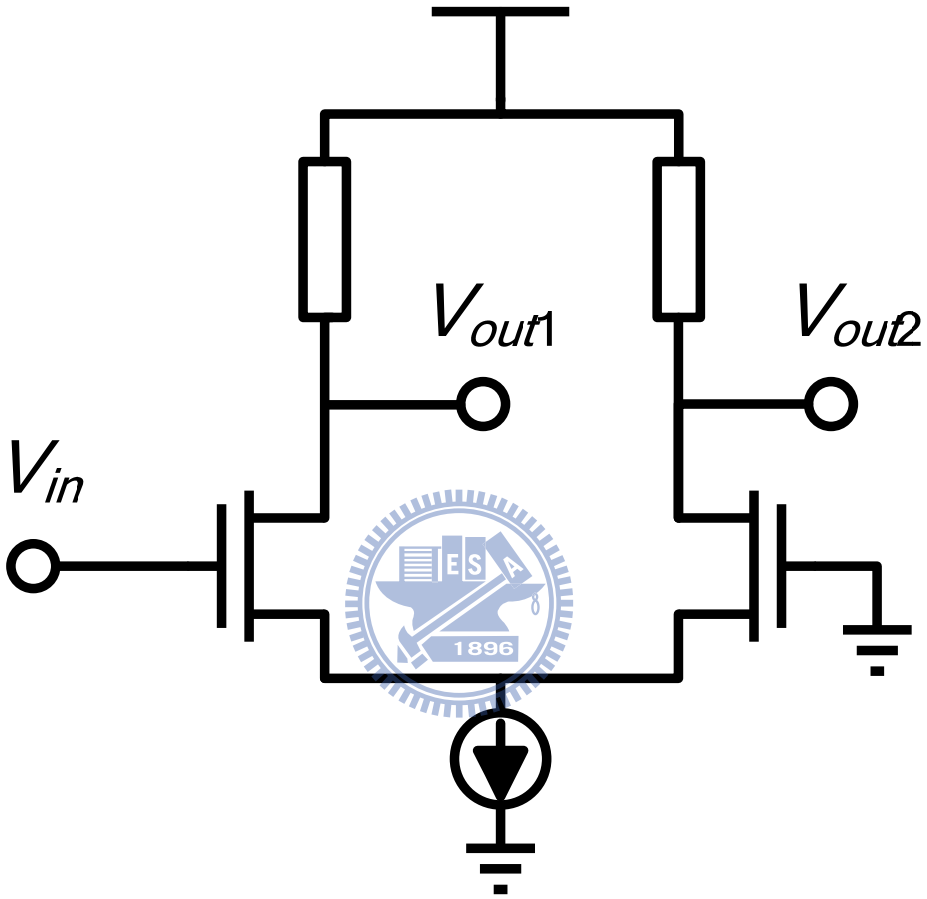


Fig. 2.13 Differential amplifier active balun.

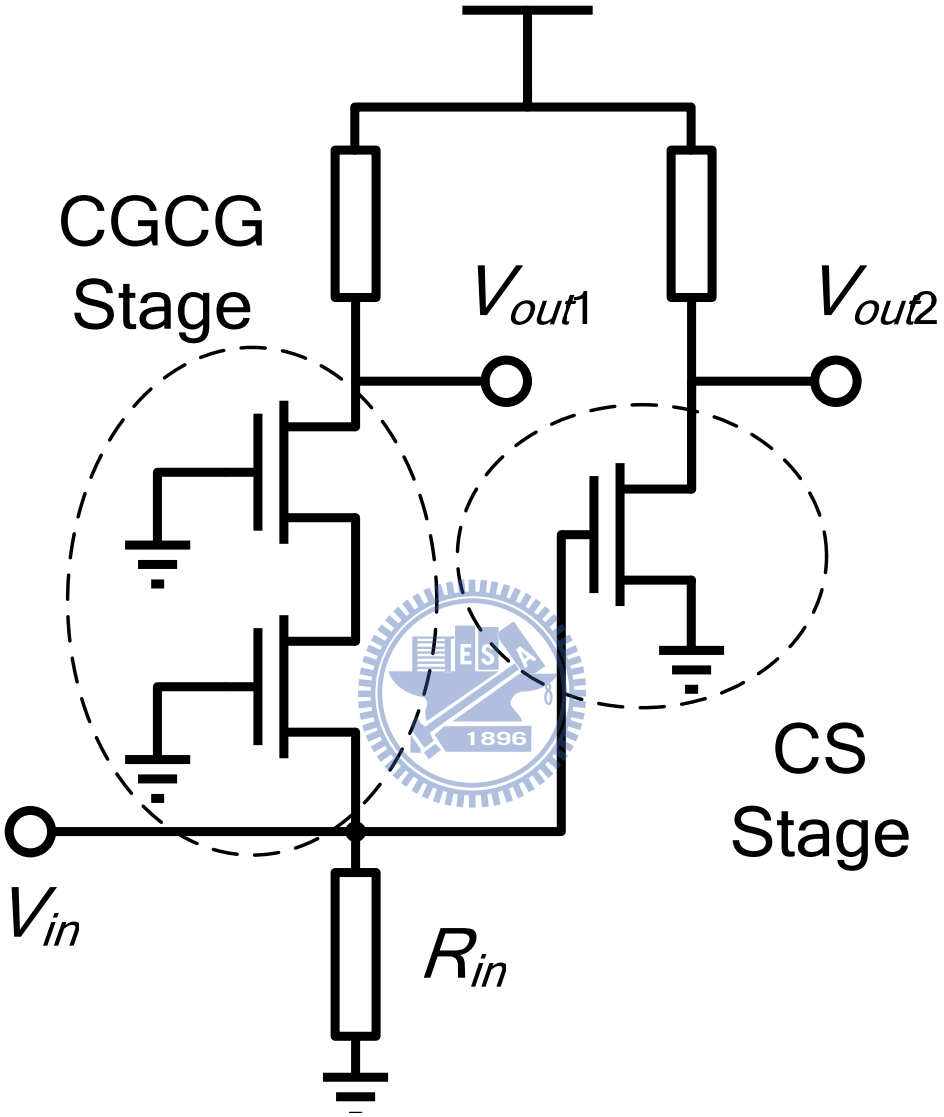


Fig. 2.14 Modified CGCS active balun.

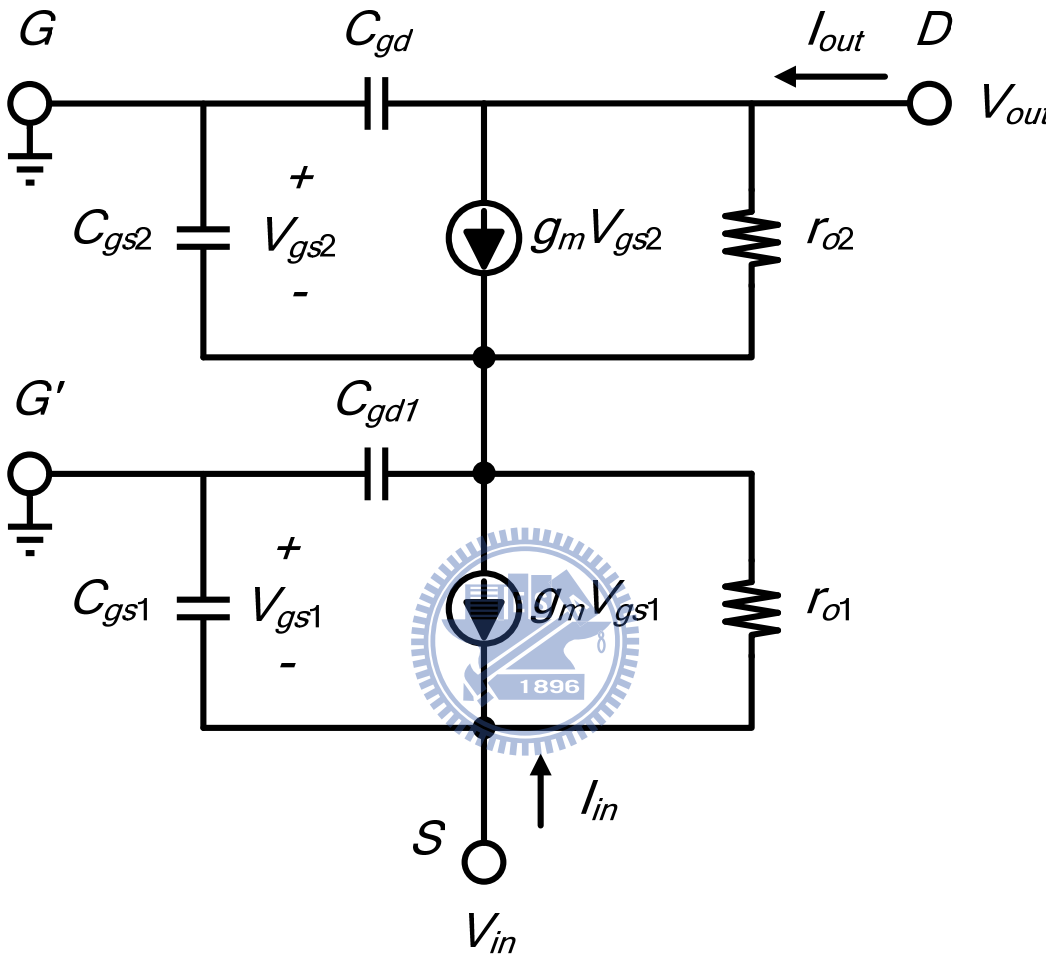


Fig. 2.15 Small-signal equivalent circuit of the cascode CG and CS structure.

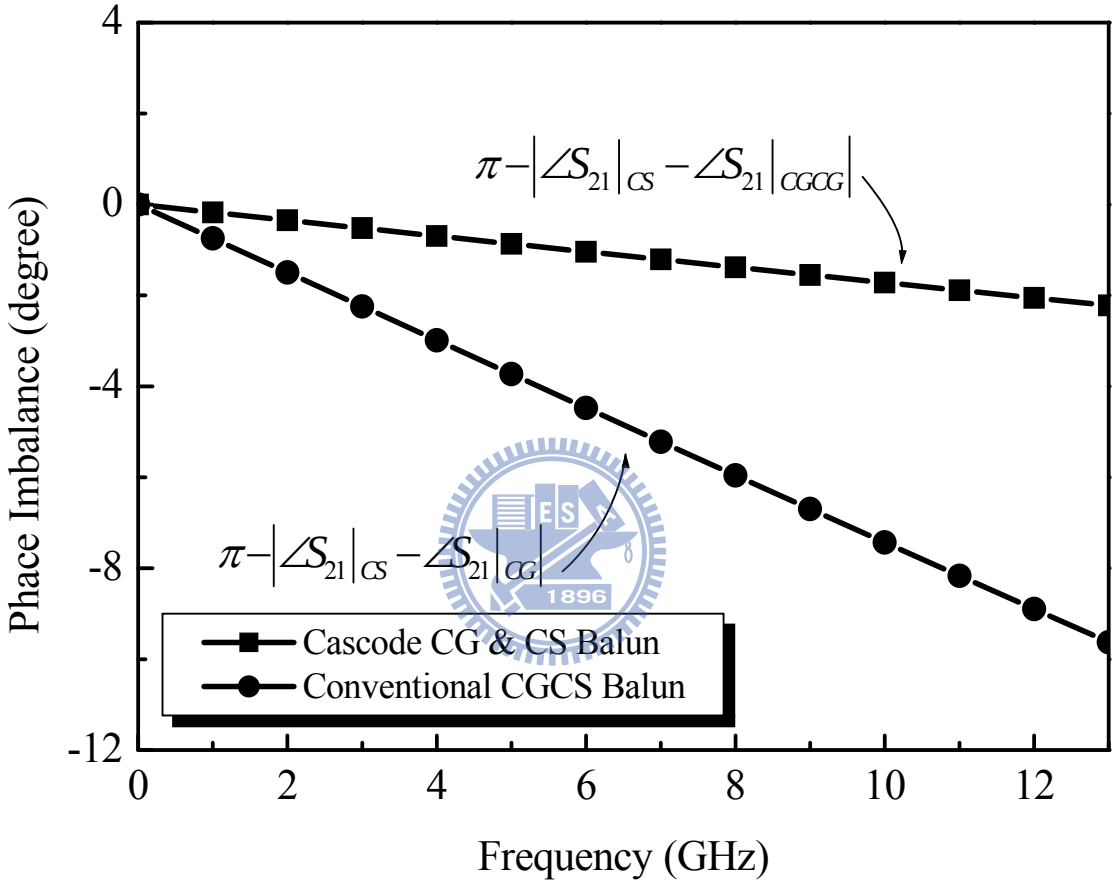


Fig. 2.16 Calculated phase imbalances of the conventional CGCS balun and cascode CG and CS balun in Fig. 2.12 and Fig. 2.14.

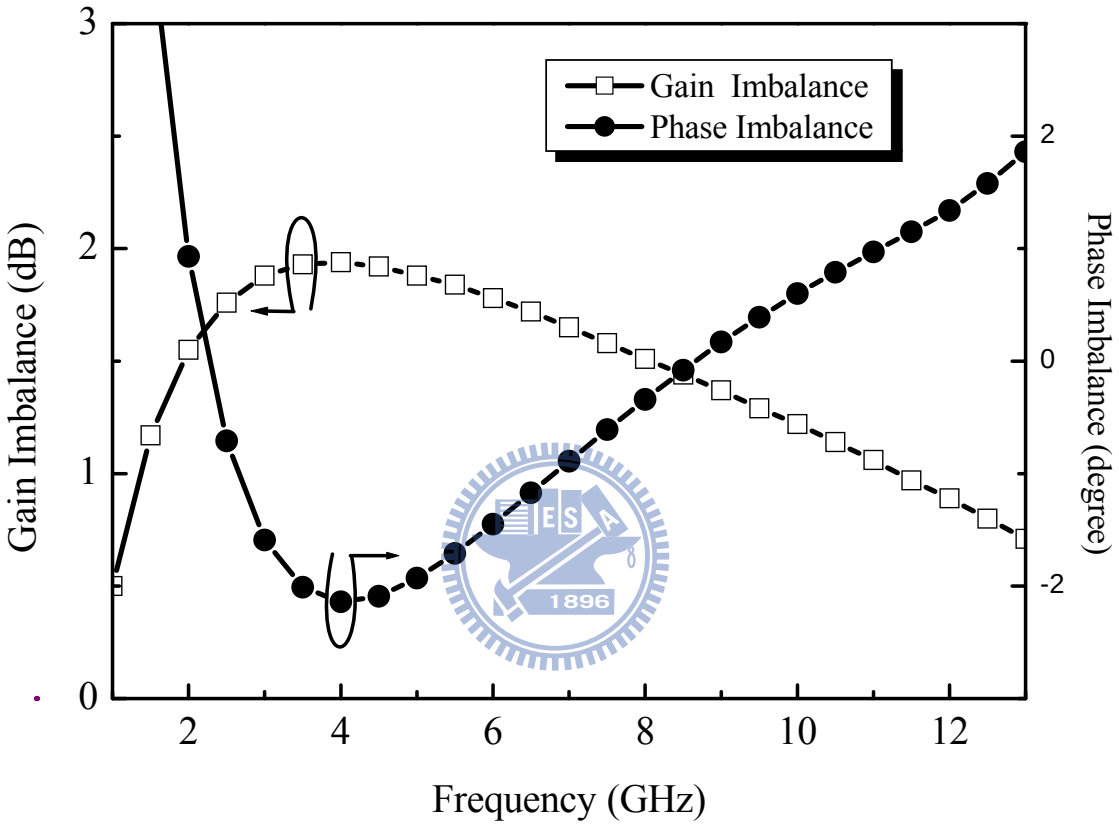


Fig. 2.17 Simulated amplitude imbalance and phase imbalance of the cascode CG and CS active balun with mixer core.

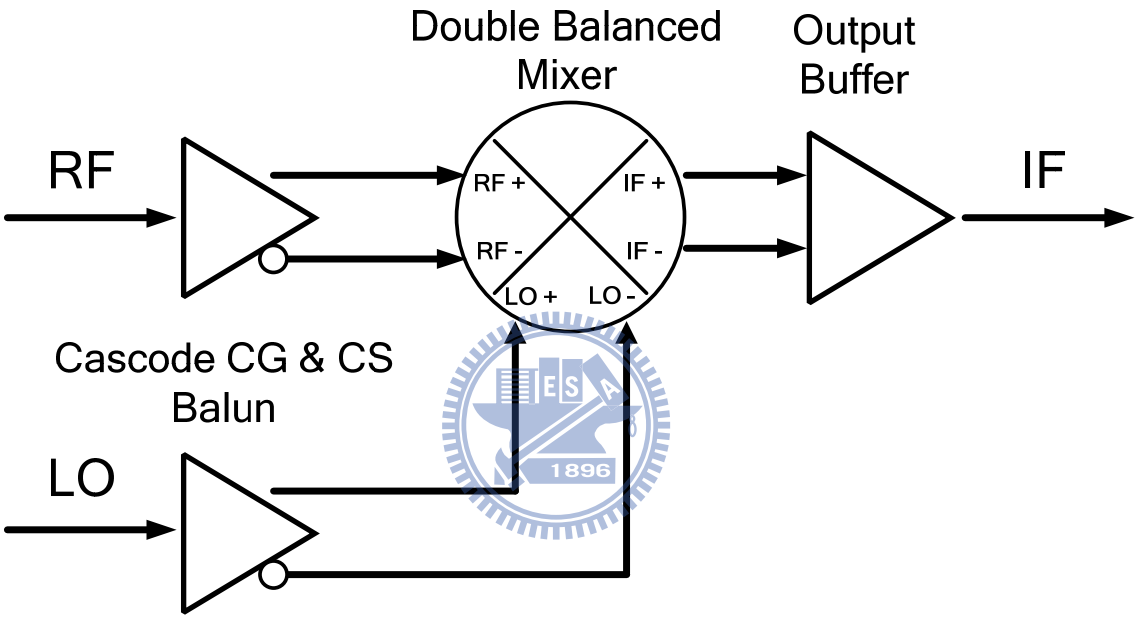


Fig. 2.18 Block diagram of the proposed mixer.

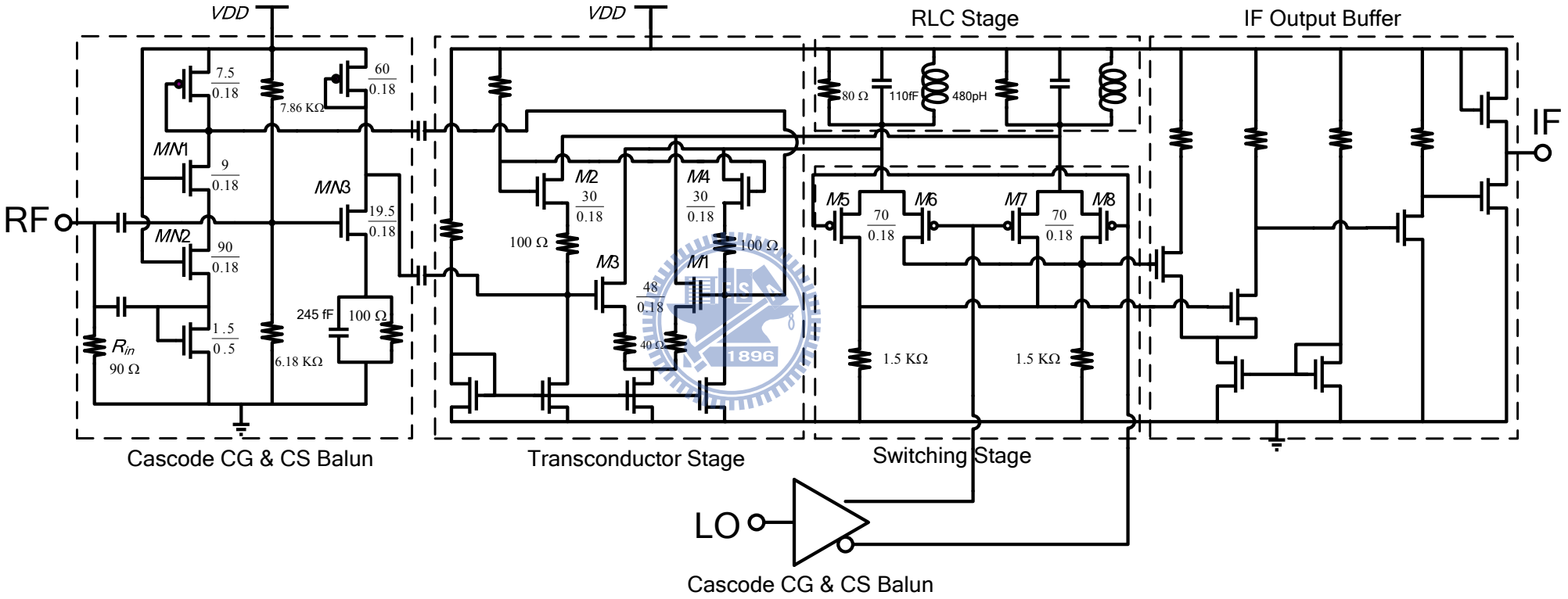


Fig. 2.19 Completed circuit schematic of the proposed mixer with wideband active baluns.

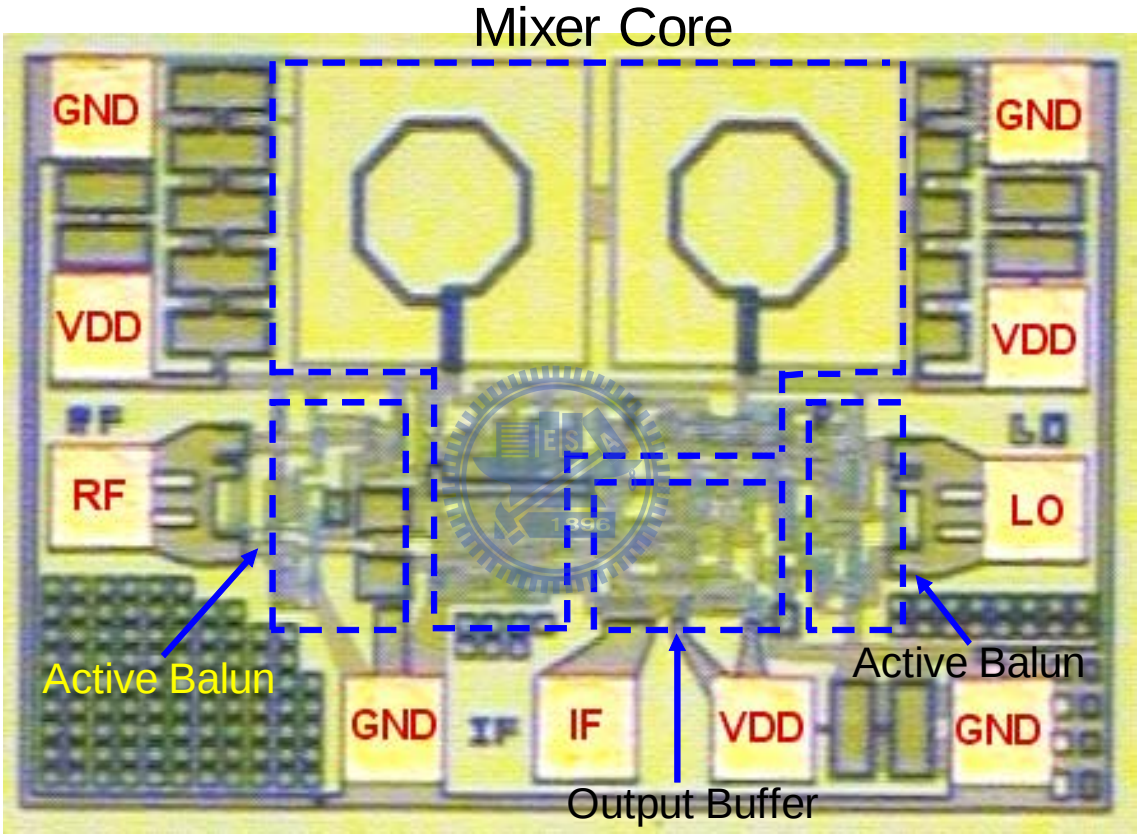


Fig. 2.20 Micrograph of the proposed mixer (size: 0.85 × 0.57 mm^2).

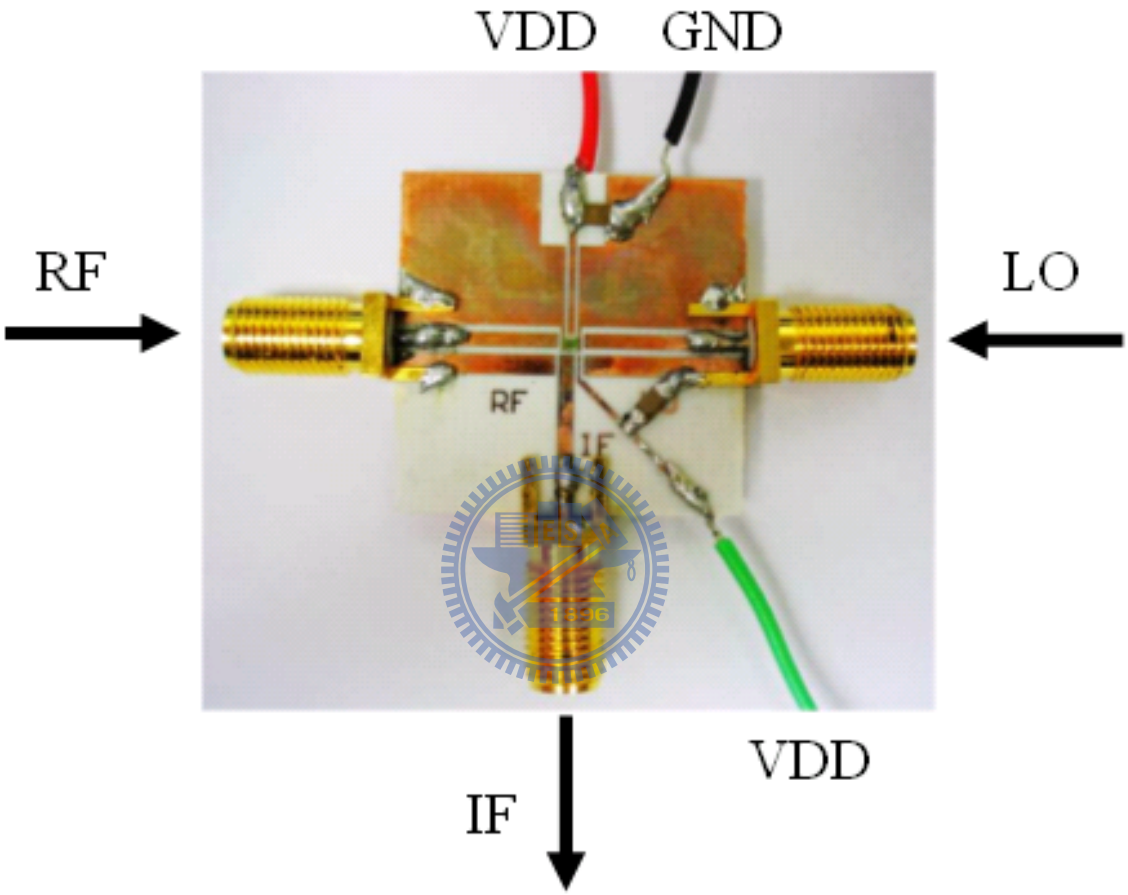


Fig. 2.21 Die mounted printed circuit board for testing.

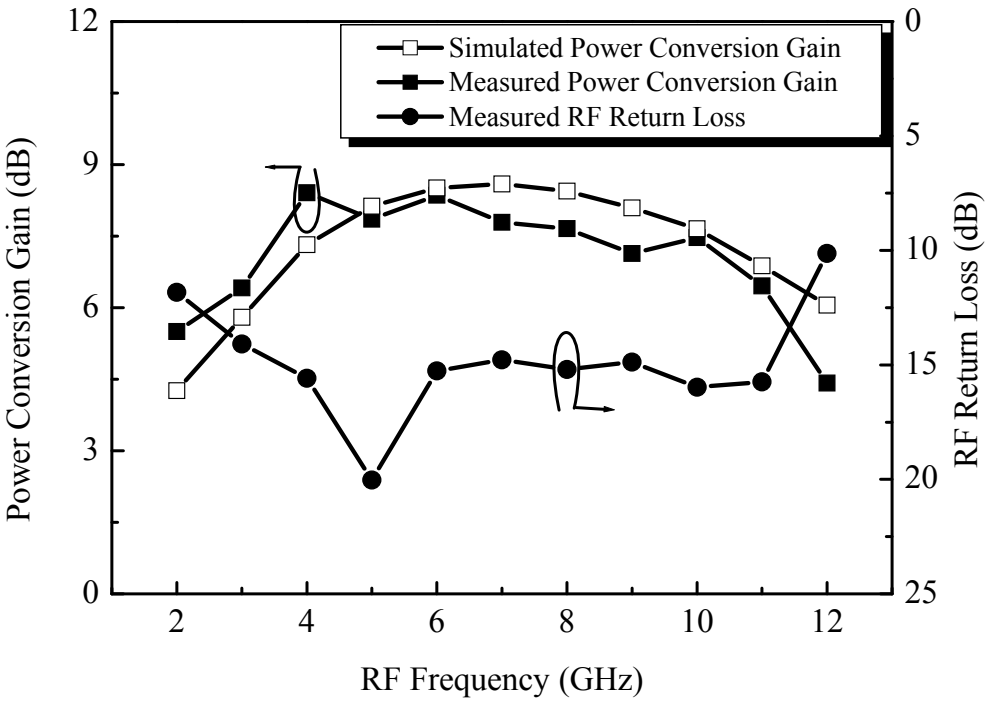


Fig. 2.22 Power conversion gain and RF return loss versus RF frequency. The IF frequency is 50 MHz, RF power is –30 dBm, and LO power is –5 dBm.

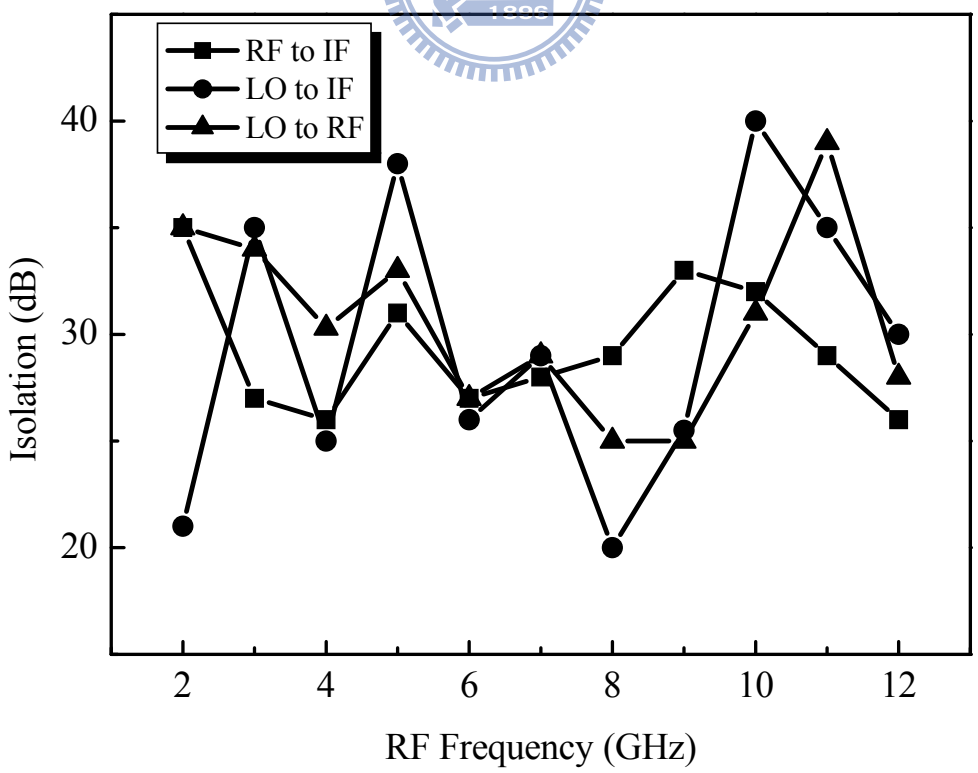


Fig. 2.23 Measured isolations versus RF frequency.

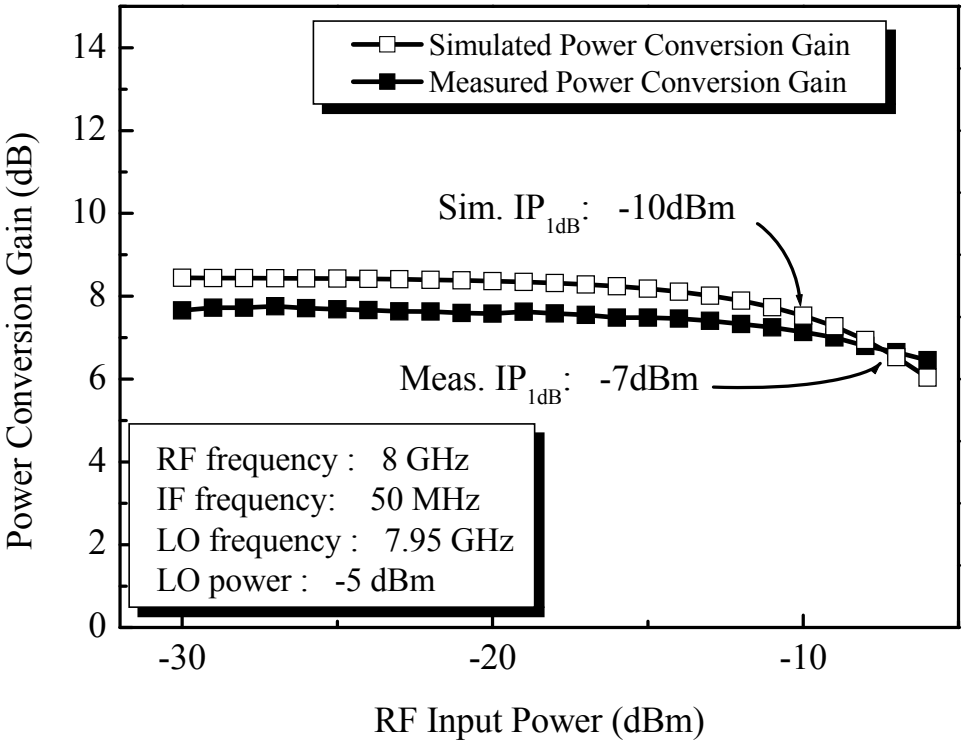


Fig. 2.24 Power Conversion Gain versus RF input power.

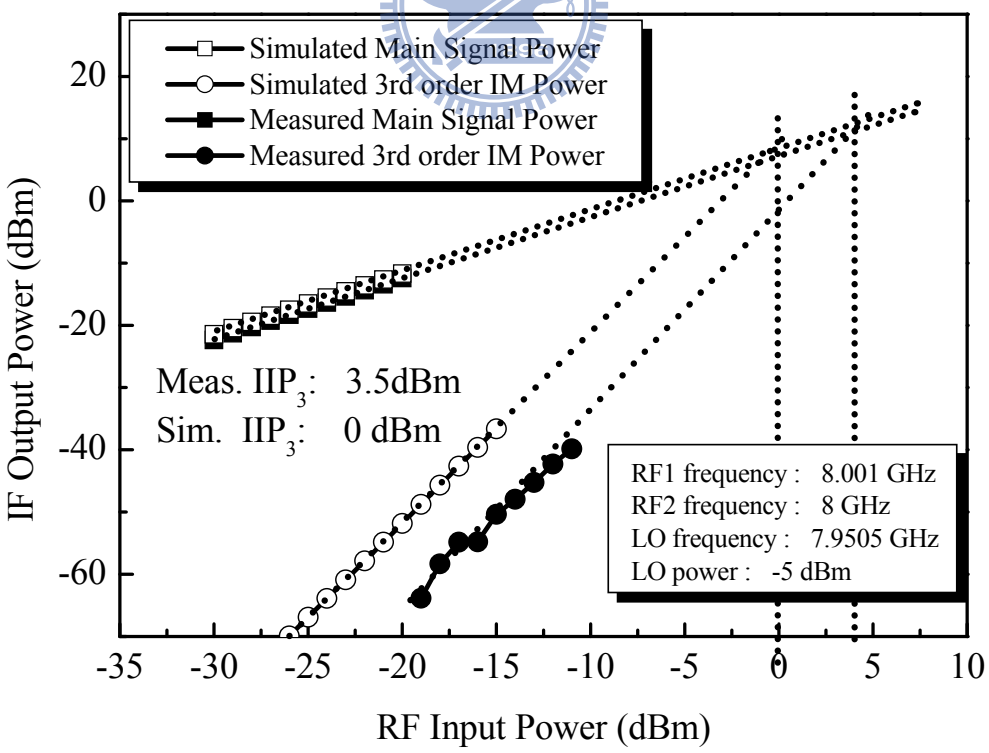


Fig. 2.25 The main signal power and third-order inter-modulation power as functions of the RF input power.

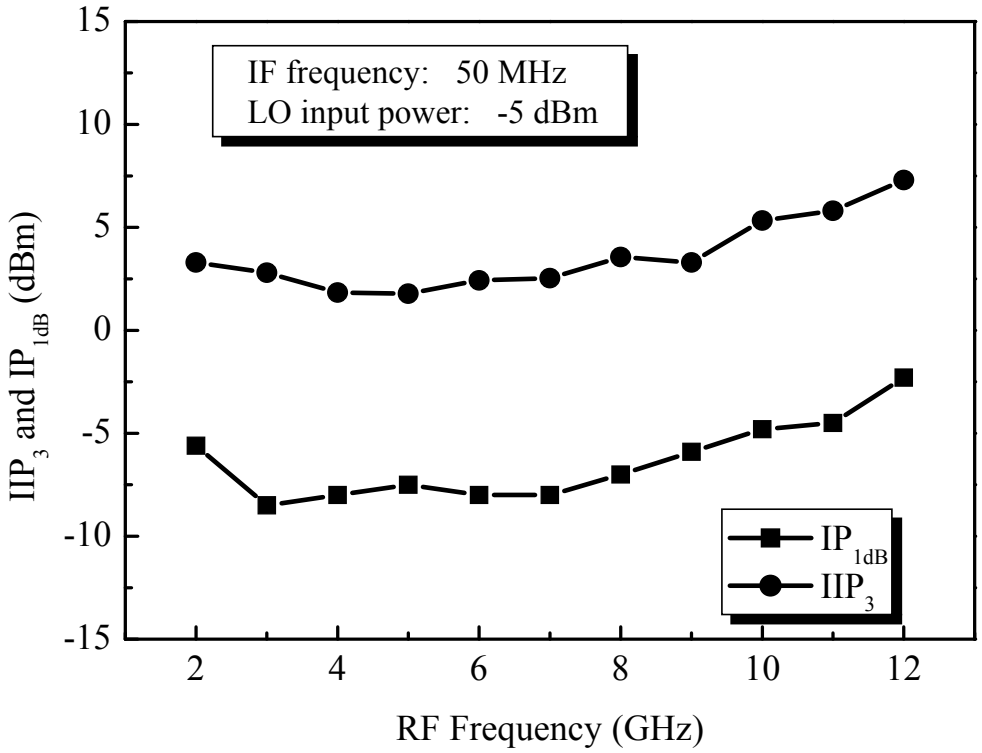


Fig. 2.26 Measured IIP_3 and IP_{1dB} versus RF frequency.

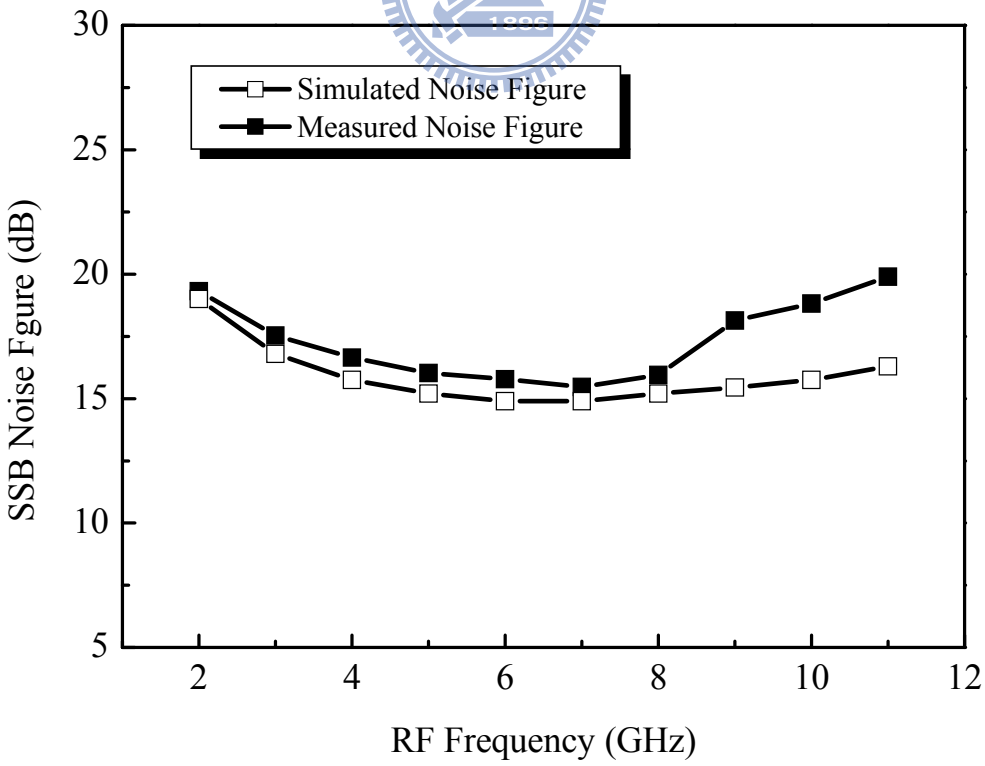


Fig. 2.27 Noise Figure versus RF frequency.

CHAPTER 3

FULL-BAND MB-OFDM UWB FREQUENCY SYNTHESIZER

According to the 802.15.3a proposal [38] provided by FCC in 2003, the MB-OFDM based UWB system separates the whole 7.5 GHz bandwidth (from 3.1 GHz to 10.6 GHz) into 14 sub-bands, each with 528 MHz bandwidth. Based on the requirement of the proposal, the guard interval duration should be less than 9.47 ns for fast frequency hopping; therefore, the UWB frequency synthesizers have to provide multi-gigahertz clocks with a fast switching speed. PLL usually takes a long setting time, so it is not suitable to use a conventional PLL synthesizer in UWB system. Although several frequency synthesizers have been proposed, none of them covers the full sub-bands with low power consumption. [39] implemented a full band frequency synthesizer and consumed power of 162 mW; [40]–[42] proposed the synthesizer satisfied 3 ~ 7 bands. This work presents the design of a fast-hopping frequency synthesizer with two PLLs and 111 mW power consumption in total.

3.1 Structure

The synthesizer is mainly composed of three parts: two PLLs, a divide-by-7 divider, and a SSB quadrature mixer for mixing and output the frequencies. The proposed UWB synthesizer is shown in Fig. 3.1. In the PLL_1, the 7392 MHz VCO output signal is fed to a divide-by-2 common-mode logic (CML) frequency divider. The divided signal keep on feeding into the divide-by-7 frequency divider, and it is

composed of Miller divider [43] and three static dividers. The output frequency f_o of the semi-dynamic frequency divider can be expressed as (3.1), where f_i is the input frequency and N is the number of the cascaded static dividers:

$$f_o = \frac{f_i}{2^N \mp 1}. \tag{3.1}$$

The minus or plus sign of denominator can be decided by choosing up or down conversion of the SSB mixer. We choose N equal to 3 and up conversion for SSB mixer with the input frequency f_i of 3696 MHz; meanwhile, the output frequency f_o is

$$f_o = \frac{3696\ \text{MHz}}{2^3 - 1} = 528\ \text{MHz}. \tag{3.2}$$

The input signal of the SSB is mixed with the output frequency f_o to achieve the divide-by-7 function. Multiple output signals can be obtained from different divider outputs in the loop of the divide-by-7 divider. Therefore, the output frequencies of the semi-dynamic frequency divider can be $\frac{2^n}{2^N \mp 1}$ f_i, where N represents the number of cascaded dividers, and n is a positive integer equal or less than N−1. In our design, 3696 MHz input will be divided into 528 MHz signal, 1056 MHz, and 2112 MHz. Furthermore, the frequency of 1584 MHz can be gathered from previous divider outputs. By mixing 2112 MHz and 1056 MHz, the mixed signal 3168 MHz will be divided into quadrature 1584 MHz output signals. In conclusion, 528 MHz, 1056 MHz, and 1584 MHz can be produced by divide-by-7 divider and selected by a multiplexer MUX1. The selected quadrature outputs are applied in SSB-Quadrature mixer mixed with the outputs signal of MUX2. The divide-by-2 divider used in the divide-by-7 divider is realized by CML divider, and the detail circuit is drawn in the

Fig. 3.2. For PLL_1, the 1/112 frequency divider is composed of the one-stage divide-by-2 CML divider, one-stage divide-by-7 semi-dynamic frequency divider, and three-stage divide-by-2 true single phase clocking (TSPC) dividers. For PLL_2, the 1/64 frequency divider is composed of the one-stage divide-by-2 CML divider and five-stage divide-by-2 TSPC dividers.

SSB-Quadrature mixer, the third part of synthesizer, is responsible for mixing the output signals from MUX2 and divide-by-7 divider. By composing those components mentioned above, the carriers of whole 14 bands from 3.1 GHz to 10.6 GHz are producible. The proposed synthesizer switches bands by gate control logic rather than modifying PLL locking frequency, and the switching time during band hopping is 2 ns that less than the standard of 9.47 ns.

The proposed PLLs produced 7.392 GHz and 5.016 GHz. The 528 MHz, 1056 MHz, and 1584 MHz can be produced via divide-by-7 divider. All the frequency bands can be mixed out from the frequencies of MUX1 outputs, DC and MUX2 outputs.

3.2 Circuit Design

3.2.1 Voltage-Controlled Oscillator

The VCO is the most important block of the PLL because it works at a high frequency and requires a low phase noise. There are several ways to build a VCO. The adapted VCO schematics are shown in Fig. 3.3. The differential output VCO resonates at 7392 MHz in PLL_1, and the quadrature output VCO resonates at 5016 MHz in PLL_2, respectively. At least, the one-MHz offset phase noise for UWB

oscillator is −91.29 dBc/Hz [44]. The VCO is made of a cross-coupled pair to generate negative resistance for the compensation of the resistive loss from the LC-tank. A center-type spiral inductor with symmetric structure and MOS varactors are used in the VCO design. The varactors are operated in accumulation mode, and they have higher Q factor than the pn-junction varactors. The common source amplifiers are employed as the output buffers for testing purpose.

3.2.2 Frequency Divider

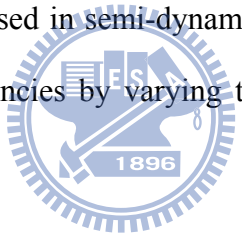
There are three types of frequency divider utilized in the PLLs: CML divider, TSPC divider, and semi-dynamic frequency divider.

3.2.2.1 Divide-by-2 Frequency Divider

The CML stage is consisted of sampling and holding pairs which can provide quadrature outputs. The CML divider uses master-slave architecture as shown in Fig. 3.2. The master-slave divider needs a differential input and then output quadrature signals (0^o, 90^o, 180^o, 270^o). Fig. 3.4 shows the schematic of the adopted TSPC divide-by-2 divider. It only needs 9 transistors and one clock with the advantage of compact circuit. To compare with the CML divider, the TSPC utilizes less transistors and the interconnections between them is highly reduced. Due to the lower interconnection capacitance, the transistor size can be closed to the minimum value and then the power consumption is decreased. However, the TSPC divider generates square wave, and that limits the speed of the TSPC divider.

3.2.2.2 Divide-by-7 Semi-dynamic Frequency Divider

The divide-by-7 frequency divider, as shown in Fig. 3.5 and Fig. 3.6, utilizes a single side-band mixer together with 3 divide-by-2 CML static dividers to implement a divide-by-7 divider. In this work, the semi-dynamic frequency divider is responsible for the generation of three frequencies, 528 MHz, 1056 MHz, and 1584 MHz, to the multiplexer. The input frequency of the divider is 3696 MHz, and the output frequency of the last stage is 528 MHz. The multiple frequencies can be got from forward divider-by-2 CML stages, i.e. 1056 MHz and 2112 MHz. The frequency of 3168 MHz can be got from mixing the frequencies of 1056 MHz and 2112 MHz. Moreover, the frequency of 1584 MHz can be generated by dividing the frequency of 3168 MHz. Each CML divider used in semi-dynamic frequency divider is optimized for its different operation frequencies by varying the device sizes of sampling and holding pairs.



3.2.3 Phase Frequency Detector, Charge Pump, and Loop Filter

The phase frequency detector is used to provide an output signal whose DC component to charge pump, and the operation principle of PFD is to detect the phase difference between two periodic input signals. The designed PLL adopted precharge-type PFD shown as Fig. 3.7. The phase frequency detector compares the phase and frequency difference between the reference signal and the signal feedback by the TSPC frequency divider, and it sends a signal UP or DOWN to charge or discharge the next stage. The UP signal will be high when the input reference signal is operating at a higher frequency than the feedback signal. The charge pump forces current into the loop filter and the VCO control voltage will be raised due to the high

UP signal. Then it increases the VCO frequency and brings the feedback signal until the frequency is the same as the reference signal, and vice versa, respectively. The adopted precharge-type PFD not only reduces the dead zone problem and the limitation of maximum operation frequency, but also lowers the chip size than the conventional PFDs.

The charge pump is served to convert the difference of the two into the corresponding current. The circuit diagram of the adopted charge pump (CP) and standard passive loop filter (LF) are shown in Fig. 3.8. The adopted charge pump consists of two switched current sources to reduce the charge sharing effect. The current sources charge into or out of the loop filter depending on the switches controlled by the output signals UP and DN of the PFD, respectively. Furthermore, the LF converts the charge into the VCO's control voltage V_C. All passive capacitors are realized by the metal-insulator-metal (MIM) capacitors. For the PLL_1, $C1_1$ = 3.69 pF and $C2_1$ = 55.32 pF with a $R2_1$ = 7.33 kΩ. For the PLL_2, $C1_2$ = 4.33 pF and $C2_2$ = 65 pF with a $R2_2$ = 5.25 kΩ.

3.2.4 Single Side-Band Mixer

The SSB mixer is used to generate multi-band carrier signals for frequency translation with electronic band selection capability. The SSB mixer can provide either upper or lower sideband output through an electronic control. In the ideal case, the SSB mixer only generates either upper or lower sideband element. In practice, the both sidebands are present due to non-quadrature phase or amplitude imbalance of the input signals.

The schematic of the UWB SSB mixer is shown in Fig. 3.9, which consists of four mixers, and two capacitor switches for selection of the differential frequency

bands. This architecture finally achieve I+/I–/Q+/Q– signals of UWB 14 bands as shown in Table 3.1.

3.3 SIMULATION RESULTS OF THE UWB FREQUENCY SYNTHESIZER

The whole synthesizer circuitry is simulated by using the commercial software package ADS. The chip microphotograph of the proposed synthesizer is shown in Fig. 3.10. The simulation result shows that output frequencies from 3.432 GHz to 10.296 GHz, less than 2 ns hopping time, and 111 mW power consumption including the output buffers of 30 mW. The simulated waveforms of two VCOs are shown in Fig. 3.11, and the simulated setting time of the two close-loop PLLs are shown in Fig. 3.12. The setting time of the PLLs are both less than 2 μs. The final total area including pads is 2.29×2.51 mm^2. Fig. 3.13 shows the four output waveforms and spectrums of the UWB frequency synthesizer and the spurious is less than –25 dBc for all bands. For the layout consideration, the RF signal paths need to be well simulated by EM simulation software as like as HFSS or ADS Momentum due to the complicated quadrature signals. Moreover, the geometric symmetry of circuitry is necessarily concerned. Therefore, the path length of quadrature signals traveled must especially maintain equal length for equivalent phase. For the noise consideration, RF ground and power source should be separated from digital noisy circuits. In some cases, well-design layout will reduce the cross-couple of RF signals.

3.4 Summary

A frequency synthesizer with the SDFD for UWB communication system is proposed and designed. The synthesizer consists of: 1) two PLLs for frequency generation; 2) a divide-by-7 SDFD to generate several frequencies; and 3) wideband SSB with capacitor switches. The proposed SDFD circuit is introduced to divide the frequency by seven and co-designed with the PLL. As can be seen from the simulation results, the SDFD has the ability to generate several different frequencies to mix for the 14 output bands. The designed CMOS synthesizer has full-band output with −7.6 dBm output power and 111 mW DC power consumption.

Finally, the recently published CMOS synthesizers [39], [45]–[46] are shown in Table 3.2. The proposed synthesizer structure provides a solution to the low-power and high-performance LO. Therefore, the proposed synthesizer is a favorable choice for use in UWB applications.

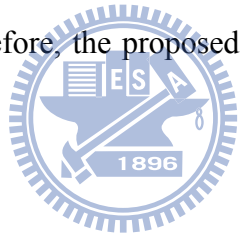


Table 3.1

Frequency plan for UWB applications (3.1−10.6 GHz).

Band Group	Band #	Center frequency (MHz)	Frequency Generation
A	1	3432	5016-1584
	2	3960	5016-1056
	3	4488	5016-528
B	4	5016	5016
	5	5544	5016+528
	6	6072	5016+1056
C	7	6600	5016+1584
	8	7128	8712-1584
	9	7656	8712-1056
	10	8184	8712-528
D	11	8712	8712
	12	9240	8712+528
	13	9768	8712+1056
	14	10296	8712+1584

Table 3.2

Comparison with published UWB synthesizers.

	Bands	VDD	Output power	Spurious (dBc)	Power Consumption (mW)	Chip Size (mm^2)
This work	14	1.3	>-7.6 dBm	-25	111 (including output buffers of 30 mW)	2.3 × 2.5
[39] 2006 ISSCC	14	1.8	-12 dBm	-35.3	162	1.2 × 1.27
[45] 2007 JSSC	9	1.5	> 400 mVpp	-22	89	2.5 × 1.4
[46] 2008 ISSCC	14	1.8	-25.9 dBm	-45	117	2.5 × 2.2

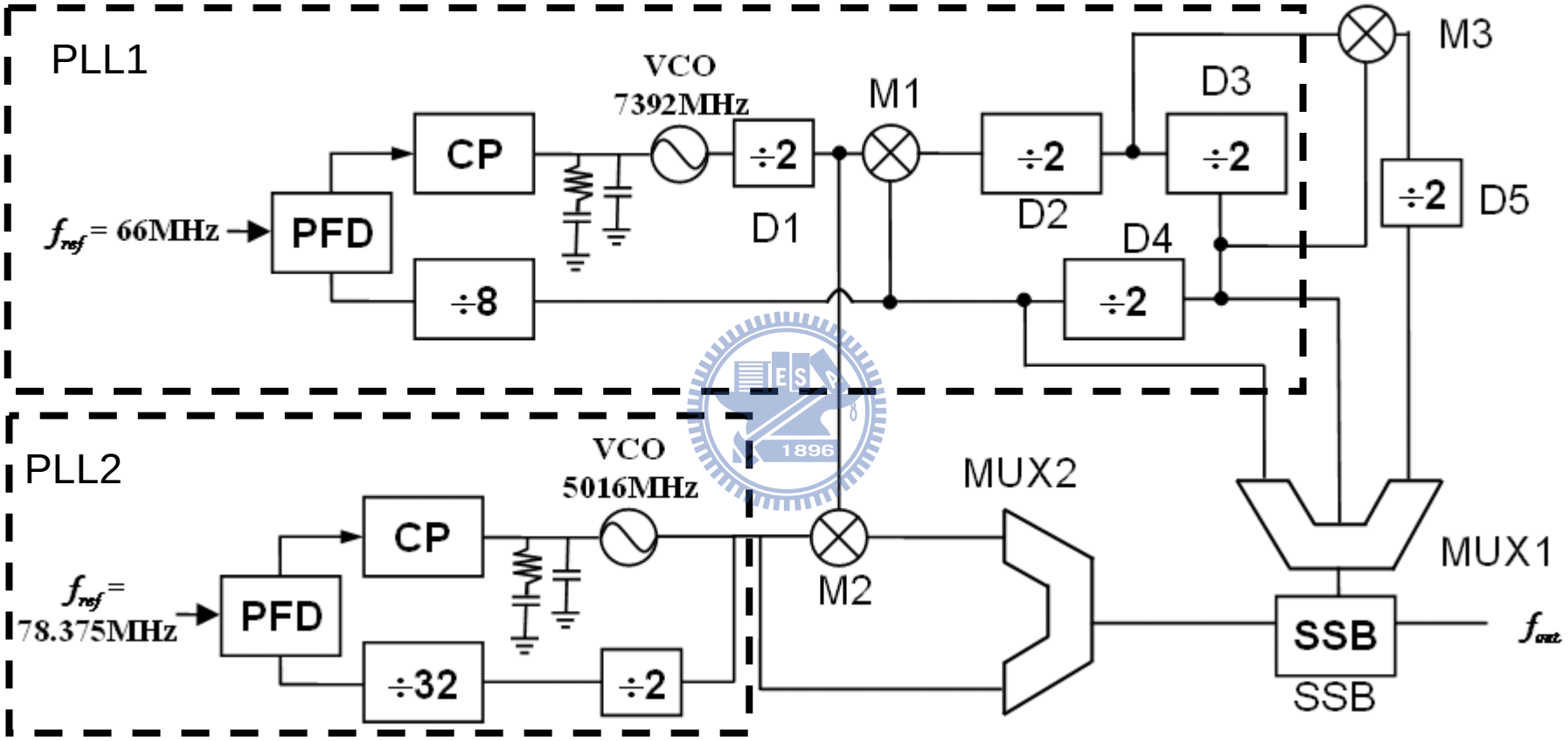


Fig. 3.1 Building block of over the UWB frequency synthesizer.

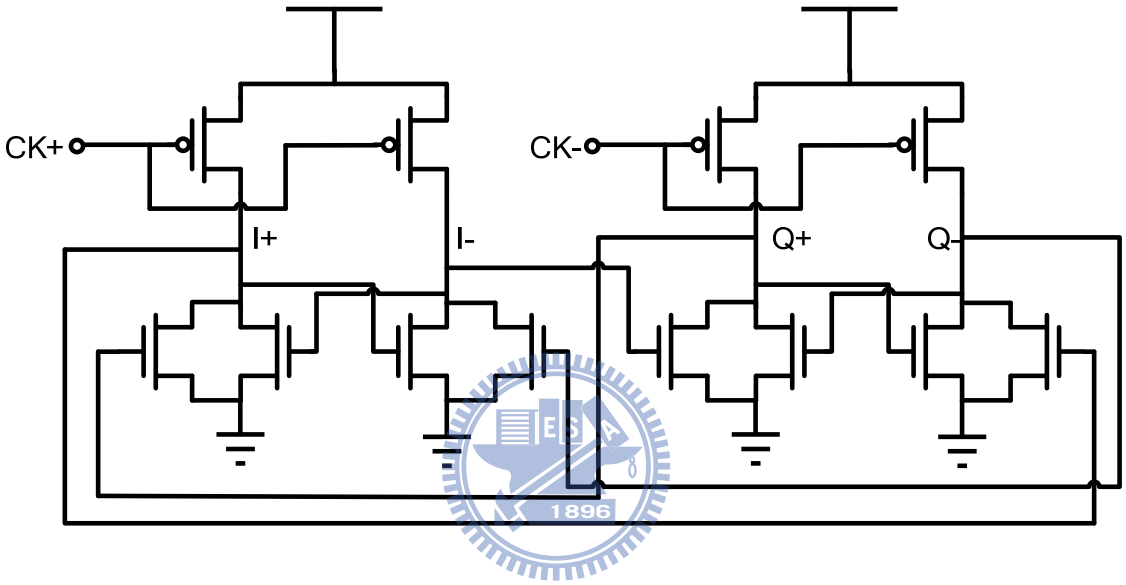
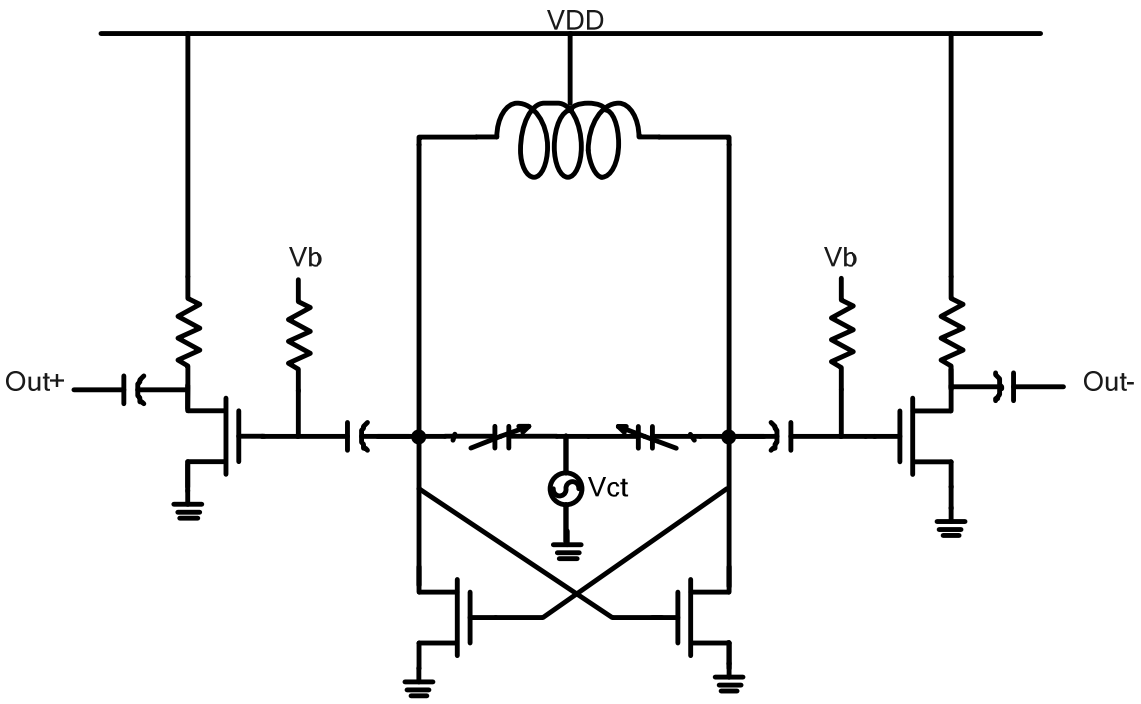
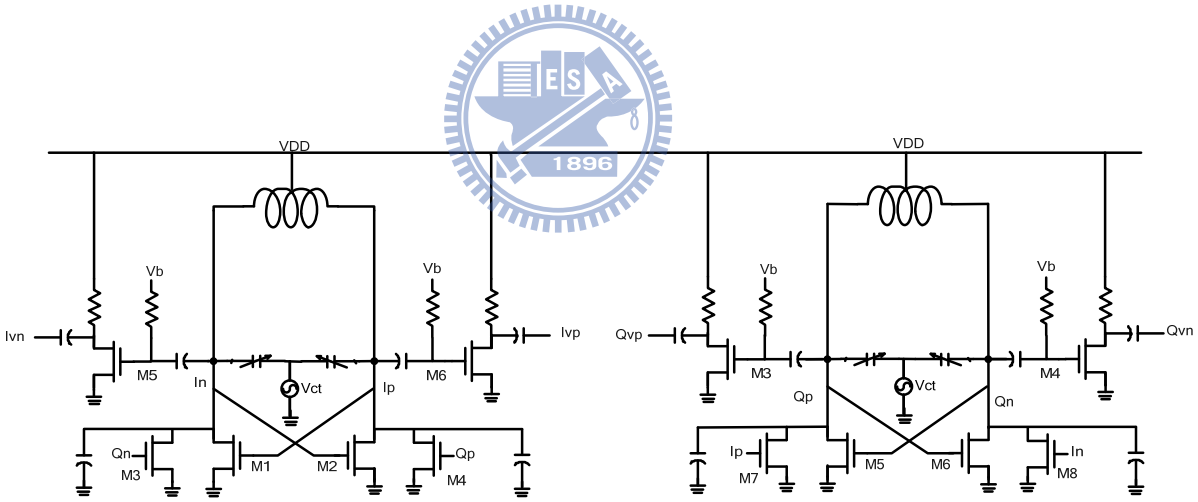


Fig. 3.2 Simplified schematic of CML static frequency divider.



(a)



(b)

Fig. 3.3 Circuit diagram of (a) 7.392 GHz VCO (b) 5.016 GHz QVCO.

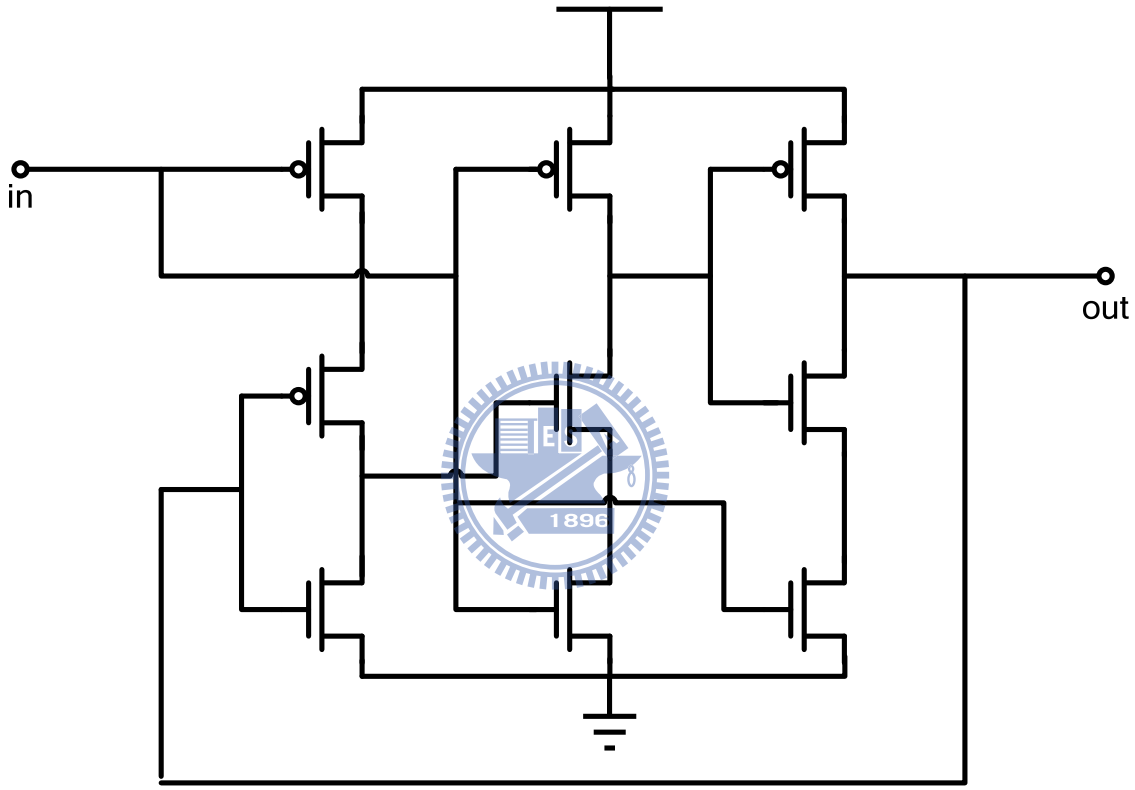


Fig. 3.4 Simplified schematic of TSPC frequency divider.

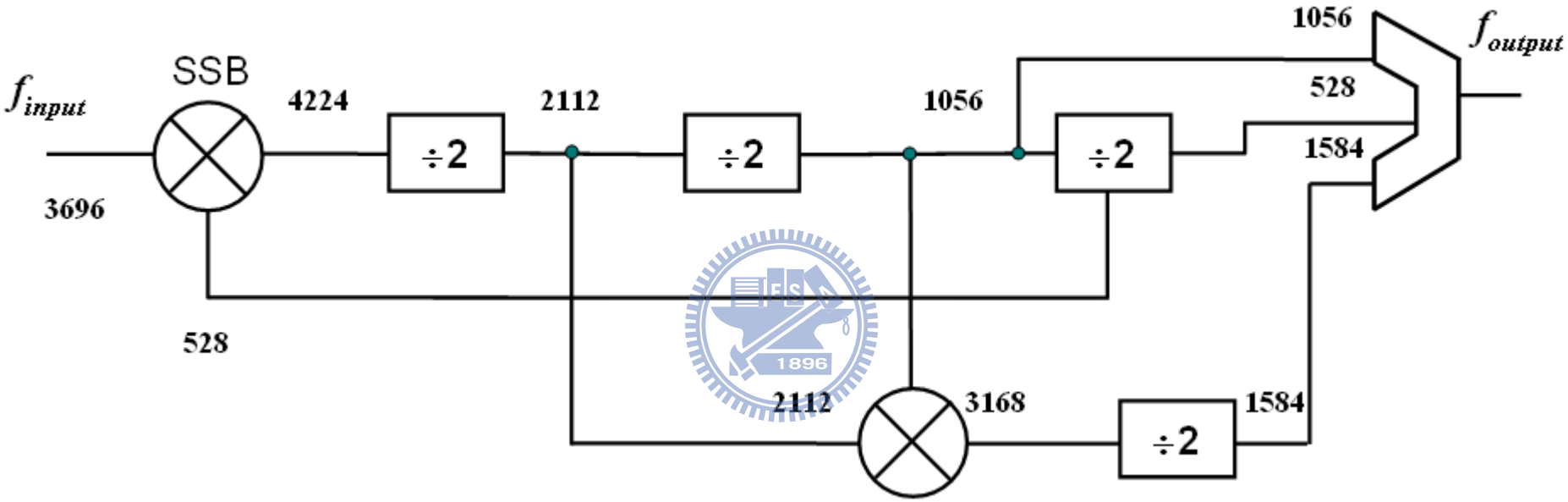


Fig. 3.5 The building blocks of the divide-by-7 divider.

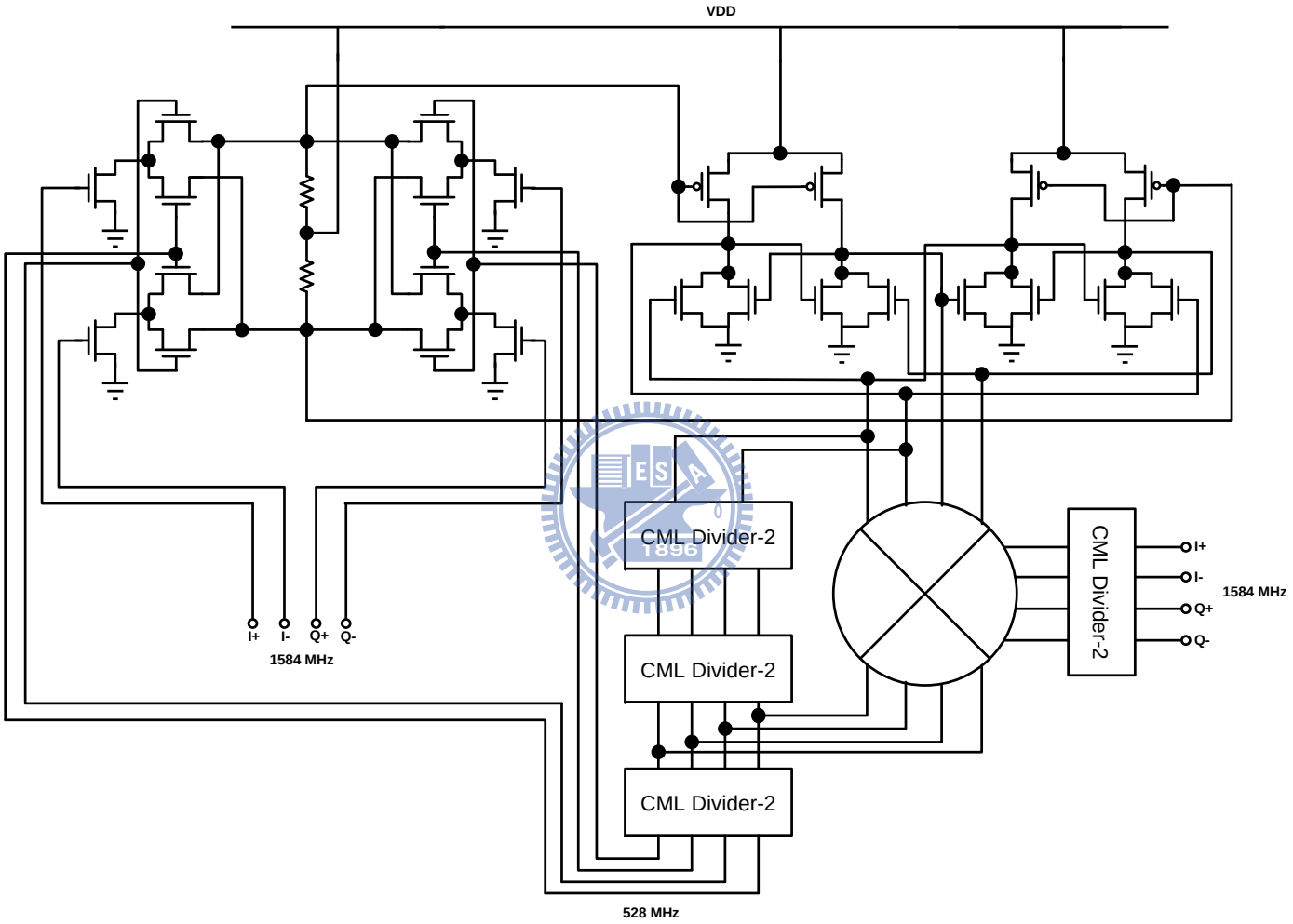


Fig. 3.6 The schematic of the divide-by-7 divider.

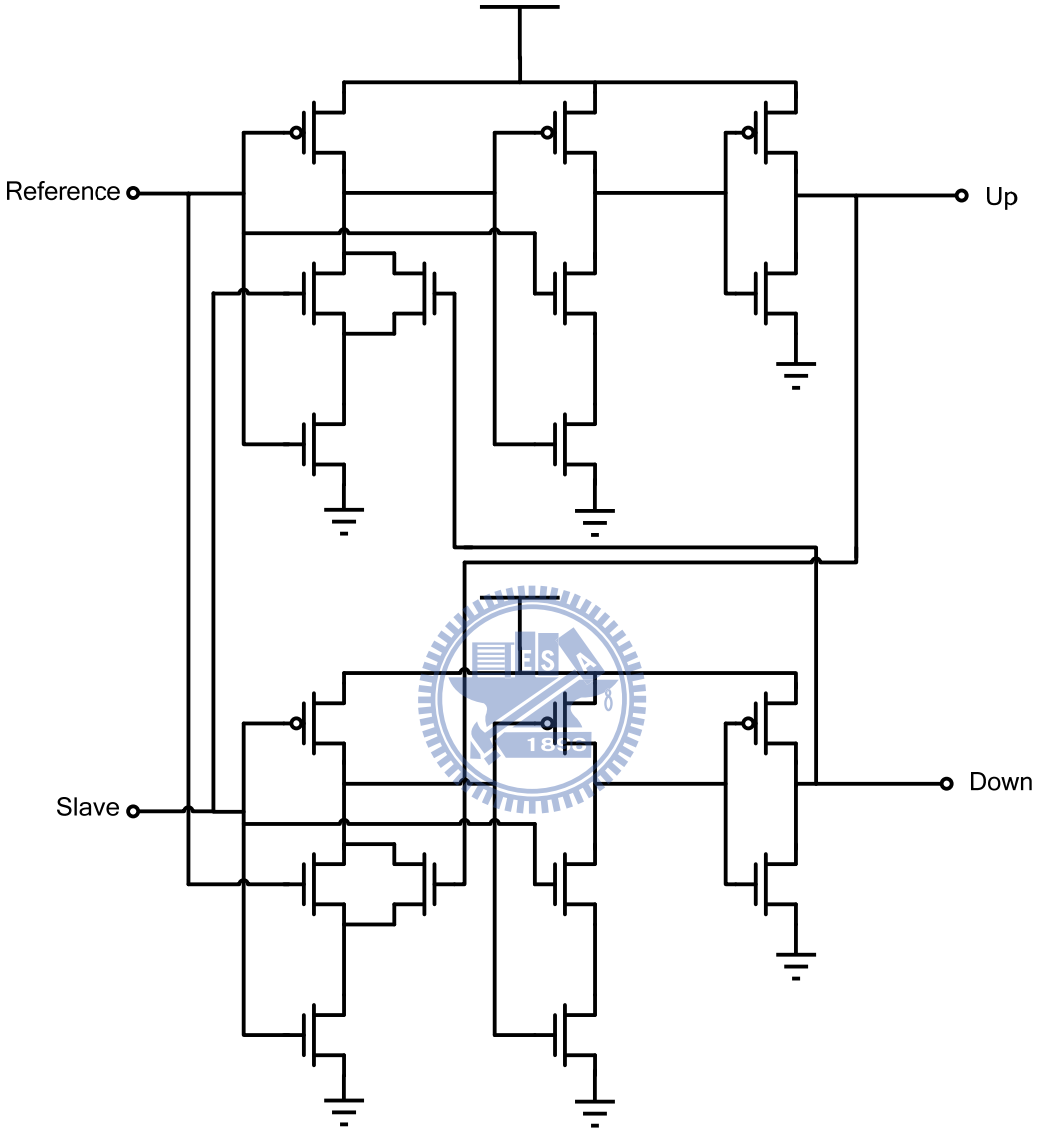


Fig. 3.7 Simplified schematic of precharge-type PFD.

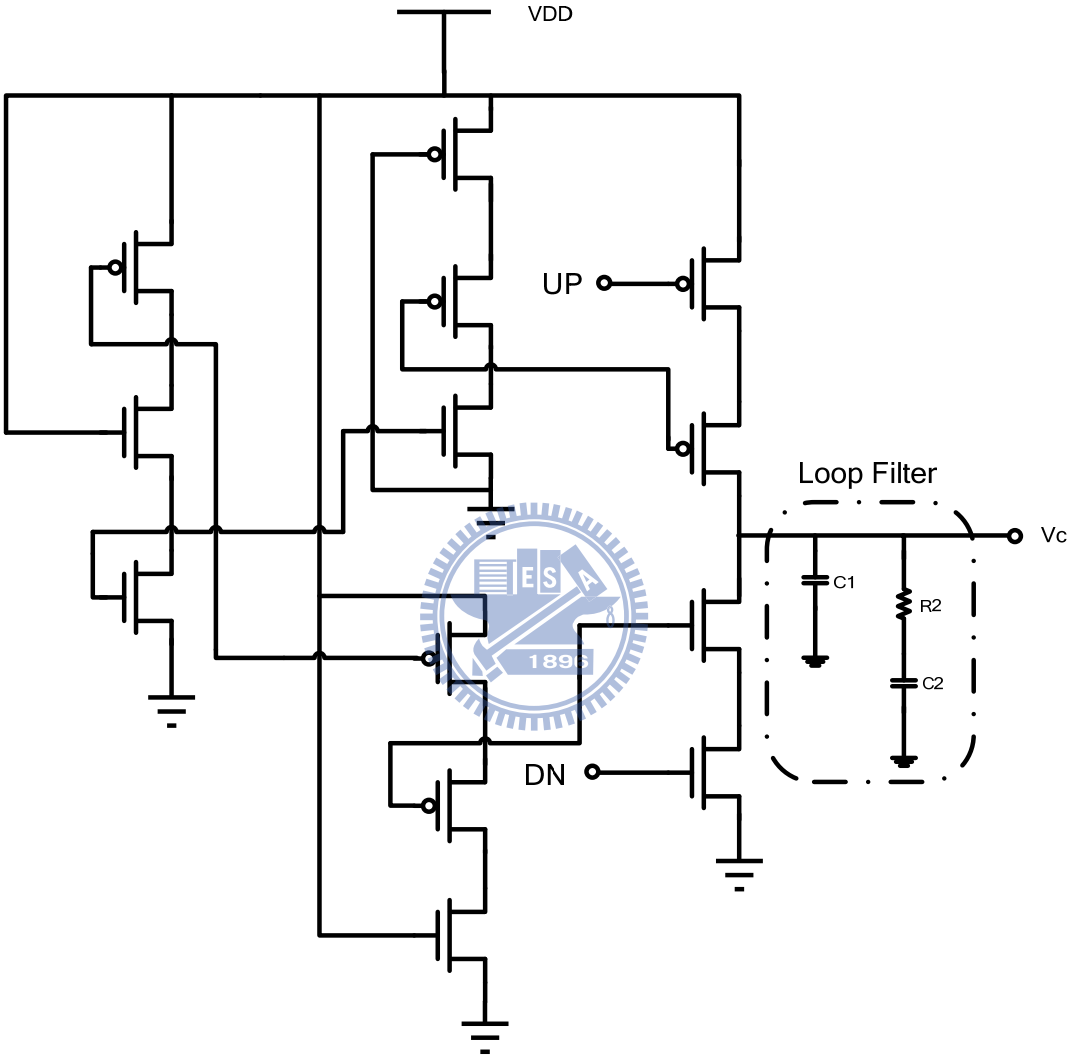


Fig. 3.8 Circuit diagram of the charge pump and loop filter.

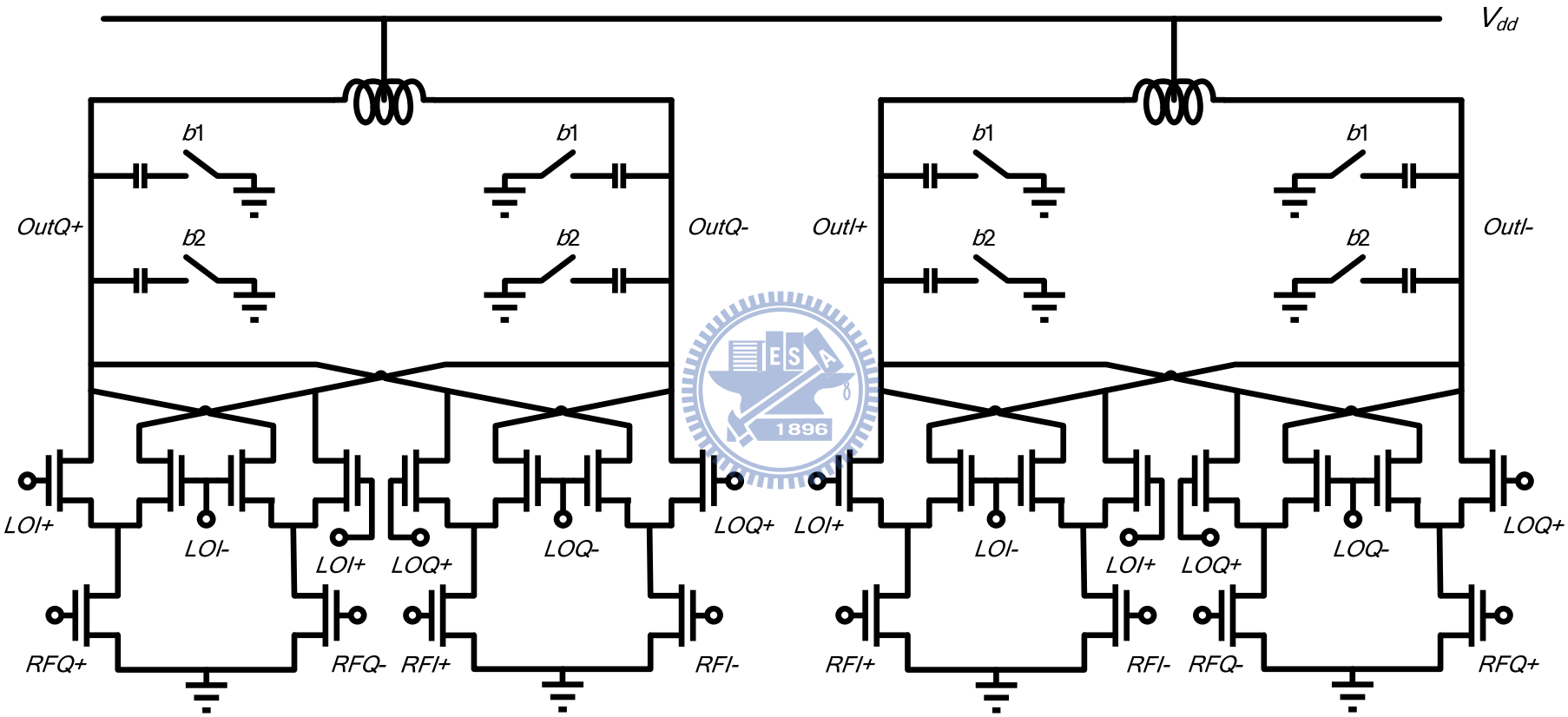


Fig. 3.9 The schematic of the SSB mixer.

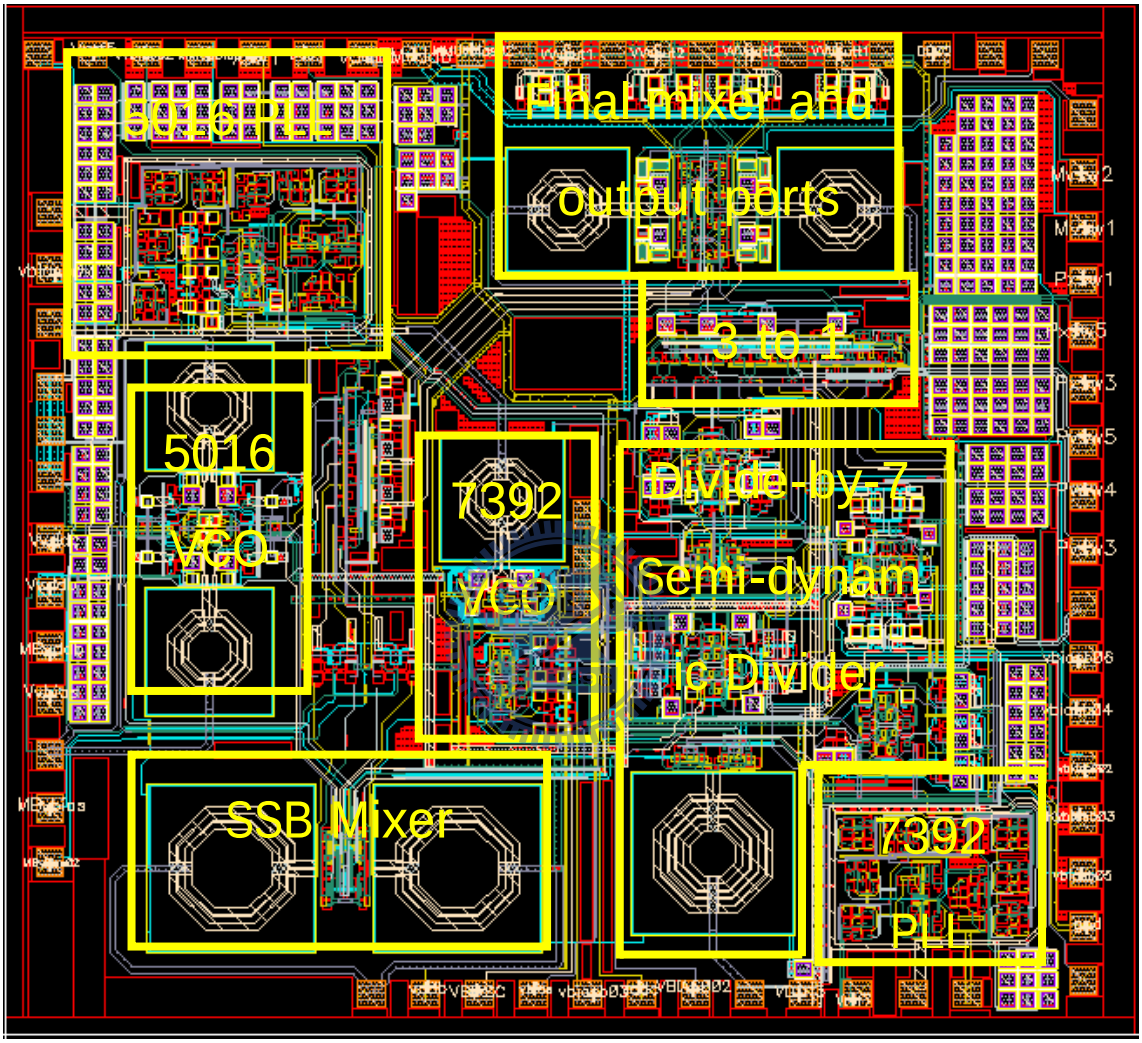
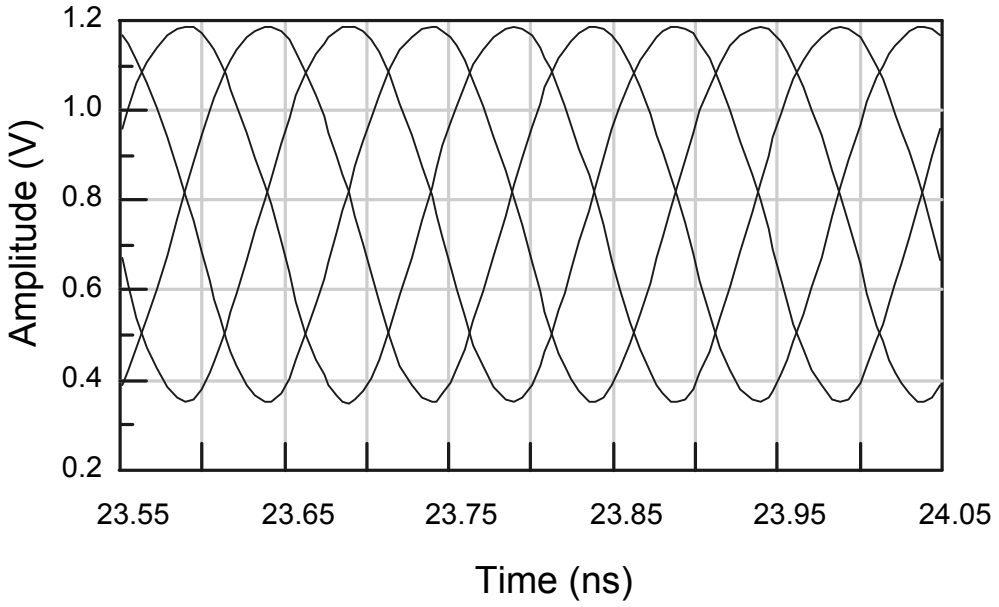
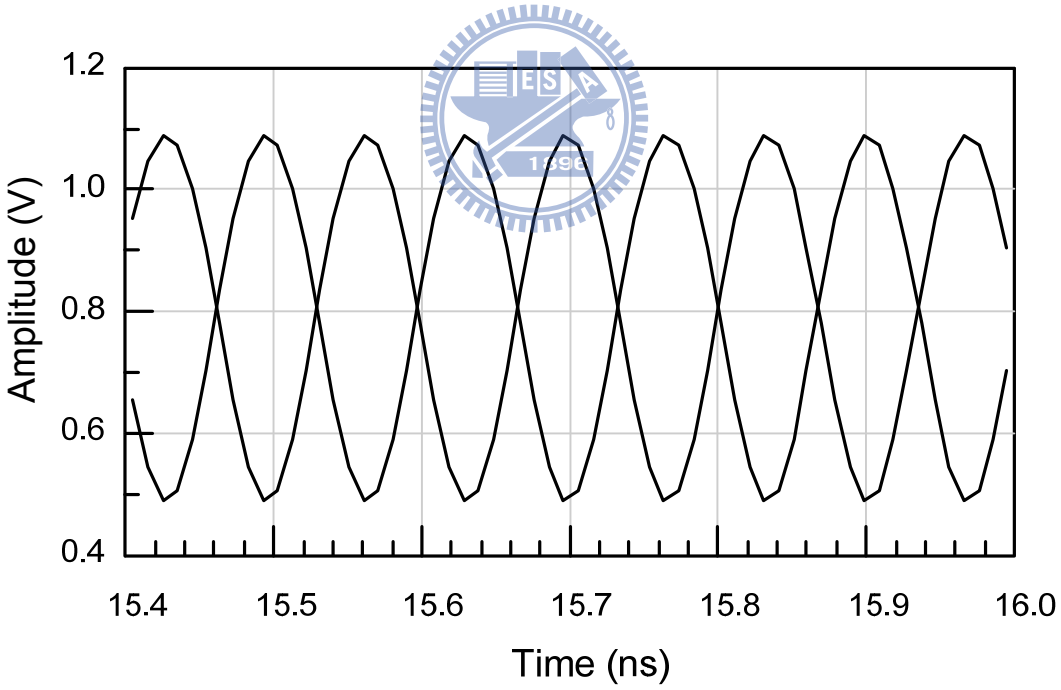


Fig. 3.10 Chip microphotograph of the proposed UWB synthesizer (2.3 × 2.5 mm^2).



(a)



(b)

Fig. 3.11 Simulated waveforms of (a) 5016 MHz QVCO (b) 7392 MHz VCO.

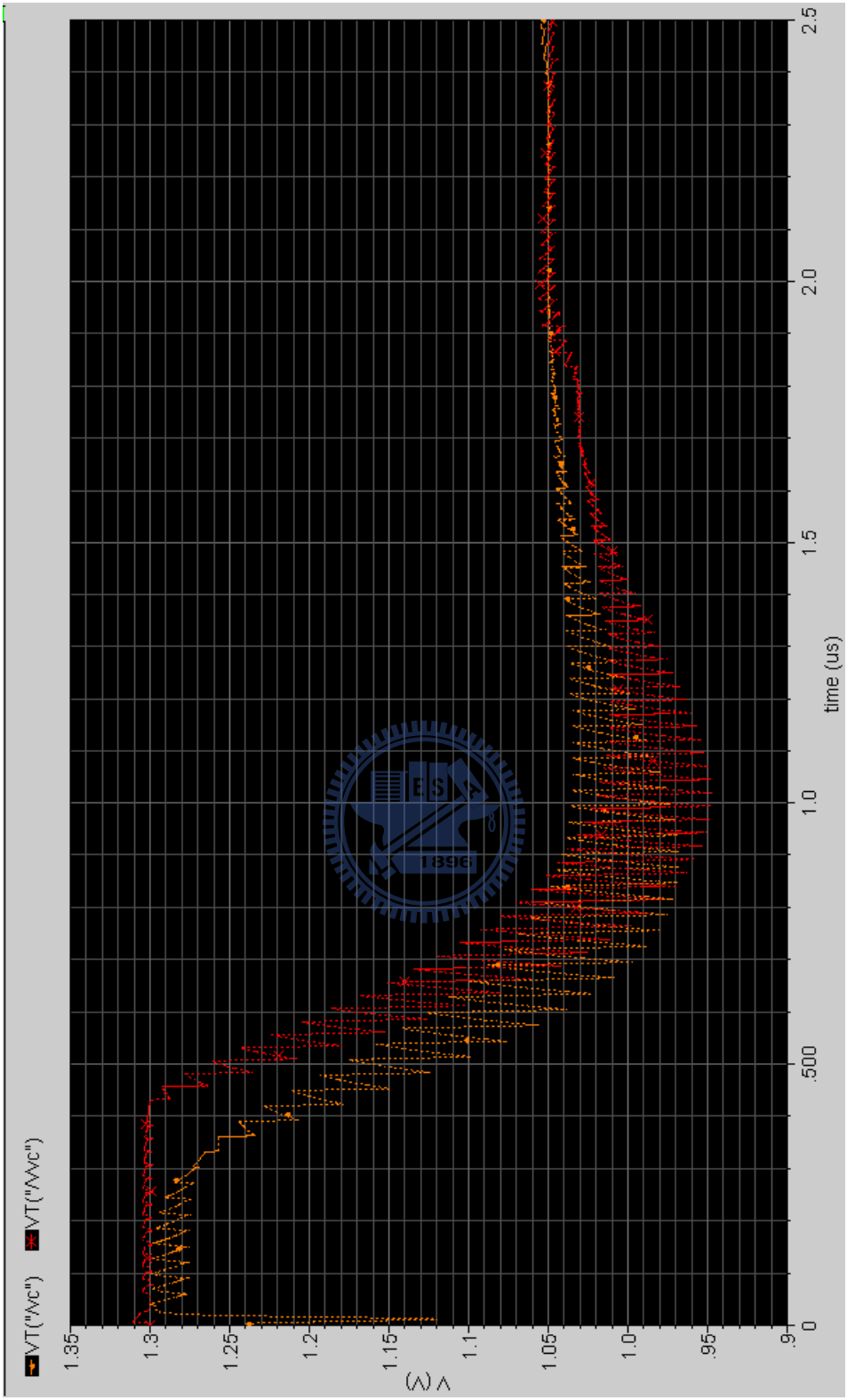


Fig. 3.12 Simulated locking time of the 7.392 GHz PLL and 5.016 GHz PLL by SpectreRF software.

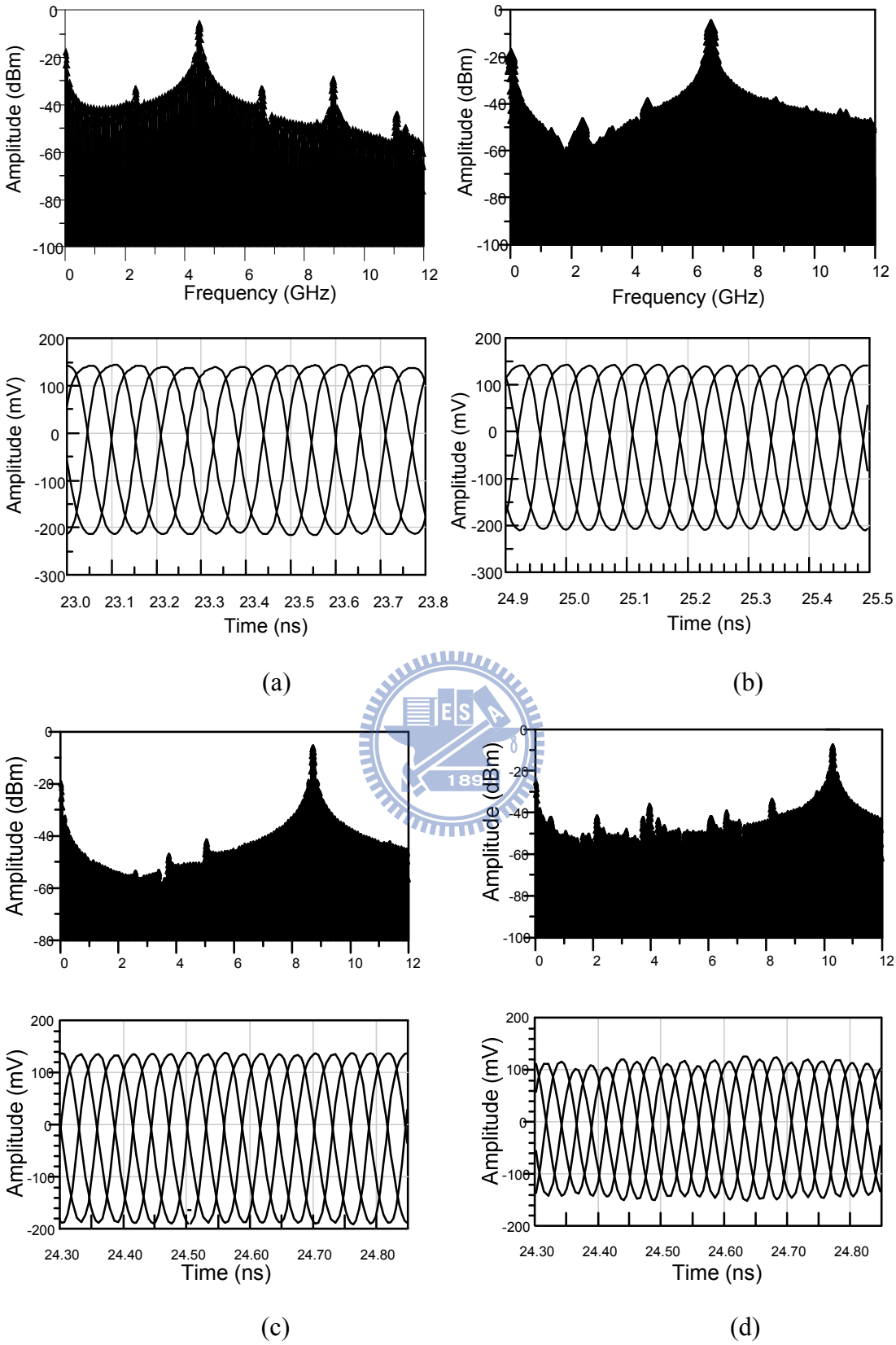


Fig. 3.13 Simulated UWB synthesizer output waveforms and spectrums at (a) 4488 MHz (b) 6600 MHz (c) 8712 MHz (d) 10296 MHz.

CHAPTER 4

DESIGN OF PTAT VCO

In this chapter, we propose an LC-tank VCO with temperature compensation active inductors by using the standard 0.18-μm CMOS process. In order to cancel the temperature effects on the active devices and decrease the area consumption, the active inductor based VCO with temperature-compensation technique is proposed. The lower resonant frequency of the oscillator often gets better phase noise. As shown in Fig. 4.1, the proposed VCO can be applied in the UWB frequency synthesizer by multiplying the frequency with frequency multiplier. The adopted active inductors are composed of MOSFETs in CMOS technology. The threshold voltage V_{THN} and mobility μ_n of these MOSFETs will be affected by the temperature variation, which in turn results in the inductance variation of the active inductors with temperature. The active inductor with temperature compensation current source is proposed in this work to solve the problems.

4.1 ACTIVE INDUCTOR FUNDAMENTAL

In recent years, with the development of wireless personal communication system, low cost and high integration process technologies are required for the integrated circuit designers. There are many passive components used to realize on-chip radio frequency integrated circuits (RFICs), as like as the resistors, capacitors and inductors. The passives usually occupy a large area of the die size, especially the inductors. There are two distinct types of inductors, i.e., passive and active inductors. In general, the passive inductors have the advantage of consuming no DC power.

However, it is lossy and expensive due to larger physical size at frequencies below X band. Oppositely, the active inductors have the characteristics of compact size and tunable inductance. That makes the active inductors more attractive in integrated circuit designs. The active inductors have been employed in radio frequency integral circuits, as like as LC-tank VCO [47]–[50], filters, power divider, multiplexer, quadrature generator, low noise amplifier, phase shifter, etc. The proposed active LC-tank VCO is shown in Fig. 4.2. The LC-tank is composed of two active inductors and parasitic capacitance. The cascode-grounded active inductor is employed in the proposed VCO, and no varactors are used. According to the Barkhausen criteria, for oscillations to occur, the loop gain must be unity and the phase shift around the loop should be a multiple of 360^{o}. The transistors M_7 and M_8 shown in Fig. 4.2 provide a negative conductance to replenish the power loss dissipated by the differential LC-tank. Active inductors are formed by M_1–M_3 (M_4–M_6), and the transistors M_N and M_P are the current sources of the active inductors. V_P and V_N are the biasing voltage of the current source. The inductance of the active inductor could be varied by tuning the controlling voltage V_{tune}. The gyrator–C topology is adopted for the active inductor, which is composed of a gain and a feedback element to transfer the capacitive impedance into inductive impedance [51]. As shown in Fig. 4.2, transistors $M_1 - M_3$ ($M_4 - M_6$) are employed to establish a back-to-back transconductor stage, where M_1 (M_4) is a common-drain stage, functioned as the feedback element, and M_2–M_3 (M_5–M_6) comprises a cascode stage, which is the gain element. The transistor M_3 (M_6) is used to be a gain-booster, with a control voltage V_C. The inductance of the active inductor could be controlled by varying the transconductance of M_3 (M_6).

The inductance L_{TC} of the proposed temperature compensation active inductor could be written as

$$L_{TC} = \frac{C_p}{g_{mPTAT} \times g_{mMOSFETs}} \tag{4.1}$$

where g_{mPTAT} represents the transconductance of M_1 (M_4), which is biased by the PTAT current source M_{13} (M_{14}). And $g_{mMOSFETs}$ is the transconductance of $M_2 - M_3$ ($M_5 - M_6$) that are biased by the normal inversely proportional to absolute temperature (NTAT) current source M_{P1} (M_{P2}). Note that the required capacitance of a typical gyrator-C active inductor is provided here by the parasitic capacitance C_p without adding an additional MIM capacitor. The parasitic capacitance of the negative conductance and the active inductors is paralleled with the coupled capacitors of the output buffers to compose the LC-tank oscillator.

4.2 TEMPERATURE EFFECTS ON ACTIVE INDUCTOR

The Process-Voltage-Temperature (PVT) variations can be considered in the design process, but the inductance variation resulted from temperature variation is unavoidable for active inductors. Take an LC-tank oscillator for example. The inductance variation will lead to a varied free running resonant frequency. Furthermore, the large frequency variation might make the phase locked loop out of lock, and fail the circuit. The more the temperature varied, the more the inductance shifted. Too much temperature variation will contribute to the circuit abort at operation frequency range. It makes the active inductor and its implemented circuits become unpractical. The temperature effect of the inductance, and thus the oscillating frequency, comes from the variation of the transconductances with temperature. The transistor M_{P1} (M_{P2}) is the current source of the cascode stage $M_2 - M_3$ ($M_5 - M_6$), which determines the transconductance $g_{mMOSFETs}$. The drain current $I_D(T)_{MOSFETs}$ of

M_{P1} (M_{P2}) depends on the mobility μ_n and the threshold voltage V_{THN}, which are strong functions of temperature [52]. Here M_{P1} (M_{P2}) is biased in the saturation region with drain current expressed as

$$I_D(T)_{MOSFETs} = \frac{\mu_n(T)\cdot C_{ox}}{2}\cdot\frac{W}{L}\cdot[V_{GS} - V_{THN}(T)]^2 . \tag{4.2}$$

The threshold voltage V_{THN} and mobility μ_n are with negative temperature coefficients. It means that $V_{THN}(T)$ and $\mu_n(T)$ will decrease as the temperature is increased. Normally, there are two operation modes for the drain current. The first one is with low V_{GS}, which has a V_{GS} near $V_{THN}(T)$. And then the drain current shown in (4.2) will be dominated by $V_{THN}(T)$. The second operation mode is with high V_{GS}, and drain current is dominated by the mobility $\mu_n(T)$ because V_{GS} is much larger than $V_{THN}(T)$. The adopted current source of the active inductor in this work is operated in saturation and high V_{GS} region. Therefore, the temperature effect of the current source is dominated by the mobility $\mu_n(T)$, and the drain current will decrease according to the increased temperature. Note that the decreased drain current will lead to a decreased transconductance, which in turn results in an increased inductance from (4.1), or a lower oscillating frequency of the LC-tank. On the other hand, the transconductance g_{mPTAT} is controlled by the current source M_{13} (M_{14}), which is mirrored by the PTAT current source that composed of a couple of the connected base-collector NPN bipolar junction transistors (B_1–B_2) [53]. The output current of the PTAT current source could be expressed as

$$I_D(T)_{PTAT} = \frac{W_{13}}{W_{12}}\cdot\frac{k\cdot T\cdot R_1\cdot\ln(n)}{q\cdot R_2} \tag{4.3}$$

where W is the width of the MOSFETs, k is the Boltzmann constant, q is unit electric charge, and n is the ratio of two p-n junction areas. It shows that the current will get larger when the temperature gets higher.

The increased current from current mirror of PTAT current source is applied to compensate the losing current of the general current source used in active inductor when temperature gets higher. The proposed active inductor adopted only one PTAT current source to prevent the current from over-compensating situation. The steady current of the active inductor represents a stable inductance and unvaried resonant frequency of the oscillator. In conclusion, as the temperature increases, the decreased $g_{mMOSFETs}$ can be compensated by increased g_{mPTAT} for stable inductance of the active inductor.

4.3 CIRCUIT DESIGN OF PTAT LC-TANK VCO

Fig. 4.2 shows the schematic of the proposed LC-tank VCO. The oscillator is composed of two active inductors, a negative conductance circuitry, and two common-source buffers for measurement. In order to avoid the problems caused by temperature shift, the active inductor combined with PTAT current source [54]–[55] is proposed to achieve the goal of temperature compensation by keeping the current more stable than the normal current source in different temperatures.

The oscillating frequency ω_0 of the LC-tank can be written as $(L_{TC} \times C_{eq})^{-1/2}$, where the parasitic capacitance C_{eq} is the total parasitic capacitance at points $P-$ or $P+$ (Fig. 4.2).

In order to guarantee the oscillations to occur, the negative conductance of the oscillator is set to double by increasing the MOSFET width, and a tail-current source

I_{tail} is used to control the total current of the VCO core circuit. The common source buffer is used to avoid the influence from external load, and provides a higher output power of the oscillator for measurement.

4.4 EXPERIMENTAL RESULTS

The proposed active inductor VCO was designed and fabricated using the TSMC 0.18-μm CMOS process. The die photo of the proposed circuit is depicted in Fig. 4.3 with a chip size of 670 × 680 μm^2, where the active region occupies 190 × 195 μm^2. All measurements were done at 1.8 V supply voltage and the total power consumption is 19.3 mW, without including that (23.4 mW) consumed in the output buffers.

As shown in Fig. 4.4 and Fig. 4.5, the transconductance g_m of M_1 (M_4) was compensated by the PTAT current source, thus the inductance of the active inductor characterizes a less variation within the operation temperature. And the simulation results of the oscillating frequency, with and without the PTAT current source, are shown in Fig. 4.6. The variation of oscillating frequency improves from 8.72 % to 0.99 % when the temperature varies from –20^{0}C to 60^{0}C. The measurement result is also depicted in Fig. 4.6, which shows good agreement with the simulation. It is obvious that PTAT current source greatly improves the oscillating frequency shift within 80^{0}C temperature variation, and is quite attractive for active inductor-based circuits. The measured tuning range is 48% from 1.76 to 2.87 GHz with a maximum output power of –9.7 dBm. And

The Fig. 4.7 depicts the measured phase noise at 2.4 GHz is in the range between –87 dBc/Hz and –91 dBc/Hz at 1 MHz offset for the considered temperature range. Because there are more transistors used for the PTAT current source, it brings in more

noise than normal one. The proposed VCO is compared with other active inductor VCOs [47]–[50] in Table I. The proposed oscillator occupies minimum active area and works well with good stability on frequency when temperature varies from -20^0C to 60^0C.

4.5 SUMMARY

An LC-tank VCO with temperature compensation active inductors in TSMC 0.18-μm CMOS technology is presented. The frequency variation is less than 1% when the temperature varies from -20^0C to 60^0C, which is a great improvement of the oscillating frequency shift for active inductor-based circuits. The measured phase noise is −91 dBc/Hz at 1 MHz offset at 2.4 GHz. The VCO occupies an active area of only 190 × 195 μm^2 and exhibits a 48% tuning range with a consumed power of 19.3 mW under 1.8 V supply voltage.

Table 4.1
Performance summary of the active inductor VCOs

Reference	this work	[47]	[48]	[49]	[50]
Technology	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Frequency (GHz)	1.7 – 2.8	5.5 – 9.2	2.32 – 2.72	0.5 – 3.0	0.5 – 2
Phase noise @ 1 MHz offset	–91 @ 2.4 GHz	–95 ~ –114	–90.3 ~ –95.2	–118 ~ –101	–78 ~ –90
Tuning range	48 %	58 %	15 %	143 %	120 %
Pdis. (mW)	19.3	12 ~ 31	51.1	6 ~ 28	13.8
Output power (dBm)	–9.7	–24.64 @ 6 GHz	–	–22 ~ –14	–21 ~ –29
Active area (μm^2)	190 × 195	300 × 400	–	150 × 400	300 × 300
Frequency variation	0.99% (–20 ~ 60^{0}C)	< 10% (–55 ~ 125^{0}C)	–	–	–

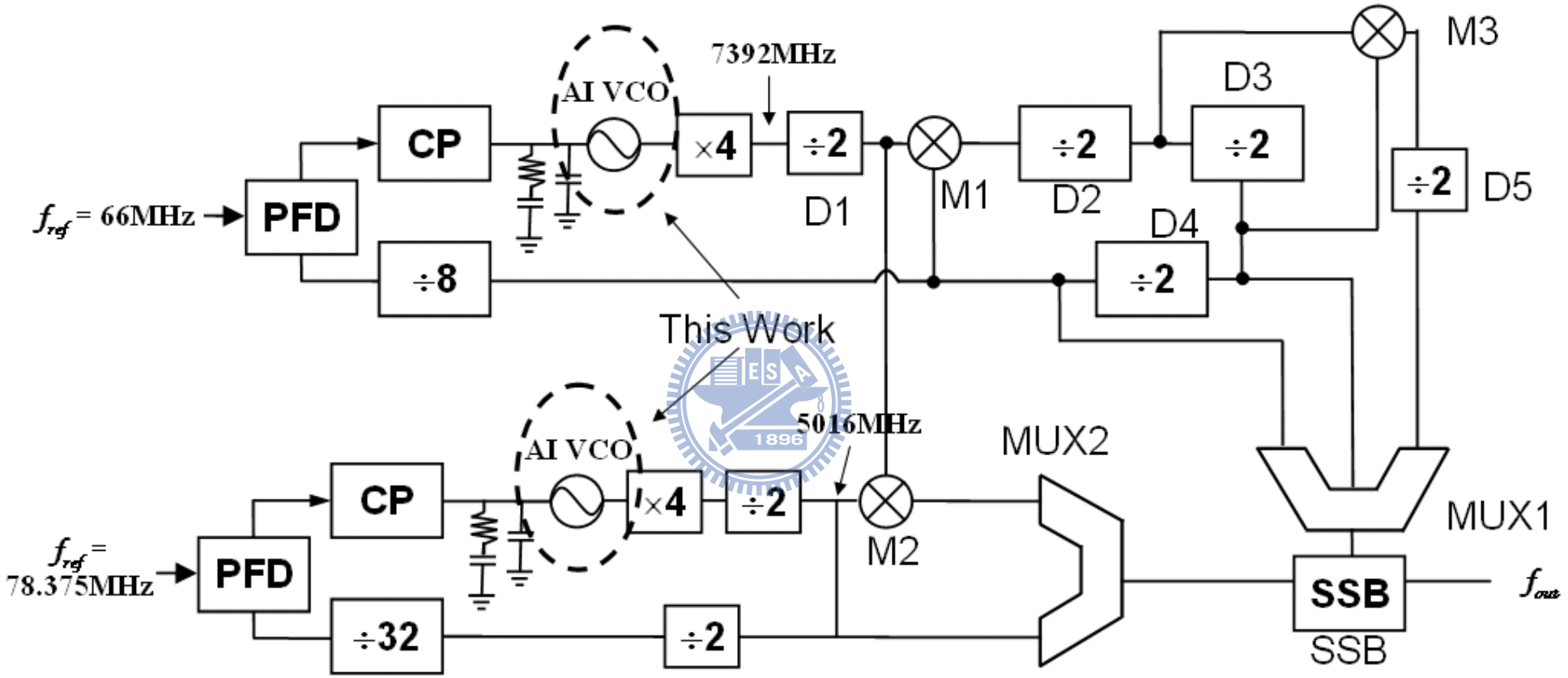


Fig. 4.1 UWB frequency synthesizer with proposed active inductor (AI) based PTAT VCOs.

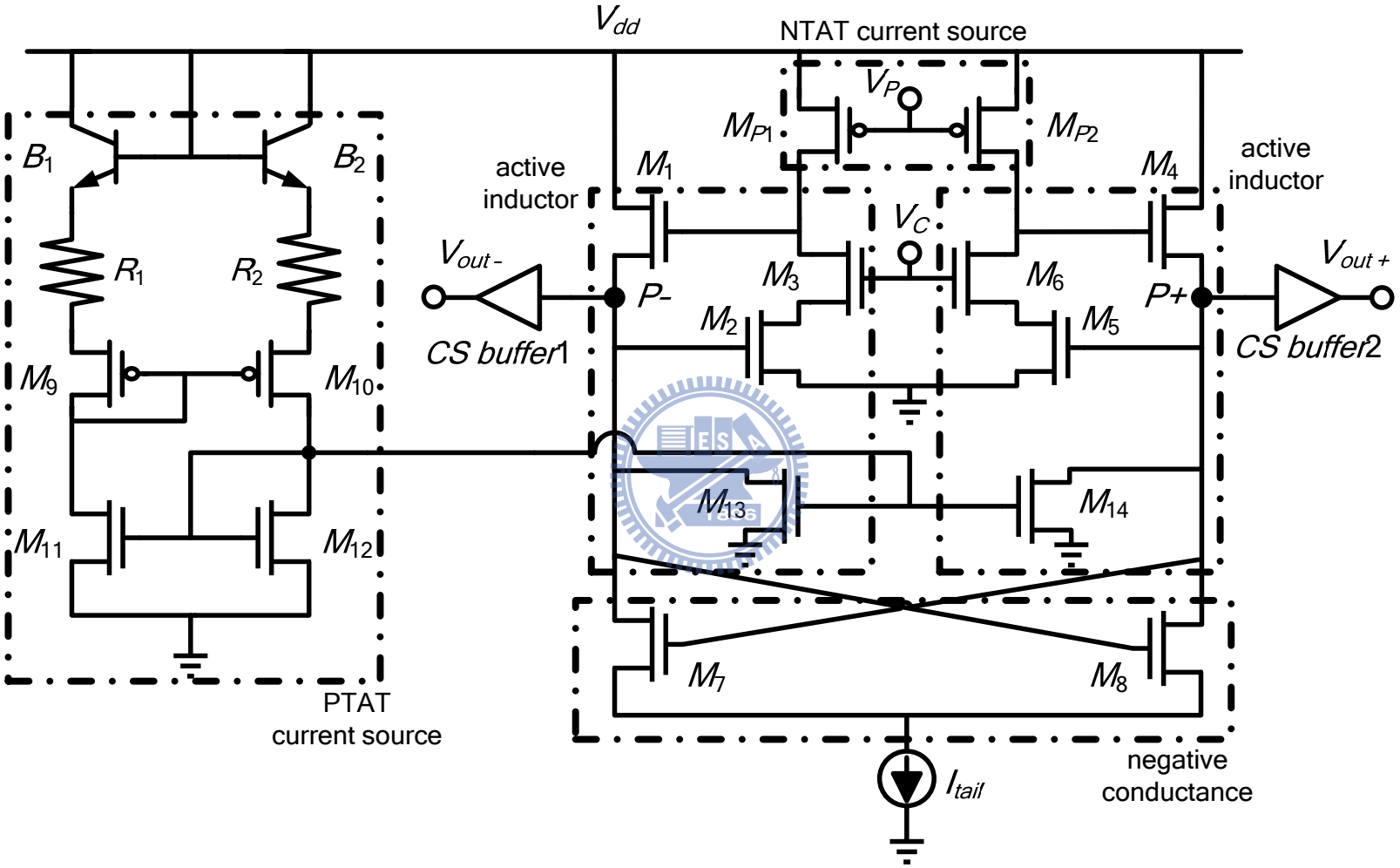


Fig. 4.2 Schematic of the proposed VCO.

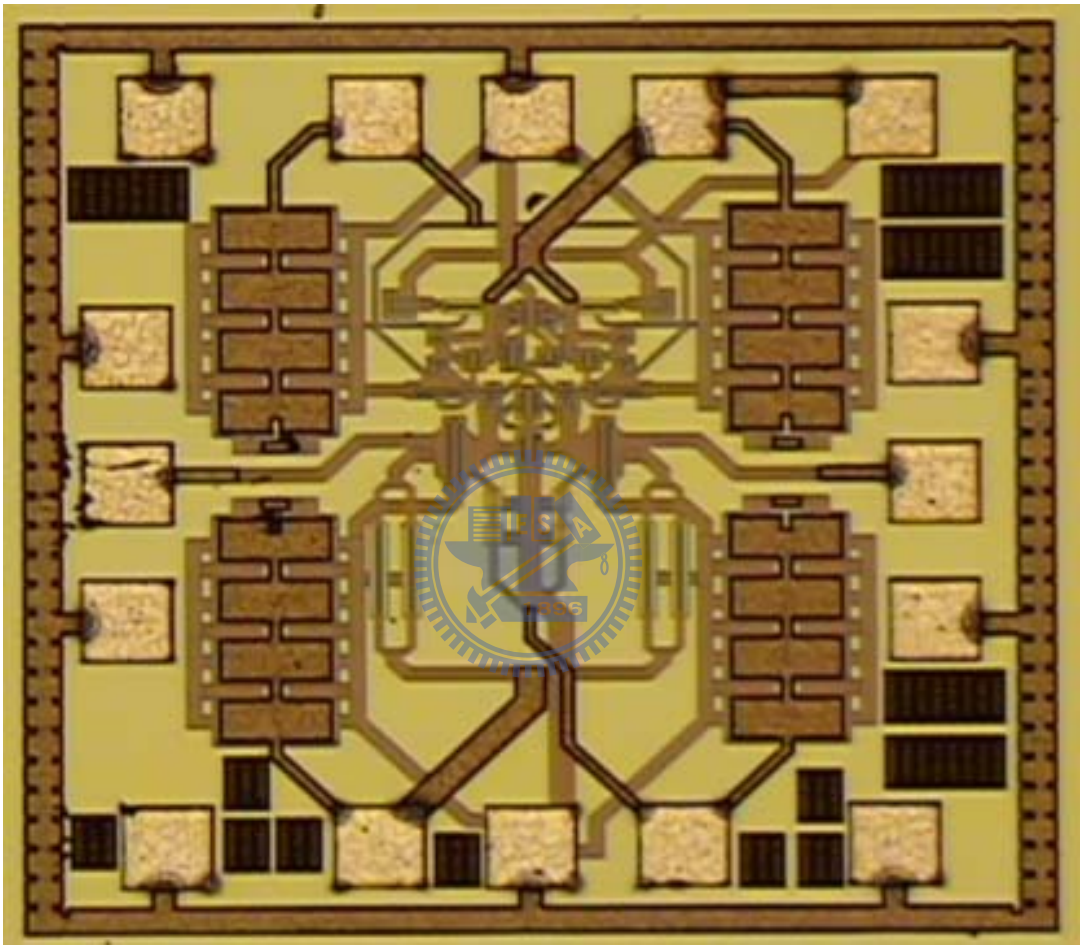


Fig. 4.3 Microphotograph of the proposed LC-tank VCO (size: 670 × 680 μm^2).

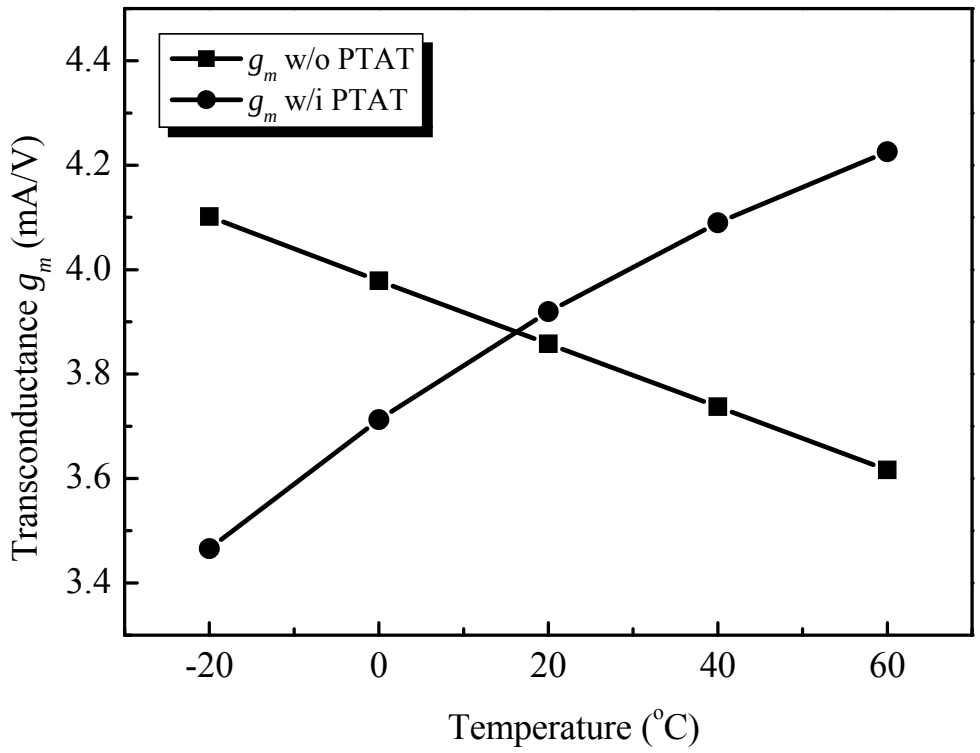


Fig. 4.4 Simulated transconductance g_m of M_1 (M_4) versus the operation temperature.

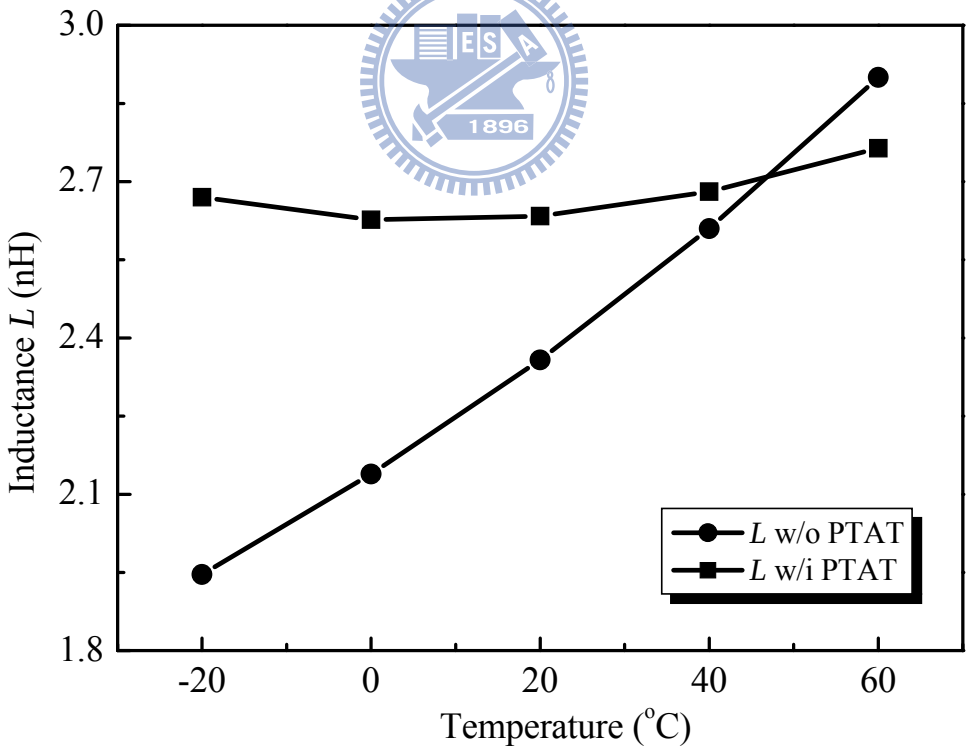


Fig. 4.5 Simulated the inductance L of active inductor versus the operation temperature.

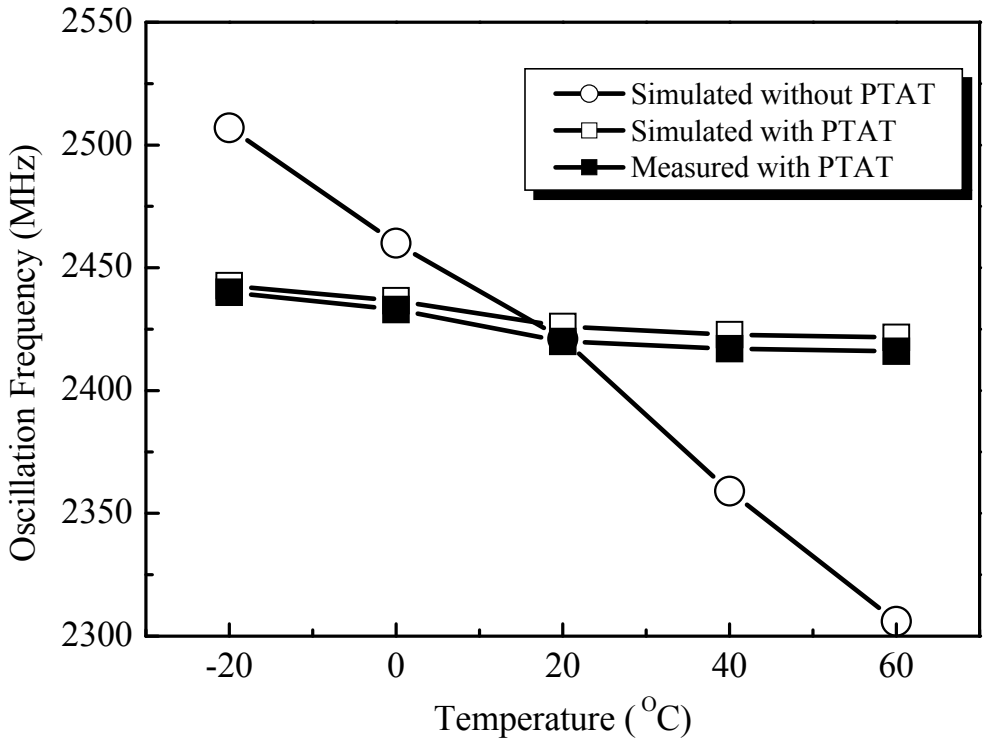


Fig. 4.6 Simulation and measurement results of oscillating frequency versus the operation temperature.

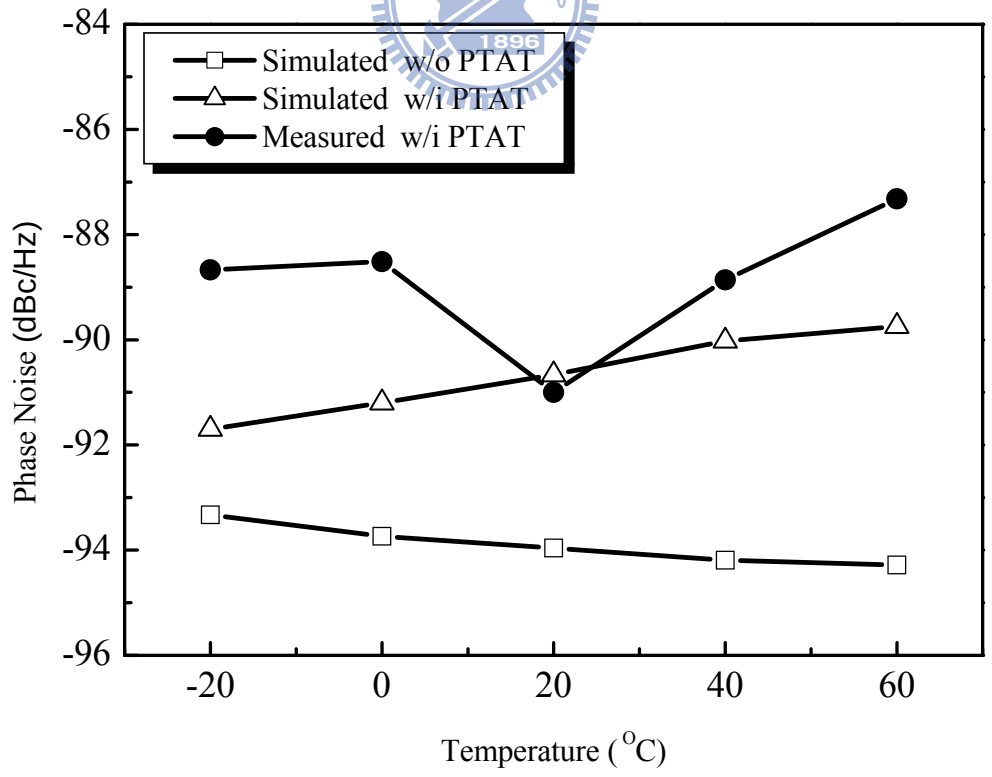


Fig. 4.7 Simulation and measurement results of phase noise at 1 MHz offset versus the operation temperature.

CHAPTER 5

DIVIDE-BY-3 FREQUENCY DIVIDER WITH ACTIVE BALUN

With the growing request for the high data communication capabilities, the 60 GHz UWB system is developed for new consumer applications. The frequency divider is the key component of the PLL. The divide-by-3 frequency divider is proposed to make the PLL architecture more compact.

The frequency divider is a key component of the PLL and frequency synthesizer. The proposed divide-by-3 frequency divider is presented to be the second stage of the frequency divider as shown in Fig. 5.1. In general, the divide-by-2 static frequency divider is the most often used element in the design. However, the divide-by-3 frequency divider can be used to simplify the PLL design with more flexibility. The divide-by-3 injection locked frequency divider (ILFD) has been studied [56]–[57], and the SDFD is also a type of ILFDs.

5.1 OPERATIONAL PRINCIPLES

Based on the Miller divider [43], the circuit diagram of SDFD is composed of a mixer, N stages of CML static frequency divider, and a feedback path to the mixer. The output frequency f_o of the SDFD can be written as

$$f_o = \frac{f_{in}}{2^N \pm 1} \tag{5.1}$$

where f_{in} is the input frequency. The division ration of the SDFD is equal to $2^N \pm 1$, and the signs of plus or minus of the equation can be decided by choosing the down or up conversion of the mixer. Therefore, the double-sideband (DSB) mixer will result in both two output frequencies simultaneously. Furthermore, there is often a low pass filter cascaded with the mixer to choose the wanted frequency. In this work, the proposed divide-by-3 frequency divider, as shown in Fig. 5.2, utilizes a Gilbert mixer together with a divide-by-2 CML static divider to implement a divide-by-3 divider. The static divide-by-2 divider is composed of two latches in a feedback loop. The latch stage is implemented by using the CML, also called source-couple logic (SCL). The conventional CML, as shown in Fig. 5.3, is constructed of a sampling pair M_1–M_2 (M_5–M_6) and a holding pair M_3–M_4 (M_7–M_8) with an inductive load. The complementary clock signals control the current to be switched between the pairs. One the one hand, when the clock signal is high to activate the sampling pair, the track is kept to the output load, which is known as the sampling mode. On the other hand, when the clock signal changes the holding pair into active, the former state will be kept by the positive feedback loop, which is known as the holding mode. In general, the parasitic capacitance at the output node is one of the key to decide the speed of the divider.

5.2 CIRCUIT DESIGN

The completed circuit schematic of the SDFD is shown in Fig. 5.3. It is composed of an active balun [10], and a static frequency divider with an active mixer. First, the compact-size cascode common-gate and common-source (CG & CS) active balun is utilized to replace the large area consumption passive balun in integrated

circuit designs, and it generates differential output signal which characterizes balanced amplitude and phase under single-end input.

Second, the adopted static frequency divider is composed of sampling pairs and latching pairs (M_1–M_8) with an inductive load to convert the current to voltage signal, and the current sources are controlled by the MOSFETs of M_9 to M_{12}, which are also the LO switching stages of the cascode mixer. Furthermore, the CML divider is designed to be able to divide the mixed frequency less than f_{in} to ensure the CML divider also has an additional function of low pass filter.

Third, the cascode mixer is based on Gilbert cell mixer, which is composed of a LO switching stage (M_9–M_{12}) and a RF transconductor stage (M_{13}–M_{14}). The M_9–M_{12} are reused by the Gilbert mixer and the static frequency divider for the same path of DC current, which not only decreases the power consumption, but also makes the circuitry more compact.

Finally, as to the feedback path, the one of differential output signals of the static divider is connected to the LO switching stage of the Gilbert mixer, and then the mixed signal from the mixer is fed into the static frequency divider at points from p_1 to p_4.

5.3 EXPERIMENTAL RESULTS

The proposed SDFD with active balun was designed and fabricated using the TSMC 0.18-μm CMOS process. The die photograph of the fully integrated circuit is depicted in Fig. 5.4 with a chip size of 1.1 × 0.8 mm^2. The effects of the chip pads, bond wires, and transmission lines in the circuit board are taken into consideration in the simulation process of the whole circuitry. All measurements were done at 1.5 V

supply voltage and the total power consumption is 12 mW without taking that consumed by the output buffers into account. The self-oscillation occurs at free running frequency about 7.35 GHz, and the closed loop of the SDFD is satisfied the Barkhausen's criteria. It means that the free running frequency will be decided by the phase shift around the loop while the loop gain is equal to unity. The injection-locked behavior will be observed as long as the input signal is applied at the triple frequency of f_o. The locking range will be increased as the input power level increases, and it was measured using an external injection source applied to the input port of the active balun. Where the injection source was provided by the Agilent 83640B signal generator and the output signal was captured by the Agilent 8564E spectrum analyzer. With an injection power of 0 dBm, the maximum bandwidth of 1080 MHz from 21.48 to 22.56 GHz was obtained. Fig. 5.5 shows the overlapped measurement result of frequency spectrum of the free-running SDFD and the locked SDFD. The sensitivity diagram of the divide-by-3 SDFD is shown in Fig. 5.6.

5.4 SUMMARY

A divide-by-3 SDFD with active balun is presented with the use of the current-reused technique. The presented SDFD is fabricated using the TSMC 0.18-μm CMOS process and the die area is 1.1 × 0.8 mm^2. Current-reused technique has advantages of less DC power consumption and compact circuitry. This technique is adopted by taking the LO switching stage of Gilbert cell mixer as the current sources of static frequency divider. The measurement results revealed a DC power consumption of 12 mW with a locking range form 21.48 to 22.56 GHz.

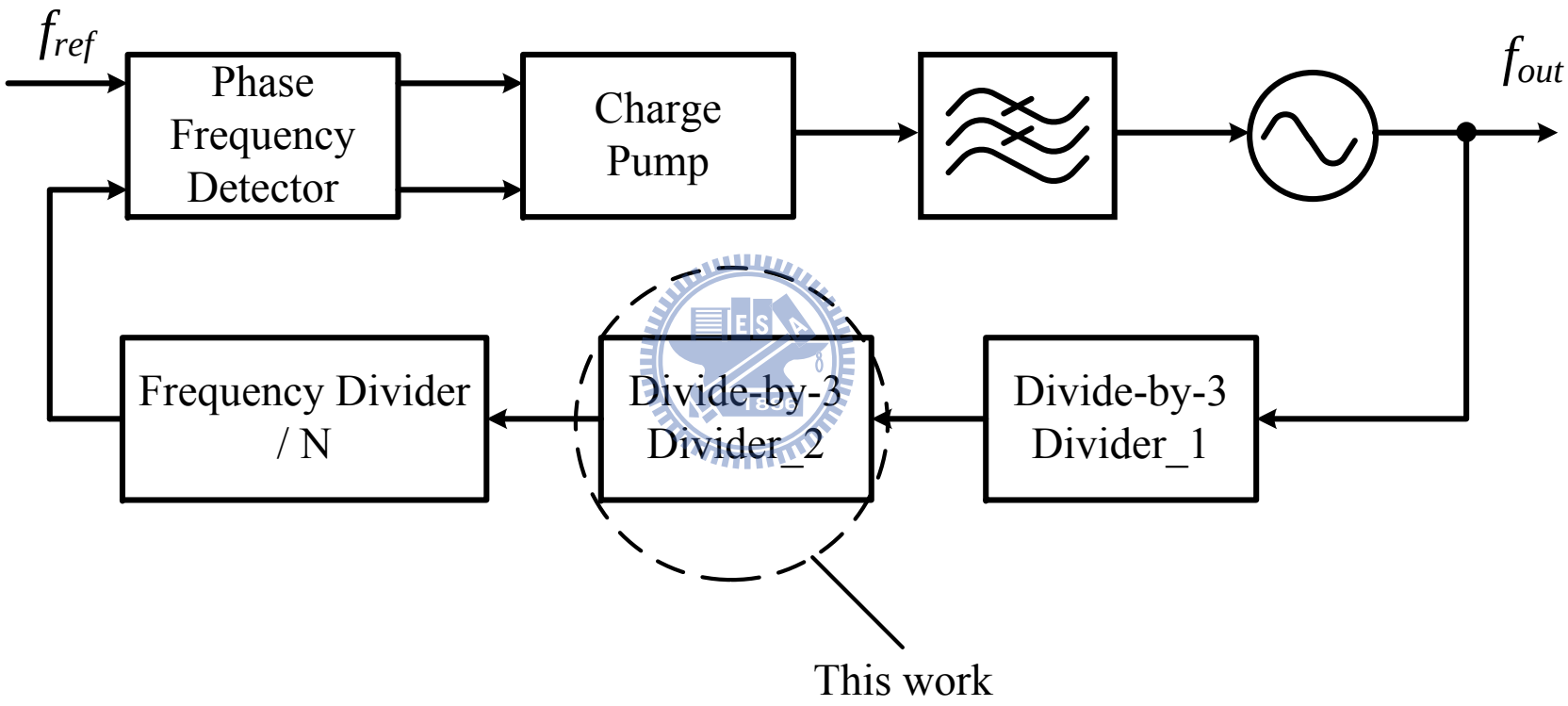


Fig. 5.1 60–GHz UWB PLL with proposed devide-by-3 semi-dynamic frequency divider.

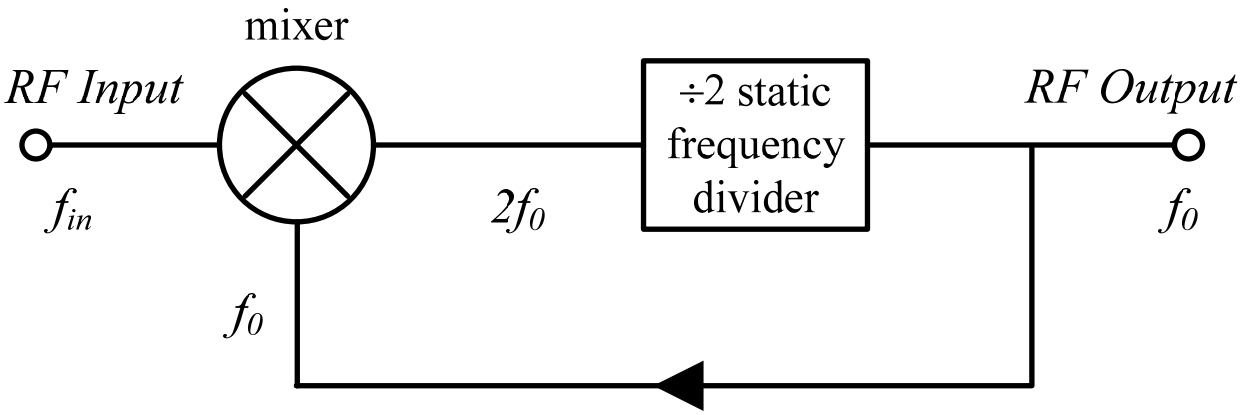


Fig. 5.2 Divide-by-3 semi-dynamic frequency divider (SDFD).

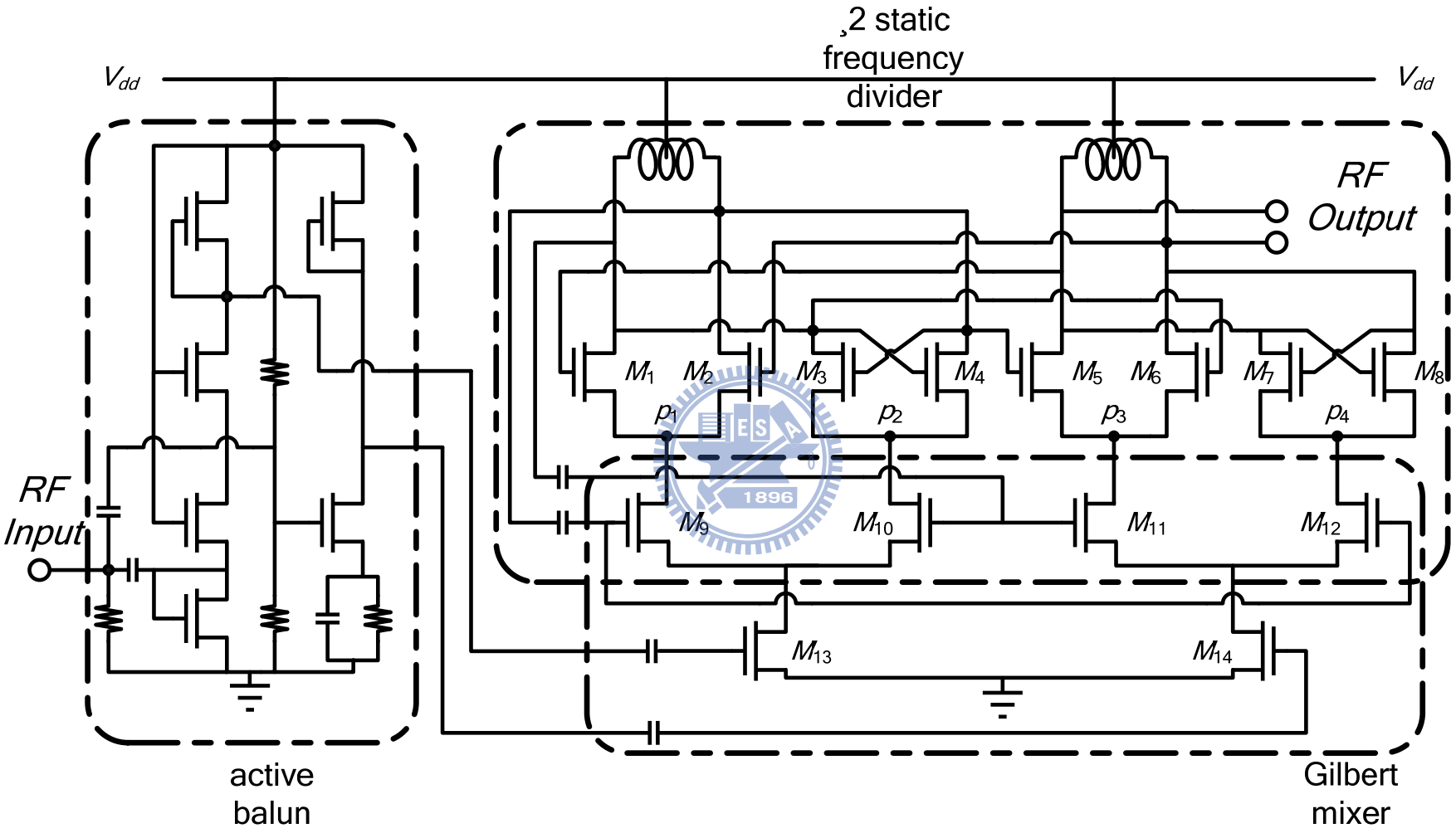


Fig. 5.3 Simplified schematic of the proposed SDFD.

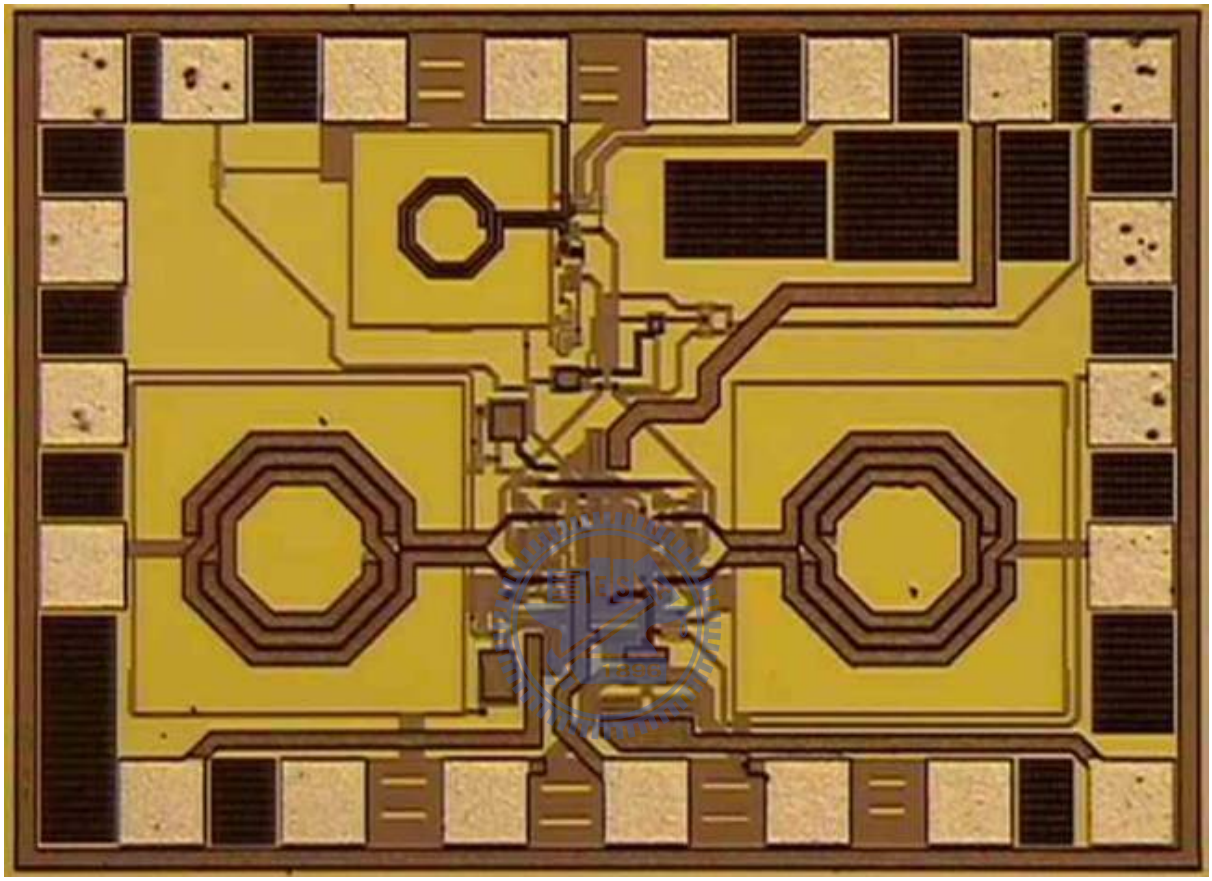


Fig. 5.4 Photograph of fabricated frequency divider, chip size is 1.1 × 0.8 mm^2.

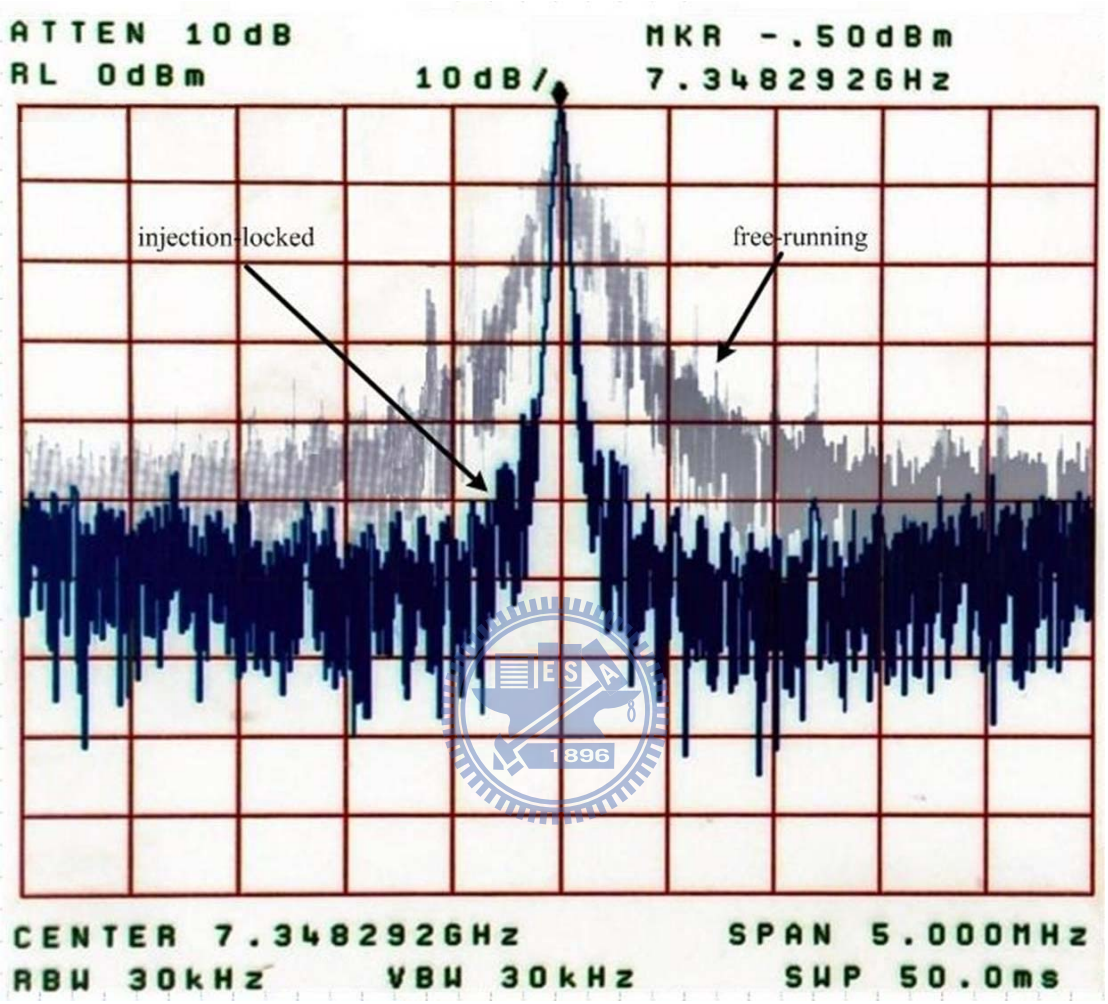


Fig. 5.5 Measured output spectrum of SDFD at 22.045 GHz input.

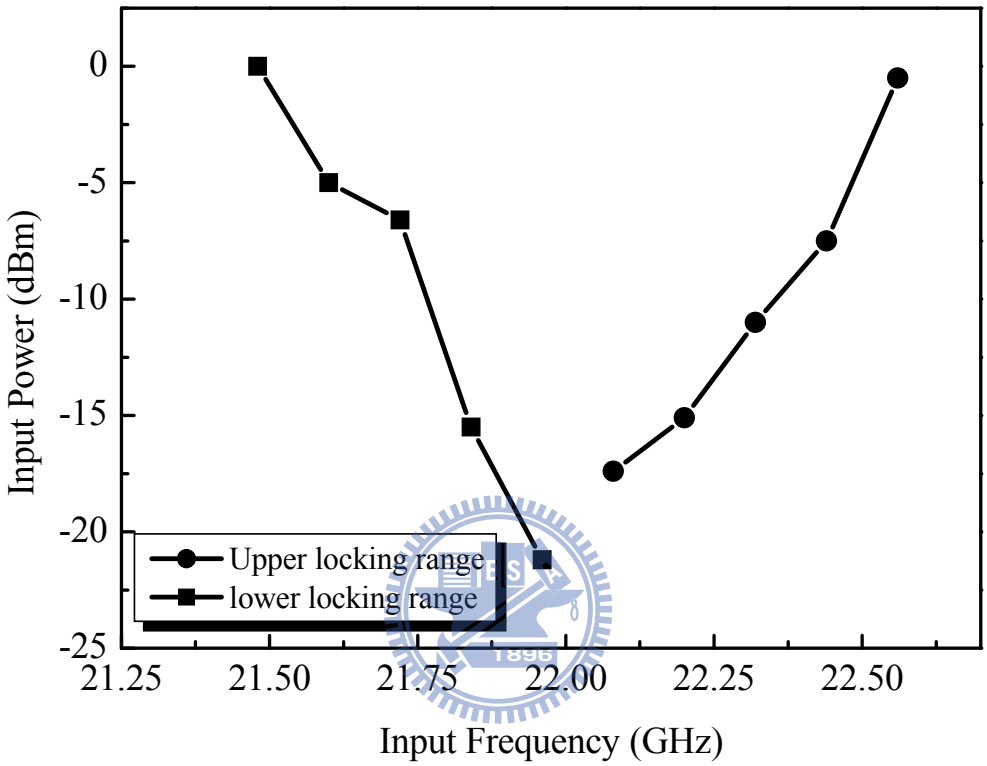


Fig. 5.6 Measured input power versus input frequency of the SDFD.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

In this thesis, the design methodologies and implementations of key CMOS RFICs including wideband down conversion mixers, a frequency synthesizer, an active inductor based PTAT VCO, and a divide-by-3 SDFD for UWB communication systems are proposed.

Firstly, a wideband mixer using LC folded cascode mixer topology and a modified feedforward compensated differential transconductor in TSMC 0.18-μm CMOS technology is presented in the first section of chapter 2. The LC folded cascode method is used to get more voltage headroom, and the feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The linearity is enhanced by a harmonic distortion canceling technique derived from the harmonic balance analysis. The finished mixer core occupies an area of only 0.7×0.58 mm^2 with a consumed power of 14.4 mW under 1.8 V supply voltage. For the second section, a wideband down conversion mixer with active balun is proposed. The cascode CG and CS active balun structure exhibits a broadband performance, which provides balance signals for mixer core from single input. The finished mixer core and active baluns possess good linearity, wide bandwidth, and occupy an area of only 0.85×0.57 mm^2 with a consumed power of 25.7 mW under 1.8 V supply voltage, which is suitable for application in various wireless communication systems.

Secondly, a frequency synthesizer with the SDFD for UWB communication system is proposed and designed. The synthesizer consists of: 1) two PLLs for frequency generation; 2) a divide-by-7 SDFD to generate several frequencies; and 3)

wideband SSB with capacitor switches. The proposed SDFD circuit is introduced to divide the frequency by seven and co-designed with the PLL. As can be seen from the simulation results, the SDFD has the ability to generate several different frequencies to mix for the 14 output bands. The designed CMOS synthesizer has full-band output with −7.6 dBm output power and 111 mW DC power consumption. The proposed synthesizer structure provides a solution to the low-power and high-performance LO. Therefore, the proposed synthesizer is a favorable choice for use in UWB applications.

Thirdly, an LC-tank VCO with temperature compensation active inductors in TSMC 0.18-μm CMOS technology is presented. The frequency variation is less than 1% when the temperature varies from -20^0C to 60^0C, which is a great improvement of the oscillating frequency shift for active inductor-based circuits. The measured phase noise is −91 dBc/Hz at 1 MHz offset at 2.4 GHz. The VCO occupies an active area of only 190 × 195 μm^2 and exhibits a 48% tuning range with a consumed power of 19.3 mW under 1.8 V supply voltage.

Finally, a divide-by-3 SDFD with active balun is presented using the current-reused technique. The presented SDFD is fabricated using the TSMC 0.18-μm CMOS process and the die area is 1.1 × 0.8 mm^2. Current-reused technique has advantages of less DC power consumption and compact circuitry. This technique is realized by taking the LO switching stage of Gilbert cell mixer as the current sources of static frequency divider. The measurement results presented a DC power consumption of 12 mW with a locking range form 21.48 to 22.56 GHz.

In summary, the CMOS RFICs can be operated with good performance in the UWB systems. Nowadays it is evident that the need for high data rate electronic applications is growing. To meet the demand for high data rate, the applications of UWB system, therefore, will be a better solution.

Future research will be focused on the integration of other RF components to form all-CMOS UWB systems. The active inductor will be applied widely in the future design because the die area is directly related to the cost when the circuits are implemented. Lowering the supply voltage less than 1.2 V will be able to decrease the total power consumption, which gets more flexibility for the electronic application. The aim of future research is to develop low-cost, high-performance, and high-frequency transceiver front-ends.

APPENDIX

Abbreviation	Full name
ADS	Agilent Advanced Design System
AI	Active Inductor
CGCS	Common-Gate Cascaded with Common-Source
CML	Common-Mode Logic
CP	Charge Pump
DSB	Double-Sideband
FCC	Federal Communications Commission
GPRS	General Packet Radio Service
GSM	Global System for Mobile
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
IIP_2	Second-order Input Intercept Point
IIP_3	Third-order Input Intercept Point
ILFD	Injection Locked Frequency Divider
IMD3	Third-Order Intermodulation Distortion
IP_{1dB}	Input 1-dB Compression Point
LF	Loop Filter
LO	Local Oscillator
MB-OFDM	Multi-Band Orthogonal Frequency Division Multiplexing
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
NTAT	Normal Inversely Proportional to Absolute Temperature
PCS	Personal Communication System
PLL	Phase Locked Loop
PTAT	Proportional To Absolute Temperature
PVT	Process-Voltage-Temperature
RFICs	Radio Frequency Integrated Circuits

SCL	Source-Couple Logic
SDFD	Semi-Dynamic Frequency Divider
SSB	Single-Side Band
TSPC	True Single Phase Clocking
UWB	Ultra-WideBand
VCO	Voltage-Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

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