

新型互補式金氧半類比至數位轉換器架構 之設計與分析

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摘要

由於現今在視頻及通訊應用領域中，類比及數位資料傳輸或介面轉換的速率越來越增加，所以高速類比數位轉換器的設計變成了一個新的挑戰。針對於此本論文提出並分析了數種新的高速 CMOS 電流模式類比至數位轉換器架構，用以突破傳統電流式類比數位轉換器的操作速度瓶頸。論文中包含了 (1) 利用電壓取樣及電流處理之開迴路導管式類比數位轉換器，(2) 電流式全波動導管式類比數位轉換器，(3) 電流式非直接傳輸波動導管式類比數位轉換器。

(1) 首先本論文提出並分析了一個八位元 CMOS 導管式類比數位轉換器的新架構。為了達到高速的轉換速率，此新架構採取了電壓模式開迴路取樣電路且用電流式電路來完成訊號相減、附屬數位類比轉換器操作及訊號比較等動作。因為電流模式取樣保持電路是電流模式導管式類比至數位轉換器的速度瓶頸，所以在提出的架構中是用電壓取樣保持電路來代替原來的電流模式取樣保持電路。又由於訊號相減的動作是使用電流模式的方法，所以可避免使用傳統電壓模式閉迴路電路，進而改進類比數位轉換器的操作速度。尤甚者，此新架構亦採用電流操縱式的方法來改進其附屬數位類比轉換器的速度。根據模擬的結果顯示，此新型導管式類比數位轉換器架構可在取樣頻率為 71.4 MS/s 時，達到八位元精確度。在 3.3V 供應電壓下，其所消耗的功率為 205 mW，所使用的製

程為 1P5M 0.25 μm CMOS 技術。在量測結果方面，因為開迴路電壓取樣電路有增益誤差問題及電流比較器會有輸入訊號偏移問題，所以差動線性度與絕對線性度只能分別維持在 $+1.9/-1$ 與 $+/-2.8$ LSB 以下。同時動態測試顯示在取樣頻率 40 MS/s 操作下，其有效位元數只能達到 6.2 位元。相信在未來的研究，針對開迴路電壓取樣電路的增益誤差及電流比較器的輸入訊號偏移等問題有所改善，將會大大改善其特性。

(2) 針對電流式類比數位轉換器，本論文提出並分析了一個新型高速電流波動導管式類比數位轉換器 (WP-IADC) 架構。在此新型 WP-IADC 架構中，波動導管理論被應用在整個類比數位轉換器導管架構中，形成一個電流式全波動導管式類比數位轉換器 (FWP-IADC)。不同於以往傳統電流式導管式類比數位轉換器，在新型 FWP-IADC 架構中，完全沒有使用電流切換 (switched-current) 電路或電流取樣保持 (current sample-and-hold) 電路。大體而言，所提出的 FWP-IADCs 具有高取樣速率、高輸入頻率、高效率的時脈使用等數個優點。同時因為整個資料路徑沒有採用電流切換電路，所以電流切換電路造成的非線性失真可以避免。

根據針對提出的 FWP-IADC 新架構所做的理論分析，其最小的取樣週期是正比於電流鏡的本質延遲 (intrinsic delay) 及對每一個波動導管級中電流鏡所增加的上升/下降時間。利用 HSPICE 模擬的結果顯示在符合奈奎司特 (Nyquist) 取樣頻率下，此新架構可達到 55 MS/s 轉換頻率並維持八位元解析度。而當輸入訊號頻率為 3 MHz 時，其轉換頻率可高達 90 MS/s 且維持八位元解析度。為了實驗驗證此新構想的可行性，整個 FWP-IADC 架構亦利用 0.35 μm CMOS 製程所研製，而實驗結果亦成功的說明 FWP-IADC 應用在高速類比數位轉換器領域的可行性。

(3) 最後為了更進一步增加電流式全波動導管式類比數位轉換器 (FWP-IADC) 的轉換速率，本論文提出並分析另一個非直接傳輸波動導管式類比數位轉換器 (ITWP-IADC) 的新架構。因為只要減少電流鏡本身的本質延遲 (intrinsic delay) 或降低每一個波動導管級中電流鏡所增加的上升/下降時間，就可以將新架構中的取樣週期最小化。所以在 ITWP-IADC 新架構中，則將電流切換電路併入原先的波動導管級中，並將

整個波動導管級拆解成數個時脈 (clock) 控制的小區段。因此所提出的 ITWP-IADCs 可以在準確性與速度間得到最佳化。ITWP-IADCs 除了有原先 FWP-IADCs 的優點之外，它也讓電流切換電路的時脈週期有更大的彈性去維持其所需要的精確度。同時跟傳統電流導管式類比數位轉換器比起來，整個資料路徑用了較少的電流切換電路，如此也可以增加其線性度。由 HSPICE 模擬結果顯示，在奈奎斯特 (Nyquist) 取樣頻率下，兩區段的 ITWP-IADC 可達到 77 MS/s 轉換頻率並維持八位元解析度。而對四區段的 ITWP-IADC 而言，在輸入頻率為 16 MHz 的情況下其取樣頻率可達到 130 MS/s。可預期的是如果電流鏡的本質延遲及電流比較器的處理時間能更進一步縮小的話，整個四區段 ITWP-IADC 在輸入頻率為 19.2 MHz 的情況下其轉換速率可達到 166 MS/s。

總而言之，本論文所發展出的新的電流模式類比數位轉換器架構，均以模擬及實驗證實其能達到高速操作的目的。且於性能上均較傳統電流式類比數位轉換器有重大的突破與改進。我們相信，於類比數位轉換器設計上，本論文所提出的新架構乃為另一種頗具前瞻可行的設計方法，同時亦於此研究領域開啟了新的視野。




The Design and Analysis of New Architectures for CMOS Analog-to-Digital Converters

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ABSTRACT

The logo of National Chiao Tung University is a circular emblem with a gear-like border. Inside the circle, there is a stylized building and the year '1896' at the bottom. The word 'ABSTRACT' is overlaid on the logo.

Recently, in video and communications applications, the transfer rate of data between analog and digital domains continues to increase, creating new challenges in the design of high-speed analog-to-digital converters. In this thesis, new architectures for high-speed CMOS current-mode analog-to-digital converters (IADCs) are proposed and analyzed to overcome the speed limitations in the conventional IADCs. The proposed IADCs include: (1) a pipelined ADC that uses the open-loop voltage-mode sampling and current-mode processing techniques; (2) a full wave-pipelined current-mode ADC (FWP-IADC); (3) an indirect transfer wave-pipelined current-mode ADC (ITWP-IADC).

At first, a new structure of 8-bit CMOS pipelined analog-to-digital converter (ADC) is proposed and analyzed. In order to achieve a high conversion rate, the proposed new structure adopts voltage-mode open-loop sampling circuit and current-mode circuits to perform subtraction, sub-DAC operation, and comparison. Since the switched-current (SI) sample-and-hold circuits is the speed bottleneck of the current-mode pipelined ADCs, the

voltage-mode circuit instead of SI circuits is used to realize the input sample-and-hold function. Due to current-mode subtraction operation, the closed-loop circuit can be avoided to improve the speed performance. Moreover, current steering sub-DAC is used to enhance the sub-DAC speed. From the simulation results on the demonstrative example, the proposed pipelined ADC architecture can achieve 8-bit accuracy with a sampling rate up to 71.4MS/s. The power dissipation of the pipelined ADC is 205mW at the conversion rate of 71.4 MS/s with a single 3.3V power supply and 1P5M 0.25 μ m CMOS process technology. Due to the effects of gain error in the sample-and-hold circuit and the input offset current in the current comparator, the measured differential nonlinearity (DNL) and integral nonlinearity (INL) for all codes are less than +1.9/-1 LSB and + 2.8/-2.8 LSB, respectively. In the experimental chip, the dynamic test shows that the effective number of bit (ENOB) is 6.2-bit under 40-MSample/s sampling rate.

Secondly, a new architecture for high-speed CMOS wave-pipelined current-mode A/D converters (WP-IADCs) is proposed and analyzed. In the new WP-IADC architectures, the wave-pipelined theory is applied to the pipeline structure, called full WP-IADC (FWP-IADC). In the FWP-IADC, each stage uses the full current-mode wave-pipelined structure without inter-stage SI cell circuits. Generally, the proposed FWP-IADCs have the advantages of high speed, high input frequency, high efficiency of timing usage, and removed number of SI cells in the overall data path for linearity improvement.

According to the theoretical analysis on the proposed FWP-IADC structures, the minimum sampling clock period is proportional to the intrinsic delay of the current mirror and the increased rise/fall time in each wave-pipelined stage. The HSPICE simulation results reveal that under Nyquist rate sampling in 8-bit resolution, a sampling rate of 55 MS/s can be achieved for FWP-IADC. Moreover, the FWP-IADC can achieve a sampling rate of 90 MS/s with 8-bit resolution when the frequency of the input signal is 3 MHz. To experimentally

verify the correct function of the proposed WP-IADC structures, the proposed new architecture of the FWP-IADC is implemented by using 0.35 μm CMOS technology. The measurement results successfully demonstrate the feasibility of wave-pipelined IADC architectures in applications of high-speed ADCs.

Finally, an indirect transfer WP-IADC (ITWP-IADC) is presented and analyzed to further increase the conversion rate of the FWP-IADC. Since the minimum sampling clock period is proportional to the intrinsic delay of the current mirror and the increased rise/fall time in each wave-pipelined stage. In order to reduce the intrinsic delay of the current mirror, in the ITWP-IADC, the switched-current cells are incorporated into the wave-pipelined stages which are divided into several sections with controlled clocks. Therefore, the proposed ITWP-IADCs perform optimally in terms of speed and accuracy in the WP-IADCs. Generally, the proposed ITWP-IADCs offer additional advantages of high clock-period flexibility in SI cells for precision enhancement and reduced number of SI cells in the overall data path for linearity improvement. From the HSPICE simulation results, it reveals that under Nyquist rate sampling in 8-bit resolution, a sampling rate of 77 MS/s can be achieved for two-section ITWP-IADC. If four wave-pipelined sections are used, the ITWP-IADC can be operated at 130 MS/s at an input frequency of 16 MHz. It is expected that if the intrinsic delay of current mirror and comparison time of current comparator can be decreased, the sampling rate of the 8-bit four-section ITWP-IADC can reach 166 MS/s at an input frequency of 19.2 MHz.

In summary, the new IADC architectures proposed in this thesis have high-speed performance as verified by computer simulations as well as experimental results measured from fabricated chips. As compared to prior works, significant improvement in speed has been obtained by using the proposed architectures in the IADCs. It is believed that the proposed IADC architectures offer promising performance and new features for future design of high-speed IADCs.

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