Chapter 1

Introduction

Analog-to-digital (A/D) conversion and digital-to-analog (D/A) conversion provide the interfaces between the analog and digital system. Under the rapid progress of semiconductor technology with device scaling, digital circuits have achieved high-speed and low-power dissipation. This trend causes some impacts on mixed-signal processing systems. One is that the speed of the A/D and D/A interfaces must increase with the speed of the digital circuits in order to fully utilize the advantage of developed technologies. The other is that the high levels of integration on a single chip is attractive for mixed-signal processing under cost consideration.

According to the above observation, it is clear that A/D converters (ADCs) and D/A converters (DACs) will continue to play an essential and significant role in mixed-signal processing systems. Moreover, in video and communication applications, the transfer rate of data between the analog and digital domains continue to increase, creating new challenges in the design of high-speed data converters.

Generally, A/D conversion requires higher circuit complexity than D/A conversion to achieve a given resolution and speed. Therefore, ADCs often appear as the bottleneck in high-performance mixed-signal systems. It leads to many researches to improve the A/D conversion algorithms, architecture of ADCs, and circuits for coming application [1]-[40].

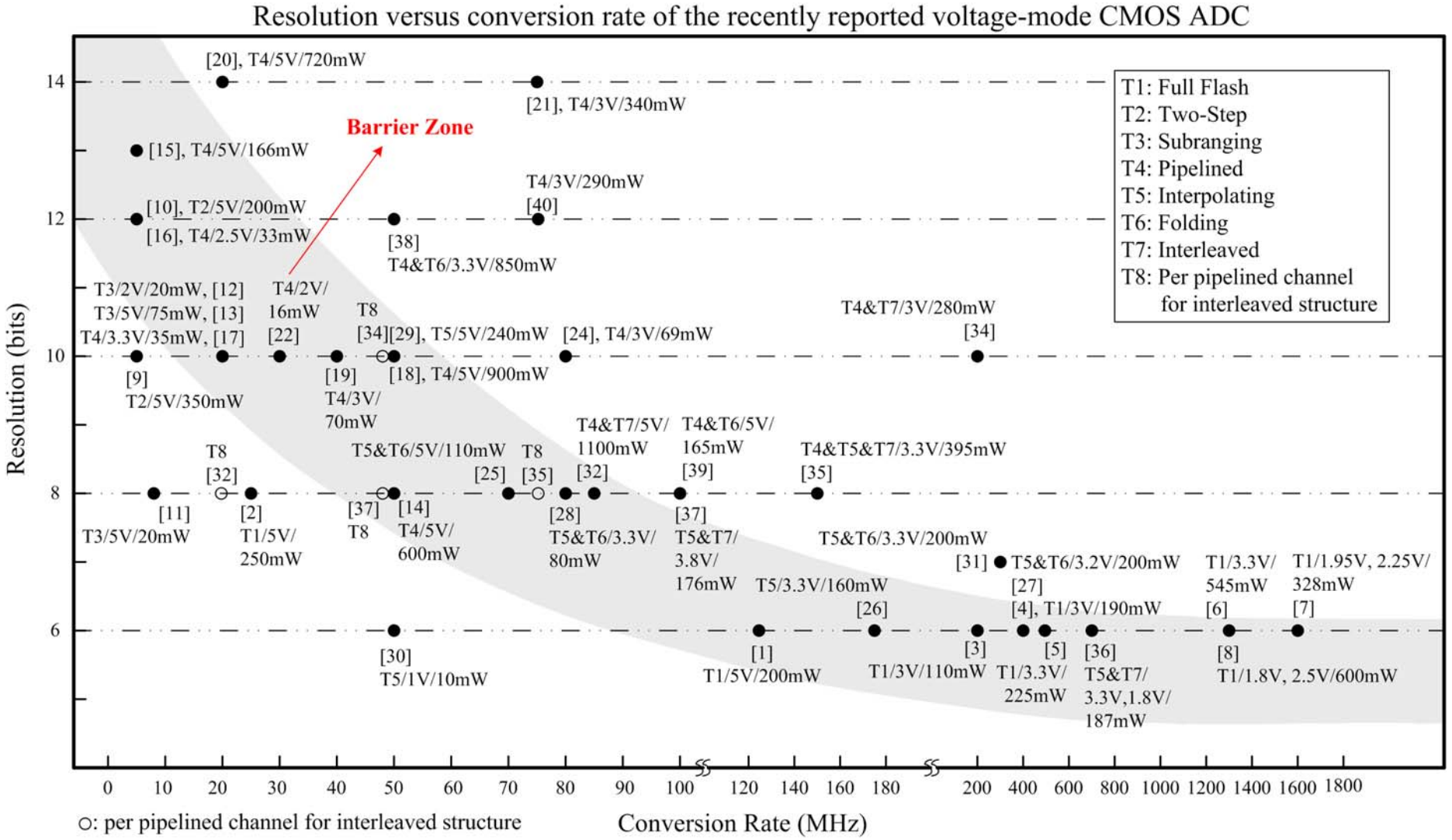

Figure 1. 1 Resolution versus conversion rate of the recently reported CMOS high-speed voltage-mode A/D converters.

1.1 High-Speed Voltage-Mode Analog-to-Digital Converter

With increasing development in electronics products, high-speed with medium resolution ADCs become more and more demand in wide application. The resolution versus conversion rate plot of recently reported CMOS high-speed ADCs with medium resolution is shown in Fig. 1.1. The input signal and quantized processing are based on the voltage-mode signals. The resolution is from 6 to 14 bits accuracy and the conversion speed is specified from several ten MHz to GHz. Based on the consideration of resolution and conversion rate, the shadow region called the "Barrier Zone" is created. As shown in Fig. 1.1, almost ADCs locate within or below the "Barrier Zone". Apparently it is difficult to break through the "Barrier Zone" and get the better performance in the design of ADCs.

Among the ADCs of Fig. 1.1, the ADCs in [1]-[8] employ the full-flash architecture. This architecture is also conceptually the easiest to understand and can be easily implemented as a repetition of simple comparator block and a decoder structure. From Fig. 1.1, the flash architecture shows the high throughput rate. However, many issues limit the usability of this architecture for resolutions above 6 bits. The flash architecture suffers from the exponential growth of the input capacitance, die area, and power dissipation. Furthermore, the comparator offset, the kickback noise [41], the feedthrough of the analog input to the resistor ladder [41][42], input dependent phase shift [42], and the problem of bubbles in the thermometer code [41][42] degrade the speed and resolution performance.

The two-step flash ADCs [9][10] and subranging ADCs [11]-[13] are multi-step converter architectures. Both kinds of ADCs are proposed to avoid the exponential growth encountered in flash ADCs. The primary advantage of the multi-step topology is that it requires less chip area and power than a flash architecture. However, this saving is obtained at the cost of longer processing time, leading to the reduction of the throughput rate. It is clearly

that the conversion rate can only achieve several ten MHz as shown in Fig. 1.1. Thus, there is a trade-off between speed performance and hardware.

In order to increase the input bandwidth for full flash or subranging architectures, the folding and interpolating architecture can be combined to adopt [25]-[31], [43]. In general, the interpolating technique can reduce the number of input amplifiers and effectively decrease the input capacitance of the ADC. Meanwhile, the number of latch comparators can be significantly reduced through the use of the folding architecture. Therefore, the combination of the two techniques can reduce the number of the folding stage and latch comparators.

In order to improve the speed performance of the subranging ADC and keep the benefit of the multi-step converter in hardware, the pipelined ADC architecture can be adopted [14]-[24]. Figure 1.2 shows the block diagram of a pipelined ADC. The pipelined ADC is similar to the subranging ADC with the exception that a sample-and-hold amplifier (SHA) and amplifier have been added to each stage. The first analog datum is applied to the first stage in the chain, and N_1 bits are detected. The analog residue can be generated and sent to the following stage. The second stage can use the SHA to sample the residue from the first stage. Meanwhile, the SHA in the first stage can sample the second input datum. This concept is similar to the idea of an assembly line because the inter-stage sampling allows all of the stages to operate concurrently. There are several advantages in the pipelined architecture. First, the throughput rate is dependent on the speed of one stage in the pipeline chain. Second, the power and chip area grow almost linearly with the number of stage. Third, the precision required of subsequent stages are relaxed by the inter-stage residue amplification. Forth, the digital error correction technique can be used to allow large offsets of the comparators. However, the high precision in the SHAs, DACs and subtractors is needed for the front stages of the conventional pipelined ADC. This reason makes the design of op amplifiers to become more difficult under device and voltage scaling.

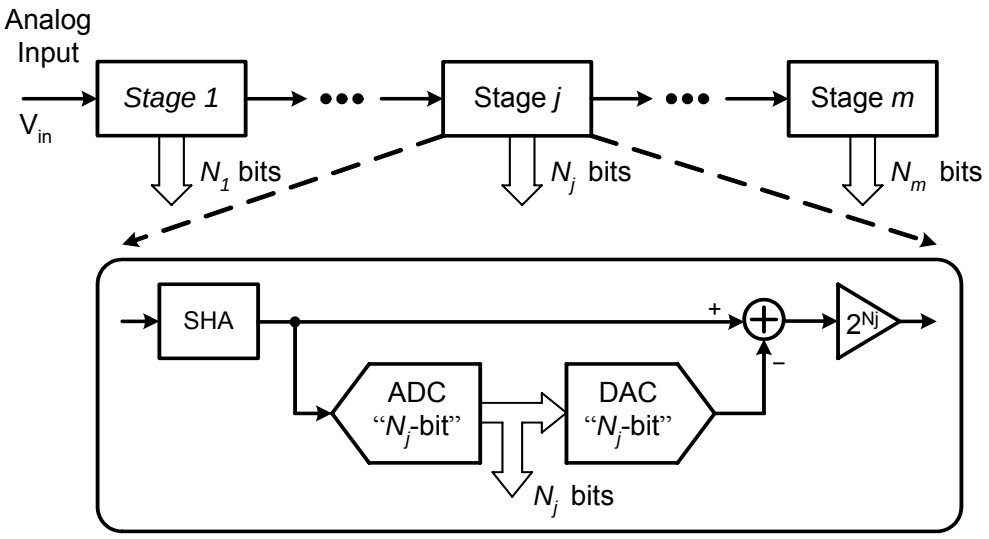

Figure 1.2 Block diagram of a pipelined ADC.

There are other techniques to improve the speed and resolution of ADCs. In the researches [32]-[35], the interleaved techniques are used to further improve the throughput rate, since the conversion rate is still limited by the settling time and accuracy requirements of the inter-stage operations in the pipelined topology. The basic principle of interleaving structure is illustrated in Fig. 1.3. The architecture consists of M identical sub-ADCs, each incorporating a SHA that tracks for time period, T1, and holds for time period, (M-1)T1. Thus, each sub-ADC can spend time, (M-1)T1, for one conversion. However, the devices and timing mismatches between the multiple parallel channels cause the performance degraded. Moreover, the researches [36]-[40] combine several techniques that is from the above mentioned to improved the conversion rate of the ADCs. It is deserved to mention that the researches [35], [40] use the concept of open-loop structure to further improve the speed performance of the ADCs.

According to the observation from the Fig. 1.1, it is clear that several architectures of ADC can break through the Barrier Zone to get better speed-resolution performance. Among these ADCs, nearly all ADCs are based on pipelined architecture [20], [21], [24], [34], [35],

[38]-[40]. Moreover, the pipelined combined with interleaved architectures can further improve the speed performance [34], [35]. Besides, some ADCs using folding interpolating architecture [31] or open-loop techniques [35], [40] can also break through the barrier zone and position at the upper right area. Generally, the pipelined architecture has the potential for the design of high-speed and medium resolution ADCs.

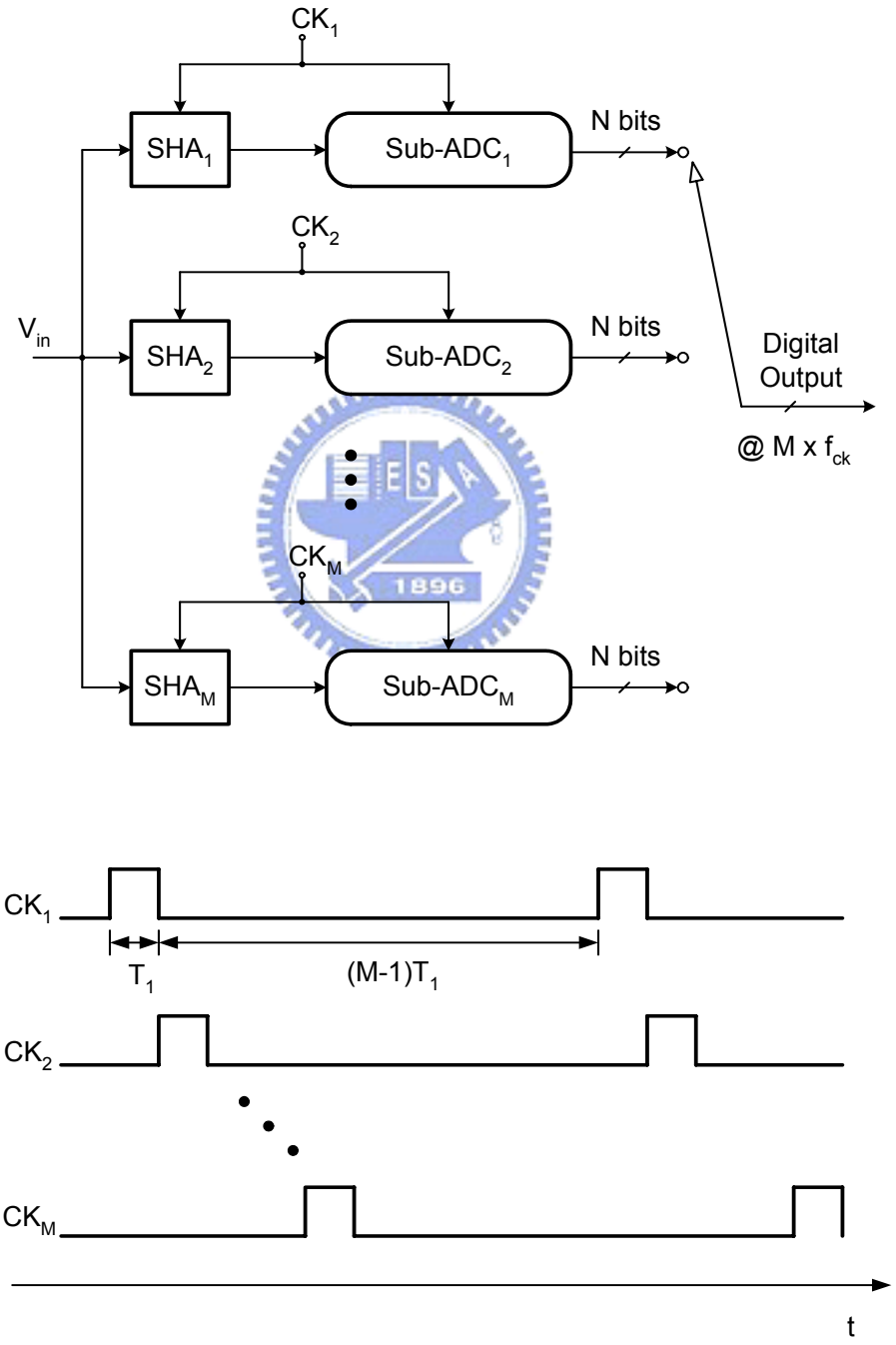

Figure 1.3 Block diagram of an interleaved ADC.

1.2 Current-Mode Techniques for Analog-to-Digital Converter Design

1.2.1 Current-Mode Analog Signal Processing

Recently, the design of current-mode integrated circuits (ICs) have been successfully applied to many analog signal processing systems. In the current-mode analog ICs design, current, instead of voltage, represents the analog signal. Due to several potential advantages [44]-[47], current-mode analog ICs have become an attractive alternative to implement analog functions. The advantages are described in the following. First, the current-mode ICs have low circuit complexity for arithmetic computation. The arithmetic computations like addition, subtraction, scaling, and inverting can be easily implemented without operation amplifiers (OP AMP) or any passive components [46], [48]. The ease of signal computations in the current domain has been extensively developed in the neural networks IC design where a massive amount of arithmetic computations are required [44], [45], [49]. Second, among various kinds of current-mode circuits, the SI technique can perform the required four basic functions of the sample-data signal processing, namely inversion, scaling, summation, and delay, without the use of linear capacitors as shown in Fig. 1.4 [46]. Therefore, the current-mode ICs design can be fully compatible with standard CMOS digital processes. Third, in some applications such as the readout of the infrared detectors or optical sensors, the output signals are inherently currents [50][51]. It is more convenient to process the current signals by current-mode circuits directly without the current-to-voltage conversion. Fourth, due to low voltage swing and inherent driving capability of current-mode circuits, the technique of current steering and current sensing can apply to the high-speed DACs [52]-[56] and CMOS SRAM design [57]-[59], respectively. Fifth, the required voltage swing of the current-mode ICs is inherent low. Due to the square I-V law of the MOS transistors operated in the saturation, the required voltage swing in the current-mode ICs is smaller than that in the voltage-mode ICs. Therefore, current-mode design is a promising technique for low-voltage

low-power applications [60]-[64].

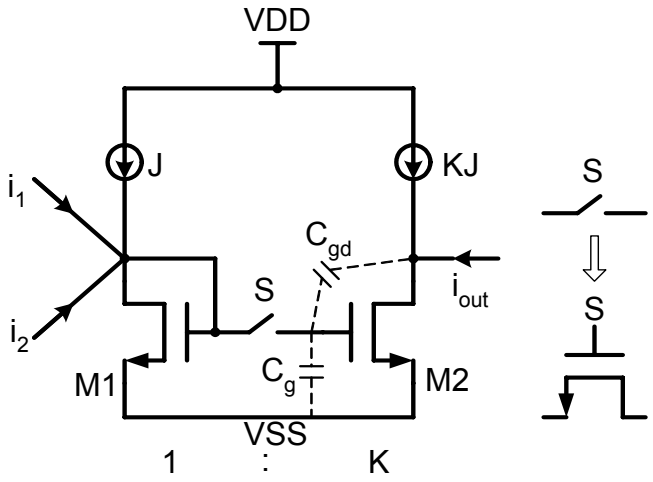

Figure 1.4 The simple current sample-and-hold amplifier performing the function of scaling, inversion, summation, and delay.

1.2.2 Switched-Current (SI) Sample-and-Hold Circuits (SHCs)

In the current-mode sampled-data signal processing, the SI SHCs are the basic building block as shown in Fig. 1.4 [46]. Especially in the design of high-speed current-mode pipelined ADCs, the SI SHCs are the key components. In order to overcome the nonlinearity errors that include clock feedthrough errors, transistor mismatches, channel length modulation effect, and finite output-to-input resistance-ratio error in the SI SHC, many techniques are proposed by the published papers [46], [60]-[81]. Table 1.1 lists the techniques and features of reported SI SHCs. The major characteristics of the reported SI SHCs are shown in Table 1.2. It is clear that the accuracy is between 8 and 13 bits. However the sampling rate is below 50 MHz. Therefore the SI SHCs are the bottleneck in the design of high-speed current-mode pipelined ADCs.

Table 1.1 Techniques and features of reported SI sample-and-hold circuits

Designation or Ref. No.	Techniques	Features
Dynamic current mirror [46], [74]	The sample mode and hold mode are operated by the same MOS transistor M1	The problem of the device mismatches are solved
Two-step current memory (S^2I) cell [66]	Double-sampling operation to achieve a higher degree of error cancellation	Eliminate the signal independent error, signal dependent error still exists
S^3I memory cell [67]	Amplifier is added to the S^2I cell	Increase the output-to-input-resistance-ratio and reduce the signal dependent clock feedthrough error
Helfenstein's method [68]	Using the coarse and fine current memory cell	To satisfy high-speed transition characteristic and reduce the switching error
[69]-[74]	Using replicate circuit	[69]: Reduce the signal independent clock feedthrough error [70]-[74]: Cancel both signal independent and signal dependent clock feedthrough error
Zero-voltage switching [75], [76], [79]	Similar to bottom-plate sampling [82]	[75], [76]: Signal dependent switching error can be eliminated, single-end topology [79]: Cancel both signal independent and dependent switching error, differential-mode
[77], [78], [80]	Amplifier is added to the basic SI cell	[77]-[78]: The output-to-input-resistance-ratio can increase and the signal dependent switching error can reduce [80]: Switching errors can be divided by the gain of the amplifier
[81]	Regulated cascade structure [83] and Miller capacitance-enhancement	Regulated cascade structure: increase the finite output resistance Miller capacitance-enhancement: increases the sampling capacitance
[60]-[65]	Combined the above several concepts	Low-voltage SI sample-and-hold circuits

Table 1.2 Major characteristics of the reported SI sample-and-hold circuits

Ref.	Supply Voltage	Sampling Rate	Linearity
[64]	1V	30 MS/s	SNR = 56 dB
[65]	3V	20 MS/s	9 bit
[68]	3V	1 MS/s	THD = -62 dB
[72]	3V	1 MS/s	11 bit
[76]	3.3V	50 MS/s	13 bit
[79]	5V	512 KS/s	HD2 = -114 dB, HD3 = -130 dB
[80]	5V	4 MS/s	THD = -60 dB
[81]	3V	100 KS/s	11 bit

1.2.3 Current-Mode Analog-to-Digital Converters

Based on the current-mode techniques and the SI SHCs, many current-mode analog-to-digital converters (IADCs) are developed since 1988 [86]-[107]. The first 8-bit algorithmic IADC in [84], [85] is constructed by cascading 8 identical bit cells. According to the reference-restoring algorithm shown in Fig. 1.5, the 8-bit IADC with 500kHz conversion rate and 85mW power consumption has been developed using the active current mirror shown in Fig. 1.6 [84], [85]. The active current mirror is a simplified current mirror using a voltage amplifier in the feedback loop to make the current input node virtually shorted to a fixed bias voltage. Therefore, the output-to-input-resistance-ratio of the active current mirror is increased by lowering down the input resistance through feedback techniques.

For the audio-band applications, SI circuit techniques have been used to implement oversampling ADCs in standard digital CMOS processes [86]-[89]. Two experimental oversampling ADCs which can be operated under 3.3 V supply voltage and achieve 10-bit linearity were reported in [86], [87]. The power consumption of the SI sigma-delta modulator in [86], [87] has been reduced to 2-mW which shows the low-voltage low-power potential of

SI circuits. Another experimental oversampling ADC that can achieve high resolution 14-bit under 5V supply voltage was also developed [88]. Through the accuracy of the current-mode oversampling ADCs are still below 14-bit up to date, the results reported in [86]-[89] indicate that the SI circuits is an attractive way to implement the low cost oversampling ADCs in standard CMOS digital process for the audio-band applications.

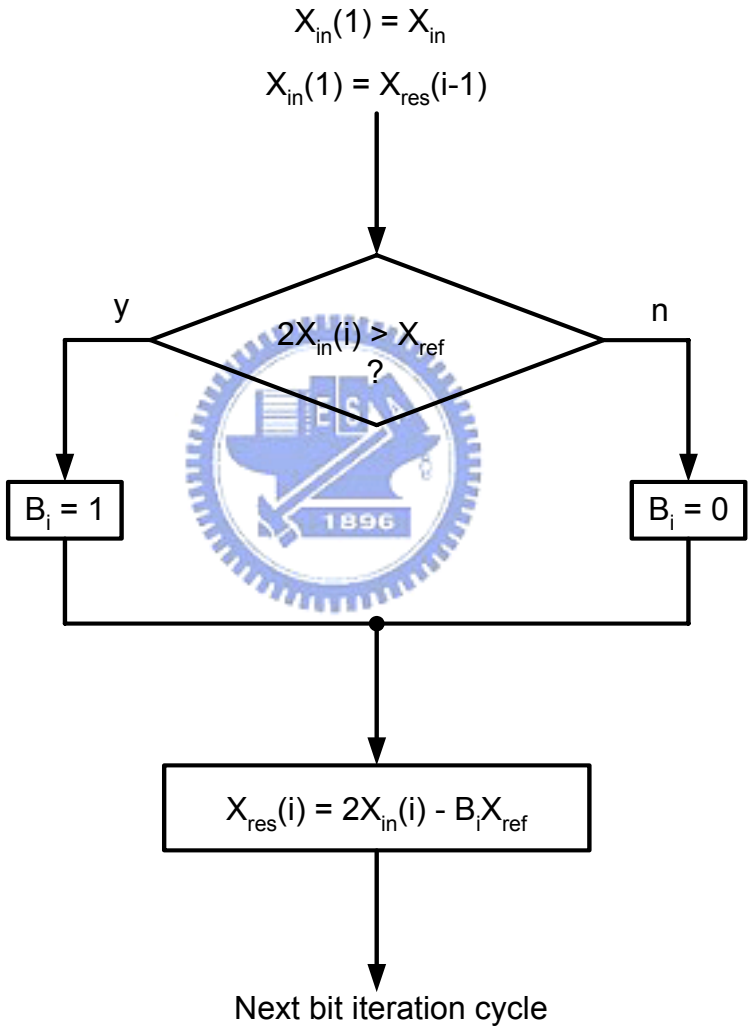

Figure 1.5 The reference-restoring ADC algorithm.

For the low cost and low power applications, three experimental cyclic IADCs are proposed [90]-[92]. The resolution of the IADC can achieve 10-bit by the ratio-independent

technique in [90]. Moreover, the power consumption of the IADC can reduce to 2-mW by the cyclic architecture [91][92].

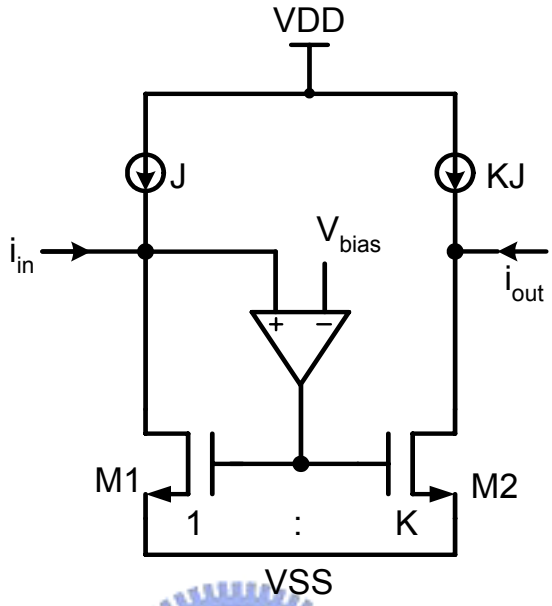

Figure 1.6 The active current mirror.

For high-speed applications, many pipelined IADCs [93]-[107] are proposed to achieve a high throughput rate at a lower cost due to the concurrent operation of each stage. Figure 1.7 shows the resolution versus conversion rate of recently reported high-speed IADCs. The Barrier Zone (shadow region) of Fig. 1.7 is created by the voltage-mode ADCs from the Fig. 1.1. Nearly all high-speed IADCs are located within the Barrier Zone of voltage-mode ADCs or below the zone. In order to get a higher conversion rate, the interleaved architecture also can be combined into the pipelined IADCs in some researches [94], [103], and [107]. Especially in the work of [107], 32 parallel pipeline IADCs were used and each IADC was run at 125-MSample/s. The overall IADC can achieve 4Gsample/s at 6-bit resolution under calibration and at an input frequency of 1 GHz.

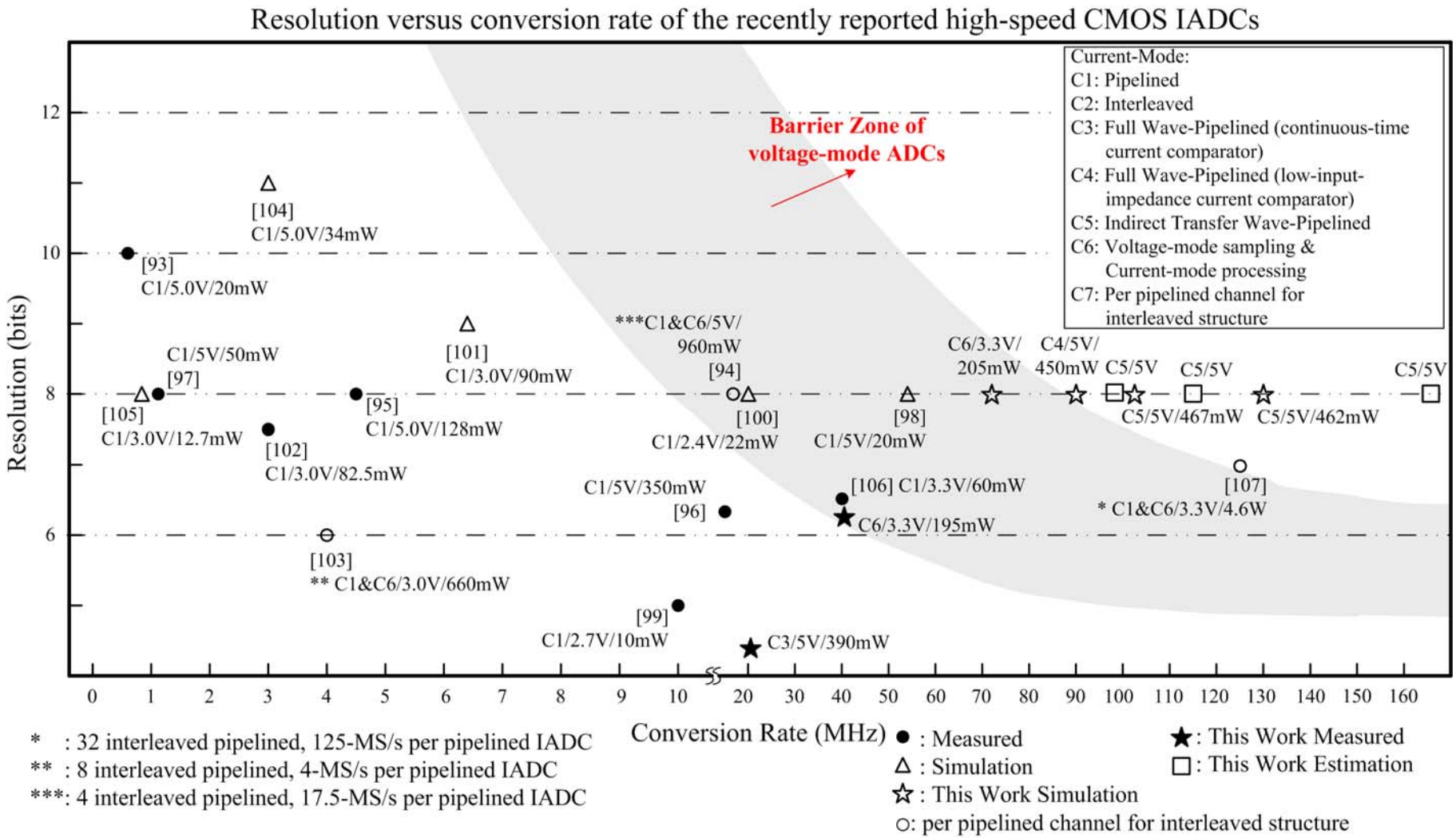

Figure 1.7 Resolution versus conversion rate of the recently reported CMOS high-speed IADC.

Comparing IADCs with voltage-mode ADCs, IADCs have the advantage of lower cost because of the compatibility with digital process. However, as shown in Fig. 1.7, the reported IADCs are almost located in the barrier zone or on the outside lower left of the shadow region. From Figs. 1.1 and 1.7, it can be understood that the published current-mode pipelined ADCs generally have a lower operating speed and resolution than voltage-mode ADCs. This is due to high accuracy SI SHC with small settling time is difficult to obtain. The related SI SHC techniques for the design of pipelined IADCs are listed in Table 1.3 and major characteristics of the reported SI SHCs are also mentioned in previous section as shown in Table 1.2. Meanwhile, the comparisons of chip area for voltage-mode and current-mode ADCs are list in Table 1.4. The comparisons are based on pipelined architecture. Since the IADCs need not use the linear capacitance, the chip area of IADC is usually smaller than the one of voltage-mode ADCs in the same technology.

Table 1.3 The related SI sample-and-hold techniques for the reported pipelined IADCs

Current-mode Pipelined ADC Ref. No.	SI sample-and-hold techniques
[93]	Regulated cascode switched-current memory cell
[94], [96], [106]	S^2I current memory cell [67]
[95]	[80]
[98]	N/A
[99]	Basic SI (NMOS switch+dummy switch)
[100]	Zero-voltage sampling [75]
[101], [102], [103]	Replica circuit [73]
[104]	Regulated cascode switched-current memory cell (MOS switch+dummy switch)
[105]	Regulated cascode, Master-slave current delay cell [81]
[107]	Digital calibration

Table 1.4 The comparisons of chip area for voltage-mode and current-mode ADCs

Mode	Ref. No.	Architecture	Resolution	Area	Technology
Voltage	[20]	Pipelined	14-bits	0.77 mm^2/b	0.5 μm
	[21]	Pipelined	14-bits	0.55 mm^2/b	0.35 μm
	[24]	Pipelined	10-bits	0.185 mm^2/b	0.18 μm
	[34]	Pipelined & Interleaved	10-bits	0.185 mm^2/b	0.5 μm
	[35]	Pipelined & Interpolating & Interleaved	8-bits	0.113 mm^2/b	0.6 μm
	[40]	Pipelined	12-bits	0.658 mm^2/b	0.35 μm
Current	[93]	Pipelined	10-bits	0.25 mm^2/b	0.8 μm
	[94]	Pipelined & Interleaved	8-bits	0.4 mm^2/b	0.8 μm
	[95]	Pipelined	8-bits	0.73 mm^2/b	0.8 μm
	[96]	Pipelined	8-bits	0.3 mm^2/b	0.8 μm
	[97]	Pipelined	8-bits	0.081 mm^2/b	1.2 μm
	[99]	Pipelined	8-bits	0.05 mm^2/b	0.6 μm
	[102]	Pipelined	8-bits	0.337 mm^2/b	0.8 μm
	[103]	Pipelined & Interleaved	8-bits	0.344 mm^2/b	0.8 μm
	[106]	Pipelined	8-bits	0.077 mm^2/b	0.35 μm
	[107]	Pipelined & Interleaved	8-bits	0.112 mm^2/b	0.35 μm

1.3 Research Motivation and Organization of This Thesis

In order to improve the speed performance of IADCs for video or communication applications, this thesis deals with the design and analysis of several new architectures for IADCs to break through the Barrier Zone of Fig. 1.7. Three kinds of new architecture are successfully proposed in this thesis. This thesis contains five chapters that include the design of pipelined ADC using open-loop voltage-mode sampling structure, full wave-pipelined current-mode ADC (FWP-IADC), and indirect transfer wave-pipelined current-mode ADC (ITWP-IADC). Chapter 1 introduces the background and explains the main motive of the thesis. Some architecture among the recently reported voltage-mode high-speed ADCs are described. Furthermore, the reported techniques for current-mode ADCs are also

demonstrated.

Chapter 2 describes the design of high-speed pipelined ADCs using open-loop voltage-mode sampling and current-mode processing techniques. Since the SI SHCs is the speed bottleneck of the current-mode pipelined ADCs, this work adopts voltage-mode sampling architecture. Moreover, open-loop structure is used to implement the design of ADCs for several high-speed and low-power applications [35], [40]. Besides, the open-loop structure is also adopted to implement the track-and-hold circuits for high-speed application [108]. Therefore, the proposed pipelined ADCs use the open-loop structure to improve the speed performance and current-mode signal processing to easily perform the subtraction function. HSPICE simulation shows that the conversion rate of the developed pipelined ADC can achieve 71.4-MSample/s with 8-bit accuracy. Experimental results and discussion are also given.

In Chapter 3, a new current-mode wave-pipelined architecture called full wave-pipelined current-mode ADC (FWP-IADC) for high-speed ADCs are designed and analyzed. From the observation of the Section 1.2, precise SI SHC with small settling time is difficult to obtain. Therefore, the SI SHCs are the bottleneck of the high-speed current-mode ADC design. An attempt to avoid the use of the SI SHCs is made in this chapter. In the FWP-IADC, each stage uses the full current-mode wave-pipelined structure without inter-stage SI cell circuits. Both measurement and simulation results are also shown. From the results of the post-simulation, the proposed FWP-IADC can achieve 8-bit accuracy with a sampling rate up to 90-MSample/s when the input signal frequency is 3 MHz.

Chapter 4 describes the modified current-mode wave-pipelined ADC that is called indirect transfer wave-pipelined current-mode ADC (ITWP-IADC). In the ITWP-IADC, the SI cells are incorporated into the wave-pipelined stages which are divided into several sections with controlled clocks. Therefore, the proposed ITWP-IADC performs optimally in

terms of speed and accuracy in the WP-IADCs. The conversion rate can further improve up to 130-MSample/s for the four-section ITWP-IADC under an input frequency of 16 MHz in 8-bit resolution. Simulation results are also given in this chapter.

Finally, the main results of the thesis are concluded in Chapter 5. Some suggestions for the future work are also addressed in the same chapter.