Chapter 2

The Design of High-Speed Pipelined Analog-to-Digital Converters Using Voltage-Mode Sampling and Current-Mode Processing Techniques

2.1 Introduction

It is known that analog-to-digital converters (ADCs) play an important role in mixed-signal integrated systems. Under the rapid progress of semiconductor technology with device scaling, great impacts have been imposed on the design mixed-signal integrated circuits and systems to achieve high-speed and/or low-power performance. Especially, the high-speed ADCs are required in many modern integrated systems for communications, instrumentation, and consumer electronics applications.

Recently, many high-speed pipelined ADCs have been proposed and analyzed [14]-[24], [32]-[35], [40]. In these ADCs, the interleaved architecture or open-loop structure is used to obtain the high-speed performance. Besides, the open-loop structure is also adopted to implement the track-and-hold circuits for high-speed application [108]. Generally, closed-loop structures have high accuracy at low frequency since the switch and capacitor are included in the feedback loop. But the bandwidth of the operational amplifiers is limited, thus they are not suitable for high-speed applications [108]. In order to achieve high-speed performance, a new open-loop structure that obviates the need for closed-loop circuits in multistage ADC's is proposed in this chapter. In the new structure, both voltage-to-current converter (VIC) and current-steering digital-to-analog converter (DAC) are applied to perform high-speed

sub-DAC and subtraction functions. Since the subtraction function can be easily implemented in the current mode, the high-speed performance can be achieved by a single signal path without feedback. Based upon the analogue operation principle and current strategy of the proposed ADC [109][110], the 3-bit digital codes can be obtained per stage. One of the digital codes is for digital error correction. The simulation results on the designed ADC example using the proposed new structure have shown that with 3.3V supply voltage and 0.25μm CMOS technology, the designed A/D converter can achieve 8-bit resolution with a 71.4MS/s sampling rate. Based on 8-bit resolution, the measurement results of the prototype chip show the differential nonlinearity (DNL) and integral nonlinearity (INL) for all codes are less than +1.9/-1 LSB and + 2.8/-2.8 LSB, respectively. The dynamic test shows that the effective number of bit (ENOB) is 6.2-bit under 40-MSample/s sampling rate. The degradation of performance is due to the effect of gain error in the sample-and-hold circuit (SHC) and the input offset current in the current comparator.

In Section 2.2, the architecture and the operating principle of the proposed ADC are introduced. Meanwhile, the circuit's implementations are also described in this section. The simulation and experimental results of the proposed ADC are presented in Section 2.3. The discussions are also described in Section 2.3. Finally, the conclusions are given in Section 2.4.

2.2 Chip Design

2.2.1 Voltage-Mode Sampling and Current-Mode Processing Architecture

Figure 2.1 shows the block diagram of the proposed new ADC architecture. It consists of pipelined stages, registers, and digital error correction circuits. The resolution of each stage except the last stage is $\log_2 (2^n-1)$ bits, where n is the number of digital output bits per stage. In this work, n is equal to 3 and the resolution per stage is about 2.8 bits with that of the last stage being 2 bits. Four pipelined stages are necessary to perform the 8-bit resolution of the

proposed pipelined ADC in this work. After the processing of each stage, the generated digital output codes are transferred into the register string at the same time. By passing a certain number of registers, digital error correction is performed. The final 8 digital bits are output in parallel.

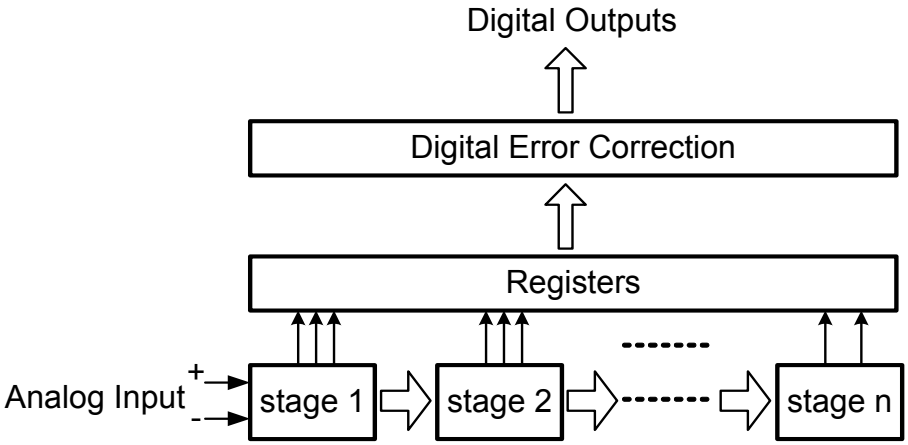


Figure 2. 1 The block diagram of the proposed ADC.

The detailed structure of a pipelined stage is shown in Fig. 2.2. Each pipelined stage except the last one consists of one voltage SHC, six voltage-to-current converters (VICs), one current steering sub-DAC, six current comparators and one thermometer-to-binary decoder to generate 3-bit binary codes and 6-bit thermometer codes. However, only three VICs and current comparators are needed in the final stage to produce 2-bit binary codes and 3-bit thermometer codes. The structure of the final stage is shown in Fig. 2.3. In Figures 2.2 and 2.3, the voltage SHC is used to hold and reproduce the input voltage. The output voltage of SHC is sent to the VICs to perform relatively currents. Meanwhile, the sample voltage is also transferred to the next stage by the unit gain of SHC. In order to improve the speed performance of the SHC, the open-loop structure is selected. In the open-loop structure, the voltage subtraction cannot be easily implemented. Therefore the voltage-to-current conversion is needed to perform the subtraction in current domain. The key circuit, SHC and VIC circuits, are described in detail in the Section 2.2.2.

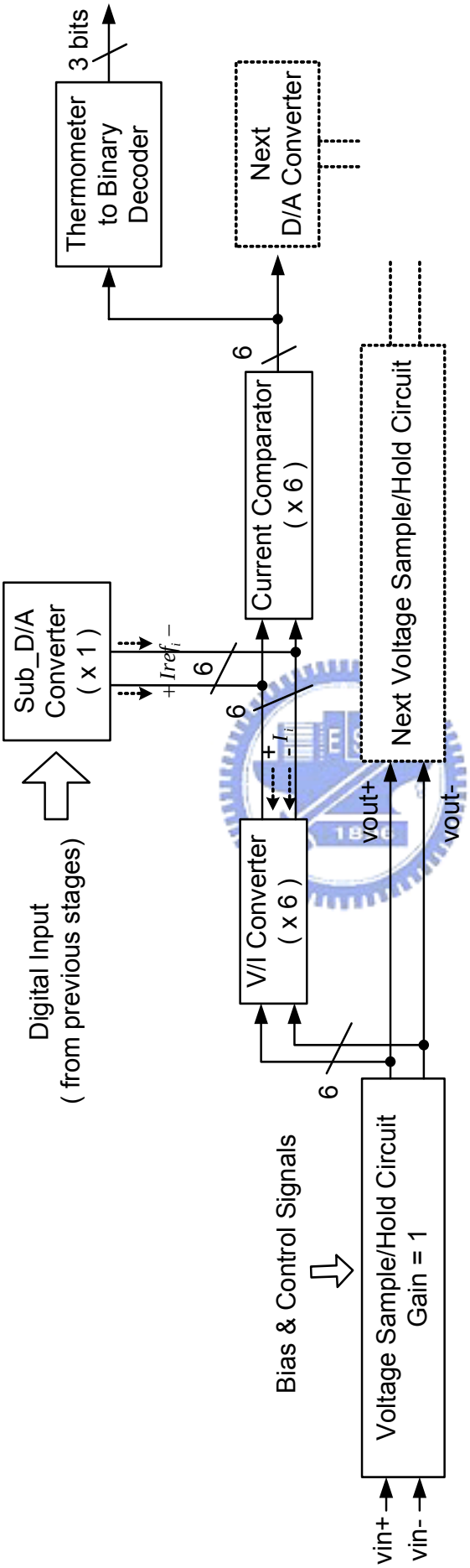


Figure 2. 2 The detailed structure of the pipelined stage i.

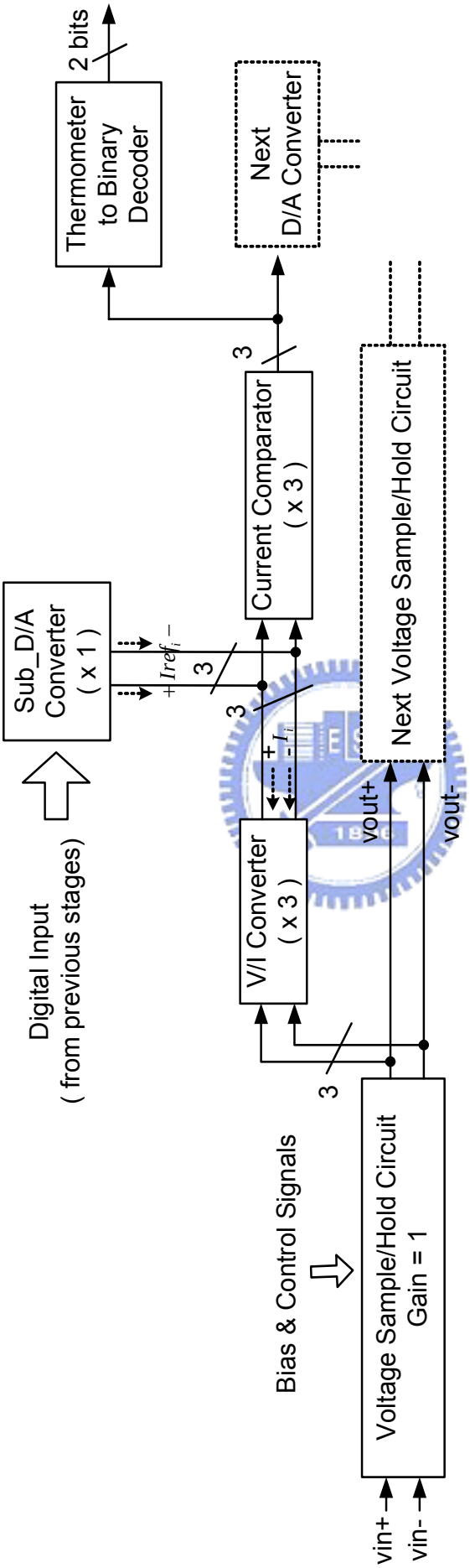


Figure 2. 3 The detailed structure of the final stage.

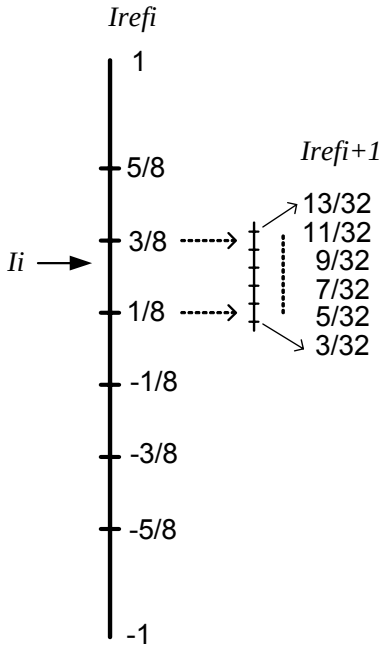


Figure 2. 4 The decision algorithm of the reference current level.

Since many high-speed DACs have been implemented successfully by using the current steering technique [52]-[56]. Thus this kind of DAC is adopted to implement the sub-DACs in this work. The digital input signals of sub-DACs are the output digital signals in previous pipelined stages. They are converted into the six pairs of output current signal $Iref_i$ to be subtracted from the output current I_i of the VIC in Fig. 2.2. The successive approximation algorithm is adopted to implement the ADC process [43], [109], [110]. Therefore the decision algorithm of the sub-DACs output current $Iref_i$ can be illustrated as shown in Fig. 2.4. In order to show clearly, the single-end reference currents are given in Fig. 2.4. If the current I_i is located on some range between the two reference current levels, the next stage reference current I_{refi+1} can be decided by dividing the range into several fine area. Thus the next 6 reference currents of sub-DAC can be obtained.

After the current subtraction, the remaining current signals are sent to the current comparator to complete the quantization operation. Finally, the 6-bit thermometer codes are

generated and sent to the next sub-DAC. Meanwhile, these thermometer codes are also transferred to 3-bit binary codes by thermometer-to-binary decoder for digital error correction.

Besides, in order to suppress the even order harmonic distortion and clock feedthrough noise, the differential signals are used in whole signal path.

2.2.2 Circuits Implementation

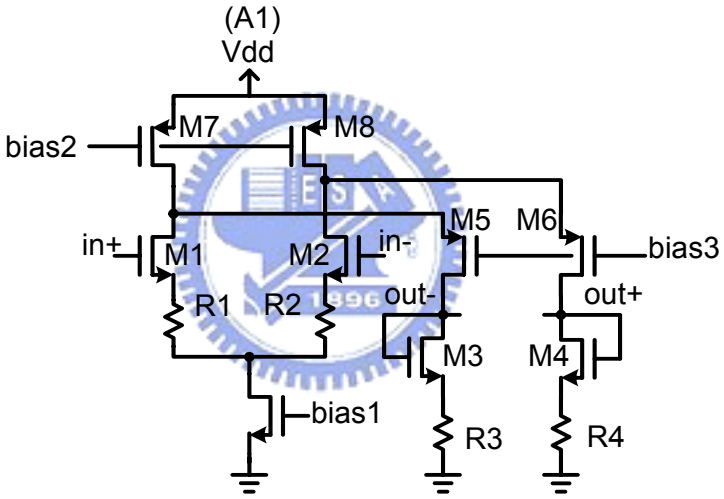
In the proposed pipelined ADC, the SHC is a basic component. It plays the roles of the voltage conveyer. Thus the design of the SHC is critical. According to Wang, Boni, and Murmann analyzed [35], [40], [108], the open-loop structure is very suitable for high-speed application. Figure 2.5 shows one stage SHC. The folded-cascode CMOS amplifier is used as the input buffer as shown in Fig. 2.5 (a) [108]. The folded structure allows the input buffer to insert the large source degeneration by means of resistors R1-R4, although the resistors waste some voltage drop. This degeneration is important for reducing the nonlinearities arising from the mismatch in the NMOS devices (M1-M4). Cascode transistors M5, M6 provide level shifting to keep the input devices M1 and M2 always in saturation region. The amplifier gain of the input buffer can be set to unity by the following equation:

$$Av = \frac{gm_1}{1+gm_1R_1}[(\frac{1/gm_3 + R_3 + ro_5}{1+gm_5ro_5}) // ro_7] \cong \frac{gm_1}{1+gm_1R_1}(\frac{1/gm_3 + R_3 + ro_5}{1+gm_5ro_5}) \qquad (2.1)$$

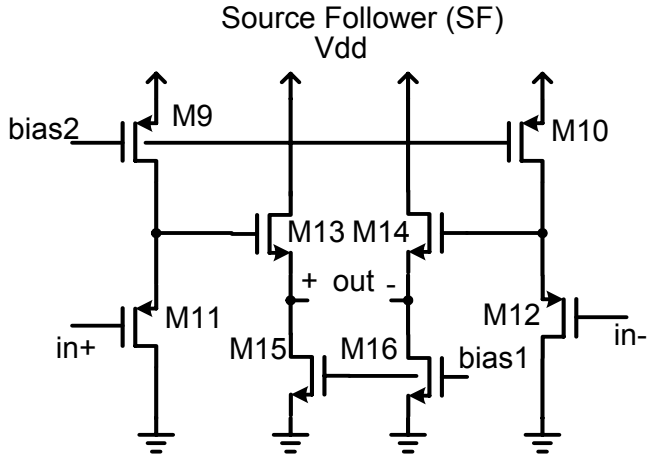
As shown in Fig. 2.5 (b), the transistors M11- M14 are served as the source followers. It shifts the output DC level to keep the output voltage and the input voltage in the same DC level.

Figure 2.5 (c) shows the whole SHCs in one stage. The stage can be divided into two parts A and B. This arrangement can allow the sub-DACs to have more time for the switching

transition. Because at the beginning sampling of the stage *i+1*, the digital outputs of the stage *i* have also been generated to control the current cell switch of the stage *i+1* sub-DAC. Thus it can spend about half-period time for the settling of the sub-DAC transition. However two nonoverlap control signals are needed to control the switches 1 and 2. Otherwise, in order to cancel the clock feedthrough effect and switch charge injection, the dummy switch and bottom plate sampling techniques are used. The switches 3 and 4 are turned off slightly before the switches 1 and 2, respectively. The differential operation as well as large sampling capacitors (1.5 pf) are used to improve the overall linearity. Also, the large capacitances reduce the kickback noise from the VIC.



(a)



(b)

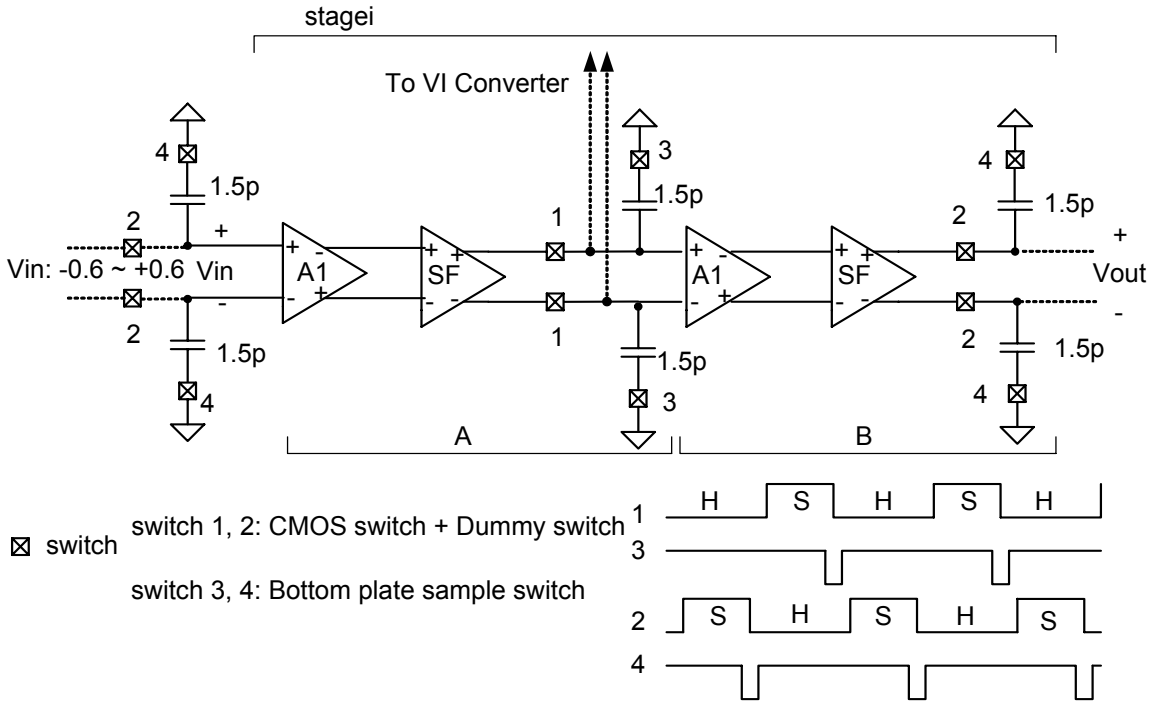


Figure 2. 5 (a) Linearized folded-cascode CMOS input buffer. (b) Source follower. (c) One stage sample-and-hold circuit.

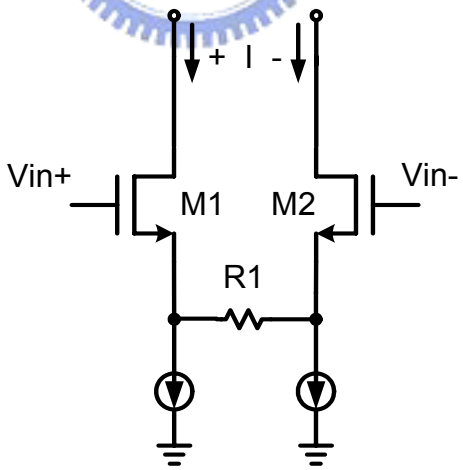


Figure 2. 6 The voltage-to-current converter.

The source degeneration differential pair circuit also can be served as the VIC to increase the linearity of the circuit as shown in Fig. 2.6. In this circuit, the Gm can be designed to the

213.33 μA/V. It makes the input voltage range 1.2V map to output current range 256 μA. Although the process variation may affect the value of Gm due to the change of the resistor value, it just changes the input voltage range. The linearity of the circuit still can be kept to an acceptable level.

All sub-DACs are implemented by current steering structure. In the sub-DACs, all bits are linearly decoded. Figure 2.7(a) shows the simple unit current cell. The threshold-voltage compensation technique [111] and cascode structure are used to implement the reference current Iref for accuracy consideration as shown in Fig. 2.7(b). The global mismatch of the threshold voltage among the current source array can be cancelled locally in the circuit of the Fig. 2.7(b). By neglecting the equivalent Early effect, the source current Iref can be written as follows.

$$\begin{aligned} \text{Iref} &= K\frac{W_2}{L_2}(VDD - V_a - |V_{th2}|)^2 \\ &= K\frac{W_2}{L_2}(VDD - VR1 + V_{SGc} - |V_{th2}|)^2 \end{aligned} \tag{2.2}$$

When M_c and M_n are operated in the saturation region, the source current I_c can be given as follows.

$$I_c = K\frac{W_c}{L_c}(V_{SGc} - |V_{thc}|)^2$$

$$\Rightarrow V_{SGc} = \sqrt{\frac{I_c}{K \cdot W_c / L_c}} + |V_{thc}| \tag{2.3}$$

Substituting (2.2) into (2.3), the equation can be rewritten as follows.

$$\text{Iref} = K\frac{W_2}{L_2}(VDD - VR1 + \sqrt{\frac{I_c}{K \cdot W_c / L_c}} + |V_{thc}| - |V_{th2}|)^2 \tag{2.4}$$

From the above equation (2.4), the source current is varied with the difference of V_{th2} and V_{thc} rather than V_{th2}. When VR1 is large and I_c is small, I_2 is dominated by VR1. Even if the

threshold voltage mismatch exists, the variation of V_{thc}-V_{th2} is still much smaller than VR1 so that the variation of Iref is also very small.

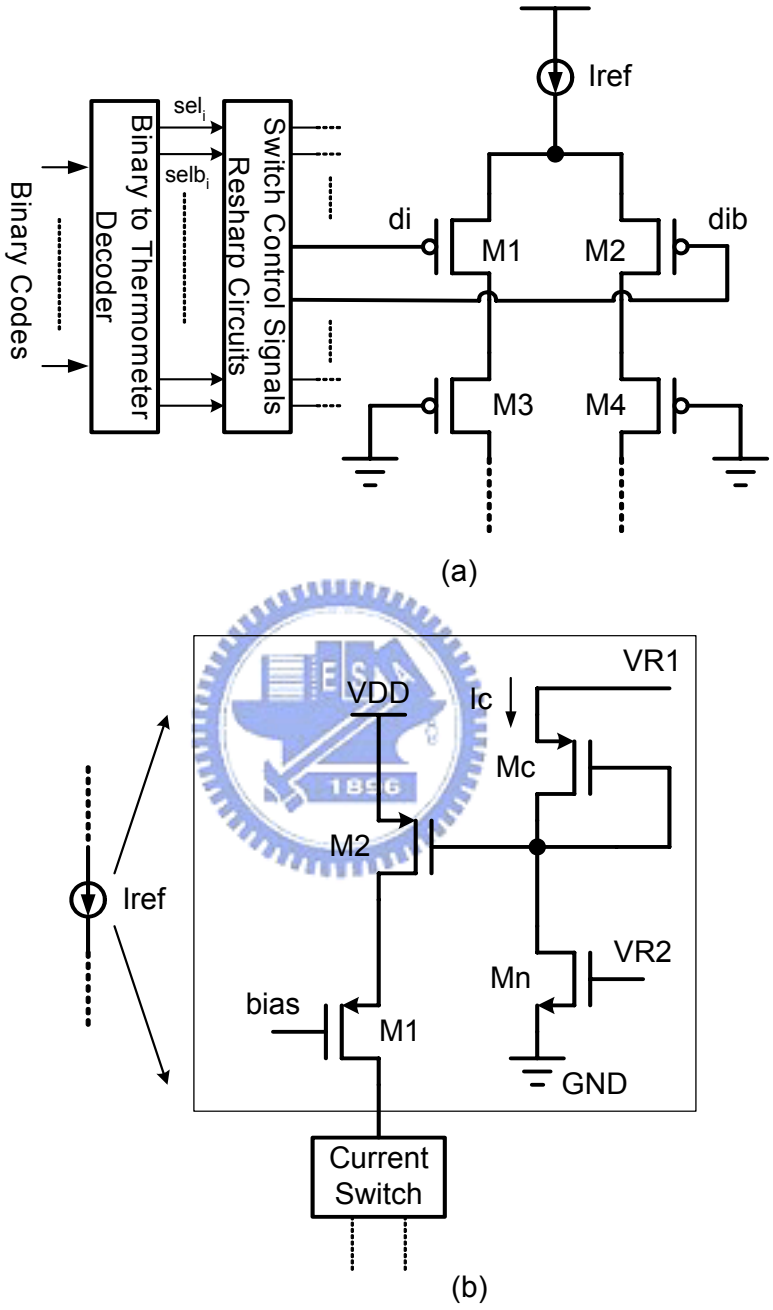


Figure 2. 7 (a) Simple unit current cell (b) Threshold-voltage compensation circuit [111].

According to the quantization result of the previous stage, the thermometer digital codes are used to control the current cell switches by the reshape circuits. The MOS transistors M3

and M4 are always turned on. They can block the feedthrough noise from the control signals di and dib to disturb output node voltage.

Figure 2.8 shows the reshape circuits of the switch control signal and the corresponding waveforms. To reduce the glitch energy and increase the settling speed, the cross point of rising/falling waveforms of di and dib signals must be low enough to control the current switches. If the cross point of rising/falling waveforms of di and dib is low enough, the differential current switches M1 and M2 in Fig. 2.7(a) will not turn off at the same time.

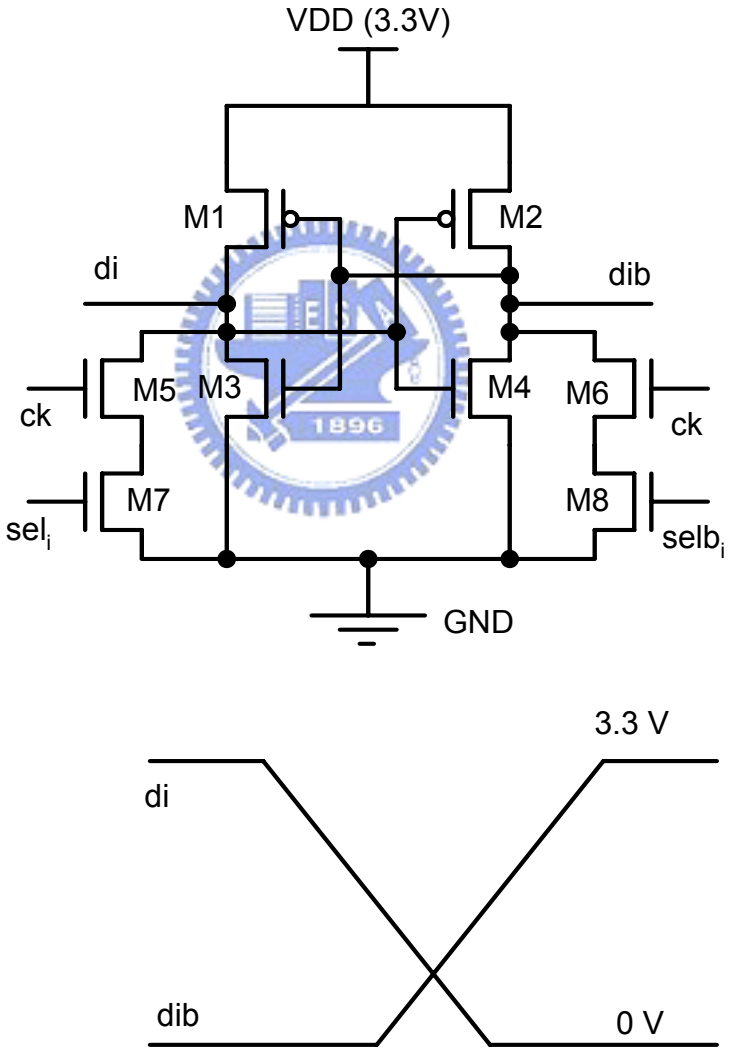


Figure 2. 8 The reshape circuits of the switch control signals and the corresponding waveforms.

Because the current comparator must receive the current to serve as the input signal, thus the low input impedance is needed to get the better transition performance. Figure 2.9 [48], [95], [112] shows the low input impedance current comparator circuits. Due to the transistors M1, M5, and M9 (M2, M6, and M10) form the negative feedback, the input impedance can be reduced. Therefore the subtracted current signal from sub-DAC and VIC can be fast settled down. The transistors M9 and M10 also are used as the source followers. The offset of the comparator depends on the mismatch of the MOS transistors. However, this offset can be corrected by the digital error correction circuit.

According to simulation and analysis results, the critical delay path consists of voltage SHC, VICs, and current comparator. In this work, the SHC needs about 7 and 4 nsec for tracking the input voltage and signal settling, respectively. The comparison time of current comparator is 2 nsec. Thus the proposed pipelined ADC can perform all operation in 14 nsec for one stage. Apparently, if the high-speed SHC can be given, the speed performance of the pipelined ADC will be improved.

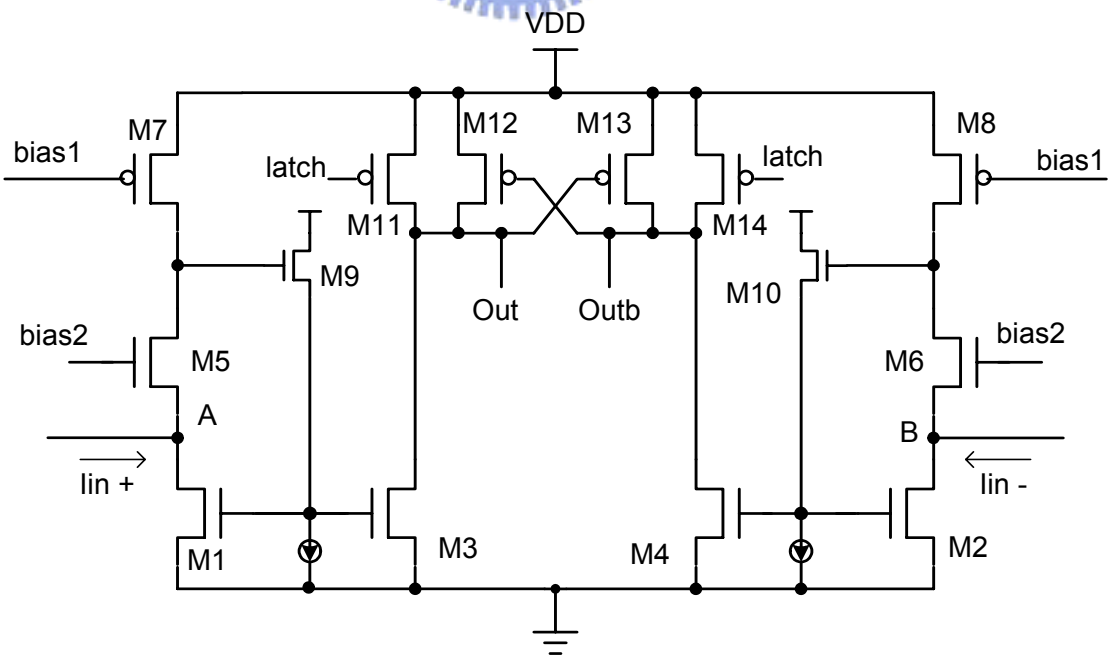
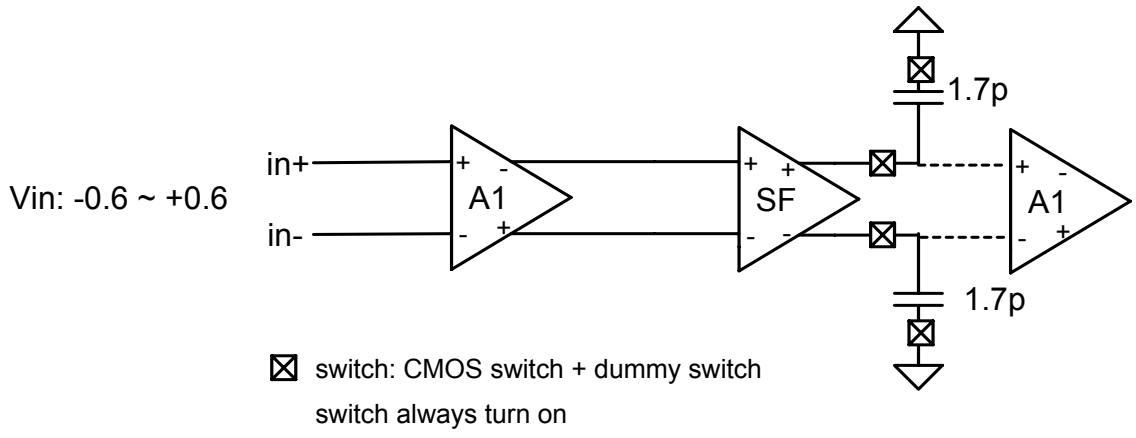


Figure 2. 9 Low input impedance current comparator.

2.3 HSPICE Simulation and Experimental Results

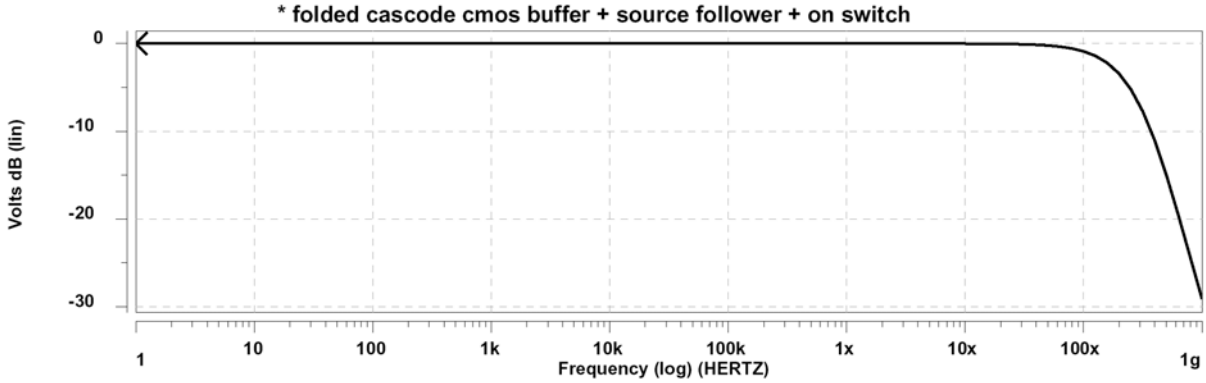
2.3.1 HSPICE Simulation Results

All simulation results are based upon the device parameters of 0.25 μm 1P5M CMOS technology with 3.3V power supply. The option of thick oxide is selected, thus the minimum channel length is 0.35 μm. Meanwhile, the parasitical capacitances are extracted to perform the post-simulation. Figure 2.10 shows the ac and linearity analysis of the SHC. In Fig. 2.10(a), the block diagram of the simulation is shown and the sampling switches are always turned on. From Fig. 2.10(b), the ac gain is unity and 3-dB bandwidth is 100 MHz. In Fig. 2.10(c), the total harmonic distortion is –75-dB when the input frequency is about 1 MHz. Figure 2.10(d) shows the slew rate of the full scale voltage swing. The slew rate is about 235.3 V/μs. The simulation results of the VIC are given in Fig. 2.11. Figure 2.11(a) shows the simulated condition of the VIC. Figures 2.11(b) and (c) show the ac and linearity analysis, respectively. The gm and total harmonic distortion of the VIC are 213.3 μA/V and –63.5 dB, respectively. Figure 2.12(a) shows the input impedance of the current comparator versus the input frequency. Apparently, the input impedance is very low at low input frequency. The transition analysis of the current comparator is shown in Fig. 2.12(b). If the differential input current is 200nA, the evaluation time need about 1.4 nsec after the latch signal setting to high.



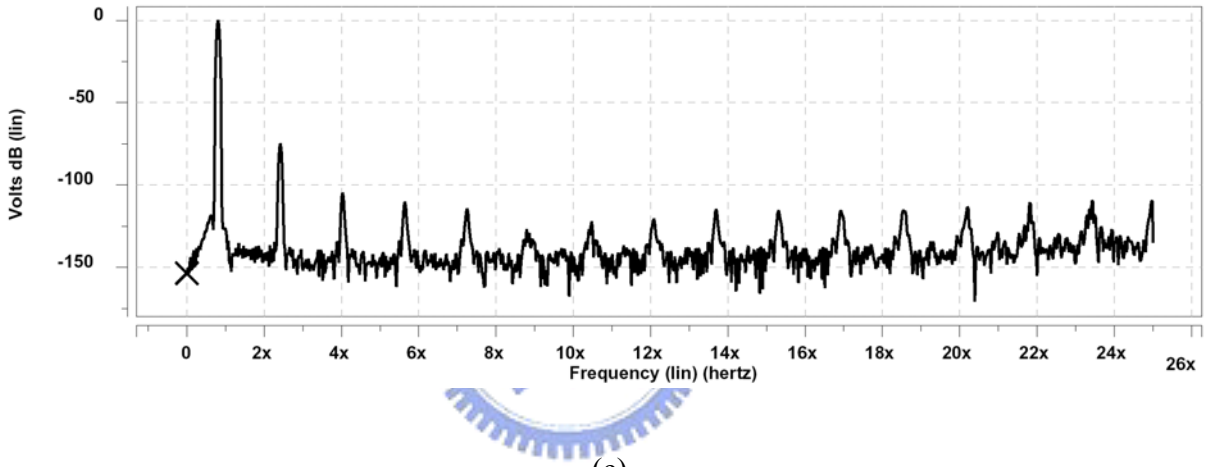
(a)

AC analysis, Gain=1



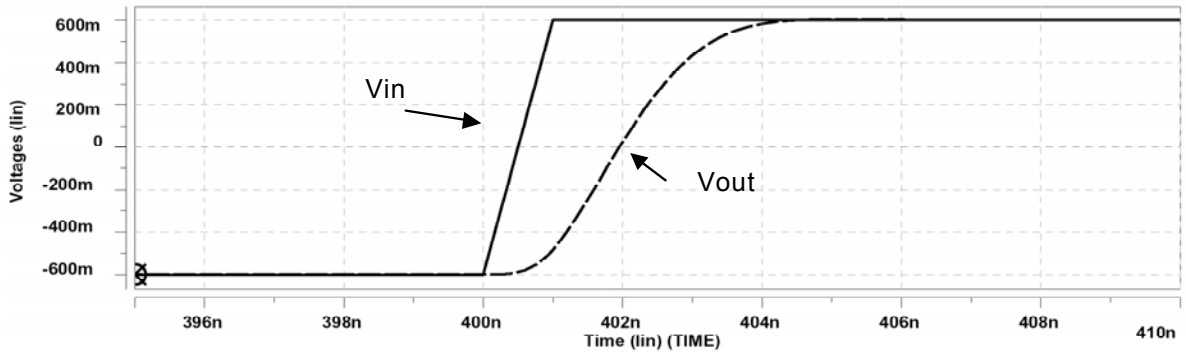
(b)

Input freq.=1 MHz, THD = -75dB



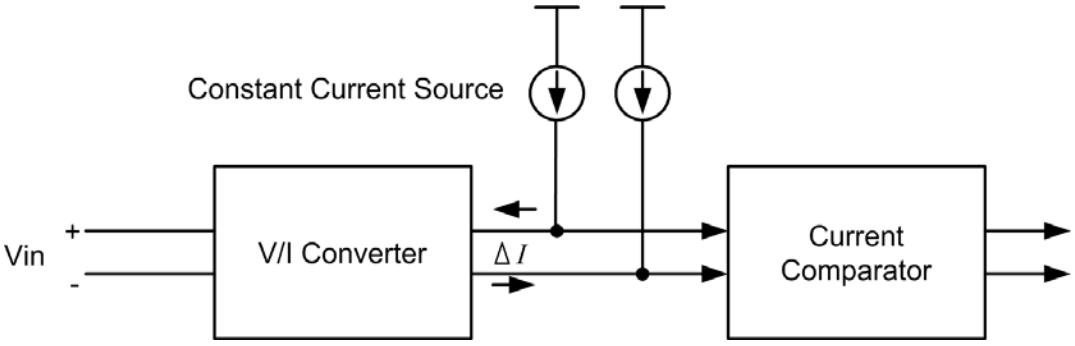
(c)

Slew Rate = 235.3 V/μs



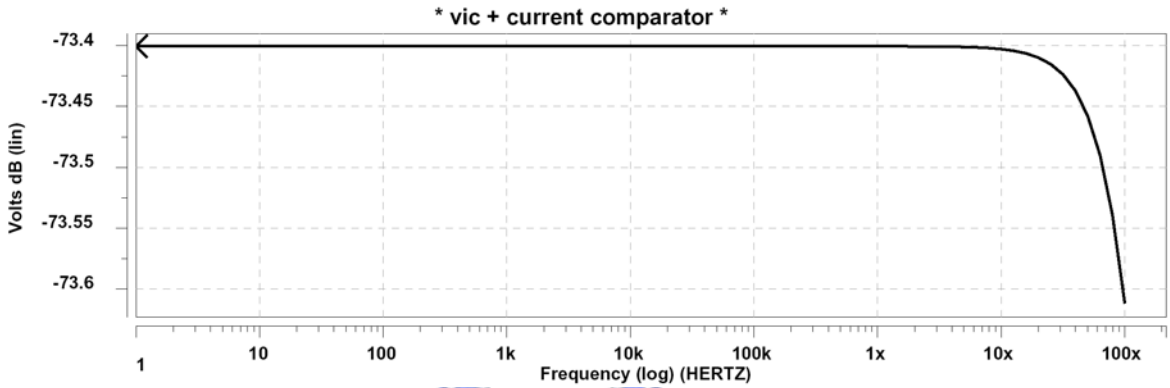
(d)

Figure 2. 10 (a) The block diagram of simulation, (b) ac analysis, (c) linearity analysis (d) slew rate analysis.



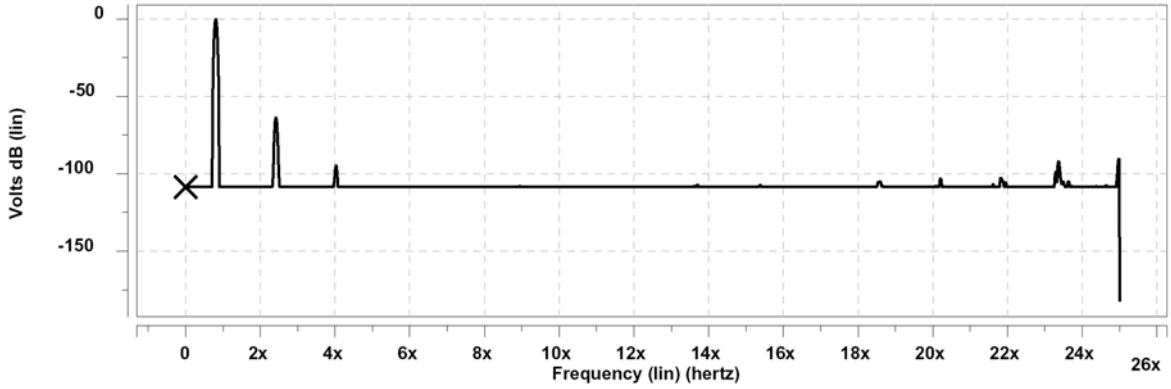
(a)

gm = 256μA/1.2V = 213.3μA/V



(b)

THD=-63.5 dB

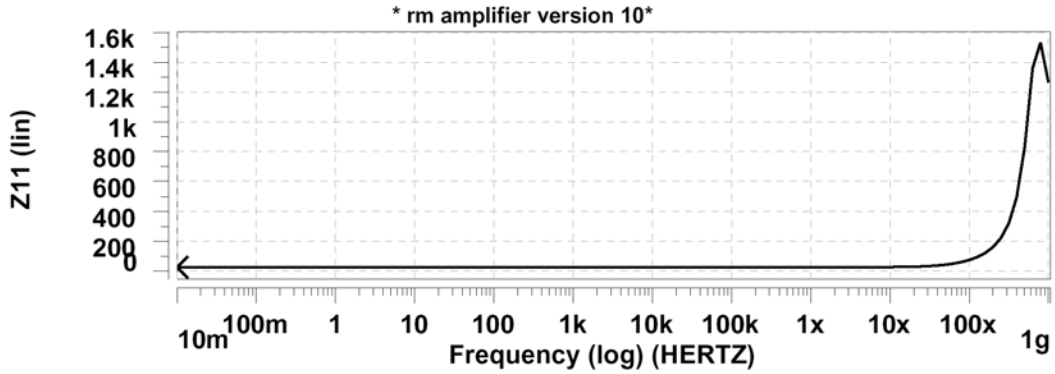


(c)

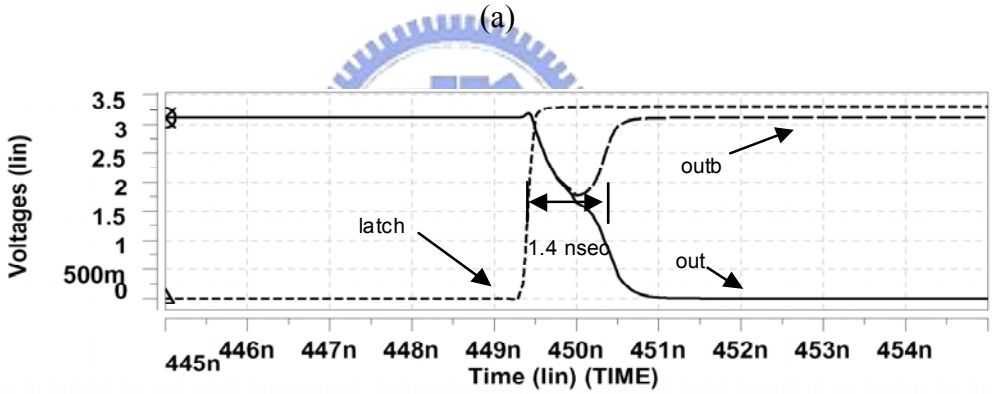
Figure 2. 11 (a) The simulated condition of the VIC, (b) AC analysis, (c) linearity analysis.

In order to simulate the static characteristic of the proposed pipelined ADC, the step voltage signal is sent to the input of the pipelined ADC. The range of the step input signal is from –0.6V to 0.6V. According to the simulation, there is no missing code in the 256 steps. The LSB bit can be correctly generated as shown in Fig. 2.13. Therefore, the DNL is below unity LSB. The dynamic operation of the proposed pipelined ADC is also by the HSPICE

simulation. The input frequency of the testing signals are 10MHz and 20MHz, and the sampling rate is 71.4 MS/s. According to the result data of the HSPICE simulation, it is feasible to use the 1024 points to perform the FFT analysis by MATLAB software. Figure 2.14 shows the result of FFT analysis when the input frequency is 20 MHz. The SNDR is about 44 dB.



(a)



(b)

Figure 2. 12 (a) The input impedance of the current comparator (b) The transition characteristic of the current comparator.

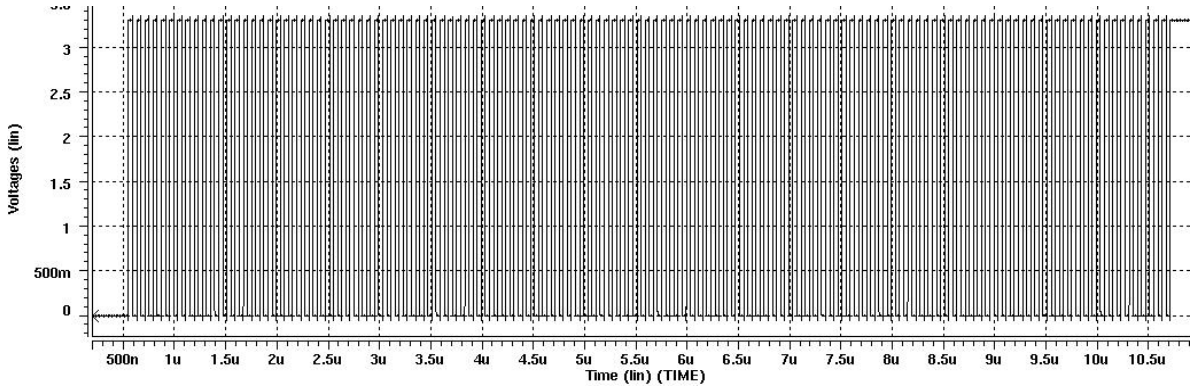


Figure 2. 13 The LSB bit of the output digital codes.

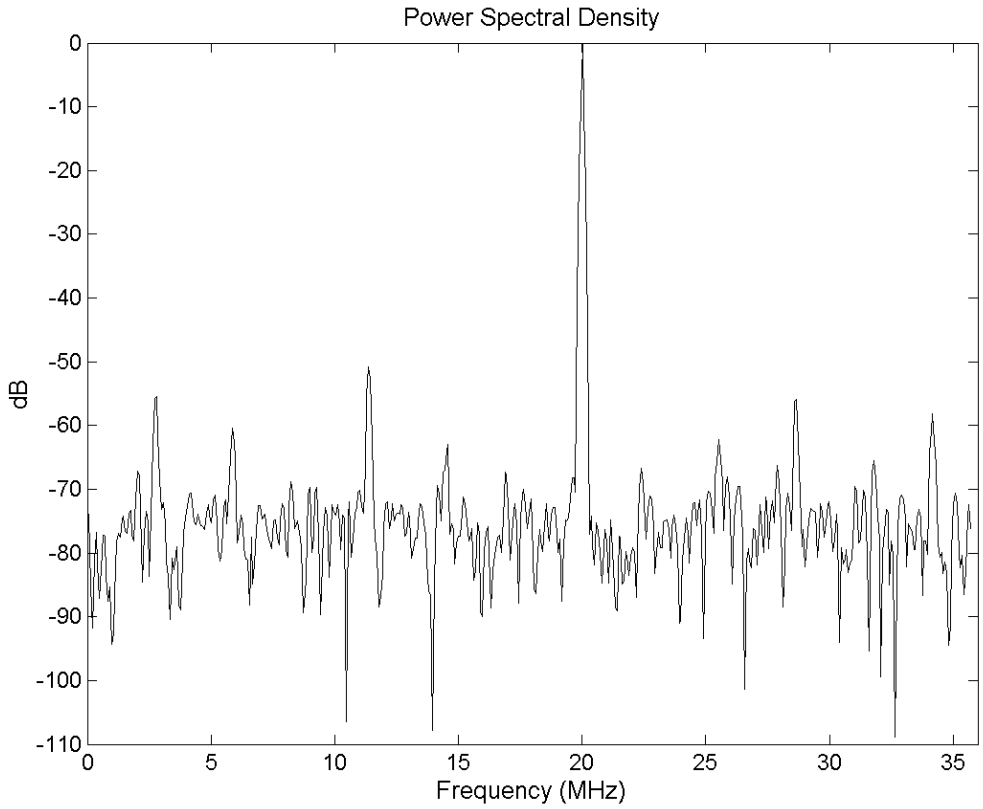


Figure 2. 14 The simulation result of the FFT analysis.

2.3.2 Experimental Results

The measurement setup is shown in Fig. 2.15. The sinusoidal signal is generated by HP 8648C and applied to a band-pass filter to remove any harmonic distortion and noise. Then the pure sinusoidal signal is sent to the test board. The logic analyzer HP16702 stores all digital output codes. All digital data can be collected and analyzed by PC. MATLAB software can be used to analyze the dynamic and static linearity. The topology of the testing board is shown in Fig. 2.16. In the testing board, the single-ended signal is converted to the differential signal by using an OP amplifier (THS4503) that is manufactured by TI. The output codes of the proposed ADC are sent to the logic analysis through the digital output buffer IC (74HC541). The digital output buffer ICs (74HC541) have enough driving capability to drive the instrument. Figure 2.17 shows the photograph of the testing board. The chip photograph of

the fabricated ADC is shown in Fig. 2.18.

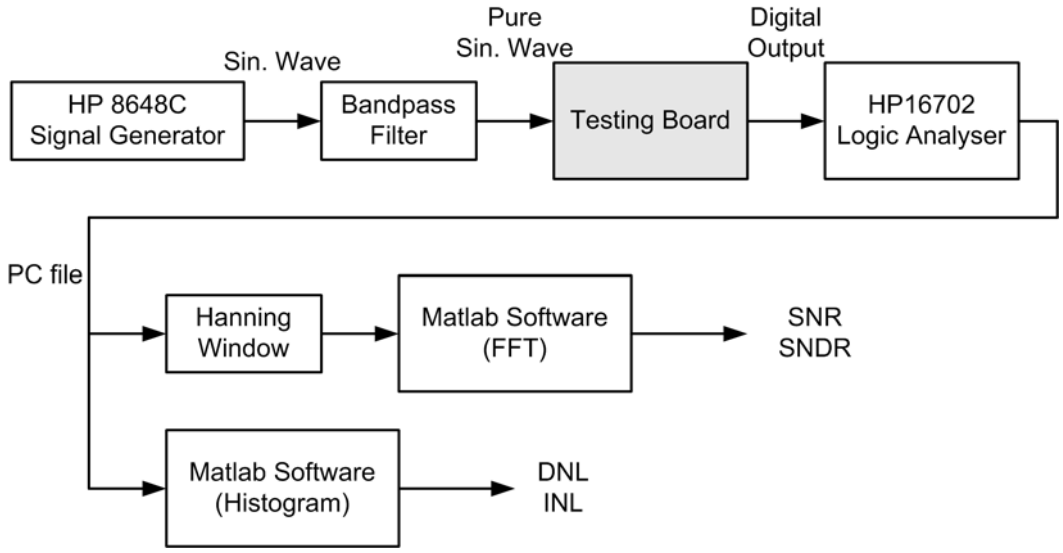


Figure 2. 15 The block diagram of the measurement setup.

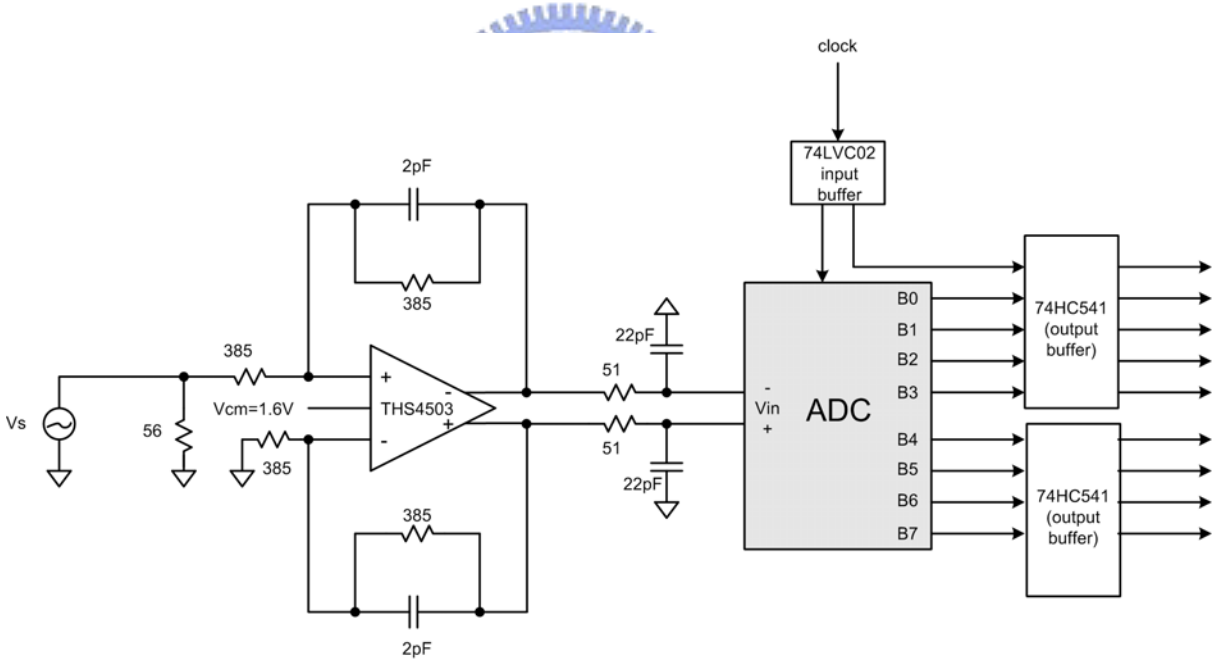


Figure 2. 16 The topology of the testing board.

(a) (b)

Figure 2. 17 (a) Top view of the testing board (b) bottom view of the testing board.

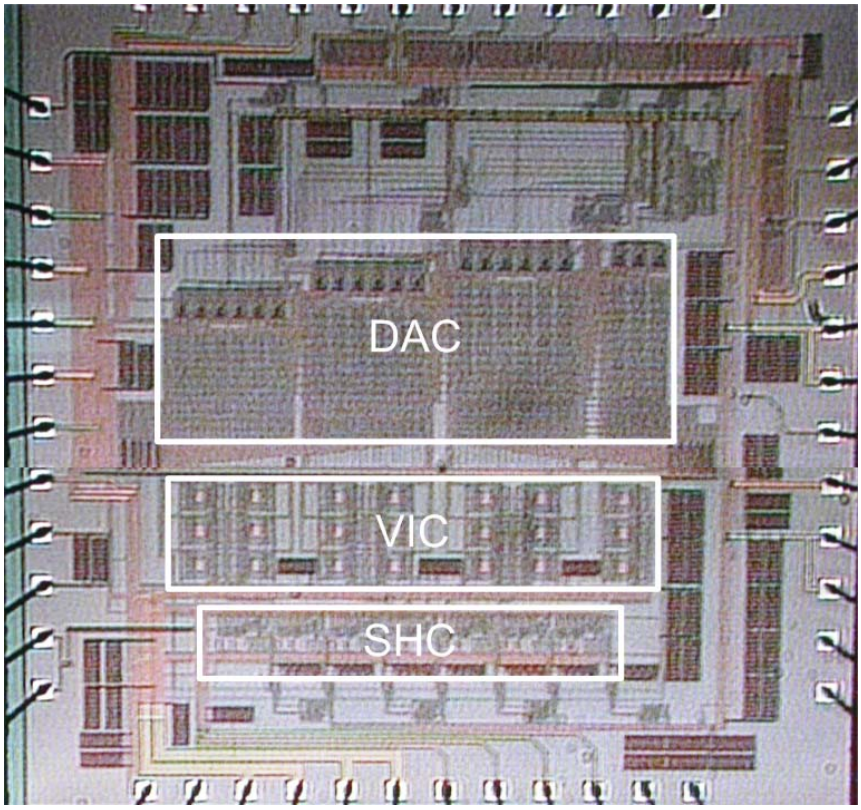
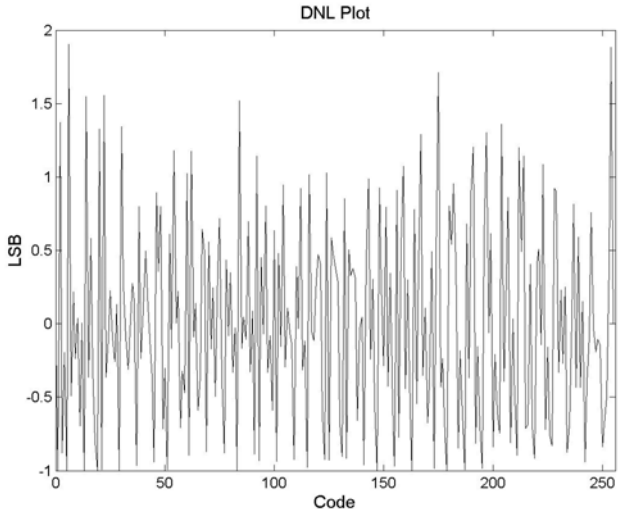


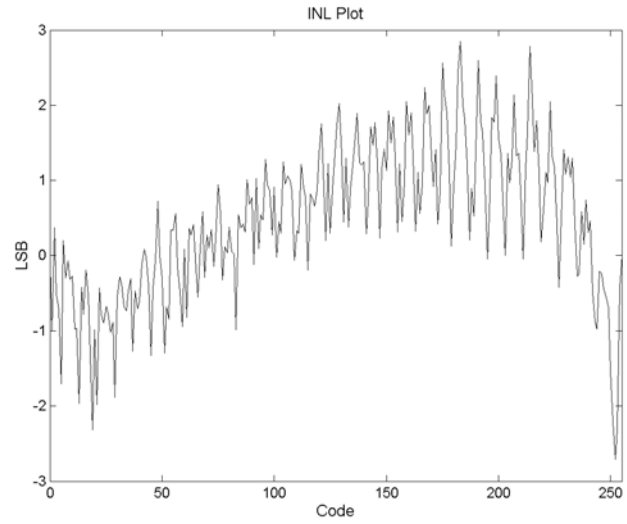
Figure 2. 18 The chip photograph of the fabricated ADC.

By using the sinusoidal histogram method [113], the differential and integral nonlinearity of the proposed ADC measured at 10 MSample/s with a 100 KHz sine input signal are shown in Figs. 2.19(a) and (b), respectively. The differential nonlinearity is within +1.9 and –1 LSB

whereas the integral nonlinearity is within +2.8/-2.8 LSB. The 16384-point FFT plot for a 1 MHz input sine wave at 40 MSample/s is shown in Fig. 2.20. The SNDR is 39.1 dB. The SNDR versus sampling rate plot at 1 MHz input frequency is shown in Fig. 2.21(a). Figure 2.21(b) shows the plot of the input frequency versus SNDR for 40 MHz sampling rate. The SNDR decrease rapidly above 40 MSample/s and decrease quickly when input frequency is increased. The reasons will be discussed in the next paragraph. Figure 2. 21(c) shows the plot of the input frequency versus SNDR under low sampling rate of 6 MS/s. It is shown that the proposed ADC can achieve Nyquist rate operation under low clock rate. Both post-simulated results and major characteristics of the measured chip are listed in Table 2.1.



(a)



(b)

Figure 2. 19 (a) The plot of DNL (b) the plot of INL.

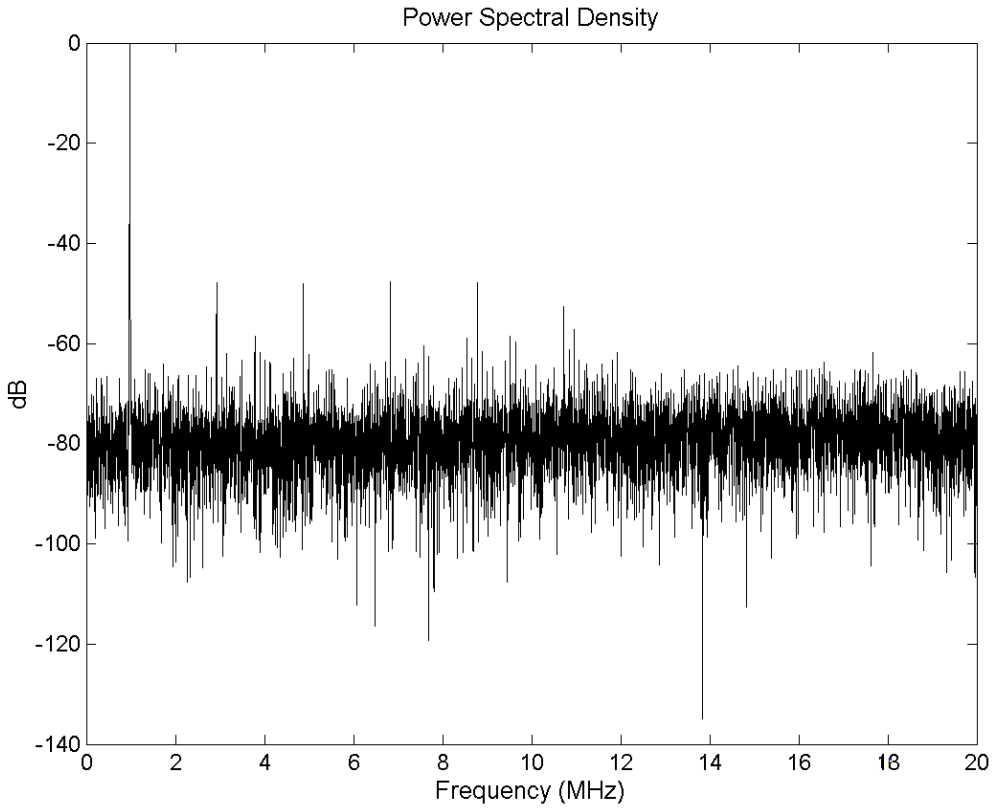
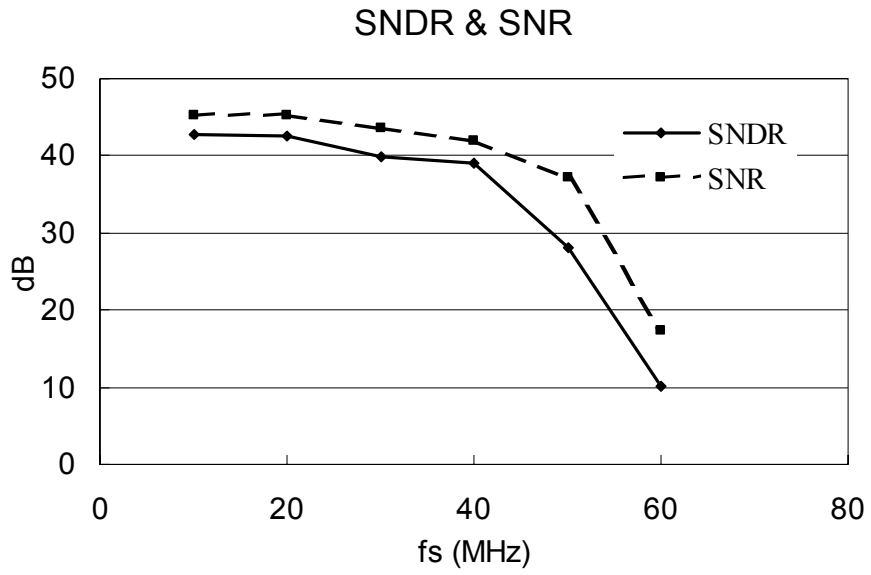
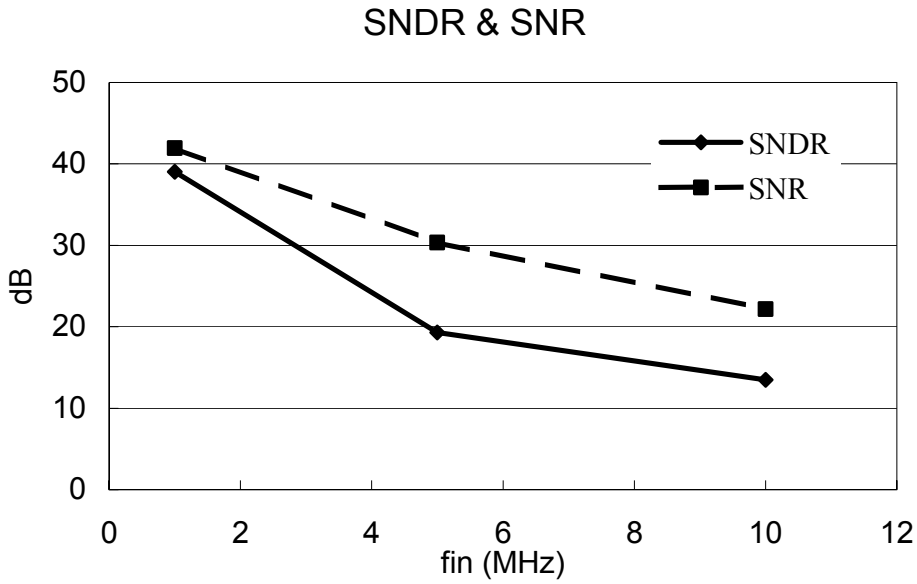


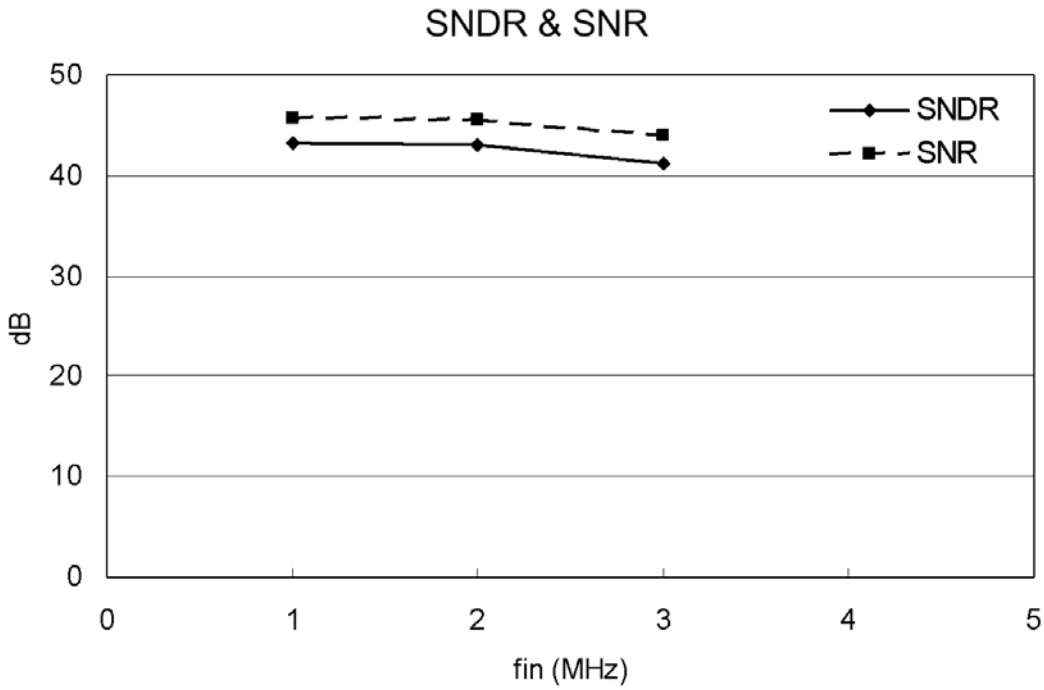
Figure 2. 20 FFT plot for 1 MHz input frequency at 40 MSample/s.



(a)



(b)



(c)

Figure 2. 21 (a) SNDR versus sampling rate plot at 1 MHz input frequency, (b) the plot of the input frequency versus SNDR for 40 MHz sampling rate, (c) the plot of the input frequency versus SNDR under low sampling rate of 6 MS/s.

Table 2. 1 The comparison of post-simulated and measured results for the proposed ADC

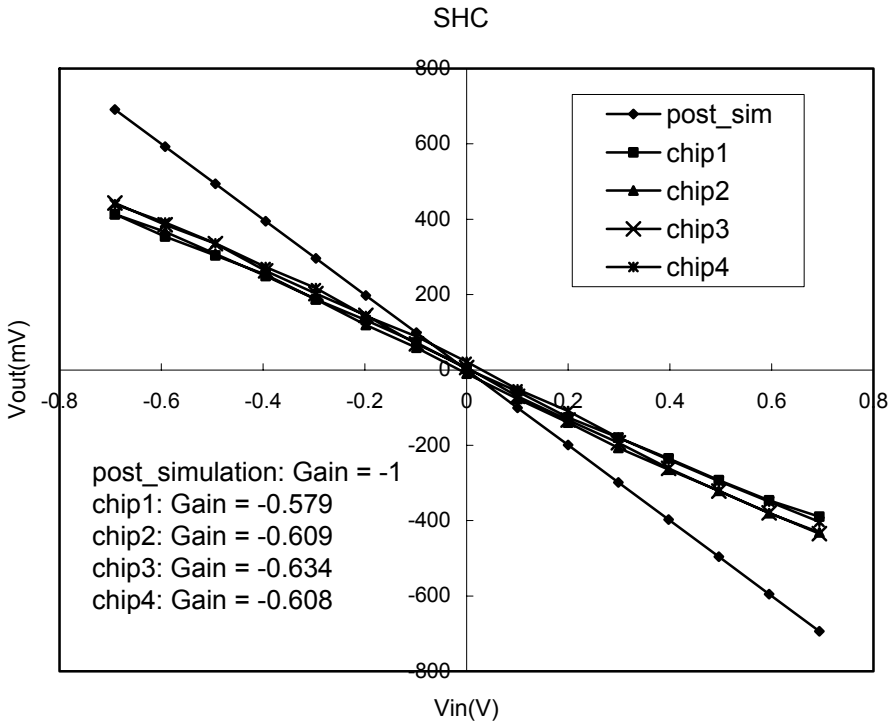
	Post-simulation	Measured
Technology	0.25 μm 1P5M CMOS (Thick oxide is selected) (Minimum channel length is 0.35 μm)	
SNDR	44.0 dB (ENOB=7-bit) (f_s = 71.4 MS/s, f_{in} = 20 MHz)	39.1 dB (ENOB=6.2-bit) (f_s = 40 MS/s, f_{in} = 1 MHz)
DNL	-1/+1 LSB	+1.9/-1 LSB (f_s = 10 MHz @ f_{in}=100 KHz)
INL	-1/+1 LSB	+2.8/-2.8 LSB (f_s = 10 MHz @ f_{in}=100 KHz)
Pipelined Stages	4	4
Full Scale Voltage	1.2 V	1.2 V
Full Scale Current	256 μA	256 μA
Unit LSB Current	1 μA	1 μA
Power Dissipation	205 mW	※ 195 mW
Power Supply	3.3 V	3.3 V
Chip Area	3.2 x 3.0 mm^2	3.2 x 3.0 mm^2

※ bias1 of current comparator is 2.27V

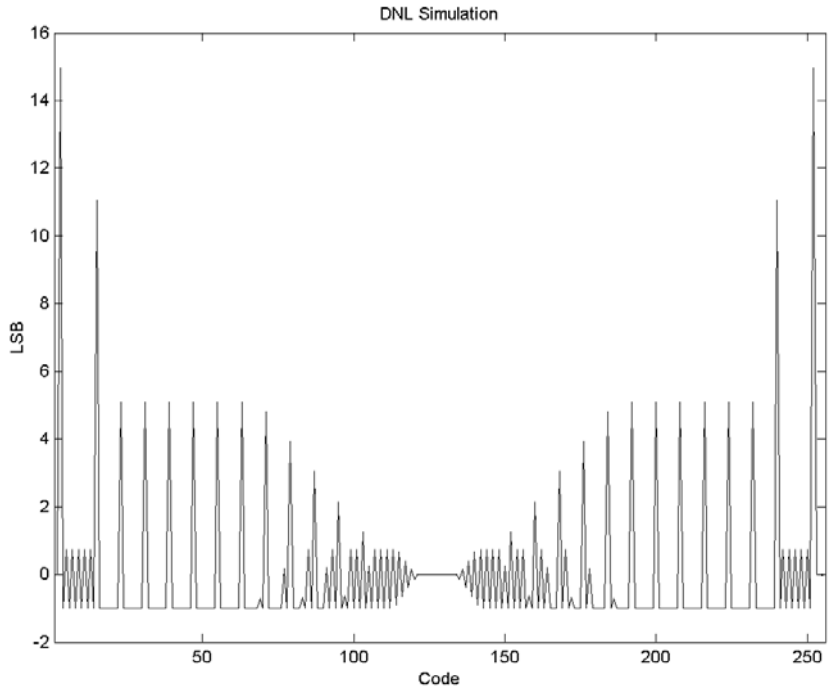
2.3.3 Discussion

A. Gain error

Since the proposed ADC adopts open-loop structure to implement the voltage SHC, the precise unity gain of the SHC is difficult to control. The gain of the SHC is very sensitive to the process variation. Figure 2.22(a) shows the measured results of the SHC. The SHC consists of 4 cascade SHC stages. The gain is the total gain of 4 cascade SHC stages. Obviously the measurement results deviate from the post-simulation results. Figure 2.22(b) shows the impacts of SHC gain error on the differential linearity (DNL) for the proposed ADC. It is based on MATLAB simulation and the gain of the SHC chain is assumed 0.579. The DNL is serious affected and up to +15 LSB.

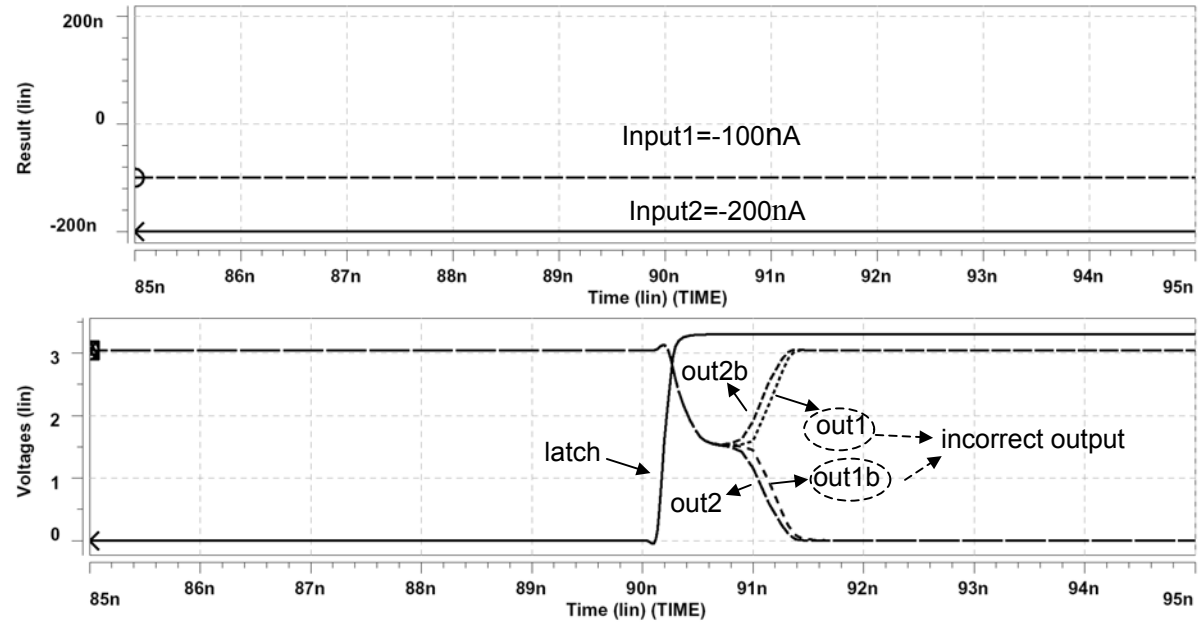


(a)

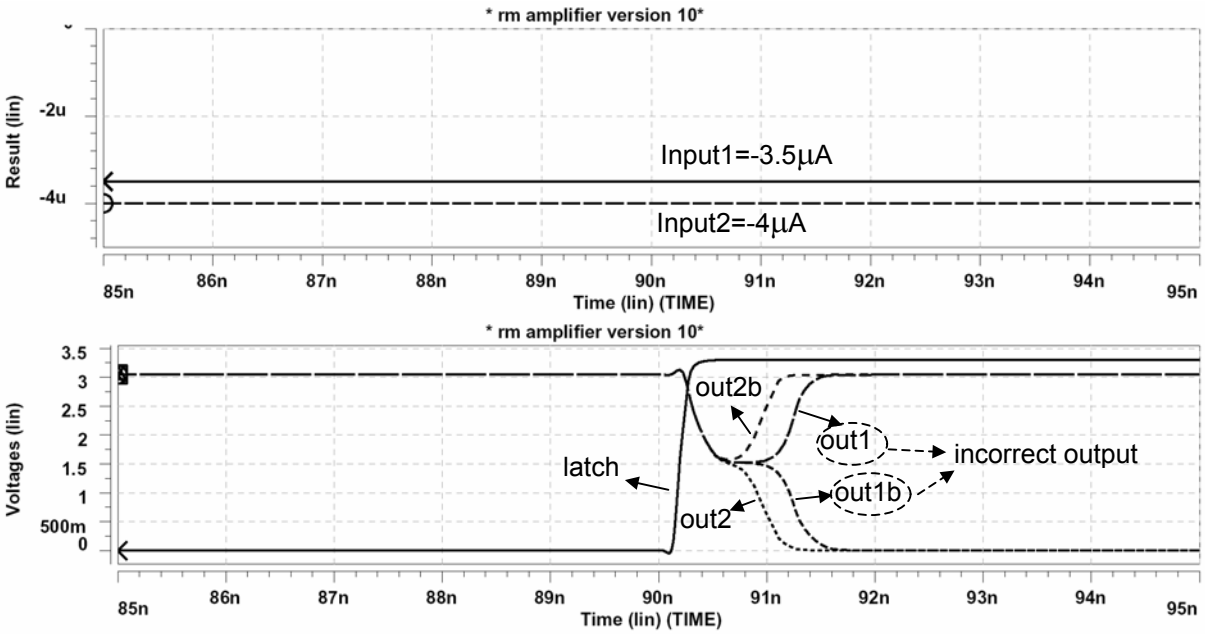


(b)

Figure 2. 22 (a) The measurement results of the test key for SHC (b) the impacts of SHC gain error on the differential linearity (DNL).



(a)



(b)

Figure 2. 23 The post-simulation results of the current comparator (a) under device perfect matching (b) under device size mismatch of 2%.

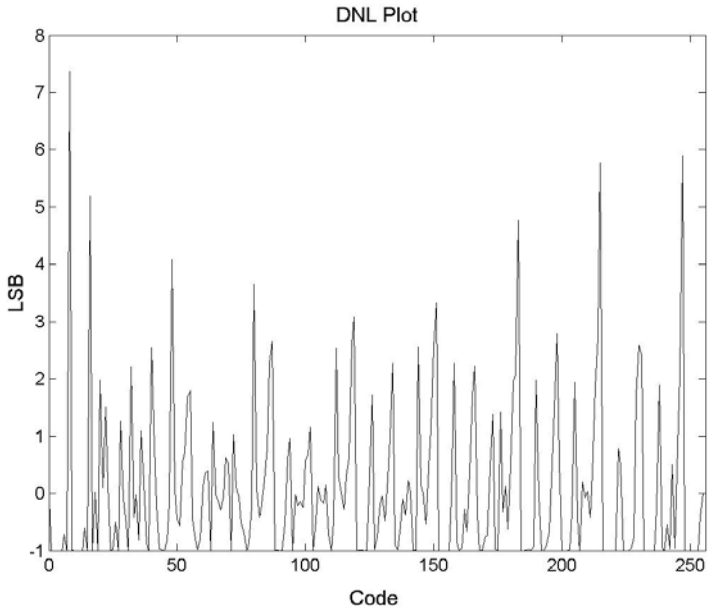


Figure 2. 24 The DNL plot (when bias1 is 2.0V for the current comparator).

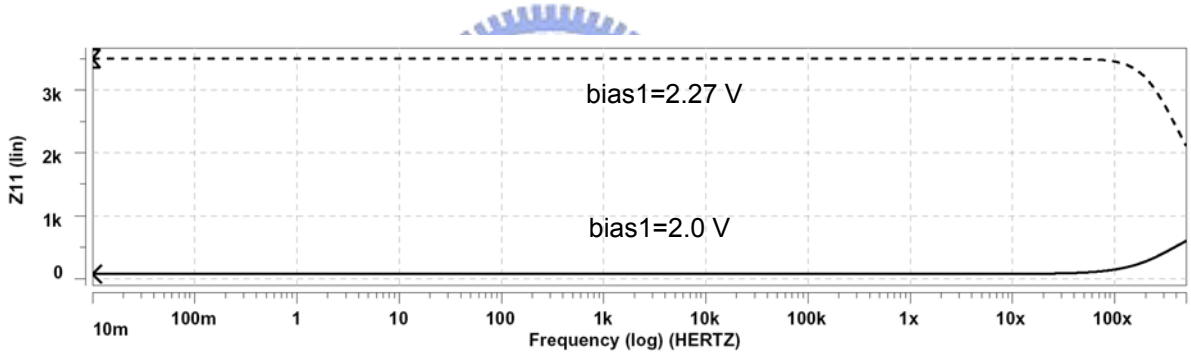


Figure 2. 25 The input impedance of the current comparator for two kinds of condition.

B. Current comparator offset

The accuracy of the current comparator in the final stage must be 8-bit resolution since successive approximation algorithm is adopted to implement the ADC process. Therefore, the input offset current of the current comparator that is shown in Fig. 2.9 severely impacts the linearity of the proposed ADC. Figure 2.23(a) shows the post-simulation results of the current comparator that is shown in Fig. 2.9 under devices perfect matching. The current comparator cannot recognize the differential current below 200 nA. When the MOS transistors M1 and

M2 have device size mismatch of 2% in Fig. 2.9, the post-simulation results of the current comparator are shown in Figure 2.23(b). It is shown that the current comparator cannot recognize the differential current below 4 μA under 2 percent device size mismatch. In order to overcome the input offset current of the current comparator, the bias voltage, bias1, of the Fig. 2.9 can be tuned from 2.0 V to 2.27 V to increase the transimpedance gain of the current comparator. According to the measurement results, the DNL of the proposed ADC is +7.5/-1 LSB as shown in Fig. 2.24 when the bias1 is 2.0V. But the DNL can decrease to +1.9/-1 LSB as shown in Fig. 2.19(a) by tuning the bias1 to 2.27V. However, the input impedance of the current comparator also increases when the bias1 is from 2v to 2.27V. Figure 2.25 shows the input impedance under two kinds of the bias1 condition. Apparently, the input impedance is increased several ten times. This phenomenon affects the settling time of the input current and the dynamic performance of the proposed ADC. It can explain the appearance things of the measurement results in Fig. 2.21.

2.4 Summary

A new architecture is proposed for the design of high-speed pipelined ADC. In the proposed new architecture, open-loop voltage sampling structure and current-mode structures for subtraction, sub-DAC operation, and comparison are used to improve the speed performance of pipelined ADC. The post-simulated results show that the proposed pipelined ADC architecture can be applied to the design of ADC with 8-bit accuracy at a sampling rate up to 71.4MS/s. The delay per pipelined stage is determined by those of voltage SHC, VIC, and current comparator where voltage SHC and VIC dominate. If the dominant delay could be reduced significantly, the speed of the proposed new ADC architecture can be greatly improved. Due to the gain error of the SHC and the input offset current of the comparator, the measurement results of the prototype chip show the differential nonlinearity (DNL) and integral nonlinearity (INL) for all codes are less than +1.9/-1 LSB and + 2.8/-2.8 LSB,

respectively. The dynamic test shows that the effective number of bit (ENOB) is 6.2-bit under 40-MSample/s sampling rate. Therefore, the gain calibration and comparator offset cancellation techniques can be used to improve the speed and accuracy performance in the future research.