

# Chapter 3

## New Current-Mode Full Wave-pipelined Architectures for High-Speed Analog-to-Digital Converters

### 3.1 Introduction

Current-mode signal processing techniques have been extensively adopted in several applications that involve low-power, high-speed or complex arithmetic computation in integrated circuits. Such applications include data converters, filters and cellular neural networks [44]-[45], [48]-[49]. As described in chapter 1, current-mode ICs have several important features. First, current-mode circuits can easily implement the basic functions of inversion, scaling, and summation, without using OP Amps [46]. Second, the voltage swing required in current-mode circuits is smaller than that required in voltage-mode circuits, due to the square I-V law of MOS transistors operated in the saturation region. Third, the current switch can achieve high-speed operation in many applications. These three features make the high-performance current-mode design feasible.

So far, many high-speed digital-to-analog converters (DACs) have been successfully implemented using the current steering technique [52]-[56]. Several current-mode analog-to-digital converters (IADCs) have been also developed [84]-[107]. Among them, the pipelined IADC structure [93]-[107] has exhibited high-speed performance. Especially in the work of [107], 32 parallel pipeline IADCs were used and each IADC was run at 125 MSample/s. The overall IADC can achieve 4Gsample/s at 6-bit resolution under calibration and at an input frequency of 1 GHz.

In a pipelined IADC, the current sample-and-hold (S/H) circuit is the most critical component. It limits both the accuracy and the conversion rate of the IADC. The current S/H circuit (SHC) is normally based on the switch-current (SI) technique. However, the switch clock feedthrough problem in SI circuits is more serious than that in switch-capacitor circuits because any error voltage produced on the gate of the current-holding transistor causes a large current error, according to the square current law. Although many circuit techniques have been proposed to improve the SI structure, a long period is still required to cancel the clock feedthrough effect [95]. Consequently, the accuracy and high-speed are traded-off in the current SHCs (switched-current circuits).

Wave-pipelined theory has been successfully adopted in regular digital systems, such as DRAM, SRAM, and digital multipliers, among others, [114]-[118] to achieve high-speed performance. In this work, wave-pipelined theory is applied to analog-to-digital converter (ADC) design [109], [110] as the first application of the theory to analog IC design. One novel wave-pipelined architecture called full WP-IADC (FWP-IADC) is proposed and analyzed. The full current-mode wave-pipelined structure is used in each stage of the FWP-IADC, without inter-stage switched-current cell circuits. The wave-pipelined architecture are analyzed and simulated by HSPICE. The proposed FWP-IADC is shown to achieve 55 MS/s (fs) with 8-bit resolution under an input frequency of 27.5 MHz. When the input frequency is 3 MHz, the conversion rate can achieve 90 MS/s with 8-bit resolution. Moreover, measured results of the experimental chip have successfully verified the function of FWP-IADC.

The rest of this chapter is organized as follows. Section 3.2 describes the architectures and the design considerations of the wave-pipelined IADC (WP-IADC). Section 3.3 explicates the circuit design. Section 3.4 presents the experimental results and discussions. The post-simulation results of the modified FWP-IADC are shown in Section 3.5. Finally,

Section 3.6 gives the summary.

### 3.2 Full Wave-Pipelined ADCs

This chapter proposes wave-pipelined architectures to improve the speed of the IADC. The proposed FWP-IADC is designed without inter-stage SI circuits. Figure 3.1 presents the underlying concept of the wave-pipelined ADC system. In Fig. 3.1, the inter-stage SHCs have been removed from the ADC system. A delayed clock, instead of a global clock, controls the digital registers, except in the first stage. Figure 3.2 displays a conceptual block diagram of the proposed FWP-IADC. An 8-bit structure is considered as an example. The 8-bit IADC consists of one voltage input S/H circuit, one voltage-to-current (V/I) conversion circuit, one pre-stage, seven identical 1-bit pipelined stages, and one final current comparator. The voltage input SHC is used to generate the sample-data waveforms of the input voltage  $V_{in}$ , whereas the V/I converter is used to convert the voltage waveforms into current waveforms as  $I_{in}$ . Accordingly, sample-data waveforms of the input high-frequency current signals can be generated.

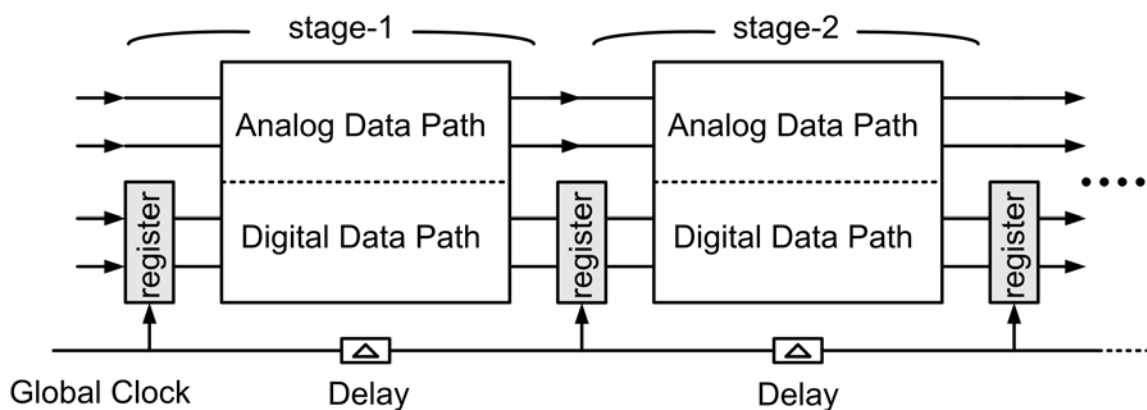


Figure 3. 1 Wave-pipelined ADC system.

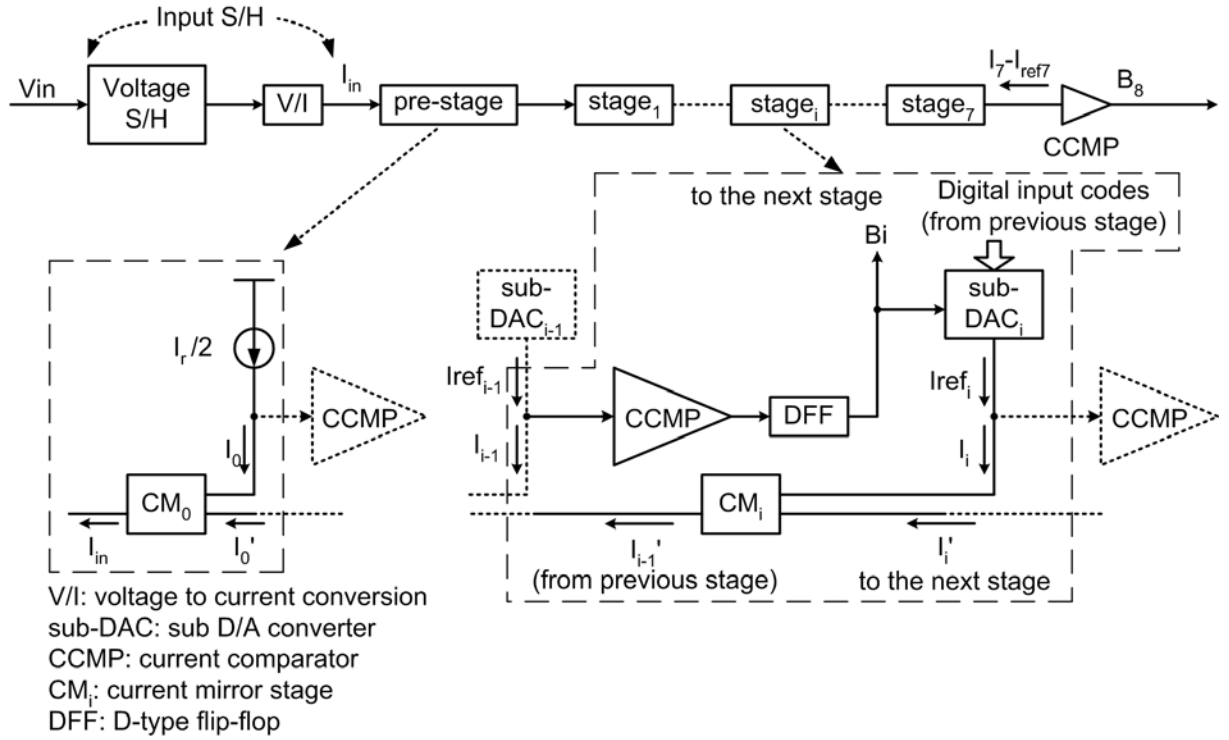
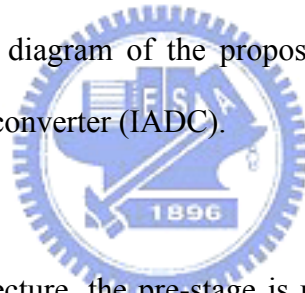


Figure 3. 2 Conceptual block diagram of the proposed 8-bit wave-pipelined current-mode analog-to-digital converter (IADC).



In the FWP-IADC architecture, the pre-stage is used to generate the difference current between the reference current  $I_r/2$  and the current signal  $I_0$ . The difference current is sent to the current comparator of stage<sub>1</sub>. Meanwhile, the current mirror stage  $CM_0$  is used to reproduce the input current  $I_{in}$  as  $I_0$  and  $I_0'$ . Each 1-bit pipelined stage includes one current mirror stage ( $CM_i$ ), one current comparator (CCMP), one D-type flip-flop (DFF) and one current-mode digital-to-analog sub-converter (sub-DAC<sub>i</sub>), as shown in Fig. 3.2. The current mirror stages  $CM_i$  are used to reproduce and propagate the input current  $I_{i-1}'$  to  $I_i$  and  $I_i'$ , with an appropriate delay to match that in the path of CCMP, DFF and sub-DAC<sub>i</sub>. The input current of the current comparator is the resultant current  $I_{i-1} - I_{refi-1}$  of the last stage. If current  $I_{i-1}$  is greater (smaller) than  $I_{refi-1}$ , then the corresponding bit  $B_i$  is set to logic ONE (ZERO). The output bit  $B_i$  is stored in the D-type flip-flop (DFF). After  $B_i$  is determined, the digital

output  $B_i$  is sent to the following stage and serves as the input signal of the sub-DAC $_i$ . The digital input signals of sub-DAC $_i$  are the output digital signals of all CCMPs in the preceding pipelined stages, as well as  $B_i$ . These signals are converted into the output current signal  $I_{ref_i}$ . The sub-DAC $_i$  output current  $I_{ref_i}$  is determined by the following rule used to implement the ADC process, in a manner similar to the successive approximation algorithm [43].

$$I_{ref_i} = \frac{I_r}{2^{i+1}} + \sum_{k=1}^i B_k \cdot \frac{I_r}{2^k} \quad i = 1 \sim 7 \quad (3.1)$$

where  $I_r$  represents the current reference and  $0 \leq I_{in} \leq I_r$ .  $I_{ref_i}$  is subtracted from  $I_i$  by directly connecting the corresponding nodes. Then the resultant current  $I_i - I_{ref_i}$  is sent to the current comparator of the next pipelined stage. After  $I_{ref_i}$  is generated, the output current  $I_i'$  and the resultant current  $I_i - I_{ref_i}$  are sent to the following stage. The above description establishes that the analog-to-digital conversion process can be implemented by the architecture presented in Fig. 3.2. After complete conversion,  $I_{in}$  can be expressed by the output digital bits as,

$$\begin{aligned} I_{in} &= B_1 \frac{I_r}{2} + B_2 \frac{I_r}{4} + \dots + B_8 \frac{I_r}{2^8} \\ &= I_r (B_1 \cdot 2^{-1} + B_2 \cdot 2^{-2} + \dots + B_8 \cdot 2^{-8}) \end{aligned} \quad (3.2)$$

Notably, the CM $_i$  path allows the input current to propagate throughout the pipelined stages without sampling or holding operations during the implementation of the wave-pipelined structure.

Figure 3.3 details the structure of the proposed FWP-IADC. Three separate signal paths, path A, path B and path C, are identified to explain the control of the timing of the wave-pipelined structure. Path A is the analog propagation path. It includes a CM $_i$  stage. The CM $_0$  stage has two current mirror circuits since the CM $_0$  stage is used only to reproduce the input current  $I_{in}$  as  $I_0$  and  $I_0'$ , as shown in Fig. 3.4. In Fig. 3.4, the other CM $_i$  stages are composed of an analog delay element and a current mirror. The analog delay elements are inserted into path A to provide a suitable delay for the analog signals, since the analog signals must be synchronized with the signal of path B to perform a correct subtraction.

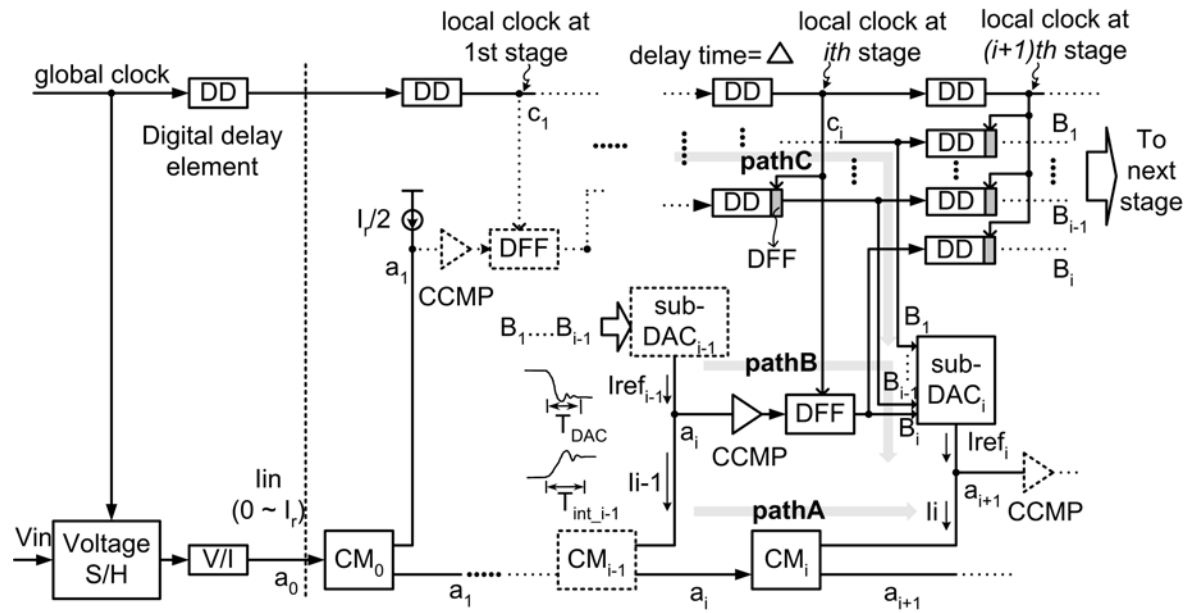


Figure 3. 3 Detailed structure of the wave-pipelined IADC.

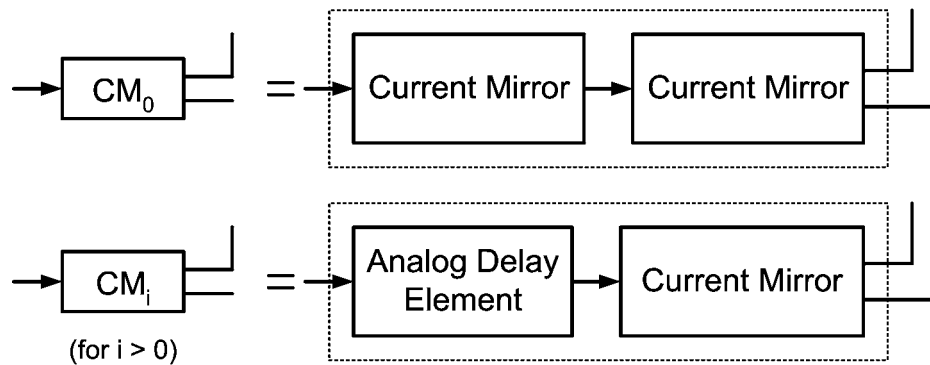
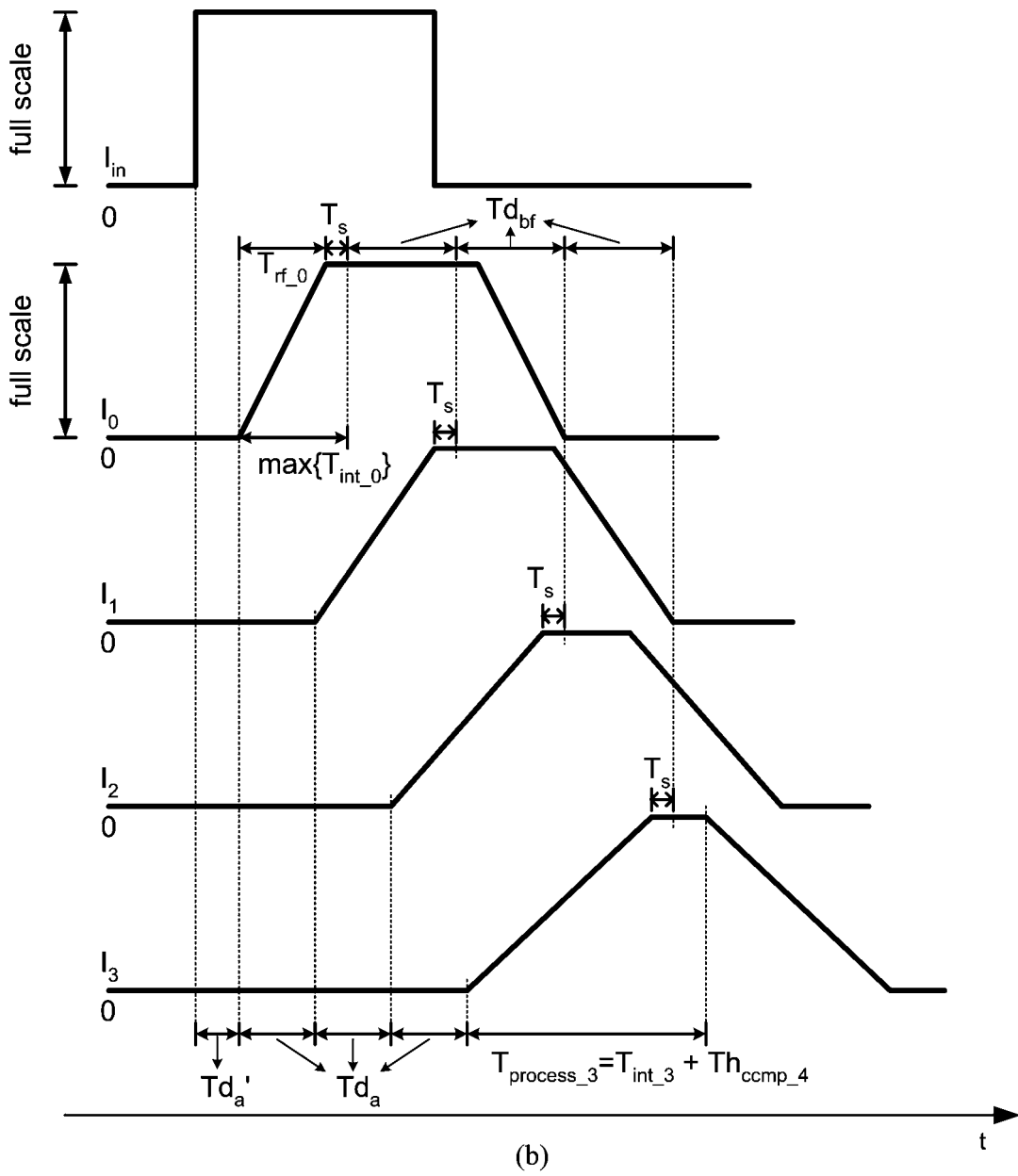
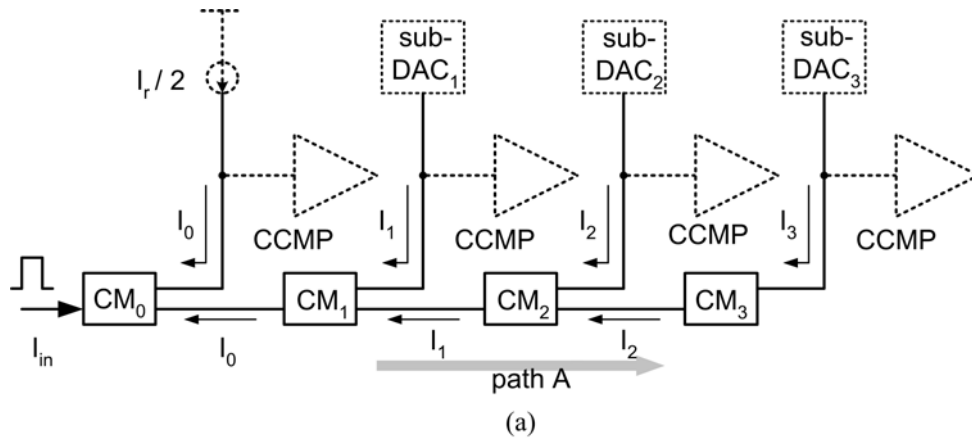


Figure 3. 4 Function block of the CM block.

Path B includes current-mode sub-DACs, CCMP, and DFF. In path B, the DFF latches the output of the current comparator, which is then sent to the subsequent sub-DAC. The DFF is needed to equalize the delay of path B in each stage because the comparison time of the current comparator depends on the amplitude of the input signal. The equally delayed clock signal from path C controls the DFF. Thus, the DFF can latch the data during the identical period.



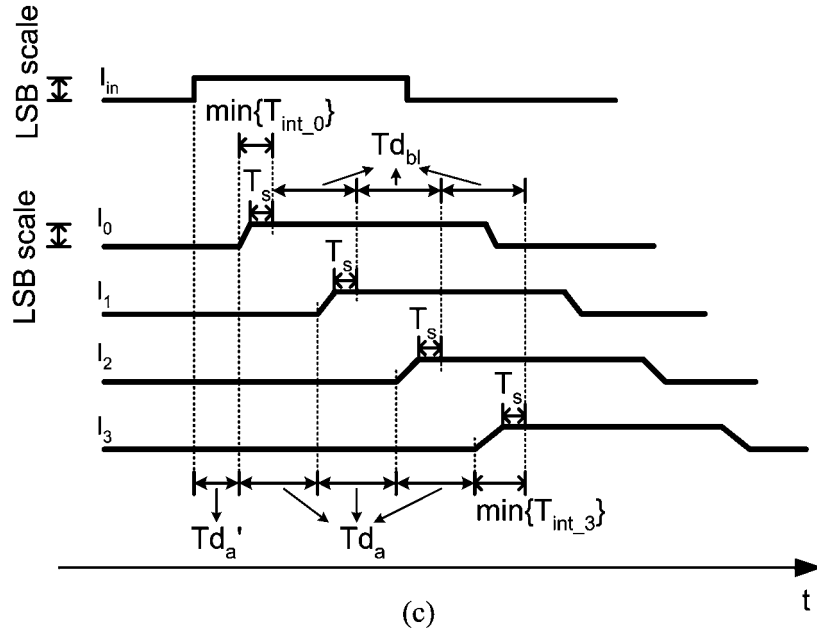


Figure 3. 5 (a) Four stage example of the wave-pipelined structure. (b) Output current waveforms of the  $CM_i$  stage for full scale input swing. (c) Output current waveforms of the  $CM_i$  stage for LSB scale input swing.

Path C is the path along which the digital signals propagate through the digital delayed elements (DD). The input signals  $B_1, \dots, \text{and } B_{i-1}$  are sent into the  $i$ th DAC through the digital delay elements in path C. After the final stage, all the digital bits can be sent out in parallel.

In general, the analog data paths A and B in Fig. 3.3 dominate the propagation delay in each stage. The characteristics of the signals in path A and path B must be detailed to determine the maximum speed of the proposed FWP-IADC. In particular, two practical considerations related to path A must be addressed in a real design. One is the rise/fall time of current signals in every  $CM_i$  stage. The other is the intrinsic delay of a current mirror.

Figure 3.5(a) shows the structure of path A in the FWP-IADC with  $CM_0$  and three identical  $CM_i$  stages. The current signal  $I_i$  is the output current signal of the  $CM_i$  stages, where  $i$  is between 0 and 3. Figures 3.5(b) and 3.5(c) show the output current waveforms of the  $CM_i$



stage when the swings of the input current signals are full scale and LSB scale, respectively. In Figs. 3.5(b) and 3.5(c),  $T_{d_a}$  is the delay between when  $I_i$  and  $I_{i+1}$  start to rise from the initial zero value.  $T_{d_{bf}}$  and  $T_{d_{bl}}$  are the delays between when  $I_i$  and  $I_{i+1}$  settle to their final values in full scale and LSB scale swing, respectively. As the figures indicate, the rise times of the current signals that propagate through each  $CM_i$  stage are increased. Therefore, the delay times,  $T_{d_{bf}}$  and  $T_{d_{bl}}$ , do not equal  $T_{d_a}$ . However, neither  $T_{d_{bf}}$  nor  $T_{d_{bl}}$  vary among stages because the increased rise/fall time is the same in every stage. Moreover, if the swing of the input current is smaller, then  $T_{d_b}$  is closer to  $T_{d_a}$ . According to Figs. 3.5(b) and 3.5(c),  $T_{d_{bf}}$  and  $T_{d_{bl}}$  represent the two extreme cases.  $T_{d_{bf}}$  is the maximum delay, whereas  $T_{d_{bl}}$  is the minimum.

The intrinsic delay of the current mirror is one of factors that limits the speed. In the  $CM_i$  stage, when the input current signal of the final current mirror changes from the present value to the next value, the output current  $I_i$  follows the change of the input current. The output current signals  $I_i$  take the rise/fall time ( $T_{rf\_i}$ ) plus the settling time ( $T_s$ ) to reach their final stable value. During this period, the input current signal of the current mirror cannot be changed. Consequently, the time for which the input current signal must be held constant can be defined as the intrinsic delay  $T_{int}$  of the current mirror. Hence, the intrinsic delay  $T_{int\_i}$  of the current mirror in the  $CM_i$  stage can be written as follows.

$$T_{int\_i} = T_{rf\_i} + T_s \quad i = 0 \sim 3 \quad (3.3)$$

Notably,  $T_{rf\_i}$  increases with  $i$  and  $T_s$  is constant in each stage. Moreover, the intrinsic delay  $T_{int\_i}$  is maximum and minimum when the input swing is full and LSB scale, respectively. The intrinsic delay of a current mirror exceeds that of a simple logic gate since the circuit of a current mirror is more complicated than that of a logic gate and the required accuracy of the output signal in the current mirror is higher. From Fig. 3.5(b), the relationships among the maximum  $T_{int\_i}$  in each  $CM_i$  stage can be explained as follows.

$$Td_a' + \max\{T_{int\_0}\} + Td_{bf} = Td_a' + Td_a + \max\{T_{int\_1}\} \quad (3.4)$$

This equation can be extended to general form.

$$Td_a + \max\{T_{int\_i}\} + Td_{bf} = Td_a + Td_a + \max\{T_{int\_i+1}\}$$

$$\max\{T_{int\_i}\} = \max\{T_{int\_i+1}\} - (Td_{bf} - Td_a) \quad i = 0 \sim 3 \quad (3.5)$$

From Fig. 3.5(c), the following equation is valid for minimum  $T_{int\_i}$ .

$$\min\{T_{int\_0}\} + 3Td_{bl} - \min\{T_{int\_3}\} = 3Td_a \quad (3.6)$$

As shown in Fig. 3.3, the output currents  $I_i$  of the  $CM_i$  stages are subtracted from the output current  $I_{ref_i}$  of the sub-DAC in the  $i$ th stage and the residue current is sent into the current comparator of the next stage. Thus, the output current signal of the  $CM_i$  stage after the settling down must be held constant for the process of comparator. The total processing time  $T_{process\_i}$  of the last current mirror in each  $CM_i$  stage can be defined as follows.

$$T_{process\_i} = T_{int\_i} + Th_{ccmp\_i+1} \quad i = 0 \sim 3 \quad (3.7)$$

In Eq. (3.7),  $Th_{ccmp\_i+1}$  is the input signal hold time of the current comparator in the  $(i+1)$ th stage.

In Fig. 3.5(b), only the total processing time  $T_{process\_3}$  of the final current mirror in the  $CM_3$  stage is shown.  $T_{int\_i}$  increases with  $i$  since  $T_{rf\_i}$  increases with  $i$ . At the final stage,  $Th_{ccmp}$  is the maximum because the input signal of the current comparator is less than 1 LSB. Thus,  $T_{process\_3}$  has the largest value because both  $T_{int\_i}$  and  $Th_{ccmp}$  have the maximum value in the example of four wave-pipelined stages.

According to the above discussion, the space-timing diagram of the analog data path A can be drawn and shown in Fig. 3.6(a). The vertical axis represents the data depth in path A and the labels  $a_i$  and  $c_i$  indicate the corresponding nodes in Fig. 3.3. The boundaries of the

shaded regions in Fig. 3.6(a) depict the flow of data through the data path A under the minimum delay case and worst delay case. Thus, the shaded regions of each data processed at  $nT_{clk}$  for  $n = 0, 1, \dots$  must not overlap one another and the minimum required time spacing is  $Th_{ccmp\_4}$  and  $\min\{T_{int\_3}\}$  so that the previous datum remains unchanged during the period  $Th_{ccmp\_4}$  to protect the correct functioning of the comparator, whereas the next LSB-swing datum requires  $\min\{T_{int\_3}\}$  time to set up. This constraint is expressed as,

$$T_{clk} + \min\{T_{int\_0}\} + Td_a' + 3Td_{bl} - \min\{T_{int\_3}\} \geq \max\{T_{int\_0}\} + Td_a' + 3Td_{bf} + Th_{ccmp\_4} \quad (3.8)$$

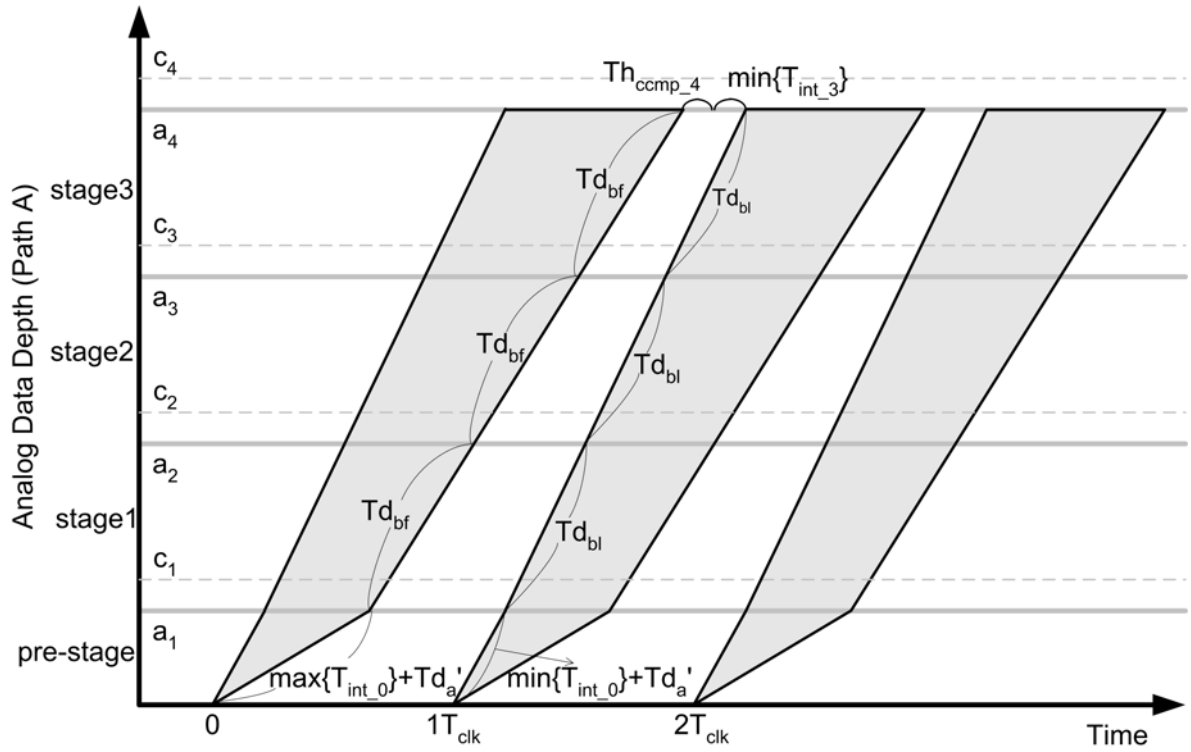
where  $T_{clk}$  is the global sampling clock period. Substituting Eq. (3.6) into Eq. (3.8) yields  $T_{clk}$  as,

$$T_{clk} \geq \max\{T_{int\_0}\} + Th_{ccmp\_4} + 3(Td_{bf} - Td_a) \quad (3.9)$$

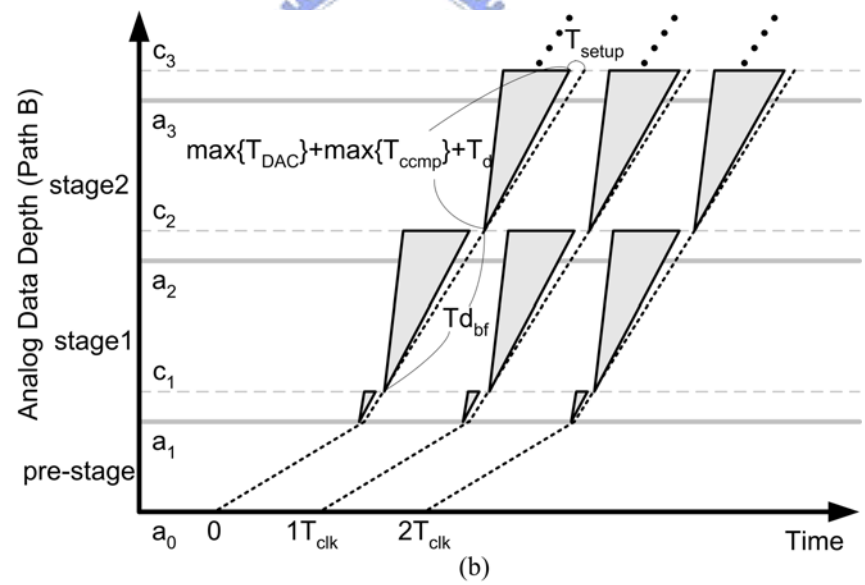
In Eq. (3.9), the first term on the right-hand side is contributed by the maximum intrinsic delay time of the final current mirror in  $CM_0$  stage. The second term is associated with the hold time of the input signal of the current comparator after stage3. The third term is related to the different rise/fall times of the output currents among the  $CM_i$  stages. If the rise/fall times of the output current are same for every  $CM_i$  stage, the third term can be set to zero. Therefore, the minimum value of  $T_{clk}$  is limited by the maximum value of intrinsic delay of the current mirror and the hold time of the current comparator. Furthermore, substituting Eqs. (3.5) and (3.7) into Eq. (3.9) yields  $T_{clk}$  in the following form.

$$T_{clk} \geq \max\{T_{process\_3}\} \quad (3.10)$$

Therefore, the maximum speed of the global clock of the path A in the proposed FWP-IADC is limited by the maximum total processing time of the last current mirror in the final  $CM_i$  stage because the rise/fall time of the output current of the  $CM_i$  stage gradually increases from stage to stage.



(a)



(b)

Figure 3. 6 (a) Space-timing diagram of the analog data path A. (b) Space-timing diagram of the analog data path B.

As may be seen from Fig. 3.5(b),  $T_{d_{bf}}$  is the maximum delay between stages  $CM_i$  and  $CM_{i+1}$  in the path A. In the path B of Fig. 3.3, the current comparator CCMP, DFF and the  $i$ th sub-DAC must generate the output current  $I_{ref_i}$  during  $T_{d_{bf}}$ . In the final stage, the delay time

$T_{DAC}$  of the sub-DAC is maximum since the changing swing of the output current  $I_{ref_i}$  in the  $i$ th sub-DAC is closer to the swing of the input current of the ADC than the one of sub-DAC in previous stage. The current comparator also has the maximum comparison time  $T_{ccmp}$ . Thus in path B, the global sampling clock period  $T_{clk}$  and the maximum delay  $T_{d_{bf}}$  must be satisfied the following relation.

$$T_{clk} \geq T_{d_{bf}} \geq \max\{T_{DAC}\} + \max\{T_{ccmp}\} + T_d + T_{setup} \quad (3.11)$$

where  $T_d$  and  $T_{setup}$  are the delay time and the set up time of the DFF, respectively. Figure 3.6(b) shows the space-timing diagrams of path B. Figure 3.6(b) shows a data depth of only three stages. The dashed lines indicate the clock delay through the clock delay unit. Clearly, that the process of the sub-DAC, the comparison of the current comparator, and the delay of DFF, must be accomplished during time  $T_{d_{bf}}$ .

The clock and digital data delay time  $\Delta$  of the digital path C in Fig. 3.3 must equal  $T_{d_{bf}}$ , because the digital data are aligned by the DFF that is controlled by the local clock. In general, the digital delay elements can be implemented easily. Therefore, path C is not critical to the design of FWP-IADC.

The maximum global sampling rate of FWP-IADC is decided according to Eqs. (3.9) and (3.11). If path B, as given by Eq. (3.11), dominates  $T_{clk}$ , then a suitable number of current mirrors must be inserted into the analog delay elements in each  $CM_i$  stage to increase the delay time  $T_{d_{bf}}$  and satisfy Eq. (3.11). If the overall delay in path B is smaller than that in path A in Eq. (3.9), then Eq. (3.9) determines  $T_{clk}$  and the number of current mirrors in analog delay elements can be decreased. In the extreme case, only two current mirrors in each  $CM_i$  stage are required. In this case, the term  $(T_{d_{bf}} - T_{d_a})$  can be reduced and the maximum sampling rate is increased.

The proposed FWP-IADC can also be designed in multi-bits per stage to decrease the

total number of  $CM_i$  stages. According to Eq. (3.10), the sampling rate can be further increased by reducing the total number of  $CM_i$  stages. Furthermore, the redundant digital bits can be used to implement the digital error correction function in the structure of multi-bits per stage.

The results of the above analysis reveal that the proposed FWP-IADC architecture has several advantages. Firstly, the efficiency of timing usage is improved. In the conventional switched-current pipelined structure [93]-[107], the half of the period  $T_{clk}$  is required to track signals, whereas the other half of this period is used to hold the signal. If the tracking time does not equal the holding time, then the efficiency of timing usage is poor. However, in the proposed FWP-IADC structure, the entire clock period is used for signal processing. Timing is used efficiently. Secondly, the signal path includes no inter-stage switched-current circuits. The proposed FWP-IADC eliminates the nonlinearity factor that is contributed by the switched-current circuits from the signal path. Thirdly, the number of controlled clocks in the FWP-IADC is reduced. Finally, the proposed FWP-IADC can accept a high frequency input signal since the voltage sample-and-hold circuits are used ahead of the V/I conversion circuit.

### **3.3 Circuit Implementation and Simulation Results**

To further verify the proposed new architectures of FWP-IADC, CMOS circuits are used to implement the ADC as a demonstrative example.

#### **3.3.1 Current Mirror Design**

The current mirror is a basic component in the proposed new architectures for FWP-IADC. It acts as a current conveyer, an inverter and an analog delay element. Accordingly, the design of the current mirror is crucial and it is necessary to make sure the gain error must be smaller than 0.5 LSB through eight CM stages. If each CM stage is consist

of ten current mirror, the gain error of current mirror must be smaller than 0.0086. Therefore, high output impedance is required in the current mirror to reduce the gain error. Figure 3.7(a) shows the adopted current mirror circuit with the enhanced output impedance, as proposed by Säckinger et. al. [83]. As shown in Fig. 3.7(a), the MOSFETs M9, M10, M11 and M12, with their associated current sources,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$  and  $I_{B4}$ , are common-source amplifiers that provide negative feedback to the cascoded devices, M1, M3, M6 and M8, respectively, and increase the output resistance of the current mirror. Assuming that the output resistances of current sources  $I_{B2}$  and  $I_{B4}$  are approximately  $r_{ds10}$  and  $r_{ds12}$ , respectively, the final output resistance can be written as,

$$r_{out} = \frac{g_{m3}g_{m10}r_{ds3}r_{ds4}r_{ds10}}{2} // \frac{g_{m8}g_{m12}r_{ds8}r_{ds7}r_{ds12}}{2} \quad (3.12)$$

Moreover, if the current mirror circuits are perfectly symmetrical, the frequency response of current mirror can be derived as,

$$H(s) = \frac{I_{out}}{I_{in}}(s) = \frac{1}{(1 + s \frac{C_g}{g_{m1}g_{m2}g_{m9}r_{ds9}r_{ds2}} + \frac{1}{2} s^2 \frac{C_{x1}C_g}{g_{m1}g_{m2}})} \quad (3.13)$$

where  $C_{x1}=C_{gs1}+C_{gd9}$  and  $C_g$  is the total capacitance including parasitic capacitance from node A to ground in Fig. 3.7(a). As may be seen from Eq. (3.13), the current gain is unity at low frequency with  $s \cong 0$ . The step response  $h(t)$  of the current mirror can be obtained by the inverse Laplace transformation of  $1/s H(s)$  as,

$$h(t) = \left[ 1 - e^{-t/a} \left( \cos ct + \frac{\sqrt{C_g}}{b} \sin ct \right) \right] u(t) \quad (3.14)$$

where  $a = g_{m9}r_{ds9}r_{ds2}C_{x1}$  ;  $b = \sqrt{-C_g + 2g_{m9}^2g_{m1}g_{m2}r_{ds9}^2r_{ds2}^2C_{x1}}$  ;  $c = \frac{b}{a\sqrt{C_g}}$  . From Eq.

(3.14), it can be seen that the constant  $a$  is the most critical factor on time response. If  $a$  is decreased, the time response of current mirror can be improved. To decrease the value of  $a$ ,

$C_{gs1}$  and  $C_{gs3}$  in  $M_1$  and  $M_3$ , respectively, should be kept small.

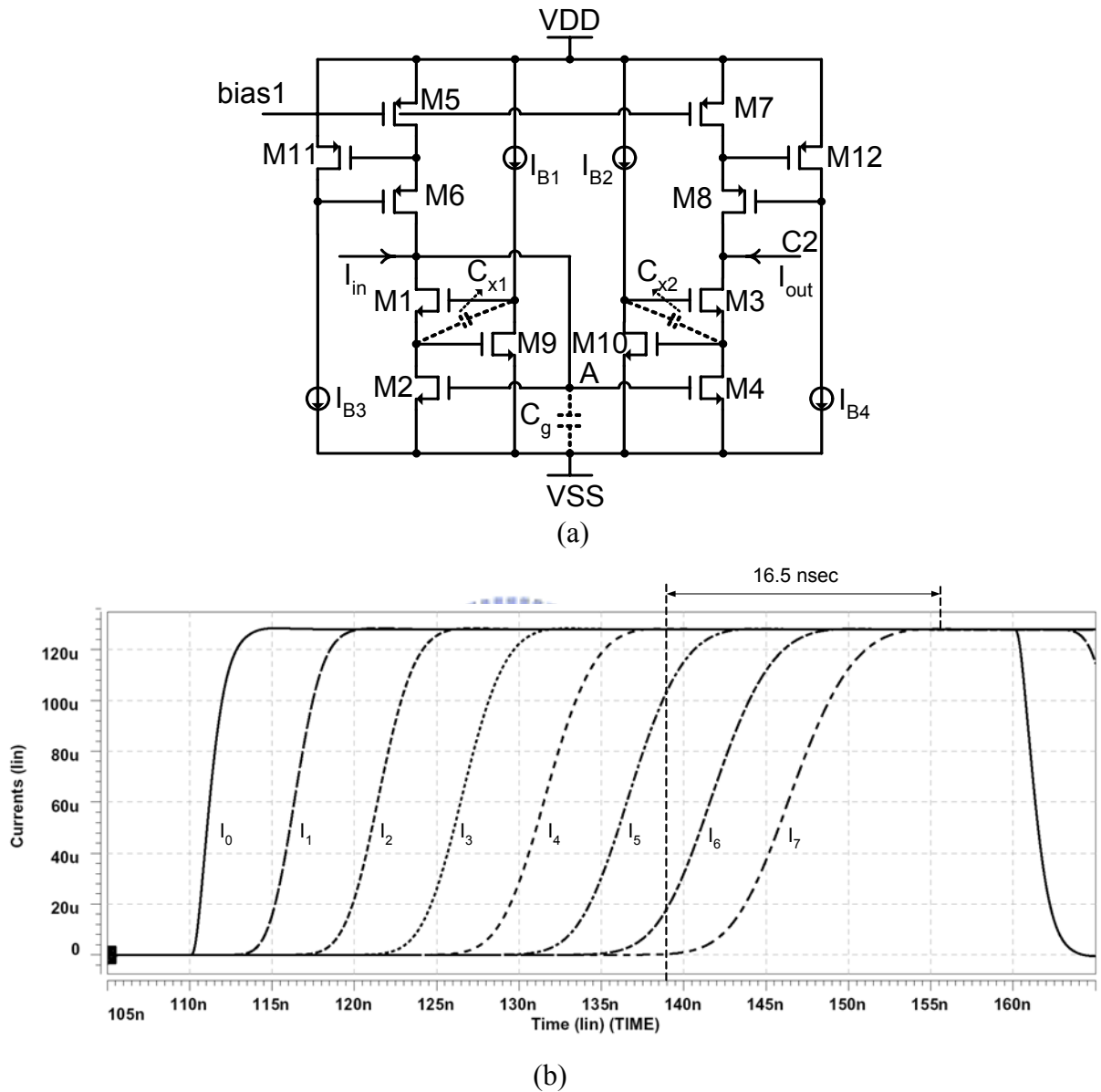


Figure 3. 7 (a) Enhanced output-impedance current mirror. (b) The simulated output current waveforms of the  $CM_i$  stage in FWP-IADC structure with full-scale step input current from 0 to 128  $\mu A$ .

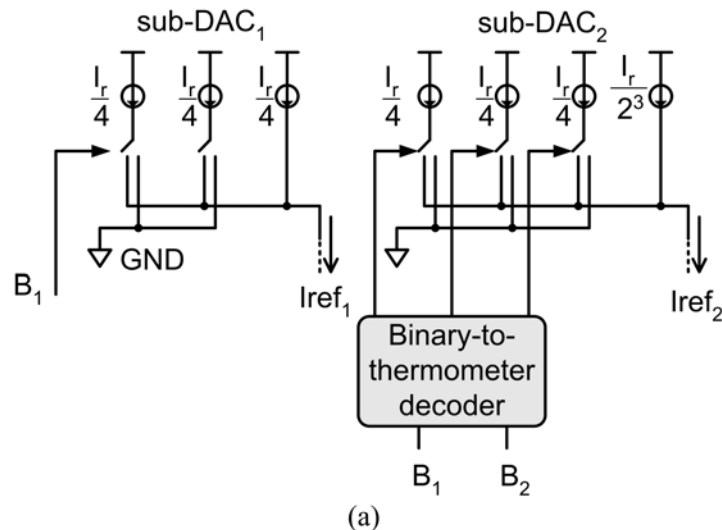
In the FWP-IADC, the current signal through the eight CM stages should have 8-bit accuracy given a suitably designed device size. From HSPICE simulation results, the output resistance of current mirror is about 3 K $\Omega$ . The HSPICE-simulated intrinsic delay of the final current mirror in a CM stage with ten current mirrors is about 16.5 nsec when the input signal



is of full scale ( $0 \sim 128 \mu\text{A}$ ), as may be seen from the simulated waveforms in Fig. 3.7(b).

### 3.3.2 Sub-DACs Design

Figures 3.8(a) and 3.8(b) present the circuit diagrams of current-mode sub-DACs. All sub-DACs are implemented using the current steering structure. From Fig. 3.8(a), the sub-DAC<sub>1</sub> is a 1-bit DAC, which is composed of three identical current sources with magnitudes of  $I_r/4$ . Two current sources are switched by the control signal  $B_1$ , which is the result of conversion of the first stage. If  $B_1=1$  ( $=0$ ), then the two current sources are switched to  $I_{ref_1}$  (GND) to make  $I_{ref_1}=3/4 I_r$  ( $1/4 I_r$ ). The sub-DAC<sub>2</sub> is a 2-bit DAC and the two bits are linearly decoded to become the thermometer code. The  $i$ th sub-DAC has a  $2+(i-2)$  segmented architecture for  $i \geq 3$ , as shown in Fig. 3.8(b). In this DAC, the two most significant bits (MSBs) are linearly decoded whereas the rest of the bits are binary weighted. Using  $2+(i-2)$  segmented architecture greatly reduces the transition time and the glitch problem of the DAC. Furthermore, the threshold-voltage compensation technique [111] and the cascode structure are used to implement the reference current source  $I_{ref}$  to ensure accuracy. The principle of the threshold-voltage compensation technique is illustrated in Eq. (2.4) of chapter 2. Figure 3.8(c) shows the output transition curve of the 7th DAC from  $0.5 \mu\text{A}$  to  $127.5 \mu\text{A}$  in the worst case. It takes 4.5 nsec to settle down to the final stable value with 8-bit accuracy.



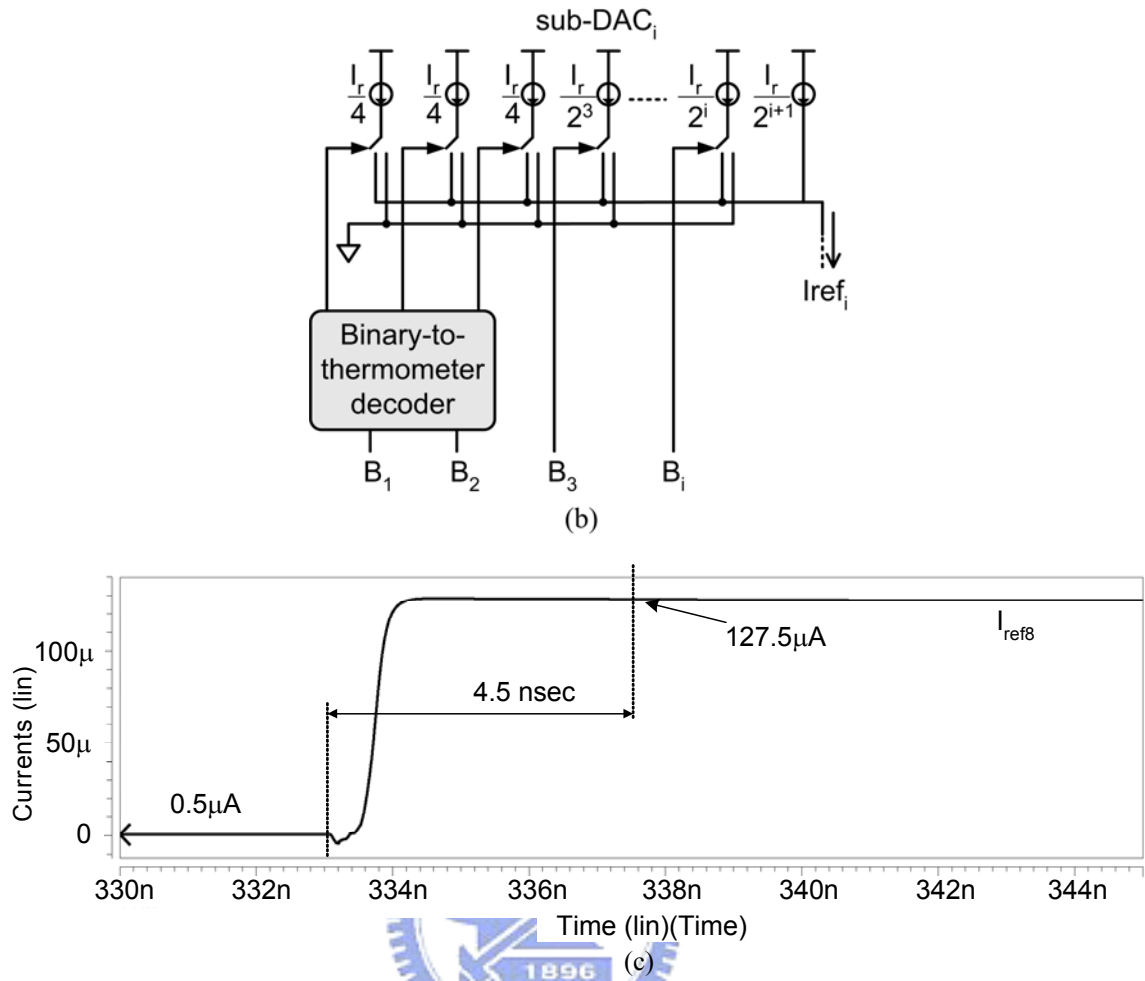


Figure 3. 8 (a) Second and third current-mode sub-DACs. (b) The  $i^{\text{th}}$  sub-DAC. (c) The output transition curve of the 7<sup>th</sup> DAC.

### 3.3.3 Current Comparator Design

There are two attempts of current comparator to use in the FWP-IADC. One is the continuous-time current comparator for the experimental chip. The other is the low-input-impedance current comparator for the modified version of FWP-IADC. Since the continuous-time current comparator need more time to decide the quantization level, the sampling rate of the FWP-IADC is limited by some factors that is analyzed from the previous section 3.2.

### A. Continuous-Time Current Comparator

The continuous-time current comparator [109] can be implemented using the inverter chain without an offset cancellation circuit, as shown in Fig. 3.9(a). The first inverter acts as an  $R_m$  amplifier. The input signal  $I_{in}$  charges or discharges the gate capacitance  $C_{gs}$  of the first inverter, according to the direction of the input signal. Each inverter serves as an inverting amplifier with a gain of  $-g_m r_o$  and amplifies the input voltage. However, the large impedance at the input node causes the significant RC delay of the current comparator. Thus, the frequency performance of the current comparator is degraded. The modified current comparator is shown in Fig. 3.9(b). In the experimental chip of the FWP-IADC, the modified current comparator can be used to serve as the continuous-time current comparator and simplify the design of the demonstrative 8-bit FWP-IADC. Two MOSFETs M1 and M2 are added to the input stage, as shown in Fig. 3.9(b), to solve the degradation of the frequency performance. MOSFETs M1 and M2 can be viewed as two resistors each with a resistance of  $1/g_m$ , where  $g_m$  is the transconductance of M1 and M2, since the gate and drain of M1 and M2 are shorted by M3 and M4. Then, the input impedance can be decreased. The MOS transistors, M1 to M4, can also be viewed as an  $R_m$  amplifier. Moreover, if the sizes of PMOS (M5) and NMOS (M6) devices in the inverter chain are the same as the sizes of M1 and M2, respectively, then the circuit operating point is located on the sharp region of the inverter transfer curve. Thus, the inverting amplifier can have a very high gain and the speed of the current comparator can be improved. From the simulation results, the continuous-time current comparator takes about 10 nsec to amplify an input current of 2 nA. Nevertheless, this kind of current comparator suffers from the problem of the offset voltage, which is discussed in the following section.

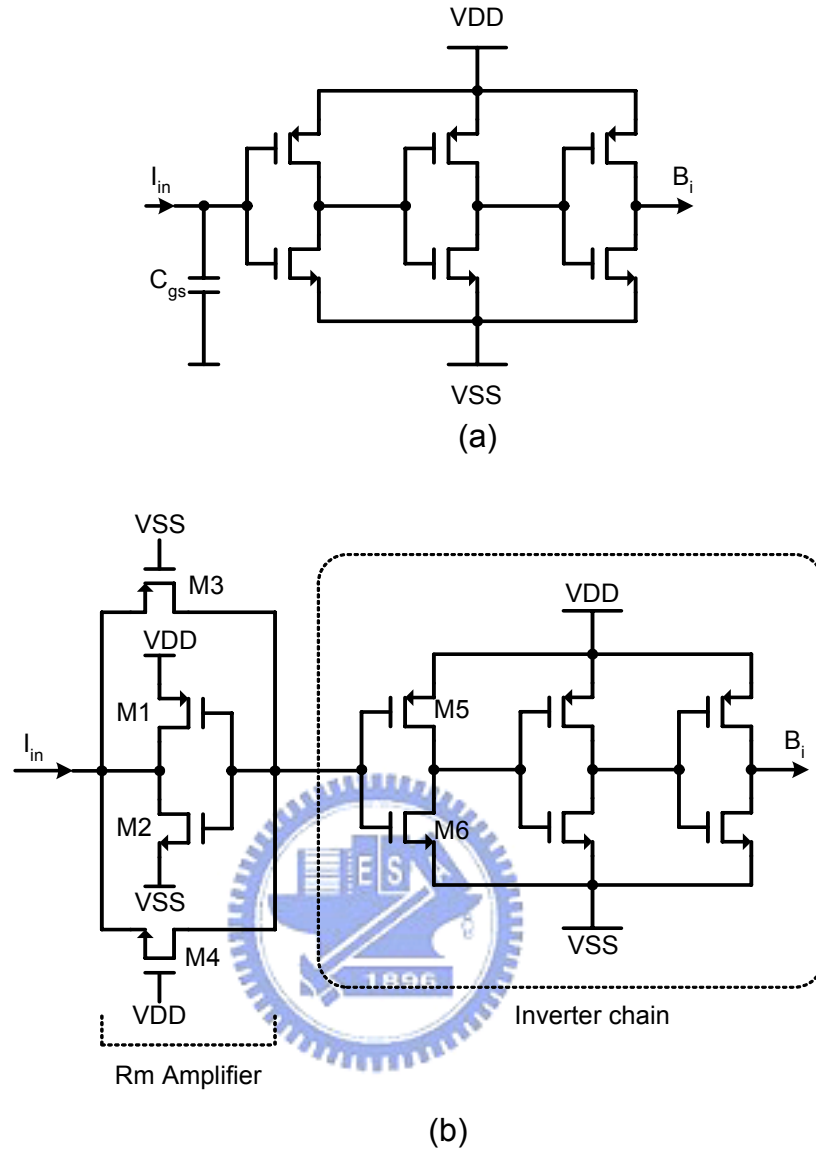


Figure 3. 9 (a) Conventional current comparator and (b) high-performance current comparator.

### B. Low-Input-Impedance Current Comparator

In order to further improve the sampling rate of the FWP-IADC, the low-input-impedance current comparator can be used in the modified FWP-IADC version. Figure 3.10(a) shows the low-input-impedance current comparator circuits [48], [95], [112]. Node B must be connected to dummy MOS transistors, as indicated in Fig. 3.10(a), since the proposed FWP-IADCs have single-ended structures. The input impedance can be reduced

greatly since transistors M5 and M1 provide negative feedback. Moreover, the input current can be amplified by the current mirror M1/M3 and PMOS latch. The regeneration characteristics of the PMOS latch improve the speed performance.

Because the input impedance of current comparator is the loading of current mirror and DAC circuits, the low-input-impedance of current comparator circuit can reduce the RC time delay. In Fig. 3.10(a), the input impedance can be derived by the small signal model.

$$Z_{in}(s) = \frac{\frac{1}{r_{ds5}} + \frac{1}{r_{ds7}} + sC_{g13}}{g_{m1}g_{m5} + sC_{g13}\left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds5}} + g_{m5}\right)} \quad (3.15)$$

where  $C_{g13}$  is the total capacitance including parasitic capacitance from node C to ground in Fig. 3.10(a). To obtain a low input resistance at low frequency, large  $g_{m1}$ ,  $g_{m5}$ ,  $r_{ds5}$ , and  $r_{ds7}$  are required. From the HSPICE simulation results, the input resistance of the current comparator is about 150  $\Omega$  at low frequency.

Generally, the time response of current comparator is related to  $Z_{in}$ , the time response of the preamplifier circuits M1-M8 in Fig. 3.10(a), and the time response of the PMOS latch. The step response of the preamplifier can be derived as,

$$h(t) \equiv \frac{I_o}{I_{in}}(t) = \left( \frac{g_{m3}}{g_{m1}} - \frac{g_{m3}}{g_{m1}} e^{\frac{-t}{C_{g13}/g_{m1}}} \right) u(t) \quad (3.16)$$

From Eq. (3.16), the time response of the preamplifier can be improved by reducing the capacitance  $C_{g13}$ . The time response of the PMOS latch can be characterize by the output voltage change versus time with the major factor as  $e^{(gm11/C_{out})}$ . Thus reducing the output capacitance  $C_{out}$  and increasing  $g_{m11}$  can improve the speed performance. According to the HSPICE simulation results, the current comparator takes 1.5 nsec to amplify an input current of 2 nA as shown in Fig. 3.10(b).

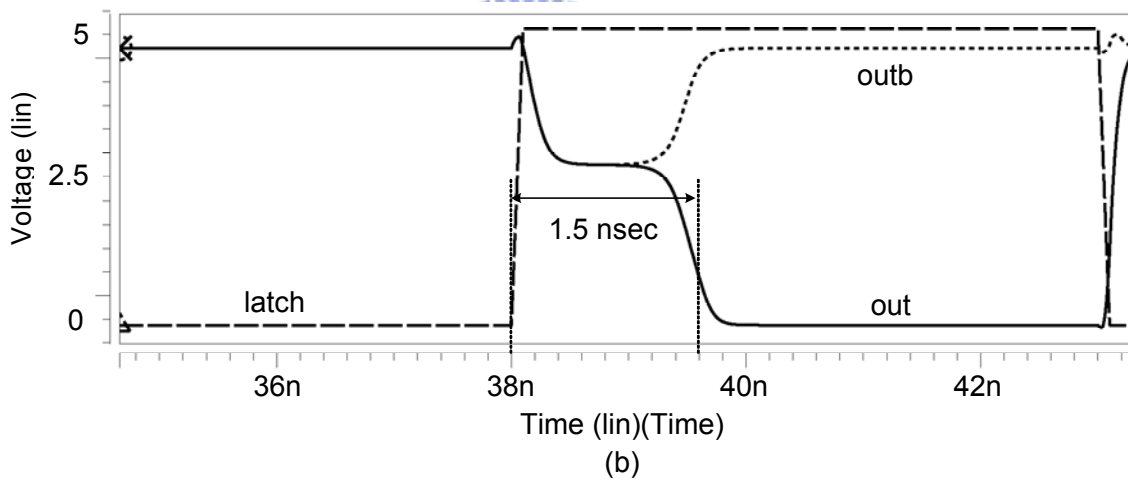
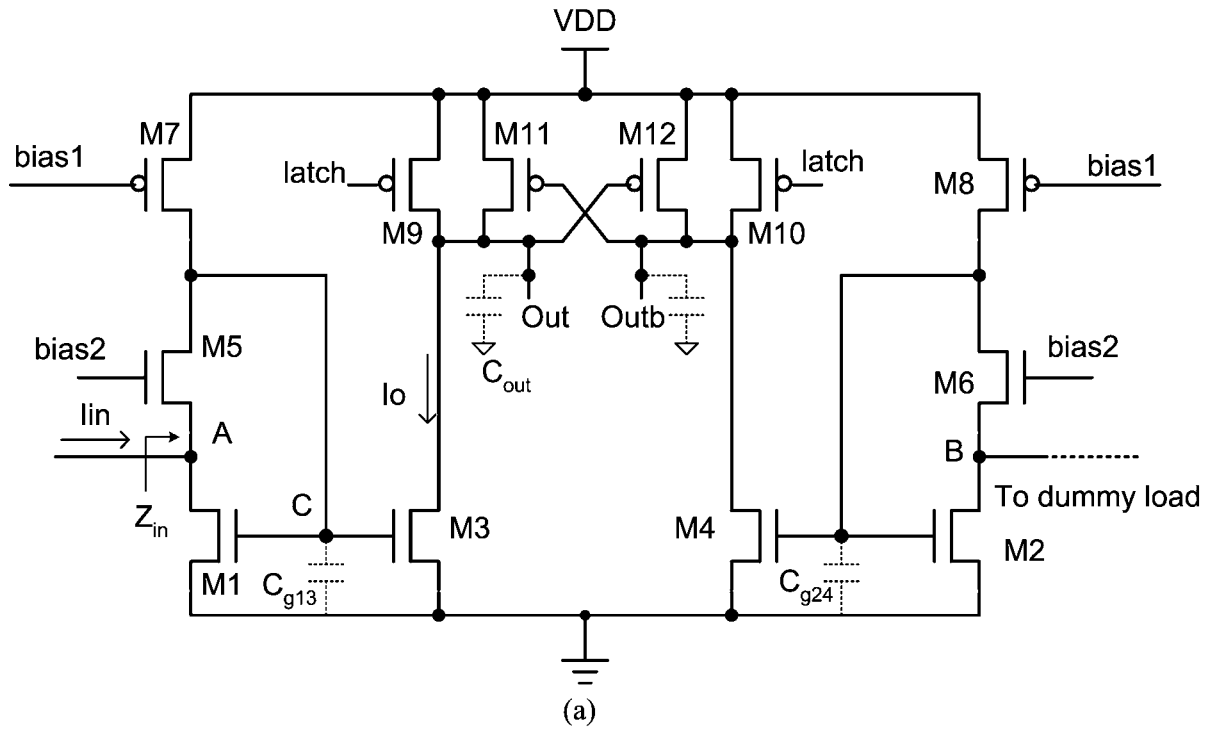


Figure 3. 10 (a) The circuit structure of the low-input-impedance current comparator. (b) The transition characteristic of the current comparator.

### 3.4 Experimental Results and Discussions

#### 3.4.1 Experimental Results

To demonstrate the feasibility and verify the function, the experimental chip of a full

wave-pipelined IADC (FWP-IADC) was designed and fabricated in a double-poly quadruple-metal 0.35 $\mu\text{m}$  CMOS process. Figure 3.11 shows the photograph of the fabricated experimental chip. For testing, the voltage SHC was not included in the whole chip, so the performance limits of the developed architecture could be recognized. Therefore, the arbitrary-waveform-generator must be used to generate the 12-bit S/H voltage signal. Because the available instruments for the input signal sources are mostly in the voltage domain, the V/I conversion interface is required to test the chip. In this test chip an on-chip linear V/I circuit [48] is employed to alleviate this limitation. The circuit diagram of the V/I conversion interface is shown in Fig. 3.12. The circuit consists of an on-chip poly resistors  $R_x$  and a current conveyor [45] to convey the current flowing through  $R_x$  to the output. The whole chip was laid out to contain eight wave-pipelined stages. For simplicity, this demonstrative design included neither digital error correction nor calibration circuits. In the experimental chip of the FWP-IADC, the simple current comparator [109] is used, as shown in Fig. 3.9(b). According to Eqs. (3.7) and (3.10), the  $T_{\text{int}_7}$  and  $T_{\text{ccmp}_8}$  are 33 and 10 nsec, respectively. Thus the conversion rate of the experimental chip can operate up to about 20 MHz.

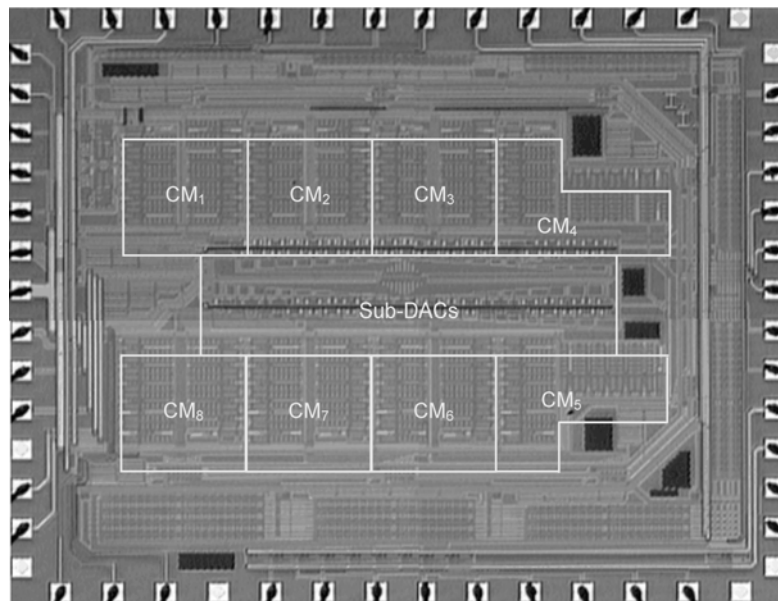


Figure 3. 11 The photograph of the fabricated chip.

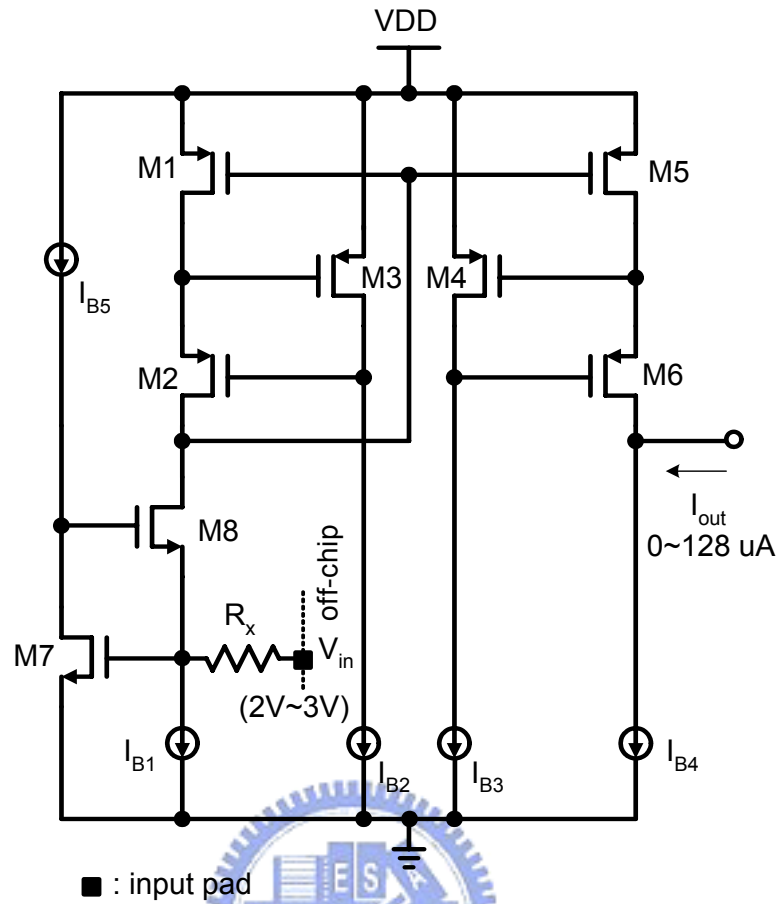
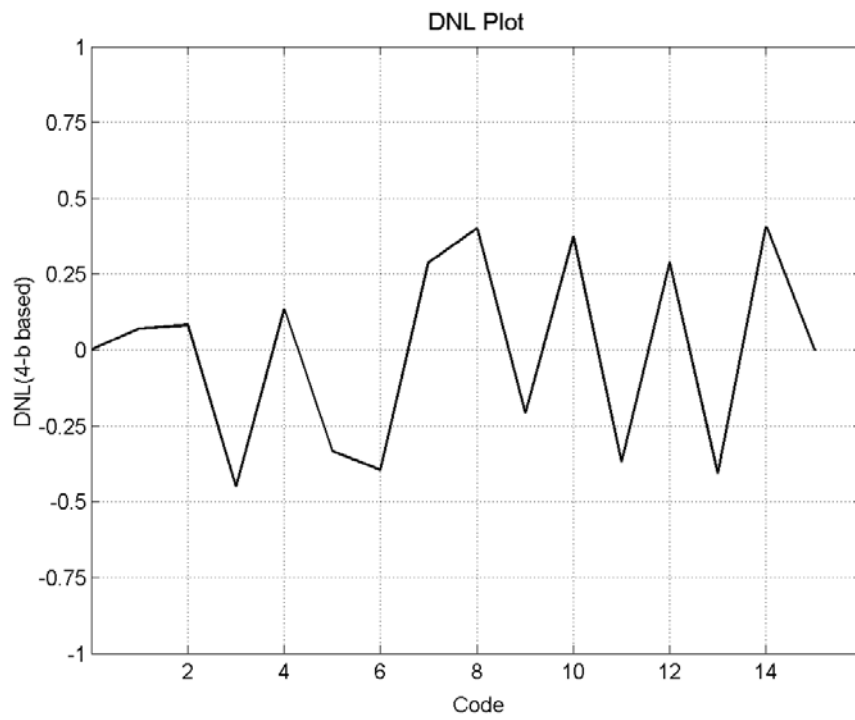
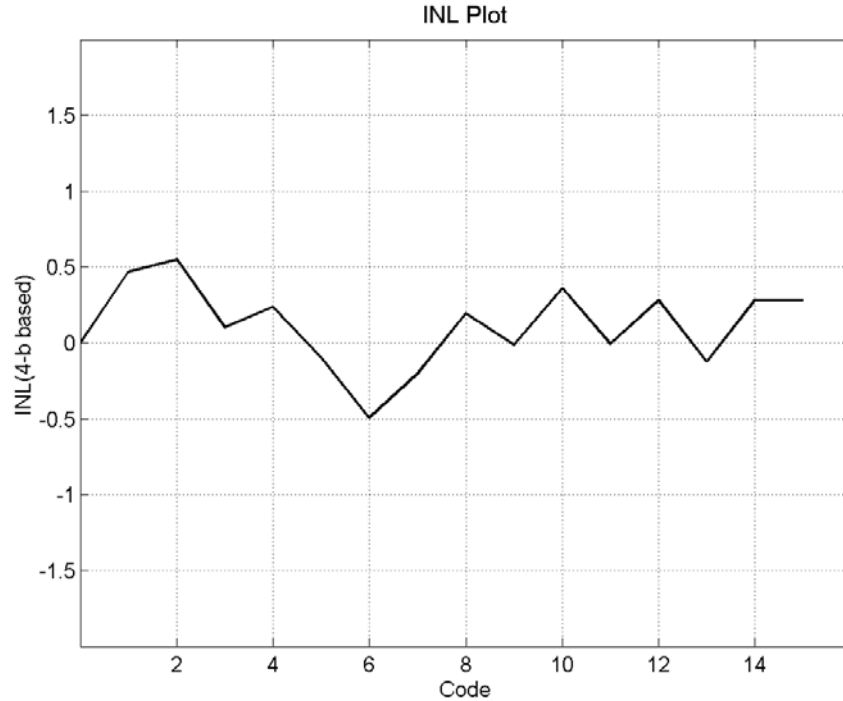


Figure 3. 12 The V-I interface circuit to convert the external voltage signals into internal current signals.



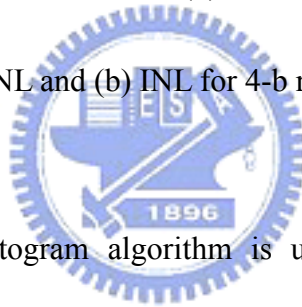
(a)





(b)

Figure 3. 13 Measured (a) DNL and (b) INL for 4-b resolution at 20MS/s conversion rate.



The sine-wave-based histogram algorithm is used to measure the linearity of the converter. Figures 3.13 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL), based on 4-b resolution when the fabricated WP-IADC is operated at 20Ms/s conversion rate. The DNL and the INL for all codes are within +/- 0.45 LSB and +/- 0.55 LSB, respectively. The comparator offset seriously degrades the resolution of the proposed FWP-IADC. This phenomenon will be discussed in detail in a later paragraph.

Figure 3.14 shows the measured fast Fourier transform (FFT) spectrum of a 1.03 MHz sinusoidal input with the fabricated IADC operated at a 20 Ms/s conversion rate. The total harmonic distortion (THD) is -28.5 dB. Clearly, the magnitude of the even harmonics distortion cannot be eliminated because of the single-end structure. The signal-to-noise-and-distortion ratio (SNDR) was measured by taking the FFT on 8192 samples from the output codes of the FWP-IADC. Figure 3.15(a) plots the measured SNDR

versus the conversion rate for the signal input frequency of 1 MHz. It can be seen that the measured SNDR remains at approximately 27 dB (effective 4.2b) when the conversion frequency is below 20 MS/s. Furthermore, the measured SNDR is decreased to 23.7 dB when the conversion frequency is increased to 40 MS/s. Figure 3.15(b) plots the measured SNDR versus the analog input frequency for a full-scale sinusoidal input at 20 MS/s. The SNDR is seen to exceed 25.4 dB when the input frequency is between 1 M and 10 MHz. The measured results verify the advantages of high input frequency and Nyquist-rate operation in the proposed architecture of FWP-IADCs.

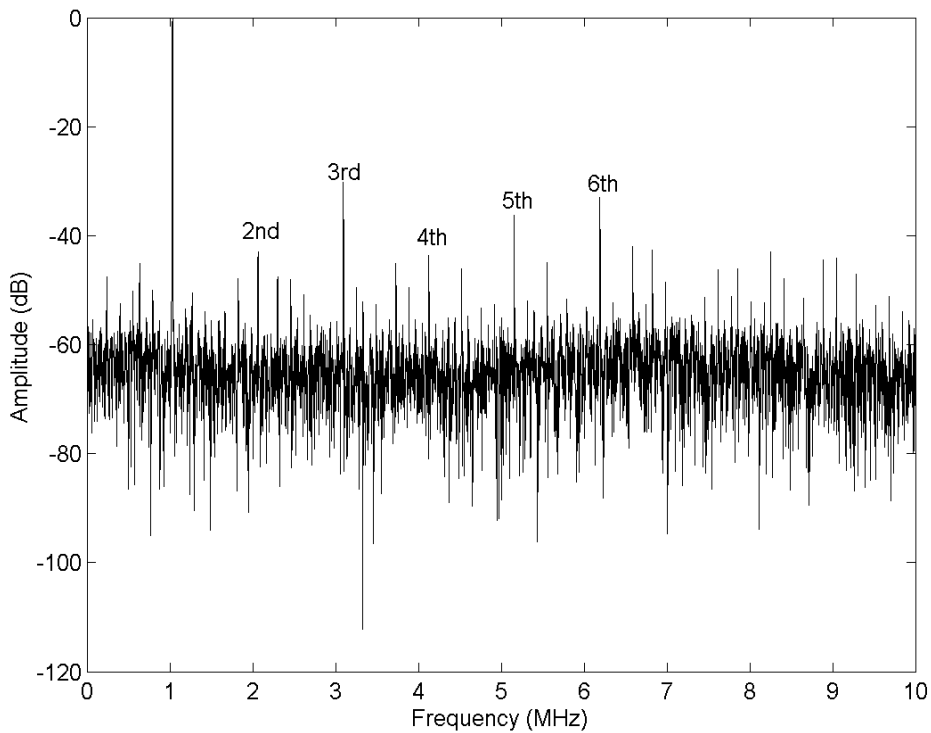


Figure 3. 14 Measured FFT spectrum of the wave-pipelined IADC for a 1.03MHz sine wave sampled at 20 Ms/s conversion rate.

Table 3.1 summarizes the post-simulation results and measured characteristics of the example FWP-IADC. The area of the chip (including the I/O pads) is  $3.7 \times 2.9 \text{ mm}^2$  and the power consumption is 390mW, with a 5V single power supply.

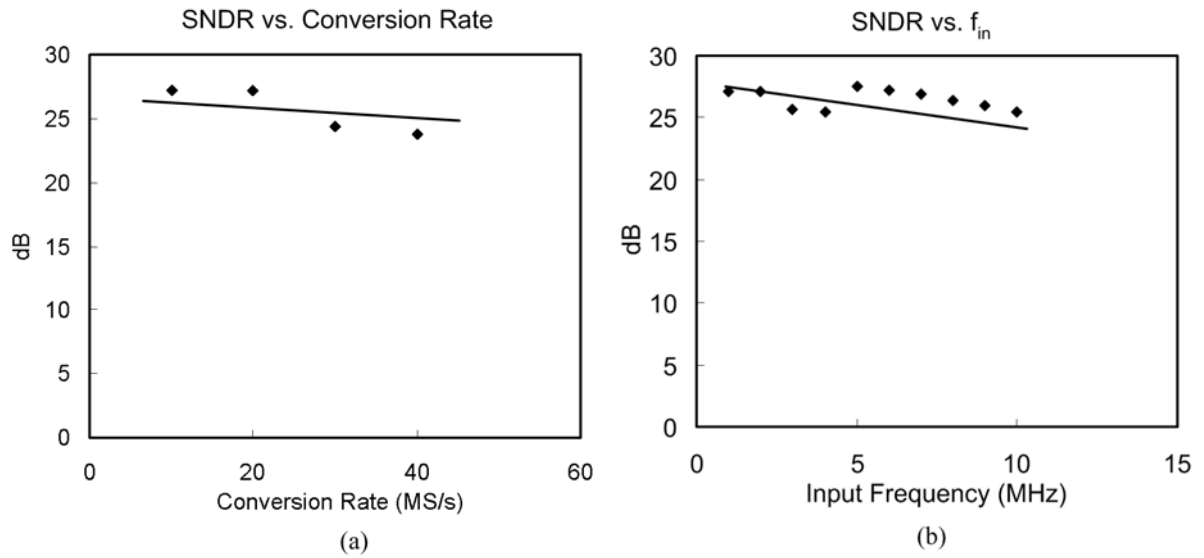


Figure 3.15 (a) The measured SNDR versus conversion rate of the wave-pipelined IADC for 1MHz analog input and (b) the measured SNDR versus analog input frequency of the wave-pipelined IADC at 20 MS/s conversion rate.

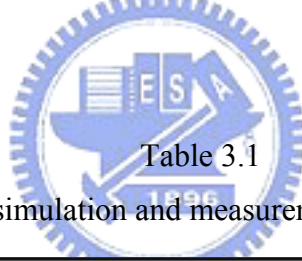


Table 3.1

The summarized post-simulation and measurement results of the FWP-IADC

	Post-simulation	Measurement
Technology	0.35 $\mu\text{m}$ 2P4M CMOS (Thick oxide is selected) (Minimum channel length is 0.5 $\mu\text{m}$ )	
SNDR ( $f_s = 20 \text{ MS/s}$ )	45.9 dB (ENOB=7.3-b, $f_{in} = 1 \text{ MHz}$ ) 35.2 dB (ENOB=5.5-b, $f_{in} = 10 \text{ MHz}$ )	27 dB (ENOB=4.2-b, $f_{in} = 1 \text{ MHz}$ ) 25.4 dB (ENOB=3.9-b, $f_{in} = 10 \text{ MHz}$ )
DNL	-1/+1 LSB	< +/-0.45 LSB (4-b, $f_s = 20 \text{ MHz}$ )
INL	-1/+1 LSB	< +/-0.55 LSB (4-b, $f_s = 20 \text{ MHz}$ )
Full Scale Current	0 ~ 128 $\mu\text{A}$	0 ~ 128 $\mu\text{A}$
Unit LSB Current	0.5 $\mu\text{A}$	0.5 $\mu\text{A}$
Power Dissipation	405 mW	390 mW
Power Supply	5 V	5 V
Chip Area	3.7 x 2.9 $\text{mm}^2$	3.7 x 2.9 $\text{mm}^2$

### 3.4.2 Discussion

#### A. Comparator offset

The input offset current of the current comparator severely impacts the linearity of the FWP-IADC since no digital error correction and calibration circuits are used in this work. As shown in Fig. 3.9(b), any mismatch between the PMOS transistors M1 and M5 (or NMOS transistors M2 and M6) causes the transfer curve of inverter to deviate from the ideal curve. Figure 3.16 explains this phenomenon. The transfer curve shifts to the right or left with the offset voltage,  $\Delta V$ , since the resistance ( $R_{on\_M5}$ ) of M5 does not equal that ( $R_{on\_M6}$ ) of the NMOS M6 when the input voltage of the inverter chain is half of VDD. This offset voltage can be considered to be the input referred offset current by the gain of the Rm Amplifier (M1~M4) in Fig. 3.9(b). The gain ( $A_v$ ) of the Rm amplifier can be determined from the transconductance of the transistors M1 and M2.

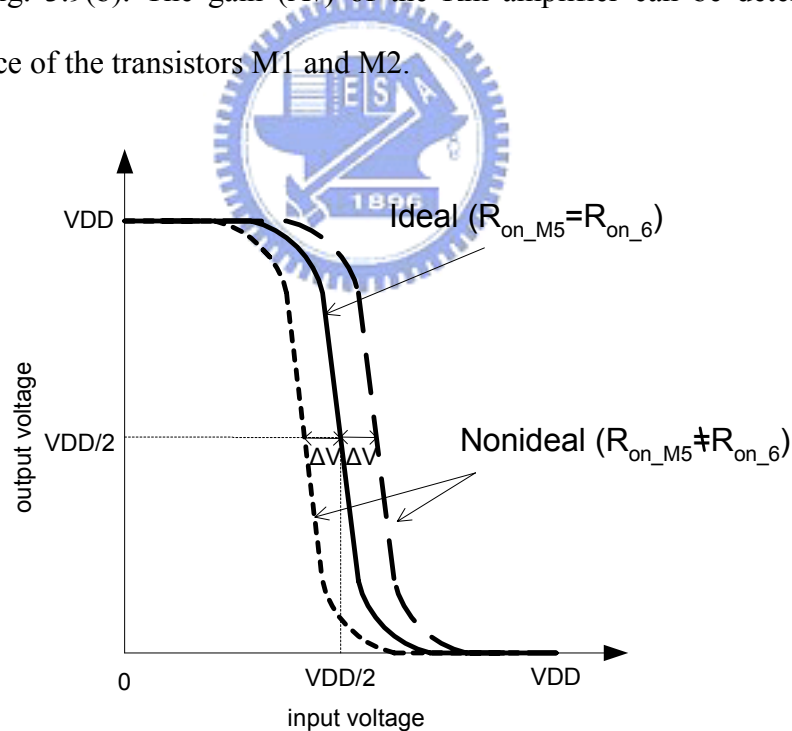


Figure 3. 16 Transfer curves of the inverter.

$$A_v \cong \frac{1}{g_{m1}} // \frac{1}{g_{m2}} \quad (3.17)$$

In order to get the better transition performance, the higher gm of transistors M1 and M2 is designed to decrease the input resistance of the current comparator. However, this strategy reduces the gain of the Rm amplifier. Therefore, the input referred offset current of the current comparator is increased to affect the linearity of the FWP-IADC.

### B. Substrate noise

In the fabricated chip, the substrate of the digital circuits directly connects to the source terminal of NMOS transistors. Therefore the ground bounce phenomenon contributes noise to the substrate. It is very serious effect especially in the output buffer. The wrong connection can be found in the layout of the output buffer, as shown in Fig. 3.17.

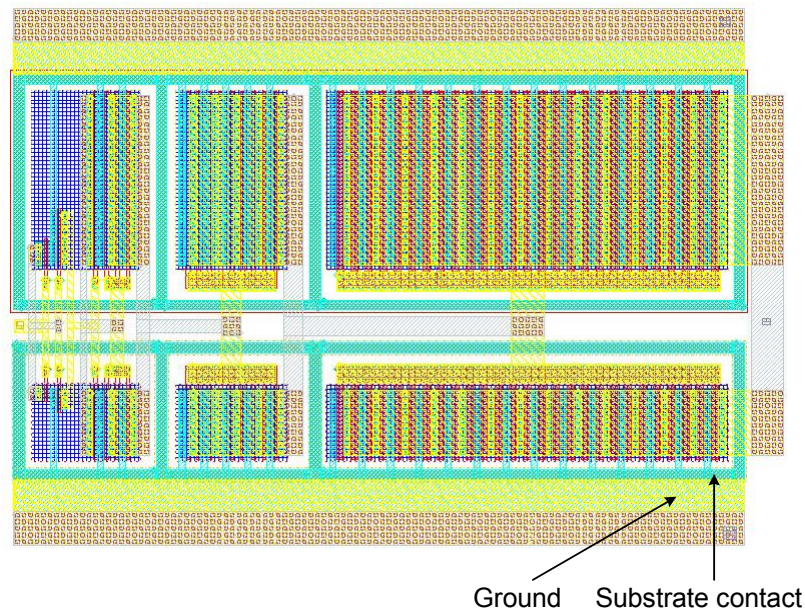


Figure 3. 17 The incorrect layout of output buffer for the fabricated ADC.

## 3.5 Post-Simulation Results of the Modified FWP-IADC

In the modified version of the proposed FWP-IADC, the substrate and the source terminal of transistors in the digital circuits are separated. Moreover, the low-input-impedance current comparators that is shown in Fig. 3.10 are used instead of the continuous-time current

comparators in the modified version. In order to suppress the input offset current that is caused by the size mismatch of MOS transistors, the techniques of layout must follow common centric symmetric rules. Figures 3.18 and 3.19 are the layout of the modified output buffer and the low-input-impedance current comparator, respectively. The layout of whole chip is shown in Fig. 3.20. All simulation results are based on 0.35  $\mu\text{m}$  2P4M CMOS technology with 5V power supply. The option of thick oxide is selected, thus the minimum channel length is 0.5  $\mu\text{m}$ . Meanwhile, the parasitical capacitances are extracted to perform the post-simulation.

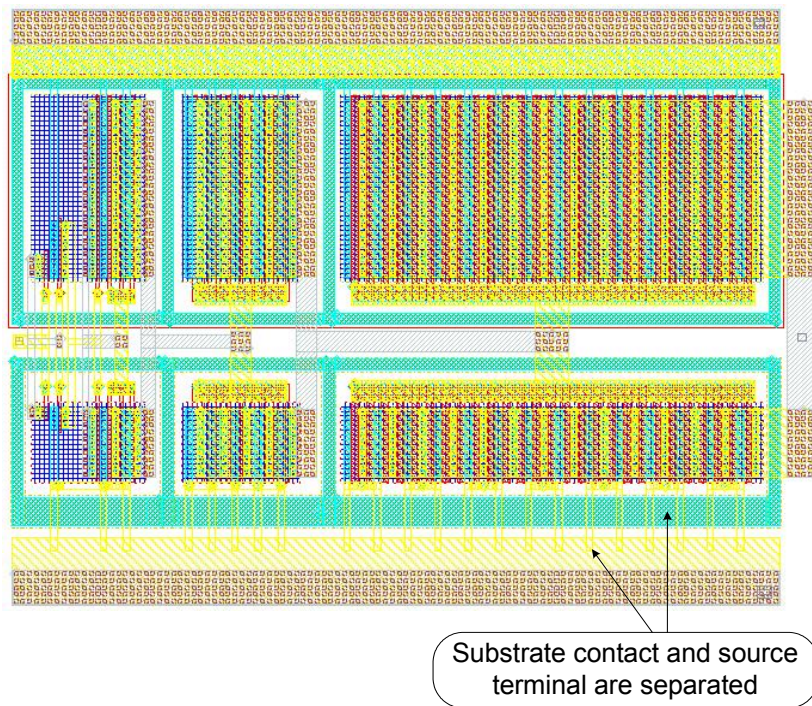


Figure 3. 18 The modified layout of output buffer for the revised FWR-IADC.

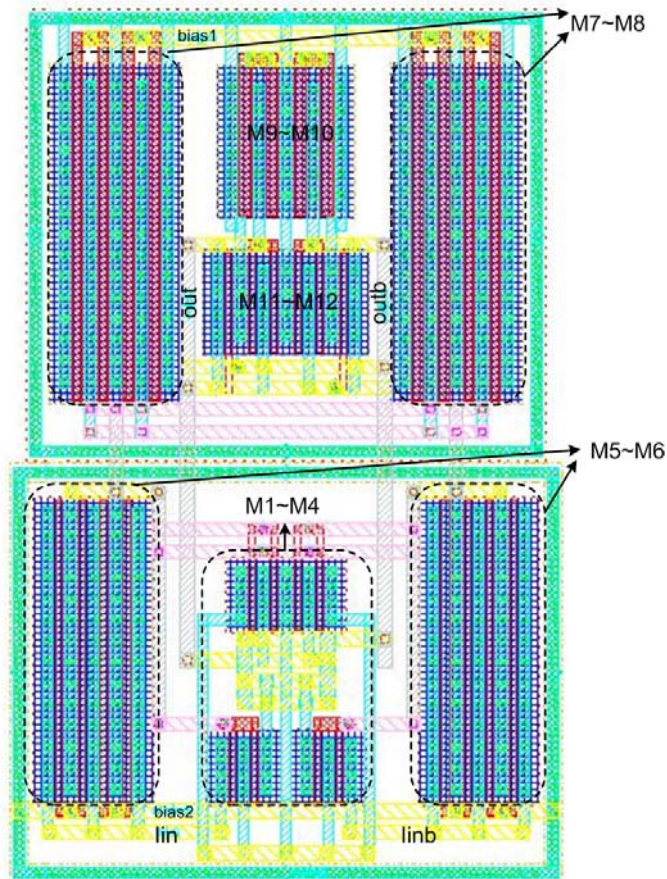


Figure 3. 19 The layout of the low-input-impedance current comparator.

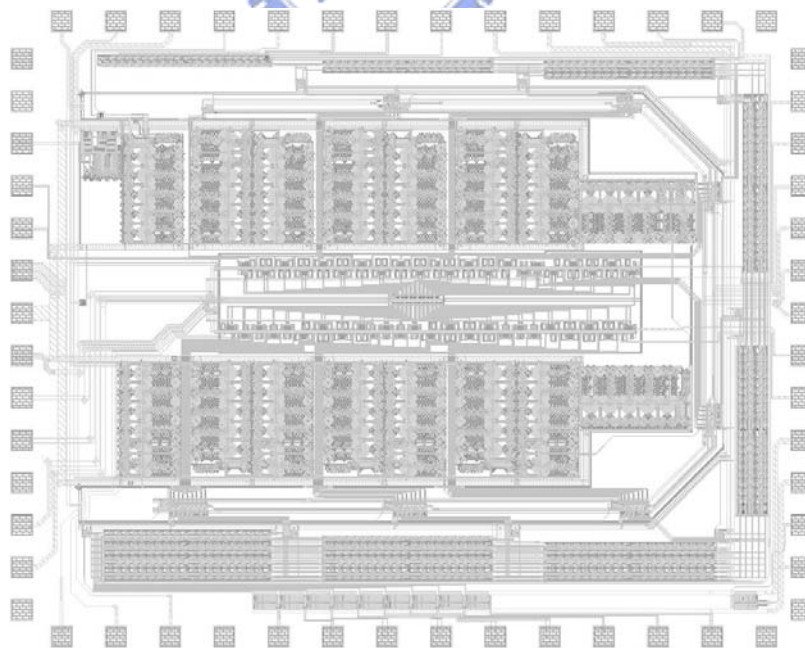


Figure 3. 20 The layout of whole chip for the modified version.

Since intrinsic delay ( $T_{int\_7}$ ) of the final current mirror in a CM stage with eight current

mirrors is about 16.5 nsec and the input signal hold time ( $T_{h_{\text{comp}_8}}$ ) of the current comparator is about 1.5 nsec, the upper limit of sampling rate can be given from the Eqs. (3.9) and (3.10). Therefore, the modified FWP-IADC can achieve 8-bit accuracy with a conversion rate up to 55 MSample/s under Nyquis rate sampling. The DNL and INL of the post-simulation results at 55 MS/s are shown in Fig. 3.21. The DNL is within +0.2 and  $-0.2$  LSB whereas the INL is within +0.1 and  $-0.1$  LSB. Since the modified FWP-IADC also adopts the single-end structure, the distribution plots of the DNL/INL are not symmetrical.

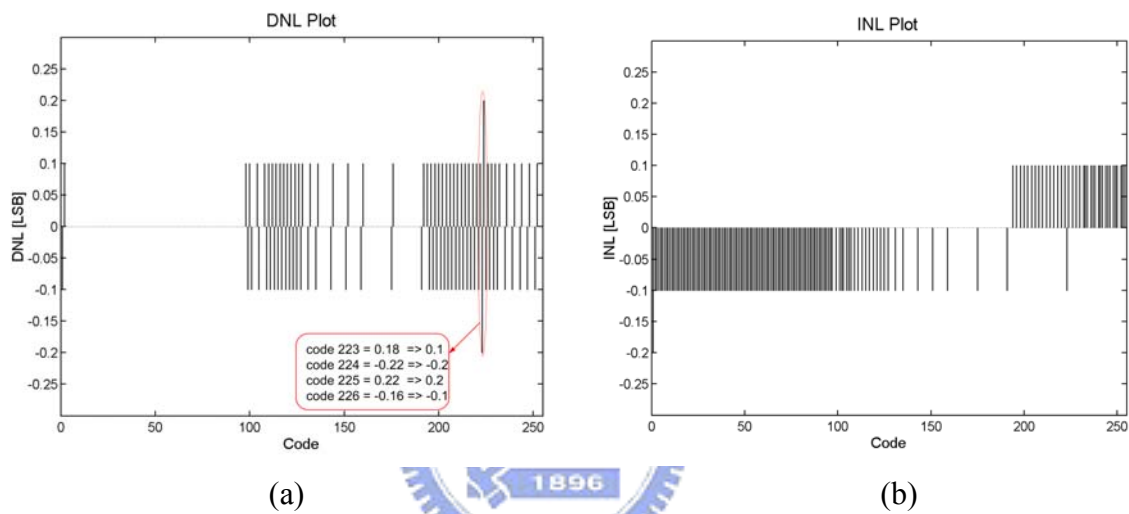


Figure 3. 21 The results of post-simulation (a) DNL and (b) INL at 55 MS/s sampling rate.

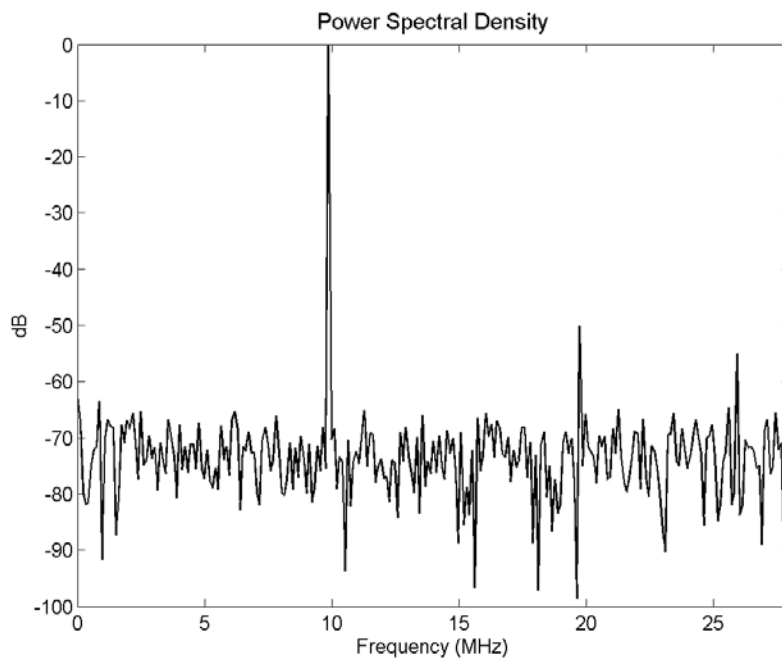


Figure 3. 22 The FFT spectrum for a 10 MHz sine-wave input signal at 55 MSample/s.



Figure 3.22 shows the fast Fourier transform (FFT) spectrum at 55 MSample/s under 10 MHz input frequency. In order to verify the characteristic of the modified FWP-IADC, the front-end V-I conversion interface is removed and the current input signal that is step sinusoidal waveform is directly applied to the proposed FWP-IADC. It can be seen from Fig. 3.22 that all the harmonic distortion components are below  $-50$  dB. The SNDR is 45 dB. The SNDR versus input frequency characteristics at 55 MHz sampling rate are shown in Fig. 3.23. The SNDR at low frequency is 48.6 dB and it starts to decrease when the input frequency is increased. At about 27 MHz (half of Nyquist sampling frequency) it becomes 35.6 dB. Figure 3.24 shows the FFT spectrum at 90 MS/s under 1 MHz input frequency. Moreover, the SNDR versus input frequency characteristics at 90 MS/s sampling rate are shown in Fig. 3.25. The SNDR at input frequency of 1 MHz is about 45.7 dB and it starts to decrease at 3 MHz. Since the input current is non-full-scale at low input frequency under 90 MS/s, the intrinsic delay of the last current mirror is reduced. Therefore, the sampling rate can increase from 55 MS/s to 90 MS/s. The major characteristics of post-simulation result are list in Table 3.2. The timing difference between two versions for FWP-IADC is listed in Table 3.3.

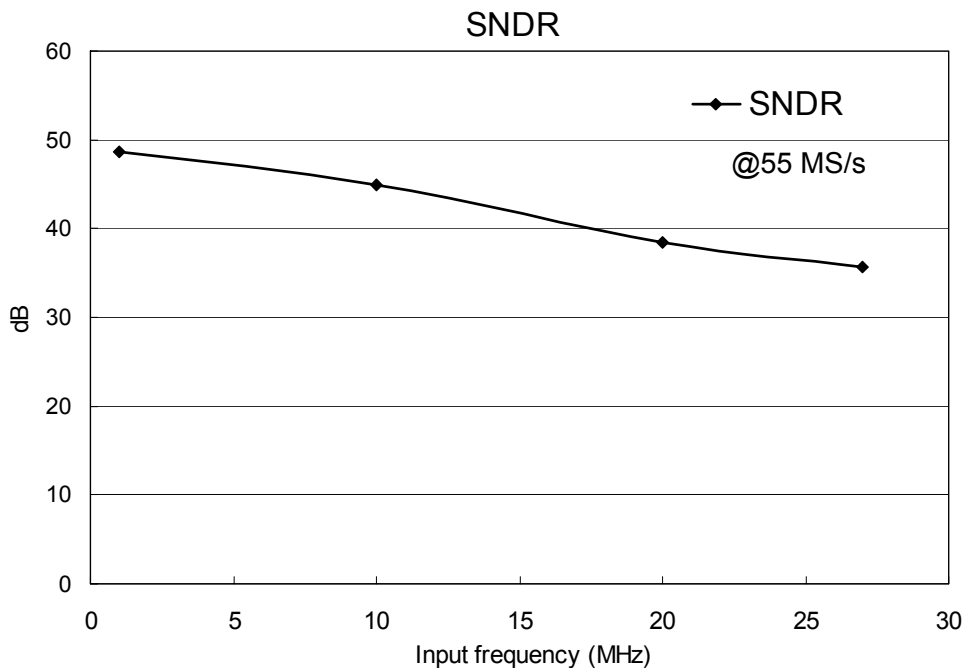


Figure 3. 23 The SNDR versus input frequency characteristics.

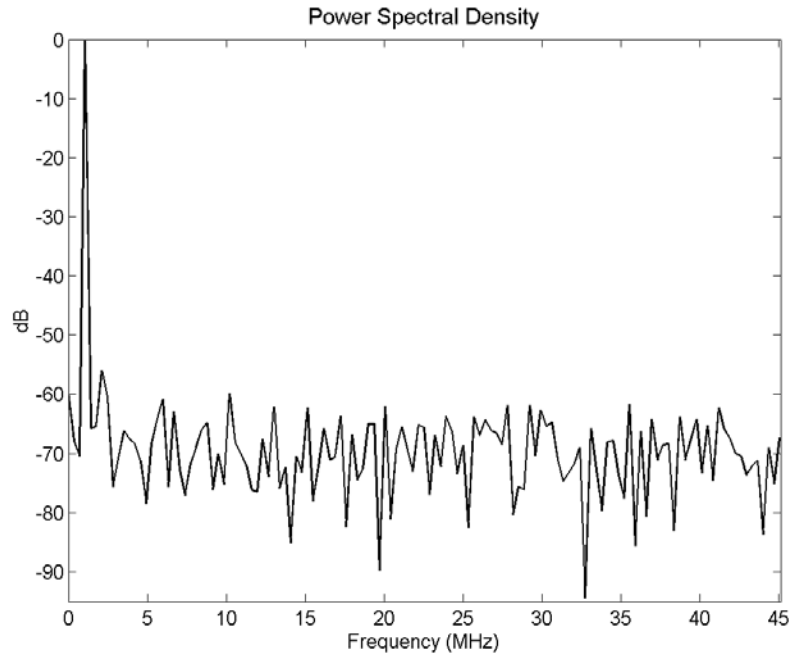


Figure 3. 24 The FFT spectrum for a 1 MHz sine-wave input signal at 90 MSample/s.

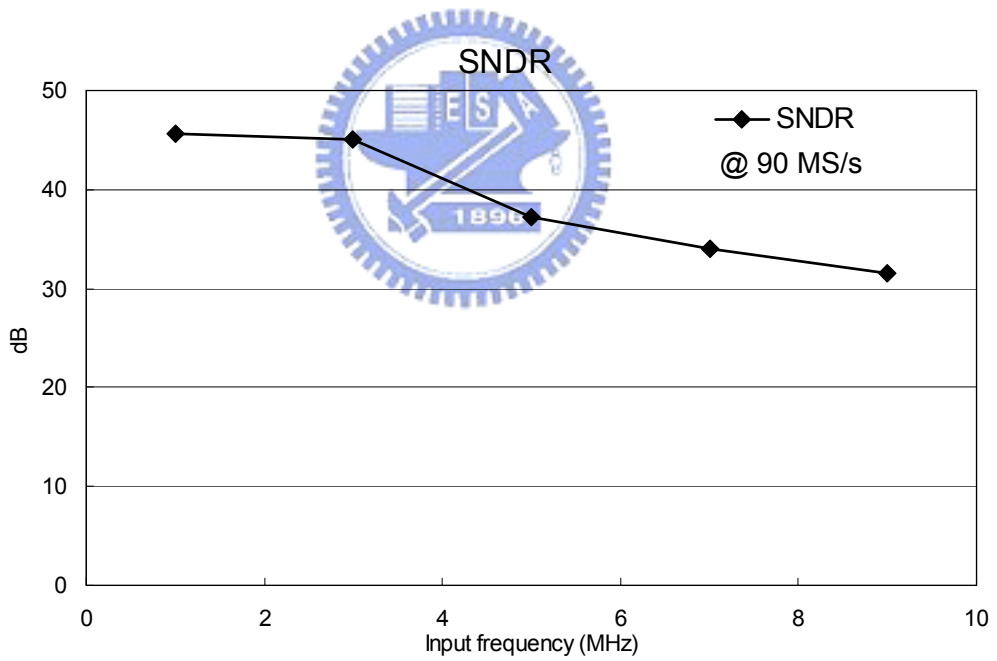


Figure 3. 25 The SNDR versus input frequency characteristics at 90 MSample/s.

Table 3. 2

Major characteristics of post-simulation results for the modified FWP-IADC

Technology	0.35 $\mu\text{m}$ 2P4M CMOS
SNDR ( $f_s = 55$ MS/s)	48.6 dB (ENOB=7.8-b, $f_{in} = 1$ MHz) 35.7 dB (ENOB=5.6-b, $f_{in} = 27$ MHz)
SNDR ( $f_s = 90$ MS/s)	45.1 dB (ENOB=7.2-b, $f_{in} = 3$ MHz)
DNL	+0.2/-0.2 LSB ( $f_s = 55$ MHz)
INL	+0.1/-0.2 LSB ( $f_s = 55$ MHz)
Full Scale Current	0 ~ 128 $\mu\text{A}$
Unit LSB Current	0.5 $\mu\text{A}$
Power Dissipation	450 mW
Power Supply	5 V
Chip Area	3.4 x 2.8 $\text{mm}^2$

Table 3.3

Timing difference between two versions for FWP-IADC

	Continuous-Time Current Comparator	Low-Input-Impedance Current Comparator
$\max\{T_{int\_7}\}$	33 nsec	16.5 nsec
$T_{h\_ccmp\_8}$	10 nsec	1.5 nsec
$\max\{T_{process\_7}\}$	43 nsec	18 nsec
$\max\{T_{DAC}\}$	10 nsec	4.5 nsec
$T_{d\_bf}$	20 nsec	6 nsec
$T_{clk}$	44 nsec	18 nsec

### 3.6 Summary

In this chapter, a new architecture of the FWP-IADC is proposed and analyzed for the design of IADC. The novelty lies in the application of wave-pipelined theory to form the FWP-IADCs and improve the speed performance of the IADCs. FWP-IADCs offer several advantages, including high-speed performance, high input frequency, more efficiency use of

timing, and increased linearity by removing the inter-stage switched-current cells. The operation timing of FWP-IADCs are derived and given in this work. HSPICE simulation results reveal that FWP-IADC can achieve sampling rates of 55 MS/s under Nyquist rate sampling with 8-bit resolution. Moreover, the FWP-IADC can achieve a sampling rate of 90 MS/s with 8-bit resolution when the frequency of the input signal is 3 MHz.

The proposed FWP-IADC was experimentally verified by a test chip fabricated using 0.35  $\mu\text{m}$  CMOS technology. The measurement results have successfully demonstrated that the proposed design concept and architectures can be applied to the design of future high-speed IADCs.

