Chapter 4

Design Techniques for Indirect Transfer Wave-Pipelined Analog-to-Digital Converters

4.1 Introduction

According to the theoretical analysis on the proposed full wave-pipelined current-mode analog-to-digital converter (FWP-IADC) structures in chapter 3, the minimum sampling clock period is proportional to the intrinsic delay of the current mirror and the increased rise/fall time in each wave-pipelined stage. In order to further improve the sampling rate of the FWP-IADC, another novel wave-pipelined architectures called indirect transfer wave-pipelined current-mode analog-to-digital converter (ITWP-IADC) is proposed and analyzed. In the ITWP-IADC, the switched-current cells are incorporated into the wave-pipelined stages to obtain better speed performance. Based upon the HSPICE simulation, the proposed four-section ITWP-IADC is shown to achieve 130 MS/s with 8-bit resolution at an input signal of 16 MHz. If the intrinsic delay of current mirror and comparison time of current comparator can be further decreased, it is expected that the sampling rate of the 8-bit four-section ITWP-IADC can reach 166 MS/s at an input frequency of 19.2 MHz. The proposed ITWP-IADC is designed in a double-poly quadruple-metal 0.35μm CMOS process with 5V power supply.

Section 4.2 describes the architectures and the design considerations of the ITWP-IADC. The switched-current circuits and other circuits are explicated in Section 4.3. Section 4.4 shows the simulation results of the whole ITWP-IADC. Finally, the summary is given in

Section 4.5.

4.2 The Architecture of the Indirect Transfer WP-IADC (ITWP-IADC)

As may be seen from Eq. (3.10), if path A of Fig. 3.3 is the critical path in the FWP-IADC, then the total processing time of the last current mirror in the final stage limits the sampling rate of the FWP-IADC. The wave-pipelined stages of FWP-IADC can be divided into several wave-pipelined sections to increase the sampling rate. The input data of each section is controlled by the delay clock. Such an architecture is called the ITWP-IADC. Figure 4.1(a) shows the structures of current-mirror wave-pipelined sections in the ITWP-IADC. Four CM stages are divided into two current-mirror wave-pipelined sections. In Fig. 4.1(a), one section consists of CM_0 and CM_1, whereas the other section consists of CM_2 and CM_3. The function block of the CM_2 stage is the same as the one of the CM_0 stage presented in Fig. 3.4. The input current of the CM_2 is not taken directly from the CM_1, but from the switched-current cells. Figure 4.1(b) shows the space-timing diagram of the ITWP-IADC in Fig. 4.1(a). As shown in Fig. 4.1(a), the first datum is sent into the first wave-pipelined section and switched-current cell 1 during the period when ϕ_1=1. The first datum is continually propagated through the wave-pipelined path for data conversion and it is also stored in switched-current cell 1. During ϕ_2, the second datum is sent into the first wave-pipelined section for processing and it is stored in switched-current cell 2. A similar operation is performed for each datum from 1 to n. When ϕ_n=1, the nth datum is sent into the first wave-pipelined section and stored in switched-current cell n. At this time, the slowest data is about to reach the final current-mirror stage and the stored first datum in switched-current cell 1 must be sent into stage CM_2 of the second wave-pipelined section to continue the wave-pipelined operation during ϕ_1', where ϕ_1' is the delay clock of ϕ_1. Therefore, the first datum is aligned at time t_{align} by switched current cell 1 and sent into the second wave-pipelined section, as shown in Figs. 4.1(a) and 4.1(b).

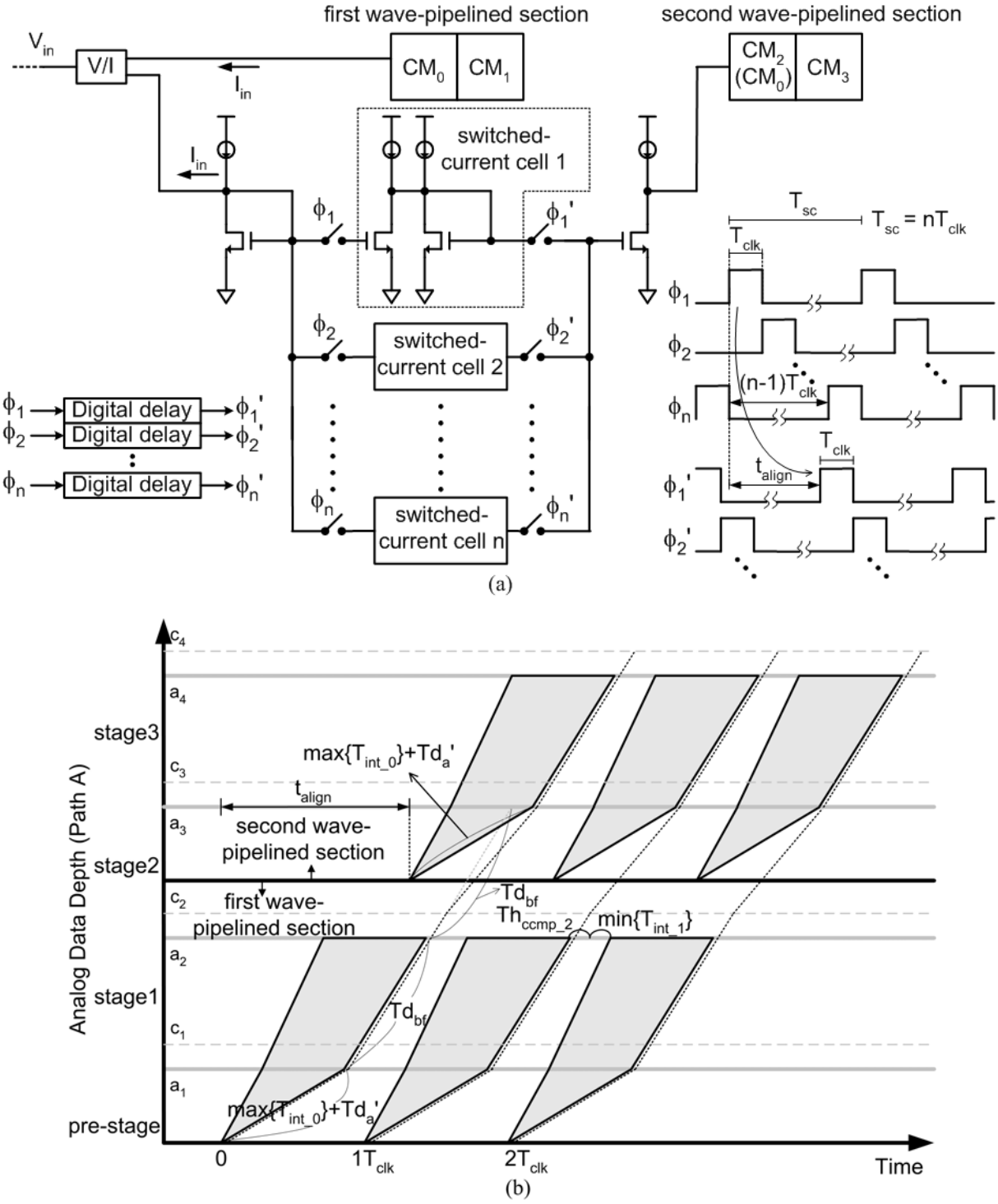


Figure 4.1 (a) The simplified block diagram of the two-section ITWP-IADC for 4 CM stages. (b) The space-timing diagram of the two-section ITWP-IADC for 4 CM stages.

In the case of the maximum sampling rate, the ITWP-IADC needs enough switched-current cells to store the input data. Thus, the following constraint must be satisfied,

as shown in Fig. 4.1(a).

$$nT_{clk} \geq t_{align} + T_{clk} \tag{4.1}$$

where T_{clk} is the minimum clock period. Meanwhile, t_{align} must satisfy the following constraint to guarantee the successful operation, as shown in Fig. 4.1(b).

$$\max\{T_{int\_0}\} + Td_a' + 2Td_{bf} \leq t_{align} + \max\{T_{int\_0}\} + Td_a'$$

Thus,

$$t_{align} \geq 2Td_{bf} \tag{4.2}$$

According to Eqs. (4.1) and (4.2), the range of aligned time t_{align} and the number n of the switched-current cells can be obtained as,

$$(n-1)T_{clk} \geq t_{align} \geq 2Td_{bf}$$

$$n \geq \frac{2Td_{bf}}{T_{clk}} + 1 \qquad \text{n is integer} \tag{4.3}$$

where T_{clk} represents the minimum clock period. After the number n of switched-current cells and t_{align} are determined, the required delay elements with a delay of t_{align}-$2Td_{bf}$ can be inserted in path C to control the sub-DAC_2.

Accordingly, the longest data path A reduces to two CM stages in the 4-bit example. T_{clk} is decreased from $T_{process\_3}$ to $T_{process\_1}$ in a two-section ITWP-IADC. Therefore, speed can be increased using the two-section ITWP-IADC in four CM stages.

Applying the same principle, the four CM stages in a two-section ITWP-IADC can be extended to eight CM stages, as shown in Fig. 4.2. Each section includes four CM stages. The current input to the CM_4 stage does not directly come from the previous CM_3 stage, but from the switched-current cells. Meanwhile, the function block of CM_4 is the same as the one of

CM_0 shown in Fig. 3.4. Thus, the sampling clock T_{clk} can be reduced to $T_{process\_3}$ in the two-section ITWP-IADC for the 8-bit example; $T_{process\_3}$ is smaller than $T_{process\_7}$ in FWP-IADC. Furthermore, the wave-pipelined stage can be further divided into four sections as shown in Fig. 4.3. Each section has two CM stages, just like the section in Fig. 4.1(a). Thus, the sampling clock T_{clk} can further reduce to $T_{process\_1}$ in the four-section ITWP-IADC; $T_{process\_1}$ is smaller than $T_{process\_3}$ in the two-section ITWP-IADC for the 8-bit example.

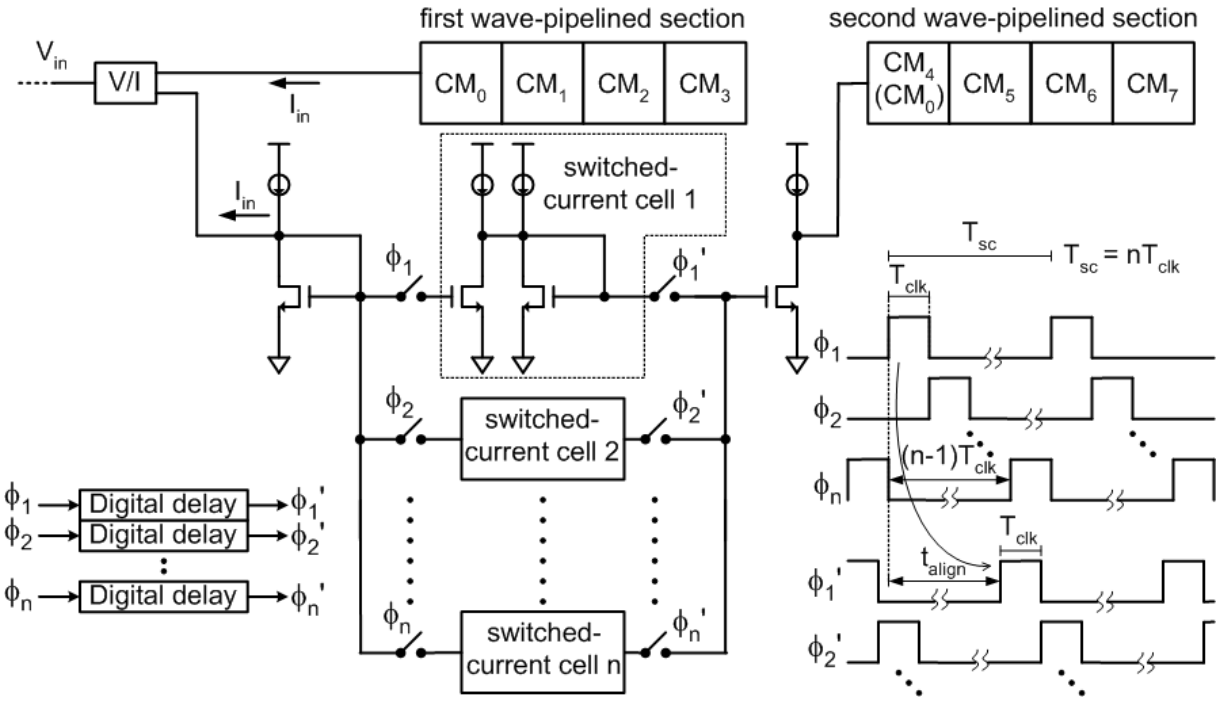


Figure 4.2 The simplified block diagram of the two-section ITWP-IADC for 8 CM stages.

According to the timing diagram of ITWP-IADC in Figs. 4.1(a), 4.2, and 4.3, the period T_{sc} of the switched-current cell equals nT_{clk}. Thus, the switched-current cells have enough time to satisfy the demand for accuracy and speed. Moreover, only a few switched-current cells are present in the overall data path of ITWP-IADC to degrade the linearity. Consequently, the linearity is expected to be better than that in the conventional pipelined IADC. Besides, the error generated by the current mirror does not accumulate through the total CM stages in ITWP-IADC. Therefore, less accuracy can be required of the current mirror in ITWP-IADC

than of that in FWP-IADC.

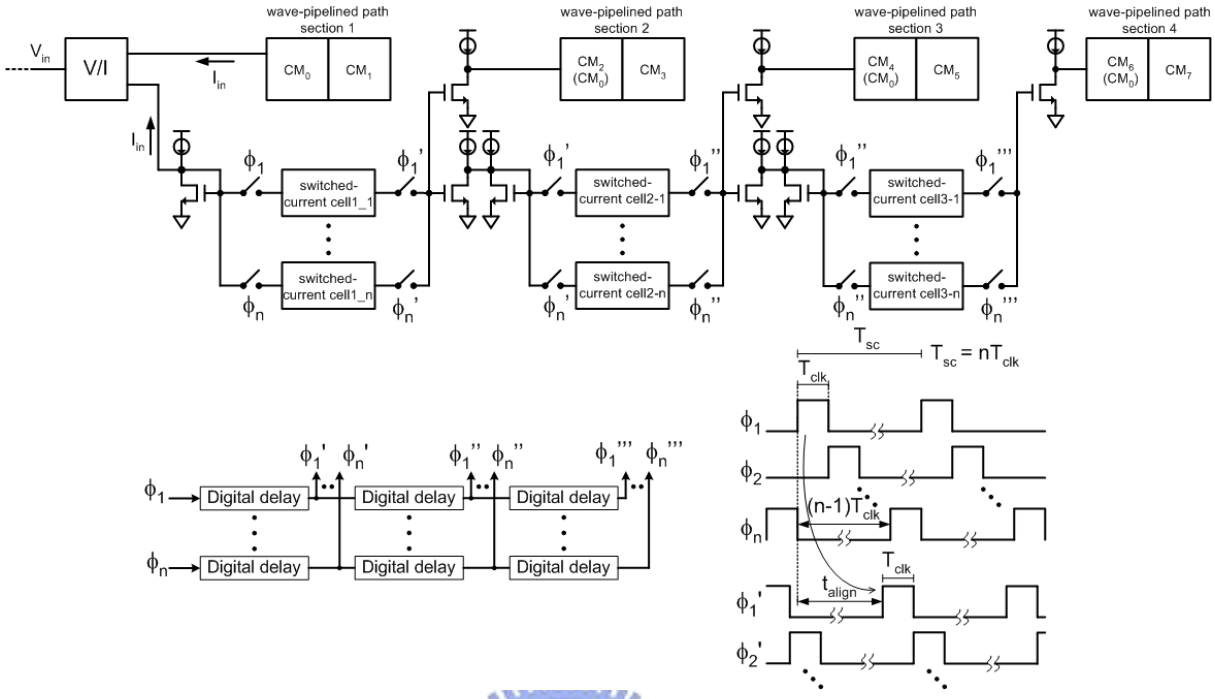


Figure 4.3 The simplified block diagram of the four-section ITWP-IADC for 8 CM stages.

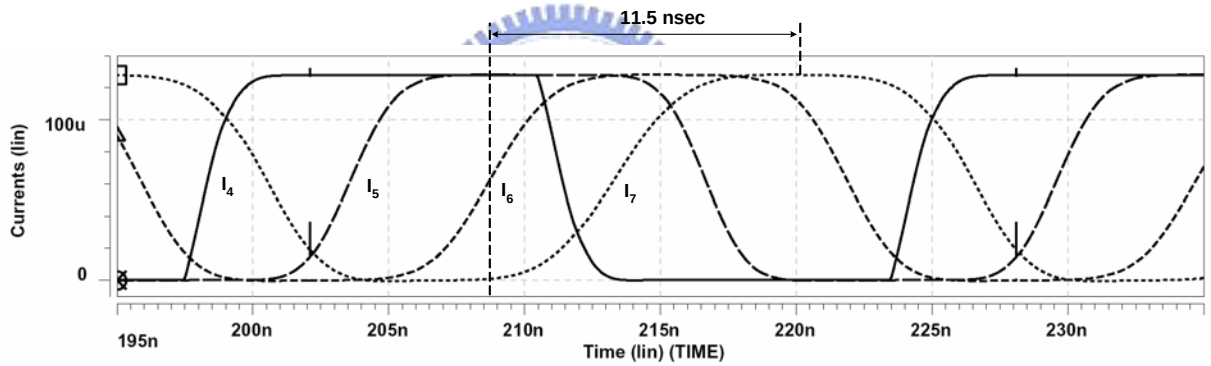
4.3 Circuit Design

4.3.1 Basic Building Block Circuits

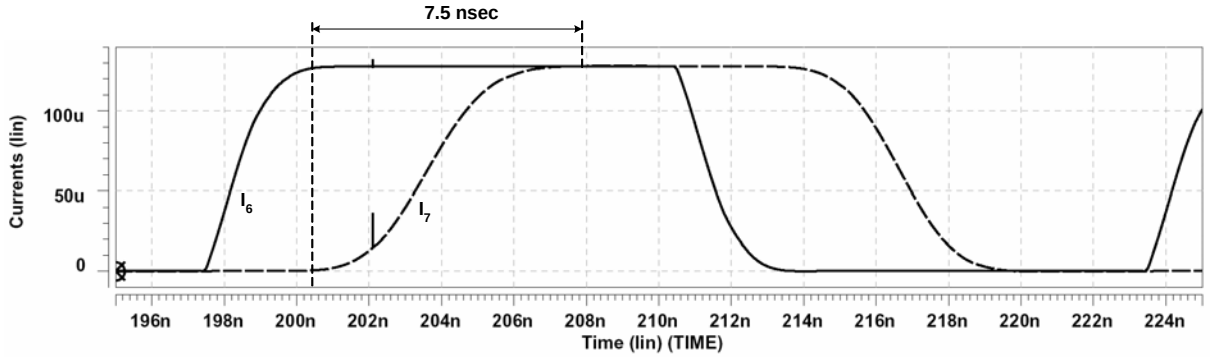
The basic building blocks, such as current mirror, sub-DACs, and low-input-impedance current comparator, are same as the FWP-IADC that is explicated in chapter 3.

According to the analyses and discussions of the Section 4.2, the sampling clock is limited by the total processing time of the last current mirror in the final stage, $T_{process\_3}$ and $T_{process\_1}$, in two-section and four-section 8-bit ITWP-IADC, respectively. Moreover, the total processing time of the last current mirror is determined by the intrinsic delay of the current mirror and input signal hold time of the current comparator, as derived from Eq. (3.7). Therefore, the rise/fall time and settling time of the current mirror are very important. Figures 4.4(a) and 4.4(b) show the waveforms of current mirror in the final section of 2-section and

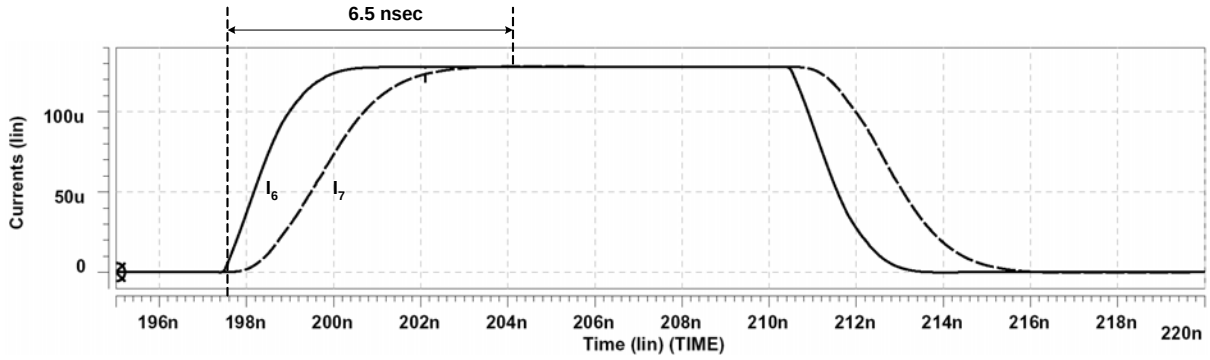
4-section, respectively. In this design, each CM stage consists of 10 current mirrors. Since the current signal only propagates through 4 (2) CM stages in 2 (4) sections ITWP-IADC, the accuracy demand of ITWP-IADC can be relaxed as compared with that in FWP-IADC. After the current mirror circuits are resized, the intrinsic delay of the final current mirror is about 11.5 nsec in the two-section ITWP-IADC when the input signal is of full scale from 0 to 128 μA, as may be seen from the simulated waveforms in Fig. 4.4(a). In Fig. 4.4(b), the four-section ITWP-IADC is adopted and the intrinsic delay of the final current mirror is about 7.5 nsec when the input signal is of full scale from 0 to 128 μA. If the four-section ITWP-IADC is adopted and each CM_i stage consists of two current mirrors. The intrinsic delay of the last current mirror can be decreased to 6.5 nsec, as shown in Fig. 4.4(c).



(a)



(b)



(c)

Figure 4.4 (a) The simulated output current waveforms of the CM_i stage in two-section ITWP-IADC structure with full-scale step input current from 0 to 128 μA. (b) The simulated output current waveforms of the CM_i stage in four-section ITWP-IADC structure with full-scale step input current from 0 to 128 μA. (c) The output current waveforms of the CM_i stage in four-section ITWP-IADC structure (2 current mirrors in each CM stage).

4.3.2 Switched-Current Cell Circuits

In the ITWP-IADC, the switched-current cells with the clock feedthrough errors cancellation technique as proposed by Sugimoto [60], [65] are used. Figure 4.5 shows the switched-current cell circuits. The MOS transistors M1-M12 and current tails (2Ie and 2Is) can be seen as single-in-to-differential-out current buffer. The MOS transistors M1-M4 and constant current source 2Is form a differential voltage-to-current converter. M5-M12 and 2Ie form a buffer amplifier whose voltage gain is one. If the current input signal is not applied to input port (IN), the voltage at terminal IN becomes equal to the bias voltage *Vb1*. When Iin is applied to terminal IN, Ie plus Iin/2 flows in M5 and Ie minus Iin/2 flows in M6, producing the voltage difference ΔV_{in}. If the size of M1, M2, M5, and M6 are identical, ΔV_{in} can be derived from the square I-V law of the MOS transistors operated in the saturation region.

$$\Delta V_{in} = V_{gs5} - V_{gs6}$$

$$= \sqrt{\frac{1}{\beta_n}} \cdot \left(\sqrt{2\mathrm{Ie} + \mathrm{Iin}} - \sqrt{2\mathrm{Ie} - \mathrm{Iin}} \right) \tag{4.4}$$

where $\beta_n = \mu_n C_{ox}(W5/L5)$. When switches sw1 and sw2 turn on, the ΔV_{in} is applied to the inputs of a differential voltage-to-current converter and is converted to I1 and I2. Then the output current Iout can be derived from I1-I2 [60].

$$\mathrm{Iout} = \mathrm{Iin} \sqrt{1 + \frac{4}{\mathrm{Iin}^2} \cdot (\mathrm{Is} - \mathrm{Ie}) \cdot \left[2\mathrm{Ie} - \sqrt{(2\mathrm{Ie})^2 - \mathrm{Iin}^2} \right]} \tag{4.5}$$

Obviously, if Ie is equal to Is, the second term in the root in Eq. (4.5) becomes zero. Therefore, the output current is same as the input current.

$$\mathrm{Iout} = \mathrm{Iin} \tag{4.6}$$

When the switches are turned off, ΔV_{in} is stored in the MOS capacitances. In order to increase the linearity, the regulated cascode structure is used [83] in the switched-current cell circuit. As shown in Fig. 4.5(a), the MOSFETs, M35-M46, with their associated current sources, I_{B1}-I_{B12}, are common-source amplifiers that provide negative feedback to the cascoded devices and increase the output resistance of the current mirror. For switches (sw1-sw4), the NMOS transistors and dummy switches are adopted, as shown in Fig. 4.5. The charge injection error and clock feedthrough can be decreased. Moreover, the clock feedthrough from switches is greatly suppressed by the common mode rejection characteristic of the differential structure. The MOS transistors also can be served as sampling capacitance when the terminals source, drain, and bulk of MOS transistor connect together. If the MOS capacitance is operated under inversion mode, the capacitance value can be viewed as constant. Figure 4.6 shows the simulated capacitance value of one NMOS vs. its terminal voltage difference in 0.35 μm CMOS process. Apparently, if the Vgs is greater than 0.9V, the NMOS transistor can operate on inversion mode and the capacitance value can keep constant. However, the operating voltage of Vgs always closes to 2.5V in this design. Thus the MOS capacitance can be linear in the operating region.

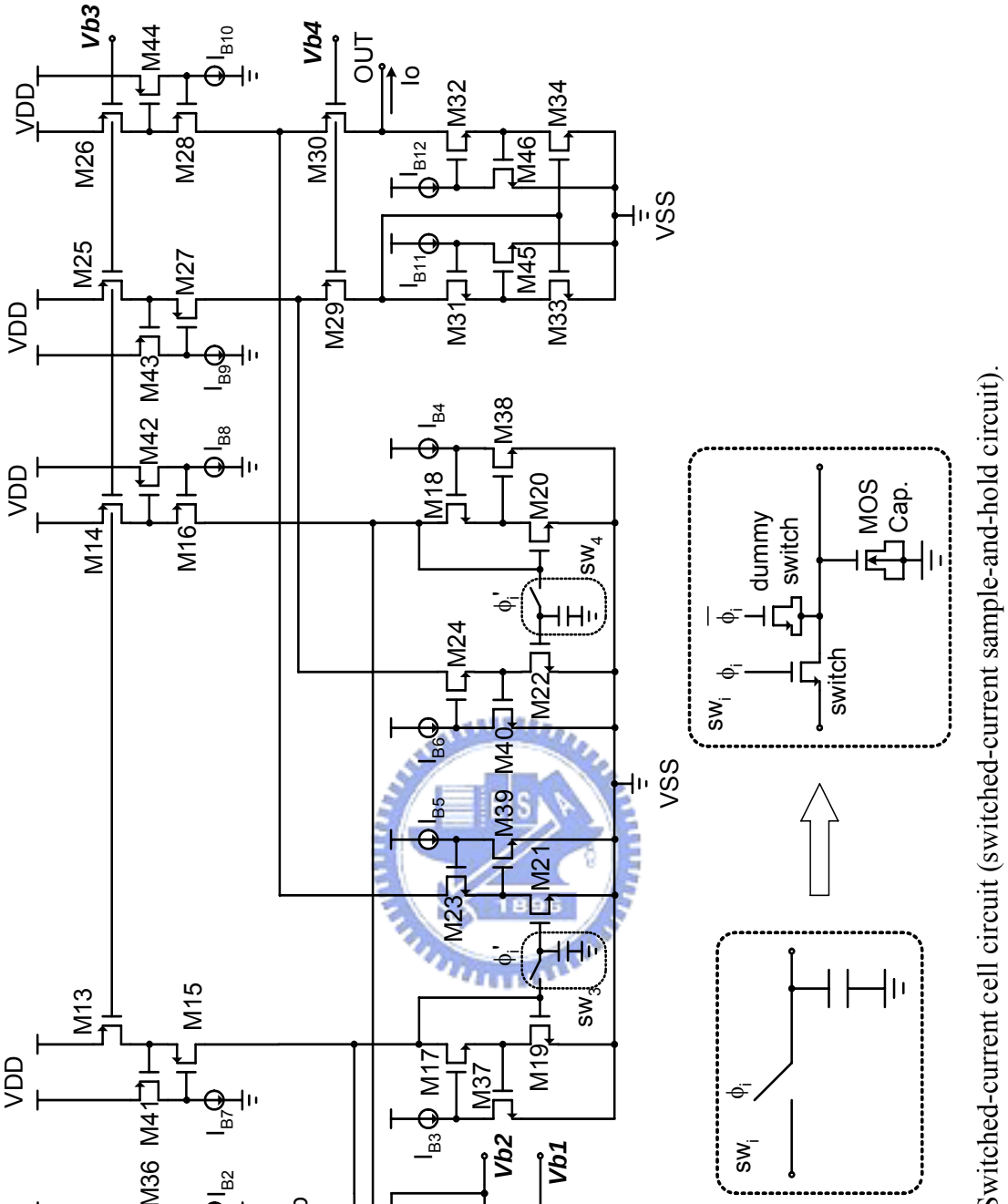


Figure 4.5 Switched-current cell circuit (switched-current sample-and-hold circuit).

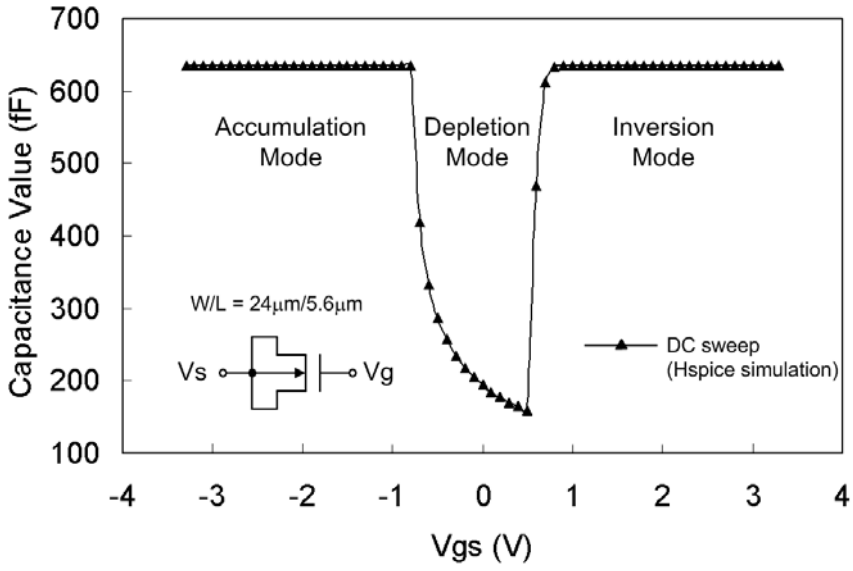


Figure 4.6 The simulated capacitance value of one NMOS vs. its terminal voltage difference in 0.35 μm CMOS process.

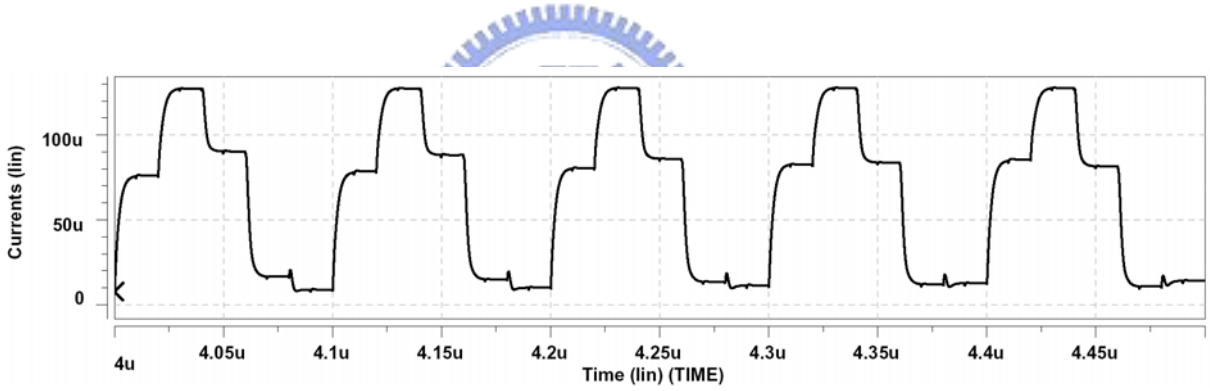
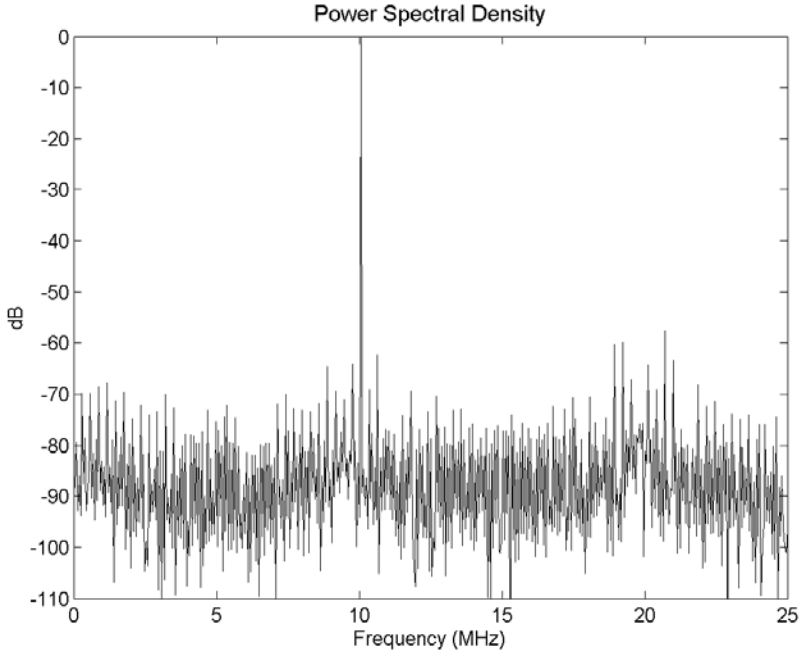
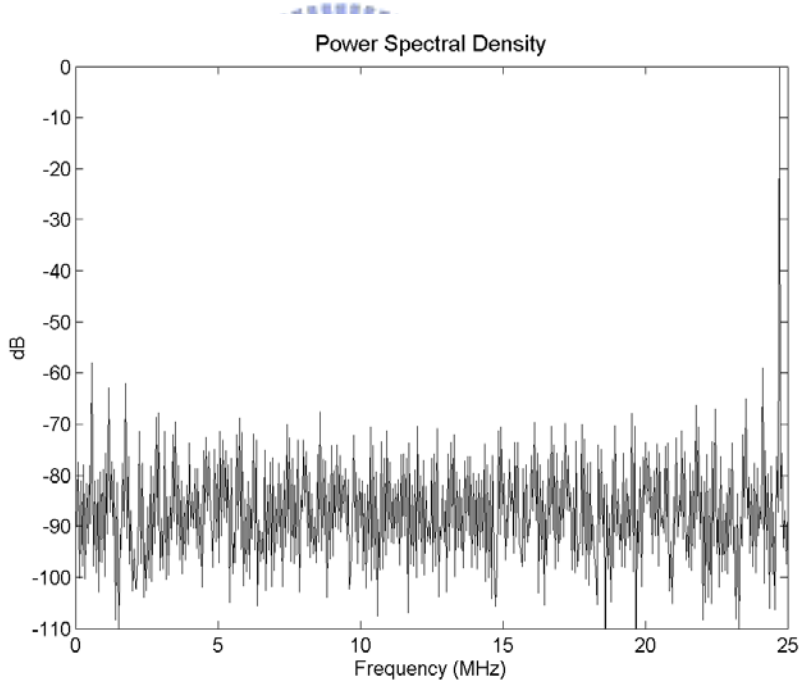


Figure 4.7 The transition waveform of the output current (Io) in switched-current cell circuit.

The transition waveform of the output current (Io) in switched-current cell circuit is shown in Fig. 4.7. The clock rate is 50 MHz and the frequency of input signal is 10 MHz. Figures 4.8(a) and 4.8(b) show the fast Fourier transform (FFT) spectrum of the switched-current cell circuits for 10 MHz and 24.7 MHz input signal, respectively. The sampling rate is 50 MHz that is the maximum necessary clock rate for switched-current cell circuit in the proposed ITWP-IADC. It can be seen from Fig. 4.8 that all the harmonic distortion components are below –58 dB.



(a)



(b)

Figure 4.8 (a) The FFT spectrum for a 10 MHz sine wave input signal, (b) The FFT spectrum for a 24.7 MHz sine wave input signal.

From the analyses of previous section, since the switched-current cells in the ITWP-IADC have relaxed timing requirement, other switched-current cell circuits could also

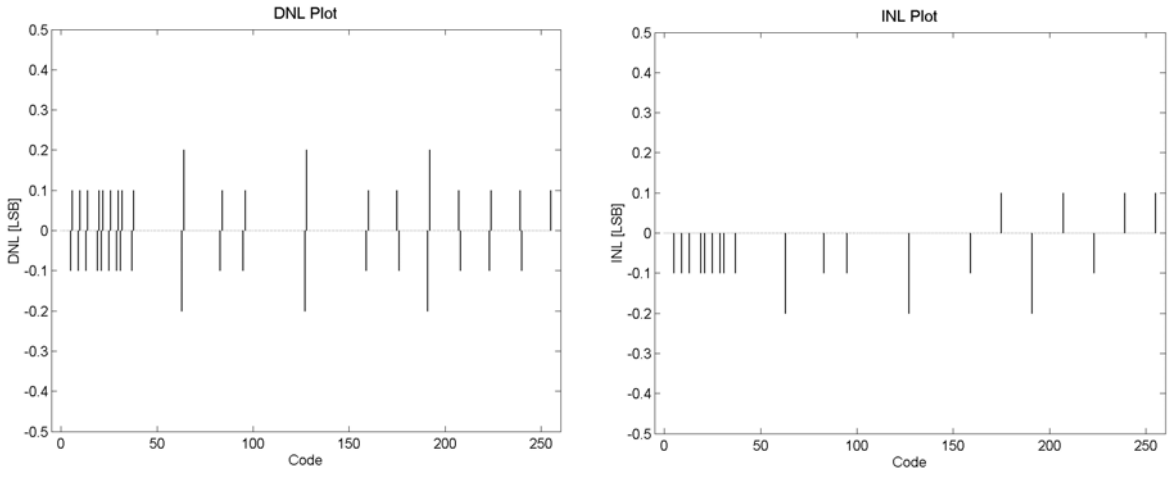
be used to satisfy both accuracy and speed requirements.

4.4 HSPICE Simulation

All simulation results are based upon the device parameters of 0.35 μm 2P4M CMOS technology with 5V power supply. The option of thick oxide is selected, thus the minimum channel length is 0.5 μm. The simulation can divide into two parts. One is for 2-section 8-bit ITWP-IADC. The other is for 4-section 8-bit ITWP-IADC.

4.4.1 Simulation Results of 2-section ITWP-IADC

Since the intrinsic delay of the final current mirror (T_{int_7}) is about 11.5 nsec in the two-section ITWP-IADC when the input signal is of full scale from 0 to 128 μA and the input signal hold time (Th_{ccmp_8}) of the current comparator is about 1.5 nsec, the proposed two-section ITWP-IADC can be operated at 77 MS/s when the input frequency is about 38 MHz. Figure 4.9 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) plot for 8-bit resolution when the proposed 2-section ITWP-IADC is operated at 77 MS/s conversion rate. The DNL and the INL for all codes are less than +0.2/-0.2 LSB.



(a) (b)

Figure 4.9 The simulation results of the 2-section ITWP-IADC (a) DNL and (b) INL for 8-bit resolution at 77 MS/s conversion rate.

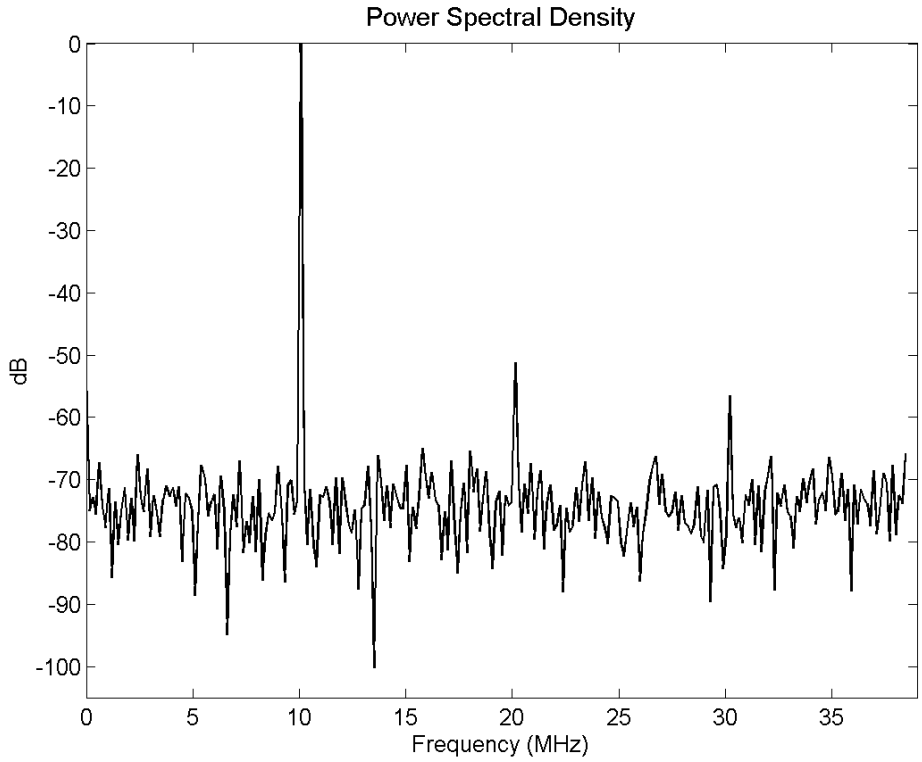


Figure 4.10 The FFT spectrum of a 10 MHz sinusoidal input with the 2-section ITWP-IADC operated at 77 MS/s conversion rate.

Figure 4.10 shows the FFT spectrum of a 10 MHz sinusoidal input with the 2-section ITWP-IADC operated at 77 MS/s conversion rate. The current input signal that is step sinusoidal waveform is directly applied to the ITWP-IADC without using the voltage-to-current (V/I) conversion interface. Since the structure of the 2-section ITWP-IADC is based on single-ended, the even harmonic are still exist. From the Fig. 4.10, the harmonic distortion components are all below -50 dB and the signal-to-noise-and-distortion-ratio (SNDR) is 45.4 dB. The SNDR versus input frequency characteristics at 77 MS/s sampling rate are shown in Fig. 4.11. It can be seen that the SNDR at low frequency is about 46 dB. Then it begins to decrease above 30 MHz and becomes 38.5 dB at 37 MHz. The degradation of SNDR at high input frequency is due to that the final current mirror needs more intrinsic delay time (T_{int_7}) to slew and settle for full-scaled current transition. A sampling rate of 100

MS/s can be achieved at an input frequency of 12 MHz. The increased sampling rate is due to the non-full-scale input currents that reduce the intrinsic delay of the last current mirror. Figure 4.12 shows the SNDR versus input frequency characteristics at 100 MHz sampling rate. Apparently, the SNDR fast degrade when the input frequency is above 12 MHz.

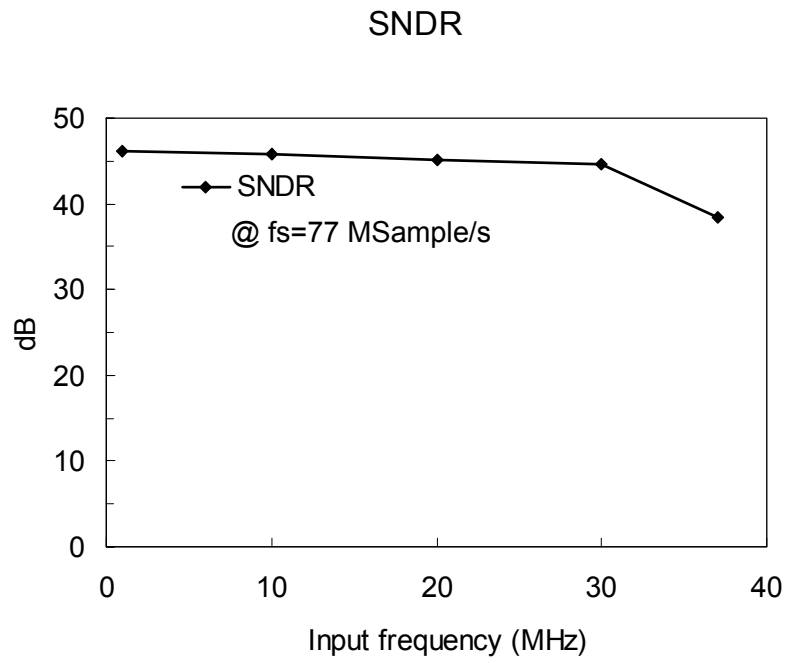


Figure 4.11 The SNDR versus input frequency characteristics at 77 MS/s conversion rate.

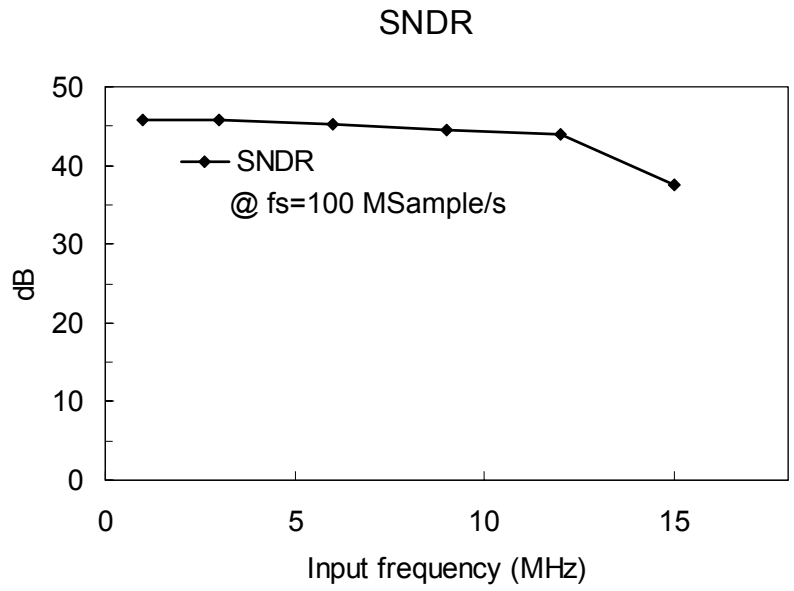
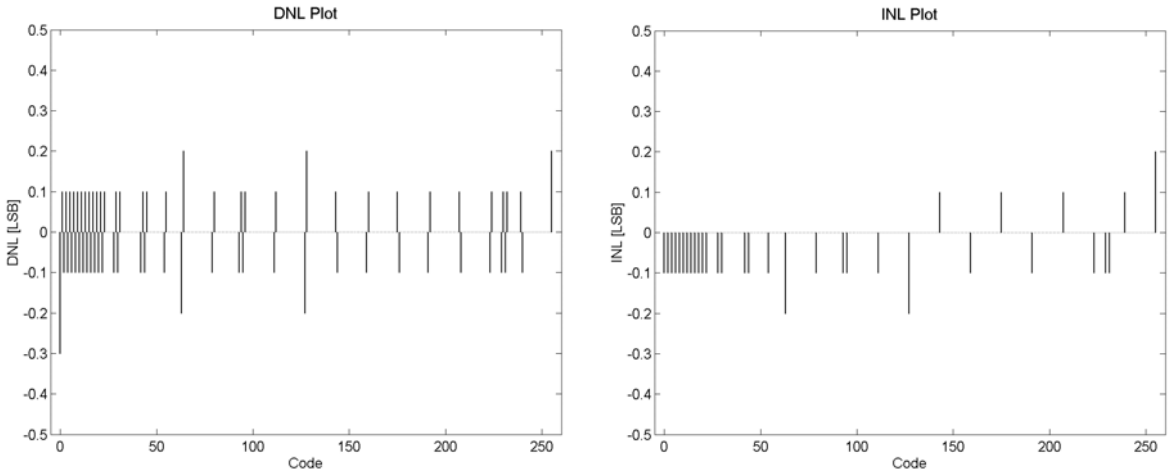


Figure 4.12 The SNDR versus input frequency characteristics at 100 MS/s conversion rate.

4.4.2 Simulation Results of 4-section ITWP-IADC

According to Fig. 4.4(b), the intrinsic delay of the final current mirror (T_{int_7}) is about 7.5 nsec in the four-section ITWP-IADC when the input signal is of full scale from 0 to 128 μA. Furthermore, the input signal hold time (Th_{ccmp_8}) of the current comparator is about 1.5 nsec. Thus the 4-section ITWP-IADC can operate at 111 MS/s (fs) when the input frequency is about 55.5 MHz (fs/2). The DNL and INL plot for the proposed 8-bit 4-section ITWP-IADC are shown in Fig. 4.13. The DNL and INL for all codes are less than +/-0.3 LSB and +/- 0.2 LSB, respectively.



(a) (b)

Figure 4.13 The simulation results of the 4-section ITWP-IADC (a) DNL and (b) INL for 8-bit resolution at 111 MS/s conversion rate.

The FFT spectrum of a 30 MHz sinusoidal input with the 4-section ITWP-IADC operated at 111 MS/s conversion rate is shown in Fig. 4.14. The harmonic distortion components are all below -50 dB and the SNDR is 44.2 dB. Figure 4.15 shows the SNDR versus input frequency characteristics at 111 MS/s sampling rate. It can be seen that the SNDR at low frequency is about 45 dB. Then it begins to decrease above 50 MHz and becomes 39.1 dB at 55 MHz. Figure 4.16 shows the SNDR versus input frequency

characteristics at 130 MS/s sampling rate. If the sampling rate is 130 MHz and input frequency is 16 MHz, the maximum transition step of input current is 50 μA. It is non-full-scaled. Thus the sampling rate can increase. Figure 4.16 shows that the SNDR fast degrade when the input frequency is above 16 MHz.

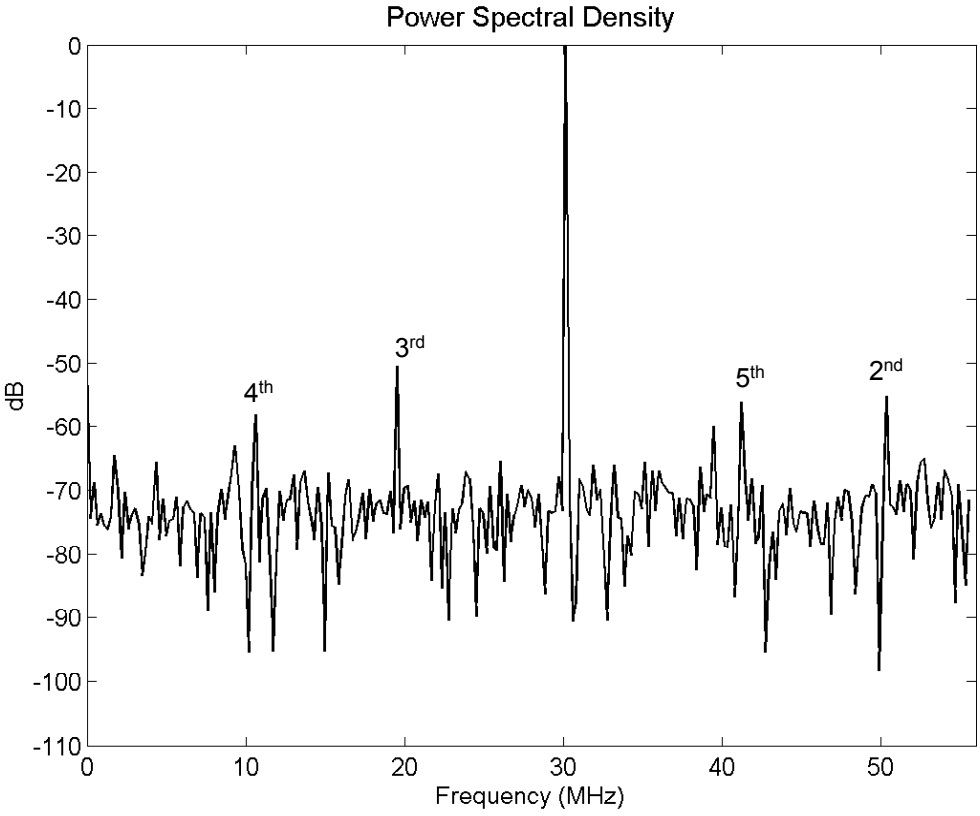


Figure 4.14 The FFT spectrum of a 30 MHz sinusoidal input with the 4-section ITWP-IADC operated at 111 MS/s conversion rate.

If the delay time of path B (as shown in Fig. 3.3) can be reduced such that the path can become non-critical, then the total number of current mirrors in stage CM_i can be reduced to two. Meanwhile, if the intrinsic delay of the last current mirror and the comparator hold time can be reduced to 5 nsec and 1 nsec, respectively, then the four-section ITWP-IADC can achieve a sampling rate of 166 MS/s at an input frequency of 19.2 MHz. The major characteristics of simulation result are list in Table 4.1.

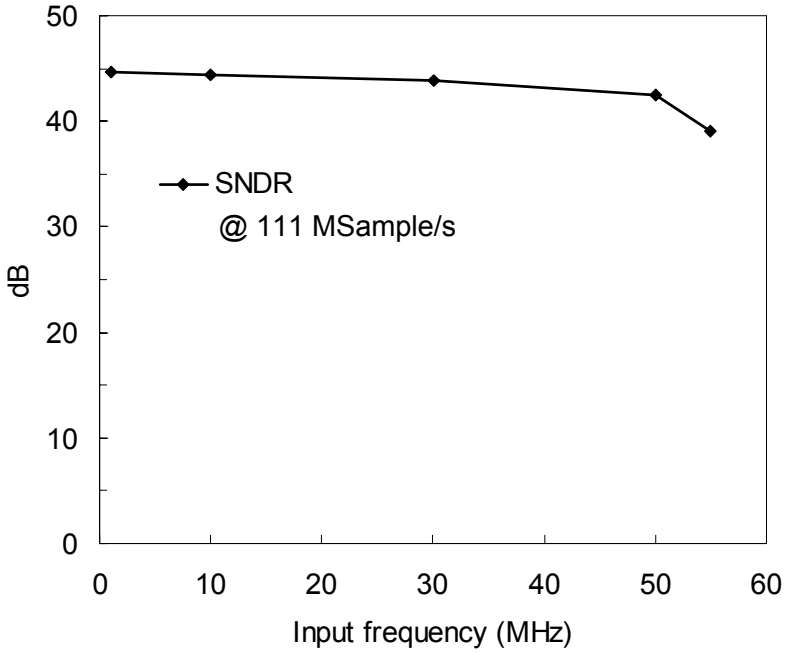


Figure 4.15 The SNDR versus input frequency characteristics for 4-section ITWP-IADC at 111 MS/s conversion rate.

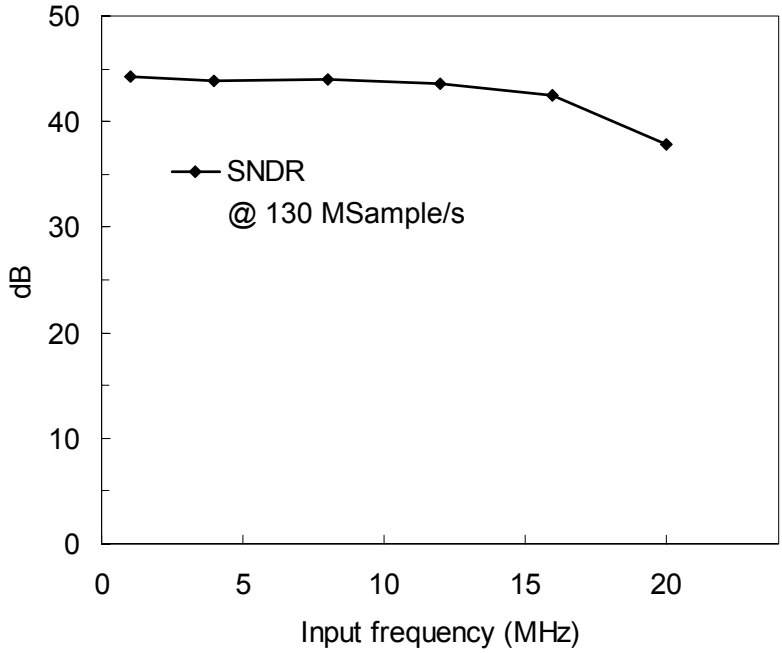


Figure 4.16 The SNDR versus input frequency characteristics for 4-section ITWP-IADC at 130 MS/s conversion rate.

In Table 4.2, the performance of the ITWP-IADC is compared with that of other known CMOS current-mode pipelined ADCs. It can be seen from that the ITWP-IADC has the superior speed performance.

Table 4.1

Major characteristics of simulation results for the ITWP-IADC

Technology	0.35 μm 2P4M CMOS	0.35 μm 2P4M CMOS
Architecture	2-section ITWP-IADC	4-section ITWP-IADC
SNDR	(f_s = 77 MHz, f_{in} = 1 MHz) 46.2 dB, ENOB=7.4-bit (f_s = 77 MHz, f_{in} = 37 MHz) 38.5 dB, ENOB=6.1-bit (f_s = 100 MHz, f_{in} = 12 MHz) 43.9 dB, ENOB=7-bit	(f_s = 111 MHz, f_{in} = 1 MHz) 45.6 dB, ENOB=7.3-bit (f_s = 111 MHz, f_{in} = 55 MHz) 39.1 dB, ENOB=6.2-bit (f_s = 130 MHz, f_{in} = 16 MHz) 43.0 dB, ENOB=6.9-bit
DNL	+0.2/-0.2 LSB (f_s = 77 MHz)	+0.2/-0.3 LSB (f_s = 111 MHz)
INL	+0.1/-0.2 LSB (f_s = 77 MHz)	+0.2/-0.2 LSB (f_s = 111 MHz)
Full Scale Current	0 ~ 128 μA	0 ~ 128 μA
Unit LSB Current	0.5 μA	0.5 μA
Power Dissipation	467 mW	462 mW
Power Supply	5 V	5 V

Table 4.2

Comparison of CMOS current-mode pipelined ADCs

	Res. (bits)	Architecture	Sample Rate	Technology
[103]	6	8 parallel pipeline ADCs	32 MS/s (4 MS/s per pipeline ADC)	0.8 μm
[94]	8	4 parallel pipeline ADCs	70 MS/s (17.5 MS/s per pipeline ADC)	0.8 μm
[102]	7.43	Pipeline ADC	3 MS/s	0.8 μm
[96]	6.35	Pipeline ADC	15 MS/s	0.8 μm
[107]	6.1	32 parallel pipeline ADCs	4 GS/s (125 MS/s per pipeline ADC)	0.35 μm
This dissertation	8	FWP-IADC	55 MS/s - 90 MS/s	0.35 μm
	8	2 - section ITWP - IADC	77 MS/s - 100 MS/s	0.35 μm
	8	4 - section ITWP - IADC	111 MS/s - 166 MS/s	0.35 μm

4.5 Summary

In this chapter, the new architectures of the ITWP-IADC are proposed and analyzed for the design of current-mode analog-to-digital converter (IADC). The novelty lies in that the switched-current cells are incorporated into the wave-pipelined stages to obtain better speed performance. The ITWP-IADCs have several advantages, including high-speed performance, high input frequency, relaxation of the clock period of the switched-current cells, and increased linearity by reducing the total number of switched-current cells. The timing constraints are also given in this chapter. HSPICE simulation results reveal that two-section ITWP-IADC and four-section ITWP-IADC can achieve sampling rates of 77 MS/s and 111 MS/s, respectively under Nyquist rate sampling with 8-bit resolution. Moreover, the ITWP-IADC with two wave-pipelined sections can achieve a sampling rate of 100 MS/s with 8-bit resolution when the frequency of the input signal is 12 MHz. It is expected that the sampling rate of the 8-bit four-section ITWP-IADC can reach 166 MS/s at an input frequency of 19.2 MHz.