# Chapter 5

# Conclusion and Future Work

## 5.1 Main Results of This Thesis

In this thesis, several new architectures for current-mode analog-to-digital converters (IADCs) have been proposed and analyzed. The developed architectures are: (1) a pipelined ADC that uses the open-loop voltage-mode sampling and current-mode processing techniques; (2) a current-mode ADC that adopts the full wave-pipelined architecture; (3) a current-mode ADC which uses the indirect transfer wave-pipelined architecture. The proposed ADC architectures are very suited to high-speed operation. Thus, they can be applied to many key applications like digital oscilloscopes, Gigabit Ethernet receivers, LCD displays, etc.

Firstly, the voltage-mode sampling is adopted to avoid the speed bottleneck of the switched-current (SI) sample-and-hold circuits. Moreover, the open-loop structure is used to overcome the speed limitation of the closed-loop structure in the conventional pipelined ADCs. For the proposed open-loop architecture, open-loop voltage sampling structure and current-mode structures for subtraction, sub-DAC operation, and comparison are used to improve the speed performance of pipelined ADC. Those of voltage sample-and-hold circuit, V-I converter, and current comparator determine the delay per pipelined stage where voltage sample-and-hold circuit and V-I converter dominate. If the dominant delay could be reduced significantly, the speed of the proposed new ADC architecture can be greatly improved. From the post-simulation results, it can be seen that the proposed pipelined ADC architecture can be applied to the design of ADC with 8-bit accuracy at a sampling rate up to 71.4MS/s. The

proposed ADC circuit has been fabricated by 0.25 μm 1P5M CMOS technology. Due to the gain error of the sample-and-hold circuit (SHC) and the input offset current of the comparator, the measurement results of the prototype chip show the differential nonlinearity (DNL) and integral nonlinearity (INL) for all codes are less than +1.9/-1 LSB and + 2.8/-2.8 LSB, respectively. The dynamic test shows that the effective number of bit (ENOB) is 6.2-bit under 40-MSample/s sampling rate. The power consumption is 195 mW. If the gain calibration and comparator offset cancellation techniques are used, it is expected that the speed and accuracy performance can be further improved.

Secondly, a new architecture of the full wave-pipelined current-mode ADC (FWP-IADC) is proposed and analyzed for the design of current-mode analog-to-digital converter (IADC). The novelty lies in the application of wave-pipelined theory to form the FWP-IADCs and improve the speed performance of the IADCs. Furthermore, it is the first application of the wave-pipelined theory in analog IC design. The full current-mode wave-pipelined structure is used in each stage of the FWP-IADC, without inter-stage switched-current cell circuits. There are several advantages in the FWP-IADCs. It includes high-speed performance, high input frequency, more efficiency use of timing, and increased linearity by removing the switched-current cells. For 8-bit resolution, the DNL and INL of the post-simulated results are below +/- 0.2 LSB when operated at the sampling rate of 55MS/s. From the HSPICE post-simulated results, the FWP-IADC can achieve sampling rates of 55 MS/s under Nyquist rate sampling with 8-bit resolution. Moreover, the FWP-IADC can achieve a sampling rate of 90 MS/s with 8-bit resolution when the frequency of the input signal is 3 MHz.

An experimental chip for the proposed FWP-IADC has been fabricated in 0.35 μm 2P4M CMOS technology. The measurement results have successfully demonstrated that the proposed design concept and architectures can be applied to the design of future high-speed IADCs.

Finally, design techniques for indirect transfer wave-pipelined current-mode analog-to-digital converters (ITWP-IADCs) are proposed and analyzed. The main concept lies in that the switched-current cells are incorporated into the wave-pipelined stages to obtain better speed performance. The advantages of ITWP-IADCs also include relaxation of the clock period of the switched-current cells and increased linearity by reducing the total number of switched-current cells except for the advantages of FWP-IADC. The timing constraints are also given in this work. The DNL and INL of the simulation results are below +/- 0.2 LSB for two-section ITWP-IADC when the sampling rate is 77MS/s. In four-section ITWP-IADC, the DNL and INL are less than +/- 0.3 and +/- 0.2 LSB, respectively when the sampling rate is 111 MS/s. From HSPICE simulation results, it can also be seen that two-section ITWP-IADC and four-section ITWP-IADC can achieve sampling rates of 77 MS/s and 111 MS/s, respectively under Nyquist rate sampling with 8-bit resolution. Moreover, the ITWP-IADC with two wave-pipelined sections can achieve a sampling rate of 100 MS/s with SNDR of 43.9 dB when the frequency of the input signal is 12 MHz. It is expected that the sampling rate of the 8-bit four-section ITWP-IADC can reach 166 MS/s at an input frequency of 19.2 MHz.

## 5.2 Future Work

According to analysis and experimental results obtained from the previous chapters, there are several suggestions for future research into the design of high-performance ADCs.

In the proposed open-loop pipelined ADC, the following suggestions can be made for future work.

1. Architecture Level:

   The proposed open-loop structure can be combined with the conventional pipelined ADC as the reported researches [40]. It can relax the required resolution in the later

pipelined stages. In other words, it can sustain more input offset of the comparator. Moreover, the calibration techniques must be adopted to solve the inaccurate gain problem of the open-loop sample-and-hold circuits.

2. Circuit Level

   High-performance current comparator is needed in this architecture. Especially, the offset cancellation techniques of the current comparator must be used to improve the resolution.

Meanwhile, there are several recommendations for future research into the design of WP-IADC.

1. Architecture Level

   First, the single-end topology in the FWP-IADC or ITWP-IADC can expand to differential topology to suppress the even order harmonic distortion. Second, the reference non-restoring algorithm [48] can adopt to improve the accuracy and relax the required resolution in the later pipelined stages. Third, the digital error correction techniques can be used to obtain the better resolution in the FWP-IADC or ITWP-IADC. Finally, the process variation must be considered carefully.

2. Circuit Level

   Because the analog delay components consist of current mirror, the high-performance current mirror is required. It is needed to develop the current mirror that has low-input-impedance and high-output-resistance. Moreover, the problem of channel length modulation must be solved. Besides, the offset cancellation techniques of the current comparator must also be used to improve the accuracy.