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應用類神經網路於蝕刻製程之缺陷分析與預測

An Online/Offline Prediction Model for RIE Using Neural
Networks

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中華民國九十五年九月

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摘要

現今半導體製程中，包含上千道的製程步驟，以及參數。要如何有效的監控與偵測製程參數異常，製程監控機制就扮演著不可或缺的角色。為了要提高產量及良率，降低製程缺陷之發生，監控製程的每一步驟是否異常，藉由製程參數之錯誤偵測(Defect Detection)，以及預先一步預測缺失的發生，來達到此一目標。本論文之目的即在氧化物反應性離子蝕刻(Reactive Ion Etching, RIE)製程中，發展一套能夠即時監控，並且預測下一批貨或是下一個製程步驟之製程參數有無出現異常之方法。來解決上述提及之問題。

在本論文中，利用主成分分析(Principle Component Analysis, PCA)以及類神經網路(Neural Network, NN)來分析製程參數資料，製程因子先經由主成分分析處理後，得到主要成分，再送入針對 RIE 製程參數所建立完成之類神經網路，預測其是否出現異常；根據實際的製程需求及情況，可將 RIE 製程分為兩部分來建立其製程監控模型，第一部份利用全部製程步驟之資訊，來偵測參數異常狀況，稱之為離線(Offline)錯誤偵測模組；另一部份利用前三個製程步驟即時資訊來預測第四個製程步驟之異常，稱之為即時(Online)錯誤偵測模組。

經由實際製程參數資料及上述兩個模組實驗驗證後，確實能夠偵測及預測出製程參數之異常。同時，藉由此監控機制，可減少當製程異常時，排除異常的時間，並且達到低成本即時控制之應用。

An Online/Offline Prediction Model for RIE Using Neural Networks

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Abstract

The fabrication of modern semiconductor products requires thousands of processing steps. A key element in achieving high yields during semiconductor fabrications is to minimize the amount of defected wafers. Therefore, detecting the defected wafers and predicting the wafer status are very important issues.

In this study, BPNN is the backbone of prediction models and the BPNN inputs were prepared in three different ways: raw data by using the first set of data points, capturing samples from the original data, and the statistical summary values by calculate the mean and standard deviation values for each step.

Four prediction models are established to predict the wafer status: offline back-propagation neural network (BPNN), offline principle component analysis BPNN (PCABPNN), online BPNN, and online PCABPNN. These models have the potential to

reduce the overall cost of ownership of semiconductor equipment by increasing the wafer yield and throughput of product wafers, and not depend upon monitor wafers or expensive metrology rather it will enable inexpensive real-time wafer-to-wafer control applications in RIE.

This study establishes a method for deciding the significant process parameters which affect the wafer status in RIE by comparing the result of applying each process parameter alone in BPNN. The significant parameters for all etching steps combined together in offline BPNN to tackle the defected wafer. Furthermore the significant parameters for the first three etching steps combined together in online BPNN to forecast the wafer status. By modifying the significant parameters when online BPNN model predicts the defected wafer, the down-time and mean-time-to-repair of the equipment can be decreased.

The evaluation results for the four models demonstrate that each model has its advantages and disadvantages under different BPNN input preparations. However, preparing statistical summary as BPNN inputs has less error prediction. Therefore, using statistical summary in online PCABPNN is recommended to enable rapid prediction of wafer status in RIE which greatly reducing test wafer necessity.

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Dedication

To some world peace is a dream; attractive, alluring,

desirable, fascinating,

perhaps even a little intoxicating; but still a dream...

Then there are those who make dreams come true...

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List of Abbreviation

AENN	: Auto-Encoder Neural Networks
AIC	: Akaikes Information Criterion
BPNN	: Back Propagation Neural Networks
DPM	: Defects per Pillion
D-S	: Dempster–Shafer theory
FIS	: Final Information Statistic
IC	: Integrated Circuit
IMC	: Internal Model Control
LVQ	: Learning Vector Quantization
MCM	:Multi-Chip Modules
MPC	: Model Predictive Control
MSM	: Metal Semiconductor Metal
NIC	: Network Information Criterion
NN	: Neural Networks
NNIC	: Neural Network Information Criterion
OES	: Optical Emission Spectroscopy
PCA	: Principal Component Analysis
PNN	: Polynomial Neural Network
PSC	:Power Ship Corp.
R&D	: Research and Development
RBFN	: Radial Basis Function Network
RF	: Radio Frequency

RG : Residual Gas Analysis
RS : Response Surface Model
SO :Shutoff Valve
TS : Time Series Neural Networks
VL : Very Large Scale Integrated

CHAPTER 1

INTRODUCTION

The technology of semiconductor fabrication is complex, and requires many specialized process steps. These steps include wafer preparation, device fabrication, device test, and packaging. Device fabrication is the most complex manufacturing step in production of semiconductor integrated circuits, and typically includes photolithography, ion implantation, etching, thermal treatments, chemical vapor deposition, physical vapor deposition, molecular beam, electroplating, chemical mechanical polishing, wafer testing and back grinding [1].

The integrated circuit (IC) growth performance over the past 40 years has been both influential, and ubiquitous as Moore's law –which states that the numbers of transistor per chip, or per IC will double every year or two– while their cost remains the same. The correctness of Moore's Law aggressively facilitates the scaling down and integration of IC devices, so that smaller and smaller devices are enabled in larger and larger quantities [2]. These advanced talents have also put more constraints on the design manufacturability. Because the manufacturing process has become less tolerant to variations, which easily could be source of defects.

1.1 Defect Reduction Overview

In order to achieve low yield loss and high quality, semiconductor manufacturer maximize their yield rates during process life cycle. The intentions of the process life cycle phases are different, consequently the technology requirements for defect detection in those phases are different and requires specific defect detection tools or recipes as well. Figure 1.1 illustrates semiconductor lifecycle phases, where these three phases are defined by the defect reduction technology subgroup [3, 4]:

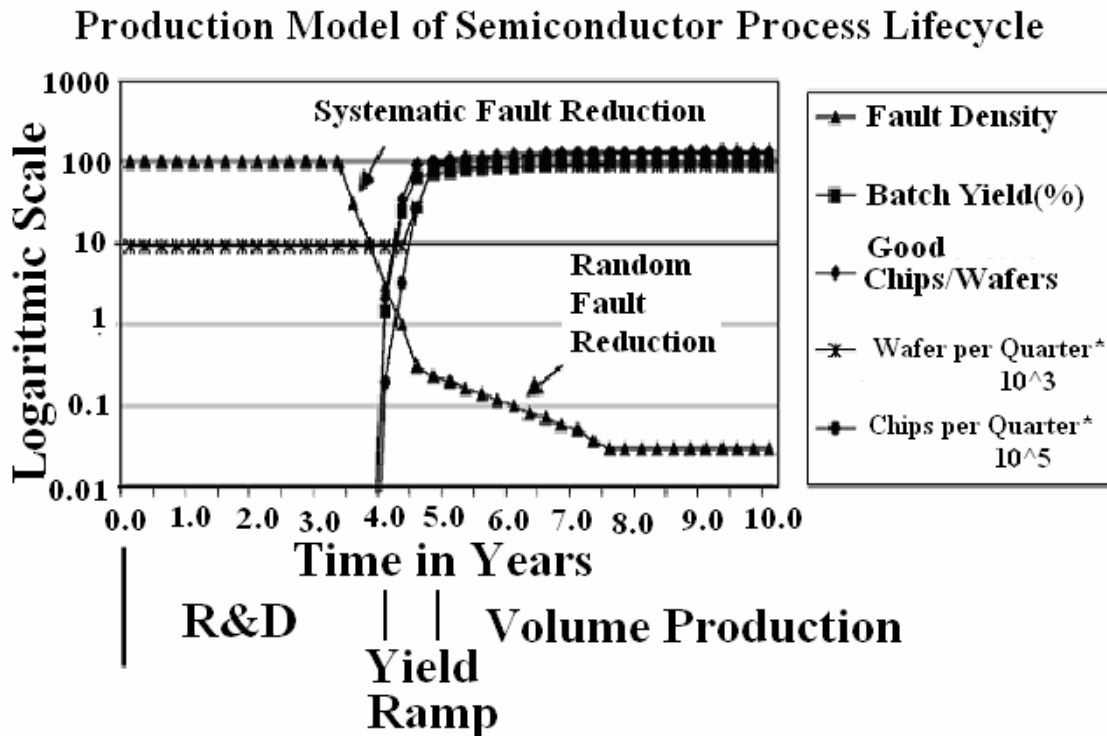


Figure 1.1: Fault density, yield, and output as a function of the time since the inception of a semiconductor technology node. [5]

- Process Research and Development (R&D): is characterized by relatively low production rates and yields, experimental development of process parameters, detailed characterization and identification of defects.
- Yield Ramp (Yield Enhancement): is defined as an improving the baseline yield for a given technology generation starts from R&D yield level and ends by volume production. During this phase, the yield moves from approximately 20% to 80%. There are two ways to achieve the required yield ramp: reduce the total number of defect and fault sources, also reduce the time to source and fix each new defect source of mechanism.
- Volume Production: This phase represents the final stage of the semiconductor process life cycle, in which no further tuning of the process control parameters is attempted. The objective of using defect detection tools in this stage is to identify process excursions as rapidly as possible, which requires very-high-throughput tools and methods. In this phase the process is well seasoned, so the problems are frequently catastrophic and could involve shutting down the line when faults occurred.

The rapid identification of defect and fault sources through integrated data management continues to be the essence of rapid defect learning [4]. Defects must be detected, analyzed, and eliminated within brief period of time. Particularly, the visual inspection plays a fundamental role in defect detection. The visual inspection is often carried out by a human expert. However, new technology features have made this inspection unreliable. For this reason, many researchers have been engaged to develop automatic analysis of manufactures processes, defect prediction models, and automatic

optical inspections. Moreover neural networks model has first-rate in defect prediction, and automatic optical inspections.

1.2 Motivation

As the semiconductor processing technology approaches the 0.1 mm feature size and 300 mm wafer diameter, the customer demands for low defects per million (DPM) have not change. Fundamentally, there are only two ways to meet these demands: first, allow fewer bad or weak die to reach the customer. Second, reduce the intrinsic number of bad or weak die [6]. In the direction of facing the customer demands, the industry has strived to improve the yield, and equipment utilization.

To optimize the yield and equipment utilization during semiconductor fabrications, the wafer defects should be minimized and properly processed wafers at each step should be confirmed. On other hand, measuring each wafer after each step is extremely difficult, due to cost and consumes long time for measuring each wafer after each step. As of now, experts in this industry usually measure and monitor wafers periodically, especially right after performing preventive maintenance and changing machine settings. A final test is performed on each wafer after all steps. Thus, if an error occurs, it is very likely that many wafers are misprocessed without notice until very late. Because of the late notice, it is extremely difficult to trace back and locate the faulty step and diagnose the problem. Therefore, one can save considerable resources by predicting the wafer state after or during each step. In this research it has been demonstrated that it is possible to do so in RIE process.

Reactive ion etch (RIE) is commonly used in VLSI as plasma etching method, where ions remove and react with wafer surface substrate in plasma environment. In addition, it is very difficult to control plasma etching process, since the physical mechanism of this process is not well understood.

Wafer defect occurs in RIE when there is a sudden change in etching behavior. This change can happen due to operator errors, or machine errors, such as gas leak, power fault, and pressure fault. The main defect in oxide RIE is un-open etch, this defect costs 10%-20% yield loss in PSC. Un-open etch signify the inadequate etching space in the wafer surface (see figure 1.2). This thesis explores the various issues of wafer defect and monitoring includes un-open etch defect diagnosis, offline defect prediction model, online defect prediction model, and the difference between these two prediction models.

Many modeling techniques have been used to model the plasma etching throughput. However, they are limited in their ability to predict the yield quality and do not provide the flexibility to detect the wafer defect during etch process. This thesis focuses on the development of RIE output by predicting the wafer defect during/after etching process. Predicting wafer status is supported by careful experimental design and implementation. In the long term, this study will improve etch yield, at least in the following aspects:

- (1) It will aid in identifying the dominant relationships between the wafer defects and etch factors. Therefore very good product quality will be achieved with continuous production.
- (2) It provides a fundamental understanding of the mechanisms involved in defects formation which is important for reliability during RIE process.
- (3) It offers offline model; this model will present a practical estimation of wafer status after etching process.
- (4) In addition, it presents online model to predict wafer status after stabilization steps during etching process.
- (5) This research performs wafer inspection for RIE process without scarifying wafers yield, and not depending upon monitor wafers or expensive metrology which is the main benefit of predicting the wafer status.
- (6) It will enable inexpensive real-time wafer-to-wafer control applications in RIE.

1.3 Problem Statement

Reactive ion etching (RIE) is a key process in VLSI circuit fabrication, which combines physical ion bombardment and chemical reactions in plasma etching process. In addition, this critical technology is not only very expensive, but also difficult to control because it is not well understood [7]. In fact, a malfunctioning plasma etcher can generate high yield loss.

Silicon dioxide film etching is one of the major interests in IC interlayer dielectric material and multi-chip modules (MCM). A silicon dioxide film etching without any errors is a complex task. One of the significant detractive defect in this process is un-opened etch (figure 1.2). Process engineers have to ensure that not only the processes and products are high-yielding but also that errors in manufacturing are eliminated as quickly as possible through continuous and timely improvements.

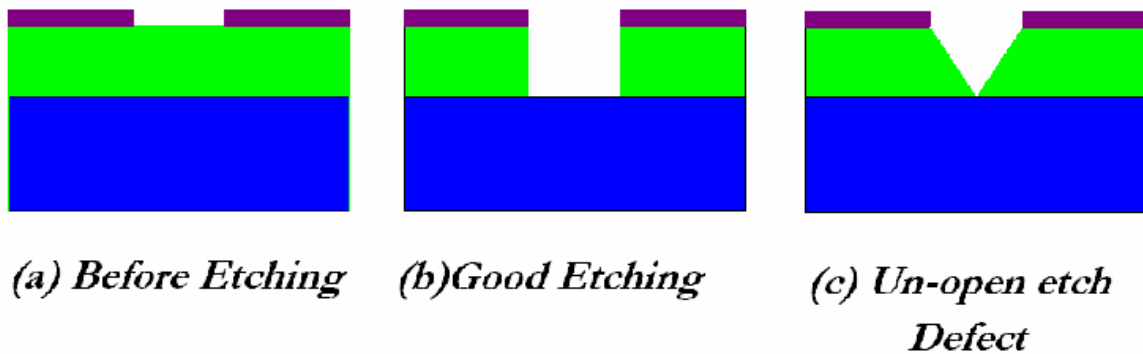


Figure 1.2: Wafer surface shape before and after etching process.

1.4 Thesis Statement

This thesis attempts to gain an understanding of the relationship between the un-open etch defect and RIE process, as well as providing empirical models to predict wafer status. Predicting wafer status in RIE is important to enhance yield, quality, and efficiency. Deep analysis has been done to improve the prediction model with the purpose of providing valuable benefits. Furthermore preparing data for neural network has been discussed and applied in three different ways.

1.5 Thesis Approach

In RIE process, the final yield is a result of intensive interactions between process factors, etchant molecules, and wafer surface. In our approach, BPNN with/without PCA provides a comprehensive view of process factors and bridging them with the wafer status during/after the RIE process, thus this approach will emphasize the applications of predicting the wafer defect and evaluate the relationship between RIE factors and wafer defect.

To more fully understand of this work, some additional background information is addressed in the next chapters. On the way to achieve the goal of predicting the wafer defect, the following steps are performed:

Step one: Full understanding of the RIE process, and some additional background information such as plasma effect on etching process, back propagation neural network, and principle component analysis.

Step two: Analyze the RIE factors and their interaction with an un-open etch defect.

Step three: Consider the RIE data from PSC, and properly prepare them in three different ways: raw data, sampling data, and statistical summary.

Step four: Apply RIE factors in BPNN each factor alone to find significant factors for each classification.

Step five: Decide the significant factors combination and apply these combination in offline BPNN model.

Step six: Using PCA to represent the original data.

Step seven: Properly apply PCs in offline PCABPNN model.

Step eight: Build online defect prediction model, using the data of the first three etching steps, and follow previous steps to obtain online BPNN model and online PCABPNN model.

Step nine: The numerical and performance results of the online and offline prediction models will be evaluated as well as, the advantages, and disadvantages will be clarified.

1.6 Thesis Organization

This thesis presents an integration framework to diagnosis the defect occurred during RIE process. We begin with Chapter 2 reviewing neural network models and related works. Chapter 3 demonstrates etch process, Chapter 4 depicts the application of PCA in RIE. Chapter 5 shows offline defect prediction model for RIE using neural networks besides, its simulation results. Also, it shows the online model. Finally, Chapter 6 the conclusion includes summarizing important contributions of this thesis and discussing some interesting future directions.

CHAPTER 2

NEURAL NETWORK

In the recent years, neural networks have been successfully applied in pattern recognition, modelling tool and as a function approximation. Furthermore, neural networks model has potential capability in modelling and control of non-linear dynamic systems, which conventionally used for dynamic processes, such as model predictive control (MPC), internal model control (IMC), and model inversion control. Several semiconductor manufacturing research investigate the application of artificial neural networks (ANN) in process optimization, control, and diagnosis [8-13].

On the other side, semiconductor manufacturers have faced unprecedented operation dilemmas and challenges, and some back-end semiconductor manufacturers were forced to merge. To survive in such a tough industry environment, semiconductor front-end manufacturers must have superb products and production technology, and they must continuously improve their production capability and increase production efficiency in order to save costs and to increase sales.

2.1 Related work

Neural networks have seen an explosion of interest over the last few decades, and are being successfully applied in semiconductor inspection systems [9, 14-17]. The major reason for adopting neural networks is because neural networks have potential capability in modelling and controls of non-linear systems categorization. Moreover neural networks have the ability of learning arbitrary nonlinear mappings between noisy sets of input and output data. Back-propagation neural network (BPNN) is currently the most popular learning rule used in supervised learning, which also known as feed forward neural networks and multilayer perceptron (MLP).

Back propagation through time is a very powerful tool, with application to solve the problems of prediction, optimization, control, and diagnosis in the semiconductor manufacturing process. [18-21]. Most of the literatures adopt BPNN because it has advantages of an easier-comprehended theory, faster recalling speed and higher learning accuracy. However, the determination of the structure architecture and the parameters under this network is difficult. Since the function approaching ability of neural network depends on the architecture of network, poor prediction can be resulted due to the parameters and the complexity of the problem itself, or an improper selection of the architecture or parameters, and vice versa. The parameters of neural network include the number of hidden layers, number of hidden units, learning rate and momentum, etc. These factors have a very great influence on the quality of approximation ability of neural network. Fogel [22] suggested the use of final information statistic (FIS) based on Akaike's information criterion (AIC) to determine the number of hidden layers and

neurons. Murata and Yoshizawa [23] and Onoda [24] proposed improved methods of AIC by applying statistical probability and energy function to determine the number of neurons. Their methods are called network information criterion (NIC) and neural network information criterion (NNIC), respectively. Taguchi method has also been used to design the parameters for neural network in previous researches. Khaw, Lim and Lim [25] applied Taguchi method to design the parameters and verified that the method could design the optimal parameters fast and robustly. Santos and Ludermir [26] applied factorial design to assist the design and implementation of a neural network.

Numerous researchers have studied pattern classification by using BPNN for the automatic inspection system in the semiconductor industry [27-29]. Zoroofi *et al.* [27] used curve recognition to detect the contamination on a wafer surface during semiconductor production. Three conventional classification models, a back-propagation technique, a minimum distance algorithm and a maximum likelihood classifier, were used and the performance of these three models was compared. The results showed that the back-propagation classifier has a better classification performance. Su *et al.* [28] proposed a neural-network approach for semiconductor wafer post-sawing inspection. BPNN, radial basis function network (RBFN), and learning vector quantization (LVQ) were employed in the inspection models. The inspection results showed that both BPNN and LVQ have excellent prediction result with 100% accuracy. Chen *et al.* [29] used BPNN in the etch semiconductor process to identify and classify endpoint curves. By real-time monitoring of changes in the endpoint curve, the abnormalities of products can be detected immediately. The system can reduce the uncertainty in the process curve

classification and provide machine shut-down suggestion immediately when necessary. In this respect, back propagation neural network utilized to identify and predict the wafer status after/ during RIE. Next section deals with back propagation neural networks (BPNN).

2.2 Back Propagation Neural Networks Structures

Neural networks have emerged as an important tool to model and diagnose problems in complex manufacturing process. There are many types of neural networks to map the complex relationship between input and output through supervised training algorithms, such as associate memory networks, radial basis functions and back propagation neural network (BPNN). The BPNN consists of input layer, output layer and several parameters include: the number of hidden layers, number of hidden neurons, learning rate, momentum, etc. All of these parameters have significant impacts on the performance of the neural-network.

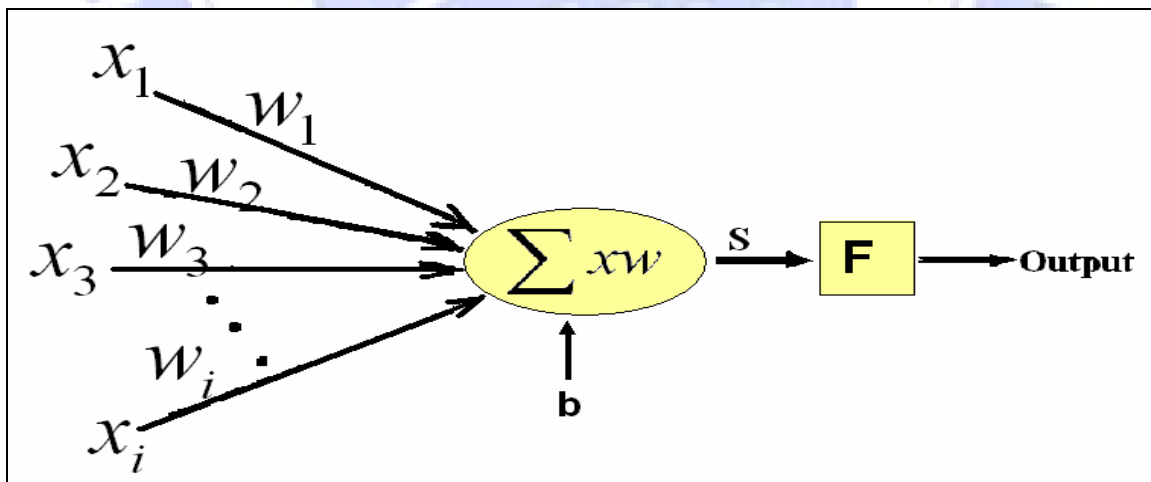


Figure 2.1: The artificial neural network cell

Neural network cells (neurons) are the basic elements of neural networks [30]. In general, the neurons are connected by links in term of weights. Neural networks may consist of multiple layers of neurons interconnected with other neurons in different layers. These layers consist of one input layer, one or more hidden layers and one output layer. As demonstrate in Figure 2.1 the inputs and the interconnected weights are processed by weighted summation function to produce a sum and then used by an activation function. The result of the activation function is the output to the neurons.

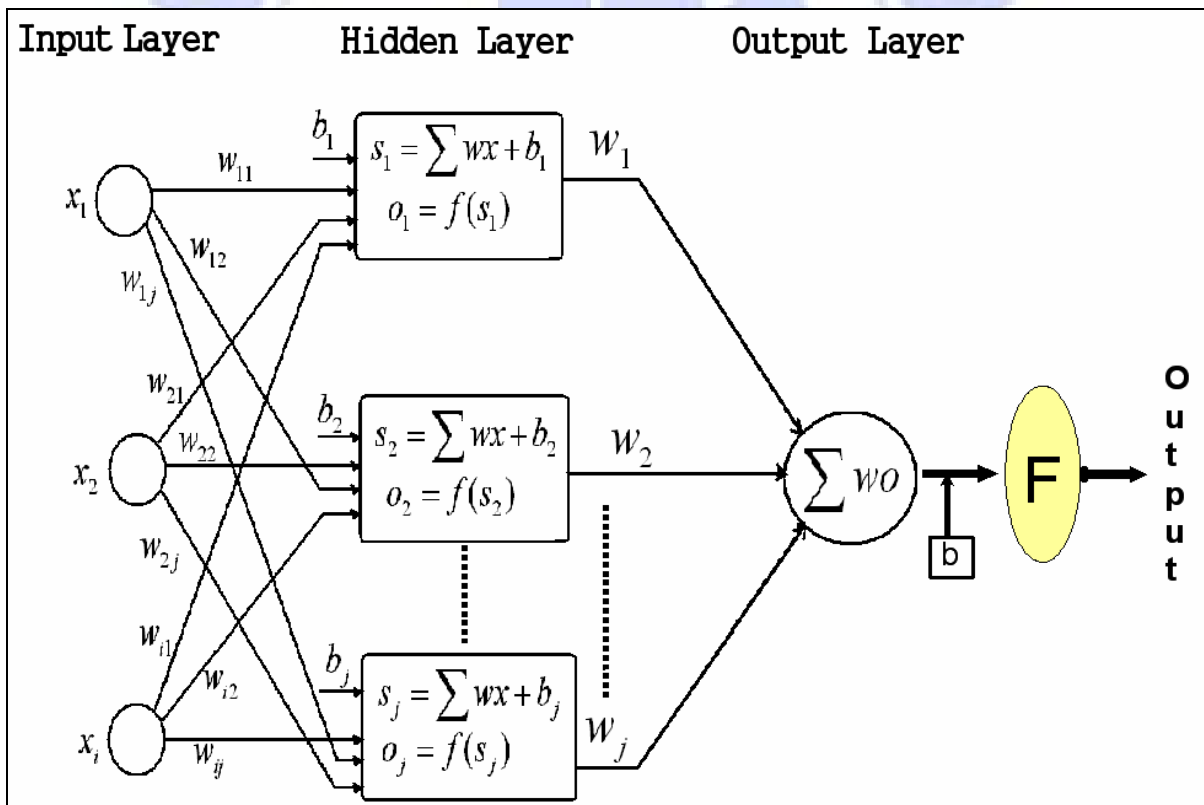


Figure 2.2: The Back propagation neural networks model with one output

Figure 2.2 illustrates the Back propagation neural network structure, where the boxes represent the hidden neurons. Each processing neuron first calculates the weighted sum of all interconnected signals from the input layer, plus a bias term as shown in equation

2.1. Then generates an output (s_j) through an activation function, where sigmoidal function (Eq. 2.2) expressed as activation function in this case. Although there are several types of activation functions, sigmoidal functions are the most commonly used.

$$s_j = \sum_{n=1}^N w_{n,j} x_j + b \quad (2.1)$$

$$f(s) = \frac{1}{1 + e^{-s}} \quad (2.2)$$

Next the outputs are calculated by finding the weighted sum of all interconnected signals from the hidden layer plus a bias term and then generates an output (y) through an activation function. In BPNN usually learns by making changes in its weights ($w_{i,j}, w_{j,k}$), when the mean square error (Eq. 2.3) is larger than acceptable limit.

$$E = \frac{1}{2} \sum_{k=1}^K (d_k - y_k)^2 \quad (2.3)$$

Where d_k is the desired output (actual output), and y_k is the BPNN output, k represent the number of output neuron, in this thesis one output neuron is constructed. In the training process, the input and output variables chosen for the network learning are presented to the model in a normalized form, and the weights between the hidden and output layers are adjusted first by using the expression below:

$$w_{j,k} = w_{j,k} + \Delta w_{j,k} \quad (2.4)$$

$$\Delta w_{j,k} = \eta \cdot f'(s_k) (y_k - o_k) o_k, \quad k = 1 \quad (2.5)$$

Where η represents a dumping or accelerating factor, Y_k comes from the input-output pairs of data (x, y) available for training the network, and O_k is the output obtained from Equation 2.2 applied to the neurons of the output layer in the m iteration. Subsequently as shown in BPNN algorithm (see figure 2.3), the weights between the input and hidden layers are changed (Eq. 2.6, 2.7). After presentation of the first input-output pair, the second pair is processed, and so on.

$$w_{i,j} = w_{i,j} + \Delta w_{i,j} \quad (2.6)$$

$$\Delta w_{i,j}^{(m)} = \eta \cdot f(s_j) \{ f(s_k) (y_k^{(m)} - o_k^{(m)}) w_{j,k}^{(m-1)} x_i^{(m)} \} \quad (2.7)$$

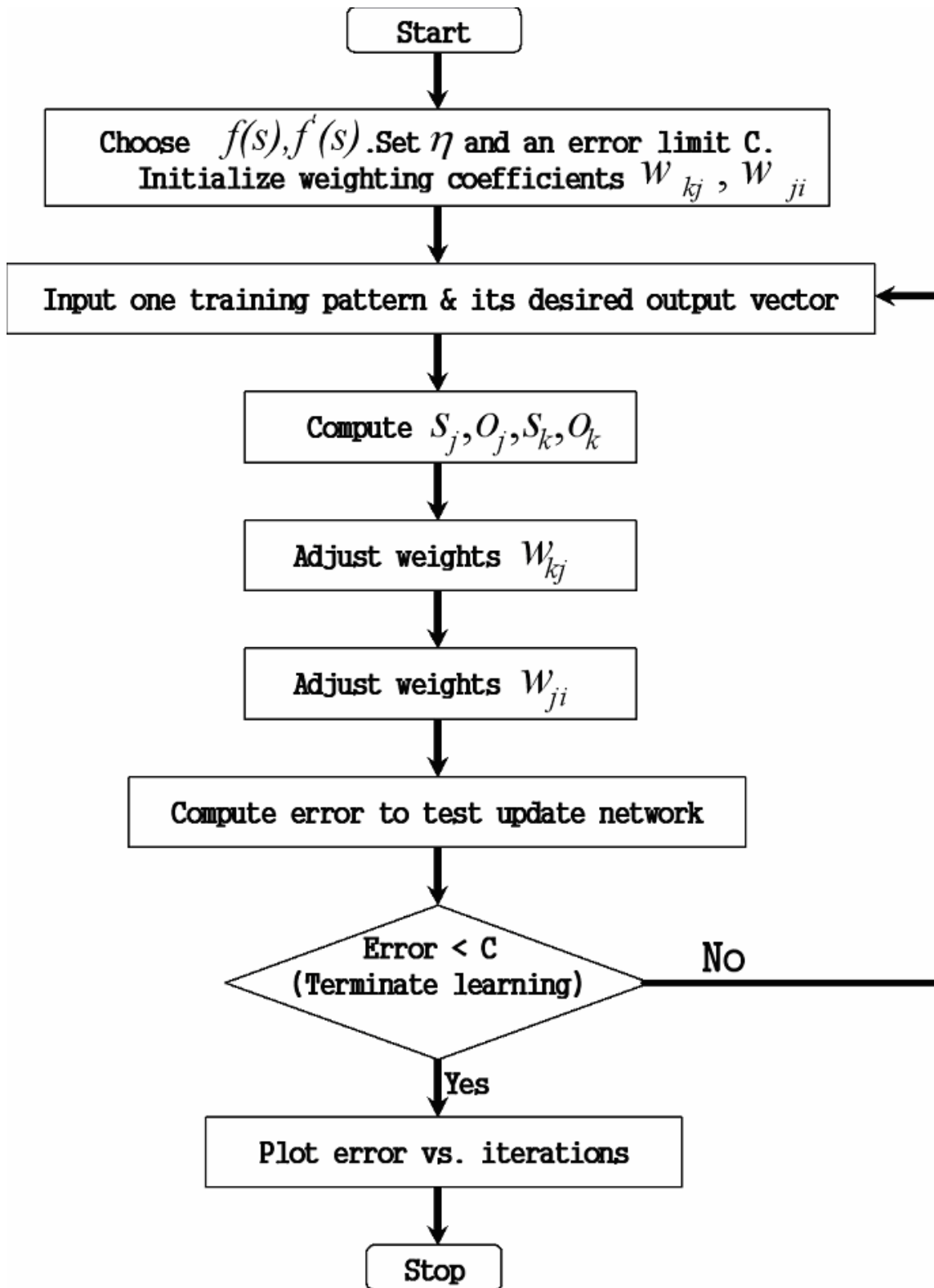


Figure 2.3: Major steps of BPNN algorithm [32]

CHAPTER 3

REACTIVE ION ETCH

One of crucial importance processes in semiconductor fabrication is plasma etching. Plasma etching first appeared in the late 1960s to interconnect the current and future generation of integrated circuit [34]. In this chapter, etch process in general and reactive ion etch process (RIE) concise is provided in four sections: the first section described the main etching types and characteristics. The second section clarifies reactive ion etch process (RIE). 2300 Exelan Flex is explained in the third section. Some relations between RIE factors and wafer defects are presented in the last section.

For fully understanding etch process, it is necessary to be familiar with the etch factors, such as etch rate, etch profile, etch bias, selectivity, uniformity, residues, and so on. These terminology and others explained in Appendix I.

3.1 Etch Process Overview

Etching process is performed immediately after photolithography, to remove undesired material from the wafer surface by either chemical etcher or physical mechanism. Usually photoresist masks or other materials are used on the top of surface to

protect specific regions of the wafer surface while permitting selective etching through opening the photo-resist layer [1, 7, and 35].

Two basic types of etch processes are used in semiconductor manufacturing: liquid (wet) chemicals, and gaseous (dry) species. In wet etch, liquid chemicals such as acids, bases, and solvents are chemically reacting with undesired surface material creating byproducts species which either dissolve or vaporize away. Table 3.1 compares the characteristics of the wet and dry etch process.

Table 3.1: Comparison between wet and dry etch characteristics

	Wet Etch	Dry Etch
Etch Bias	Unacceptable for $< 3\mu\text{m}$	Minimum
Etch Profile	Isotropic	Anisotropic to isotropic, controllable
Etch rate	High	Acceptable, controllable
Selectivity	High	Acceptable, controllable
Equipment cost	Low	High
Throughput	High	Acceptable, controllable
Chemical usage	High	Low

On the other hand, dry etches is the primary etching method in advanced wafer fabrication. The goal of the dry etching process is to form significant features such as gates and interconnect lines, and contact holes. Contact holes will be filled with metal to connect the source and drain, and to connect different metal layers. The significant features formed in chips by reproducing the image of a mask on wafer surface with a high degree of integrity.

In general, dry etching mechanism is divided into the four basic phenomenological categories as shown in Figure 3.1: sputtering, chemical etching, ion-enhanced energetic or RIE and ion-enhanced inhibitor processes [1, 7, and 35].

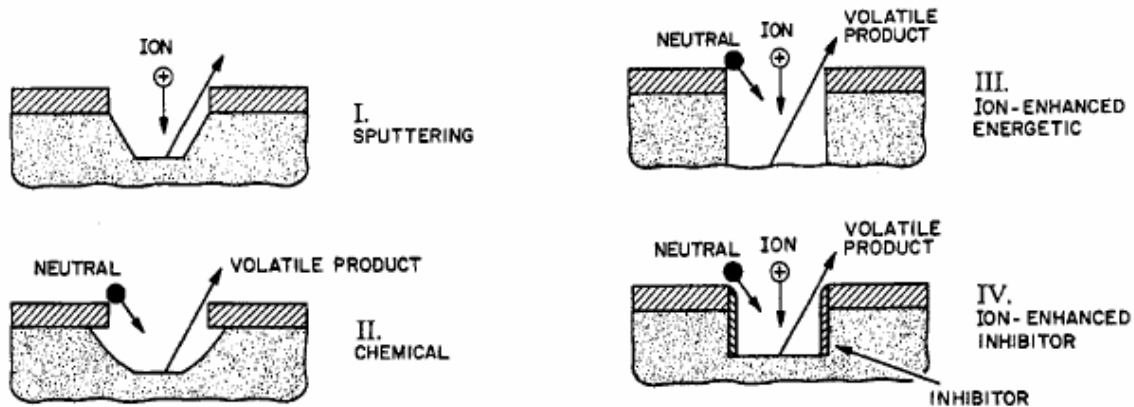


Figure 3.1: The four phenomenological etching mechanisms: I sputtering, II Chemical etching, III Ion- enhanced energetic etching IV Ion enhanced inhibitor etching.

The four phenomenological dry etching mechanisms : (I) Sputtering is the nonselective surface atoms removal, where the non-reactive feedstock gas ions are induced by plasma to strike the target surface. Chemical Etching (II) is an isotropic and selective surface atoms removal, where plasma induced gaseous etchant atoms or molecules (free radicals) which chemically react with the surface layer and forming gaseous volatile etch products. (III)RIE -Ion-Enhanced Energetic - is the highly anisotropic etching of surface layers due to gaseous etchant and energetic ions. (IV) Ion Enhanced Inhibitor Etching where in this mechanism plasma supplies chemical etchant, and inhibitor precursor molecules. The inhibitor molecules adsorb or deposit on the substrate to form a protective layer or polymer film.

3.2 Reactive Ion Etch

Reactive ion etch is suitable technique for removing material from the wafer surface, and is widely used in VLSI manufacturing because the resist mask pattern can be accurately transferred to the film. Furthermore, RIE control the etching profile and under layer selectivity.

A typical RIE system consists of a cylindrical vacuum chamber with a wafer platter situated in the bottom portion of the chamber (figure 3.2). The wafer platter is electrically isolated from the rest of the chamber, which is usually grounded. Gas flow is introduced through small inlets in the top of the chamber and is evacuated out to the vacuum pump system through the bottom of the chamber. The types and amount of used gas is determined by the etch process.

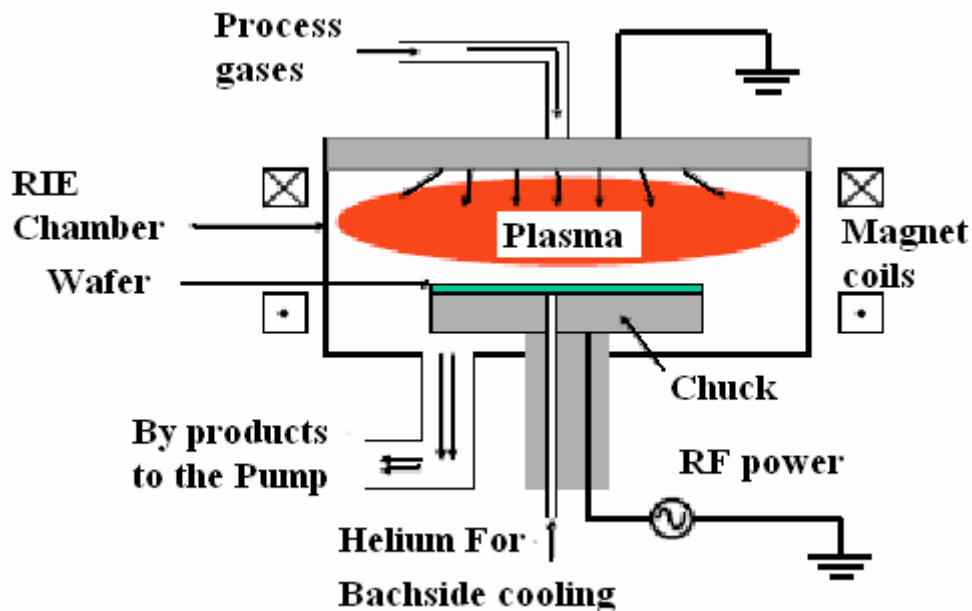


Figure3.2: Reactive Ion Etch Tool

RIE procedure starts by vacuuming chamber until the pressure arrives to the required limit. After that the etchant gas will be introduced to the vacuum chamber at the same time RF powers are used to increase the electrons energy. Some of the etchant molecules dissociate from the impact of the collisions with electrons forming as in Eq. (3.1), which generate free radicals. These free radicals diffuse across the boundary layer, to reach the wafer surface, and are adsorbed on the surface (3.2). With the help of ion bombardment (3.4), these free radicals react with the surface atoms or molecules very quickly and form gaseous byproducts (3.3). The volatile byproducts desorbed from the surface (3.5), diffuse across the boundary layer, get into the convection flow, and are pumped out from the chamber. It is easy to conclude that RIE contains two kinds of etch mechanism:

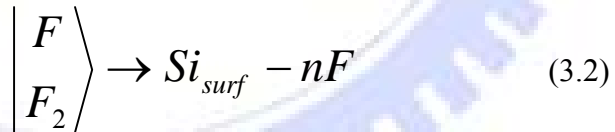
- I- Chemical etching caused by suitable reactive chemicals
- II- Physical etching caused by ion bombardment.

The following equations and Figure 3.3 clarify the RIE mechanism

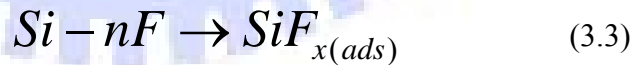
Etchant Formation



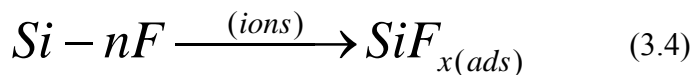
Adsorption on Substrate



Chemical Reaction



Ion Assisted reaction



Product Desorption



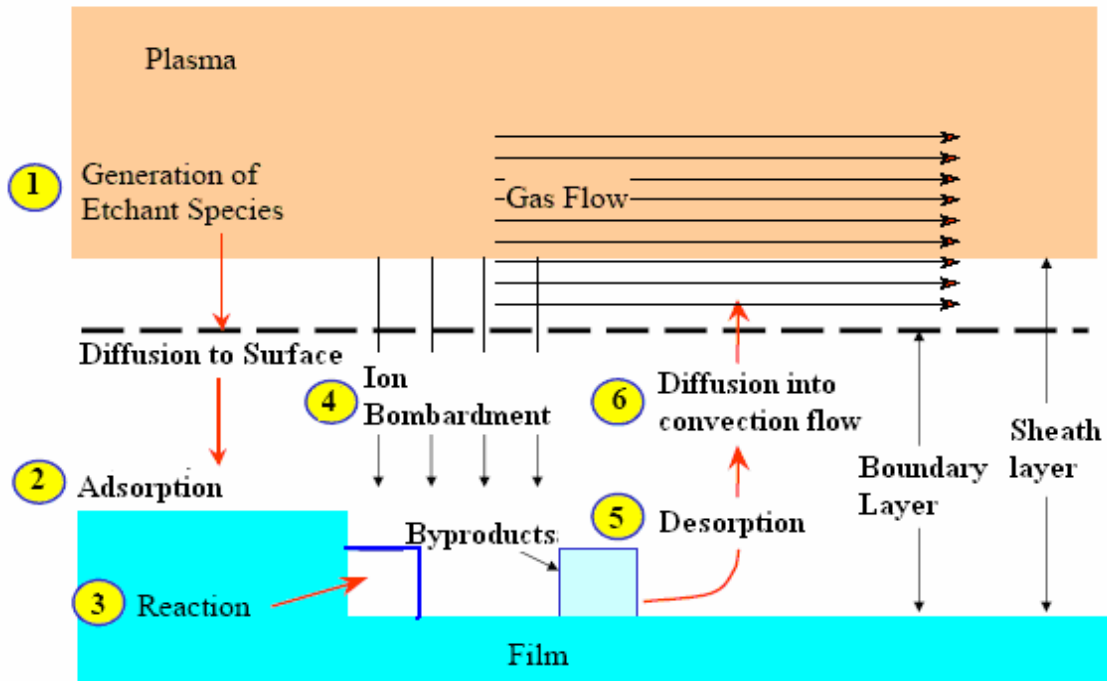


Figure 3.3: RIE Mechanism

3.2.1 Plasma in RIE

Plasma can be generally described as an ionized gas composed of ions, free electrons, and a variety of neutral species. It contains approximately equal concentrations of positively charged particles (positive ions) and negatively charged particles (electrons and negative ions). While this description encompasses a wide range of plasma types and conditions, specific class is typically used in semiconductor processing called a "low pressure glow discharge", this type of plasma is weakly ionized (most of the gas molecules are neutral), low pressure (1 mTorr to 1 Torr), and nonequilibrium electrons contain most of the energy and the ions remain near room temperature. The advantage of this kind of plasma is surface chemical reactions with plasma can take place under nonequilibrium conditions and at low temperature. Plasma effectively controls the main

etching characteristics, such as the etching rate, anisotropy, selectivity and uniformity provides.

It is well known that the plasma process is affected by chemical and physical features, several features of plasma are described in this section such as: thermal velocities of the free electrons and ions inside the plasma. These thermal velocities are described by the following equations,

$$v_e = \left(\frac{eT_e}{m} \right)^{\frac{1}{2}} \quad (3.6)$$

$$v_i = \left(\frac{eT_i}{M} \right)^{\frac{1}{2}} \quad (3.7)$$

Where, e is the electron charge, and the ionized particle charge, T_e and T_i are the electron and ion temperatures, and m and M are the masses of the electron and ion, respectively. For typical semiconductor processing plasmas, T_e is between 1 and 10V (here, temperature and voltage can be considered equivalent through the relation $V = \frac{K_B T}{q}$ therefore, $300\text{K} \equiv 0.026\text{V}$), while T_i is near room temperature. The ion mass is also much larger than the electron mass. For these two reasons $v_e \gg v_i$, and during the time immediately after the plasma is ignited, the electrons are lost to the chamber walls much more rapidly than the ions. This leaves the bulk plasma with a net positive charge, which sets up an electric field from the plasma to the walls. The high electric field region near the walls is called the sheath.

The sheath thickness is one of the plasma features. This thickness is the order of 1 mm and is the only separated charge region. All other areas can be considered quasi-neutral over a length scale larger than $\sim 15 \mu\text{m}$. The potential across the sheath relative a floating surface (the floating potential) is typically 10-30 V and accelerates ions that enter the sheath towards the floating surface. Since the ion temperature in the bulk plasma is low ($\approx 0.026\text{eV}$), the energy of the ions bombarding the chamber walls is on the order of several T_e . If the wafers to be processed are placed on one of the walls, these ions will strike the wafers with high velocity, and at nearly-normal incidence. This ionic bombardment is the basis for the anisotropic etching.

3.2.2 Cooling System in RIE

In reactive ion etch process, large heat is generated by electrons strikes and heavy ion bombardment, where the high temperature can cause photoresist reticulation. Consequently, Temperature control is needed to keep wafer health and protect wafer photoresist. Where low pressure is not good to transfer the heat a cooling system is required. Thus, Helium backside cooling is commonly used as shown in figure 3.4., either clamp ring or electrostatic chuck (E-chuck) is hold wafer. So in this cooling process, Helium is pressurized at the wafer back so heat transfer from wafer to water cooled chuck.

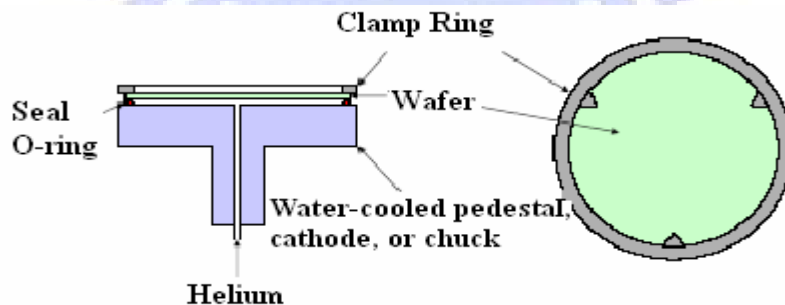


Figure 3.4: Helium backside cooling system

3.3 Case Study: Oxide RIE in PSC

This thesis studied one of reactive etching process in Power Ship Corp., where 2300 Exelan Flex (figure 3.5) used to etch the dioxide silicon films. This equipment is a complete package with an integral power supply, RIE chamber, and internal cooling system.



2300 Exelan Flex

Figure 3.5: 2300 Exelan Flex, etching equipment in many VLSI factories.

This advanced Reactive Ion Etching equipment made up of many different sections (figure 3.6). Some of these sections are maintenance and controller sections. The main electronics monitor the status and manipulate the values of controlled variables such as: Pressure, Temperature, gas mass flow, voltage, current, and RF power.

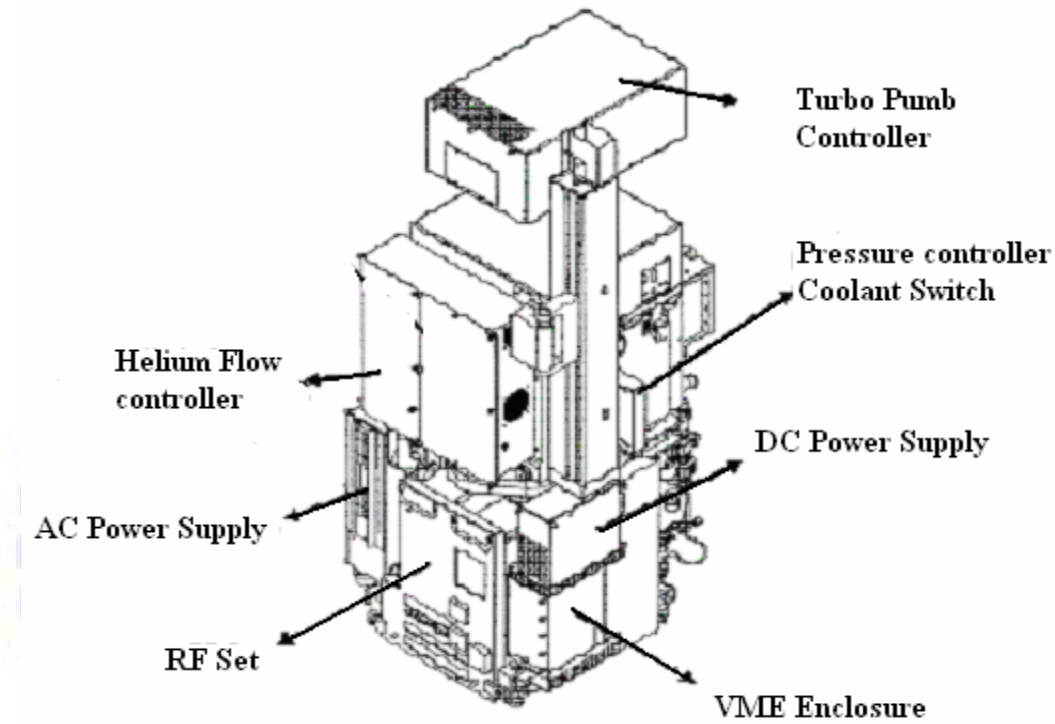


Figure 3.6: Sketch of 2300 Exelan Flex equipment includes some controller

The other main section in 2300 Exelan Flex is RIE chamber (figure 3.7). The main etching chamber configured inside the vacuum chamber for optimal efficiency, where these two chambers separated by quartz confinement rings, these rings effort pressure controller for the main chamber. This chamber as typical RIE (sec 3.2) consists two parallel plates, Esc, RF power supply, and pumping system.

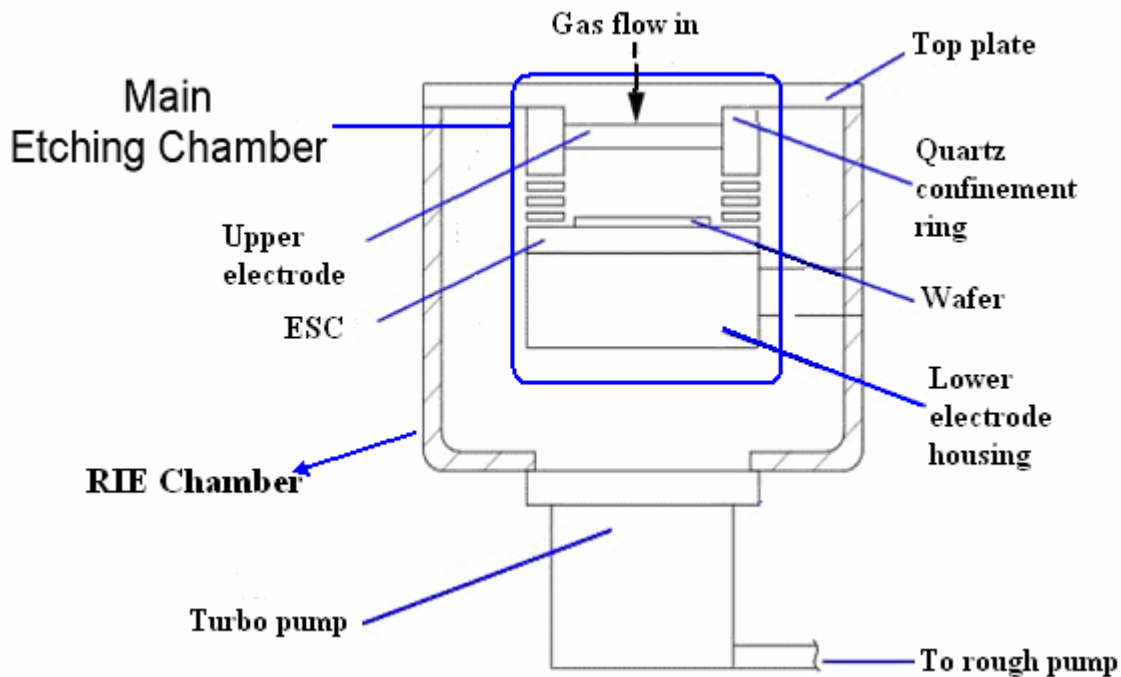


Figure 3.7: Sketch of the main etching chamber inside RIE chamber

The purpose of oxide reactive ion etch is to create the trenches, which are filled by metal to connect wafer layers. To achieve this purpose three main oxide etching steps applied during oxide etch process, which contains eleven steps. Before the main etching process, good plasma environment must be prepared by stabilization steps (stable step, strike plasma step, and ramp up plasma step).

The first step in RIE recipe starts by opening high vacuum pump automatically followed by closing rough vacuum pump, thus ultra-high vacuum (1mTorr) is achieved inside RIE chamber, after that the opened area between the vacuum chamber and main etch chamber is minimized by quartz confinement rings, at this instant the fluorine gas mixture is introduced to the main chamber as the end of the first step.

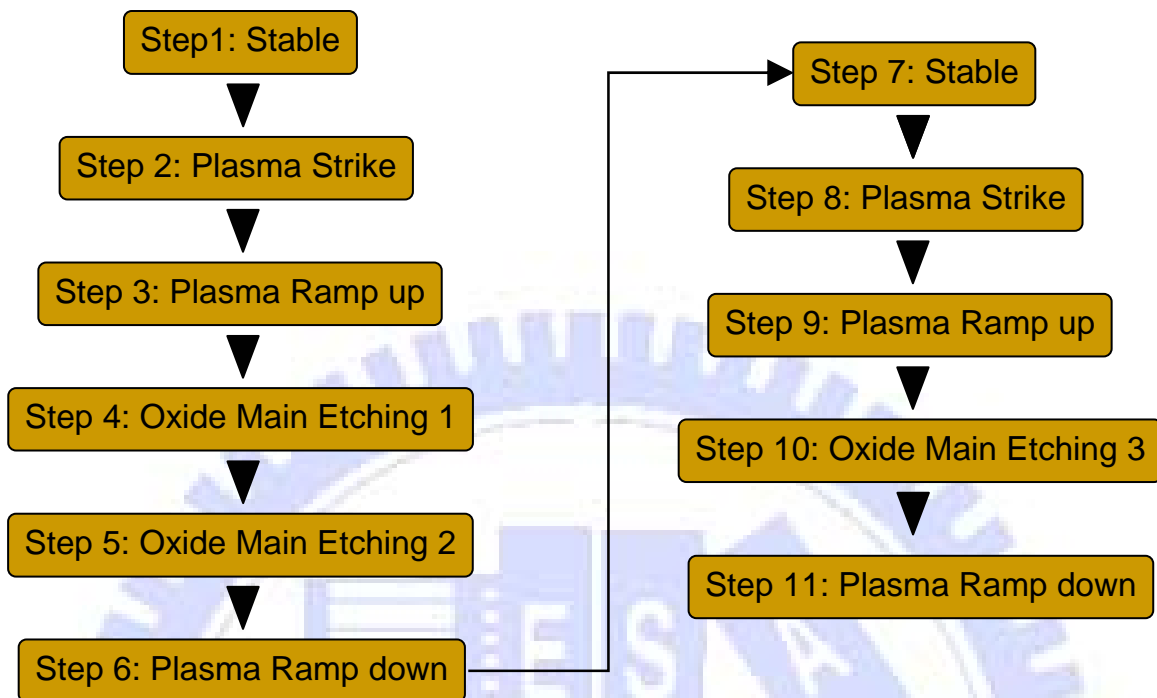
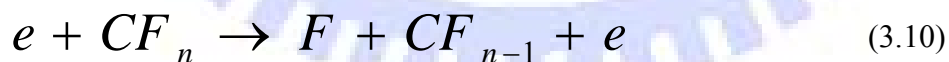


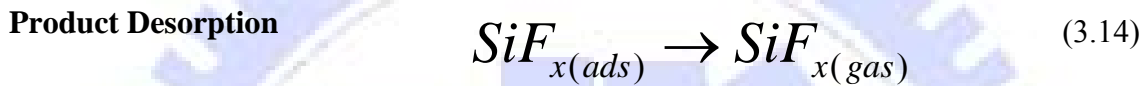
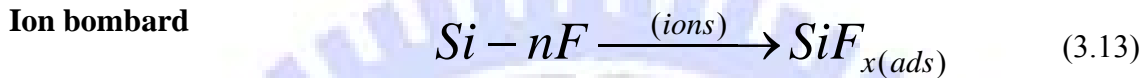
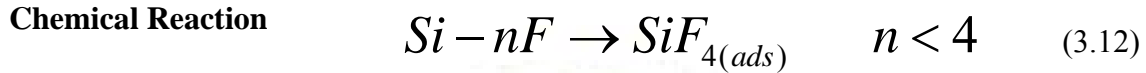
Figure 3.8: Process recipe for oxide film etching in RIE

The second step objective is to strike the plasma. Plasma is initiated in the system through applying RF power to the wafer platter. This power is typically applied at a few hundred watts with twenty seven and two megahertz, these frequencies create an oscillating electric field that ionizes few gas molecules by stripping them of electrons, creating plasma as shown in equation 3.10. In step three the values of the RF power will be increased to enhance the plasma amount until plasma reaches the required density.



After plasma enhanced, the main etching process is occurred by physical and chemical mechanisms. More physical than chemical mechanisms occurred in silicon oxide etching processes. In addition, free fluorine radicals are the main etchant for this etching process. When etching oxide, oxygen byproduct can react with C to free more

fluorine (equation 3.10). The reactions between the etchant atoms and oxide silicon wafer surface shown in the following equations:



As shown in figure 3.8 there are three main etching steps: the first oxide etch step is outlined the wafer surface shape from the rounded mask. The second main etch step provides the pattern etch. The third main oxide etch occurs in deepest depth to prepare the contact areas between two layers, thus this etching need higher plasma density than the previous etching steps to achieve its purpose. So the stabilization steps repeated with same procedure but different RF power and gas flow values preparing new plasma.

3.4 RIE Factors

For reactive ion etching systems (case study) mainly forty different signals were collected from 2300 Exelan Flex equipment in PSC, twenty two signals are carefully chosen from the whole signals, the chosen signals are directly impact the wafer status. Figure 3.9 clarifies the main twenty one factors except the time factor. For more understanding table 3.2 provides more elaborations about RIE factors.

Table 3.2: RIE factors and its clarification

#	Factor	Factor explanation
1	Bias Voltage	Direct-current voltage at electrode. The value of the bias voltage depends on the size of the electrode and on the gas pressure.
2	ESC Clamp Voltage	Electrostatic chuck. (a mechanism for holding wafers using electrostatic attraction.)
3	ESC Current1	The Current pass in the first selected point on ESC
4	ESC Current2	The Current pass in the second selected point on ESC
5	ESC Temperature	Electrostatic chuck. Temperature (a mechanism for holding wafers using electrostatic attraction.)
6	Fluorine Pressure	The mixed Gases pressure inside the pipe
7	Forward Power 27 MHz	Applied 2 MHz for dissociation
8	Forward Power 2MHz	Applied 2 MHz for bombard
9	Gas 1	C_1F_8 mass flow rate
10	Gas 10	Xe mass flow rate
11	Gas 11	C_4F_6 mass flow rate
12	Gas 4	Ar mass flow rate
13	Gas 7	O_2 mass flow rate
14	He Flow Inner	Mass flow rate for Helium gas inside the Inner tube of cooling system
15	He Flow Outer	Mass flow rate for Helium gas inside the outer tube of cooling system
16	He Pressure Inner	Helium gas Pressure inside the Inner tube of cooling system
17	He Pressure Outer	Helium gas Pressure inside the outer tube of cooling system
18	Pressure	The pressure value inside the RIE chamber
19	Process Time	The time from the initial to the end process
20	Reflect Power 27 MHz	The reflected 27 MHz which has not been used at the process
21	Reflect Power 2 MHz	The reflected 2 MHz which has not been used at the
22	Top Plate Temperature	The temperature on the upper plate

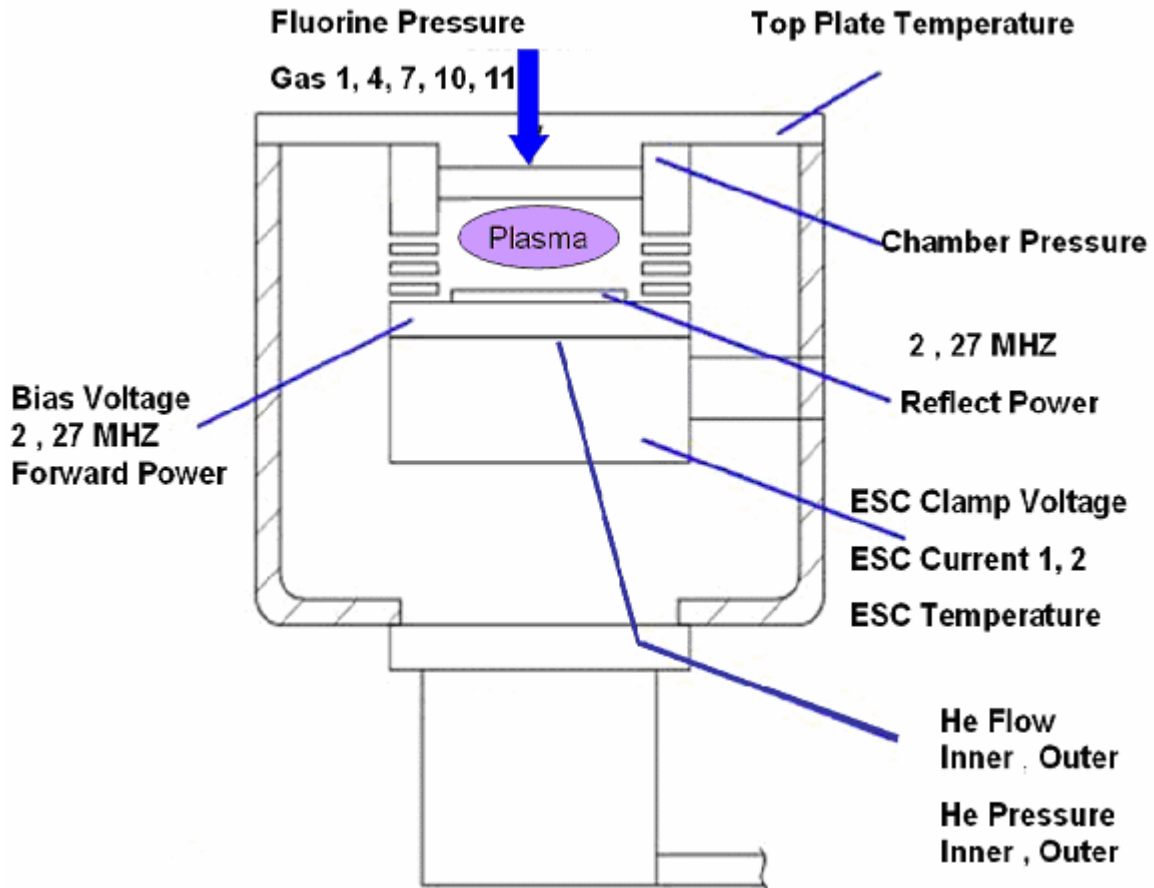


Figure 3.9: Main factors of oxide RIE.

3.4.1 RF Power

The energy of the ions bombarding the substrate can be increased by employing an additional capacitive source of RF. Thus the etch rate increase linearly with the RF power supply. RF power present the most important knob that controls etch rate. When etch rate is out of specifications the first response the engineers do is checking RF system. four signals related to RF power presented in 2300 Exelan Flex table 3.2, 2 MHZ power supply, 27 MHZ power supply, 2MHZ reflected power and 27MHZ reflected power. In addition to RF, DC bias is highly correlated to etch rate as shown in figure 3.10.

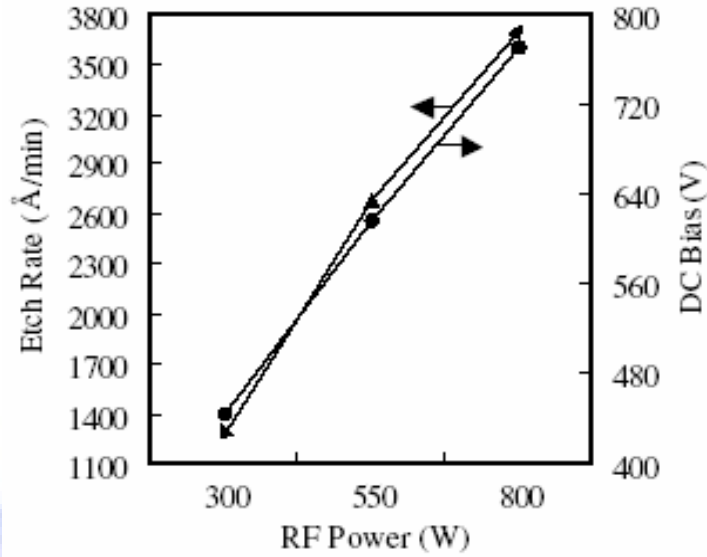


Figure 3.10: Etch rate and DC bias as a function of the RF power.

3.4.2 Pressure

Gas pressure in RIE is typically maintained in a range between a few millitorr and a few hundred millitorr by adjusting gas flow rates or adjusting an exhaust orifice. Normally, as pressure is decreased below about 100 mTorr, the potential across the discharge characteristically increases. At very low pressure, physical etching mechanisms tend to dominate (figure 3.11) , because of high ion energy, low reactant density, and long mean free paths.

According to the kinetic theory of molecular gases, the mean free path of a gas molecule at constant temperature is inversely proportional with the pressure. So when the pressure decreases the mean free paths of the species increases, and the energetic particles in the plasma can easily transfer their kinetic energy to the atoms at the oxide silicon film surface.

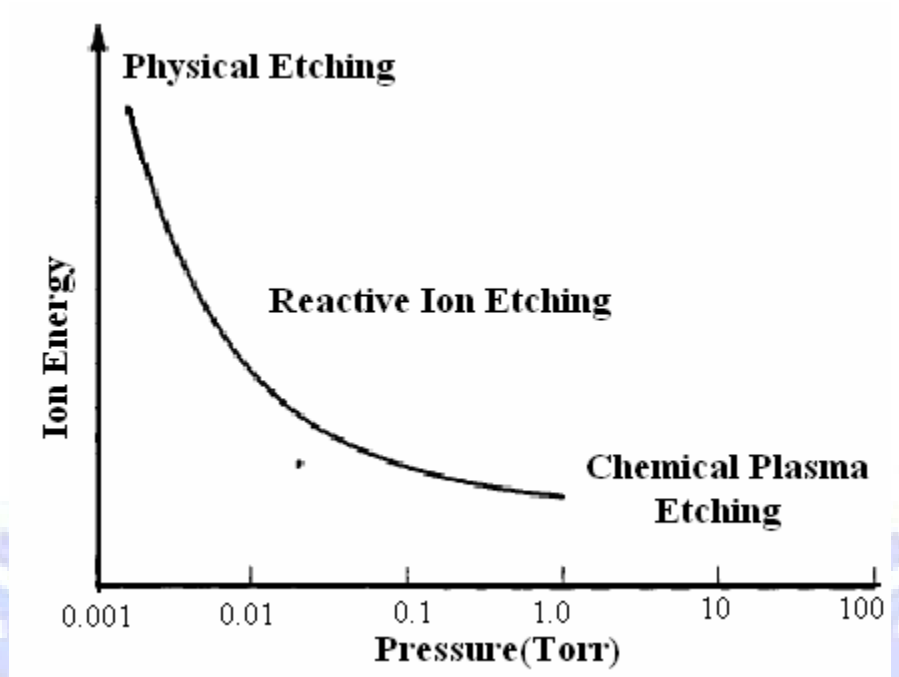
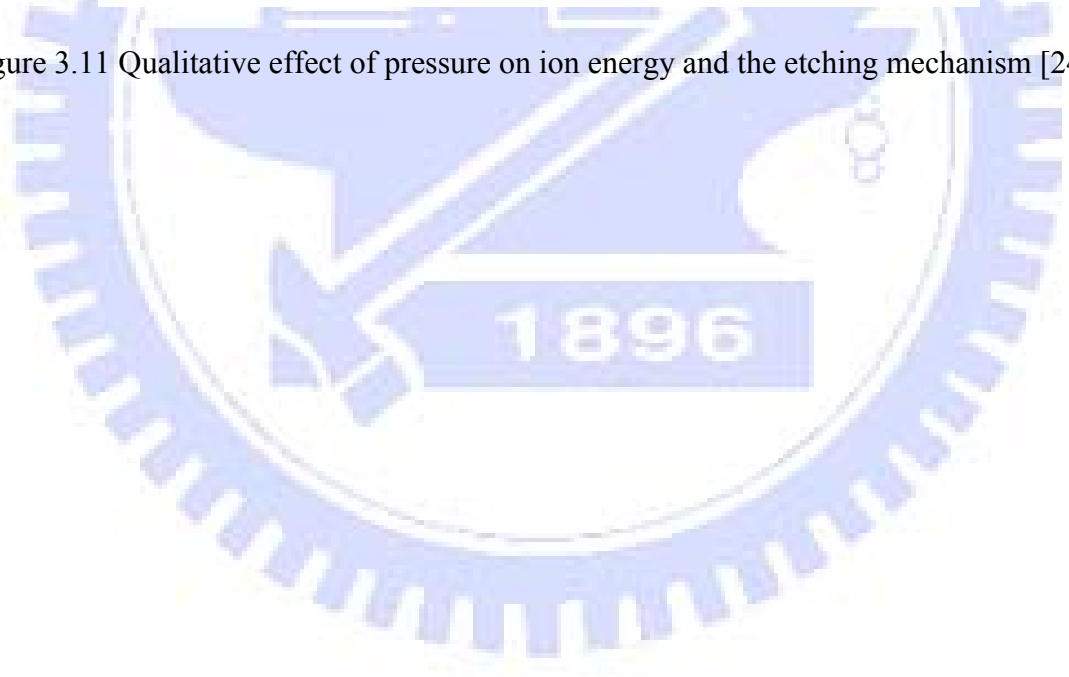


Figure 3.11 Qualitative effect of pressure on ion energy and the etching mechanism [24]



CHAPTER 4

PRINCIPAL COMPONENT ANALYSIS

Principal component analysis (PCA) is an important analysis technique in multivariate statistics, it was first suggested in 1901 by Pearson [36], and formally developed by Hotelling [37]. The main idea of principal component analysis (PCA) is to represent number of correlated variables into a smaller number of uncorrelated variables called principal components. The first principal component accounts for as much of the variability in the data as possible, the second PC is the linear combination with the second largest variance and orthogonal to the first PC, and so on. There are as many PCs as the number of the original variables. For many datasets, the first several PCs explain most of the variance, so that the rest can be disregarded with minimal loss of information. The objectives of using PCA are to reduce the dimensionality of a data set, and to identify new underlying variables that are now orthogonal.

To enhance performance of prediction model in this study, PCA is suggested to represent the RIE factors, since simple neural networks with few nodes and connections tend to have better generalization capability. In this chapter, PCA technique

automatically extracts three principle components (PC) from all RIE factors (twenty two factors). Table 4.1 shows the RIE factors and its abbreviation.

Table 4.1 RIE factors and its abbreviation.

x_1	Bias Voltage	x_{12}	Gas 4
x_2	ESC Clamp Voltage	x_{13}	Gas 7
x_3	ESC Current1	x_{14}	He Flow Inner
x_4	ESC Current2	x_{15}	He Flow Outer
x_5	ESC Temperature	x_{16}	He Pressure Inner
x_6	Foreline Pressure	x_{17}	He Pressure Outer
x_7	Forward Power 27MHz	x_{18}	Pressure
x_8	Forward Power 2MHz	x_{19}	Process Time
x_9	Gas 1	x_{20}	Reflect Power 27MHz
x_{10}	Gas 10	x_{21}	Reflect Power 2MHz
x_{11}	Gas 11	x_{22}	Top Plate Temperature

It is important to treat each step separately in PCA, because each etching step has different inherent physical/chemical characteristics, and by considering the overall process characteristics and the objective of model simplicity, it was decided that utilizing one PCA for each of the eleven steps might yield a better solution than utilizing a single PCA for the entire process. In this thesis, principal component analysis was utilized for 90 training wafers, the principle components are found by computing the sample covariance* matrix and selecting its eigenvectors (loading vectors) for the k biggest eigenvalues as shown in figure 4.1.

* Covariance matrix $Cov(X)$ is a good choice to capture the dependence between variables of the matrix (X).

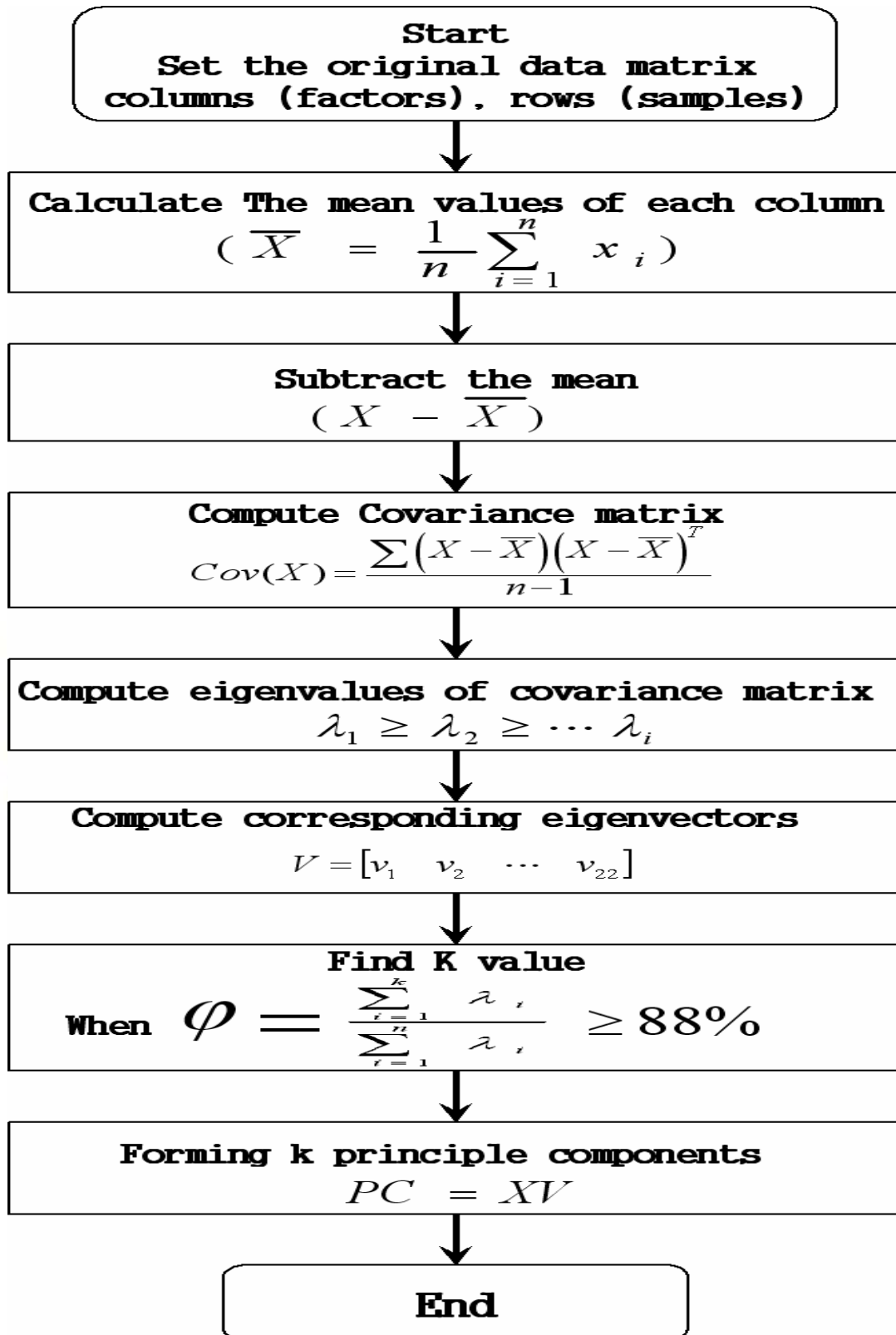


Figure 4.1 Flow chart of principle component analysis (PCA) algorithm.

The covariance matrix $Cov(X)$ can be obtained by:

$$Cov(X) = \frac{(X - \bar{X})^T (X - \bar{X})}{n-1} \quad (4.1)$$

Where $X = [X_1 \ X_2 \ \dots \ X_{22}]$

is data matrix with n samples (rows) and 22 variables (columns), as well as each column represents one of RIE factors.

X_i represents vector i of data matrix

$(X - \bar{X})$ stands for subtract the mean value of each column from the corresponding column .

To find the eigenvalues and eigenvector of the covariance matrix, $Cov(X)$ represented by using singular value decomposition (SVD) as shown in the following equation:

$$Cov(X) = V \Lambda V^T \quad (4.2)$$

where $V = [v_1 \ v_2 \ \dots \ v_{22}]$

is an 22 by 22 unitary matrix of corresponding eigenvector

$$\Lambda = \begin{bmatrix} \lambda_1 & 0 & 0 & \dots & \dots \\ 0 & \lambda_2 & 0 & \dots & \dots \\ \vdots & & & & \vdots \\ 0 & 0 & \dots & \dots & \lambda_{22} \end{bmatrix}$$

the matrix Λ is 22 by 22 diagonal matrix of the corresponding eigenvalues (λ) on the diagonal and zeros off the diagonal, where $\lambda_1 \geq \lambda_2 \geq \dots \geq \lambda_{22}$ Table 4.2 shows the

eigenvalues for the eleven steps. Figure 4.2 shows the decrease in eigenvalues λ for each of etching step.

The variance of the i th PC is equal to the i th largest eigenvalue of the covariance matrix [38]. Because of this important property, the φ percentage (equation 4.3) is used as a guide in choosing an appropriate number of PC. The goal is to choose as small a value of k as possible while achieving a reasonably high percentage of PC variance. The φ values shown in table 4.3 give the cumulative proportion of the variance explained by the first k PCs, φ is larger than 88% when k equals three, thus three principle components are selected to characterise the twenty two RIE factors by using equation 4.4:

$$\varphi = \frac{\sum_{i=1}^k \lambda_i}{\sum_{i=1}^{22} \lambda_i} \quad (4.3)$$

$$PC = XV \quad (4.4)$$

Score equations ($T = XV$) is tend to identify the three principle components according to RIE factors. Score equations for each etch step is shown in Appendix II

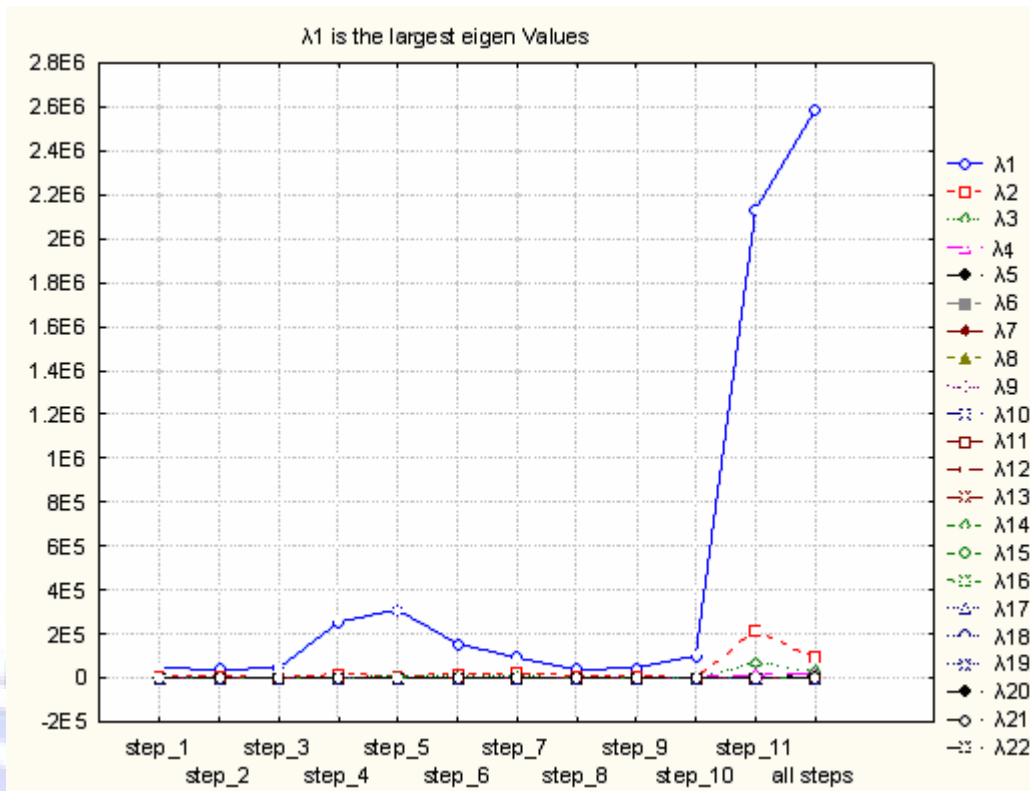


Figure 4.2 Eigenvalues of the covariance matrix for RIE steps

Table 4.2 Eigenvalues of the covariance matrix for the RIE steps

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Step 10	Step 11
λ_{11}	48062.88	36463.5	45458.36	258757	310931.3	153335.9	96148.68	35666.89	43176.34	100821.5	2131219
λ_{12}	5047.313	8460.603	1981.925	13296.19	9879.858	12382.57	24076.99	9486.769	11175.77	3397.501	218662.3
λ_{13}	4381.343	2626.144	1572.036	2618.225	5813.466	5264.326	7770.408	3599.852	2689.245	1740.743	70542.74
λ_{14}	1743.932	2061.922	291.4701	2131.54	2453.279	3592.547	4010.08	3189.305	2398.51	241.2595	12932.93
λ_{15}	1328.845	876.0741	254.9945	955.3121	2345.141	1401.493	878.7746	1120.373	543.464	42.70433	4206.568
λ_{16}	1068.565	362.7985	198.915	770.6035	900.8051	377.2102	767.8016	525.5306	333.1243	24.55001	821.7999
λ_{17}	821.8268	304.0512	141.3106	264.9442	446.6567	313.139	396.9665	427.7351	214.0356	18.60568	362.9603
λ_{18}	560.5313	167.2168	92.63	260.4574	327.0133	181.5321	381.368	263.6799	169.3079	14.72632	321.3758
λ_{19}	501.7918	98.20662	81.66254	163.6374	255.7505	130.2501	236.7117	176.6344	128.2413	10.51319	223.7872
λ_{10}	388.9135	45.65539	36.8668	114.6787	150.6866	100.5717	149.2104	101.5296	98.06473	2.247188	28.03805
λ_{11}	310.4795	27.72156	27.53846	91.64595	139.447	85.97648	128.7427	94.67434	93.35378	1.517441	15.83644
λ_{12}	169.808	26.101	23.75819	72.62664	89.08971	76.16953	92.36265	71.80552	66.58398	0.965449	5.551829
λ_{13}	132.3441	16.10837	16.38294	52.43167	72.30287	44.80435	53.08281	27.50362	35.66227	0.808228	4.853813
λ_{14}	105.7057	4.112478	4.391223	14.05196	26.66527	22.13461	33.40167	19.12257	24.0238	0.098895	3.921343
λ_{15}	90.63773	3.247694	3.078894	9.411111	21.32502	17.41058	18.10036	12.79197	16.67304	0.027842	2.088574
λ_{16}	87.22377	2.971524	1.260329	2.860032	16.84798	16.72032	12.99528	8.140811	12.2359	0.023689	1.044506
λ_{17}	64.17076	2.351149	0.99188	1.752256	15.92226	10.40523	11.23824	6.651263	8.293824	0.002104	0.901431
λ_{18}	54.30509	1.079706	0.759306	1.326145	14.19353	6.335162	9.424229	6.478083	2.342275	0.000377	0.518034
λ_{19}	31.58907	0.297334	0.314738	0.730349	1.446266	3.775627	8.691249	2.384221	1.362077	0.000127	0.227624
λ_{20}	21.94994	0.20754	0.233974	0.551161	0.712777	3.41368	3.363049	1.826439	1.094912	0.000103	0.203242
λ_{21}	16.6412	0.203164	0.151927	0.32573	0.480537	0.595521	0.481324	0.236635	0.287105	2.50E-05	0.049632
λ_{22}	1.827028	0.106573	0.07559	0.197485	0.415602	0.348956	0.291158	0.157483	0.162379	2.16E-05	0.020371

Table 4.3 PC variance percentages for RIE steps

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Step 10	Step 11
$\Phi 1$	73.951285	70.73331	90.57415	92.55188	93.1203	86.45089	71.12159	65.07361	70.56321	94.83032	87.36808
$\Phi 2$	81.717263	87.14551	94.52307	97.30764	96.0792	93.4322	88.93144	82.38205	88.8278	98.02593	96.33201
$\Phi 3$	88.458556	92.23981	97.65529	98.24413	97.82027	96.40023	94.67924	88.94991	93.22284	99.66323	99.22387
$\Phi 4$	91.141833	96.2396	98.23604	99.00653	98.555	98.42571	97.64552	94.76874	97.14273	99.89015	99.75404
$\Phi 5$	93.186442	97.93904	98.74411	99.34823	99.25734	99.21587	98.29555	96.81284	98.03091	99.93032	99.92649
$\Phi 6$	94.830574	98.64282	99.14044	99.62386	99.52712	99.42854	98.8635	97.77167	98.57534	99.95341	99.96018
$\Phi 7$	96.095067	99.23263	99.42199	99.71862	99.66089	99.60509	99.15713	98.55206	98.92514	99.97091	99.97506
$\Phi 8$	96.957521	99.557	99.60655	99.81178	99.75883	99.70744	99.43923	99.03314	99.20184	99.98476	99.98823
$\Phi 9$	97.729596	99.7475	99.76926	99.87031	99.83542	99.78087	99.61433	99.35541	99.41142	99.99465	99.99741
$\Phi 10$	98.327992	99.83607	99.84272	99.91133	99.88055	99.83758	99.7247	99.54065	99.57169	99.99676	99.99856
$\Phi 11$	98.805707	99.88984	99.89759	99.94411	99.92231	99.88605	99.81993	99.71338	99.72426	99.99819	99.99921
$\Phi 12$	99.06698	99.94048	99.94493	99.97009	99.94899	99.92899	99.88825	99.84438	99.83308	99.9991	99.99943
$\Phi 13$	99.270609	99.97172	99.97757	99.98884	99.97065	99.95425	99.92752	99.89456	99.89136	99.99986	99.99963
$\Phi 14$	99.433252	99.9797	99.98632	99.99386	99.97863	99.96673	99.95223	99.92945	99.93062	99.99995	99.99979
$\Phi 15$	99.57271	99.986	99.99245	99.99723	99.98502	99.97655	99.96562	99.95279	99.95787	99.99998	99.99988
$\Phi 16$	99.706916	99.99176	99.99496	99.99825	99.99007	99.98598	99.97523	99.96764	99.97787	100	99.99992
$\Phi 17$	99.805651	99.99633	99.99694	99.99888	99.99483	99.99184	99.98354	99.97978	99.99142	100	99.99996
$\Phi 18$	99.889207	99.99842	99.99845	99.99935	99.99909	99.99541	99.99051	99.9916	99.99525	100	99.99998
$\Phi 19$	99.937811	99.999	99.99908	99.99962	99.99952	99.99754	99.99694	99.99595	99.99748	100	99.99999
$\Phi 20$	99.971584	99.9994	99.99955	99.99981	99.99973	99.99947	99.99943	99.99928	99.99927	100	100
$\Phi 21$	99.997189	99.99979	99.99985	99.99993	99.99988	99.9998	99.99979	99.99971	99.99974	100	100
$\Phi 22$	100	100	100	100	100	100	100	100	100	100	100

CHAPTER 5

PREDICTION MODELS FOR RIE

The computing, telecommunications, aerospace, automotive and consumer electronics industries all rely heavily on integrated circuits (ICs). Next-generation IC manufacturing equipment will require dramatic improvements in cost, quality, throughput, and flexibility. Reducing manufacturing cost involves increasing chip yield, reducing cycle time, maintaining consistent product quality, improving equipment reliability, and maintaining stringent process control. Since IC fabrication consists of hundreds of steps, maintaining product quality requires the control of thousands of variables. Process steps are performed in sequence, and yield loss may occur at every step. However, analyzing wafer defects is the regular method for evaluation semiconductor technologies. Wafer defects carry a lot of wafer status information which can be analyzed in order to characterize the quality of processes and products. If the prediction model accurately predicts the wafer status, the repeated etching failure rate should be prevented, process yield should be greatly enhanced, inspection cost should be reduced and profit should be increased.

The experimental process of this study is as depicted in figure 5.1, and four models are included: offline back-propagation neural network (BPNN), offline principle

component analysis BPNN (PCABPNN), online BPNN and online PCABPNN. These models have the potential to reduce the overall cost of ownership of semiconductor equipment by increasing the wafer yield and throughput of product wafers, and not depend upon monitor wafers or expensive metrology rather it will enable inexpensive real-time wafer-to-wafer control applications in RIE. The capability of the four prediction models to predict the wafer status correctly is discussed in this chapter.

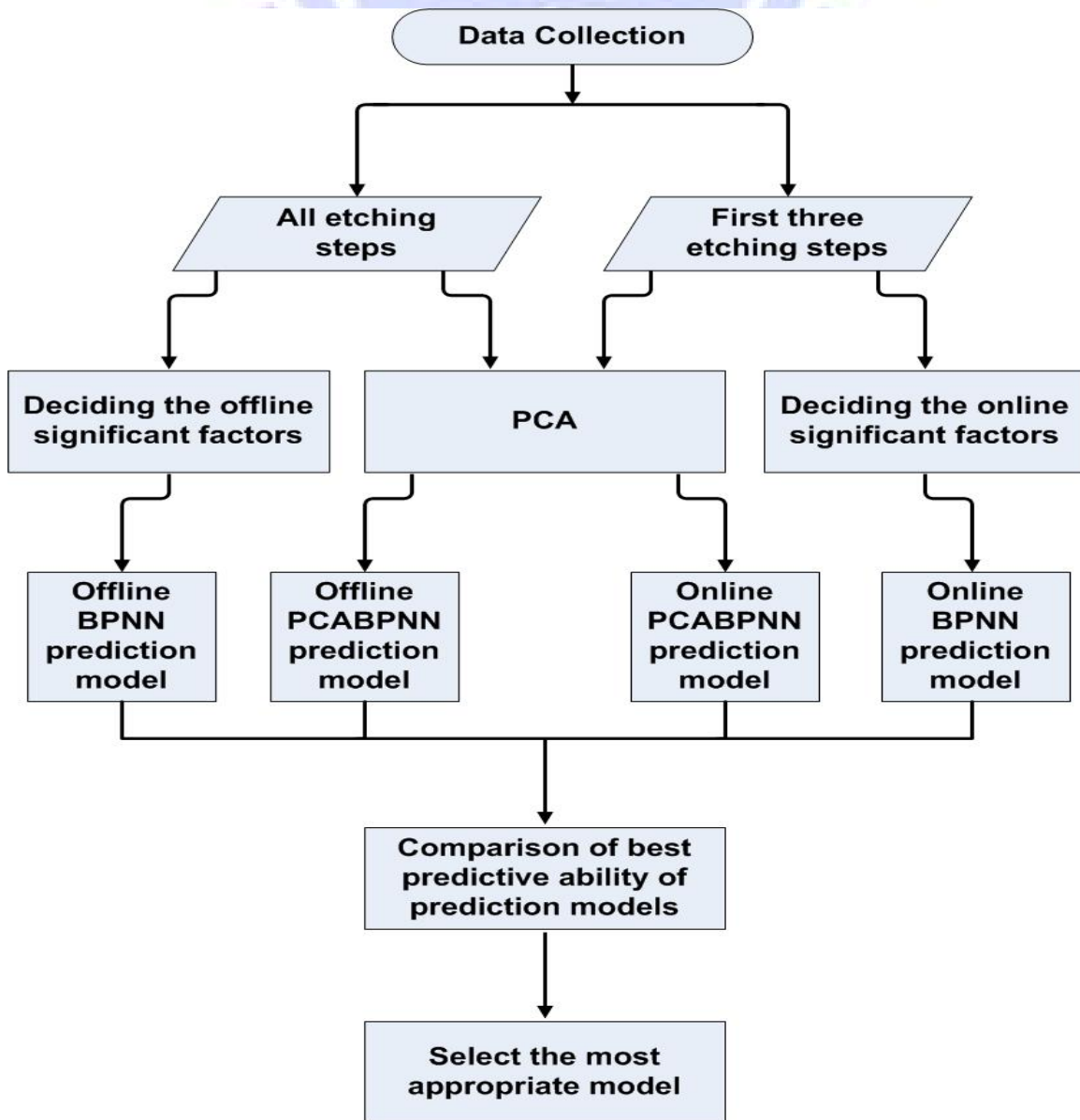


Figure 5.1: Flow chart of the experiment.

5.1 Data Collection from RIE.

The most important step in semiconductor process modelling is the collection of data. It is essential to gather a sufficient sample of representative data; or else it is impossible to train a neural network or any other type of model. In this study, the parameters data of 2300 Exelan Flex machine is collected by engineers in Powerchip Semiconductor Corp (PSC) factory based on their experience. These parameters include chamber temperature and pressure, forward and reflected RF power, DC bias and gas flow rates (table 3.2).

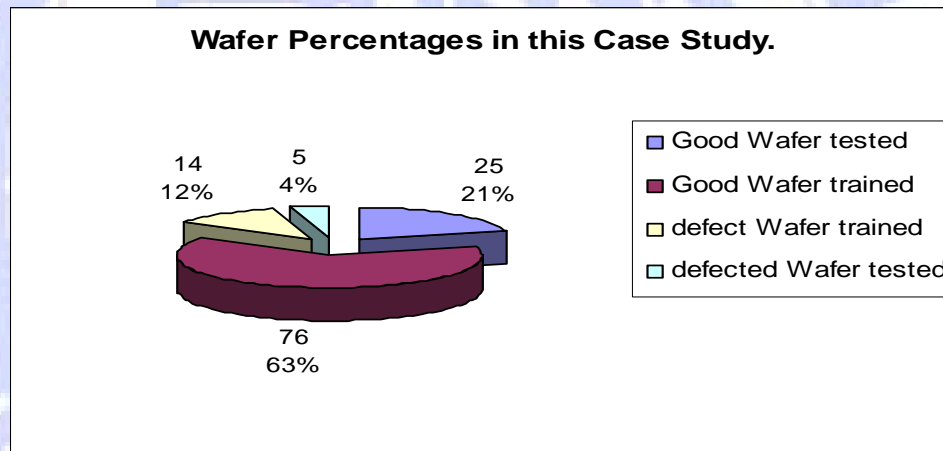


Figure 5.2 Percentage of the training and testing wafers in this case study.

Figure 5.2 presents the training, and testing percentage of one hundred twenty wafers which collected from 2300 Exelan Flex machine, and the percentage of training wafers to testing wafers which is three to one, where fourteen wafers (12%) from the ninety training wafers (75%) stand for unopened etch defected wafers, and five wafers (4%) from the thirty tested wafers (25%) stand for defected wafers (unopened etch).

5.2 Data Preparation.

This section explain the details of the preparation data performed in this study, data preparation techniques are used to obtain good prediction results. Figure 5.3 reveals the variation of the data point number/ process time for each step, for example in step five the number of data points is between 10- 140 with 60 data points as an average of step five . Because of this dissimilarity, it is hard to decide the BPNN inputs. Therefore three different data preparation techniques are suggested and prepared such as: raw data, sampling data and statistical summary data.

- Raw data preparation: one hundred eighty four data points is the minimum number of data points from the collected data, thus the first one hundred eighty data points are suggested as raw data inputs for offline prediction models. And twenty data points are suggested as raw data inputs for online prediction models.

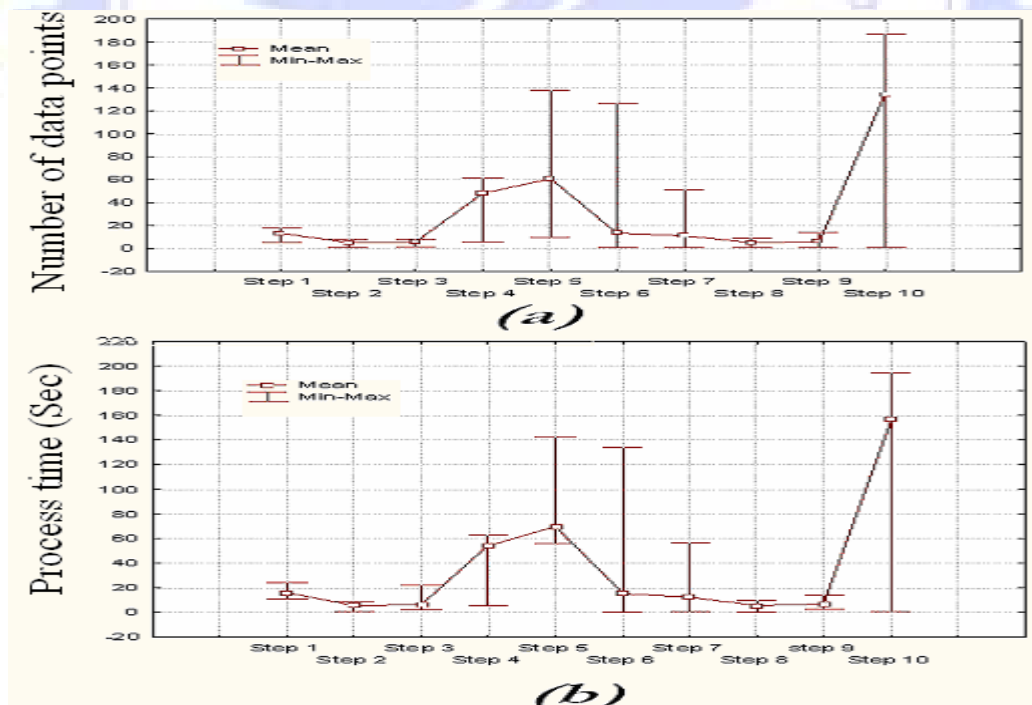


Figure 5.3: (a) Box plots of data input number versus each step of given data (b) Box plots of Process Time versus each step of given data

- Sampling: non symmetric sampling is the second suggested preparation technique, which has ability to cover all etching steps (figure 3.8), at the same time focusing on the main three etching steps (step 4, step 5 and step 10). Table 5.1 shows the number of captured samples in each step, where two samples captured from stabilization steps (step 1, 2, 3, 7, 8, and 9) and two from plasma ramp down steps (step 6 and 11), more than half of the captured samples are captured from the main etching steps (step 4, 5, and 10), as a result thirty four captured samples cover all etching steps. These thirty four captured samples used as inputs for offline prediction models.

Table 5.1: Number of suggested sampling for each step in the sampling technique

Step Number	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Step 10	Step 11
Number of sample	2	2	2	6	6	2	2	2	2	6	2

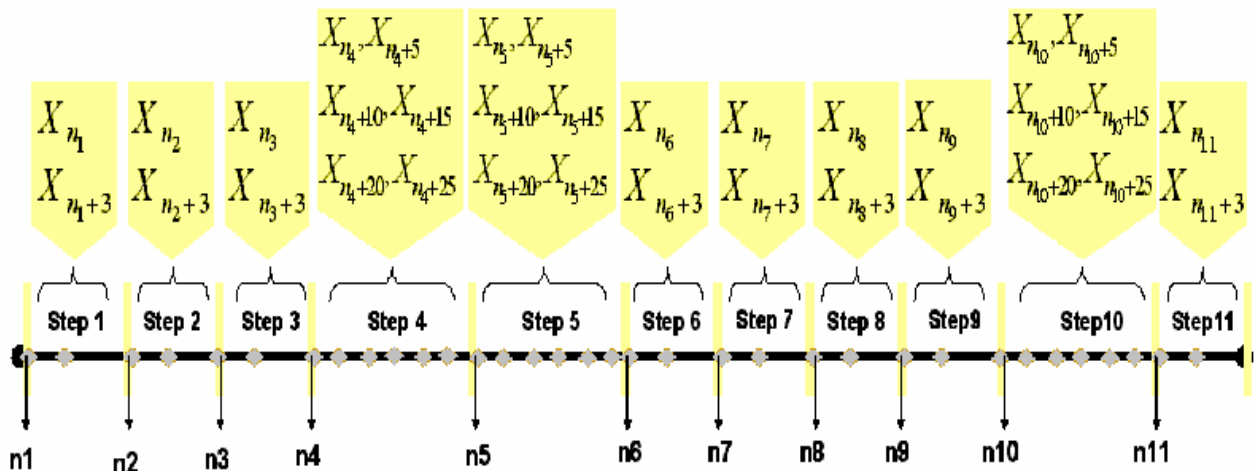


Figure 5.4: The position of captured samples.

Figure 5.4 illustrates the position of captured samples, where the first data point of each step is captured, and the suggested sampling rate for the main etching steps is five and three for other steps. The first seven captured samples are suggested as the input of

the online prediction models, these samples includes the first data point of each stabilization steps, the third point after the beginning of the first three stabilization steps and the end point of the third step (which is the first data point of forth step).

- Statistical summary preparation: the last suggested preparation technique, and depends on mean and standard deviation values. The following equations show the calculation of the two statistical summary values.

$$\bar{X} = \frac{1}{N} \sum_{i=1}^N x_i \quad (5.1)$$

$$\sigma = \sqrt{\frac{1}{N-1} \sum_{i=1}^N (x_i - \bar{X})^2} \quad (5.2)$$

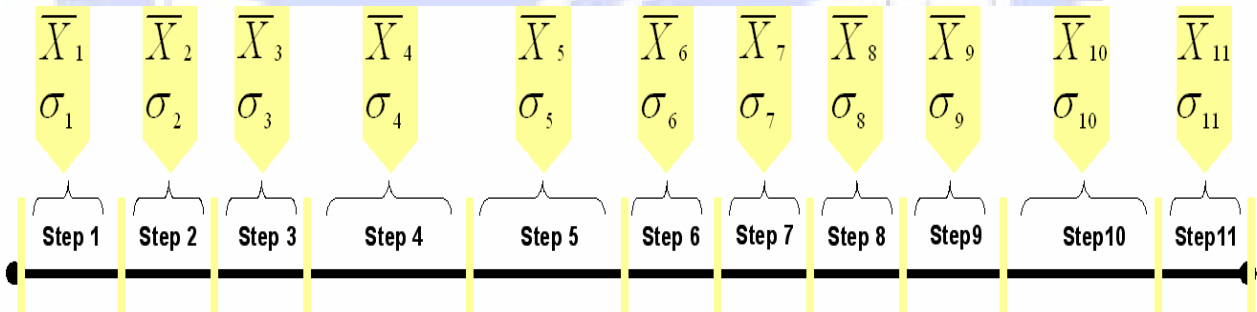


Figure 5.5: Statistical summary data preparation technique

Because of many samples have no data for the sixth step, this step became out of interest. This means there is ten steps will be statistical summarized and applied in offline prediction models.

5.3 Architecture of prediction models

As stated before, many researchers have been adopted BPNN to solve the problem of categorization, prediction and examination the manufacturing process, because the advantages of BPNN such as: easy and fast to comprehend, high accuracy and fast recalling speed. This study combines back propagation neural network (BPNN) and principle component analysis (PCA) to construct the four prediction models as shown in table 5.2. Offline prediction models concern about all etching process steps to predict the wafer status after the end of etching process. In other hand, online prediction models concern about the first three stabilization steps. Online prediction models are capable to reduce the defected wafers more than offline prediction models, due to the abnormalities of the etching process can be predicted as soon as possible and before the end of the first main etching step (step 4).

Table 5.2: The methods used in each prediction model.

	PCA	BPNN	Notes
Offline BPNN		※	Concern about all etching steps
Online BPNN		※	Concern about the first three steps
Offline PCABPNN	※	※	Concern about all etching steps
Online PCABPNN	※	※	Concern about the first three steps

5.3.1 BPNN

BPNN in this study consists three layers of neurons: the input layer, hidden layer, and output layer. The input layer receives external information such as RIE processing factors or principle components. From the output layer, predictions are produced, the prediction values expressed as a binary values to represent the wafer status, since the network output is between zero to one, the zone that is smaller than the Min value is set to zero and the zone that is greater than the Max value is set to one. If the network output value is equal to one that means the wafer status is good, and otherwise is bad (defected wafer). When the network output value is between Min and Max values, then the network fails to predict the wafer status. The defined value range must be established to determine whether the output value is close to the target value.

The BPNN also incorporates hidden layers of neurons, these neurons do not interact with the outside world, but assist in performing nonlinear feature extraction on the data provided by the input and output layers. The number of hidden layers was set to one in this application. With a description of the BPNN network structure, training matters have to be settled.

5.3.2 Training

As previously mentioned the overall objective in training is to minimize the discrepancy between real data and the output of the network. During training, the network is trained to associate outputs with input patterns, this principle is referred to as

supervised learning. The training is continued until the training reached the maximum number of epochs or training neural network has MSE less than 1×10^{-6} . The maximum number of epochs used during training the networks is set to 10000 epochs.

After training, the prediction performance of the prediction models is estimated with two test sets. The first test set is formed by comparing the prediction error of new data set, data of twenty five good wafers and five defected wafer stand for testing data set. Two type of error obtained in the first test: type I prediction error occurred when good wafer is predicted as bad wafer, and type II prediction error occurred when defected wafer is predicted as good wafer.

The second test set depends on the recognition rate/ rejection rate. The recognition rate is the percentage of test samples recognized correctly and the output value is located outside the zone values (Min and Max values). The rejection rate is the percentage of input samples that could not be assigned to any particular class; because the output value is located somewhere within the zone values. The Min and Max values are determined for every prediction models after testing the training wafers, where Min value is the highest output value for defected wafer, and Max value indicates the lowest value for good wafer.

5.4 Significant Factors

Process engineers in anonymous companies select the RIE factors which is critically affect the quality of etched wafer based on their experience. These factors are gas flow, pressure, and radio frequency, bias voltage. If inappropriate factors are selected as BPNN inputs, the result will be much less than desired. Conversely, the prediction result will be much more than significant if RIE significant factors are selected as BPNN inputs. In PSC company, some RIE factors is well controlled such as the etchant gases, so deciding the significant factors which is practically affect the wafer status in RIE is very important to obtain a good result. To decide the significant factors which affect the wafer status in RIE, new technique is establishes in this application. This new technique depends on comparing the network testing result of each process factor.

5.4.1 Significant Factors for Offline BPNN

In offline BPNN prediction model, selecting RIE significant factors is necessary to achieve accurate prediction of wafer status. Significant factors of RIE process have a major impact with the wafer status. The following three tables (table 5.3, 5.4 and 5.5) show the network testing result of each factor of RIE factors by using three different data preparation techniques, where the BPNN testing results reveals the significant factor. Mean square error for training and testing wafers in BPNN are shown in the first two columns. In addition, there are twenty five good wafers and five defected wafers are tested in BPNN. The fifth column in the following tables show the number of type I error, which express the number of good wafers which predicted as bad wafer by using

BPNN. The sixth column represents the number of defected wafers which predicted as good wafer (type II error), and the last column summarizes the total error predictions.

Table 5.3 illustrates the network testing result of the first 180 data points of each factor. The result shows that there are two significant factors: He flow outer and Bias voltage. These two factors have zero error prediction, which means these two factors strongly affect the wafer status.

Table 5.4 illustrates the network testing result of the 34 captured samples of each factor. These results reveal three factors from RIE factors as significant factors: Bias voltage, He flow inner and He flow outer. In table 5.5, Bias voltage, He flow inner, He flow outer, Pressure, and Reflect Power 2MHz have zero error prediction, these five factors considered as significant factors for offline BPNN model. It is obvious that statistical summary preparation technique has the best result for deciding the RIE significant factors.

Table 5.3: Significant factors of RIE process decided after applying the first 180 data points of each factor in BPNN

	Factor	Training MSE	Testing					
			MSE	Total ok	Total NG	Prediction Error		
						Type I	Type II	Total
1	Bias Voltage	9.27E-07	4.41E-07	25	5	0	0	0
2	ESC Clamp Voltage	6.69E-06	0.163705	25	5	3	4	7
3	ESC Current1	3.17E-06	0.100155	25	5	0	3	3
4	ESC Current2	2.89E-06	0.100123	25	5	0	3	3
5	ESC Temperature	1.32E-05	0.168854	25	5	1	4	5
6	Foreline Pressure	9.98E-05	0.159136	25	5	1	5	6
7	Forward Power 27 MHz	8.75E-07	0.143639	25	5	3	3	6
8	Forward Power 2MHz	6.48E-05	0.099038	25	5	0	3	3
9	Gas 1	2.31E-06	0.204308	25	5	1	5	6
10	Gas 10	0.111322	0.366876	25	5	16	2	18
11	Gas 11	0.11456	0.11782	25	5	0	4	4
12	Gas 4	0.10851	0.314963	25	5	23	1	24
13	Gas 7	0.019724	0.082154	25	5	0	3	3
14	He Flow Inner	3.25E-06	0.014994	25	5	0	1	1
15	He Flow Outer	1.6E-06	5.7E-07	25	5	0	0	0
16	He Pressure Inner	1.53E-06	0.099997	25	5	0	3	3
17	He Pressure Outer	1.91E-06	0.092254	25	5	0	3	3
18	Pressure	4.37E-06	0.032177	25	5	0	1	1
19	Process Time	7.67E-06	0.184015	25	5	1	5	6
20	Reflect Power 27 MHz	1.94E-06	0.168614	25	5	1	5	6
21	Reflect Power 2 MHz	9.72E-06	0.033455	25	5	0	1	1
22	Top Plate Temperature	6.48E-06	0.097917	25	5	0	3	3

Table 5.4: Significant factors of RIE process decided after applying the 34 captured samples of each factor in BPNN.

	Factor	Training MSE	Testing					
			MSE	Total ok	Total NG	Prediction Error		
						Type I	Type II	Total
1	Bias Voltage	4.11E-06	1.10E-05	25	5	0	0	0
2	ESC Clamp Voltage	1.11E-01	0.178685	25	5	2	3	5
3	ESC Current1	1.26E-05	0.100866	25	5	0	3	3
4	ESC Current2	1.81E-05	0.100813	25	5	0	3	3
5	ESC Temperature	2.22E-04	0.160666	25	5	1	4	5
6	Foreline Pressure	4.14E-04	0.146022	25	5	0	4	4
7	Forward Power 27 MHz	9.99E-05	0.11473	25	5	3	1	4
8	Forward Power 2MHz	3.16E-04	0.10403	25	5	0	3	3
9	Gas 1	3.15E-05	0.217221	25	5	3	4	7
10	Gas 10	0.11376	0.326518	25	5	10	2	12
11	Gas 11	0.141822	0.377467	25	5	20	2	22
12	Gas 4	0.147345	0.366534	25	5	10	4	14
13	Gas 7	0.020965	0.139837	25	5	0	4	4
14	He Flow Inner	6.8E-06	1.1E-06	25	5	0	0	0
15	He Flow Outer	7.1E-06	9E-06	25	5	0	0	0
16	He Pressure Inner	4.56E-04	0.1033	25	5	0	3	3
17	He Pressure Outer	2.03E-05	0.12282	25	5	2	2	4
18	Pressure	2.42E-05	0.039188	25	5	0	2	2
19	Process Time	1.14E-04	0.188832	25	5	2	4	6
20	Reflect Power 27 MHz	1.86E-05	0.148802	25	5	0	5	5
21	Reflect Power 2 MHz	1.11E-04	0.022695	25	5	0	1	1
22	Top Plate Temperature	1.66E-05	0.099002	25	5	0	3	3

Table 5.5: Significant factors of RIE process decided after applying the twenty statistical summary values of each factor in BPNN.

	Factor	Training MSE	Testing					
			MSE	Total ok	Total NG	Prediction Error		
						Type I	Type II	Total
1	Bias Voltage	3.75E-05	3.88E-04	25	5	0	0	0
2	ESC Clamp Voltage	2.81E-02	0.197152	25	5	6	5	11
3	ESC Current1	2.28E-05	0.099976	25	5	0	3	3
4	ESC Current2	4.30E-05	0.101419	25	5	0	3	3
5	ESC Temperature	7.72E-04	0.304	25	5	5	4	9
6	Foreline Pressure	5.14E-03	0.181269	25	5	4	2	6
7	Forward Power 27 MHz	6.80E-04	0.301056	25	5	8	3	11
8	Forward Power 2MHz	1.97E-02	0.298276	25	5	7	3	10
9	Gas 1	1.10E-03	0.097395	25	5	1	2	3
10	Gas 10	0.000611	0.114359	25	5	1	2	3
11	Gas 11	0.026534	0.195254	25	5	3	3	6
12	Gas 4	0.040709	0.275859	25	5	5	3	8
13	Gas 7	0.000976	0.065575	25	5	0	2	2
14	He Flow Inner	7.1E-06	7.1E-06	25	5	0	0	0
15	He Flow Outer	8.1E-06	5.4E-06	25	5	0	0	0
16	He Pressure Inner	4.79E-04	0.107106	25	5	1	2	3
17	He Pressure Outer	3.50E-04	0.076432	25	5	2	1	3
18	Pressure	8.28E-05	1.55E-03	25	5	0	0	0
19	Process Time	6.34E-04	0.130328	25	5	0	4	4
20	Reflect Power 27 MHz	7.38E-04	0.241023	25	5	5	2	7
21	Reflect Power 2 MHz	9.93E-05	8.48E-03	25	5	0	0	0
22	Top Plate Temperature	2.52E-05	0.103611	25	5	0	3	3

5.4.2 Significant Factors for Online BPNN

The success of prediction model relies heavily on the model inputs. Therefore, deciding the RIE significant factors of the first three stabilization steps is important to achieve accurate prediction of wafer status in online BPNN prediction model. To decide the RIE significant factors, the three data preparation techniques are applied in online BPNN for each single factor, consequently the significant factors will be easily observed. The observed RIE significant factors for the stabilization steps are highlighted in the following three tables (table 5.6, 5.7 and 5.8). The following three tables represent the network testing result of applying the three preparations technique for each single factor in BPNN.

Table 5.6 illustrates the accuracy of predicting the wafer status by training and testing the first twenty data points of each single factor of RIE factors in BPNN. These twenty data points cover the etching process mainly before the fourth step. This trial set up to find the significant factors which affect the wafer status. He flow outer is the only factor with zero error prediction, thus He flow outer is considered as significant factor.

Table 5.6: Significant factors of the first three stabilization steps decided after applying the first 20 data points in BPNN

	Factor	Training MSE	Testing					
			MSE	Total ok	Total NG	Prediction Error		
						Type I	Type II	Total
1	Bias Voltage	7.92E-04	0.029784	25	5	1	1	2
2	ESC Clamp Voltage	1.32E-01	0.216189	25	5	5	4	9
3	ESC Current1	1.58E-04	0.080873	25	5	1	1	2
4	ESC Current2	1.44E-04	0.07315	25	5	1	1	2
5	ESC Temperature	2.79E-02	0.173156	25	5	3	2	5
6	Foreline Pressure	1.74E-02	0.159202	25	5	2	3	5
7	Forward Power 27 MHz	8.34E-02	0.239934	25	5	2	5	7
8	Forward Power 2MHz	8.01E-02	0.281741	25	5	4	4	8
9	Gas 1	3.12E-04	0.138975	25	5	2	3	5
10	Gas 10	0.118018	0.346585	25	5	21	2	23
11	Gas 11	0.052708	0.280751	25	5	9	3	12
12	Gas 4	0.073181	0.259781	25	5	5	4	9
13	Gas 7	0.035394	0.076258	25	5	0	2	2
14	He Flow Inner	2.28E-05	0.044679	25	5	0	2	2
15	He Flow Outer	4.6E-06	0.00094	25	5	0	0	0
16	He Pressure Inner	1.10E-03	0.132547	25	5	1	3	4
17	He Pressure Outer	2.10E-03	0.28873	25	5	4	4	8
18	Pressure	9.29E-04	0.087312	25	5	1	2	3
19	Process Time	2.68E-04	0.238938	25	5	3	5	8
20	Reflect Power 27 MHz	1.28E-01	0.310348	25	5	8	5	13
21	Reflect Power 2 MHz	5.53E-02	0.208809	25	5	2	4	6
22	Top Plate Temperature	2.05E-03	0.164	25	5	0	5	5

Table 5.7: Significant factors of the first three stabilization steps decided after applying the seven captured samples in BPNN.

	Factor	Training MSE	Testing					
			MSE	Total ok	Total NG	Prediction Error		
						Type I	Type II	Total
1	Bias Voltage	2.80E-03	0.124238	25	5	1	1	2
2	ESC Clamp Voltage	2.94E-01	0.309331	25	5	11	4	15
3	ESC Current1	1.23E-03	0.158672	25	5	1	4	5
4	ESC Current2	8.39E-04	0.090059	25	5	1	2	3
5	ESC Temperature	6.93E-02	0.298836	25	5	7	3	10
6	Foreline Pressure	1.48E-02	0.173443	25	5	2	4	6
7	Forward Power 27 MHz	1.65E-01	0.210804	25	5	7	2	9
8	Forward Power 2MHz	1.07E-01	0.162356	25	5	3	4	7
9	Gas 1	1.48E-01	0.310306	25	5	6	5	11
10	Gas 10	0.14105	0.284822	25	5	8	2	10
11	Gas 11	0.11419	0.285237	25	5	10	2	12
12	Gas 4	0.126058	0.306326	25	5	10	2	12
13	Gas 7	0.059369	0.089669	25	5	0	3	3
14	He Flow Inner	0.004679	0.07716	25	5	0	2	2
15	He Flow Outer	5.57E-06	0.066095	25	5	0	2	2
16	He Pressure Inner	4.99E-02	0.21924	25	5	7	2	9
17	He Pressure Outer	1.13E-01	0.134201	25	5	2	2	4
18	Pressure	1.61E-02	0.087549	25	5	3	0	3
19	Process Time	1.68E-02	0.278871	25	5	4	4	8
20	Reflect Power 27 MHz	1.49E-01	0.277897	25	5	7	4	11
21	Reflect Power 2 MHz	1.10E-01	0.164839	25	5	2	4	6
22	Top Plate Temperature	1.63E-02	0.173433	25	5	0	5	5

Table 5.8: Significant factors of the first three stabilization steps decided after applying the six statistical summary values of each factor in BPNN.

	Factor	Training MSE	Testing					
			MSE	Total ok	Total NG	Prediction Error		
						Type I	Type II	Total
1	Bias Voltage	3.96E-03	0.039172	25	5	0	1	1
2	ESC Clamp Voltage	1.10E-01	0.20522	25	5	2	5	7
3	ESC Current1	0.00012	2.6E-05	25	5	0	0	0
4	ESC Current2	0.00018	0.00014	25	5	0	0	0
5	ESC Temperature	2.10E-02	0.259008	25	5	3	5	8
6	Foreline Pressure	8.39E-02	0.379738	25	5	8	3	11
7	Forward Power 27 MHz	1.34E-01	0.20496	25	5	3	5	8
8	Forward Power 2MHz	3.49E-02	0.075093	25	5	0	2	2
9	Gas 1	2.13E-02	0.214935	25	5	2	4	6
10	Gas 10	0.062548	0.170302	25	5	1	4	5
11	Gas 11	0.062872	0.299138	25	5	8	2	10
12	Gas 4	0.093493	0.280031	25	5	8	2	10
13	Gas 7	0.021478	0.050584	25	5	0	2	2
14	He Flow Inner	0.00064	0.00041	25	5	0	0	0
15	He Flow Outer	2.3E-05	2E-05	25	5	0	0	0
16	He Pressure Inner	1.69E-01	0.444219	25	5	10	5	15
17	He Pressure Outer	3.45E-02	0.34526	25	5	5	5	10
18	Pressure	0.00455	0.003	25	5	0	0	0
19	Process Time	1.73E-02	0.184719	25	5	1	4	5
20	Reflect Power 27 MHz	5.14E-02	0.388797	25	5	9	4	13
21	Reflect Power 2 MHz	5.85E-04	0.038753	25	5	2	0	2
22	Top Plate Temperature	3.82E-04	0.079331	25	5	0	3	3

The seven captured samples of each single RIE factor are applied as BPNN inputs. The training and testing results of these factors are shown in table 5.7. It is obvious there is no indicator for any of RIE significant factor in this trial. The last trial to find the significant factor is using statistical summary values of each single factor in BPNN. In this trial the mean values and standard deviation are calculated for the first three steps and applied in BPNN. Table 5.8 highlights five factors with zero error prediction, these five factors introduce the significant factors of the first three stabilization steps. He flow outer, He flow inner, ESC current 1, ESC current 2, and pressure considered as significant factors for online BPNN model.

5.5 Evaluations of prediction models

The major aspects in this section is to evaluate the performance of the prediction models, and decide the best prediction model with respect to a constraint, the same training and testing samples for all prediction models. The experimental data examined were collected from an etching of silicon dioxide thin film in reactive ion etching.

5.5.1 Offline BPNN prediction model

Figure 5.6 illustrates offline BPNN prediction model, where the five significant factors (Bias voltage, He flow inner, He flow outer, Pressure, and Reflect power 2MHZ) are the model inputs. By using three different data preparation techniques, the number of input neurons of BPNN is different. when raw data preparation technique applied in

offline BPNN, the number of input neurons is nine hundred, as well as one hundred seventy when captured sample is applied, and one hundred for statistical summary preparation technique.

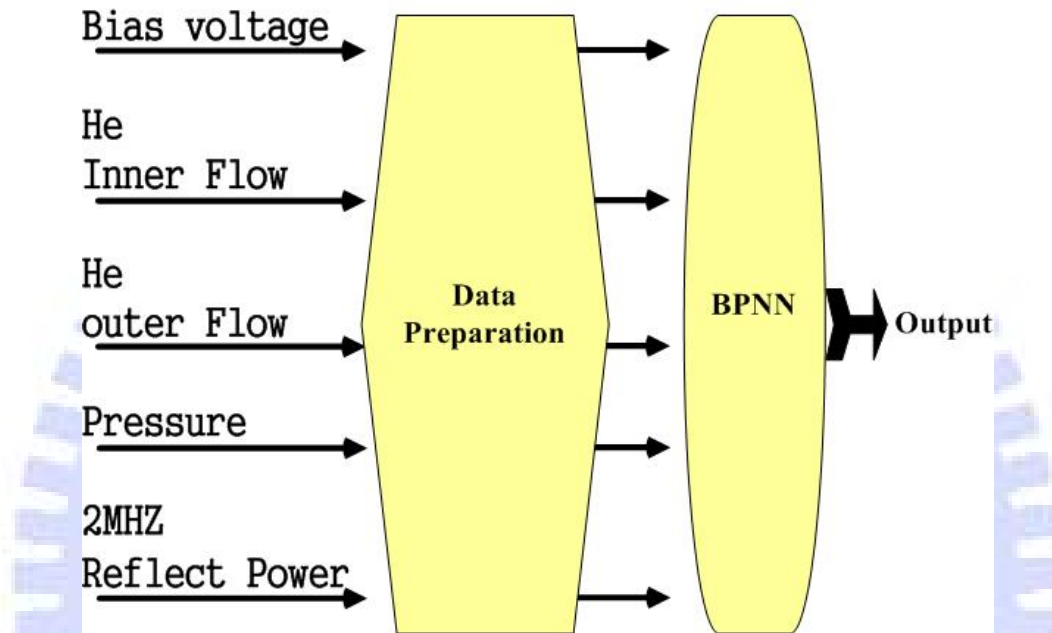


Figure 5.6: Offline BPNN prediction model

The first data preparation technique does not prepare data as well as other data preparation techniques, even it has good prediction of wafer status by using two factors (He flow outer, and Bias voltage), this refers to huge number of input neurons. In addition the raw data preparation technique has no ability to cover all etching steps. Table 5.9 illustrates the offline prediction model performance by using sampling and statistical summary preparation techniques. Both data preparation techniques assist the offline BPNN prediction model to achieve zero error prediction and 100% recognition rate.

100% recognition rate represents the percentage of test samples recognized correctly and the output values of test samples are located outside the zone values (0.1-0.9).

Table 5.9 : The performance of offline BPNN prediction model.

	Data preparation technique used in offline BPNN	
	Sampling	Statistical summary
Recognition rate	100%	100%
Training MSE	1.94311E-07	1.47594E-06
Testing MSE	5.12016E-09	7.46886E-07
# of input neurons	170	100
Error prediction	0%	0%

5.5.2 Online BPNN prediction model

Online BPNN prediction model follows the same data preparation techniques as offline BPNN prediction model, where the data is prepared in three different ways: raw data, sampling, and statistical summary. Furthermore un-open etching is the only defect occurred during the process. This defect starts in the first oxide main etching step (step 4). Therefore studying the stabilization steps as the environment preparation for the main etching step is the best way to predict the defect before it occurs.

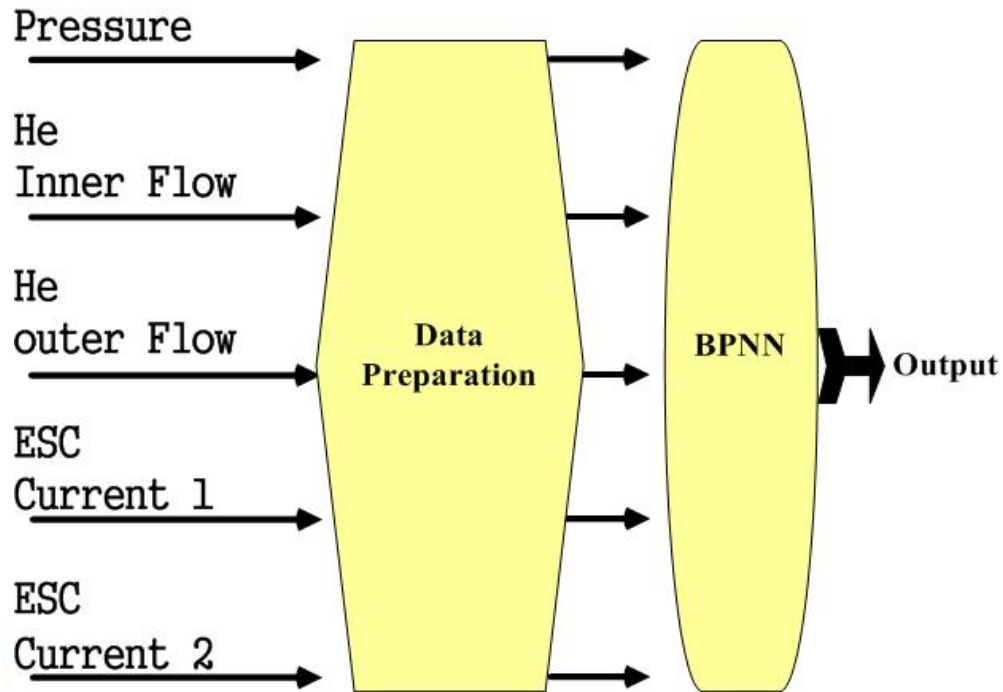


Figure 5.7: Online BPNN prediction model

The above figure illustrates the online prediction model and NN inputs include He flow outer, He flow inner, ESC current 1, ESC current 2 and pressure. In this part the asset of the three different data preparation techniques is compared, and this comparison is shown in table 5.9. First the raw data is used as BPNN input, where each factor has 20 data points, thus the total input is 100. Many error predictions occur by applying this data as shown in table 5.10. In addition, nineteen samples from thirty tested samples were clamped between the two zone values (0.1-0.9). Second, the thirty five captured samples represent the seven captured sample from each of RIE significant factor. The result of applying these prepared captured samples in online BPNN model is better than applying the raw data but still not desired. The good results are obtained by implement the prepared statistical summary in BPNN. Table 5.10 confirms that the best prediction

results are obtained by using the statistical data preparation techniques for online BPNN prediction model.

Table 5.10: The performance of online BPNN prediction model

	Data preparation technique used in online BPNN		
	Raw Data	Sampling	Statistical summary
Recognition rate	36.67%	100%	100%
Training MSE	6.88063E-06	5.33321E-06	1.52697E-05
Testing MSE	0.257240698	0.065732305	1.86654E-05
# of input neurons	100	35	30
Error prediction	33.33%	6.67%	0%

5.5.3 Offline PCABPNN prediction model

To construct offline PCABPNN prediction model, principle component analysis (PCA) and back propagation neural network (BPNN) combines together. First, PCA is adopted to extract valuable information from the twenty two RIE factors for each step. Then the extracted principle component for all steps combined together and prepared by the three different techniques. After that, neural network is trained by the prepared PC data of 90 training wafers, and the prepared PC data of 30 testing wafers are used to test the prediction accuracy, and the three different data preparation techniques are: raw PC, sampling PC, and statistical summary of PC.

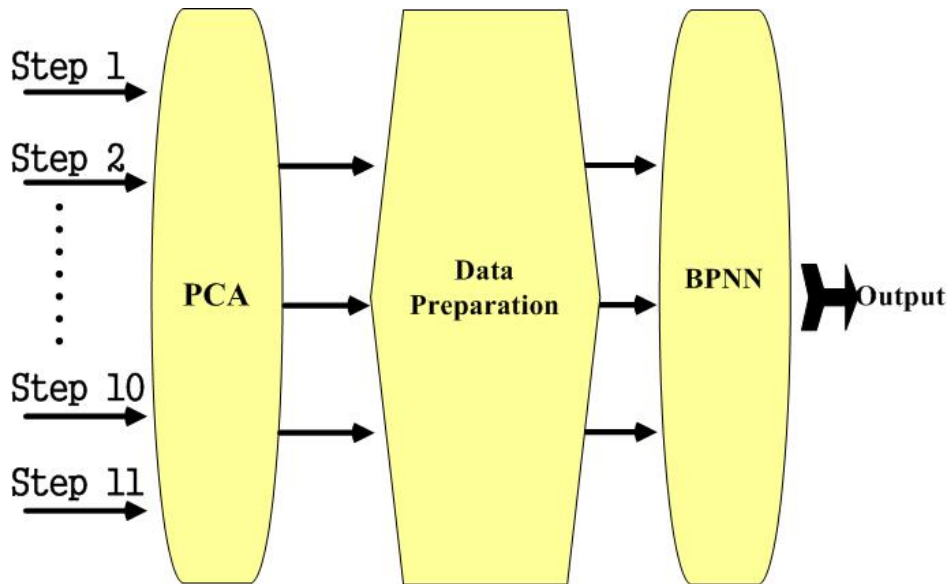


Figure 5.8: Offline PCABPNN prediction model

The above figure illustrates the offline PCABPNN prediction model. Principle component analysis is applied in this model to extract the input parameters for neural networks. Moreover the required time to find the principle components is much less than the required time to find the significant parameter.

One hundred eighty data points of each principle component parameters is prepared by raw data preparation technique. Totally, there are five hundred and forty neuron inputs for the three PCS. Since the raw data covers the first one hundred and eighty data of PCs, the rest of data points are ignored. The ignored points of PCs may contain important information. As shown in figure 5.9, three defected wafers incorrectly predicted as good wafer by using raw data preparation technique. Obviously all error prediction takes place in type II prediction error.

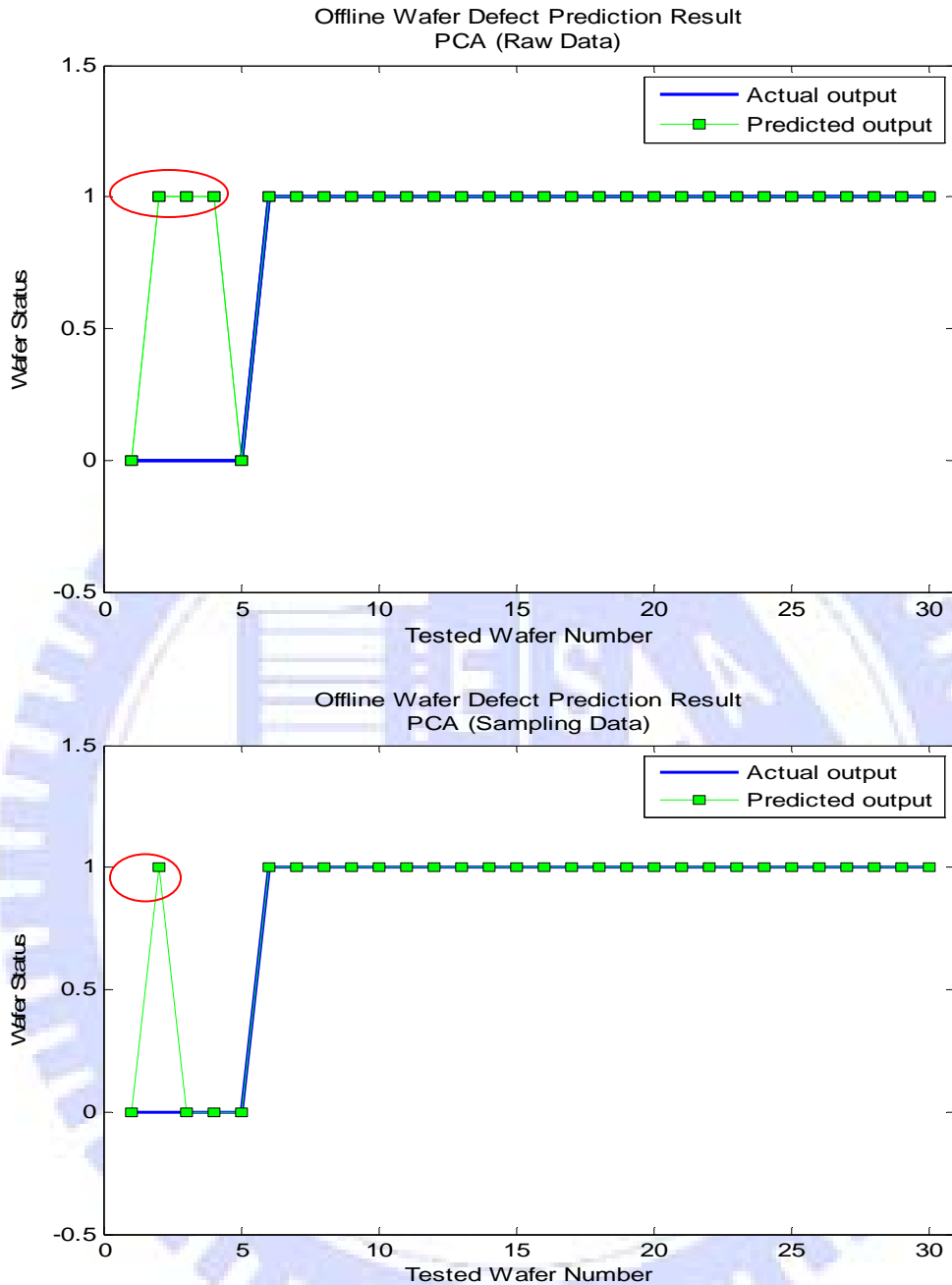


Figure 5.9: Result of testing 30 wafers in offline PCABPNN prediction model by using a) raw data of PCs b) sampling PCs

In the manner of minimizing the input data size more and more, one hundred and two captured samples from the three principle components are trained and tested in BPNN (table 5.11). Four samples from thirty tested samples were clamped between 0.1-

0.9 (the Max and Min zone values) by applying captured samples in offline PCABPNN prediction model, one by applying the first bunch of data sets, and by applying statistical summary there is no samples found in the failure zone, due to high accuracy (100% recognition rate) of the prediction model. Generally a statistical summary preparation technique has the best ability to enhance the accuracy of the offline PCABPNN prediction model.

Table 5.11: The performance of offline PCABPNN prediction model

	Preparation technique used in offline PCABPNN		
	Raw PC	Sampling	Statistical summary
Recognition rate	96.67%	86.67%	100%
Training MSE	1.29021E-06	2.4213E-05	4.52214E-06
Testing MSE	0.101489096	0.041548198	4.05693E-05
# of input neurons	540	102	60
Error prediction	10.00%	3.33%	0%

5.5.4 Online PCABPNN prediction model

Previously in offline PCABPNN prediction model, three principle components is used to represent the RIE factors then properly prepared, trained and tested in BPNN for all etching steps. In this section, the same strategy will be followed by using the three stabilization steps. Figure 5.10 illustrates the online PCABPNN prediction model.

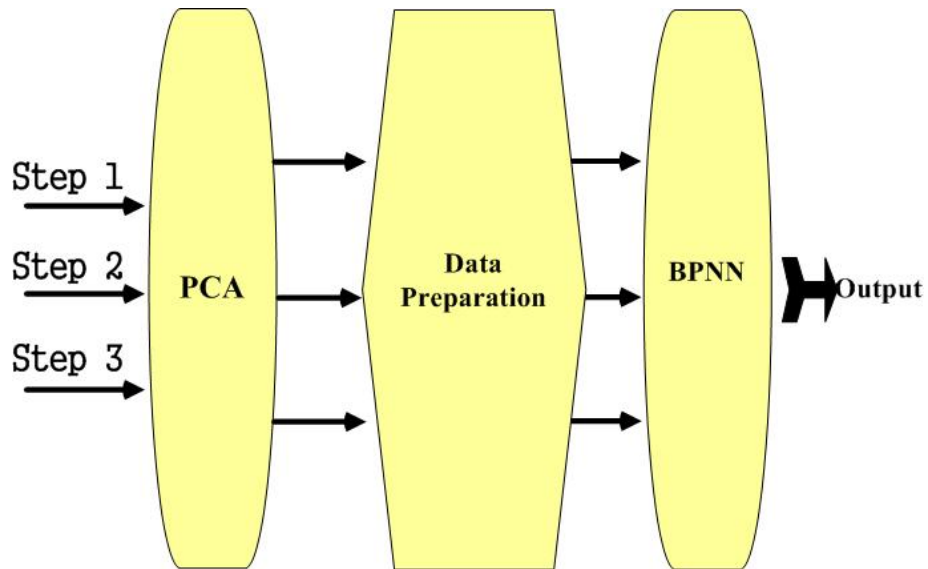


Figure 5.10: Online PCABPNN prediction model

Table 5.12: The performance of online PCABPNN prediction model

	Preparation technique used in online PCABPNN		
	Raw PC	Sampling	Statistical summary
Recognition rate	83.33%	86.67%	100%
Training MSE	0.000128213	0.001259355	6.35134E-05
Testing MSE	0.097786026	0.114389121	0.000143241
# of input neurons	60	21	18
Error prediction	13.33%	10.00%	0%

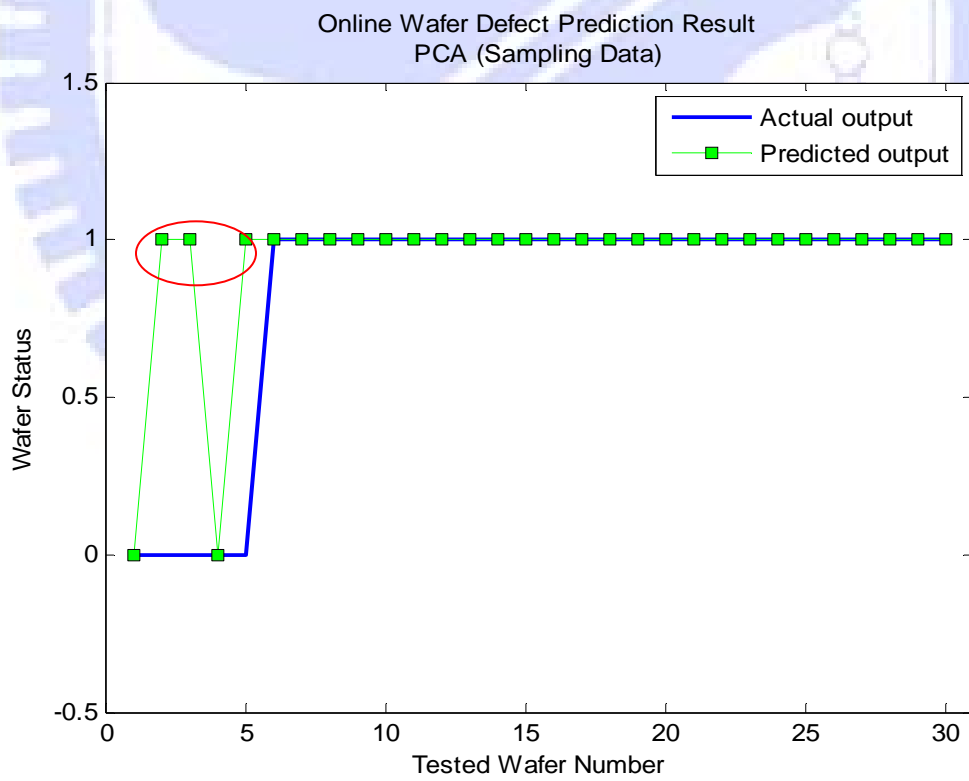
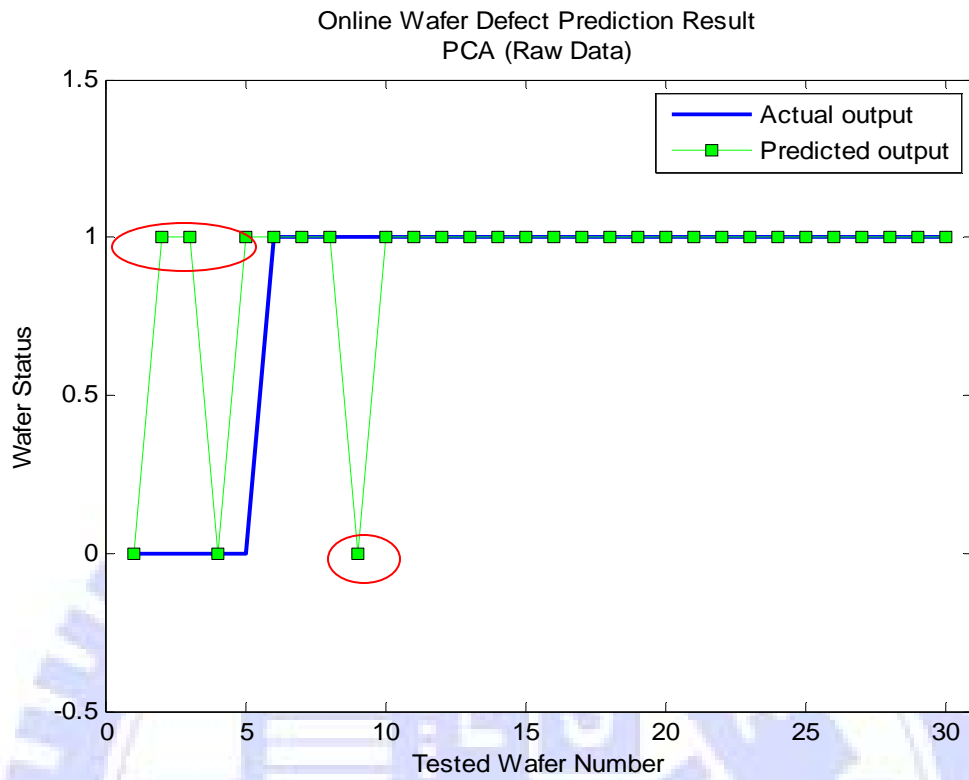


Figure 5.11: Result of testing 30 wafers in online PCABPNN by using a) raw data of PCs
b) sampling PCs

Figure 5.11 clarify the number of error prediction in raw and sampling preparation techniques. Four predictions incorrectly predicted by using the raw preparation technique data, and three by using the sampling preparation techniques, while there is no error prediction by using statistical summary. Four samples from thirty tested samples were clamped between 0.1-0.9 (the failure zone) by applying captured samples in online PCABPNN prediction model, and five by applying the first twenty data sets, and by applying statistical summary there is no samples found in the failure zone, due to high accuracy (100% recognition rate) of the prediction model. Generally online PCABPNN prediction model using sampling PCs has a slight better ability than using raw PCs in prediction and statistical summary has the best ability to enhance the accuracy of the online PCABPNN prediction model.

The best result is obtained by applying PCs statistical summary. This input classification technique has ability to support BPNN to predict the wafer status without any error, as well as short training time of neural network with minimum values of mean square error as shown in table 5.12.

5.6 Summary

In this chapter, BPNN is the backbone of prediction models, and four prediction models are established to predict the wafer status: offline BPNN, offline PCABPNN, online BPNN, and online PCABPNN. The original data in three different ways: raw data by using the first set of data points, capturing samples from the original data, and the statistical summary values by calculate the mean and standard deviation values for each step. The defined value range (Max and Min zone values) must be established to determine whether the output value is close to the target value. 0.1 is the highest output value for defected wafer and 0.9 value is the lowest value for good wafer.

This chapter introduce method to decide the significant process parameters which affect the wafer status in RIE by comparing the result of applying each process parameter alone in BPNN. The significant parameters for all etching steps combined together in offline BPNN to tackle the defected wafer. The offline significant factors are: bias voltage, He flow inner, He flow outer pressure, and reflect power 2MH. Furthermore the significant parameters for the first three etching steps combined together in online BPNN to forecast the wafer status. Online significant factors are: He flow outer, He flow inner, ESC current 1, ESC current 2, and pressure.

The four prediction models are capable to predict the wafer status correctly by using statistical summary preparation techniques. Offline models predict the wafer status concerning all etching process. In other hand, online prediction models depend on the

stabilization steps, thus the wafer defect can be predicted before the end of the first main etching step.

Figure 5.12 summarize the error prediction of online and offline models. The first six columns represent the offline prediction models with different data preparation techniques. The rest columns represent the online prediction models.

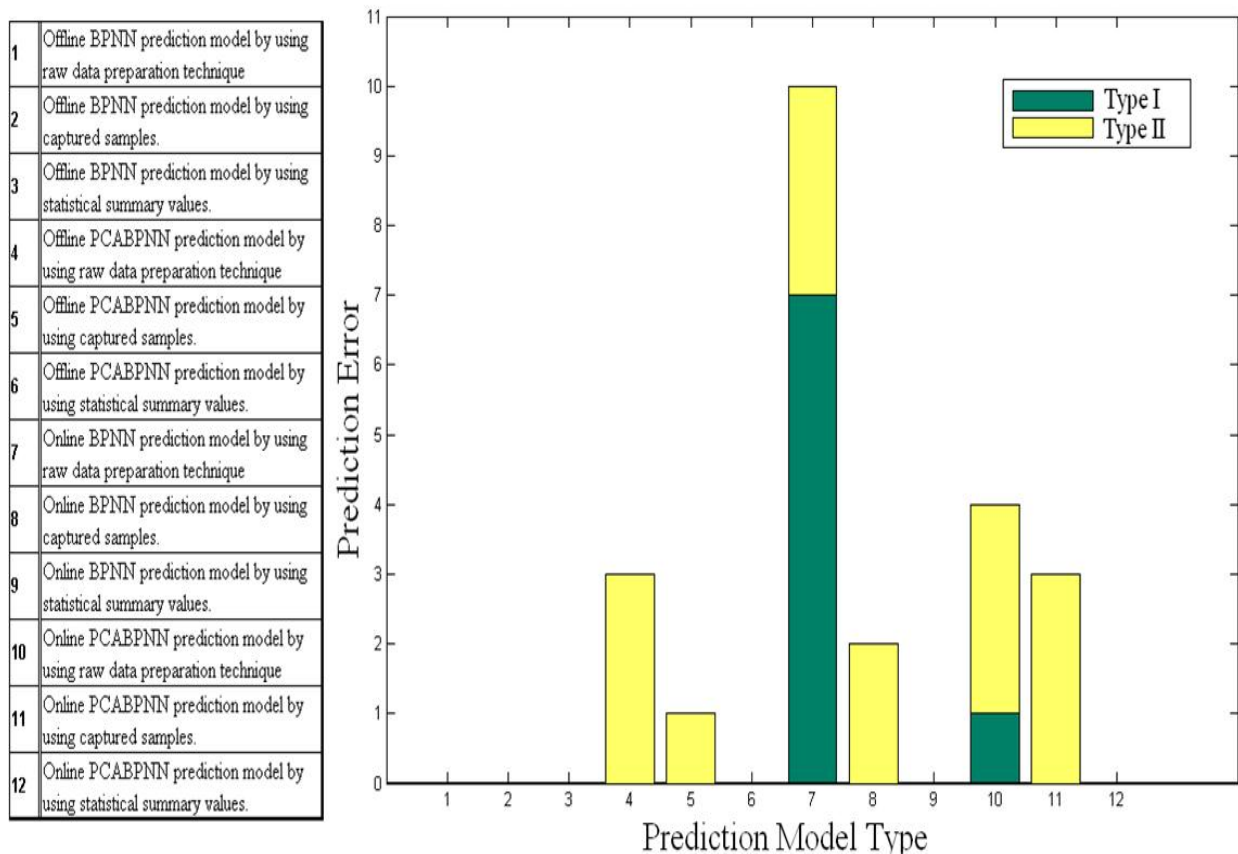


Figure 5.12: Summary of error prediction in online/offline prediction models using several data preparation techniques.

CHAPTER 6

CONCLUSION

6.1 Conclusion

The goal of this thesis is to predict the wafer status during/after RIE process by using online/offline prediction models. BPNN is the backbone of the four prediction models: offline BPNN, offline PCABPNN, online BPNN, and online PCABPNN. In order to achieve fast and robust predictive model, only the first three preparation steps of the RIE process is used in online prediction models. This thesis describes the potential of these prediction models to reduce the overall cost of semiconductor and achieving high yields and throughput during semiconductor fabrications, where these models not depend upon monitor wafers or expensive metrology rather it will enable inexpensive real-time wafer-to-wafer inspection application.

Achieving the accurate prediction of the wafer status faced some difficulties, such as: managing the huge data for each wafer, dealing with missing data, deciding the RIE significant factors, preparing a homogeneous set of input data for BPNN, covering the variation of RIE steps, having a shortage of defected wafer samples. The thesis also explains the implemented techniques to solve these difficulties.

Preparing data technique is important to prepare a homogeneous set of input data for BPNN in three different ways: raw data by using the first set of data points, capturing samples and the statistical summary values by calculate the mean and standard deviation values for each step. However, by comparison between prediction models with different data preparation techniques, the statistical summary technique provides high ability to cover all data of etching process in convenient way. Statistical summary preparation technique avoids using a huge data as raw data, or missing critical data as sampling.

Other technique is deciding RIE significant factor technique by comparing the result of applying each process factor alone in BPNN. When defected wafer is predicted by online prediction models, the significant parameters are modified to avoid any defect during the process and to decrease the down/ repair time of the equipment. Unlikely, the offline prediction models, which are built to track the defected wafer after RIE process.

The results from the evaluation of the four prediction models indicate that robust, accurate and stable predictors have been constructed. Furthermore, a greater accurate performance of prediction models has been achieved by online BPNN prediction model.

6.2 Future Extensions

The techniques presented here for deciding the significant factors in RIE process are general in the sense and can be applied to many other plasma environments process. Moreover, this methodology can also be applied to other semiconductor equipment to find the significant factors.

The best performance of prediction models has been achieved by online BPNN prediction model. This model can be further extended to predict the plasma characteristic, etching parameters and other type of defect. The online BPNN performance can be enhanced by implement fast and continuance feedback control.

Statistical summary preparation technique has the potential to meet the prediction models requirements in RIE process. Excellent models could be achieved by implementation the statistical summary preparation technique in multi-step processes.

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APPENDIX I

TERMINOLOGY

- Critical Dimension** CD. The width of a patterned line or the distance between two lines of the sub-micron sized circuits in a chip.
- Dielectric** A material that conducts no current when it has a voltage across it; an insulator. Two dielectrics commonly used in semiconductor processing are silicon dioxide (SiO₂) and silicon nitride (SiN).
- Drift** A change of a reading or a set point value over long periods due to several factors including change in ambient temperature, time, and line voltage
- Electrostatic Chuck** Lower plate in a chamber that holds wafers using electrostatic attraction, allowing the temperature to be regulated with confined helium gas. Different types of ESC include bipolar designs based on dual electrodes in the chuck and monopolar chucks with a single electrode. Plasma gas that comes in contact with the wafer provides the other electrode in the circuit that clamps the wafer in place. Also called a chiller plate (temperature typically = 15 C).
- Etch** A solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material

either selectively or non-selectively.

FAB Semiconductor fabrication facility. Under precise conditions, silicon or other semiconductor materials are transformed along with other basic elements into semiconductors, or microchips.

In situ In the natural or original position or place. For SensArray, this means performing tests in or on the actual device (process chamber, hotplate, etc.) that will be used to produce the end product. This provides real world data as to the characteristics of the device.

Insulator Nonconductive dielectric films used to isolate electrically active areas of the device or chip from one another. Some commonly used insulators are silicon dioxide, silicon nitride, boro-phospho-silicate glass (BPSG), and phospho-silicate glass (PSG).

Ion Implantation A process technology in which ions of dopant chemicals (boron, arsenic, etc.) are accelerated in intense electrical fields to penetrate the surface of a wafer, thus changing the electrical characteristics of the material.

Load Lock An isolation chamber that allows a process chamber to be protected from ambient conditions.

Metallization The deposition of a layer of high-conductivity metal such as aluminum used to interconnect devices on a chip by CVD or PVD. Metals typically used include aluminum, tungsten, and copper.

Photo-resist	A light-sensitive organic polymer that is exposed by the photolithography process, then developed to produce a pattern which identifies areas of the film to be etched.
Plasma	Ionized gases that have been highly energized—for example, by a radio frequency energy field. This can be used to remove resist, to etch, or to deposit various layers onto a wafer.
Plasma-Enhanced TEOS Oxide Deposition	A deposition process in which tetraethoxysilane (TEOS) is used as a silicon source to deposit silicon dioxide on a wafer surface.
Polysilicon (Poly)	Polycrystalline silicon; extensively used as conductor/gate material in a highly doped state. Poly films are typically deposited using high-temperature CVD technology.
Process Chamber	An enclosed area in which a process-specific function occurs during wafer manufacturing.
PVD	Physical Vapor Deposition (also called sputtering). A process technology in which molecules of conducting material (aluminum, titanium nitride, etc.) are "sputtered" from a target of pure material, then deposited on the wafer to create the conducting circuitry within the chip.
RIE	Reactive Ion Etch. A combination of chemical and physical etch processes using electrical discharge to ionize and induce ion bombardment of the wafer surface to obtain the required etch properties.

Short Term Drift	A change in the temperature reading of the sensor(s) at a fixed ambient reference temperature over short periods of time. Usually expressed as degrees C change per hour.
Silicon (Si)	A brownish crystalline semimetal used to make the majority of semiconductor wafers.
Silicon Dioxide(SiO₂)	A passivation layer thermally grown or deposited on wafers. It is resistant to high temperatures. Oxygen or water vapor is used to grow silicon dioxide at temperatures above 90 C. Silicon dioxide is used as a masking layer as well as an insulator.
Stepper	Equipment used to transfer a reticle (mask) pattern onto a wafer.
Substrate	A material that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits. Examples of a substrate would include a silicon wafer or a glass panel.
Test Wafer	A wafer used for process monitoring during semiconductor manufacturing. The two types are the reclaim test wafer and the virgin test wafer. With test wafers you are looking at some telltale indication of differences in film thickness, a change in resistance in material, the width of a line, or a feature (critical dimension) due to changes in the temperature of the wafer.
Wafer	The thin, circular slice with parallel faces of pure silicon cut from a semiconductor crystal on which semiconductors are built.
Yield	The percentage of wafers or die produced in a process that

conform to specifications.

APPENDIX II

PRINCIPAL COMPONENT SCORES

First Step

T1=5.86708E-05* X1+0.546231739* X2+0.459104457* X3-0.687346122* X4+ 0.120997137*X5-0.024607657*X6-0.01546252*X7+0.037171837*X8-0.008616296*X9-0.027682561*X10-0.015565648*X11+0.000749651*X12+0.000993437*X13+0.017607152*X14+0.004106208*X15+0.001762721*X16-0.011273633*X17+0.000400883*X18-0.000195308*X19-0.000247851*X20+0.000143606*X21-0.000923064*X22

T2=0.986038172*X1+0.104385047*X2-0.115933952*X3+0.006370927*X4-0.000647477*X5+0.017977415*X6-0.048535924*X7+0.000639341*X8+0.01554936*X9-0.009793151*X10-0.008988219*X11+0.00076505*X12+0.00617509*X13+0.003001199*X14+-0.012319314*X15-0.007244526*X16-0.000181166*X17-0.000789505*X18-0.000466365*X19-0.000166924*X20-0.000335061*X21+1.48487E-05*X22

T3=0.008021016*X1+0.013376482*X2-0.019808141*X3+0.003497373*X4-0.000741688*X5-0.014390371*X6+0.016886632*X7-0.00111331*X8-0.038140459*X9-0.089417401*X10+0.006995821*X11+0.001394329*X12-0.148079622*X13-0.111822932*X14 +0.627665724*X15+0.240686736*X16+0.002168992*X17+0.034033381*X18-0.009380544*X19+0.001048596*X20+0.019866493*X21-0.708084741*X22

Second Step

T1=-0.354114706*X1+0.035521819*X2-0.878591862*X3-0.311590495*X4+0.05696743*X5+0.006044721*X6+0.023719273*X7+0.019545046*X8-0.009772107*X9-0.002392207*X10-0.000575023*X11-0.000174334*X12-0.000102076*X13+1.8192E-05*X14-0.000134733*X15-0.000171802*X16-0.000763645*X17-0.000104452*X18-7.37068E-05*X19+3.11709E-05*X20+4.93154E-05*X21-2.39054E-06*X22

T2=0.602331325*X1+0.721616167*X2-0.202175066*X3-0.035037909*X4-0.00375017*X5-0.049427968*X6+0.10908854*X7-0.191688965*X8-0.087223692*X9+0.007681086*X10+0.090988065*X11-0.047546442*X12+0.006836049*X13-0.015198189*X14-0.044003165*X15+0.018545951*X16+0.000904692*X17+0.014537893*X18+0.045280312*X19+0.006767968*X20-0.010336403*X21-0.009109348*X22

$T3=0.004534557*X1+0.004740745*X2-0.000967676*X3+0.000283037*X4+7.37904E-05*X5-0.003701451*X6+0.003848999*X7+0.016360947*X8+0.042280312*X9-0.042969926*X10-0.142139569*X11-0.20737578*X12+0.654802509*X13+0.030119638*X14+0.006177543*X15-0.024643304*X16-0.708422833*X17+0.024061247*X18+0.006784032*X19-0.002273661*X20-0.001308064*X21+0.001898524*X22$

Third Step

$T1=0.430688639*X1+0.847478428*X2-0.165820994*X3+0.086554107*X4-0.197860797*X5+0.112048955*X6-0.081460464*X7+0.046883485*X8+0.01078079*X9-0.009227447*X10+0.000290796*X11-0.021466767*X12-0.009919743*X13-2.77792E-05*X14-0.000914824*X15-0.000232031*X16+6.07323E-05*X17-0.00028271*X18-3.22174E-05*X19+8.2611E-05*X20+1.8679E-05*X21-9.93881E-06*X22$

$T2=-0.514382513*X1+0.335243688*X2+0.625946137*X3+0.339111142*X4-0.053939665*X5-0.193932407*X6-0.208174561*X7+0.127930391*X8-0.015477023*X9-0.019894857*X10-0.101250889*X11-0.001383593*X12+0.008990209*X13-0.01712394*X14-0.048612491*X15+0.010611435*X16-0.005579367*X17-0.002615967*X18-0.045617352*X19+0.001295207*X20-0.00979156*X21+0.006322221*X22$

$T3=-0.004189428*X1+0.002295447*X2+0.003633652*X3-0.001456438*X4-0.006443019*X5-0.003852316*X6+0.008183371*X7-0.05939669*X8-0.00948419*X9+0.034161819*X10+0.011786961*X11-0.418911675*X12+0.565158005*X13+0.033366206*X14+0.005702036*X15-0.132466162*X16+0.01054651*X17-0.693260971*X18-0.003421485*X19+0.021789178*X20+0.010976664*X21-0.001424268*X22$

Fourth Step

$T1=0.368620854*X1-0.430848807*X2-0.644626727*X3+0.503884164*X4+0.0712812*X5+0.046859269*X6+0.020478759*X7+0.017175169*X8-0.021740932*X9+0.001626559*X10+0.00221292*X11+0.020450627*X12-0.012292147*X13-0.002045109*X14+0.000169736*X15-0.000360146*X16-8.6131E-06*X17-0.000238984*X18+1.33751E-05*X19-4.39971E-05*X20-2.59677E-06*X21+1.44149E-08*X22$

$T2=-0.26107794*X1+0.6779526*X2-0.10558619*X3+0.618415541*X4+0.058284557*X5-0.069163594*X6+0.040921583*X7+0.165583636*X8-0.115117276*X9+0.06123872*X10-0.114213051*X11+0.075425831*X12-0.015084612*X13+0.004905207*X14-0.053417504*X15-0.016390162*X16+0.003324123*X17+0.001174298*X18+0.045380094*X19-0.003549852*X20+0.011687835*X21-0.005351677*X22$

$T3=-0.003121539*X1+0.002105527*X2+0.005574911*X3-0.006562001*X4+0.058260926*X5-0.018911829*X6-0.009825818*X7+0.01375895*X8+0.134485055*X9-0.048327995*X10+0.214599357*X11+0.57620168*X12+0.303949769*X13+0.017051337*X14+0.00416464*X15+0.000253212*X16+0.003900452*X17-0.709971383*X18+0.015578234*X19-0.016787738*X20+0.009535875*X21+0.00266647*X22$

Fifth Step

$$T1=0.365956063*X1+0.084013161*X2+0.924990635*X3-0.034408355*X4-0.031511413*X5+0.028409836*X6-0.005644674*X7-3.08385E-06*X8+0.018651207*X9-0.000274675*X10+0.004698971*X11+0.000166843*X12-0.003840744*X13-0.002294469*X14-3.8956E-05*X15+0.000887946*X16-0.001877223*X17+7.35268E-05*X18-2.3266E-05*X19-3.3814E-05*X20+ 6.47739E-06*X21-2.73504E-06*X22$$

$$T2=-0.252078084*X1-0.49686573*X2+0.17735191*X3+0.659618411*X4+0.401038469*X5+0.040495219*X6+0.01834063*X7+0.048147654*X8+0.203858359*X9-0.050874526*X10+0.07606143*X11+0.015362716*X12+0.006052801*X13-0.010645192*X14-0.024916738*X15-0.006220284*X16-0.0274209*X17+0.062067383*X18-0.028769885*X19-0.038662152*X20+0.000416643*X21+0.000666248*X22$$

$$T3=-0.003563025*X1-0.005320426*X2+0.0024016*X3+0.019478196*X4-0.010718771*X5-0.0045951*X6+0.013361096*X7+0.083093811*X8+0.133430648*X9-0.091284804*X10-0.665944999*X11-0.020888086*X12+0.164570601*X13-0.688680913*X14+0.022028582*X15+0.008305847*X16+0.141730778*X17-0.015529404*X18+0.005622276*X19+0.004221272*X20+0.001212558*X21-0.000460269*X22$$

Sixth Step

$$T1=0.354580568*X1+0.027713338*X2+0.17382398*X3-0.917917501*X4+0.012380125*X5-0.002382986*X6-0.003498559*X7-0.015468861*X8+0.011755643*X9+0.003355274*X10+0.010579234*X11-0.000726698*X12+0.006026301*X13+0.002387839*X14+0.001296119*X15-0.000819123*X16+0.000396554*X17+0.000527211*X18-0.000301053*X19+9.25346E-05*X20+1.59576E-05*X21-1.20968E-05*X22$$

$$T2=-0.255655531*X1-0.637224146*X2+0.680144788*X3+0.00683278*X4+0.010530315*X5-0.021728555*X6-0.013784199*X7+0.104760186*X8-0.11574109*X9-0.056307313*X10+0.005611104*X11+0.097732697*X12-0.13648432*X13+0.040363359*X14+0.044819938*X15+0.007816626*X16+0.01042188*X17-0.005511137*X18+0.063285641*X19-0.005921726*X20+0.038734217*X21-0.006169062*X22$$

$$T3=-0.004062506*X1-0.007813051*X2+0.008604574*X3-0.002318515*X4-0.00263726*X5-0.011863917*X6+0.014870324*X7-0.346889469*X8-0.172416783*X9-0.021724342*X10-0.598084314*X11+0.043499413*X12+0.023075443*X13+0.171346549*X14+0.13081052*X15-0.646869444*X16-0.153758875*X17-0.012663054*X18-0.008527571*X19-0.003322232*X20-0.003688184*X21-0.001506919*X22$$

Seventh Step

$$T1=0.33647838*X1-0.015538579*X2+0.081535218*X3-0.935183493*X4+0.068258325*X5+0.019050631*X6-0.005471934*X7-0.011329101*X8+0.000349688*X9-0.005161869*X10-0.007019663*X11+0.006904662*X12+0.003193943*X13-0.002480654*X14-0.000613684*X15-0.001838597*X16+0.000488617*X17+0.00035862*X18+0.000286916*X19-3.79954E-06*X20-1.91935E-05*X21-1.15881E-05*X22$$

$$T2=-0.279000558*X1+0.911324425*X2+0.091455252*X3-0.109681988*X4-0.027038587*X5-0.046093078*X6+0.050872952*X7+0.01372742*X8-0.143189167*X9-0.190746611*X10-0.040677451*X11-0.010094689*X12-0.011802336*X13-0.0075988*X14-0.004722408*X15-$$

0.002690163*X16+0.043377532*X17-0.004906011*X18+0.022620602*X19-0.052113724*X20-0.039688*X21-0.006421394*X22

T3=-0.004340388*X1+0.009635578*X2-8.73757E-05*X3-0.0049822*X4-0.00945227*X5-0.017746015*X6+0.000688668*X7-0.008566808*X8+0.00939179*X9+0.0403564*X10+0.055686045*X11-0.519168475*X12+0.484298329*X13+0.070818635*X14+0.038869329*X15-0.460038348*X16+0.134982175*X17-0.365648433*X18-0.346800682*X19+0.006635867*X20-0.00602675*X21-0.007441692*X22

Eighth Step

T1=0.383460303*X1-0.089948782*X2-0.033637064*X3-0.912177057*X4-0.047278856*X5+0.081599692*X6+0.048737168*X7+0.005041032*X8-0.014832059*X9-0.005014885*X10-0.008382352*X11+0.007086067*X12+0.000743782*X13+0.002644473*X14+0.000973795*X15+0.000571081*X16+0.000130895*X17-5.01955E-06*X18+3.12363E-06*X19-3.22849E-05*X20-7.74237E-06*X21-8.42386E-06*X22

T2=-0.580649567*X1+0.692519386*X2-0.107900903*X3-0.304578503*X4-0.00111383*X5-0.06796587*X6+0.112274152*X7-0.058350067*X8-0.149001297*X9-0.002133197*X10-0.166804174*X11+0.027782667*X12+0.003114838*X13+0.004287839*X14-0.033312996*X15+0.009788076*X16+0.013173508*X17+0.010488597*X18+0.058739998*X19+0.028508795*X20-0.039488689*X21-0.008963988*X22

T3=-0.006059678*X1+0.006626124*X2+0.000396917*X3-0.006851063*X4-0.002013383*X5-0.025395817*X6-0.007684929*X7+0.00380128*X8-0.00020068*X9-0.032880197*X10-0.002334102*X11+0.000688318*X12-0.356410217*X13-0.59888028*X14+0.348040669*X15+0.612722612*X16-0.1244754*X17+0.009418507*X18-0.012488118*X19-0.001755972*X20-0.006141005*X21-0.005998429*X22

Ninth Step

T1=0.434169921*X1+0.333741296*X2-0.178016661*X3-0.808546515*X4+0.077819878*X5+0.042275292*X6-0.077036336*X7+0.008482664*X8-0.007092484*X9-0.018007962*X10+0.013856207*X11+0.007641633*X12-0.013382094*X13+0.000532896*X14-0.004130055*X15+0.000416251*X16-0.002062043*X17+0.000214287*X18-0.000234298*X19-0.000464177*X20+1.01021E-05*X21+4.58091E-06*X22

T2=-0.545359547*X1+0.759282029*X2-0.002172991*X3+0.048626841*X4+0.035725594*X5+0.288532471*X6-0.058025897*X7+0.007986958*X8+0.095671122*X9-0.095446917*X10+0.096444101*X11+0.027386666*X12-0.025372316*X13+0.017650929*X14+0.036151789*X15+0.006878677*X16-0.007397823*X17-0.058514624*X18+0.000432573*X19+0.002569153*X20-0.039774559*X21-0.007398028*X22

T3=-0.005769303*X1+0.009479674*X2+0.001185837*X3-0.00523533*X4+0.027177928*X5+0.014060466*X6-0.007148443*X7-0.010726084*X8+0.002810879*X9-0.041322565*X10+0.014032601*X11-0.007800987*X12+0.676843928*X13-0.200380862*X14-0.028598487*X15+

0.001068294*X16-0.030158155*X17-0.04114025*X18+0.151297081*X19-0.687159832*X20+
9.51477E-07*X21-0.001281719*X22

Tenth Step

T1=0.124137*X1-0.004652*X2-0.106555*X3-0.044890*X4+0.043621*X5+0.026096*X6-0.026676*X7-
0.011304*X8-0.010170*X9+0.028126*X10-0.065352*X11+0.201877*X12+
0.258898*X13+0.25666*X14+0.580403*X15-0.47441*X16-2.44308*X17+1.78379*X18+ 0.1153*X19 -
1.6740*X20-0.2414*X21-0.093*X22

T2=0.005050*X1-0.057781*X2+0.057254*X3+0.337367*X4+0.292113*X5+0.271200*X6+
0.115685*X7+0.819238*X8-0.045968*X9-0.428254*X10-0.028633*X11+0.012117*X12+
0.065238*X13-0.09649*X14+0.112155*X15-0.04521*X16-0.02117*X17+0.03360*X18+ 0.0077*X19 -
0.0457*X20+0.0040*X21+0.041*X22

T3=-0.070804*X1+0.222462*X2-0.052241*X3+0.051533*X4+0.098335*X5+0.018543*X6-
0.068935*X7-0.016599*X8-0.046855*X9+0.055178*X10-0.675068*X11-0.123001*X12+
0.126466*X13+0.21376*X14+0.208800*X15-0.15170*X16+0.07814*X17-0.11000*X18+ 0.0306*X19 -
0.3028*X20-66.7008*X21+7.527*X22

Eleventh Step

T1=0.978819*X1-0.148912*X2+0.041304*X3-0.079048*X4-0.108462*X5-0.000037*X6-0.004292*X7-
0.001217*X8+0.000004*X9+0.000319*X10+0.000031*X11-0.000033*X12+ 0.000010*X13-
0.000003*X14-0.000011*X15+0.000011*X16+0.000005*X17-0.000002*X18-
0.000001*X19+0.000001*X20

T2=-0.497487*X1+0.860423*X2-0.049980*X3-0.097920*X4-0.009503*X5-0.000887*X6+
0.000065*X7+0.000068*X8-0.000393*X9+0.000191*X10-0.000269*X11+0.000035*X12-
0.000090*X13+0.000069*X14-0.000012*X15-0.000010*X16-0.000002*X17-0.000003*X18-
0.000004*X19+0.000003*X20

T3=-0.726223*X1+0.623964*X2+0.042757*X3-0.176362*X4-0.001025*X5-0.028279*X6+
0.053120*X7+0.010456*X8+0.011983*X9+0.006454*X10-0.115982*X11-0.039236*X12+
0.138793*X13-0.086707*X14+0.005794*X15+0.014646*X16+0.006590*X17-0.005666*X18+
0.054923*X19-0.036161*X20-0.000005*X21-0.000592*X22