Chapter 1

Introduction

1.1 An overview of poly-Si TFTs technology

In recent years, polycrystalline silicon thin film transistors (poly-Si TFTs) have attracted more and more attention because of their wide applications in active matrix liquid crystal displays (AMLCDs)[1-3], and in some memory devices such as dynamic random access memories (DRAMs)[4], static random access memories (SRAMs)[5], electrical programming read only memories (EEPROMs)[6], and electrical erasable programming read only memories (EPROMs)[7]. In addtion, several linear image sensors [8], thermal printer heads [9], photodector amplifier [10], and three dimension LSIs [11] have also adopted poly-Si TFTs technology. Among these, AMLCDs are the most primary application of poly-Si TFTs and lead extensively rapid development in poly-Si TFTs.

Unlike amorphous silicon (a-Si) TFTs, poly-Si TFTs have much larger carrier mobility which usually exceeds 100 cm^2 / Vs by present mature technology. Its superior carrier mobility is essential to successfully integrate polys-Si TFTs and peripheral driving circuits [5] on the same panel to reduce the assembly complexity and cost. Therefore, the low process temperature of poly-Si TFTs with the high mobility makes it possible to realize the ultimate goal, system-on-panel [12]. Furthermore, due to the higher mobility of poly-Si TFTs, the dimension of the poly-Si TFTs can be made smaller than that of a-Si TFTs to achieve high density and high resolution AMLCDs.

However, there are still some problems existed in poly-Si TFTs. Compared to single crystalline silicon, poly-Si has a lot of defects at the grain boundaries. These defects, regarding as trap states, locate in the disordered grain boundary region and degrade device performance severely. In other words, the performances of poly-Si TFTs are strongly affected

by the grain structure inside the channel region. Thus, the larger grain with less grain boundary defects is desirable and currently many researches attempting to achieve this goal have been studied, such as solid-phase crystallization (SPC)[13], metal-induced-lateral crystallization (MILC)[14] and laser crystallization [15]. As a result, one of the major barriers in developing the technology lies in the growth of poly-Si grains with high uniformity and large grain size at the same time.

In summary, the poly-Si TFTs will play an important role in many aspects in the future, especially as the three-dimensional circuit era is coming.

1.2 Laser crystallization technology

The excimer laser annealing (ELA) has been successfully used on LTPS production lines; however, it suffers from unstable laser source power and requires high calibration and maintenance cost [16-18]. Also, the process window of lateral growth region that exhibits large grain structure is limited under critical laser energy. This causes ELA technology on production line need to be controlled within vertical growth regime with smaller grain size but higher uniformity. Compared to the ELA technology, solid state laser with Nd:YAG laser source have advantages such as stable laser power and low maintenance fee on AMLCD mass production applications. Many researches have been proposed to use the 2nd harmonic wave of Nd:YAG laser (532-*nm* wavelength) to crystallize the a-Si film [19-21]. Most papers discuss the large lateral grains produced by low-power continuous-wave Nd:YAG laser [19-21]. However, rectangular grain size causes device deviation when different current flow directions are designed on the same substrate. To overcome these problems, high power Nd-YAG pulsed laser is proposed.

1.3 Motivation

As mentioned in section 1.2, many laser crystallization techniques have already been

proposed. Among them, high power Nd-YAG solid state pulsed laser (SSL) has lots of advantages and is more competent than others. However, the characteristics of poly-Si thin film annealed by SSL have not been studied very clearly yet. Therefore, in this paper, we focus on SSL annealing technique in several aspects such as thin film property, crystallization mechanism, devices performance and so on. At the same time, the conventional excimer laser annealing is used as a comparison. We also conduct a research on the a-SiGe thin film due to its better light absorption at 532-*nm* wavelength. Because of this feature, a-SiGe thin film maybe employed to construct the active layer directly or the light absorption enhanced layer to improve crystallization in the future.

In addition to fundamental crystallization mechanism and device characteristics, the mobility model is also developed. The mobility which can represent carrier transport is a substantial parameter in poly-Si TFTs. Thus, we aim to build a new mobility model directly through the thin film property rather than numerous fitting parameters. Eventually, a physically-based analytical mobility model, and accordingly a new *I-V* model are established. Professional validations are found between calculated results and experimental data for devices with several channel lengths at various temperatures.

1.4 Thesis Outline

This thesis is organized into the following manner.

In chapter 1, a brief overview of poly-Si TFT for various kinds of applications is introduced. Then, we will describe several popular laser crystallization technologies because they seem to be very promising to fulfill low temperature polycrystalline silicon (LTPS). Finally, the motivation of this work will be expressed.

In chapter 2, we give experimental procedures for both a-Si and a-SiGe. In addition, several thin film characterizing techniques containing material and electrical aspects are described. We also introduce the methods to measure or extract the typical parameters

including threshold voltage, mobility, subthreshold swing and thermal activation energy of turn-on region.

In chapter 3, the discussion is divided into three parts: First, we investigate and give clear definition of the crystallization mechanism of the high power Nd:YAG pulsed laser and process window to obtain large and uniform grains. The device performance and material analysis are also demonstrated in this section. Second, the crystallization of a-SiGe is carefully studied. Third, we focus on 50-*nm*-thick active layer for further analysis of electrical property and establishment of mobility model. We consider three different channel lengths which are 6 μm, 12 μm and 30 μm with fixed channel width as 6 μm for three kinds of laser energy densities. Comparisons between simulated and measured data are demonstrated and discussed. In the end, a new mobility model considering not only grain boundary barrier effect but also phonon lattice scattering effect has been established and implemented into the device *I-V* model.

In chapter 4, the conclusions are given.

Chapter 2

Experimental Procedures

2.1 a-Si thin film re-crystallization and poly-Si TFTs fabrication

2.1.1 Laser annealing system

In my experiment, there were two different laser annealing systems. One was typical excimer laser annealing (ELA) system with 308 *nm* wavelength and the other was solid state green laser (SSL) with 532 *nm* wavelength. The former system had large beam size which was 300 *m* × 0.4 *mm* and maximum of laser power was equal to 1 *J*. Additionally, the beam profile of ELA was flat top with pulse frequency as 300 *Hz*. The latter one with high power (up to 175 *W*) Nd:YAG (2ω) laser source, long line beam with beam length as 105 *mm* can be produced. In the sort-axis direction, the beam profile had Gaussian-like energy distribution with the Full Width at Half Maximum (FWHM) as 40 *μm*. Its Gaussian-like beam profile was a great advantage because it was much easier to induce lateral crystallization compared to typical ELA system. Besides, the scan pitch can be varied from 1 *μm* (overlap 97.5%) to 30 *μm* with repetition rate as 4 *kHz*. Although the beam size of SSL was much smaller than ELA, its high repetition rate can make the throughput to be comparable to ELA in mass production.

2.1.2 Device Fabrication

In this study, we fabricated the devices with standard top-gate structure. The schematic device structure was showed in Fig. 2-1. There were two laser annealing techniques to re-crystallize the a-Si thin film, so we fabricated devices in two groups. Except the re-crystallization step, other process steps were identical.

Firstly, in order to prevent the impurity contamination from glass substrate, we deposited double layers which were nitride and oxide film on it as the buffer layer, then followed by the

deposition of 50-*nm*-thick a-Si film by plasma enhanced chemical vapor deposition (PECVD). After dehydrogenization, the a-Si film was put into the laser process chamber and pumped down to 10^{-2} *Torr* following with nitrogen purging to 1 *atm*. Then, samples were irradiated by the solid-state laser with laser energy density varying from 277 mJ / cm^2 to 691 mJ / cm^2. The illustration diagram of laser annealing was demonstrated in Fig 2-2. On the other hand, some samples were annealed by excimer laser with the process condition as the comparison. Subsequently, for both two groups, the active region was patterned and 100-*nm*-thick oxide was deposited by PECVD to serve as the gate insulator. Afterward, the metal gate electrode was deposited and patterned. Devices with various channel lengths and widths were designed on the same mask. The device channel length varied from 4 μm to 30 μm when the channel width was fixed to 6 μm. After implantation was carried out, dopant activation was done by rapid thermal process. Finally, we deposited the metal pad and the passivation layer.

2.2 a-SiGe thin film re-crystallization by SSL

2.2.1 UHVCVD system

The Ultra high vacuum chemical vapor deposition (UHVCVD) system was first proposed by Meyerson in 1985 and was originally designed for the purpose of low temperature growth of Si and $Si_{1-x}Ge_x$ alloys [22]. It was well known that high quality $Si_{1-x}Ge_x$ thin film can be obtained under low growth temperature. Besides, the super clean deposition environment was another giant advantage of UHVCVD system because of less impurity contamination compared to conventional LPCVD. Therefore, it was a promising technique to acquire good $Si_{1-x}Ge_x$ alloys at low deposition temperature.

A homemade UHVCVD system was utilized to deposit $Si_{1-x}Ge_x$ thin films in my experiment. The schematic diagram of UHVCVD system was shown in Fig. 2-3. This system consisted of a load-lock chamber and a growth chamber. The former was made of stainless steel while the latter was a quartz tube of 6-*inch* in diameter. These two chambers were

connected by a gate valve and pumped down respectively by their own turbo and mechanical pumps. The base pressure in the growth chamber was maintained at around 2×10^{-8} *Torr* which comprised O_2 and H_2O less than 10^{-9} and 5×10^{-9} *Torr*, separately. In the standby state, the quartz tube temperature was maintained at about 500 ℃. The flow rates of the gases were controlled by their own mass flow controllers (MFC). Pure disilane (Si_2H_6) and germane (GeH_4) were used as the source gases for Si and Ge, respectively. Each MFC was connected to the computer for a flexible process control via automation.

2.2.2 Deposition and crystallization of a-SiGe thin film

First, we deposited nitride and oxide thin film as the buffer layer on the 4 *inch* glass substrate. Before depositing a-SiGe, we cleaned samples by using ultra sonic vibrator with acetone, IPA and DI water in order and then were blown dry with nitrogen gas. Second, we put wafers on a quartz boat inside the loading chamber and pumped down to around 8×10^{-6} *Torr*. When approaching close to limit pressure, the gate valve was open and samples were loaded into process chamber via a magnet-coupled transfer rod and baked for 1 hour at 450 ℃ before following deposition. Pre-baking step can reach stable heat equilibrium between samples and the quartz tube. It was a necessary step to deposit uniform a-SiGe thin film.

In order to analyze the influence of Ge concentration on thin film property including light absorption and crystallization mechanism, we deposited high quality a-SiGe alloys with two different Ge concentrations by decomposing semiconductor purity source gases disilane (Si_2H_6) and germane (GeH_4). Each Ge concentration had its own deposition recipe. For high Ge concentration (sample A), flow rates of Si_2H_6 and GeH_4 were 7.5 and 5 *sccm*, respectively. During deposition, both temperature and pressure were kept at 390 ℃ and about 110 *mmTorr*, respectively for 4.5 hours. For low Ge content (sample B), flow rates of Si_2H_6 was still fixed as 7.5 and that of GeH_4 is changed to 3 *sccm*. The thin film was deposited at a temperature of 410 ℃ under pressure of 100 *mmtorr* for 4.5 hours. After a-SiGe thin film deposition,

irradiation of solid state laser on samples had been implemented with laser energy density which varied from 277 mJ / cm^2 to 645 mJ / cm^2 and scan pitch was fixed to 2 μm in a clean chamber. The chamber was pumped down to 1×10^{-2} *Torr* and then filled with nitrogen to 1 *atm* before laser annealing.

2.3 Material analysis of thin film

In this section, we briefly introduced several experimental techniques adopted in this work to characterize the material and electrical properties of the thin film.

In parallel to the device fabrication, thin film properties with various laser annealing conditions were first analyzed by the HR800 Micro-Raman system and the scanning electron microscopy (SEM).

The HR800 Micro-Raman system which was manufactured by Jobin-Yvon Corporation was used to characterize the thin film property, such as crystallinity, crystal quality and so on. It consisted of an Olympus BX-41 confocal microscope, a Raman spectrometer, and a liquid nitrogen cooled CCD detector. The laser beam (at 488 *nm*) from Coherent Innova 90C-A6 multiline visible laser, and reflected by five UV mirrors. After passing the interference filter, the laser beam was guided into the microscope and focused by the objective lens, with the spot size on the sample about 2 μm. The Raman signals from the sample and the laser signals reflected by the sample were both collected by the objective lens. However, after the notch filter, only the Raman signal passed into the Raman spectrometer with the spectral solution better than 0.4 cm^{-1}. Finally, the dispersed Raman signals were collected by the CCD detector.

The average grain size was determined by top view image of scanning electron microscopy (SEM) after secco etching. We also observed cross section view of sample by SEM to verify thickness and interface situation of thin film.

On the other hand, the optical property of thin film was investigated by ultraviolet-visible (UV-VIS) spectrophotometer (Perkin Elmer Lambda 650) and n-k analyzer.

The former was used to measure the transmittance, and the latter can obtain reflectance both from 300 to 700 *nm* wavelength. After some numerical calculation, the light absorption of thin film can be determined.

For device electrical performances, they were measured by HP 4156A semiconductor parameter analyzer with source grounded under several temperatures and several important parameters were extracted from the measured data, such as mobility, threshold voltage, subthreshold swing, activation energy and so on. Except *I-V* measurement, we also analyzed *C-V* characteristics of devices by HP 4284.

2.4 Methods of device parameter extraction

2.4.1 Determination of field effect mobility

Typically, the field effect mobility, μ_{FET} was determined from the transconductance, g_M at low drain bias. The transfer characteristics of poly-Si TFTs were similar to those of conventional single crystalline MOSFETs, so the first order *I-V* relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FET} C_{OX} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \qquad (2\text{-}1)$$

Where C_{OX} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length, and V_{th} is the threshold voltage. If V_D is much smaller than V_G-V_{th} (i.e. $V_D << V_G$-V_{th}) and $V_G > V_{th}$, the drain current can be approximated as:

$$I_D = \mu_{FET} C_{OX} \frac{W}{L}(V_G - V_{th})V_D \qquad (2\text{-}2)$$

The transconductance is defined by

$$g_M = \frac{\partial I_D}{\partial V_G}|_{V_D=const.} \qquad (2\text{-}3)$$

From Eq.(2-2), we find the transconductance to be

$$g_M = \frac{W}{L} C_{OX} \mu_{FET} V_D \qquad (2\text{-}4)$$

Thus,

$$\mu_{FET} = \frac{L}{C_{OX} W V_D} g_M$$

2.4.2 Determination of threshold voltage

Plenty ways were used to determine the threshold voltage which was the most important parameter of semiconductor devices. Here, the method to determine the threshold voltage was the constant current method that the voltage at a specific drain current I_N was considered as the threshold voltage. This method was adopted in most research of poly-Si TFTs. Compared to the threshold voltage obtained by the complex linear extrapolation method, it was more efficient to get the threshold voltage of the device and the value was close to the former one. In general, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ was specified at 10 nA for $V_D = 0.1$ V and 100 nA for $V_D = 5$ V in most papers to extract the threshold voltage of TFTs.

2.4.3 Determination of Subthreshold Swing

Subthreshold swing $S.S$ (V / dec) was a typical parameter to describe the control ability of gate toward channel which was the turn on / off speed of a device. It was defined as the amount of gate voltage required to increase / decrease drain current by one order of magnitude.

In this study, the subthreshold swing was defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude. The threshold current was specified to be the drain current when the gate voltage was equal to threshold voltage.

2.4.4 Extraction of thermal activation energy of turn-on region

The activation energy (E_a) of turn-on region that stood for grain barrier height (E_B) of thin film for carrier transporting is a very important parameter. In my experiment, the

activation energy (E_a) of the on current was extracted from the slope of Arrhnius plot (Fig. 2-4) of drain current. The data which was taken over a temperature range from 298 *K* to 343 *K*, followed a straight line. This method can achieve accurate determination of E_a.

Chapter3

Results and Discussions

3.1 Crystallization mechanism by SSL

3.1.1 Thin film analysis

We have several a-Si thin film with different thickness which varies from 50-*nm* to 150-*nm*. The typical active layer thickness of poly-Si TFTs is usually 50-*nm*, so we focus on 50-*nm* a-Si to investigate the crystallization mechanism by SSL annealing.

Fig. 3-1 shows the SEM images of poly-Si films after solid-state laser (SSL) annealing with laser energy density varies from 392 mJ / cm^2 to 645 mJ / cm^2. We can find the relationship between the average grain sizes and laser energy density. As the laser energy density increases, the average grain size goes up till reaching the maximum average grain size when the laser energy density is 484 mJ / cm^2. Between laser energy density of 484 mJ / cm^2 to 553 mJ / cm^2, the grain structures and the average grain sizes are very similar. Then, over specific laser energy, the fine grain region appears.

In order to further characterize the crystalline quality of these poly-Si films, their Raman peak positions and FWHM are compared in Fig. 3-2 [23, 24]. Since the Raman peak of single crystalline silicon is located at 520.8 cm^{-1}. It is known that when the Raman peak position approaches 520.8 cm^{-1} indicating that the crystalline quality gets more similar to the single crystalline. Also, the smaller the FWHM is, the better the crystal quality is. In Fig. 3-2, the FWHM curve becomes smaller with increasing laser energy density in lower laser energy density region. In higher laser energy density region, on the contrary, it increases as the laser energy density increases. The lowest FWHM value and the highest peak position approximately locate between the laser energy density from 484 mJ / cm^2 to 553 mJ / cm^2. This corresponds well to the analysis results of SEM images.

3.1.2 Crystallization Mechanism

From the above statements, we can propose three regions in the crystalline mechanism. As illustrated in Fig. 3-3, three regions named vertical crystallization (VC), super lateral crystallization (SLG) and fine grain (FG) regions are divided by two specific laser energy. The first is the critical energy (E_c) that stands for the laser energy to fully melt the a-Si film. The second is the fine-grain energy (E_{fg}) that stands for the minimum energy to cause the fine grain structure. Three regions will be further described as follows.

In region Ⅰ, the laser energy is not high enough to completely melt the a-Si film. As a result, the nucleation sites are located at the boundary between melted Si film and the bulk a-Si film. Vertical growth dominates the crystallization mechanism and gives rise to small grain structure. The grain size increases as the melted zone increases along with increasing laser energy density. The scan pitch also influences the grain size in this VC region. As shown in Fig. 3-4, the SEM images of poly-Si films annealed by the same laser energy density but different scan pitches are compared. When the scan pitch decreases, the grain size becomes larger. This is due to the increase of laser beam overlap and also the increase of melted Si zone. In other words, the absorbed energy per unit area of the Si film is increased when the scan pitch decreases.

In region Ⅱ, named the SLG region, grain size becomes large when the laser energy exceeds the critical energy (E_c). In this region, a-Si film is fully melted. Nucleation happens at the cooling boundary produced by the Gaussian-distributed laser beam profile. Super lateral crystallization dominates the crystal mechanism. In this region, the grain size is not dependent on the laser energy obviously. It is plausible that reducing the beam profile slope can further increase the grain size. However the verification is still beyond our facility. It is also worthy to note that the critical energy E_c increases from around 461 mJ/cm^2 to 553 mJ/cm^2 when the a-Si film thickness increases from 50 nm to 100 nm. This corresponds to the proposed critical energy concept that causes the a-Si film fully-melted.

In region Ⅲ, the laser energy exceeds the second specific laser energy which is the fine grain energy (E_{fg}). Fine grain areas next to the large grain areas start to appear. We will see in the later discussion about device performance that the fine grain areas degrade device performance tremendously whereas the existence of large grain areas. Since the slope of the Gaussian profile increases when we enlarge the peak laser energy. It is plausible that the fine grain areas are caused by the large cooling rate. Further evidence can be found when comparing the SEM images of poly-Si films annealed at the same laser energy but different scan pitches as in Fig. 3-5. Obviously when scan pitch increases from 2 μm to 5 μm, fine grain areas appear due to the increased cooling rate. Large cooling rate produces areas where temperature variation is very large. In these specific areas, many nucleation sites appear simultaneously and form the fine grain structure.

3.1.3 Device Performance

Typical TFT devices fabricated by using poly-Si films with different SSL annealed conditions are compared in this section. In Fig. 3-6(a), the relationship between field-effect mobility and SSL annealed laser energy density is depicted. The threshold voltage and the subthreshold swing as a function of the SSL annealed laser energy are also compared in Fig. 3-6(b). The annealing scan pitch is fixed to be 2 μm. The device channel width and length are 6 μm and 12 μm, respectively. Indeed, the device parameters such as the field-effect mobility, the threshold voltage and the subthreshold swing are well correlated to material analysis results including Raman spectrum and SEM image.

Apparently the best device performance locates between the annealed laser energy density from 484 mJ / cm^2 to 553 mJ / cm^2, which is exactly the same window as the SLG region proposed in the above discussions. In the SLG region, the field effect mobility around 250 cm^2 / Vs and the threshold voltage lower than 1 V can be obtained. Compared to conventional ELA technology, the large process window for SLG region in this Nd:YAG

annealing system is a very great advantage. It is also proposed that better device performance, larger grain size and larger SLG process window could be achieved if the slope of the laser beam profile becomes smaller in the peak area.

3.1.4 Process Window Definition

In the section 3.1.2, in order to separate three different regions and their own crystallization mechanism, we define two energies, E_c (the energy density that the grain starts to laterally grow) and E_{fg} (the energy density that fine grain region starts to appear), respectively. There are several factors that will affect the value of E_c and E_{fg}. E_c is affected by three major factors: the green laser absorption of a-Si film (depends on a-Si film thickness), laser energy and scan pitch. The higher green laser absorption or higher laser energy density will lead E_c to lower laser energy. On the other hand, E_{fg} will be influenced mainly by cooling rate and scan pitch. As the cooling rate is fast or scan pitch becomes larger, E_{fg} will become higher laser energy.

The SLG process window can be defined between E_c and E_{fg}. For example, for devices with 50-*nm* active layer, their output characteristics become excellent while the active layer is annealed by laser with energy density from 484 mJ / cm^2 to 553 mJ / cm^2 and scan pitch as 2 μm. Within this process window, the device performance is good and uniform. With typical top-gate structure, the field effect mobility can be larger than 250 cm^2 / Vs, and the threshold voltage can be lower than 1 V. Unlike ELA laser crystallization, this Nd:YAG laser with Gaussian beam profile provides large process window for the super lateral growth (SLG) crystallization regime on a-Si thin film.

For further study of the process window, we also examine the device performance on different thickness of active layer. Fig. 3-7, there is electrical property of 100-*nm* active layer and we can obviously find that SLG region which varies only from 553 mJ / cm^2 to 576 mJ / cm^2 is much narrower than that of 50-*nm* active layer. The E_c of 100-*nm* active layer is higher

than that of 50-*nm* active layer because of poorer absorption of laser irradiation energy. On the other hand, about the interval between E_{fg} and E_c, 100-*nm* active layer is smaller than 50-*nm* active layer due to its faster cooling rate. This result confirms to our above process window definition very well.

3.1.5 Comparison between SSL and ELA

In this work, we also prepare some sample annealed by conventional ELA system as the comparison. Here, we will focus on active layer as 50-*nm* and discuss the difference between two laser annealing techniques in several aspects including the grain size, crystal quality and device performance. The Raman peak positions and FWHM versus laser energy density of 50-*nm* Si annealed by ELA are showed in Fig. 3-8. The lowest FWHM value and highest Raman peak position occurs corresponding to laser energy density which varies from 380 mJ / cm^2 to 400 mJ / cm^2. For ELA (Fig. 3-8) and SSL (Fig. 3-2), the smallest FWHM value is around 5.14 cm^{-1} and 4.63 cm^{-1} respectively and the Raman peak position is located at wavenumber about 516.49 cm^{-1} and 517.27 cm^{-1}, individually. Therefore, based on these facts, it can be inferred that SSL has the better crystal quality and its crystalline is more similar to single crystal silicon than ELA.

The SEM images after secco etching of 50-*nm* a-Si annealed by ELA and SSL at each process laser energy density are shown in Fig. 3-9. We can apparently recognize that the average grain size of ELA is only about 0.3 μm while that of SSL is around 1 μm which is approximately three times larger than the former. Thus, it is a further evidence to prove that SSL is superior to ELA not only in the grain quality but also in the grain size.

At the same time, we also inspect the device performance of ELA for more detail analysis. In Fig. 3-10, there is the comparison of typical transfer characteristic for n-channel poly-Si TFTs annealed by ELA and SSL at each process laser condition and the several important parameters are collected in Table Ⅰ for comparison. It obviously indicates that SSL

has higher mobility, lower threshold voltage and lower subthreshold swing. The result of electrical property is consistent with previous material analysis data. Hence, we can conclude that SSL is preferable to ELA in many aspects and has great chance to play an important role in the next generation.

3.1.6 Discussion of a-SiGe crystallization

In addition to a-Si thin film, we also investigate crystallization of a-SiGe thin film. As mentioned in section 2.2.2, there are two kinds of a-SiGe thin film which are called as sample A (high Ge content) and sample B (low Ge content). The light absorption versus wavelength of a-Si and a-SiGe thin film is depicted in Fig. 3-11. A-Si has the largest light absorption at 532 *nm* wavelength and sample A is slightly lower than a-Si, whereas sample B absorbs the far less light than a-Si and sample A. It infers that higher Ge content of a-SiGe thin film has a better absorption at 532 *nm* wavelength and is comparable to a-Si.

On the other hand, a-SiGe thin films annealed by SSL with different laser energies are characterized as well. Fig. 3-12 shows typical Raman spectra obtained on a-SiGe thin film before and after laser irradiations performed in different conditions. Before annealing, the Raman spectrum is composed of broad bands located at around 250 and 400 cm^{-1}. These two components are characteristic of an amorphous system. After laser irradiation, the presence of the three prominent peaks shows that re-crystallization has occurred, through a laser induced melt-re-growth process, but with significant differences with respect to their laser energies and relative intensities. We observe that Raman intensity increases and FWHM decreases with increasing laser energy until reaching a maximum. When exceeding the critical laser energy, Raman intensity begins to decrease immediately. This behavior is similar to crystallization mechanism of a-Si. According to the smallest FWHM value of $Si_{1-x}Ge_x$ alloy which means the best crystal quality, the best laser energy for sample A and sample B is about 110 *W* and 125 *W*, respectively. Furthermore, re-crystallization of sample A appears at lower

laser energy than sample B. It indicates that the higher Ge content of a-SiGe thin film requires lower threshold energy to re-crystallize. This is consistent with above light absorption results. Moreover, the quality of poly-SiGe annealed by SSL at optimum laser condition is close to single crystal $Si_{1-x}Ge_x$ [25]. Thus, we probably can use poly-SiGe directly as the active layer to replace poly-Si in the future due to its higher hole mobility.

3.2 Mobility modeling of poly-Si TFTs by SSL

3.2.1 Two main mechanisms affecting mobility

For poly-Si TFTs, there are two main mechanisms which affect mobility. One is activation energy, *Ea*, which stands for the energy barrier height (E_B) on grain boundary and the other is phonon lattice scattering. At the small gate voltage bias, the barrier height is still large and has strong influence on the mobility. The carrier transports crossing the grain boundary by thermionic emission, so the mobility will increase when the temperature increases. On the contrary, at the larger gate voltage bias, the barrier height on the grain boundary is almost suppressed by gate induced charges. Thus, the dominated mechanism of mobility is changed to phonon lattice scattering and mobility will decrease with increasing temperature. In fact, the phonon lattice scattering effect is also observed in single crystalline silicon.

Fig. 3-13 shows the mobility versus gate voltage at several temperatures varying from 298 *K* to 343 *K*. Indeed, we easily discover that mobility becomes larger as the temperature is getting higher at small gate voltage bias and that mobility decreases with increasing temperature at larger gate voltage bias. This result presents the same trend as the discussion in previous paragraph even in the case of different channel lengths.

In order to separate two mainly dominated mechanisms, we divide gate voltage into two regions by a critical voltage (V_c). The gate voltage behind V_c is called as region A and the gate voltage above V_c is defined as region B. The mobility at V_c is independent of temperature.

Besides, we also investigate the grain barrier height (E_B) versus gate voltage in Fig. 3-14. It exhibits an interesting and crucial phenomenon that E_B at V_c is close to 0.026 eV which is the thermal voltage multiplied by electron charge for different channel geometry. Furthermore, if gate voltage exceeds V_c, E_B will no longer have a great effect on the mobility. Hence, the primary mechanism is replaced by phonon lattice scattering. This meaningful fact leads V_c to be an essential parameter to distinguish what the dominated mechanism of mobility is.

However, if the laser energy density is getting lower than the ideal condition, the grain size will reduce noticeably. When the grain size is too small and the number of grain boundaries becomes relatively large, the phonon lattice scattering intra the grain will almost relieve. In this case, as shown in Fig. 3-15, the mobility at large gate voltage bias is primarily influenced by grain boundary barrier rather than phonon lattice scattering. Therefore, the lower laser energy is, the slighter the lattice scattering is.

3.2.2 Modeling equation and Physical meaning

In poly-Si TFTs, not all charge carriers induced in the channel by the gate voltage will be free to contribute to the drain current. Instead, a significant of the carriers will be captured by traps associated with the grain boundaries, especially near and below threshold. M. Jacunski et al. propose an appropriate mobility model to take this effect into account and the equation is expressed as: [26]

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_1 \left| \frac{2V_{gte}}{\eta V_{th}} \right|^{m_u}} + \frac{1}{\mu_0} \qquad (3\text{-}1)$$

where m_μ, μ_0 and μ_1 are extractable mobility parameter.

Unfortunately, this model is not valid when temperature changes. Because of this reason, the above formula fails to precisely describe the behaviors of carrier mobility.

Recently, Apostolos T. Voutsas propose another mobility model which is given as: [27]

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_{SIMOX}} + \frac{1}{\mu_{Defect}} + \frac{1}{\mu_{GB}} \qquad (3\text{-}2)$$

where μ_{app} is the measured mobility, μ_{SIMOX} is the equivalent SIMOX mobility accounting for lattice scattering, μ_{Defect} is a mobility term attributed to defect-scattering and μ_{GB} is a mobility term attributed to grain-boundary scattering. However, this model is complicated to use because of too many fitting parameters. Therefore, we propose a physically-based mobility model including temperature variation effect by using only few fitting parameters.

In section 3.2.1, we have given the definition for two regions which are separated by V_c and explained the mechanism of each region clearly. After acquiring the valuable information, we can proceed to derive two formulas that can more accurately represent the mechanism of each region. A complete physically-based mobility model can then be built precisely.

In region A, the mobility is dominated by grain barrier height. If we assume that the main conduction mechanism through the grain boundaries is the thermionic emission over the grain boundary energy barrier (E_B), the equation is generally written as:

$$\mu_{GB} = \mu_f \exp(\frac{-E_B}{kT}) \qquad (3\text{-}3)$$

where

μ_f is electron mobility in the intra-grain region,

μ_{GB} is electron mobility in the grain boundary region,

E_B is energy barrier at the grain boundary,

k is Boltzmann constant.

However, during our experiment, we learn that the above formula can be refined to address the significance of grain and grain boundary size. In our attempts to analyze the relationships between the field effect mobility and the grain size, we notice a linear relationship between the two. Fig. 3-16 shows the mobility versus grain size at various low gate voltage biases for different channel lengths where the average grain size of different

laser energy is defined from their SEM images as in Table Ⅱ. The similarly linear relationships are apparently found in all devices. Therefore, we improve the Eq. (3-3) by including a new term L_G / L_{GB} to describe the effect of grain and grain size on carrier mobility. Fig. 3-17 is the illustration diagram for equation derivation. We make an assumption that the whole film is composed of identical grains and grain boundaries in periodical structure. Furthermore, we consider each of them as an equivalent resistance and combined them by the Ohmic's Law. The derivation is provided below:

$$R_{ch} = \frac{L}{L_G} R_f + \frac{L}{L_G} R_{GB}$$

$$= \frac{L}{L_G} \frac{L_G}{\mu_f nqt_{ch} W} + \frac{L}{L_G} \frac{L_{GB}}{\mu_{GB} nqt_{ch} W}$$

$$= \frac{L}{Wnqt_{ch}} \left(\frac{1}{\mu_f} + \frac{1}{\frac{L_G}{L_{GB}} \mu_{GB}} \right)$$

$$I_D = \frac{V_D}{R_{ch}} = V_D \frac{W}{L} qnt_{ch} \left(\frac{\mu_f \mu_{GB} \frac{L_G}{L_{GB}}}{\mu_{GB} \frac{L_G}{L_{GB}} + \mu_f} \right) = JWt_{ch} = \sigma \frac{V_D}{L} Wt_{ch}$$

$$J = \frac{V_D}{L} \times qn \left(\frac{\mu_{GB} \frac{L_G}{L_{GB}}}{1 + \frac{\mu_{GB}}{\mu_f} \frac{L_G}{L_{GB}}} \right)$$

$$\mu_{eff} = \frac{\mu_{GB} \frac{L_G}{L_{GB}}}{1 + \frac{\mu_{GB}}{\mu_f} \frac{L_G}{L_{GB}}} = \frac{\mu_{GB} \frac{L_G}{L_{GB}}}{1 + \frac{L_G}{L_{GB}} \exp(\frac{-E_B}{kT})} \approx \mu_{GB} \frac{L_G}{L_{GB}} = \frac{L_G}{L_{GB}} \mu_f \exp(\frac{-E_B}{kT}) \qquad (3\text{-}4)$$

where

μ_f is electron mobility in the intra-grain region,

L_G is average grain length,

L_{GB} is average grain boundary length.

In region B, the mobility is dominated by phonon lattice scattering and in general the

equation is given as:

$$\mu_{scattering} = \mu_{T0} \cdot \left(\frac{T}{T_0} \right)^b \tag{3-5}$$

where

T_0 is the room temperature which equals to 298 K,

b represents the magnitude of temperature dependence. The value of single crystalline Si is -3/2. When approaching to this value, it means that the crystal quality intra the grain is getting closer to single crystalline Si.

After deriving mobility equations of region A and B, we take the inverse of each term and the complete mobility model can be written as:

$$\frac{1}{\mu_{cal}} = \frac{1}{\mu_{eff}} + \frac{1}{\mu_{scattering}} = \frac{1}{\frac{L_G}{L_{GB}} \mu_f \cdot \exp(\frac{-E_B}{kT})} + \frac{1}{\mu_{T0} \cdot \left(\frac{T}{T_0} \right)^b} \tag{3-6}$$

3.2.3 Mobility Fitting Results

We adopt our proposed mobility model in Eq. (3-6) to fit the measured mobility of devices with different channel geometries and laser annealing conditions at a temperature range which varies from 298 K to 343 K. There are total three laser annealing conditions and three channel lengths while channel width fixed as 6 μm. The fitting procedure is described as below:

First, μ_{GB} / L_{GB} can be obtained from the slope of mobility versus grain size figure at low gate bias (region A) around 1.5 V and we use measured E_B to determine μ_f / L_{GB} value. After L_G is given, μ_{eff} is decided simultaneously. Then, we fix μ_{eff} and fit mobility versus various temperatures at larger gate bias (region B) via using $\mu_{scattering}$ equation by two fitting parameters, μ_{T0} and b. Finally, the calculated mobility will be obtained. The several important fitting parameters are listed in Table Ⅲ.

All of the results are showed from Fig. 3-18 to Fig. 3-26. Consequently, improved mobility model shows excellent agreement over wide range of gate bias voltages and the calculated and experimental results are considerable matched in all devices. It clearly indicates that this mobility model is suitable for using in the channel length varying from 30 μm to 6 μm at a temperature range varying from 298 K to 343 K.

3.2.4 Output Characteristics

In addition, we also aim to simulate the output characteristics of devices in order to further confirm the accuracy of our proposed mobility model.

Generally, above threshold, the drain current (I_D) is given by [27]

$$I_D = \mu_{cal} C_{OX} \frac{W}{L}[(V_G - V_{th})V_{DSe} - \frac{V_{DSe}^2}{2\alpha_{sat}}] \quad (3\text{-}7)$$

where

W is the channel width,

L is the channel length,

V_{th} is the threshold voltage,

α_{sat} accounts for velocity saturation, which reduces the value of the saturation voltage as the channel length is decreased.

For simplicity, the model for all regimes of operation should be combined into a single expression which is everywhere continuous and smooth. This is accomplished by defining effective drain voltages as [26]

$$V_{DSe} = \frac{V_{DS}}{[1 + (\frac{V_{DS}}{V_{sat}})^m]^{\frac{1}{m}}} \quad (3\text{-}8)$$

V_{DSe} is approximately V_{DS} for $V_{DS} < V_{sat}$, but remains constant at V_{sat} in saturation; m is a fitting parameter that controls the transition from V_{DS} to V_{sat}.

On the other hand, we also use C-V measurement to identify which gate voltage is

corresponded to strong inversion. This specific gate voltage can be regarded as on voltage (V_{on}) which represents strong inversion appeared and means that the device really turned on. Moreover, we also extract Von from transfer characteristics of device by using $G_{M,max}$ tangent method. We find out the $G_{M,max}$ first and then do tangent at that point to find the intersection of x-axis. The value of V_{on} extracted from this method is almost the same to *C-V* method. The *C-V* characteristics and transfer characteristics of devices annealed by different laser energies are put together as shown in Fig. 3-27. The threshold voltage and on voltage with their corresponding grain barrier height at 298 *K* with different channel geometries and laser powers are listed in Table Ⅳ. Although both the value of V_{th} and V_{on} are different for each device, their corresponding grain barrier heights are almost the same. It is inferred that grain barrier height is the dominant factor to determine what the value of V_{th} and V_{on} are. Then, we replace the V_{th} in Eq. (3-7) with V_{on} because V_{on} is more appropriate for on current regime simulation.

Consequently, we combine the proposed mobility model in Eq. (3-6) into the *I-V* model in Eq. (3-7). The calculated results and the measured results for devices with several channel geometries and film quality at different temperatures are depicted from Fig. 3-28 to Fig. 3-36. Except some Kink effect appearing in shorter channel length, the validity of the proposed model for three laser annealing conditions within a temperature range from 298 *K* to 343 *K* and channel length varying from 30 μm to 6 μm is demonstrated well. Excellent agreement is found to verify our proposed model.

Chapter 4

Conclusion

In this thesis, first, the poly-Si films annealed by high power solid state Nd:YAG pulsed laser have been analyzed. Poly-Si TFT characteristics with the corresponding poly-Si films are also investigated. It is found that, unlike ELA technology, this laser system provides larger SLG process window. Within the window, the filed effect mobility around 250 cm^2 / Vs and the threshold voltage lower than 1 V can be easily achieved. Along with the advantages such as low maintenance fee and stable laser power, the solid state pulsed laser system is well applicable to fulfill system-on-panel (SOP).

Second, poly-SiGe crystallization is studied as well. We successfully verify that high quality poly-SiGe can be achieved by SSL. In addition, influences of Ge content on threshold laser energy of re-crystallization have been demonstrated. Moreover, due to higher hole mobility of poly-SiGe, we probably can use it directly as the active layer to replace poly-Si in the future.

Finally, we propose a new mobility model including two main mechanisms which are grain boundary barrier and phonon lattice scattering. Most of parameters in our mobility model are extracted by device measurement. Thus, this new model can be directly related to thin film property precisely with only a few fitting parameters. When comparing the measured data and the calculated results, good agreements were found for devices with different channel length and laser annealing conditions. We also demonstrate that this model can provide reliable predictions for mobility variation under various temperatures. Moreover, adopting this mobility model, calculation and measurement of output characteristics match quite well. Hence, this mobility model containing more physical meanings can accurately predict device performance.

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