N型低溫複晶矽薄膜電晶體在閘極交流電壓下的劣化研究

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摘要

複晶矽薄膜電晶體(poly-Si TFT)最近幾年在液晶顯示器(AMLCD)及有機發光二極體(AMOLED)顯示器應用中之所以會是眾所注目的焦點，是因為其優異的元件特性。相較非晶矽薄膜電晶體，複晶矽薄膜電晶體有較高電流趨動能力及較好的可靠度，因此在複晶矽薄膜電晶體顯示器裡，它可以被用來整合畫素電路及周邊驅動電路於同一片玻璃基板上，如此使面板結構簡單化且可以減少週邊半導體零組件的使用數量以及後段模組在組裝時的接點數目，進而提高工程可靠度，除此之外更可降低驅動 IC 成本，維持低耗電特性，提供高精細的畫質表現。所以，複晶矽薄膜電晶體被視為實現系統化面板(System on Panel)的關鍵技術。

然而不同於畫素的薄膜電晶體，在驅動電路上的薄膜電晶體會受到高頻的閘極脈波電壓所驅動。因此，薄膜晶體在交流訊號操作下的劣化機制必須要仔細的探討。

在這篇論文中，我們研究了低溫複晶矽薄膜電晶體在交流訊號下的劣化。假

設劣化的程度會和靠近源極和汲極的橫向電場的大小以及載子數目變化有關。當閘極電壓是從-15V 掃到 15V 時，我們觀察到元件的劣化只會和閘極脈波下降的時間有關，和上升的時間無關。然而，我們第一次觀察到如果閘極電壓範圍都是小於臨限電壓的化，元件的劣化會同時和閘極脈波上升的時間以及下降的時間有關。

我們提出了薄膜電晶體的 Slicing Model，它是考慮了電晶體通道的電阻以及閘極氧化層的電容，來解釋複晶矽電晶體在交流訊號下的劣化。在實驗的數據以及模擬的結果合理的對照之下，劣化的程度真的是會和靠近源極和汲極的橫向電場的大小以及載子數目變化有關。此外，利用模擬的結果引入一個新的指標，它和劣化的程度幾乎是呈正比。

對顯示面板上的周邊電路，NAND 和 NOR 邏輯閘是基本是組成電路。當邏輯閘輸入端 A 和 B 分別為 0 以及 1 時，會出現汲極是浮動的現象。所以會出現新的交流訊號操作情況，稱為浮動汲極的交流操作，我們將在第三章討論。

Study of N-type LTPS TFTs Degradation Under Gate Pulse Stress

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Abstract

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have recently attracted much attention in the application on the integrated peripheral circuits of active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diode (AMOLED) displays. The significant advantages over amorphous silicon (a-Si) TFTs are in the higher current driving capability and the better reliability. In poly-Si TFT-controlled displays, poly-Si TFTs are used to implement pixel circuits and driving circuits on a single glass substrate to reduce system cost and posses compact module. Therefore, the poly-Si TFT is the best candidate to realize system–on–panel (SOP).

However, unlike pixel TFTs, TFTs in driver circuits are subjected to high-frequency voltage pulses. Therefore, the degradation mechanism under dynamic operation should be understood in detail.

In this thesis, the device degradation of low-temperature polycrystalline thin film transistor under AC stress has been investigated. The degree of degradation is concerned with the magnitude of the lateral transient electrical field and the variation of the number of the carriers near the source/drain. For the gate voltage swing of -15V to 15V, it is observed that the degradation depends on the falling time of the gate

pulse but does not depend on the rising time. However, it is firstly observed that the degradation is both dependent of rising time and falling time if the voltage swings below the threshold voltage. TFT's slicing model take channel resistance and oxide capacitance into consideration is proposed to explain the degradation of poly-Si TFTs under Gate Pulse Stress. A reasonable agreement between the experiment data and the simulation results reveals that the degradation is related to the transient electrical field and the various amount of the charge near the edges of the channel. In addition, a new index which can be simulated using a slicing model is proposed and it is almost proportional to the degradation degree.

For the peripheral circuit in poly-Si panel, NAND and NOR logic gates are the fundamental elements. When input terminals A and B of NAND and NOR are 0 and 1, respectively, floating drain TFTs appear. Therefore, a new AC stress condition is needed to discuss, called floating drain AC stress. We will also discuss the phenomenon for poly-Si TFT under floating drain AC stress in the chapter 3.

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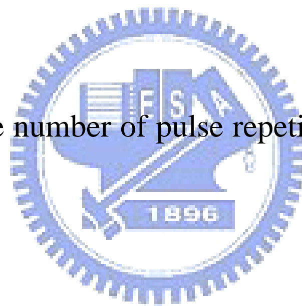

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