Chapter 1
Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In recent years, low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have attracted much attention because they have been used very successfully for active matrix displays, such as active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs). Expect large area displays, poly-Si TFTs have been applied into some memory device such dynamics random access memories (DRAMs), static random access memories (SRAMs), and have great potential for 3-dimention ICs' applications.

Compared to conventional a-Si TFTs, the field-effect-mobility of poly-Si TFTs is much higher. Higher field-effect-mobility means transistor can provide higher driving current. The higher driving currents can allow the pixel-switching element TFT's dimension shrinkage, resulting higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Besides, the superior mobility performance allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry on the same glass substrate, which brings the era of system-on-glass (SOG) that will include a memory, central processing unit (CPU), and display.

The process complexity can be greatly simplified and manufacturing cost can be substantially reduced. The ability of fabricating high-performance LTPS TFTs enables their use in a wide range of new applications. Therefore, there is great interest in improving the performance of LTPS TFTs.

In comparison with signal-crystalline silicon, poly-Si suffers many grain boundary defects and intra-grain defects. The order of poly-Si grain size is about 0.1um. At present, when poly-Si TFTs are used in LCD applications, the minimum feature size is typically much larger than 10μm, and therefore a large number of grain boundaries are present in the channel. Electrons are scattered at the grain boundaries or trapped by the interface states, leading to lower mobility than in single crystal silicon. Much effort has been made to increase the performance of LTPS TFTs. Crystallization of a-Si thin films has been considered the most critical process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrate, and formation of high-quality poly-Si.

From the viewpoint of device technologies, various structural improvements, such as offset gate, lightly doped drain (LDD), multi-gate structure, and gate-overlapped LDD have been proposed. Most of these structures effectively reduce the electric field near the drain junction. Consequently, the anomalous leakage current and kink current of poly-Si TFTs can be effectively reduced accompanying with a promotion of reliability in poly-Si TFTs.

In summary, it is expected that the poly-Si TFTs will becomes increasingly important in future technology, especially when the 3-D circuit integration and SOP era is coming. There are lots of interesting and important topics that are worthy to be researched.

1.2 Motivation

In order to make LTPS TFTs suitable for advanced circuits, besides the improvement of performance of LTPS TFTs, the improvement of reliability is also significant. Therefore, reliability testing and understanding of reliability mechanisms become more and more necessary.

The reliability mechanisms of LTPS TFTs under DC (direct current) bias stress have been widely discussed. However, up to now, the reliability of LTPS TFTs under AC (alternating current) stress has been paid much less attention, shown in Fig. 1-1. At first, in practice, the LTPS TFTs used as switching elements for AMLCDs are operated in an AC mode, thus AC stress is much closer to real operational condition than conventional DC stress. Secondly, unlike pixel TFTs, the TFTs in driver circuits are subjected to high-frequency voltage pulses. Therefore, it is extremely important to understand the degradation mechanisms of LTPS TFTs under AC stress.

In this study, the mobility ratio of n-channel LTPS TFTs under various AC stress conditions, including frequencies, swing range, and falling/rising times, was discussed to verify the degradation mechanism under AC stress.

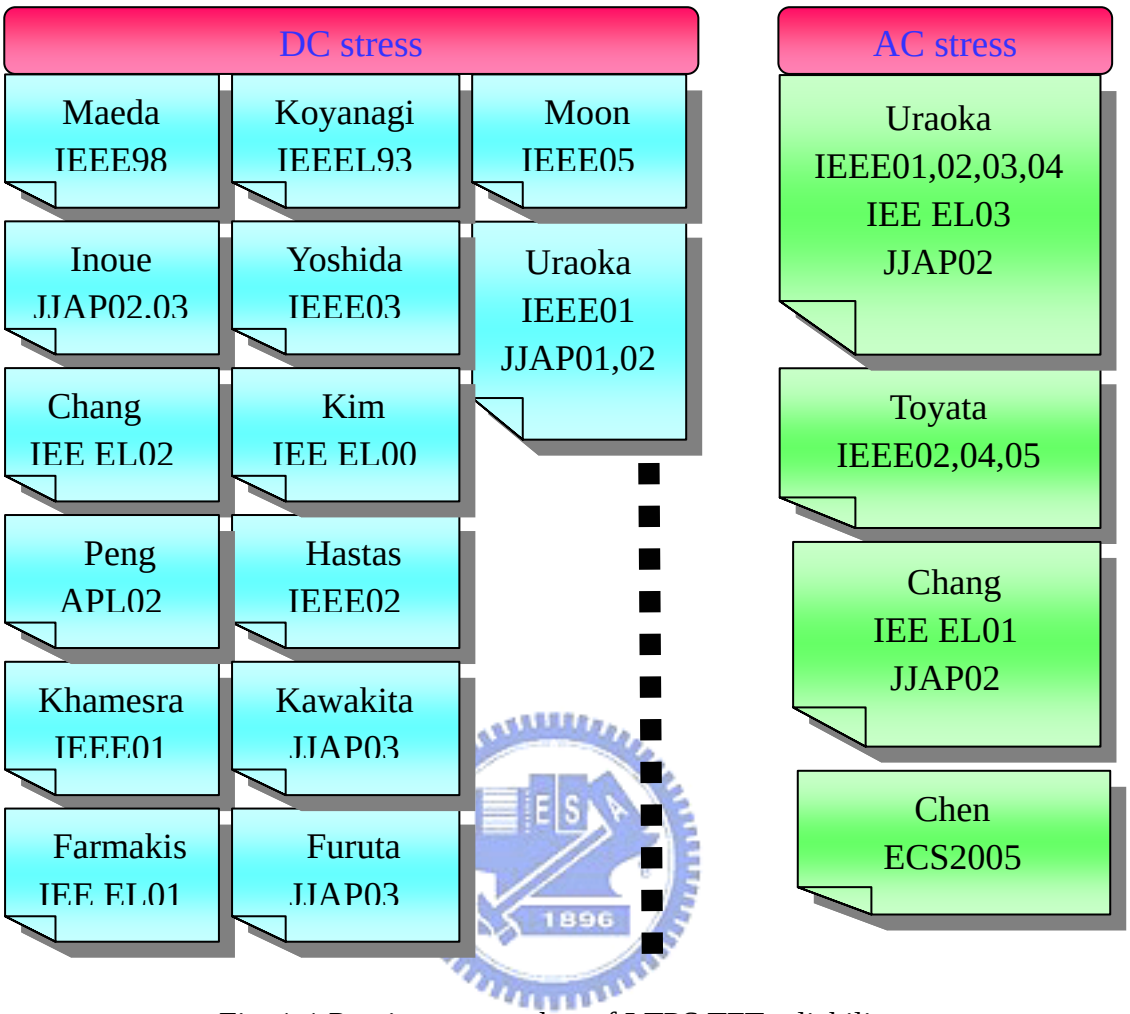

Fig. 1-1 Previous researches of LTPS TFT reliability

1.3 Review of Degradation Model for TFT under AC Stress

In previous reports, Toyota et al. proposed that mobile carriers are able to follow the transient variation of gate voltage while the electrons trapped in the midgap state aren't. In addition, Uraoka et al. attributed the dominant ac degradation mechanism to hot electrons generated by trapped electrons exposed to the high electric field and gain energy from the electric field during ac stress. The mechanism was analyzed by using a picosecond emission microscope and a device simulation to examine the transient current experimentally and theoretically, respectively.

The earlier degradation model under ac stress is described as follow. When the gate voltage is high, the electrons gather to form a channel shown in Fig. 1-2(a). When the gate voltage drops, the electrons in the channel move rapidly to the source and drain shown in Fig. 1-2(b). Some of the trapped electrons are exposed to the high electric field and grain energy from the field. Hot electrons are generated at this moment and form electron traps shown in Fig. 1-2(c), and a density of state (DOS) in tail edge of poly-Si is increased by the hot electrons.

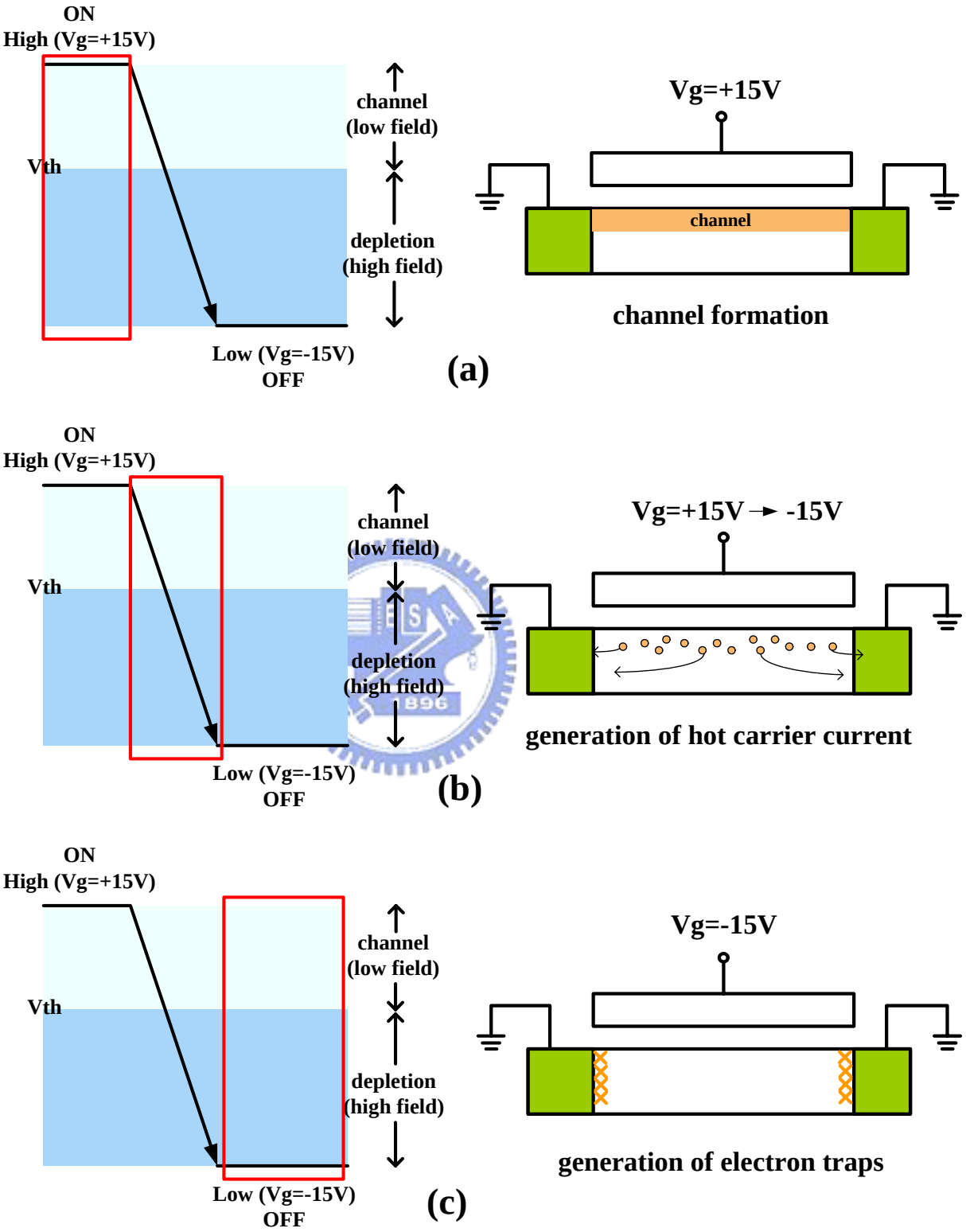

Fig. 1-2 A schematic diagram for degradation model of the poly-Si TFT

1.4 Thesis Organization

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Chapter 2
N-Poly-Si TFT under Gate Pulse Stress with Drain and Source Ground

2.1 Experiments

2.1.1 Procedures of Fabrication of LTPS TFTs

LTPS TFTs used in the experiment were the conventional top-gate structure and fabricated on the glass substrates. The cross-section views of n-channel LTPS TFTs are shown in Fig 2-1. The basic process flow is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates by the PECVD system. Then, XeCl excimer laser was used to crystallize a-Si:H film followed with poly-Si active area definition. Subsequently, gate insulator was deposited by PECVD. The thickness of gate oxide is 650Å. Next, the metal gate formation and source/drain doping were performed. Dopant activation and hydrogenation was carried out after interlayer dielectric deposition. Finally, contact holes formation and metallization were performed to complete fabrication work. The lightly doped drain (LDD) structure was used in the n-channel TFTs to enhance hot carrier endurance. The width/length of the TFT was 20 μm/5 μm. The TFT of the same dimension will be used for reliability testing in the chapter 3.

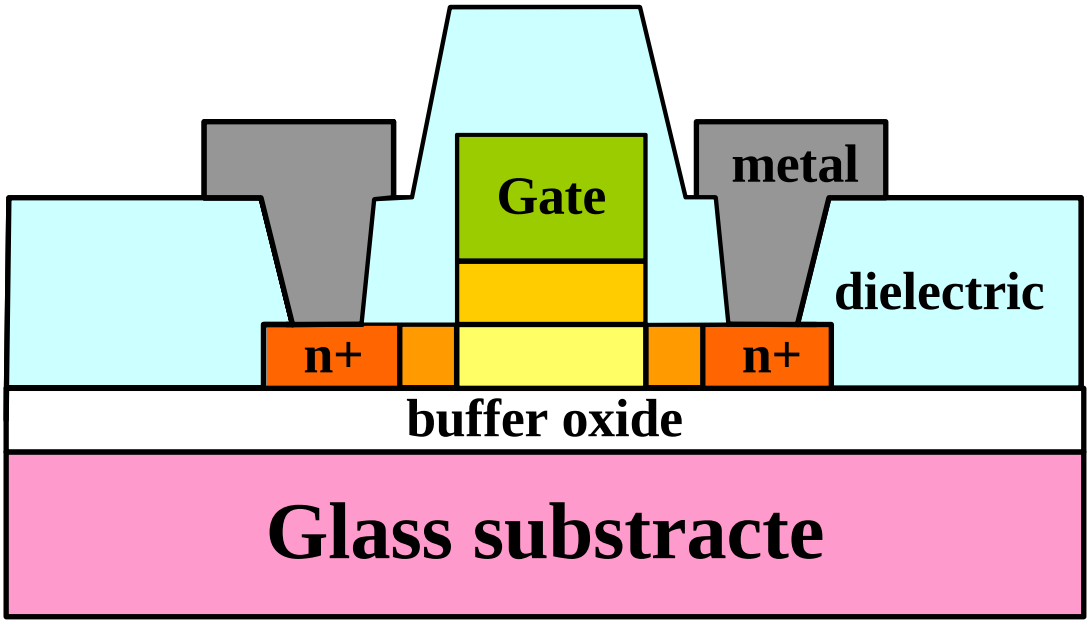

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Fig. 2-1 The cross-section views of n-channel LTPS TFTs with LDD structure

2.1.2 AC Stress Conditions

The basic parameters of AC signal consists of frequency (F), signal high level (Vgh), signal low level (Vgl), high-level time (Vgh), low-level time (Vgl), rising time (Tr), and falling time (Tf). Fig 2-2 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is given as follow:

$$T = Tr + T\_vgh + Tf + T\_vgl \quad (2.1)$$

$$F = 1/T \quad (2.2)$$

$$\text{Duty ratio} = (Tr + T\_vgh)/T \quad (2.3)$$

where T is the signal period.

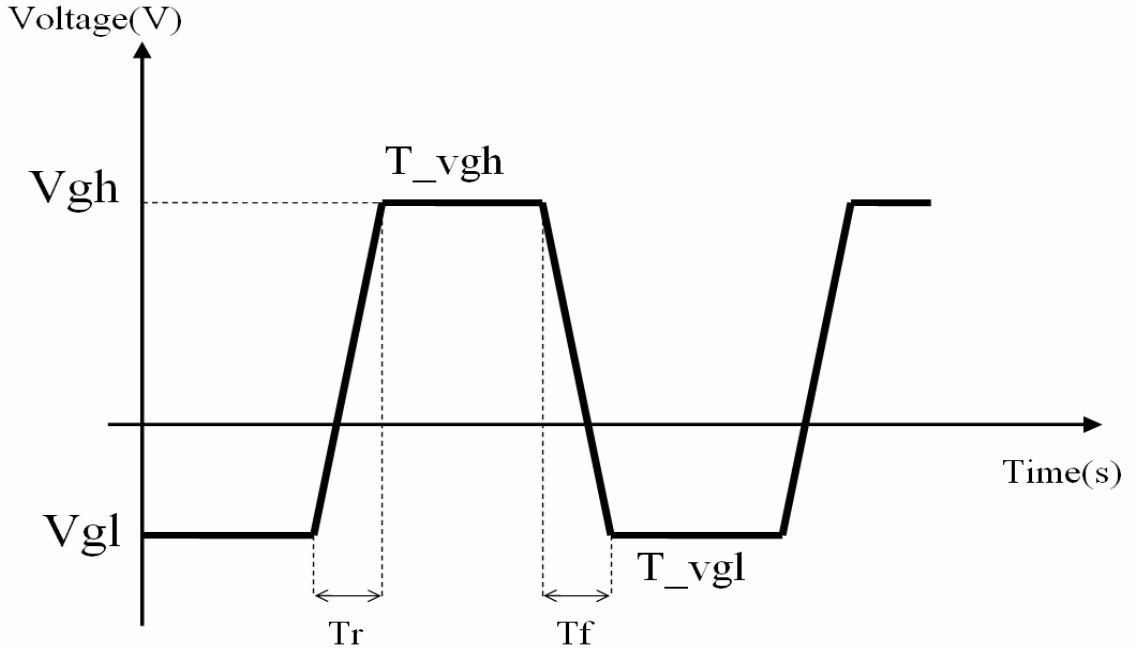

Fig. 2-2 Waveform and definition of the AC signal

Under AC stress, pulse voltage was applied to the gate electrode and source and drain were grounded, which is shown in Fig 2-3. The standard stress condition in the experiment is the gate voltage swing of -15 V to 15 V, F of 500 kHz, Tr and Tf of both 100ns, and duty ratio of 50%. These parameters can be adjusted and then various stress conditions on the gate electrode are performed to realize the reliability of LTPS TFTs. To investigate which parameter of the stress pulse dominates the degradation of the n-channel l TFT transfer characteristic, we will make four experiments. Firstly, we change frequency from 0.5 kHz to 500 kHz. Secondly, we change Vgh and Vgl of AC signal fixed amplitude of 15 V at one time, called Vg leveling. Thirdly, we will change Tr and Tf from 100ns to 700ns for gate swing range of -15 V to 15 V. And finally, as new experiments, the effects at Tr and Tf for the gate swing in the depletion region are studied.

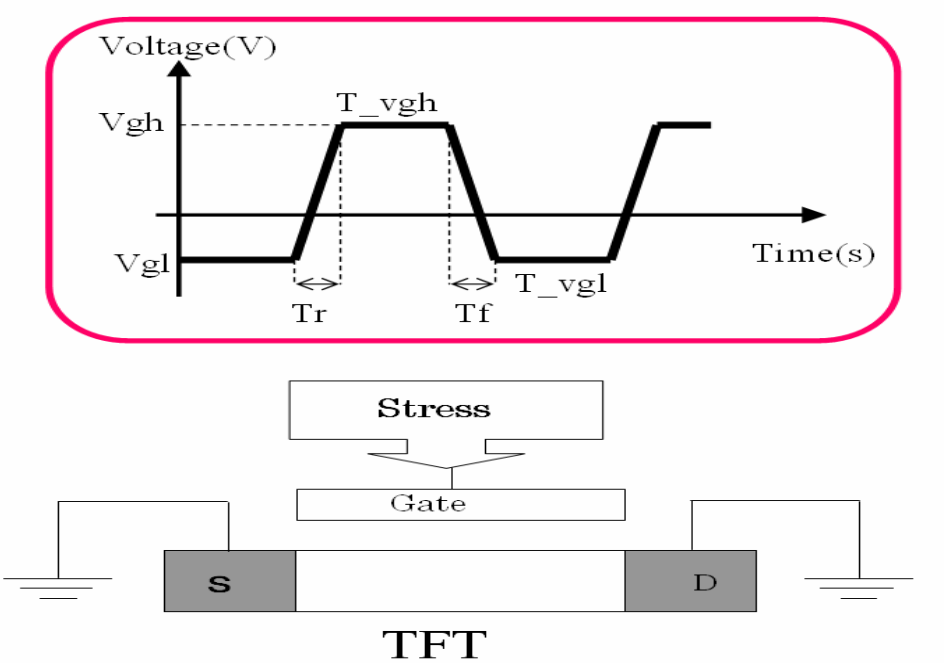

Fig. 2-3 TFT under AC stress with source and drain grounded

2.2 Results and Discussions

2.2.1 Frequency

The frequency dependence of the device degradation for n-channel TFT is shown in Fig. 2-4. The degradation is expressed as the ratio of degraded mobility (μ) to initial mobility (μ_0), where μ_0 and μ are the field effect mobility derived from the maximum transconductance at the drain voltage of 0.1 V before and after stress. Degradation is enhanced by the increase in frequency. For n-channel TFT, when the frequency increases, the mobility decreases, as shown in Fig. 2-4.

Previously, the mechanism of mobility degradation of poly-Si TFT under AC stress was reported by Uraoka et al. They discussed the relationship between the decrease in mobility and the generated electron traps. Generally, mobility is derived from measured conductance *gm* using following equation,

$$gm = \frac{I_d}{Vg} = \frac{\mu W C_i Vg}{L} \qquad (2\text{-}4)$$

where W and L are gate width and length, C_i is capacitance of the gate oxide, and μ is mobility. V_{TH} is for here set to zero for simplicity. In this equation, C_iVg corresponding to the total charge Q_t is considered to be equivalent to the charge of free carriers (Q_{mob}) when no other trapped charge exists. If the trapped charge $Q_{trapped}$ is generated, equation (2-1) is expressed as

$$gm = \mu_{FET}Q_t = \mu_{FET}\,(Q_{mov} + Q_{trapped}) = \mu_{real}Q_{mov}\,, \qquad (2\text{-}5)$$

where μ_{real} is real mobility, μ_{FET} is derived mobility from the measured drain current in the linear region, and W/L here is assumed to be one. Consequently,

$$\mu_{FET} = \frac{\mu_{real}(Q_t - Q_{trapped})}{Q_t} \qquad (2\text{-}6)$$

This equation indicates that the number of mobile charges is affected by the trapped charged $Q_{trapped}$. Depending upon the polarity of the trapped charges, mobility appears to increase, or decrease. For n-channel TFT, $Q_{trapped}$ is negative, because electrons are assumed to be trapped, and Q_t is negative. The mobility decrease for n-channel TFT can be matched between the measurement and the calculation.

The frequency dependence of the degradation of n-channel TFT is re-plotted as the repetition number dependence as shown in Fig. 2-5. Disregarding the frequency, all lines follow the universal curve. The figure clearly indicates the relationship between the degradation and the repetition number and the independence of the frequency. In other words, the degradation arisen by the unchanging voltage can be ignored.

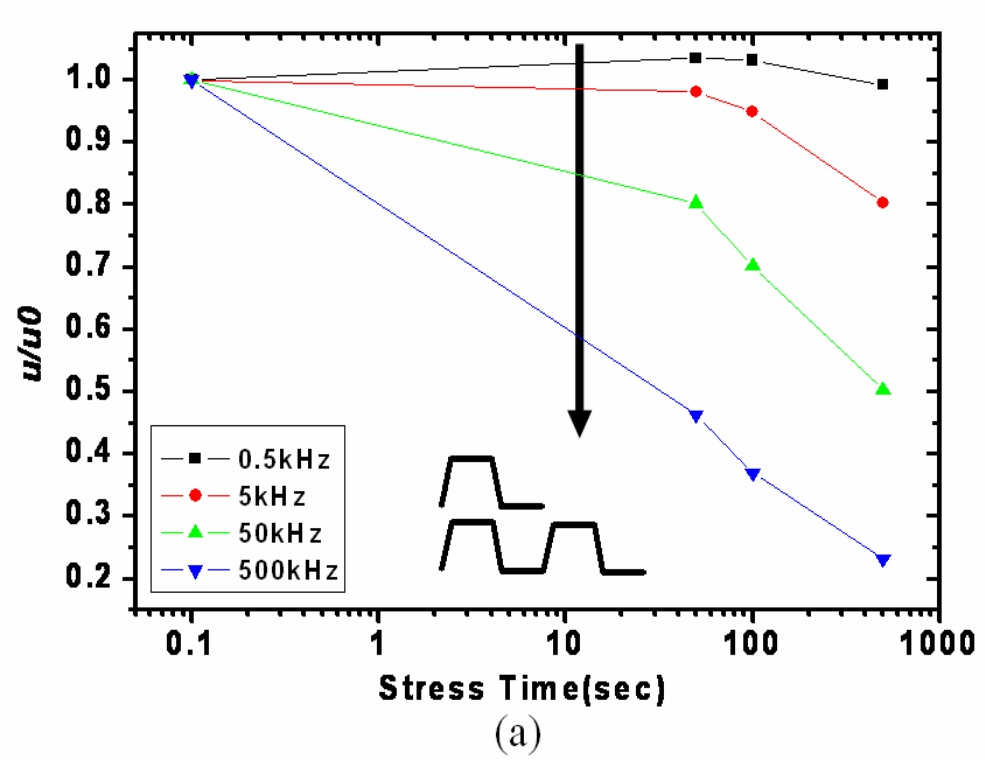

Fig. 2-4 Frequency dependence of degradation of n-channel TFT

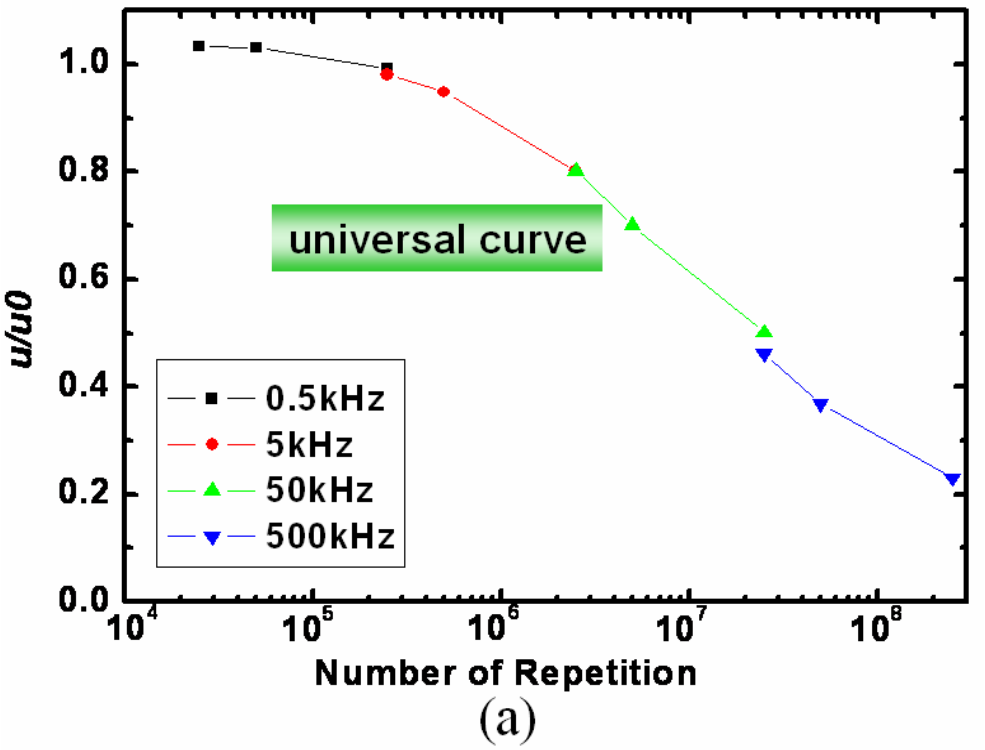

Fig. 2-5 Dependence on the number of pulse repetitions of n-channel TFT

2.2.2 Gate Voltage Leveling

The range of the gate pulse swing is separated into two parts according to the threshold voltage, as shown in Fig 2-6(a). In the ON region, the channel is formed, while in the OFF region, the channel was fully depleted. Fig. 2-6(b) clearly indicate that the degradation of mobility strongly depends on the levels of the gate voltage. For the gate pulse swing in the ON region, the degradation is very small, however, that for the gate pulse swing fully in the OFF region become large. It is because the transient electrical field is high in the OFF region, but that is very low in the ON region. Carriers can gain energy from high electrical field and become hot carriers, and the traps are generated.

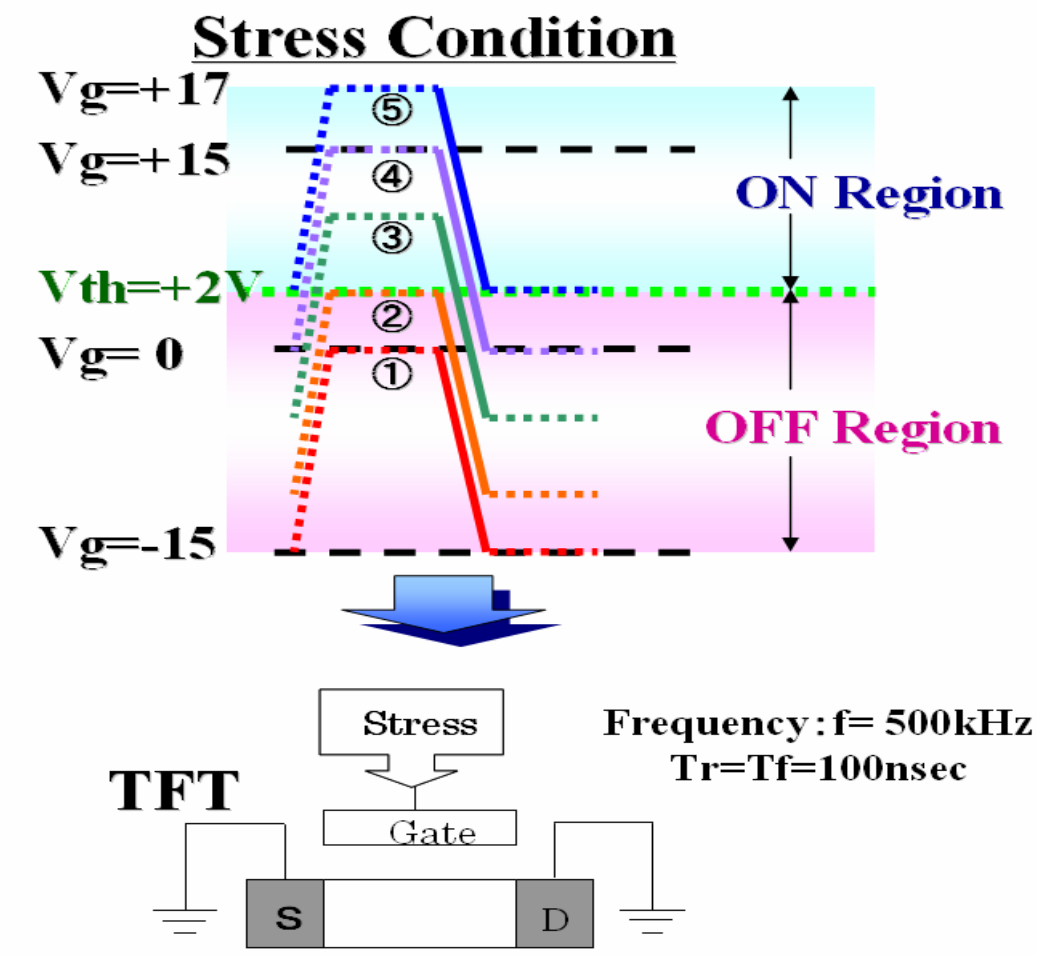

Fig. 2-6(a) Swing region

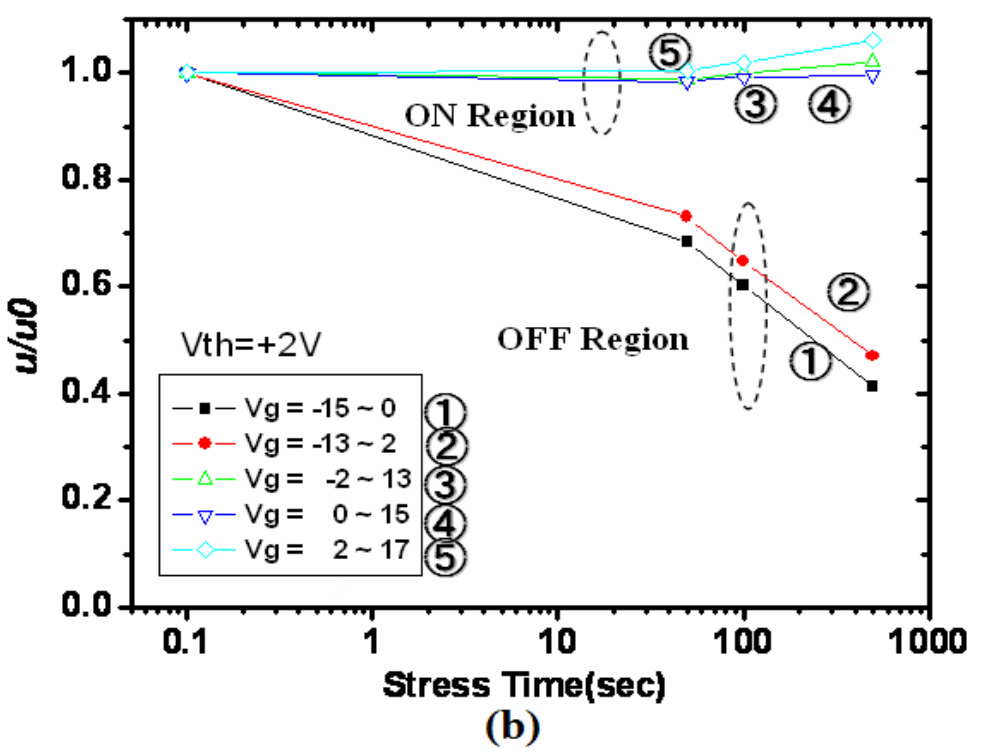

Fig. 2-6(b) Dependence of degradation on swing region for n-channel TFT

2.2.3 Rising Time and Falling Time for Vg of ON and OFF Region

The transient time dependence for the degradation was examined as shown in Fig. 2-7. During the variation of rising time Tr from 100 ns to 700 ns with a fixed Tf of 100 ns, no significant change in μ/μ_0 was observed as shown in Fig. 2-7(a). On the contrary, the degradation depended strongly on the falling time Tf as shown in Fig. 2-7(b). The degradation is remarkably accelerated with the decrease of the falling time from 700 ns for 100 ns for a fixed Tr of 100 ns. In the case of changing rising time, the gate voltage varies from OFF region to ON region, and the mobile carriers are sited at so low electrical field that no device degradation is formed. But in the case of changing falling time, the gate voltage varies from ON region to OFF region, some

carries remain in the channel and are subjected to the high electrical field becoming hot carries.

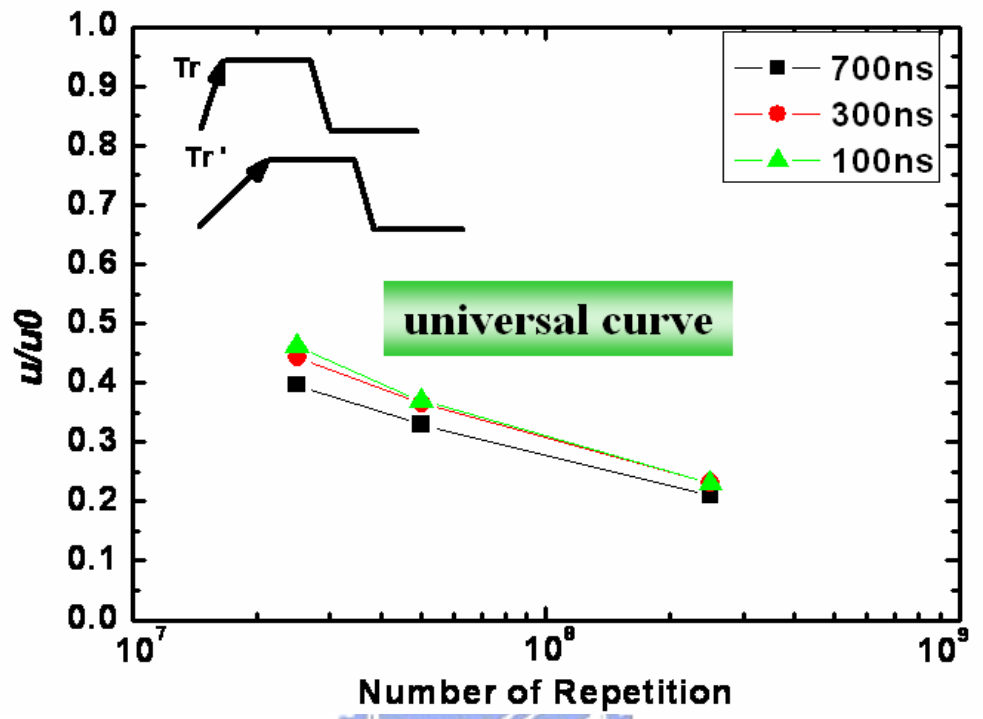

Fig. 2-7(a) Rising time dependence of the degradation.

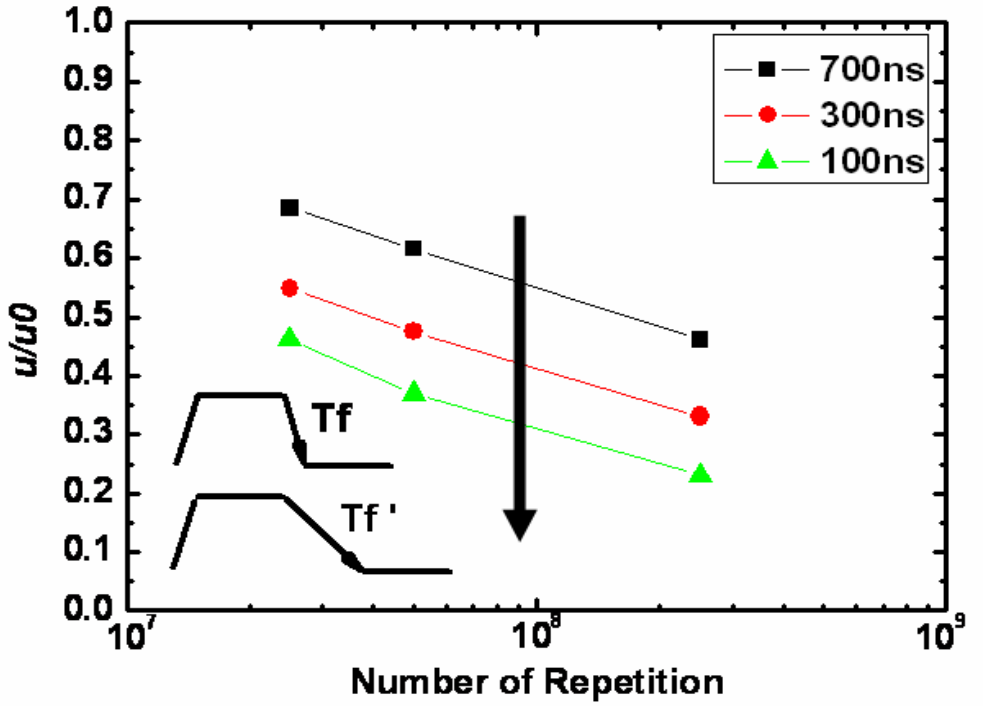

Fig. 2-7(b) Falling time dependence of the degradation.

2.2.4 Rising Time and Falling Time for Vg in the Depletion Region

Reviewing section 2.2.2, we have known that degradation by pulse swing for the ON region was very small, however, that by pulse swing for the OFF region was large. In section 2.2.3, we already observe the transient time dependence for the degradation of n-channel TFTs under AC stress with Vg = -15 V to 15V. For this gate swing, it can be taken as steps of Vg = -15 V to 0V and Vg =0 V to 15V. For n-channel TFT, Vg = -15 V to 0V is OFF region, and Vg =0 V to 15V is ON region. Because no device degradation is formed for n-channel TFT under AC stress with Vg = 0 V to 15 V, we are only interested in the transient time dependence for the degradation of n-channel TFT at Vg = -15 V to 0V. For the gate voltage swings from -15 V to 0 V, it is firstly observed that the degradation is obviously dependent on both the rising time and falling time, as shown in Fig. 2-8(a) and Fig. 2-8(b). Since there are no induced electrons for these applied gate voltages, it reveals that the previously proposed model may be incomplete.

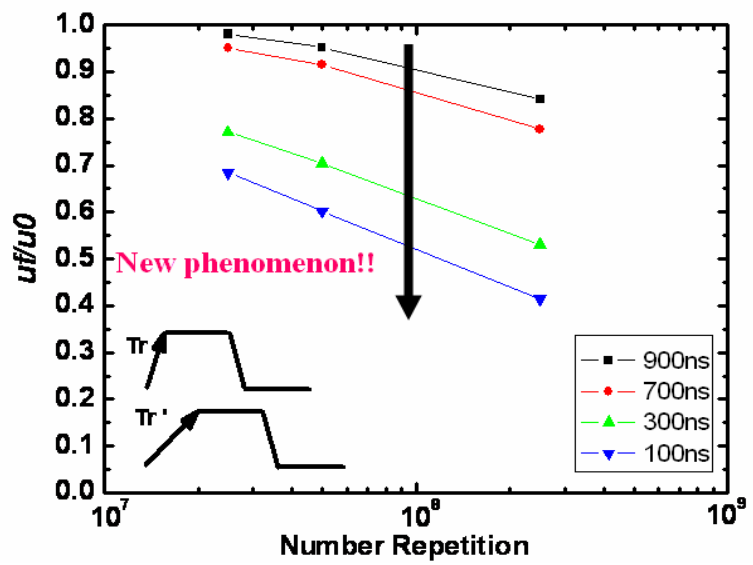

Fig. 2-8(a) Degradation of μ/μ_0 in n-channel TFT under AC stress with Vg = -15 V to 0 V measured for various rising times Tr and for Tf = 100 ns.

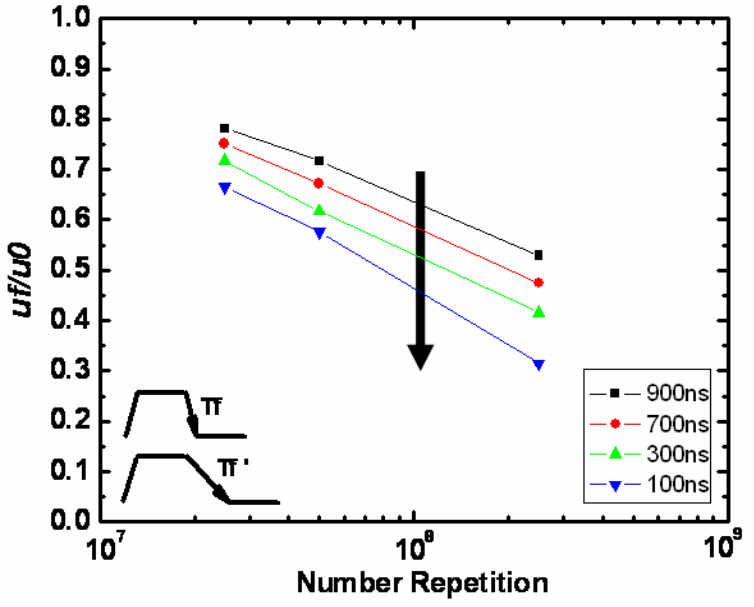

Fig. 2-8(b) Degradation of μ/μ_0 in n-channel TFT under AC stress with Vg = -15 V to 0 V measured for various rising times Tf and for Tr = 100 ns.

2.2.5 Summary of Results

	Experiments	Phenomena
1	**Frequency effect** for -15V~15V	Mobility decrease is dependent on the repetition number.
2	**VG leveling effect** for swinging range of 15V	Degradation occurs in depletion region, i.e., Vg < Vth = 2V
3	**Tr/Tf effect for Vg ON/OFF**	Degradation is dependent on Tf but independent of Tr.
4	**Tr/Tf effect for Vg in the depletion Region**	Vg = -15V~0V Degradation is both dependent on Tr and Tf.

2.3 Universal Exploration of the Degradation Mechanism for AC Stress

2.3.1 Factors of Degradation Mechanism

In order to analyze the degraded phenomena, two factors are taken into consideration, that is, the transient electric field in the lateral direction and the changes in the number the channel electrons under the lateral voltage difference. To understand the transient fields and charge distributions in the channel, a slicing method is used on the device for simulation. A whole TFT is sliced into many shorter ones in series, and a short TFT consists of segment of channel resistance and gate oxide, as shown in inset of Fig. 2-9.

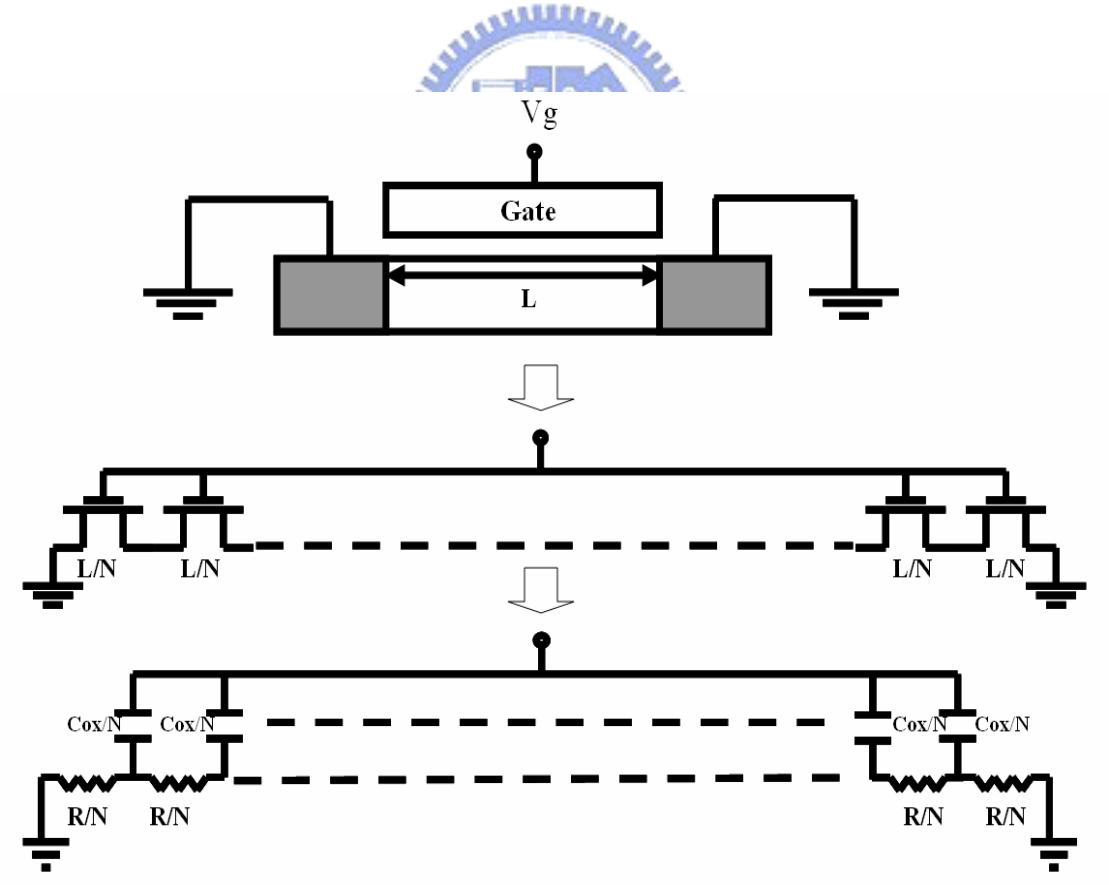

Fig. 2-9 TFT's slicing model

2.3.2 The Transient Voltage Distribution in the TFT Channel

For simplicity, ten short TFTs are used in the slicing model. Because source and drain are grounded, the channel voltage is symmetric in the middle of the channel. The voltage of the edge TFT is called *Ve*, and the other voltages are V_{21}, V_{32}, V_{43}, V_{54}, respectively, as shown in Fig 2-10(a).

Using a commercially available circuit simulator SPECTRE, the transient voltage distribution in the TFT channel under AC stress can be qualitatively expressed. Firstly, we observe the transient voltage distribution in the channel of TFT under AC stress with Vg = -15 V to 15 V, Ve is the largest voltage among the sliced node voltages, shown in Fig. 2-10(b). Referring to the previous report, the emission image of the n-channel TFT under dynamic stress indicates that the degradation is the worst at the edges of the channel, shown in Fig. 2-10(c). It also accords with the simulation results that *Ve* is the largest voltage in the channel. In this section, we call ON region as channel region, and OFF region as depletion region. In the channel region, the channel voltages are almost zero. On the contrary, in the depletion region, the channel voltages are very large. Therefore, device degradation mainly occurs in the depletion region, and not in the channel region.

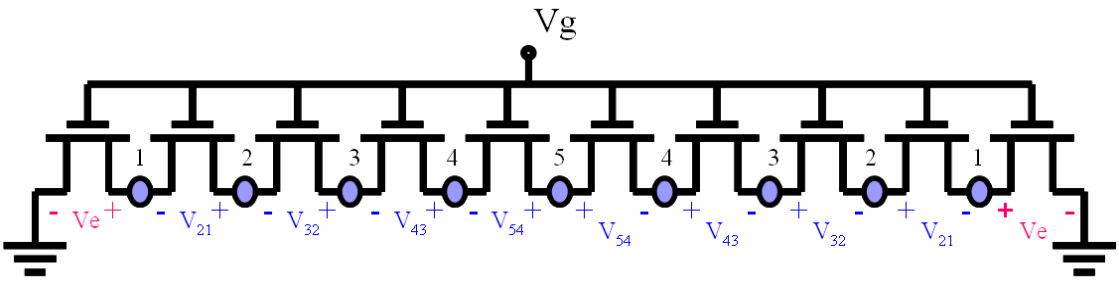

Fig. 2-10(a) 10 TFT's slicing model

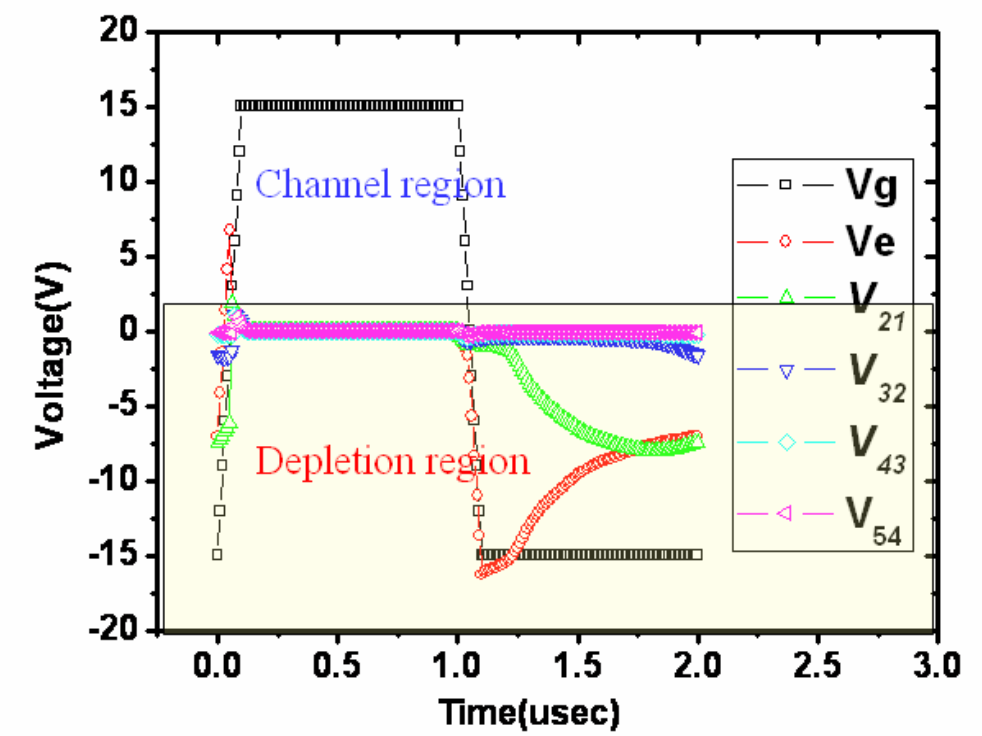

Fig. 2-10(b) The transient voltage distribution of n-channel TFT

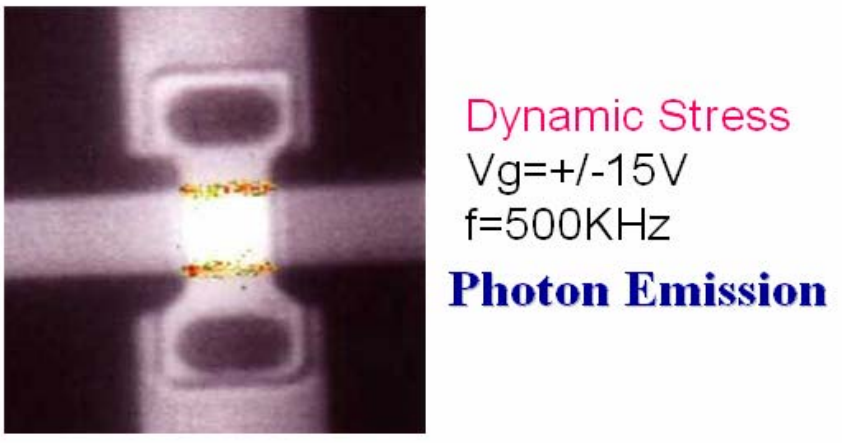

Fig. 2-10(c) Photon emission

2.3.3 Transient Voltage Distribution for AC Stress with Various Rising Time and Falling Time

As the mention of the section above, we know that *Ve* is the largest voltage in the channel, and thus *Ve* simulation result is used to explain the transient time dependence for the degradation of n-channel TFT at Vg = -15 V to 15V. As shown in Fig. 2-11, when Vg rises in the depletion region, Ve follows the change of Vg owing to coupling effect, reflecting the scarce change in the channel carrier number. As the gate voltage goes above threshold voltage (V_{TH}), the channel is formed and *Ve* is quickly discharged to zero, such that the lateral field is too low to speed up the carriers. Therefore, the mobility degradation is independent of Tr. For the period of gate voltage above V_{TH}, the channel is of very low resistance and thus *Ve* is almost zero. As the gate voltage falls to the depletion region, *Ve* is coupled to a large negative value by Vg. *Ve* is then slowly charged toward ground during T_vgl. The lateral voltage different at the TFT edge may be so high that the carriers can gain energy to become hot carriers, resulting in the mobility degradation. The coupling magnitude of this transient electrical field becomes larger with shorter Tf, resulting in the Tf dependence of the mobility degradation.

On the other hand, for the gate voltage swing of -15V to 0V, the simulation result is shown in Fig. 2-12. Since the gate voltage is all below V_{TH}, TFT is kept in the depletion region. Consequently, as the gate voltage swings in Tr and Tf, Ve will be coupled by Vg. This coupled Ve would be discharged slowly during T_vgh and T_vgl, such that carriers may obtain high energy and cause the device degradation. Since the coupled magnitude of Ve is concerned with the changing speed of Vg, the mobility degradation is accordingly dependent on Tr and Tf.

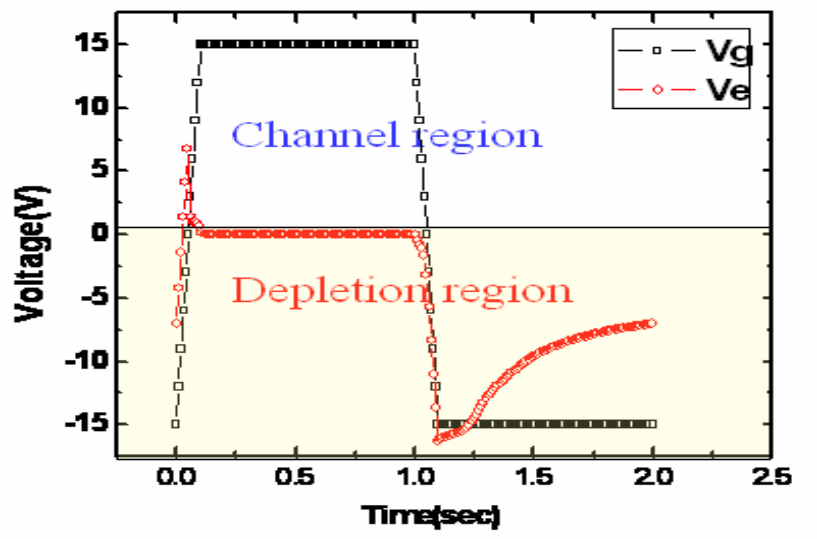

Fig. 2-11(a) Ve for Vg = -15 V ~15 V of Tr = Tf = 100 ns

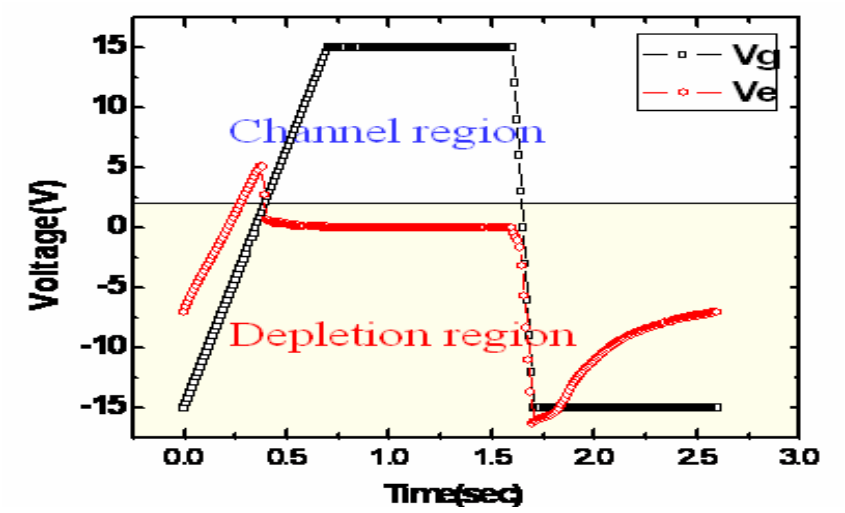

Fig. 2-11(b) Ve for Vg = -15 V ~ 15 V of Tr = 700 ns, Tf = 100 ns

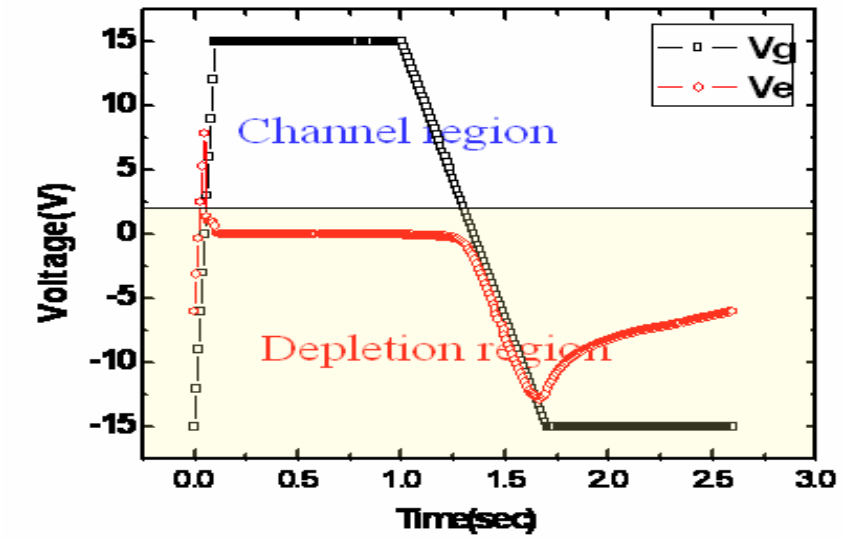

Fig. 2-11(c) Ve for Vg = -15 V ~ 15V of Tr = 100 ns, Tf = 700 ns

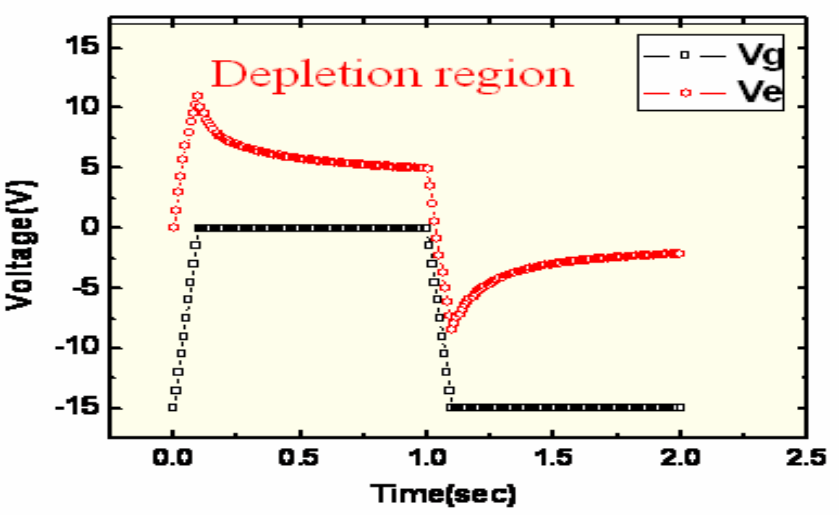

Fig. 2-12(a) Ve for Vg = -15 V ~ 0 V of Tr = Tf = 100 ns

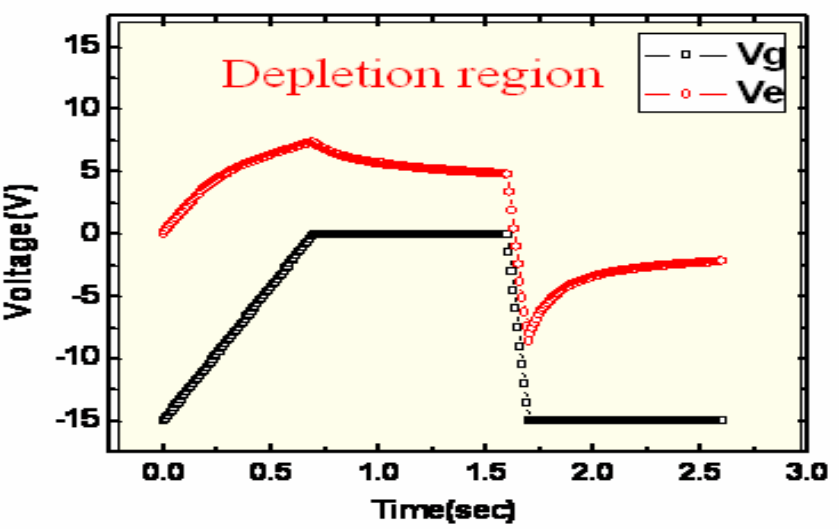

Fig. 2-12(b) Ve for Vg = -15 V ~ 0 V of Tr = 700 ns, Tf = 100 ns

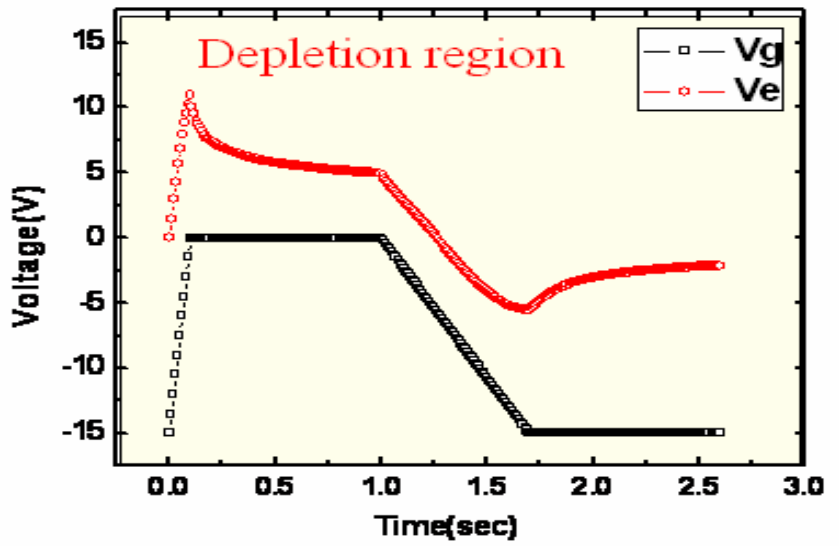

Fig. 2-12(c) Ve for Vg = -15 V ~ 0 V of Tr = 100 ns, Tf = 700 ns

2.3.4 A new Index Π to estimate the degraded degree

In order to describe the degree of the degradation, a new index Π calculated from simulation result is further introduced, which is given as

$$\Pi = \sum \frac{1}{Ti} \int_{Ti} Ve \bullet [Cox \bullet d(Vg - Ve)/dt] \bullet dt \qquad (2\text{-}7)$$

where Ti corresponds to Tr, Tf, T_vgh, and T_vgl, and *Cox* is the gate capacitance per unit area. This index accounts for two factors. The first one is *Ve*, corresponding to the transient lateral electrical field at the edge of the sliced TFT. And the second term is *Cox* • *d(Vg – Ve) / dt*, representing the charges flow outward through the edge of the sliced TFT. For simplicity, we assume that *Ve* follows the change of Vg at Tr and Tf, thus *Vg – Ve* is kept constant and its time differentiation is zero. Therefore, the coupling magnitude of *Ve* and its duration dominate the value of Π. The mobility degradation ($1-\mu/\mu_0$) versus the index Π under different AC stress conditions are plotted in Fig. 2-13. The fair linearity exhibits the validity of the proposed mechanism.

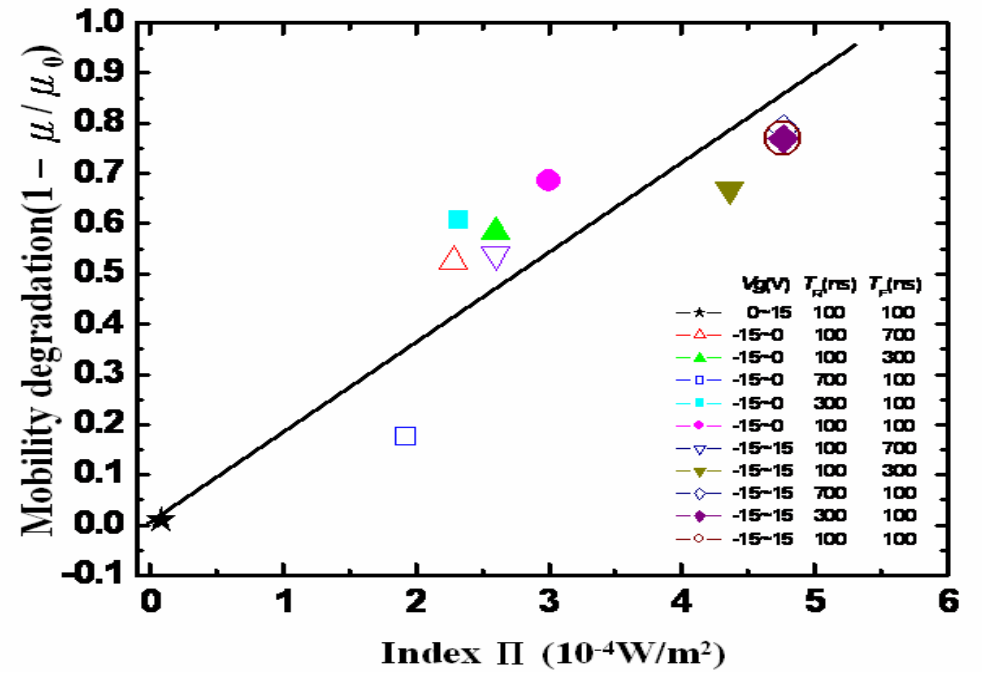

Fig. 2-13 Mobility degradation ($1-\mu/\mu_0$) versus Index Π for n-channel TFT

Chapter 3

N-Poly-Si TFT under Gate Pulse Stress with Drain Floating and Source Grounded

3.1 Introduction

For the peripheral circuit in poly-Si panel, NAND and NOR logic gates are the fundamental elements. When input terminals A and B of NAND and NOR gates are 0 and 1, respectively, floating drain TFTs appear, as shown in Fig. 3-1. Therefore, a new AC stress condition needs to be discussed, called floating drain AC stress. Under floating drain AC stress, pulse voltage was applied to the gate electrode and source was grounded and drain was floating, which is shown in Fig 3-2.

The initial stress condition in this experiment is the gate voltage swing of -15 V to 15 V, F = 500 kHz, Tr and Tf are both 100ns, and duty ratio is 50%. As the same as the experiments in the chapter 2, we will also make four experiments. Firstly, we change frequency from 0.5 kHz to 500 kHz. Secondly, we change Vgh and Vgl of AC signal fixed amplitude of 15 V at one time, called Vg leveling. Thirdly, we will change Tr and Tf from 100ns to 700ns for gate swing range of -15 V to 15 V. And finally, the effects at Tr and Tf for the gate swing in the depletion region are also studied.

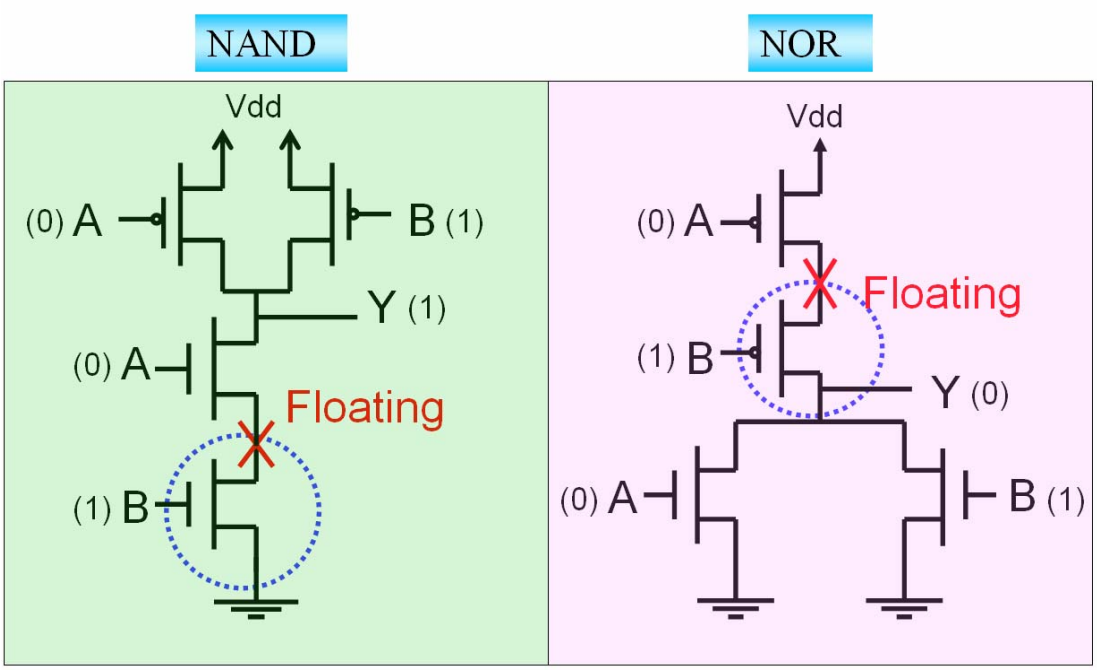

Fig. 3-1 One terminal of TFT floating

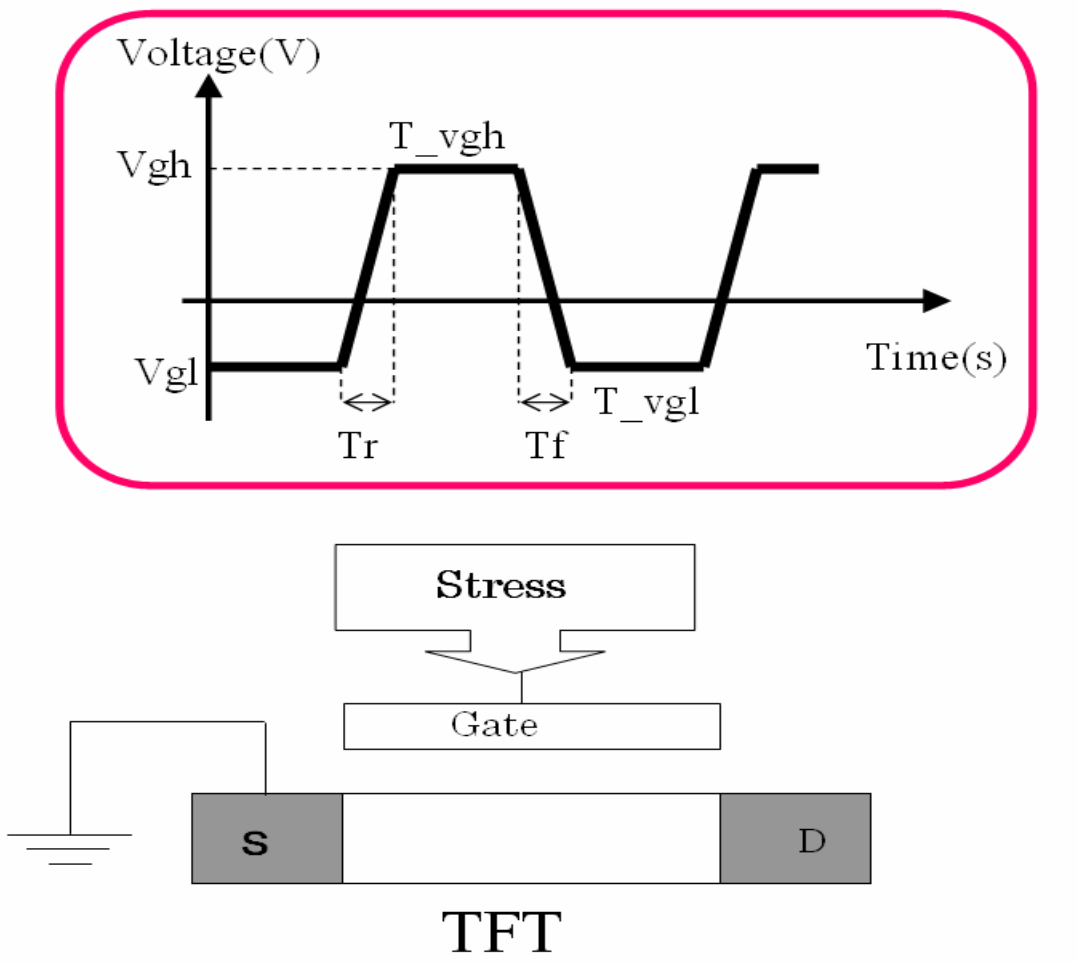

Fig. 3-2 Floating drain AC stress condition

3.2 Floating Drain AC Stress Model

We assume that the floating drain voltage of poly-Si TFT under AC stress follows the gate voltage by the coupling effect. Therefore, the channel is only formed near the source, but not formed near the drain. When TFT starts to be stressed from ON region to OFF region, hot carriers are generated near the source. We can suggest that only the source is damaged, and no degradation is formed in the drain. The floating drain AC stress model is shown in Fig. 3-3.

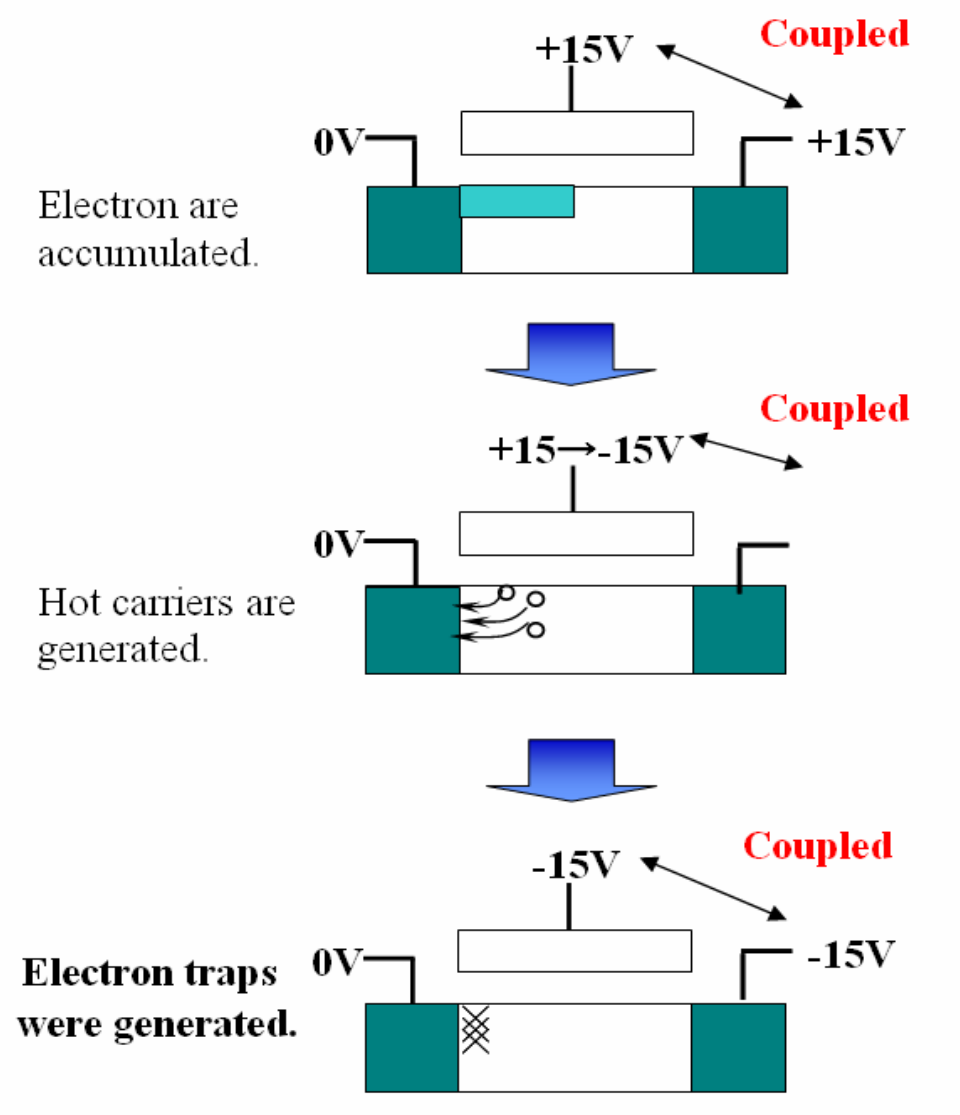

Fig. 3-3 Floating drain AC stress model

3.3 Experiments

In order to verify the proposed floating drain AC stress model, the comparison between forward saturated current with reverse saturated current is used. As shown in Fig. 3-4, in the forward mode, the source and drain connections are the same as during stress; in the reverse mode, they are swapped). The field effect mobility is extracted from maximum transconductance in the saturated region of Id – Vg characteristics at |Vds| = 6 V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of Id = at |Vds| = 0.1 V. The V_{TH} shift is defined as the difference between V_{TH2} and V_{TH1}, where V_{TH1} is the threshold voltage before stress and V_{TH2} is the threshold voltage after stress.

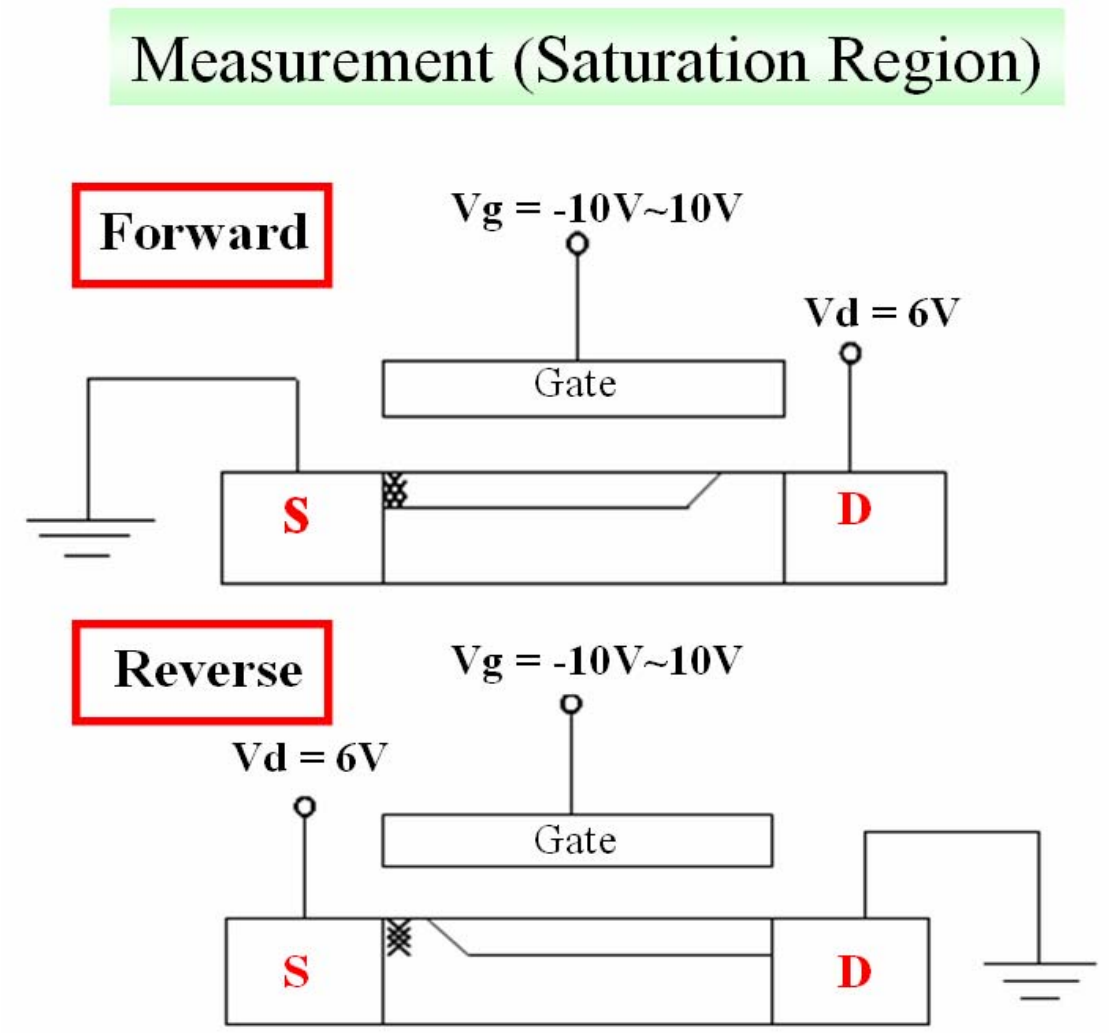

Fig. 3-4 Forward and reverse modes

3.4 Results and Discussions

3.4.1 Frequency

The frequency dependence on mobility decrease of the forward and reverse modes are shown in Fig. 3-5(a) and Fig. 3-5(b), respectively. In the forward mode, the degradation is enhanced by the increase in frequency, but in the reverse mode, the degradation is nearly zero. For n-channel TFTs, the experimental evidence indicates that traps generated by floating drain AC stress are localized closed to the source.

During saturated operation, with the TFT biased in the reverse mode, the traps lie in the source pinch off region, and provide that the source field is high enough, the channel current will not be severely degraded. On the other hand, when the TFT is forward, the extra traps lie close to the source where they impede injection of carriers into the channel and have a much greater effect on the channel current.

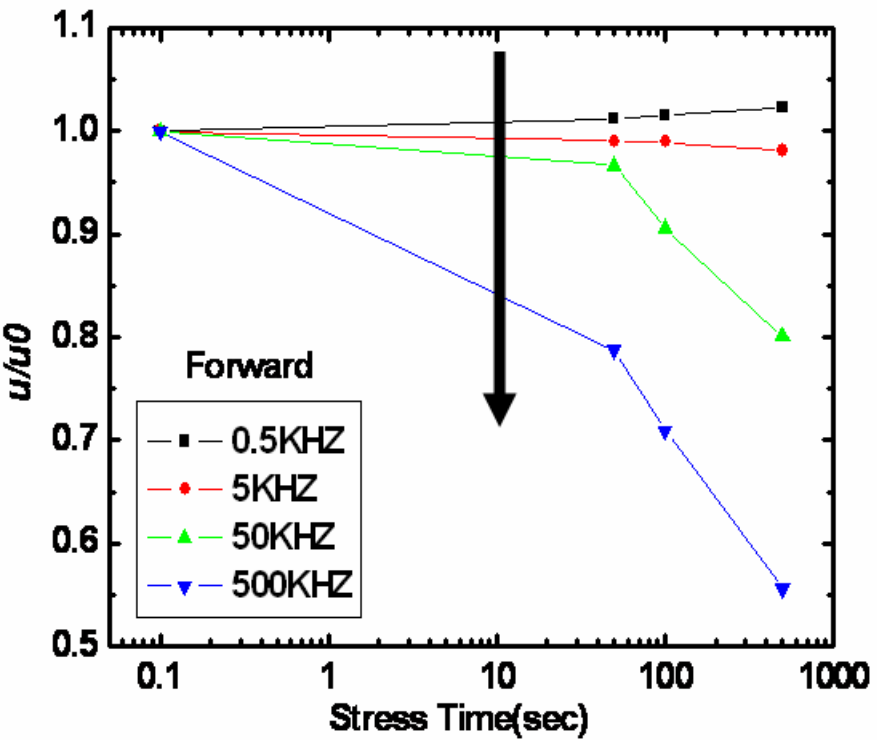

Fig. 3-5(a) Frequency dependence of forward mode

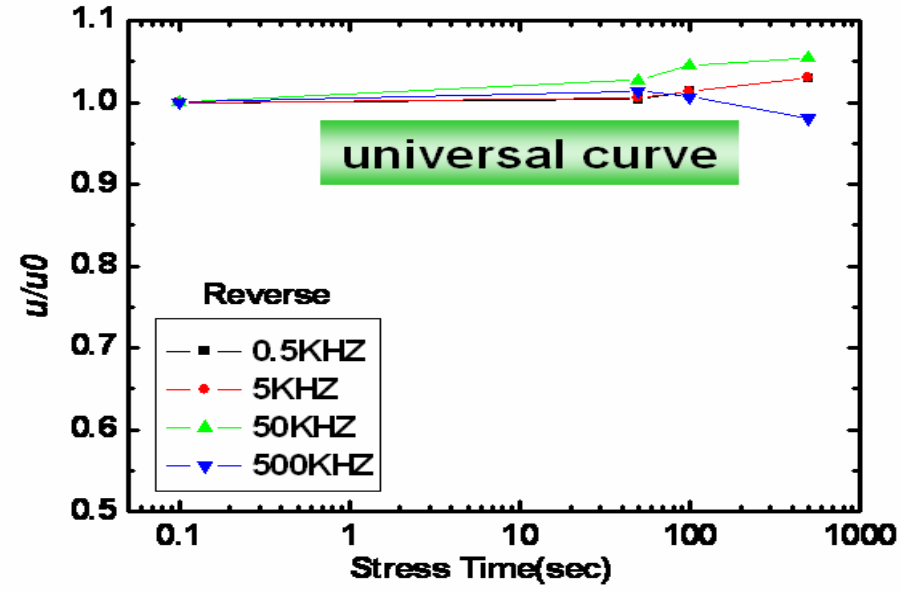

Fig. 3-5(b) Frequency dependence of reverse mode

The frequency dependence of the degradation of n-channel TFT is re-plotted as the repetition number dependence as shown in Fig. 3-6. Disregarding the frequency, the forward mode follows the universal curve. Fig. 3-6 clearly indicates the relationship between the degradation and the repetition number and the independence of the frequency.

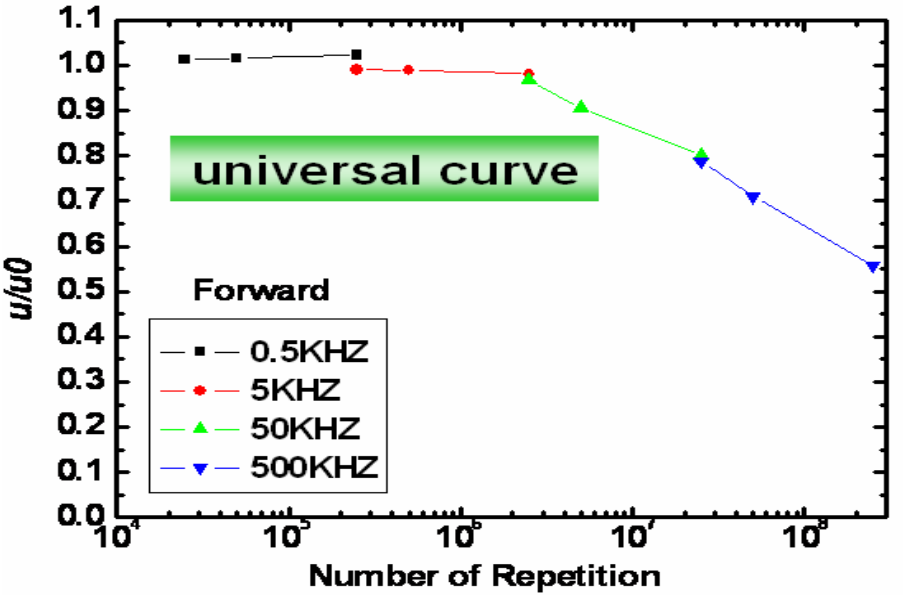

Fig. 3-6(a) Dependence on the number of pulse repetitions of the forward mode of the n-channel TFT

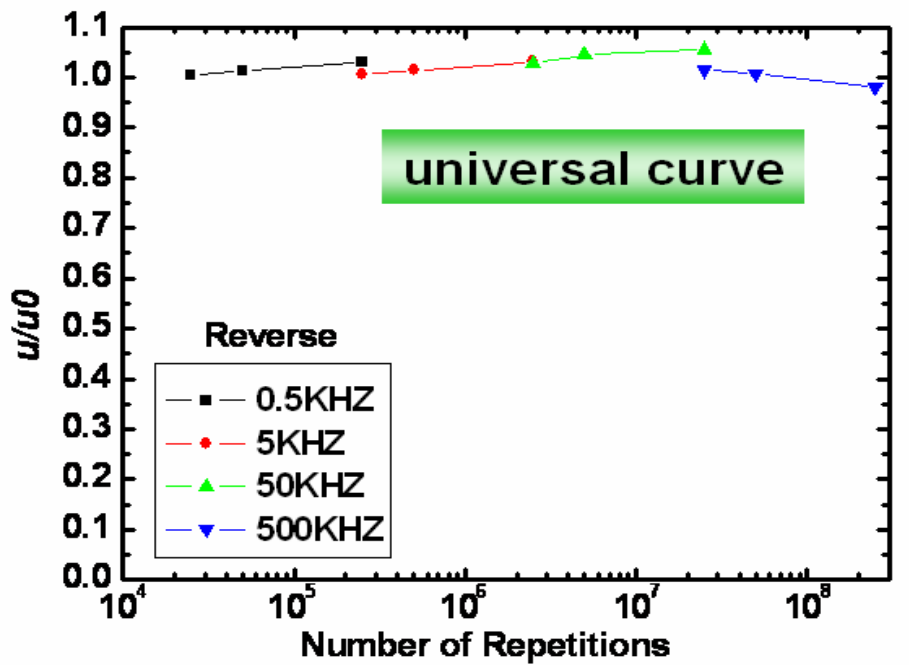

Fig. 3-6(b) Dependence on the number of pulse repetitions of the reverse mode of the n-channel TFT

3.4.2 Gate Voltage Leveling

The range of the gate pulse swing is separated into two parts according to the threshold voltage, shown in Fig 3-7(a). In the ON region, the channel is formed, while in the OFF region, the channel was fully depleted. Fig. 3-7(b) clearly indicates that the degradation of the forward mobility strongly depended on the levels of the gate voltage. For the gate pulse swing in the ON region, the degradation is very small, however, that for the gate pulse swing fully in the OFF region become large. Fig 3-7(c) shows that no degradation of the reverse mode is formed either in the ON region or in the OFF region.

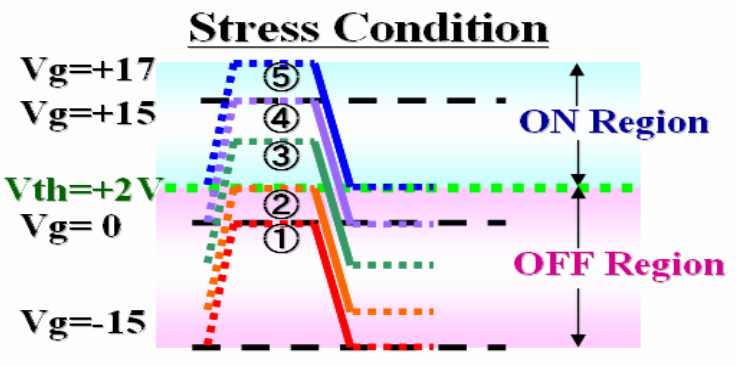

Fig. 3-7(a) Swing region

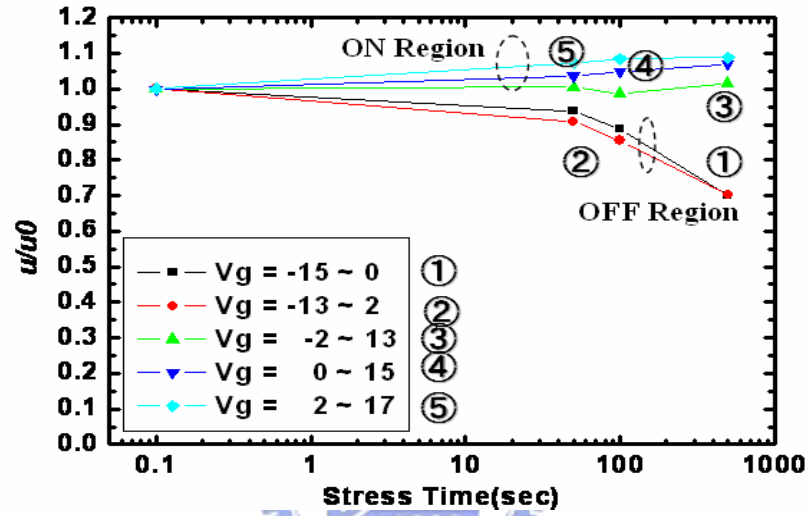

Fig. 3-7(b) Dependence of degradation on swing region for the forward mode of n-channel TFT

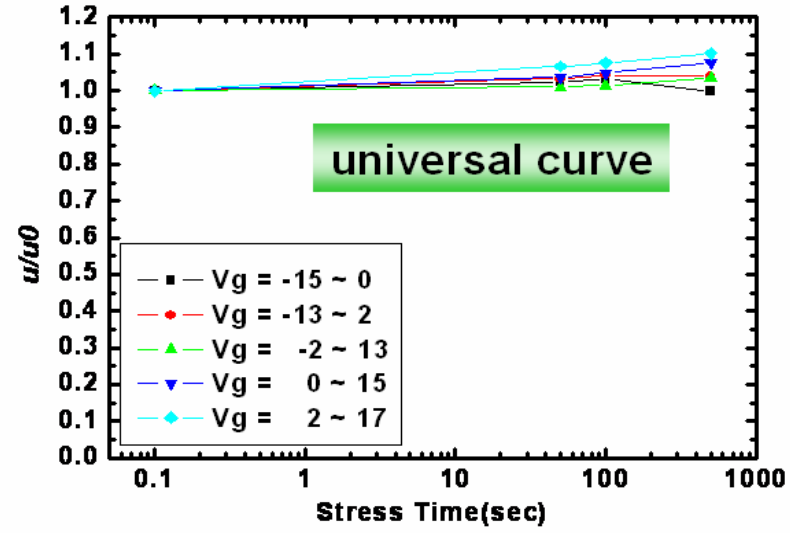

Fig. 3-7(c) Dependence of degradation on swing region for the reverse mode of n-channel TFT

3.4.3 Rising Time and Falling Time for Vg of ON and OFF Regions

The transient time dependences for the degradations of forward and reverse mode were examined as shown in Fig. 3-8. During the variation of the rising time Tr from 100 ns to 700 ns with a fixed Tf of 100 ns, no significant change in μ/μ_0 was observed as shown in Fig. 3-8(a). On the contrary, the degradation of the forward mode depended strongly on the falling time Tf as shown in Fig. 3-8(b). But the degradation of the reverse mode is almost zero. The experiment accords with the proposed mode with n-channel TFT under floating drain AC stress.

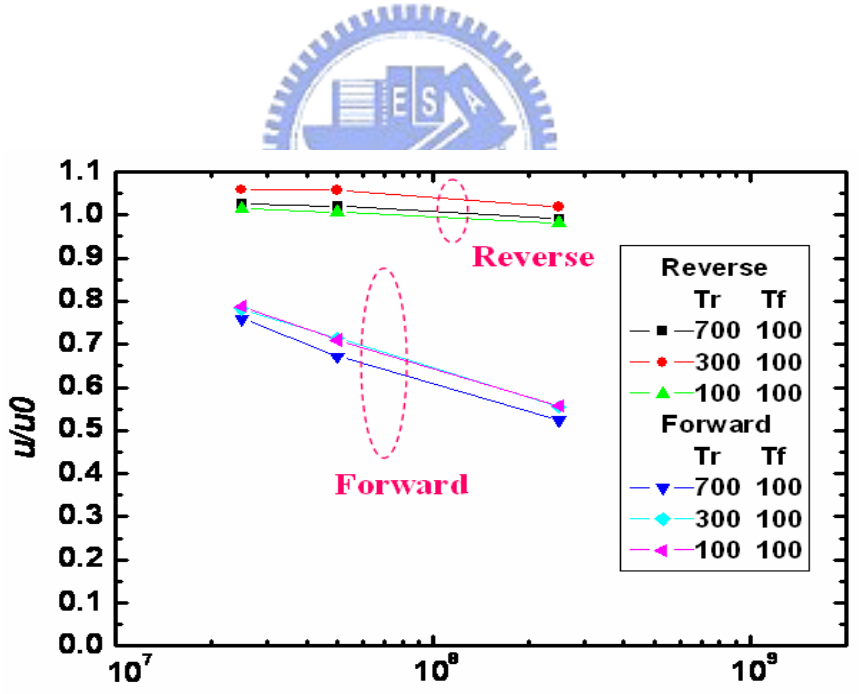

Fig. 3-8(a) Rising time dependence of the degradation

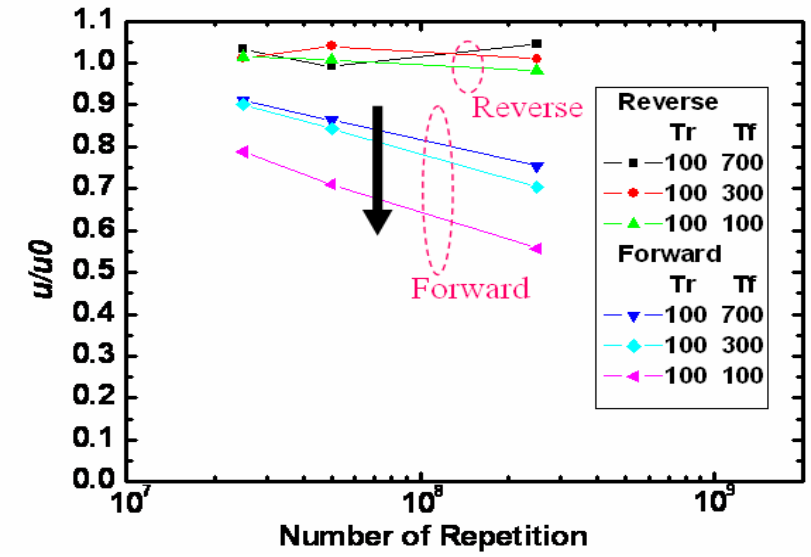

Fig. 3-8(b) Falling time dependence of the degradation

3.4.4 Rising Time and Falling Time for Vg in the Depletion Region

For n-channel TFT, the forward result is the same as the section 2.2.4, shown in Fig. 3-9. The degradation of the forward mode is both dependent of the rising time and the falling time. The reverse mode is also no degradation. It goes a step further to verify the proposed model.

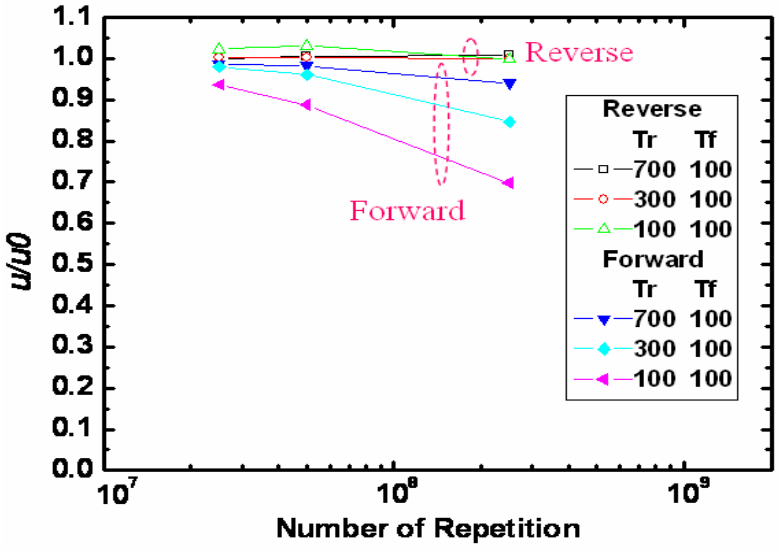

Fig. 3-9(a) Rising time dependence of the degradation

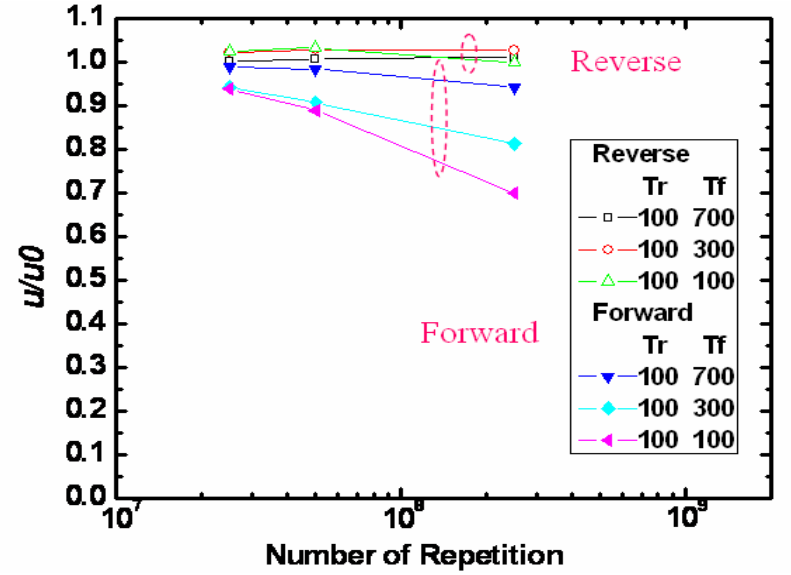

Fig. 3-9(b) Falling time dependence of the degradation

3.5 Universal Exploration of the Degradation Mechanism for AC Stress

3.5.1 Factors of Degradation Mechanism for AC Stress

In order to analyze the degraded phenomena dependence on the transient time of poly-Si TFT under floating drain AC stress, two factors are also taken into consideration, that is, the transient electric field in the lateral direction and the changes in the number the channel electrons under the lateral voltage difference. To understand the transient fields and charge distributions in the channel, a slicing method is used on the device for simulation, too. A whole TFT is sliced into many shorter ones in series, and a short TFT consists of segment of channel resistance and gate oxide. For simplicity, ten short TFTs are used to be slicing model. The source is ground and the drain is floating, and the AC signal is applied to the gate such that the voltages are distributed in the channel. The voltage near the source of TFT's slicing

model is called Ves, and the voltage near the drain of TFT's slicing model is called Ved. The other voltages in the channel are V_{21}, V_{32}, V_{43}, V_{54}, V_{65}, V_{76}, V_{87}, and V_{98}, respectively, as shown in Fig. 3-10(b).

To be the simulated circuit, the drain connected with a very large resistance is simulated to be floating, as shown in Fig. 3-10(b). And the simulation method is the same as the section 2.8.2. In the flowing section, we also observe the transient voltage distribution in the channel, and try to analyze the degradation of poly-Si TFT under floating drain AC stress.

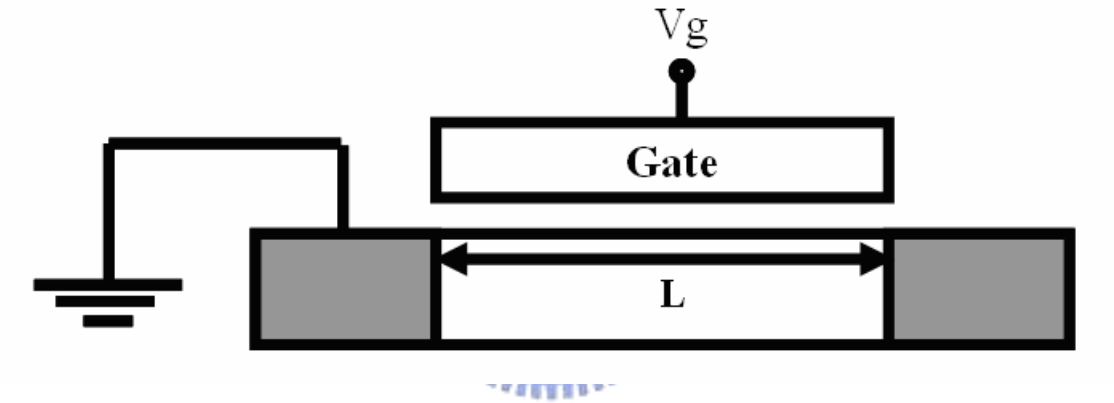

Fig. 3-10(a) TFT under floating drain AC Stress

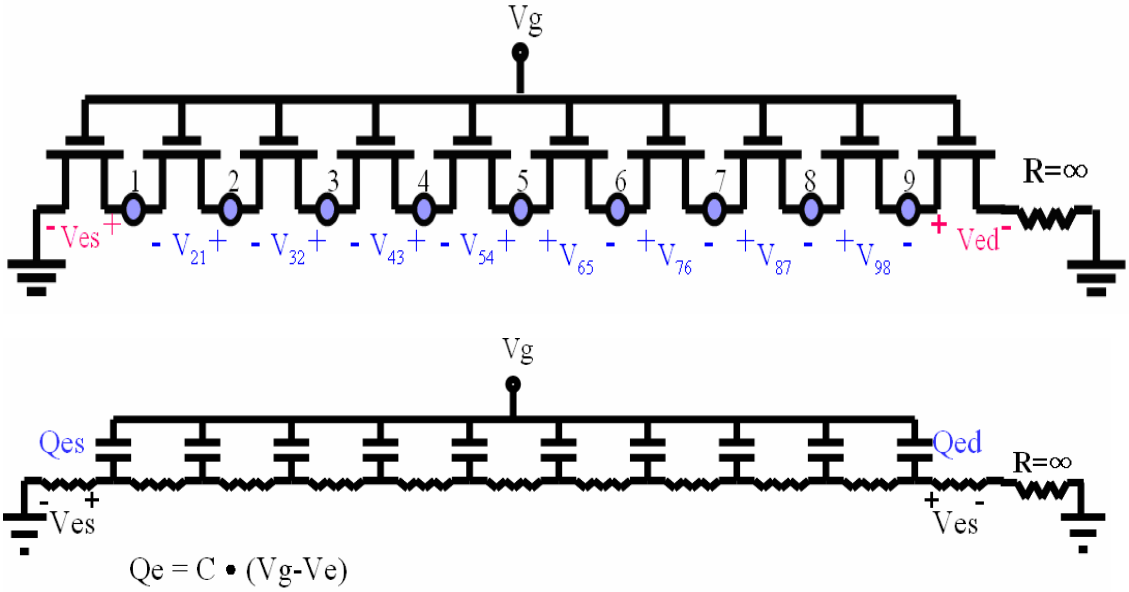

Fig. 3-10(b) TFT's slicing model

3.5.2 The Transient Voltage Distribution in the TFT Channel

Using a commercially available circuit simulator SPECTRE, the transient voltage distribution in the TFT channel under AC stress can be qualitatively expressed. Firstly, we observe the transient voltage distribution in the channel of TFT under AC stress with Vg = -15 V to 15 V, *Ves* is also the largest voltage than the other TFTs' voltages, and Ved is almost zero, as shown in Fig. 3-11. Referring to the previous report, the emission image of the n-channel TFT under AC stress indicates that the degradation is the worst at the edges of the channel, shown in Fig. 2-10(c). Therefore, we can suggest that the emission image will only occurs near the source for n-channel TFT under floating drain AC stress. In this section, we also call ON region as the channel region, and OFF region as the depletion region. We can observe that the channel voltages are almost zero in the channel region by the simulation; in the depletion region, the channel voltage Ves is very large.

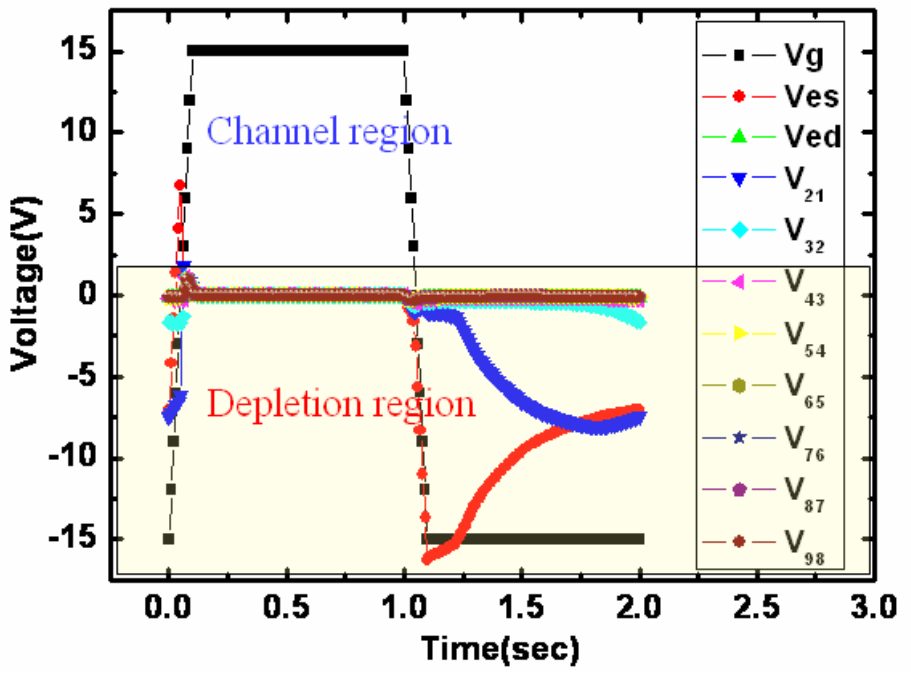

Fig. 3-11 The transient voltage distribution of n-channel TFT

3.5.3 Transient Voltage Distribution for AC Stress with Various Rising Time and Falling Time

As the mention of the section above, we know that *Ves* is the largest voltage in the channel and Ved is almost zero, and thus the simulation result is used to explain the transient time dependence for the degradation of n-channel TFT under floating drain AC stress at Vg = -15 V to 15V. As shown in Fig. 3-12, when Vg rises in the depletion region, Ves follows the change of Vg owing to coupling effect, reflecting the scarce change near the source in the channel carrier number. As the gate voltage goes above threshold voltage (V_{TH}), the channel is formed and *Ves* is quickly discharged to zero, such that the lateral field is too low to speed up the carriers. Therefore, the mobility degradation is independent of Tr. For the period of gate voltage above V_{TH}, the channel is of very low resistance and thus *Ves* is almost zero. As the gate voltage falls to the depletion region, *Ves* is coupled to a large negative value by Vg. *Ves* is then slowly charged toward ground during T_vgl. The lateral voltage different at the TFT edge may be so high that the carriers can gain energy to become hot carriers, resulting in the mobility degradation. The coupling magnitude of this transient electrical field becomes larger with shorter Tf, resulting in the Tf dependence of the mobility degradation. And for Ved, the voltage is zero at all time, so there is no degradation near the drain.

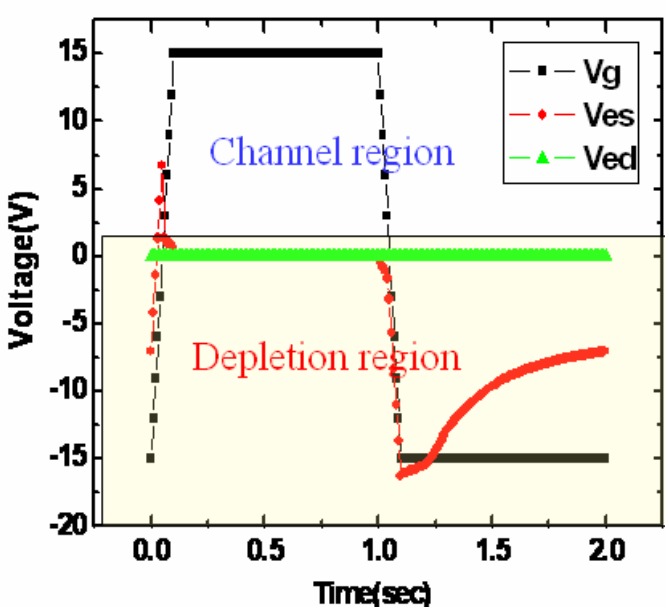

Fig. 3-12(a) Ves and Ved for Vg = -15 V ~15 V of Tr = Tf = 100 ns

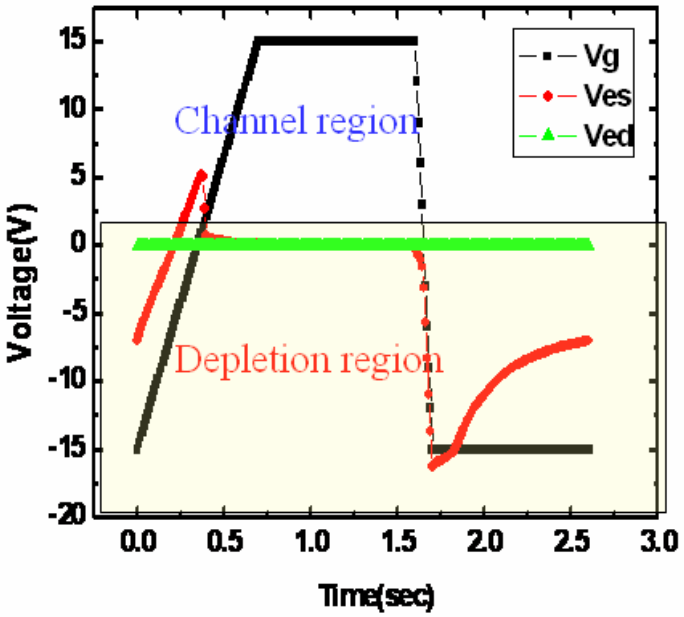

Fig. 3-12(b) Ves and Ved for Vg = -15 V ~15 V of Tr = 700 ns, Tf = 100 ns

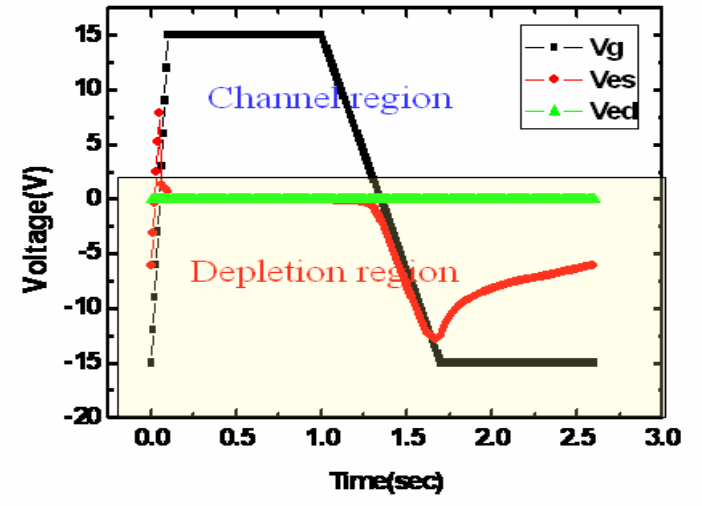

Fig. 3-12(c) Ves and Ved for Vg = -15 V ~15 V of Tr = 100 ns, Tf = 700 ns

On the other hand, for the gate voltage swing of -15V to 0V, the simulation result is shown in Fig. 3-13. Since the gate voltage is all below V_{TH}, TFT is kept in the depletion region. Consequently, as the gate voltage swings in Tr and Tf, Ves will be coupled by Vg. This coupled Ves would be discharged slowly during T_vgh and T_vgl, such that carriers may obtain high energy and cause the device degradation. Since the coupled magnitude of Ves is concerned with the changing speed of Vg, the mobility degradation is accordingly dependent on Tr and Tf. And for Ved, the voltage is zero at all time, so there is also no degradation near the drain.

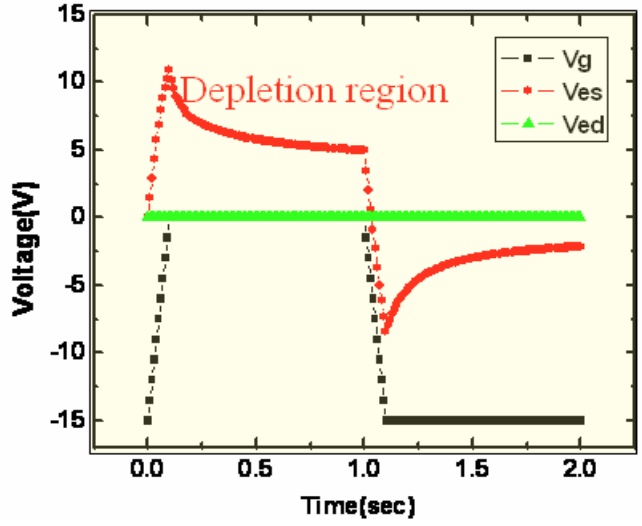

Fig. 3-13(a) Ves and Ved for Vg = -15 V ~ 0 V of Tr = Tf = 100 ns

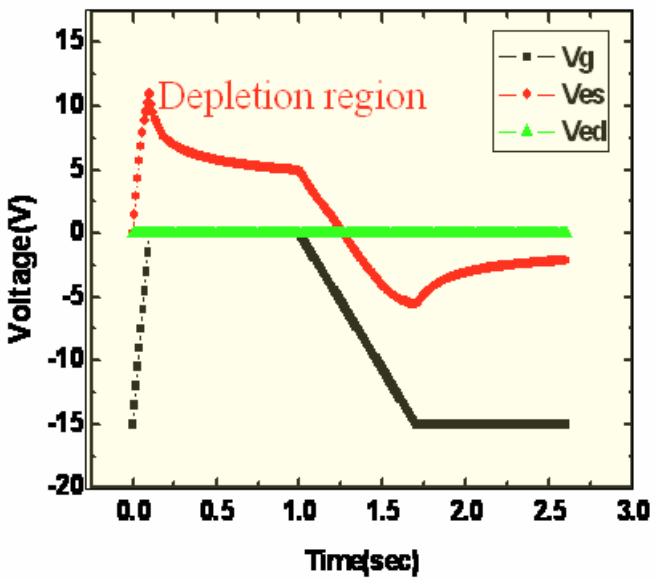

Fig. 3-13(b) Ves and Ved for Vg = -15 V ~0 V of Tr = 700 ns, Tf = 100 ns

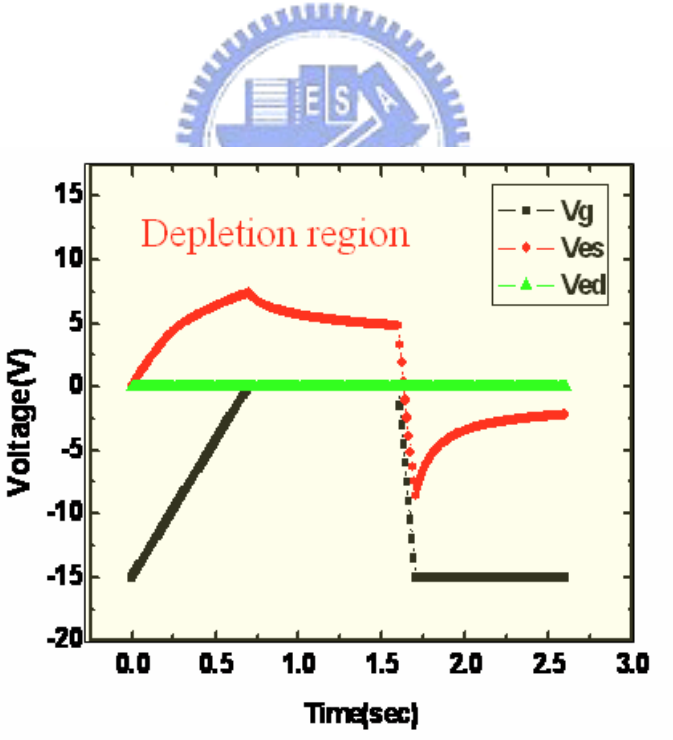

Fig. 3-13(c) Ves and Ved for Vg = -15 V ~ 0 V of Tr = 100 ns, Tf = 700 ns

3.5.4 The Index Π to estimate the degraded degree

In order to describe the degree of the degradation, the index Π calculated from simulation result is also introduced, which is given by replacing *Ve* in equation (2-7) with *Ves*. Similarly, the forward mobility degradation ($1-\mu/\mu_0$) versus the index Π under different AC stress conditions are plotted in Fig. 3-14. The fair linearity exhibits the validity of the proposed mechanism.

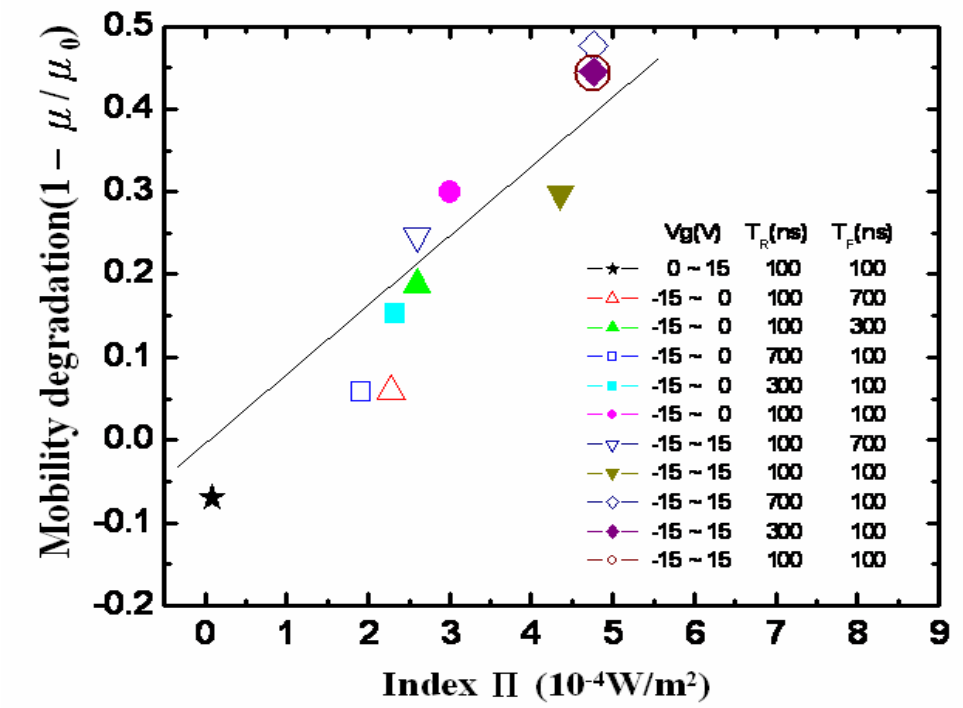

Fig. 3-14 Forward mobility degradation ($1-\mu/\mu_0$) versus Index Π for n-channel TFT

Chapter 4
Conclusion

For AC stress with the gate voltage toggling between -15 V and 15 V, it is observed that the degradation depends on the falling time T_F of the gate pulse but does not depend on the rise time T_R. However, for the gate voltage swinging from -15 V to 0 V, it is observed that the degradation is both influenced by T_R and T_F. A slicing method is used for the simulation of channel voltage distribution and the change in the number of the carriers at the edge to explain the degradation behaviors. A new index Π considering the two factors is introduced and it shows good linearity with the mobility degradation for various gate pulse stress conditions. The universal linearity gives the index a potential modeling for reliability simulation and lifetime prediction of poly-Si TFT circuitry.

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N 型低溫複晶矽薄膜電晶體在閘極交流電壓下的劣化研究

(Study of N-type LTPS TFTs Degradation Under Gate Pulse Stress)