# 國立交通大學

## 光電工程學系 顯示科技研究所


## 碩士論文

# 五環素有機薄膜電晶體可靠度之研究

# Study on the Reliability of Pentacene-Based Organic Thin Film Transistor


研究生：陳弘根

指導教授：劉柏村 博士



中華民國九十五年七月

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# 五環素有機薄膜電晶體可靠度之研究

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## 摘要

在有機薄膜電晶體的技術演進中，其載子遷移率表現出來的電性已經迎頭趕上複晶矽薄膜電晶體的電性了。而其中五環素為電洞導通的有機半導體，載子遷移率最高已高過 $1cm^2/V\,s$，可說已到了單晶有機的傳輸極限了。不過儘管電性已有大幅改善，但是在接面電阻，導通機制和電性上的不穩定這三個方面還未作有系統的探討。

因而在本論文裡，首先我們會利用四點探測法來了解接面電阻。而四點探測是在上源極和汲極結構時，同時製作上去的，而非額外多了兩根測電位的探針製作步驟。因此我們用原本兩個電極(源極和汲極)注入並接收電流，另外通道中的兩個電極來感測電壓。這手法跟最近報導的四點探針電晶體很像。而相較於傳統的電阻對通道長作圖法求接觸電阻，四點探測主要優點是可在單一顆元件上單獨量到薄膜電阻和各接觸電阻，並使得元件元件間在既存在的電阻差異下更容易對此元件作評估。因此我們可利用它來作進一步作現象分析。

接著我們作變溫量測，此可在遷移率與溫度有關的半導薄膜上作量測。在與溫度相關的遷移率中，蘊育著半導體和傳導機制有關或和缺限分布有關的資訊。有一些模型已提出來解釋這些半導晶體中熱活化的載子遷移率現象，然而“Multiple trapping and release model(MTR)”是最為被大家所廣泛接受的。因此我們再利用橫

向電導，可同時來觀測Meyer-Neldel relationship的電性傳輸行為。而我們也適當的利用Multiple trapping and release model(MTR)來解釋變溫量測中過程的熱活化現象。

最後，我們在連續量測中了解到有機薄膜電晶體電性上的不穩定性，進而在定汲極電流的運作下，來探討這五環素有機薄膜電晶體的特性。在此我們也發現極化現象在定電流運作過程中扮演很重要的角色。因此提供簡單的能帶圖來陳述有機薄膜電晶體的特殊行為，而這些是載子受到束縛而在臨界電壓和遷移率上的不穩定現象也都一一會被探討。

# Study on the Reliability of Pentacene-Based Organic Thin Film Transistor

Student: Hung-Keng Chen Advisor: Dr. Po-Tsun Liu

Department of Photonics & Display Institute

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## Abstract

Recent progress in organic thin film transistor (OTFT) technology has led to charge carrier mobility comparable to amorphous silicon. Pentacene, a hole conductor, has shown the highest OTFT mobility(>1 $cm^2/V \cdot s$) to date, and has nearly reached the intrinsic transport limit of organic single crystals. Despite the progress in realizing OTFTs with good properties, three important aspects of OTFTs have not been systematically studied: contact resistance, conduction mechanism, and electrical instability.

In this thesis, at first, we use an improved four-probe method for ascertaining contact resistance. The four-probe method is based on the standard OTFT source and drain geometry, but with two additional mid-channel voltage sensing probes. Thus, we use two electrodes to inject and receive current, and two to sense voltage in the OTFT channel. The technique we employ is similar to other recently reported four-probe transistor devices. The major advantage of the four-probe method over conventional R

vs L plots is that it allows the film and each contact resistance to be measured independently in a single device, which facilitates assessment of device-to-device variation in these resistances. Hence, we use it to further analyze the phenomenon.

Variable temperature TFT measurements are adapted later. It can be used to determine the temperature dependence of the mobility in a semiconductor thin film. The temperature dependence of the mobility can yield information about the conduction mechanism and trap states in the semiconductor. Several models have been proposed to explain thermally activated mobility in crystalline organic semiconductor films, but the multiple trapping and release (MTR) model is the most widely accepted. Thus, a Meyer–Neldel relationship was simultaneously observed for electrical transport, using a transconductance. We properly use the multiple trapping and release model to explain the thermally activated phenomenon from the variable temperature measurement.

Finally, we understand the instability of electrical characteristics in a continued series measurements and investigated the characteristics of bottom-contact pentacene-based OTFTs under drain current stress conditions. Here, we find that polarization phenomenon plays an important role during stress, and thus we provide the rough energy band figure to depict these special properties of OTFTs. The effect of these charge trapping instability on the measured threshold voltage and mobility of the transport studies would be discussed.

# 誌 謝

我的老師:

感謝劉柏村老師，在我的碩士二年生涯中給予我指導，並灌輸給我嚴謹的治學態度和積極的辦事習慣。也要感謝張鼎張老師，在我的研究遇到困難時，能即時提供我再走下去的方向，並在我報告時，給予我關照，叮嚀和指正。

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Figure 4-24:(a)The resistances as a function of drain voltage under gate bias ($V_G$=-30V) for drain side, source side, and channel between probe1 and probe2. (b)The voltage drop of channel between probe1 and probe2, drain side, and source side as a function of drain voltage. They after stress and release would be compared.

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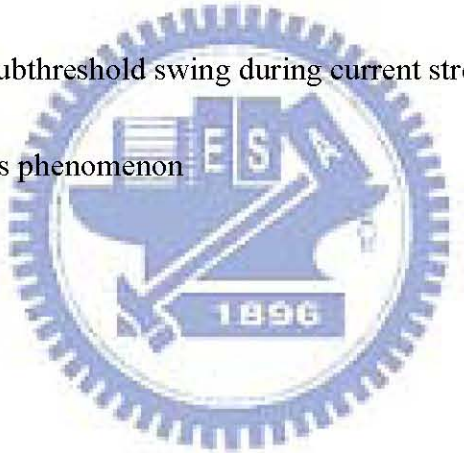


# Chapter 1

# Introduction

## 1.1 Overview of Organic Thin Film Transistor

Electronics based on organic and polymer materials have attracted much attention in recent years. The interest can be attributed to emerging demands in novel electronic devices like radio frequency tags (wireless transponders), smart cards, and display media (active and passive) on low cost and/or flexible substrates. Progress in this field has been sustained by improvements of the material properties [1–3] (see Figure 1-1) and in the development of processing techniques such as printing [4–7], stamping, or other high volume parallel processing technologies. The processing techniques facilitate patterning of organic and inorganic materials without using standard photolithography. Therefore, most of the research has been driven by an interest in low cost electronics.

Currently, hydrogenated amorphous silicon, the most widely used broad area electronic material requires temperatures of 250-350°C for high-quality material deposition and thus requires the use of glass or other high-temperature substrates. Up to now amorphous and polycrystalline silicon have dominated low cost electronics due to low processing temperatures and the application of low cost substrates like glass or flexible foil, which facilitates scaling of the process to larger substrates.

Pentacene, or other organic semiconductors, may allow device fabrication on flexible plastic substrates. For applications such as active matrix liquid crystal displays (AMLCD's), which currently use glass substrates, this would allow displays with decreased weight and improved ruggedness. The use of a flexible substrate could also

dramatically lower fabrication cost by allowing continuous web processing. In addition, although the bonds are often quite strong, individual molecules are held together by relatively weak van der Waals forces. Hence the electronic properties of the material are primarily determined by the molecular properties, potentially making organic devices more tolerant to at least some types of impurities than devices fabricated from covalently bonded inorganic materials.

At present, Pentacene ($C_{22}H_{14}$) has demonstrated the highest hole and electron mobility of organic small molecules. The material exhibits a strong tendency to form highly ordered films which depend on the growth conditions and the substrate. Bulk single crystals are not favorable for low cost electronics, because the fabrication is time consuming and the crystals are small. Thin films are more favorable, because they can be fabricated on various low cost substrates. The hole mobility of thin film pentacene is close to the intrinsic transport limit of bulk single crystals, and thin film transistors (TFTs) with mobility of >1 $cm^2/Vs$ have been fabricated by several groups [2,8–11]. The mobility is therefore comparable with that achieved by amorphous silicon TFTs and hence pentacene TFTs might be considered for large area active matrix arrays. Promising methods for the fabrication of pentacene for low cost electronics on large areas are organic vapor phase deposition [12] and thermal evaporation [8]. In this thesis we focus on thermally evaporated pentacene.

The thermally evaporated material is polycrystalline and has large grains. The diameters are usually in the range of a few microns [8,11,13]. Despite the enormous progress in the realization of TFTs with good properties, the transport mechanism especially of polycrystalline films is not completely understood. In order to investigation, most of organic TFTs so far have been fabricated on thermal oxide coated

crystalline wafers. Thermal oxide on silicon wafers is a favorable substrate for the growth of pentacene, and proper to operate with more stable characteristic.

Pentacene transistor drain-source contacts can be made in one of two configurations—top contact and bottom contact. It has been demonstrated that the bottom contact configuration gives inferior performance to the top contact configuration for a range of deposition conditions and material thickness [14-15]. As a consequence of this behavior, the top contact configuration is almost exclusively studied and reported in the literature. Shadow masking is generally used in the laboratory to define the top contacts made to pentacene, a procedure which does not lend itself well to manufacturing. To create a manufacturable process photolithographically defined drain and source contacts are needed. The performance levels needed for commercial technologies have only been demonstrated in top contact devices, however, and since no photolithography may be performed after pentacene has been deposited, bottom contact devices are the only option for a fully lithographic pentacene process.

## 1.2 Properties of Pentacene

Structure of pentacene is shown in Figure 1-2. Crystals of pentacene are triclinic lattice (see Figure 1-3). The lattice parameters of pentacene were shown in Table1-1. And the other important parameters were described as follows [14-15]:

Pentacene Formula : $C_{22}H_{14;}$

Molecular weight : 278.3;

Melting point: 573 K;

Volume of the unit cell : 705.0 $Å^3$;

Density: 1.303 $g.cm^{-3}$ (calculated with Z = 2) ,

1.30 $g.cm^{-3}$ ( measured ).

Optical Bandgap: 2.8 eV.

Absorption coefficient for X-rays: $\lambda$ = 1.542 nm.

Resistivity: ~$10^{14}$-$10^{15}$ ohm-cm;

We have fabricated organic thin film transistors (OTFTs) using pentacene, a fused-ring polycyclic aromatic hydrocarbon, as the active material. It is typically used as p-type semiconductor. These devices have field-effect mobility comparable to hydrogenated amorphous silicon (a-Si:H) TFTs (> 0.5$cm^2$/V-s). While the bulk electrical conductivity of acenes such as pentacene (~10-15 S/cm) is well known, the field-effect properties of pentacene and many other conjugated materials remain relatively unexplored.

On organic small molecules, pentacene ($C_{22}H_{14}$) has demonstrated the highest hole and electron mobility. Pentacene has a strong tendency to form molecular crystals and when deposited by evaporation will typically form well-ordered films even for low substrate temperatures. With pentacene, for example, ordered films are obtained when deposited by evaporation at temperatures as low as 0°C. This tendency to form ordered films at low temperature may be extremely important.

The material exhibits a strong tendency to form highly ordered films, which, depending on the deposition and substrate conditions, can be poly or single crystalline. In the case of single crystal material, hole mobility of 3.2$cm^2$/V-s and electron mobility of 2.0 $cm^2$/V-s have been realized at room temperature using metal - insulator - semiconductor (MIS) transistor structures. However, the size of the single crystal substrates is relatively small in comparison to large area and/or low cost substrates. A more promising process to realize large area electronics is the thermal evaporation of

the organic material. The thermal evaporated material is poly crystalline with large grain sizes, usually in the range of a few microns. The mobility of polycrystalline transistors at room temperature is about 0.1-1 $cm^2$/V-s, achieving the same range as amorphous silicon.

## 1.3 Operation of Organic Thin Film Transistor

The operation of the pentacene-base OTFT is described below [18]. Organic thin film transistors are opposed to the usual inversion mode operation of silicon MOSFETs and primarily operated as a P-type accumulation-mode enhancement type transistor.

When zero bias was applied to three terminals of OTFT, the carrier distribution is uniform without the electrical field effect, which's schematic diagram is shown in Figure 1-4(a). If applied a small drain bias ($V_D$), in this condition, the source-drain current, ($I_D$), will be not easy to conduct and small enough to neglect .

When a negative bias ($V_G$), is applied to the gate electrode, the voltage is dropped over the insulator and over the semiconductor near insulator/semiconductor interface and accumulate more positive charge in the accumulation region to form a conduction channel. The schematic diagram is shown in Figure 1-4(b). The additional positive charge is supplied by the ohmic source and drain contact and will reduce the resistance of channel. When a small bias is applied on the drain terminal, the source-drain current will form.

In Figure 1-4(c), the schematic diagram shows the depletion mode for device. When a positive bias is applied, the band bending occurs in the semiconductor at the insulator interface. Charge will reject from the interface and depletion region will form.

The channel resistance is large so the source-drain current will smaller than the Mode in Figure 1-4(a). Because of the large band gap, inversion layer cannot be observed in the organic TFTs.

When a negative bias, more than gate bias, is applied to drain electrode in Figure1-4(a), the positive charge near the drain will be swiped in to drain electrode and form a depletion region. The schematic diagram is shown in Figure 1-4(d). This condition is similar to saturation mode of silicon MOSFETs. In this mode the source-drain current will not increase with increase drain bias voltage.

## 1.4 Motivation

Recent focus and attention on organic thin film transistors ( TFTs ) resulted in dramatic performance improvements [1-3]. Earlier literature pointed out that the properties of organic TFTs were highly dependent on the film quality of organic semiconductors, which were determined by pre-layer ' s morphology, surface energy, process temperature, thickness and so on. In the early stage, researches interests on the formation of large poly-grains or single crystal of pentacene film due to that the larger poly grain of pentacene usually have higher mobility. However, the large poly grain is not the only factor to reach high mobility. The detail mechanisms are still under investigated.

Equations describing TFT operation assume ohmic ( negligible resistance ) contacts, which often may not be the case for OTFTs. Recent reports reveal that contact resistance in OTFTs can be of the same order of magnitude or more than the film channel resistance. The traditional method for determining contact resistance involves

making multiple OTFTs with various channel lengths, measuring device resistance versus channel length, and then extrapolating back to zero channel length to determine the contact resistance. For the instability of OTFT, we use an improved four-probe method for simple investigation of contact resistance, comparing it to the variation of length and width. The four-probe method is based on the standard OTFT source and drain geometry, but with two additional mid channel voltage sensing probes.

Despite the enormous progress in the realization of TFTs with good properties, the transport mechanism especially of polycrystalline films is not completely understood. Variable temperature electrical measurements are a will-established means for determining the conduction mechanism in semiconductors. In amorphous and polycrystalline silicon, for example, temperature dependent measurements have been used to determine whether charge transport occurs in extended states, by variable range hopping (VRH) or by multiple trapping and release (MTR). Each of these models predicts a specific temperature dependence of the charge carrier mobility that can be used to identify the underlying conduction mechanism. Therefore, it would be adopted to further investigation on transport mechanism.

Besides, electric stability of OTFTs during long time operation is another important needed subject of research. Typically, the instabilities are observed as a shift of the threshold voltage ($\Delta V_{th}$) accompanied by a possible change in the charge carrier mobility, which is due to charge trapping at the gate insulator– dielectric interface or at defect sites in the active layer itself. Both change are found in pentacene-based TFTs. Also the origin of the changing threshold voltage is not known, which complicates both the analysis of the transport properties and depredates potential use of organic TFTs in applications. Therefore, we applied the current stress and attempted to analysis

instability phenomenon and explain trapping charge mechanism during stress.

## 1.5 Thesis Organization

This thesis addresses the investigation of the reliability on the pentacene-based OTFT. The organization is as followings.

In chapter 1, we introduce the background of organic thin film transistor.

In chapter 2. First, we took the simple material measurements to understand the crystallization and growth mechanisms of pentacene through deposition . Pentacene was thermal evaporated at different substrate temperatures. The film quality was characterized by atomic force microscope ( AFM ) , scan electron microscope ( SEM ) and referenced X-ray diffraction ( XRD ). They help us to further understand the crystallization process for pentacene under our fabrication and check the phenomenon depicted on paper at the same time . Next, for the instability of OTFT, we use an improved four-probe method for facilitating investigation of contact resistance, and compare to the electrical characteristics of devices with different length and width. The four-probe method is based on the standard OTFT source and drain geometry, but with two additional mid-channel voltage sensing probes. Thus, we use two electrodes to inject and receive current, and two to sense voltage in the OTFT channel. The major advantage of the four-probe method over conventional R vs L plots is that it allows the contact resistance at source side, drain side and in channel to be measured independently in a single device, which facilitates assessment of device-to-device variation in these resistances.

In chapter 3, variable temperature electrical measurements are a will-established

means for determining the conduction mechanism in semiconductors. Variable temperature TFT measurements can be used to determine the temperature dependence of the mobility in a semiconductor thin film. The temperature dependence of the mobility can yields information about the conduction mechanism and trap states in the semiconductor. Several models have been proposed to explain thermally activated mobility in crystalline organic semiconductor films, but the multiple trapping and release (MTR) model is the most widely accepted. We properly use the multiple trapping and release model to explain the thermally activated phenomenon .

In chapter 4, we found the instability of electrical characteristics in a continued series measurements and further investigated the characteristics of bottom-contact pentacene-based OTFTs under the condition of drain current stress. Here, we find that polarization phenomenon play an important role during stress, and thus we provide the rough energy band figure to depict these special properties of OTFTs. The effect of these charge trapping instability on the measured threshold voltage and mobility on the transport studies are discussed.

In chapter 5, we concludes all results and provide further recommendations.

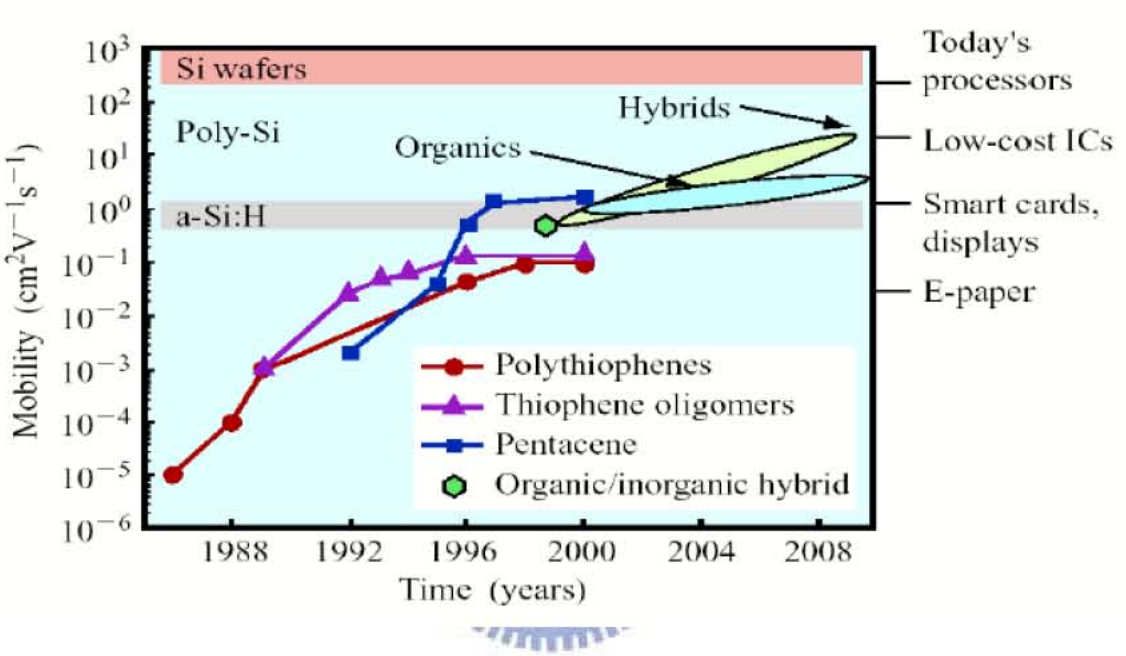



Figure 1-1: Mobility of organic semiconductors have improved by five orders of magnitude over the past 15 years. Large research efforts using materials such as these led to some of this increase.

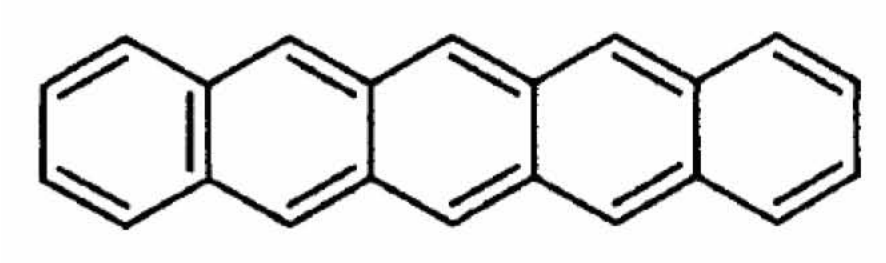
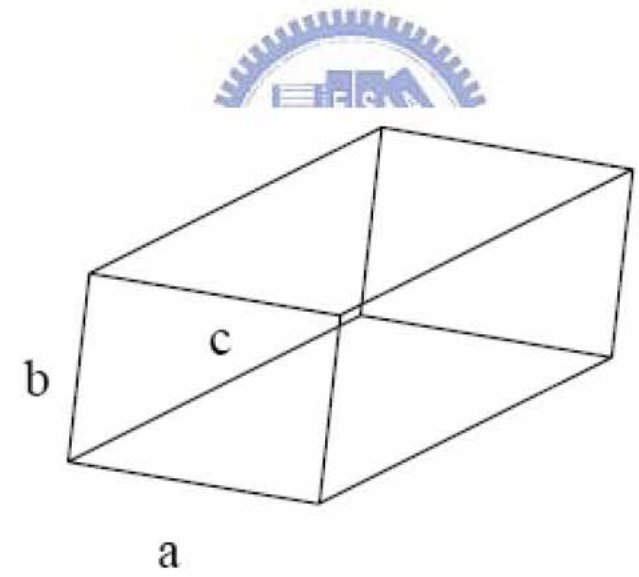


Figure 1-2: Pentacene molecular structure




$$a \neq b \neq c,$$

$$\alpha \neq \beta \neq \gamma \neq 90^{\circ}$$

Figure 1-3: Triclinic lattice

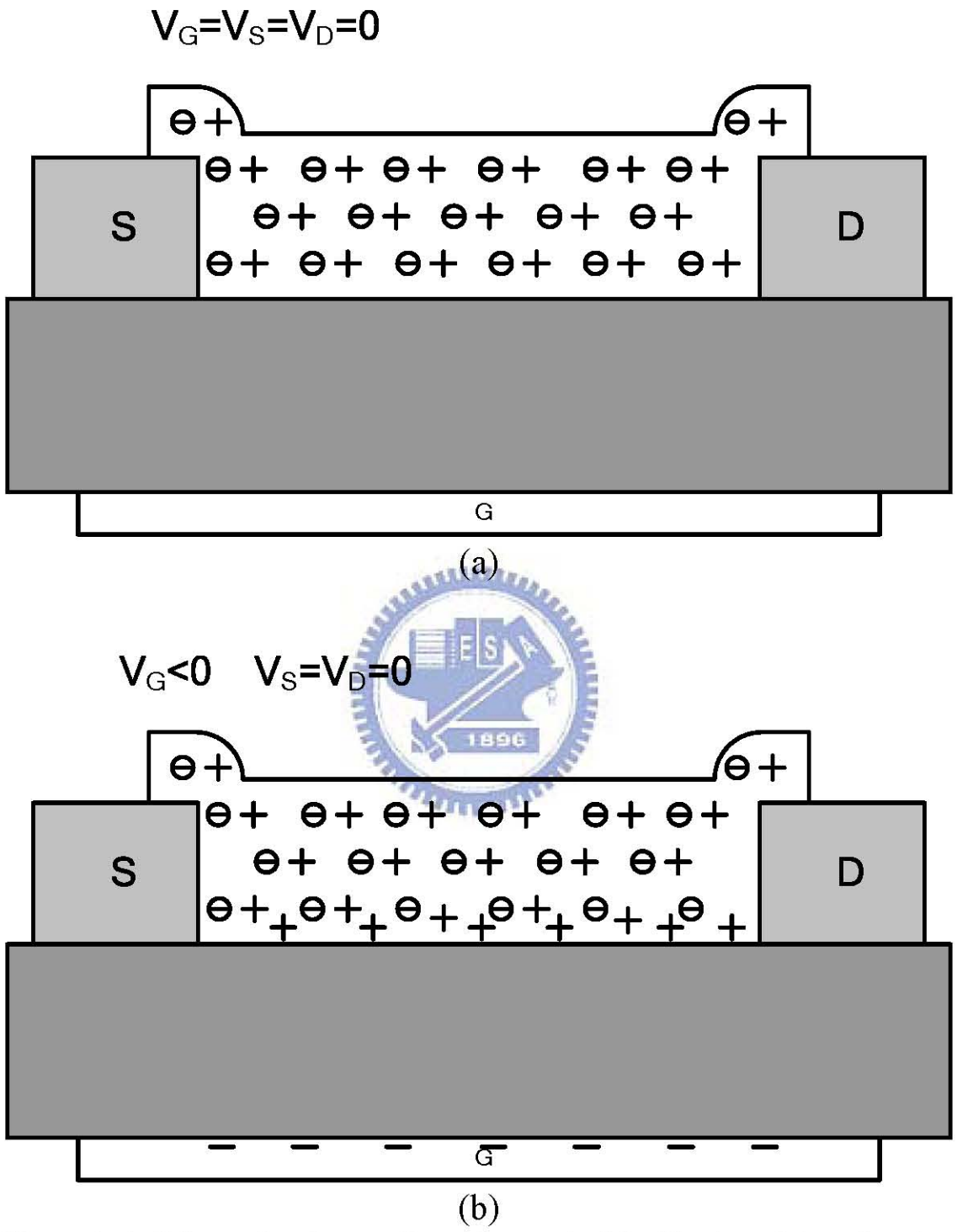
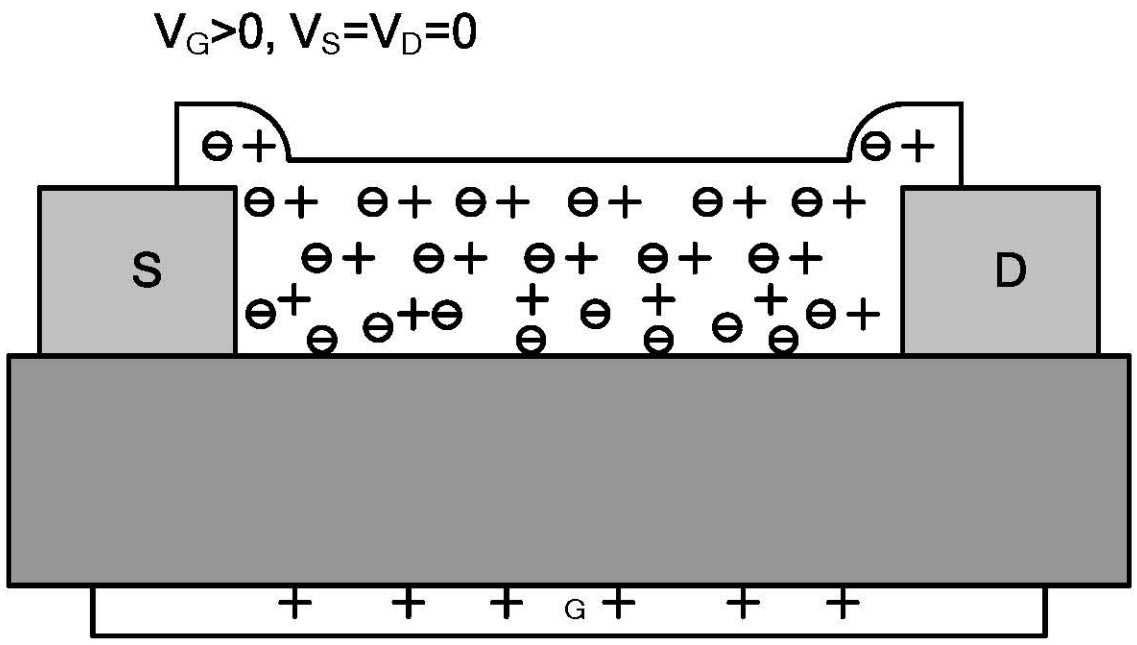
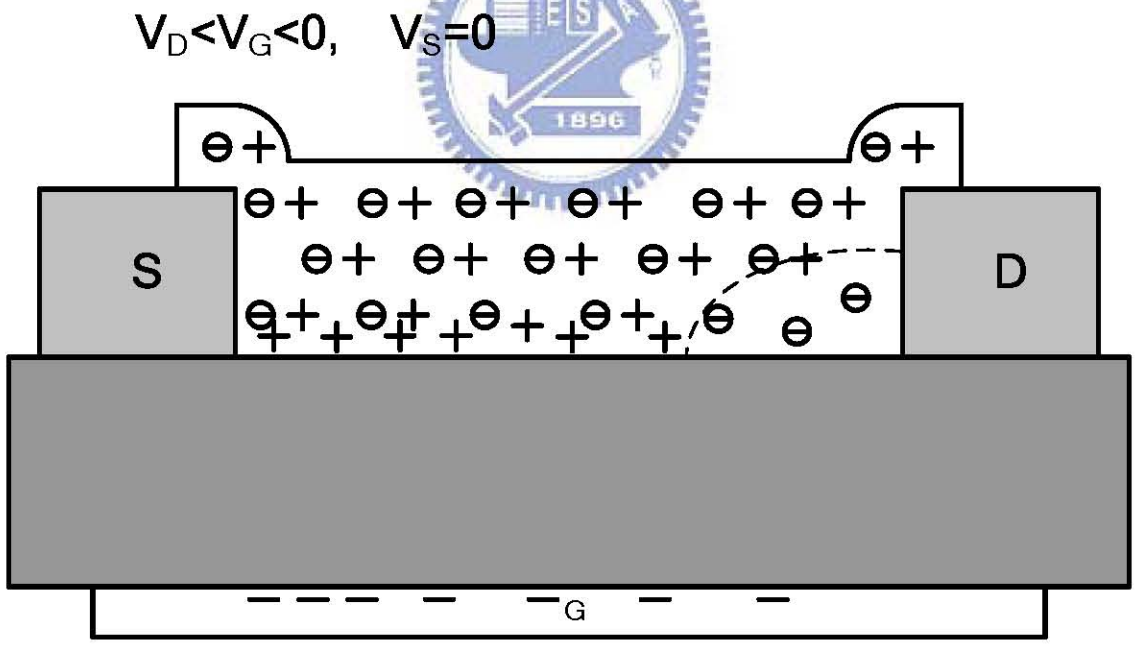



Figure 1-4: Schematic of operation of organic thin film transistor, showing a lightly p-doped semiconductor: + indicates a positive charge in semiconductor ; - indicates a negatively charge counterion (a)no-bias (b) accumulation mode (c)depletion mode (d)channel pinch-off (continue)




(c)




(d)

Figure 1-4: Schematic of operation of organic thin film transistor, showing a lightly p-doped semiconductor: + indicates a positive charge in semiconductor; - indicate a negatively charge counterion (a)no-bais (b) accumulation mode (c)depletion mode (d)channel pinch-off

| Oligomer materials | Channel | Thin film deposition | Mobility ($cm^2$/V-s) | Comments |
|---|---|---|---|---|
| ***α***-6T (***α***-hexathienylene) | p-type | Vacuum evaporation | 0.01~0.03 | Highly purified oligomers |
| ***α***-6T | p-type | Single crystal | 0.075 | |
| DH-***α***-6T (dihexyl-***α***-6T) | p-type | Vacuum evaporation | 0.03~0.05 | Thermal annealing at 100~250°C |
| **Pentacene** | p-type | Vacuum evaporation | 0.06~2.1 | Substrate at T>25 °C |
| **Pentacene** | p-type | Solution cast | $10^{-5}$~$10^{-3}$ | |
| **Pentacene** | p-type | Single crystal | 3.2 | |
| $C_{60}$ (fullerene) | n-type | Vacuum evaporation | 0.08 | |
| TCNQ (tetracyanoquinodimethane) | n-type | Vacuum evaporation | $10^{-10}$~$10^{-4}$ | |
| NTCDA | n-type | Vacuum evaporation | 1~3x$10^{-3}$ | Substrate at T=55°C |
| PTCDA | n-type | Vacuum evaporation | $10^{-5}$~$10^{-4}$ | |
| $F_{16}$CuPc | n-type | Vacuum evaporation | 0.03 | |

Table 1-1: Thin film transistor performances for different oligomer active layers

# Chapter 2

# Devices Fabrication and Four Probe Measurement

## 2.1 Introduction

Recent focus and attention on organic thin film transistors ( TFTs ) resulted in dramatic performance improvements [19-21]. Earlier literature pointed out that the properties of organic TFTs were highly dependent on the film quality of organic semiconductors, which were determined by pre-layer's morphology, surface energy, process temperature, thickness, and so on [22]. In the early stage, researches interests on the formation of large poly-grains or single crystal of pentacene film due to that the larger poly grain of pentacene usually have higher mobility. However, the large poly grain are not the only factor to reach high mobility [22]. The detail mechanisms are still under investigated.

In one part of this chapter, we took the simple material measurements to understand the crystallization and growth mechanisms of pentacene through deposition. Pentacene was thermal evaporated at different substrate temperatures. The film quality was characterized by atomic force microscope ( AFM ), scan electron microscope ( SEM ) and reference X-ray diffraction ( XRD ). They help us to further understand the crystallization process for pentacene under our fabrication and check the phenomenon depicted on paper at the same time.

On the other hand, we report on OTFTs based on pentacene and specifically focus

on characterizing the contact resistance, and the voltage drop between channel. Equations describing TFT operation assume ohmic ( negligible resistance ) contacts, which often may not be the case for OTFTs [23]. Recent reports reveal that contact resistance in OTFTs can be of the same order of magnitude or more than the film channel resistance [24-26]. Katz et al. noted that contact resistance played a key role in the operation of n-channel OTFTs [27]. The traditional method for determining contact resistance involves making multiple OTFTs with various channel lengths, measuring device resistance versus channel length, and then extrapolating back to zero channel length to determine the contact resistance.

In the another part of this chapter, we use an improved four-probe method for facilitating investigation of contact resistance, and compare to the electrical characteristics of devices with different width and length. The four-probe method is based on the standard OTFT source and drain geometry, but with two additional mid-channel voltage sensing probes. Thus, we use two electrodes to inject and receive current, and two to sense voltage in the OTFT channel. The technique we employ is similar to other recently reported four-probe transistor devices [28-30]. The major advantage of the four-probe method over conventional R vs L plots is that it allows the contact resistance at source side, drain side and in channel to be measured independently in a single device, which facilitates assessment of device-to-device variation in these resistances.

## 2.2 Devices Fabrication and Measurement

### 2.2.1 Process Flow of Pentacene-Based OTFT Fabrication

***Film Growth and Characterization***

Thin films of pentacene were prepared by thermal evaporation from an boron crucible onto the transistor test substrate consisting of dummy silicon wafer of low resistivity (1-100 Ω-cm), and a 200 nm thick thermal oxide layer grown in furnace. The base pressure in the evaporation system was about $10^{-7}$ torr. Film thickness was measured by a calibrated quartz crystal monitor. The substrate holder held at constant temperature during deposition. The different substrate temperatures ($T_S$) were investigated into 25°C, 70°C, 120°C, and 150°C.

After deposition, the sample was determined by atomic force microscopy (AFM) and Scan electron microscope (SEM). Film grain structure and morphology were examined using atomic force microscopy. A Digital Instruments Multimode AFM was used in tapping mode, and all images were taken in ambient conditions. Figure 2-2 shows an atomic force topography of a 650-Å-thick pentacene film grown at $T_S$=70°C. Sometimes, the thickness of the film was determined by scan electron microscope (SEM) in order to calibrate quartz crystal monitor.

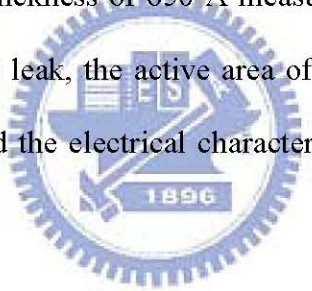
***Device Fabrication***

A bottom gate, inverted staggered transistor structure was used to characterize the pentacene thin films. The cross section of four probe structure is shown schematically in Figure 2-8. The gate and insulator layers consisted of 2000 Å thermally deposited silicon oxide on a dummy silicon wafer of low resistivity (1-100 Ω-cm) in furnace. The measured capacitance of the thermal oxide layer was about 17 nF/cm$^2$, which compares

well with the theoretical limit of 17.26 nF/cm$^2$. Source and drain electrodes were defined by thermal evaporation of metal through a shadow mask onto thermal oxide.

The contact metal of a patterned gold layer formed ohmic contacts as the four probe structure, including of the source, drain electrodes, sense probe1 and sense probe2, were investigated. The typical thickness of the contact metal was 600 Å for gold. It noted that the transistor channel width (W) range from 1000um to 50 um with the length (L) between 1000um and 40um.

The organic TFTs are prepared by evaporated pentacence on a transistor structure of bottom contact in thermal coater. The base pressure in the evaporation chamber was $10^{-6}$ torr, and stayed below $10^{-7}$ torr during deposition. Thin films of pentacene were thermally evaporated up to a thickness of 650 Å measured by calibrated quartz crystal monitor. To minimize parasitic leak, the active area of pentacene film was defined by shadow masking. We measured the electrical characteristics of OTFT as soon as after fabrication.



## 2.2.2 Electrical Characteristics of Pentacene-Based OTFTs

***Measurement***

The electrical characterization was measured in probe station with semiconductor parameter analyzer of E5270B at room temperature in atmosphere around dark environment. All measurements were carried out in an electrically shielded box. Drain current was measured by using semiconductor parameter analyzer of E5270B. Figures 2-10 and 2-11 show the transfer curves and the output characteristic, respectively, for a pentacene base TFT with the thermal oxide insulator and Au contacts.

In the output characteristics, the drain-source current, $I_{DS}$, was measured as a

function of the drain-source voltage, $V_{DS}$, to observe FET-like characteristics. In the transfer curve, drain current also was measured as a function of the gate voltage, $V_D$= -5V, which was constructed to determine the gate bias modulation of the FET conductive channel and at the drain voltage of -15V, which are usually present for OTFT.

Some parameters were extracted from the experimental I-V curves: the transistor threshold voltage ($V_{th}$), the current modulation (the ratio of the current in the accumulation mode over the current in the depletion mode, also referred to as ON-OFF current ratio), and the field effect mobility (μ). The $V_1$ and $V_2$ between channel was sensed by probe 1 and probe 2 at the same time. Furthermore, we can use the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon. The detail extraction method will be discussed in the following sections.

***ON-OFF Ratio***

Inorganic semiconductors, such as Si or Ge, can be operated in three modes: depletion mode, accumulation mode, and inversion mode. For organic semiconductors such as pentacene-based OTFTs, they can not be operated in the inversion mode. Therefore, pentacene-based OTFTs were turned ON in the accumulation mode ( $V_G$<0, see Figure 1-4(b) ) and were turned OFF in the depletion mode ( $V_G$>0, see Figure 1-4(c) ).

Therefore, the ratio of the current in the accumulation mode over the current in the depletion mode also refers to as ON-OFF current ratio. We think it as the ratio of the maximum drain current under accumulation region to the minima current under depletion region.

***The Extraction Methods of Mobility and Threshold Voltage***

Linear and saturation regime mobility is calculated based on standard TFT equations [31]. Pentacene-based OTFT is PMOS like FET. Therefore, the field effect mobility in the linear regime can be obtained by the calculation described below.

At low drain voltage ($V_D$), source-drain current ($I_{DS}$) increases linearly with $V_D$ (linear regime) and is approximately determined from the following equation (2-1):

$$I_D = \frac{W}{L}\mu C_{ox}(V_G - V_{th})\,V_D \cdots for\cdot\cdot linear\cdot\cdot region \qquad (2\text{-}1)$$

where L is the channel length, W is the channel width, $C_{ox}$ is the capacitance per unit area of the insulating layer, $V_{th}$ is the threshold voltage, and μ is the field effect mobility, which can be calculated in the linear regime from the transconductance,

$$G_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=connst} = \frac{WC_{ox}}{L}\mu V_D \cdots for\cdot\cdot linear\cdot\cdot region \qquad (2\text{-}2)$$

by plotting $I_{DS}$ versus $V_G$ at a constant low value of $V_D$, with $-V_D \ll -(V_G - V_{th})$, and equating the value of the slope of this plot to $G_m$. We can compute the linear regime mobility from equation (2-2). Threshold voltage ($V_{th}$) was determined from a linear plot of drain current ($I_D$) versus gate voltage ($V_G$) extrapolated to the *x*-axis intercept.

On the other hand, the field effect mobility in the saturation regime can be obtained by the calculation described below. At high drain voltage, source-drain current increases with the square of ($V_G$-$V_{th}$) (saturation regime) and is approximately determined from the following equation (2-3):

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_G - V_{th})^2 \cdots for\cdot\cdot saturation\cdot\cdot region \qquad (2\text{-}3)$$

where L is the channel length, W is the channel width, $C_{ox}$ is the capacitance per unit area of the insulating layer, $V_{th}$ is the threshold voltage, and μ is the field effect mobility,

which can be calculated in the saturation regime from the transconductance,

$$G_m = \left.\frac{\partial\sqrt{I_D}}{\partial V_G}\right|_{V_D=connst} = \sqrt{\frac{1}{2}\frac{WC_{ox}}{L}\mu} \cdots for \cdot\cdot saturation \cdot\cdot region \qquad (2\text{-}4)$$

by plotting $I_{DS}$ versus $V_G$ at a constant high value of $V_D$, with $-V_D >> -(V_G - V_{th})$, and equating the value of the slope of this plot to $G_m$. We can compute the saturation regime mobility from equation (2-4). Threshold voltage ($V_{th}$) was determined from a linear plot of square root of drain current ($\sqrt{I_D}$) versus gate voltage ($V_G$) extrapolated to the *x*-axis intercept.

For most devices, transfer curves were taken in 0.92 V gate steps from 10 V up to -35 V. The devices made in our lab had mobility as high as 1.574 and 1.142 $cm^2$/V-s in linear region and saturation region respectively at temperature of 70°C, as shown in Figure 2-10 and 2-11. The threshold voltages ranging from -10V to 10 V depending on the device (see the Figure 2-10: $V_{th}$= -8.1V in linear region and $V_{th}$ = -2.6V in saturation region), and on-to-off current ratio (on/off) about $10^6$. We were able to fabricate devices of this quality several times, but observed some variability from run to run. The drain current of the transfer curve measured as a function of gate voltage at drain voltage of -5V and -15V. Later, the output characteristics is taken at gate voltage $V_G$= -10 and VG= -30V. The $V_1$ and $V_2$ between channel was sensed by probe 1 and probe 2 at the same time. In four-probe measurements, floating potentials of two mid-channel sensing probes were measured using Aglient E5287 (high resolution SMU module ) with the zero current source. Furthermore, we use the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon.

Finally, the sample would be stored carefully in dry cabinet to avoid moisture and pollution after measurements.

## 2.3 Results and Discussions

### 2.3.1 The Growth of Pentacene

Film grain structure and morphology were examined using atomic force microscopy after deposition of pentacene on thermally oxide silicon substrate. A Digital Instruments Multimode AFM was used in tapping mode, and all images were taken in ambient conditions.

The most of difficulties to analyze the properties of pentacene based TFTs is the uncertain reproducibility. Therefore, the study on the properties of pnetacene TFTs sometimes focused on the qualitative analysis rather than quantitative analysis. Figure 2-1, 2-2, and 2-3 denotes the surface morphology of pentacene at different substrate temperatures of 25°C, 70°C, and 120°C, respectively. Figure 2-1 and 2-2 shows an atomic force topography of a 650-Å-thick pentacene film grown at the different substrate temperature of 25 and 70 °C. The morphology of grain is similar but the grain size are smaller at lower substrate temperature of 25°C. In Figure 2-2 and 2-3, pentacene films grown at the substrate temperature of 70°C and 120°C have similar grain sizes about 2.5um, observed by optical microscopy and AFM. Additionally, there are some different about the morphology of grain boundary. Obviously, the sizes of ploy grains gradually increase from 0.5um to nearly 2.5 um when substrate temperature increases in process.

The phenomenon was also observed by C.D. Dimitrakopoulos et al [32]. At very low substrate temperature, the rod-like pentacene molecules do not have sufficient momentum to move during deposition, thus the molecules would immediately stick

when they reach the surface of substrate, therefore forming an amorphous type in film structure. When the substrate temperature increases, the pentacene molecules have enough momentum to arrange a will-ordered crystalline structure, therefore a ploy crystalline morphology would be observed. In our experiments, the room temperature sample formed a poly crystalline morphology with smaller poly grains, as shown in Figure 2-1. When substrate temperature approach at 70°C or ,even more, 120°C, the grain size was growing about 2.5um (see Figure 2-2 and 2-3).

It is interesting to find the variation of morphology in grain boundary. At temperature of 25 and 70°C, the grain size is textured with micron-sized, terraced dendritic grains. However, at the temperature of 120 and 150°C, the film get together with many pieces like crystal piece.

We can further investigate by the nucleation process of pentacene at subtract temperature of 150°C, as shown in Figure 2-4, 2-5 and 2-6. IBM reported that the pentacene growth mechanism would be divided into three steps [33]. First, the resolution limit step, pentacene molecules form the crystalline seeds in the beginning. The resolution strongly depends on the interaction between pentacene molecules and surface molecules of substrate. Second, the diffusion limit aggregation step, where molecules diffuse on a surface and stick to any existing island, without further diffusion. Third, the coarsening step, the pentacene islands coarsen until the grains touch each other. We monitor the nucleation process of pentacene (see Figure 2-4, 2-5, and 2-6) and find that the grown of pentacene is crystalline pieces but dendritic in shape during deposition. Hence, we find papers which depict about this phenomenon.

The surface morphology of the thin films was studied by x-ray diffraction (XRD). Figure 2-7 shows a typical X-ray diffraction of pentacene thin film taken on paper [34]

and XRD pattern illustrates the crystalline order in the films. There is the crystalline phase of so-called " thin film phase" with d(001') value of 15.4 Å, which give the first order diffraction peak at 5.7°. But in the oxide case, another crystalline phase of so-called "single crystal phase" with d(001) values of 14.4 Å at the peak range from 5.9-6.2° appears. Pentacene grown on the oxide mixes two crystalline phase.

In Figure 2-7, the sharp primary peak at $2\theta$ =6.10° assigned to (001) corresponds to a distance spacing of 14.4 Å. There is a second smaller peak at $2\theta$ =12.22°, which corresponds to the second order reflection (002) of the primary peak. In thicker films, more high order (00*k*) peaks are observed. In films grown with low substrate temperature, XRD reveals another set of peaks (00k') based on a different primary peak with the longer distance spacing. In films grown at the substrate temperature of 25°C and 70°C, the major part was (00*k*') peaks in the mixture phase, and almost only (00*k*) peak sets were observed at 150°C. Thereby, we can tell the difference in shape of grain boundary. At temperature of 25 and 70°C, the grain size was texture with micron-sized, terraced dendritic grains. However, at the temperature of 120 and 150°C, the film got together with many pieces of crystal pieces.

The single crystal structure of pentacene reveals $\pi$ stacking in a triclinic structure with a *c*-axis length of 16.01 Å, which corresponds well to the (00*k*) distance spacing of 14.4 Å . We find that it would be thin films grown at 150°C. Therefore, the (00*k*) film ordering corresponds to single crystal-like packing, with the c-axis parallel to the surface normal. We attribute the (00k') peaks observed at low substrate temperature to a ''thin film phase'' of pentacene. The thin film phase may be a metastable growth-limited phase or a thermodynamically stable polymorph. These thin film polymorphs have also been observed in the previous research of pentacene [35]. The

TFTs based on mixed phase films exhibited inferior transistor performance.

In a short summary, pentacene crystallization as a continuous film was influenced by substrate temperature, morphology and different phase. Although many approaches were proposed to enhance pentacene grain growth, however larger poly grains do not mean better electrical properties. A good interface between pentacene and gate dielectric layer is another key factor. In material, however, a single phase of pentacene crystal is preferred for carrier transport due to the lack of interference between two kinds of orientation of pentacene molecules.

### 2.3.2 Four Probe Measurement

Contact resistance was investigated in TFTs by two different methods: (1) Four-probe conductance measurements on operating TFTs, and (2) resistance versus channel length ($R$ vs $L$) plots. Both techniques have been used to study contact resistance in $a$-Si TFTs [32], however, they are not widely used in organic TFT research. In our four-probe conductance measurements, voltage sensing probes were evaporated simultaneously with the source and drain electrodes in the staggered structure ( see Figure 2-8 ). Figure 2-9 shows a schematic of the four-probe geometry used to determine film and contact resistance in operating pentacene-based TFTs. The probes are typically 10 um in width, and penetrate into the channel one fifth of the width. The sensing probes make up less than 10% of channel length and locate at one third and two third of channel length. The small geometric footprint and staggered geometry of the sensing probes minimize impact to the operating TFT.

The sense probes float at a voltage ($V_1$ ,$V_2$) corresponding to the channel voltage at that position; thus, the voltage drop at the source and drain electrodes (due to carrier

injection) can be determined by extrapolating the channel voltage gradient back to the source and drain. Figure 2-12 shows a schematic of the voltage profile determined from a four-probe TFT measurement. The voltage drops between the probe1 and probe2 ($\Delta V_{film}$), are calculated by the following equations:

$$\Delta V_{film} = V_2 - V_1$$

The voltage drops at the source and drain electrode ($\Delta Vs$ , $\Delta V_D$ ), are calculated by the following equations:

$$\Delta Vs = [V_1 - (V_2 - V_1)/(L_2 - L_1) \times L_1] - Vs \quad (2\text{-}5)$$

$$\Delta V_D = V_D - [V_2 - (V_2 - V_1)/(L_2 - L_1) \times (L - L_2)] - Vs \quad (2\text{-}6)$$

where $V_S$, $V_D$, $V_1$, $V_2$ are the voltages at the source, drain and sense probes, respectively, and $L_1$ , $L_2$ , and L are distances measured from the source electrode to the first probe, the second probe, and drain electrode respectively. These voltage drops represent the voltage required to inject carriers into the film.

In Figure 2-13, plot of sense probe ($V_1$ ,$V_2$) and source/drain voltage drops ($\Delta V_S$ , $\Delta V_D$) as a function of gate voltage. The data correspond to transfer curve in Figure 2-10 operating with $V_D$= -5 V and $V_D$= -15 V. We can find the voltage drop across the channel would increase with the rising gate voltage due to induce channel conduction. In the beginning, the increasing gate voltage from small value lets the longitudinal field enough to form the depletion region at fix drain voltage as shown in Figure 2-14(a) and gate voltage induces the weakly band bending at source side. When the gate voltage become high, the band bending lets the voltage drop at source side increasing, but eased depletion region at drain side leading to the voltage drop decreasing as shown in Figure 2-14(b). It is additionally noted that the reasons for voltage drop at contact maybe the

schottky barrier, organic dipole barrier, depletion region and the access resistance at contact .

Using the drain current and sense probe data, the contact resistance can be calculated using

$$Rc=(\Delta V_D+\Delta V_S)/I_D=R_D+R_S \quad (2\text{-}7)$$

Separating source ($R_S$) and drain ($R_D$) contact resistances can be similarly determined, and this is an advantage of the four probe technique compared to R vs L plots, which lump both source and drain contact resistance together. The film resistance ($R_{film}$) is calculated according to

$$R_{film}=\Delta V_{film}/I_D \quad (2\text{-}8)$$

where $\Delta V_{film}$ is the voltage drops between the probe1 and probe2. Figure 2-15 shows the plots of film resistance, source resistance, drain resistance and total contact resistance as a function of gate voltage for an operating OTFT. The data correspond to the device in Figure 2-10 operating at room temperature with $V_D$= -5 V and $V_D$= -15 V. $R_S$ decreases weakly with increasing gate voltage, while $R_D$ and $R_{film}$ decrease significantly and soon line out. The decreasing resistance is originated from the more carrier concentration. The difference between Figure 2-15 (a) and (b) is the different drain voltage of -5V and -15V. When the applied drain voltage is -5V, smaller than -15V, it leads to the depletion region at drain side reduced. Therefore, the drain resistance at $V_D$= -5V is obviously smaller than at $V_D$= -15 V as shown in Figure 2-16.

Sense probe data are only valid for characterizing contact resistance in the linear regime of TFT operation. In the saturation regime, the pinch off effect (non uniform channel electric field) complicates the voltage profile but we can still use them due to long channel which minimized the effect of the non uniform channel electric field. Next,

we double check these voltages and resistances as function of drain voltage. In figure 2-17, the plot of sense probe ($V_1$ ,$V_2$) and source/drain voltage drops($\Delta V_S$ , $\Delta V_D$) as a function of drain voltage. The data correspond to the device in Figure 2-11 operating at room temperature with $V_G$= -10 V and $V_D$= -30 V. In the beginning, the voltage drops of all increase with the applied drain voltage rising . When the channel pinch off at drain side, the voltage drops at source side and the voltage sensed from probe1 and probe2 would enter into the saturation condition. In contrary, the voltage drop at drain side would go up abruptly. Therefore, the resistance at drain side should increase abruptly as the channel pinches off, as shown in Figure 2-18. the plots of film resistance, source resistance, drain resistance and total contact resistance as a function of drain voltage for an operating OTFT. The data correspond to the device in Figure 2-11 operating at room temperature with $V_G$= -10 V, $V_G$= -30 V. In the same way, the film resistance and the resistance at source side would increase with rising drain voltage till the channel pinches off.

Similar to the four-probe result, the contact resistance measured conventionally by *R* vs *L* plots is observed to decrease with increasing gate voltage (carrier concentration). TFTs using *R* vs *L* plots has shown that contact resistance decreases with increasing carrier concentration [36-38]. There is also well-documented evidence of decreased $R_C$ with decreased $R_{film}$ (increased carrier concentration, or increased mobility) in amorphous silicon TFTs [39]. Thus, it is important to note that when comparing contact resistance determined from four-probe and *R* vs *L* plots, the devices must have similar mobility and threshold voltage.

### 2.3.3 Sensitivity to Deposition Substrate Temperature

We can further investigate on the OTFT for different substrate temperature during

deposition by four probe structure. The transfer characteristics $I_D$-$V_G$ at the drain voltages of -5V are compared with the different substrate temperature of 25°C and 70°C. We also have simultaneously the comparison of the output characteristics $I_D$-$V_D$ with different deposition temperature of 25°C and 70°C at the gate voltages of -10V and -30V, separately. In traditional analysis, the electrical characteristics of OTFT at the temperature of 70°C would be better, including of higher on-current, better mobility, and smaller subtresold swing as shown in Figure 2-19 and 2-20.

In Figure 2-21, we can have the comparison of film resistance, source resistance and drain resistance as a function of gate voltage with different deposition temperature of 25 °C and 70 °C for an operating OTFT. The data correspond to the device in Figure 2-19 operating at room temperature. The smaller film resistance was affected by high quality and large grains at the higher substrate temperature rightly. At the same time, it is interesting to find that the resistance at drain and source side reduced more obviously. It imply that the higher substrate temperature not only improve the thin film growth, but also help the connection of the contact between metal and semiconductor. Bottom contact devices consistently gave much higher contact resistance, which may be associated with poor semiconductor film morphology around the metal 0electrodes [40]. However, it can be improved by the increasing the substrate temperature during deposition.

We can double check these resistances as function of drain voltage as shown in Figure 2-22 and 2-23. Similar to the result of the resistance as function of gate voltage, the film resistance and the contact resistance is observed to decrease with increasing substrate temperature.

### 2.3.4 The Effect of Scaling

At first, we compared with the electrical characteristics for the different lengths of device. Figure 2-24 shows the transfer characteristics of the device at drain voltages $V_D$= -5V and $V_D$= -15V, and the output characteristics at gate voltage $V_G$= -10 and $V_G$= -30V, compared with the length of 1000um, 500um and 100um.

As we known, the drain current with the longer length for device would be lower. However, we have the investigation on the threshold voltage versus length under drain bias ($V_D$= -5V and -15V), in linear and saturation region respectively, and the effect of threshold voltage shift toward positive is observed in Figure 2-25. In the other word, the OTFT is easy to turn on or normally on like the short channel effect even if the smallest length still keeps with 40um. It is also surprised to observe Figure 2-26 (a). The subthreshold swing versus length under the drain voltage of -5V and -15V is strongly dependent on length even if the instability of OTFT still exists. Hence, the phenomenon of normally-on current is the significant reason for bad subthreshold swing due to the poor gate voltage controlling. In Figure 2-26 (b), the linear and saturation mobility versus length under drain bias ($V_D$= -5V and -15V) also depicts that the trend of curve downward with the decreasing length.

It implies that the electrical characteristics are strongly dependent on the effect of length. Figure 2-26(b) and 2-25 shows the variation of extracted mobility and threshold voltage versus channel length for organic devices. As expected, for OTFTs the extracted mobility decreases at shorter channel lengths [23]. Because of a large drain-source voltage drop at source/drain series resistance in comparison to the channel resistance for a shorter channel-length OTFT (the channel resistance is smaller), this results in a lower extracted mobility. For a longer channel-length OTFT, e.g. L=1000um,

the channel resistance is much larger than source/drain series resistances, and the extracted mobility approaches its intrinsic mobility value (1.17 cm /Vs).

In addition, the percentage of total device resistance indicated as $R_{film}$% is a convenient gauge to understand the effect how contact resistance affects in device performance. We defined that,

$$R_{film}\% = \frac{R_{film}}{Rtot} = \frac{R_{film}}{3R_{film} + R_D + R_S} \tag{2-9}$$

Therefore, two kinds of devices with length (1000 um and 500 um) would be compared with the percentage of the film resistances. In Figure 2-27(a), the percentage of the film resistances as a function of gate voltage under drain bias ($V_D$= -5V and -15V), the percentage of the film resistance with L=1000um is more than with 500um. It depicts that there is the larger portion of the contact resistance in the shorter channel of 500um, rather than 1000um. For the same reason, the percentage of the film resistances as a function of drain voltage under gate bias ($V_D$= -10V and -30V) in Figure 2-27(b) show the similar result.

Then, we compare with the electrical characteristics for the device with different widths. Figure 2-28 shows the transfer characteristics of the device at drain voltages $V_D$= -5V and $V_D$= -15V, and the output characteristics at gate voltage $V_G$= -10 and $V_G$= -30V, compared with the device width of 1000um, 500um, 100um and 50um. Similar to the general result of TFT, the current with the narrower width for device would be lower. Next, we observe the subthreshold swing versus width and the threshold voltage versus width under drain bias ($V_D$= -5V and -15V) as shown in Figure 2-29. It is unfortunate to find that there is no relation with the different width, maybe due to instability of device.

In Figure 2-30, the linear and saturation mobility versus width under drain bias

($V_D$= -5V and -15V) also have the trend of curve upward with the decreasing width. We take the further investigation on this phenomenon by normalize resistance and the percentage of the film resistance. We define the normalized resistance as the resistance divided by 1000 of width. In Figure 2-31, the normalized film resistance and the normalized resistance at drain side as a function of gate voltage under drain bias $V_D$= -5V and -15V were taken with the different widths of 1000um, 500um, 100um and 50um. We can find that the normalized resistance between the probe1 and the probe2 and at drain side reduced with the decreasing width. It also depicts that the resistances are sensitive to the width. There must be some additional effect to affect the film resistance which reduced as the width decreased. Therefore, we review our process and check our device as shown in Figure 2-32. The border effect for device, which result from active region fabricated by shadow mask should be considered. It attributed to the additional drain current. If we assume that the ideal drain current ($I_o$) and the additional drain current (I') from the edge of active region, the total drain current as shown below:

$$I_{tot} = W \times J_o + I' \tag{2-10}$$

Then we estimate the mobility in linear regime by Equation ( 2-2 ), it yields

$$\mu_w = \frac{L}{C_{ox}}\left(\frac{\partial J_o}{\partial V_G} + \frac{1}{W}\frac{\partial I'}{\partial V_G}\right) \cdots for \cdot\cdot linear \cdot\cdot region \tag{2-11}$$

The relationship between mobility and channel width corresponds well to the phenomenon as shown in Figure 2-30. We can also estimate the normalized film resistance as follows:

$$N.R_{film} = \frac{R_{film}}{W} = \frac{\Delta V_{film}}{I_{tot} \times W} = \frac{\Delta V_{film}}{J_o + I'/W} \tag{2-12}$$

The relationship between normalized film resistance and channel width corresponds well to the phenomenon as shown in Figure 2-31, too. We can find that the narrower width is significantly affected by the border effect. The additional current at the edge of

active area would be an important portion of drain current as the decreasing width. Hence, the extracted mobility increases for devices with the narrower channel width. The normalized resistance also reduced due to addition drain current. It is believed that the rising mobility is affected by the additional current due to additional edge through patterning active region. Mobility should be modified by additional width when it is extracted. In Figure 2-33, we can find that the modified mobility is not more dependent on width and between 0.1 and 0.2 $cm^2/V$-s eventually.

## 2.4 Summary

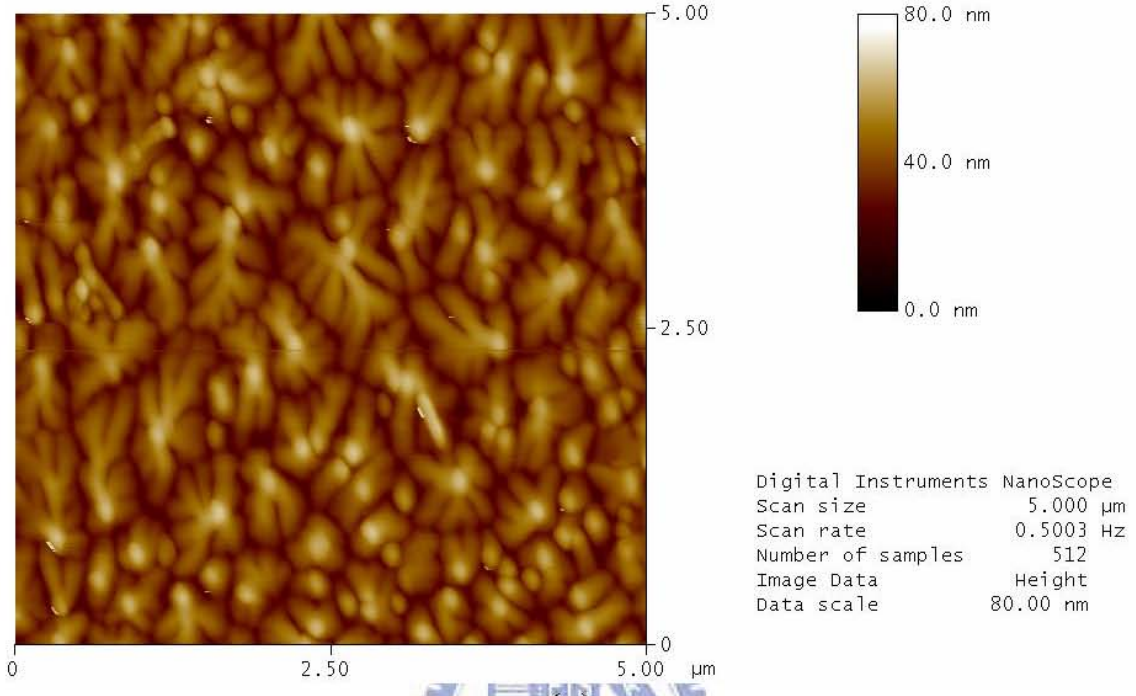
In this chapter, the pentacene crystallization as a continuous film is influenced by substrate temperature, morphology and the difference phase. Although many approaches were proposed to enhance pentacene grain growth, however larger poly grains do not mean better electrical properties. In material, a single phase of pentacene crystal is preferred for carrier transport due to the lack of interference between two kinds of orientation of pentacene molecules.

The four probe measurement are proposed to analyze the voltage drops and the resistances for device. The voltage drops were further discussed and the increasing carrier concentration with the rising gate voltage attributes to the reduced resistances.

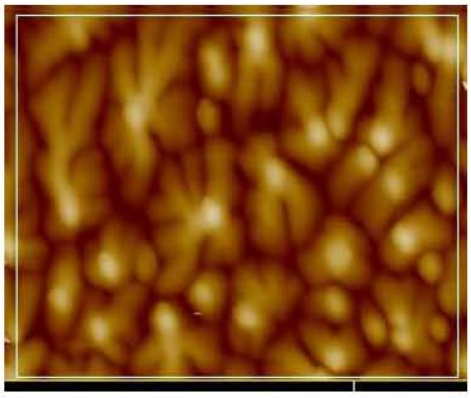
The higher substrate temperature not only improves the thin film growth, but also helps the connection of the contact between metal and semiconductor.

As expected, for OTFTs, the extracted mobility is smaller at the shorter channel length device. This is due to a large drain-source voltage drop at source/drain series resistance in comparison to the channel resistance for a shorter channel-length OTFT

(the channel resistance is smaller); this results in a lower extracted mobility. For a longer channel-length OTFT, e.g. L=1000um, the channel resistance is much larger than source/drain series resistances, and the extracted mobility approaches its intrinsic mobility value (1.17 cm /Vs). In addition, mobility is sensitive to the width. We can find that the performance of device with the narrower width is significantly affected by the border effect. The additional current at the edge of active area would be an important portion of drain current as the width decreases. Hence, the extracted mobility increases at the narrower channel width device. The normalized resistance also reduced due to addition drain current.




(a)



Box Statistics

| | |
|---|---|
| Z range | 44.837 nm |
| Mean | -0.090 nm |
| Raw mean | 1.635 µm |
| Rms (Rq) | 8.172 nm |
| Mean roughness (Ra) | 6.644 nm |

(b)

Figure 2-1:(a)A 5um×5um AFM topography of pentacene film at the substrate temperature of 25°C during the deposition, and (b) the mean roughness of the thin film is about 6.644nm

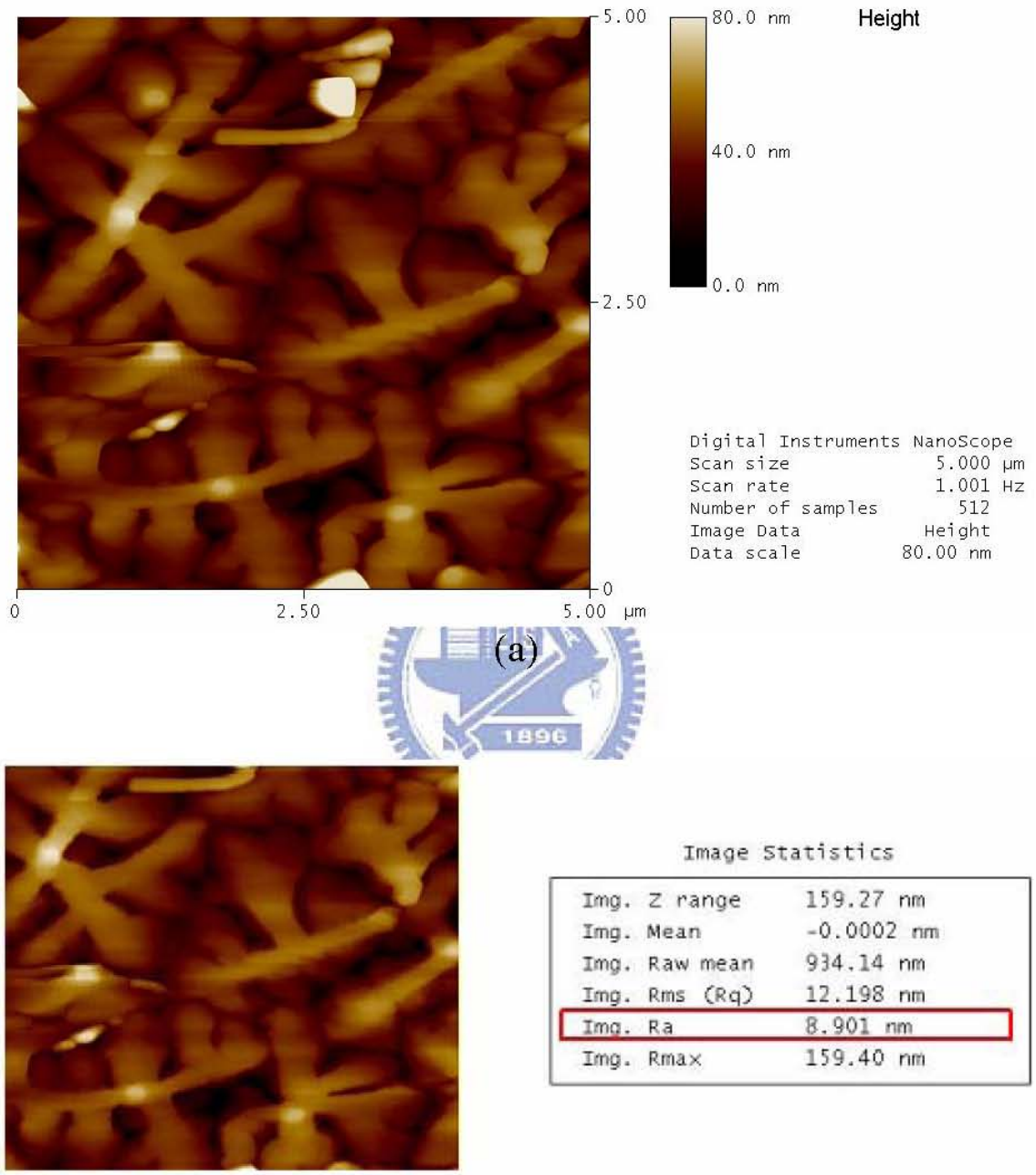
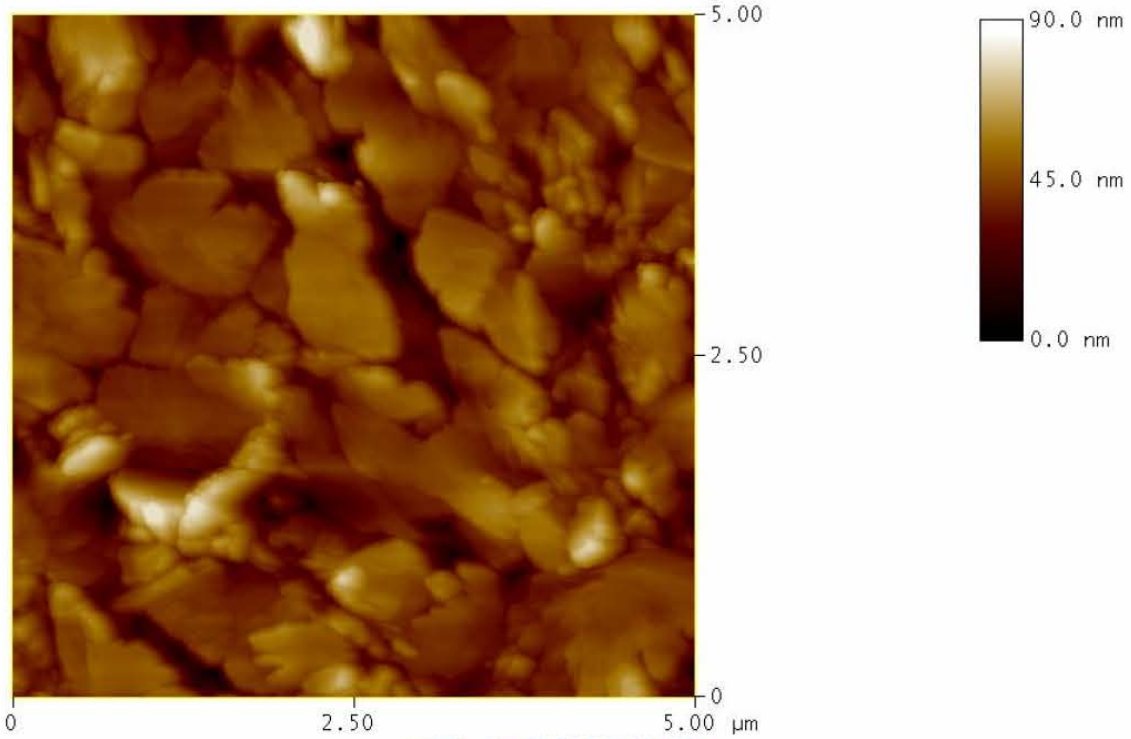



Figure 2-2:(a)A 5um×5um AFM topography of pentacene film at the substrate temperature of 70°C during the deposition, and (b) the mean roughness of the thin film is about 8.901nm




(a)

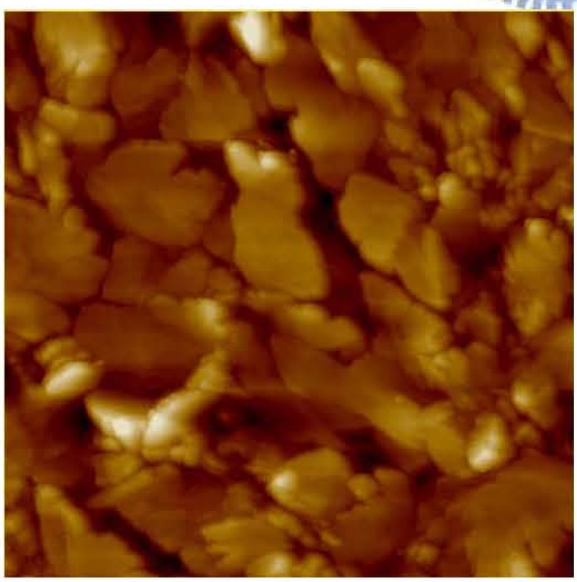
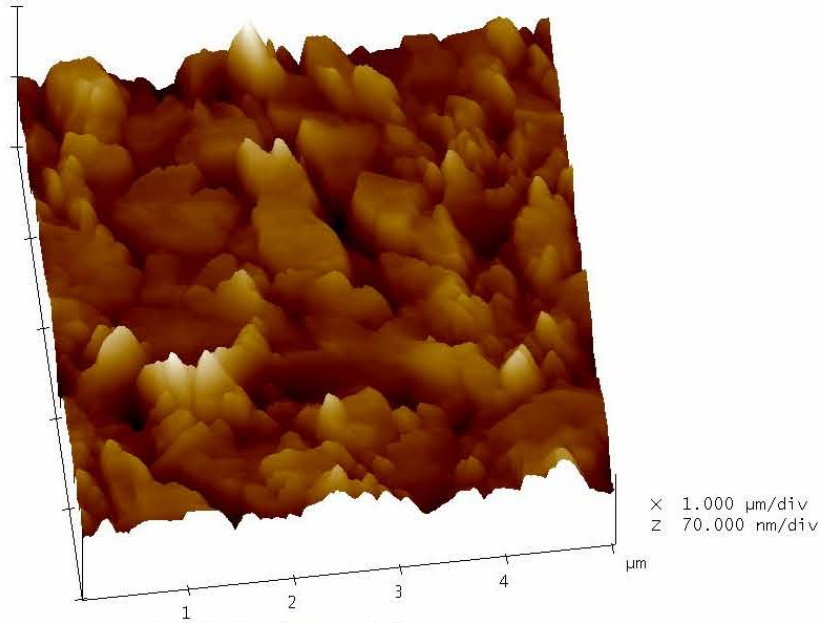


Image Statistics

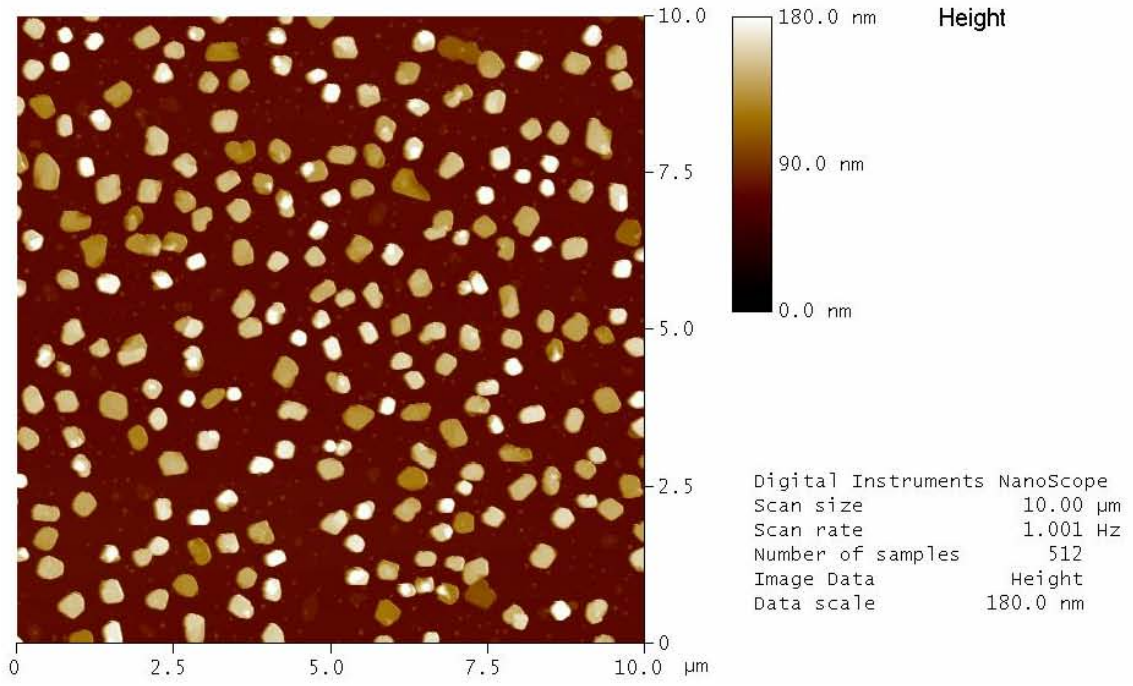
| | |
|---|---|
| Img. Z range | 82.720 nm |
| Img. Mean | 0.000001 nm |
| Img. Raw mean | -252.95 nm |
| Img. Rms (Rq) | 8.860 nm |
| Img. Ra | 6.655 nm |
| Img. Rmax | 82.720 nm |

(b)

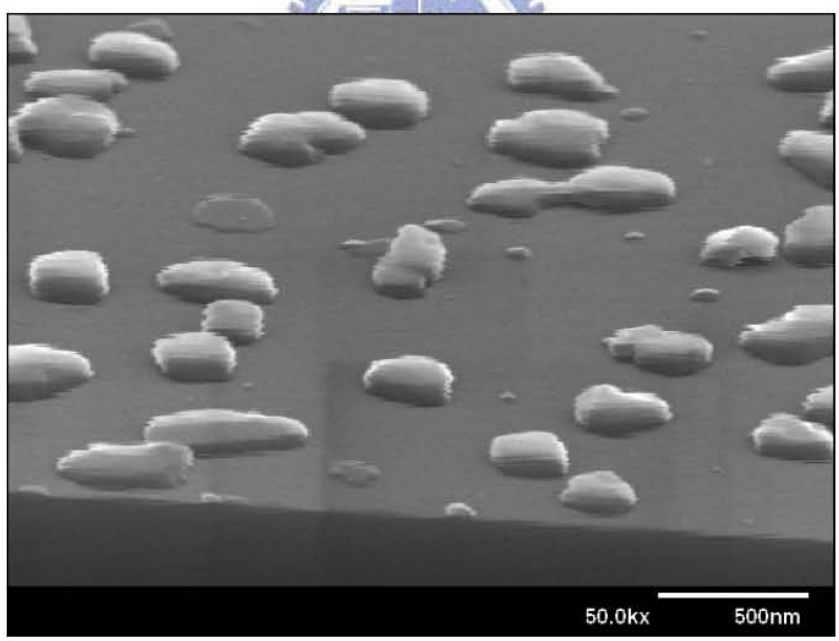



(c)

Figure 2-3:(a)A 5um×5um AFM topography of pentacene film at the substrate temperature of 120°C during the deposition, and (b) The mean roughness of the thin film is about 6.655nm. (c)The lateral view of three dimension AFM topography




(a)




(b)

Figure 2-4: (a)The 10um×10um AFM topography of pentacene film ,and (b)the lateral viewing SEM image of pentacene film in the initial period of crystallization. The morphology is like crystalline species.

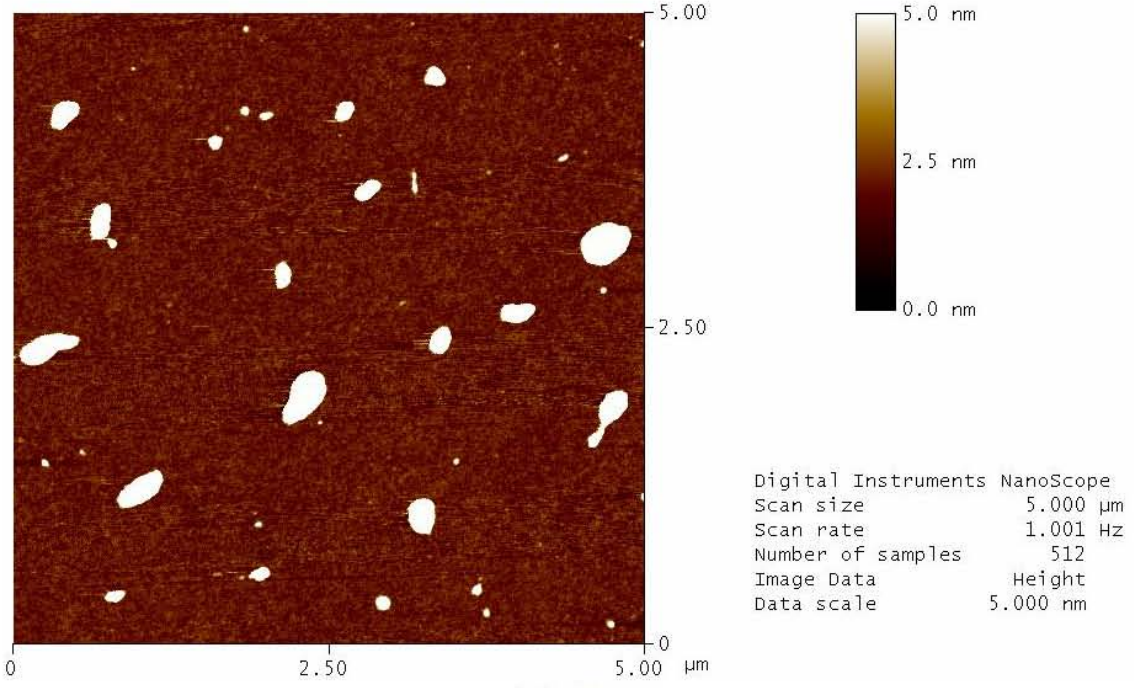
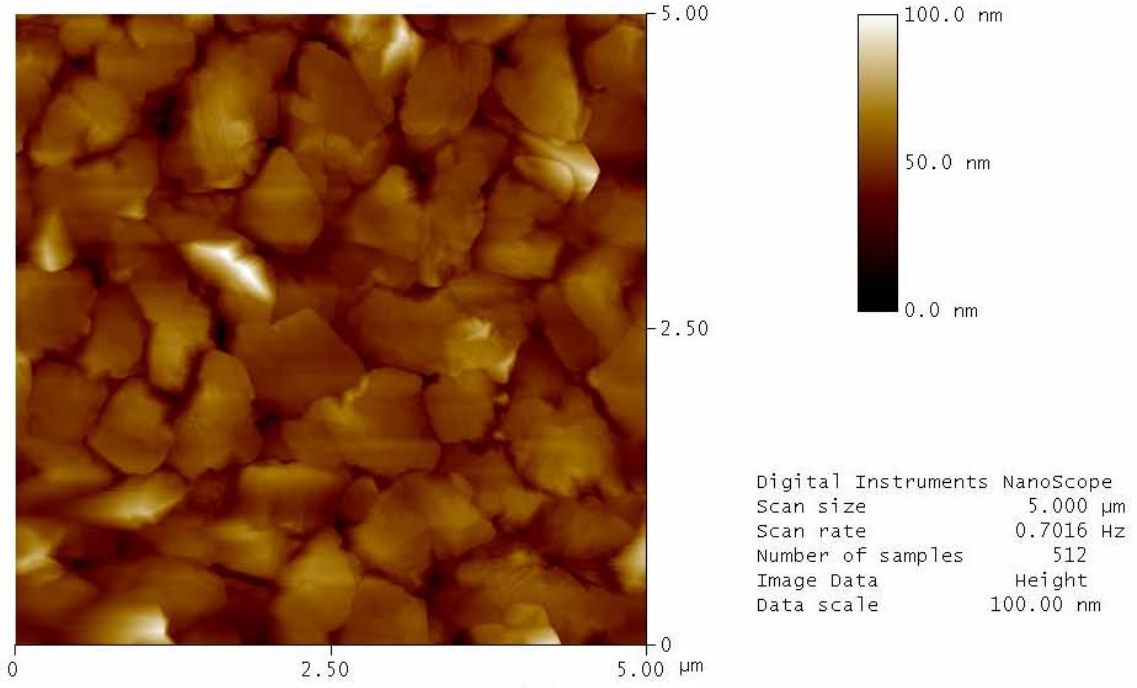
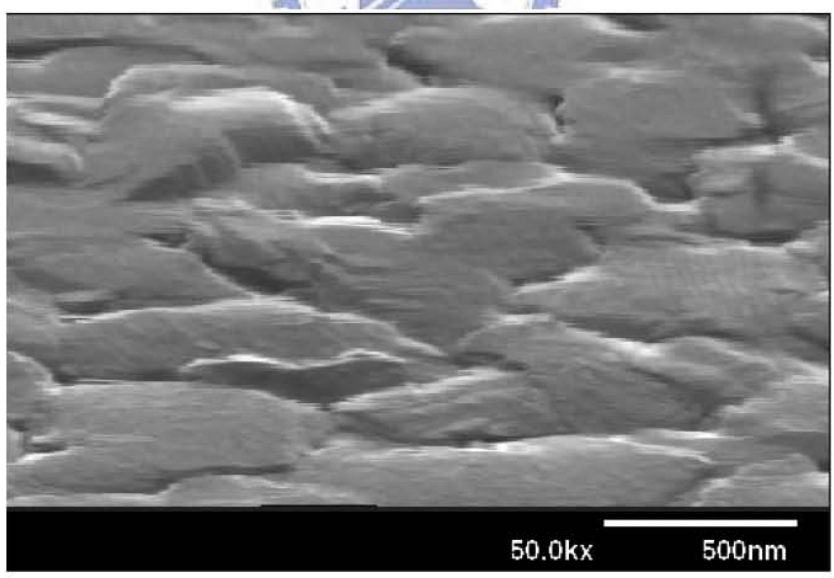



Figure 2-5: The AFM topography of pentacene film in the second period of crystallization is the diffusion limit aggregation step, where molecules diffuse on a surface and stick to any existing island, without further diffusion.




(a)




(b)

Figure 2-6: (a)The AFM topography of pentacene film, and (b)the lateral view SEM image of pentacene film in the third period of crystallization is the coarsening step, the pentacene islands coarsen until the grains touch each other.

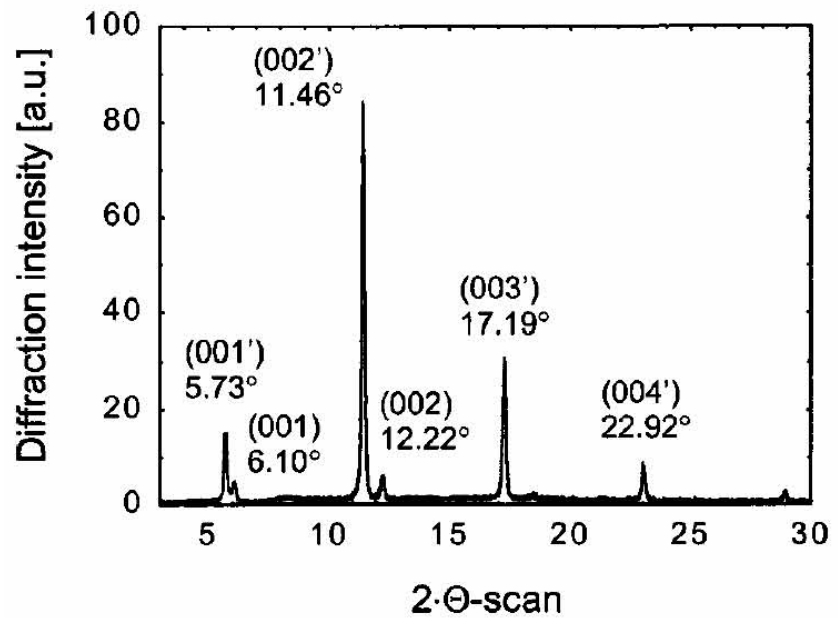



Figure 2-7: X-ray diffraction pattern of thermally deposited pentacene film on thermal oxide film. (D. Knipp et al., J. Appl. Phys. 2003)

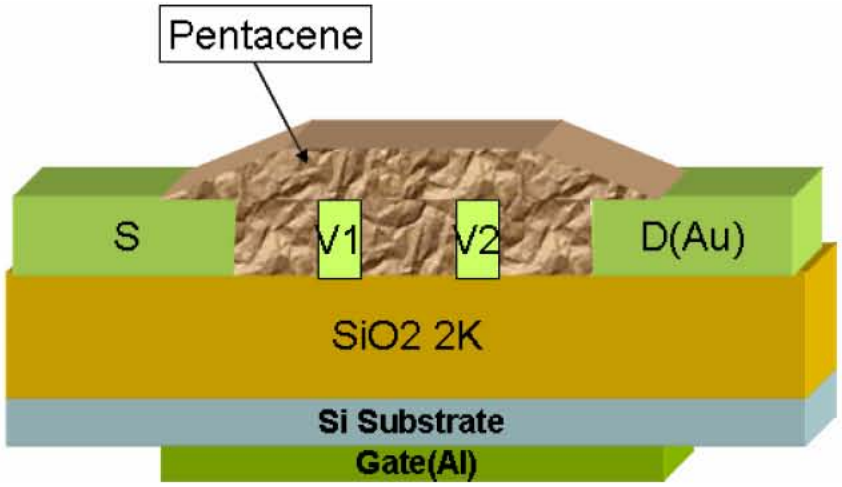



Figure 2-8: The schematic diagram of the bottom-contact OTFT with four probe structure. The voltage sensing probes are evaporated simultaneously with the source and drain electrodes in the staggered structure.

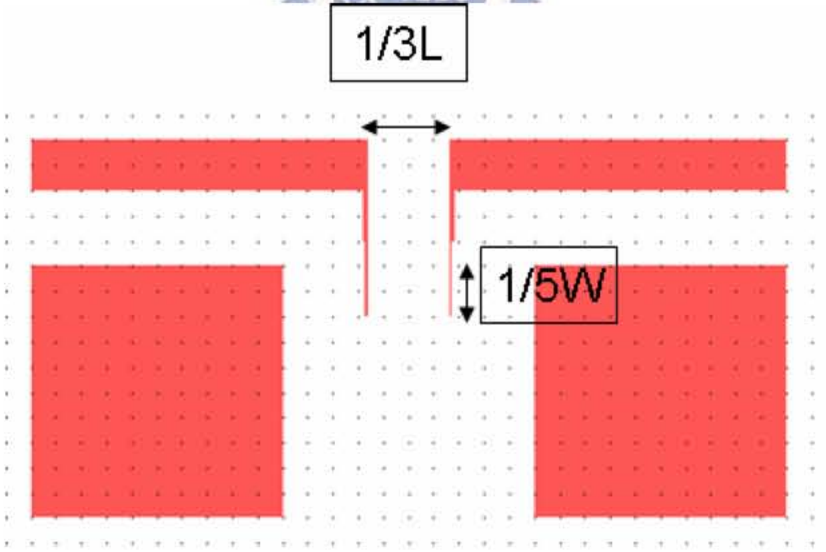



Figure 2-9: Top-view schematic of the four-probe OTFT geometry. Pentacene films are patterned to minimize overlap between the sense probe leads outside the channel area.

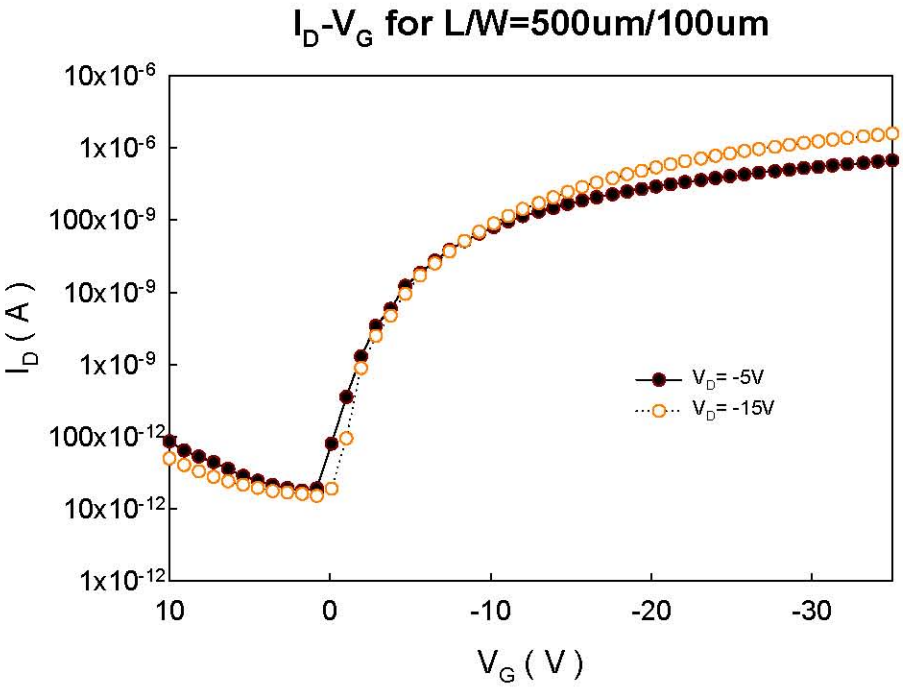



Figure 2-10: The transfer characteristics $I_D$-$V_G$ of OTFT at the drain voltages of -5V and -15V with length/width = 500um/1000um

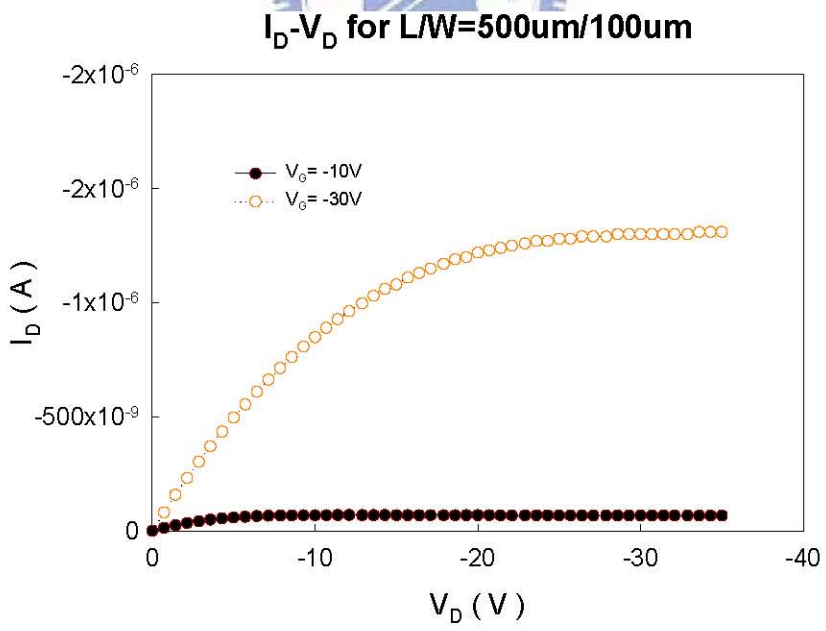



Figure 2-11: The output characteristics for pentacene-based OTFT with four probe structure at the gate voltage of -10V and -30V.

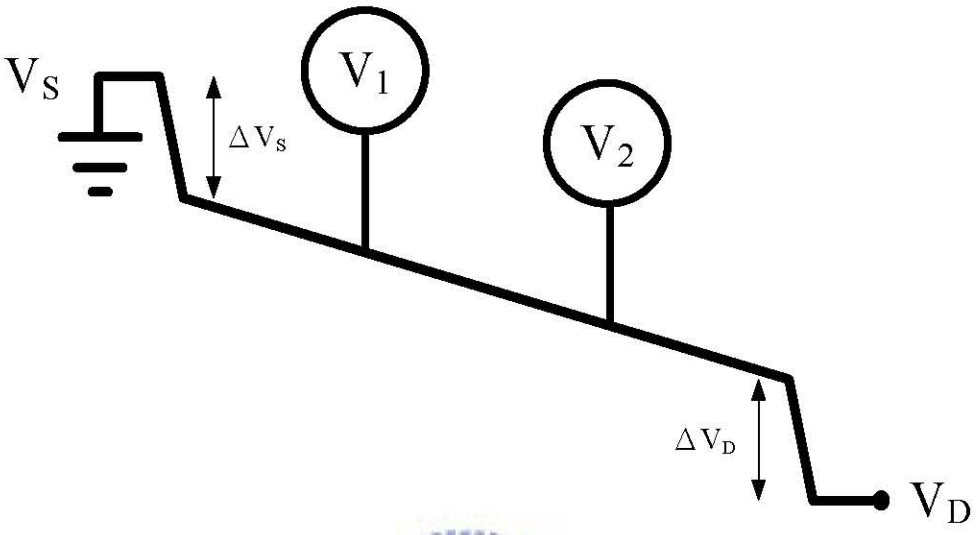
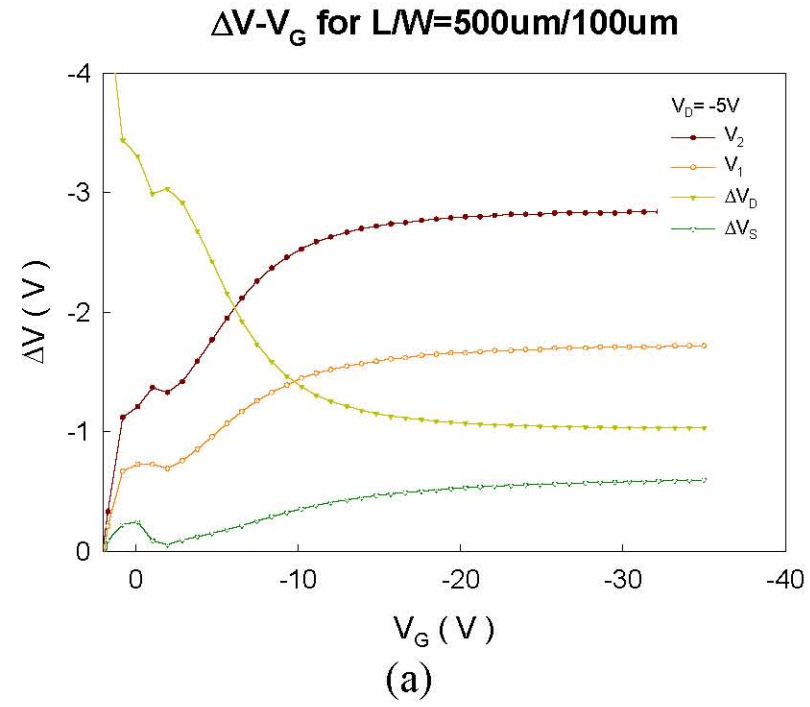
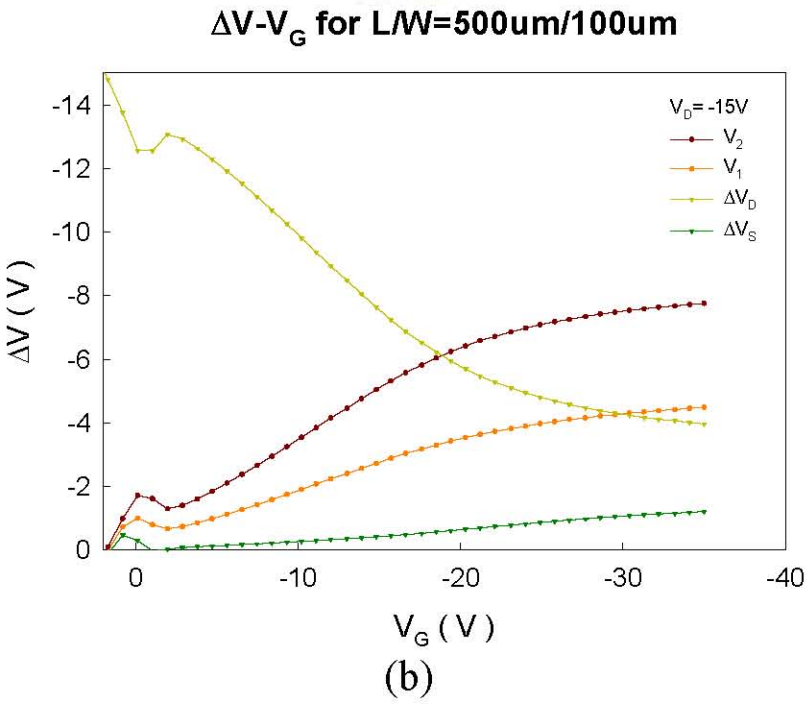



Figure 2-12: Model of voltage drop in the channel as determined by voltage probes $V_1$ and $V_2$. $\Delta V_S$ and $\Delta V_D$ are voltage drops at the source and drain, extrapolated from the channel gradient.

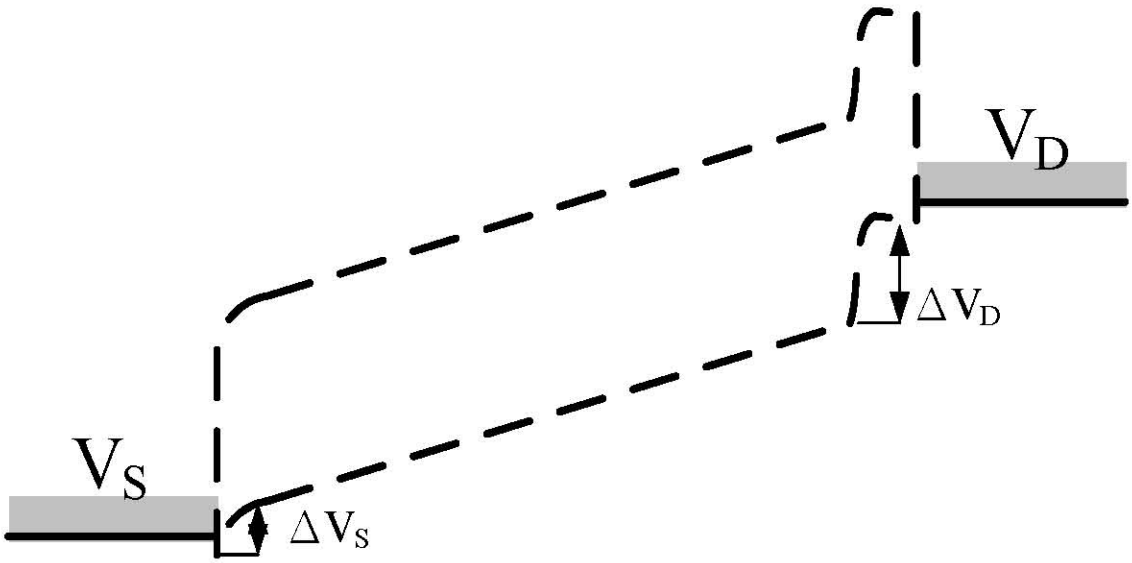



(a)

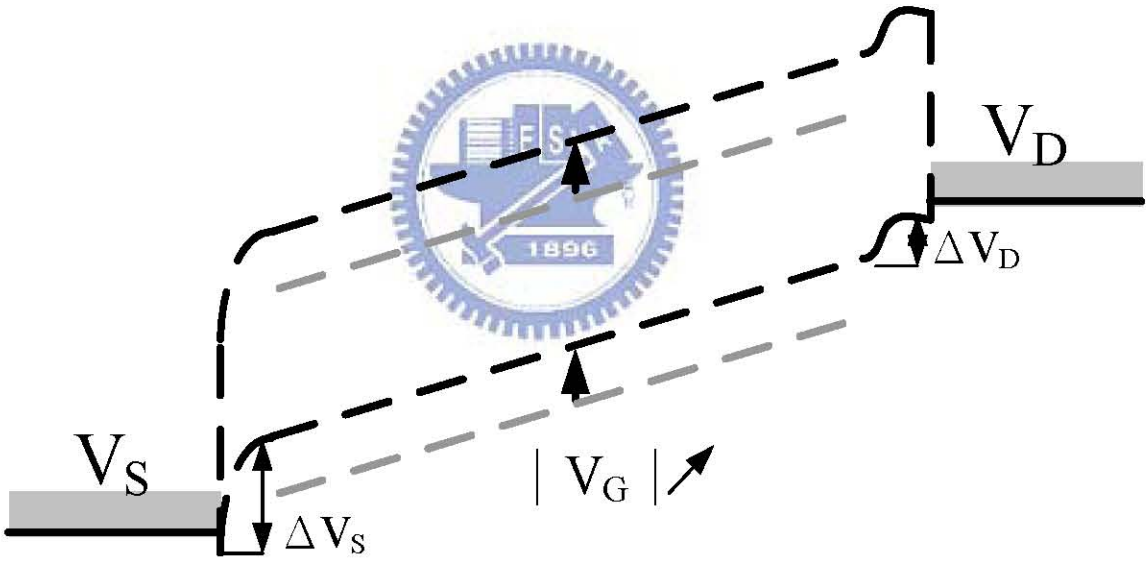



(b)

Figure 2-13: Plot of sense probe ($V_1$ ,$V_2$) and source/drain voltage drops($\Delta V_S$ , $\Delta V_D$) as a function of gate voltage. The data correspond to the device in Figure 2-10 operating at room temperature with (a)$V_D$= -5 V, (b)$V_D$= -15 V.

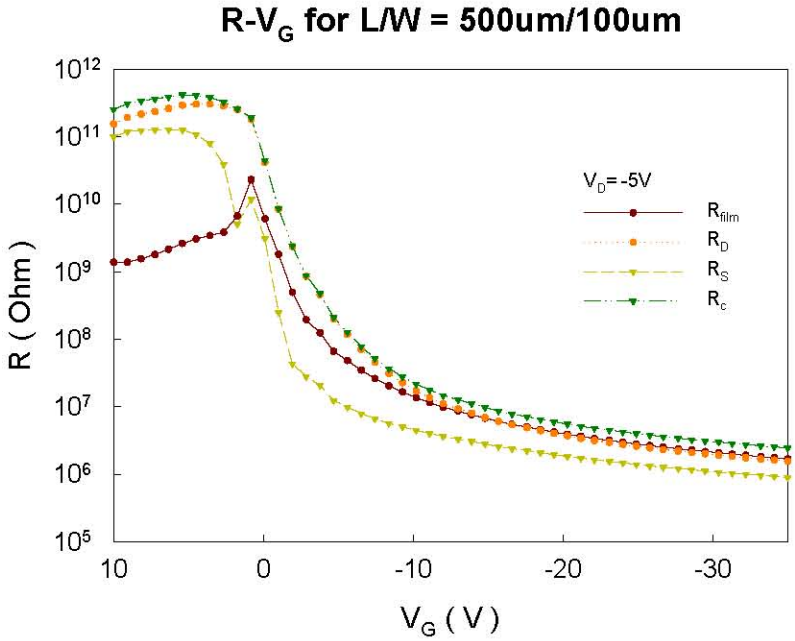



(a)

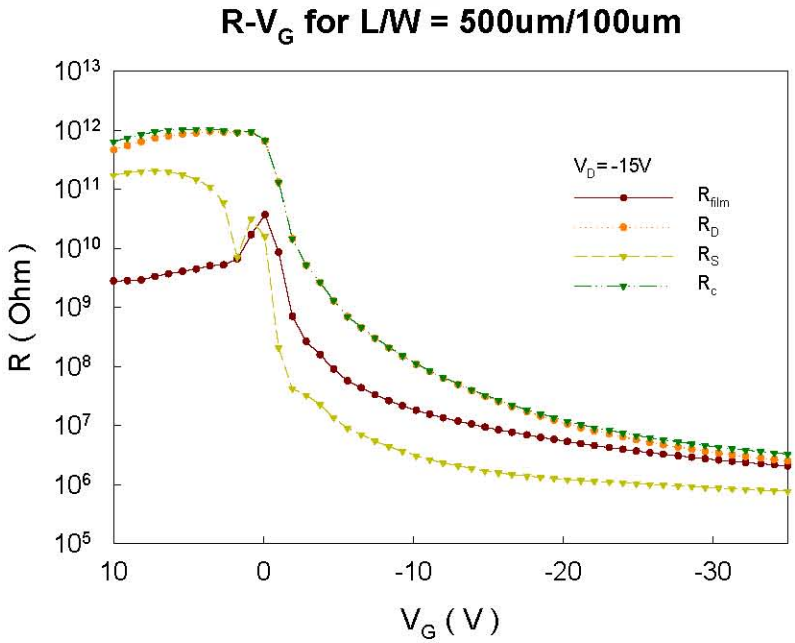



(b)

Figure 2-14: The diagram of energy band along the channel. (a)At the smaller gate voltage, band bending leads to the more depletion region at drain side and the less voltage drop at source side. (b)At the large gate voltage, band bending leads to the less depletion region at drain side and the more voltage drop at source side.




(a)




(b)

Figure 2-15: Plots of film resistance, source resistance, drain resistance and total contact resistance as a function of gate voltage for an operating OTFTs. The data correspond to the device in Figure 2-10 operating at room temperature with (a)$V_D$= -5V and (b)$V_D$= -15V.

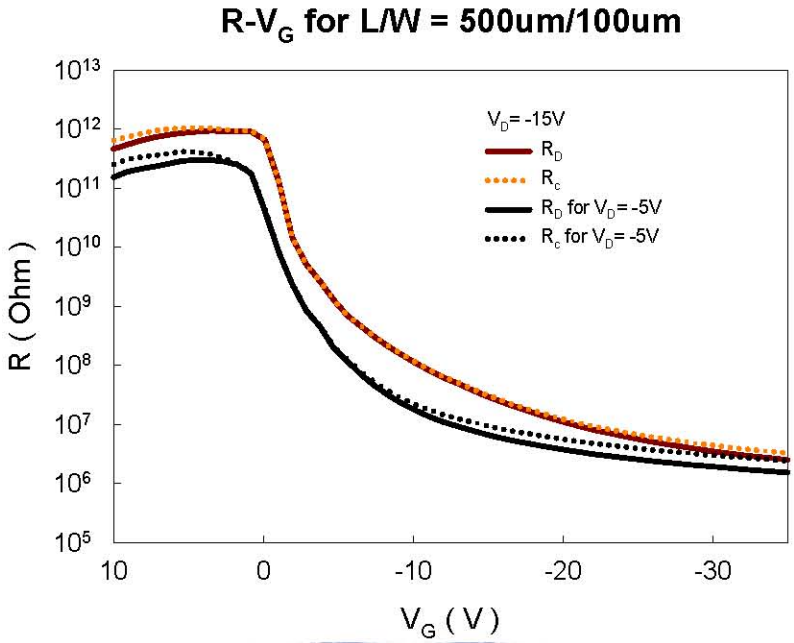
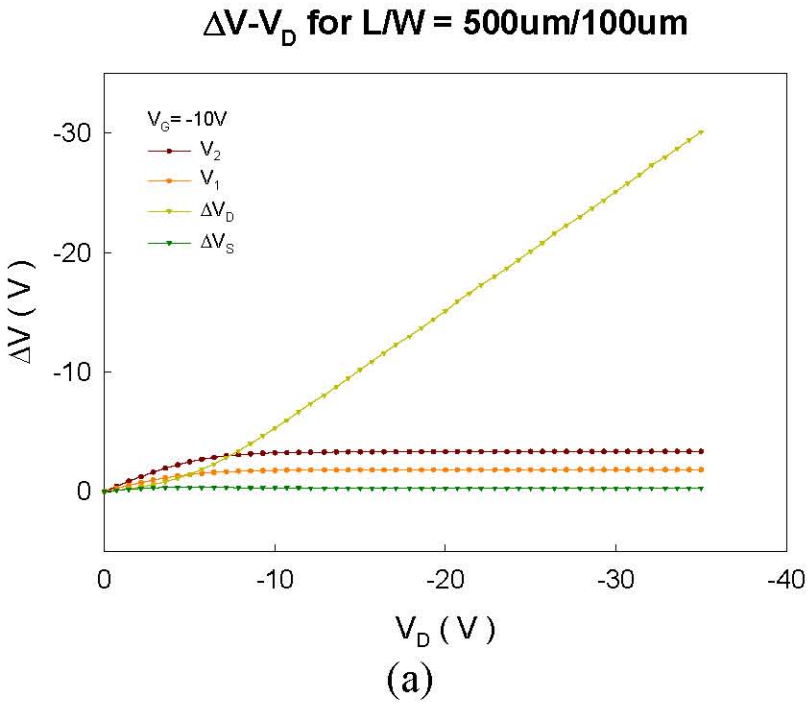
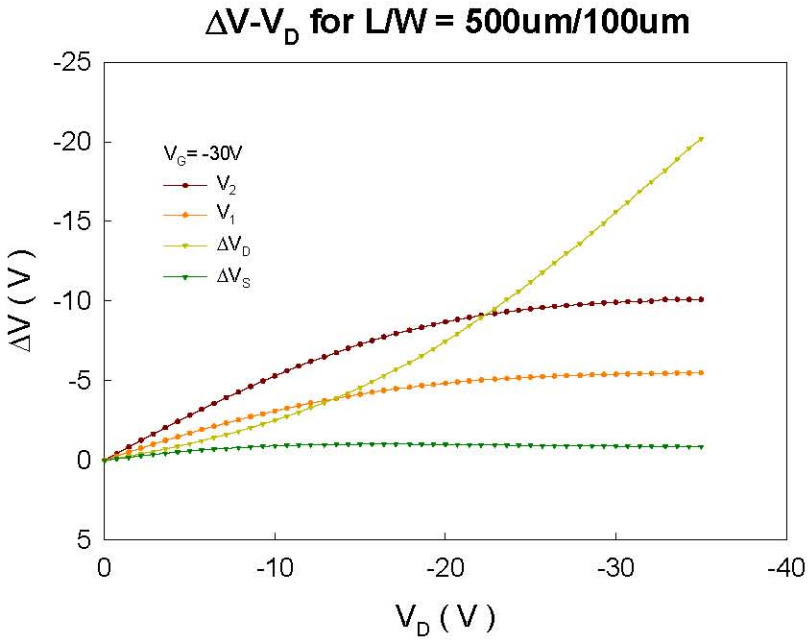



Figure 2-16: Comparison of the contact resistance and the resistance at drain side with the applied different drain voltage drops ($V_D$= -5 and -15V).

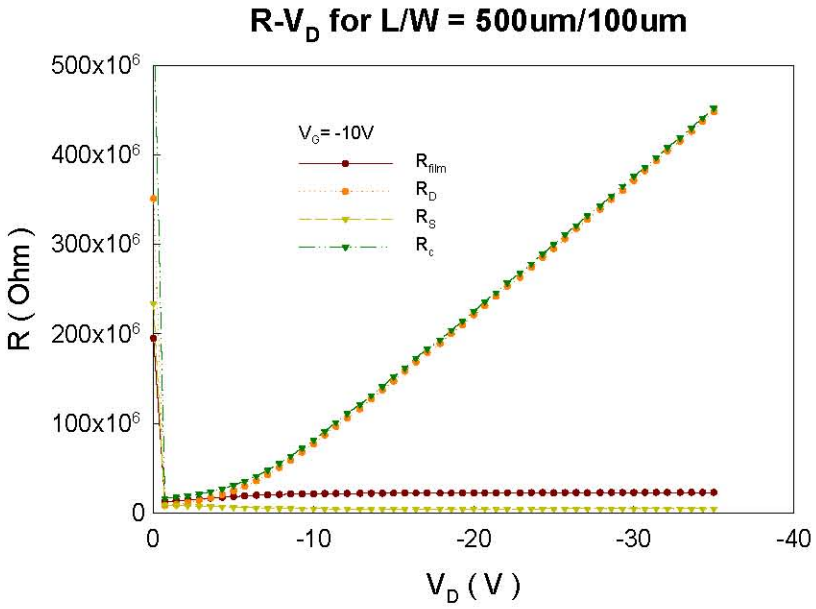



(a)

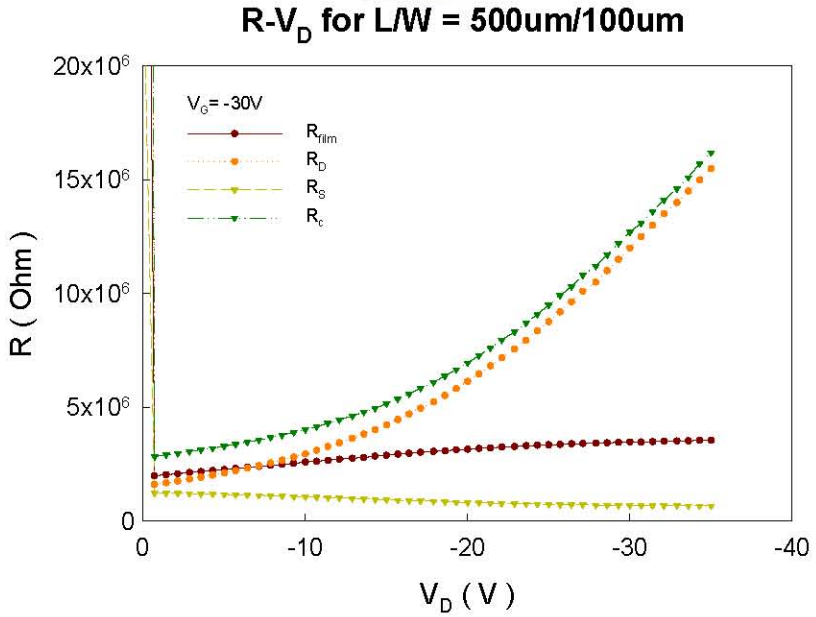



(b)

Figure 2-17: Plot of sense probe ($V_1$ ,$V_2$) and source/drain voltage drops($\Delta V_S$ , $\Delta V_D$) as a function of drain voltage. The data correspond to the device in Figure 2-11 operating at room temperature with (a)$V_G$= -10V and (b)$V_D$= -30V.




(a)




(b)

Figure 2-18: Plot of film resistance, source resistance, drain resistance and total contact resistance as a function of drain voltage for an operating OTFTs. The data correspond to the device in Figure 2-11 operating at room temperature with (a)$V_G$= -10V and (b)$V_G$= -30V.

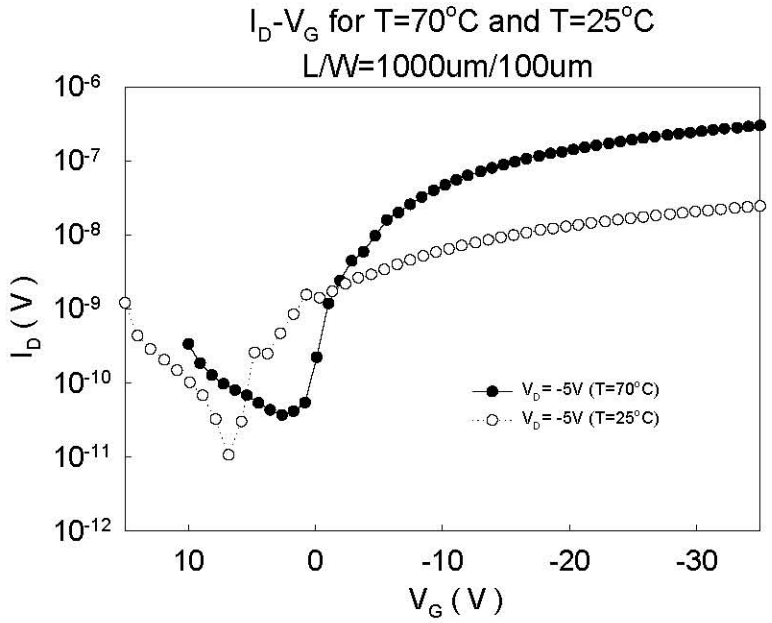



Figure 2-19: Comparison of the transfer characteristics $I_D$-$V_G$ with the different deposition temperature of 25°C and 70°C at the drain voltages of -5V

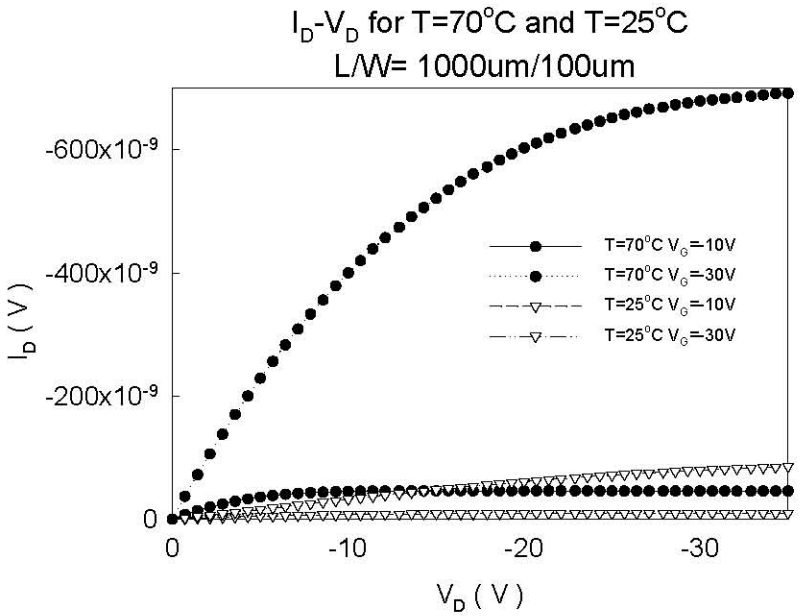
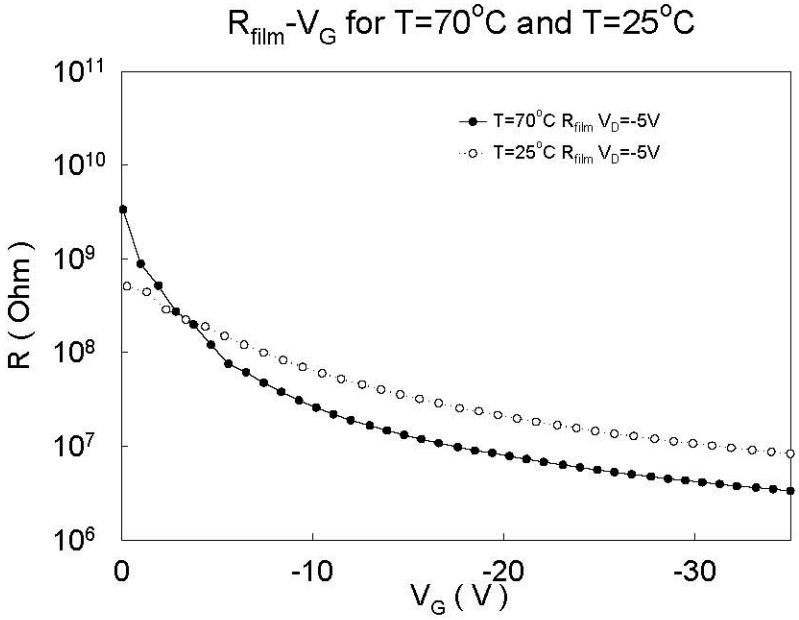
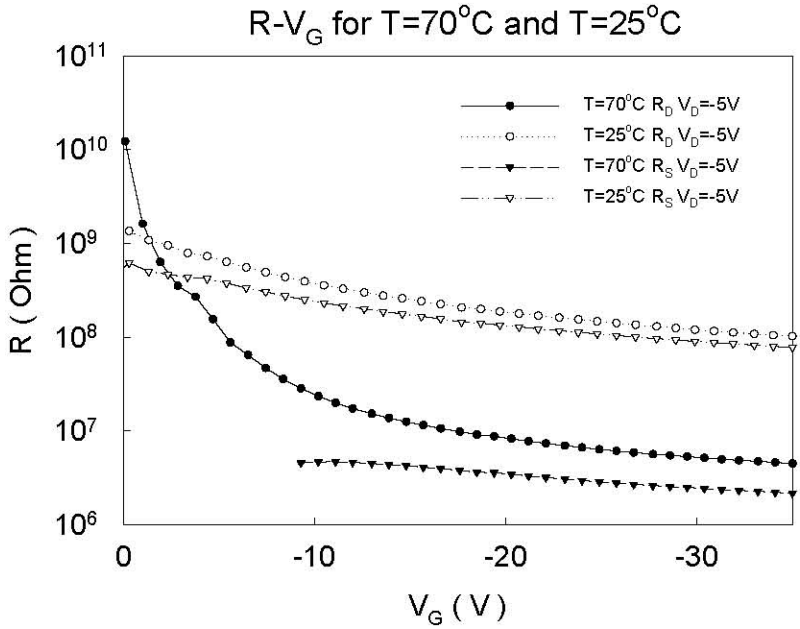



Figure2-20: Comparison of the output characteristics $I_D$-$V_D$ with the different deposition temperature of 25°C and 70°C at the gate voltages of -10V and -30V,separately.

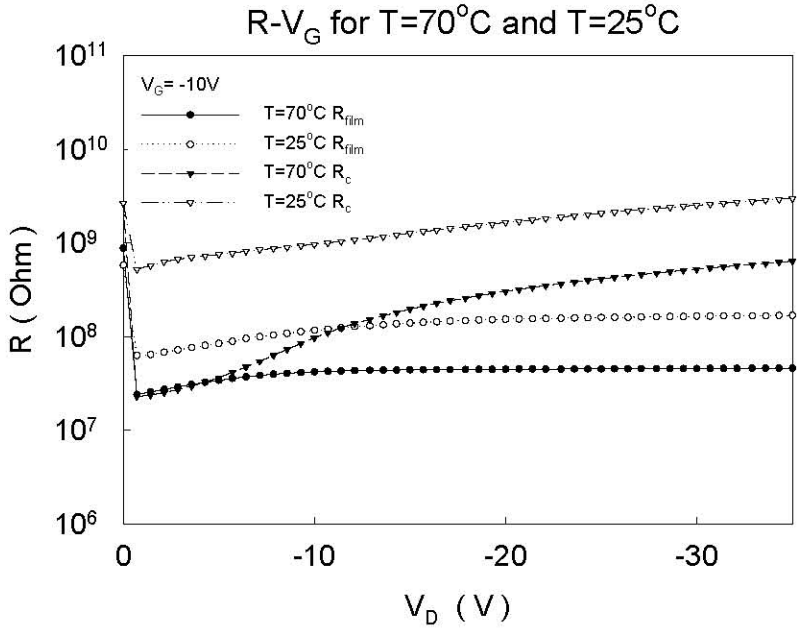



(a)

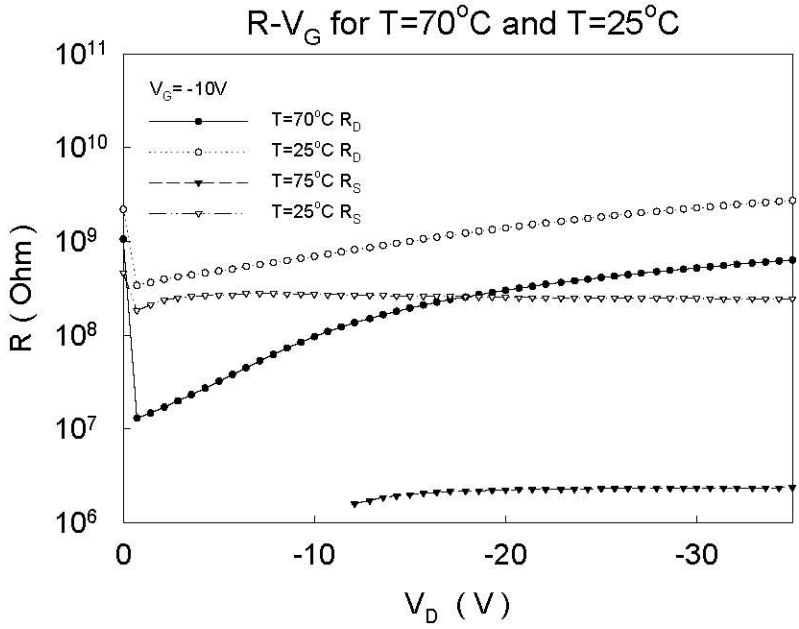



(b)

Figure 2-21: Comparison of (a)film resistance, (b)source resistance and drain resistance as a function of gate voltage with different deposition temperature of 25°C and 70°C for an operating OTFT. The data correspond to the device in Figure 2-20(a) operating at room temperature

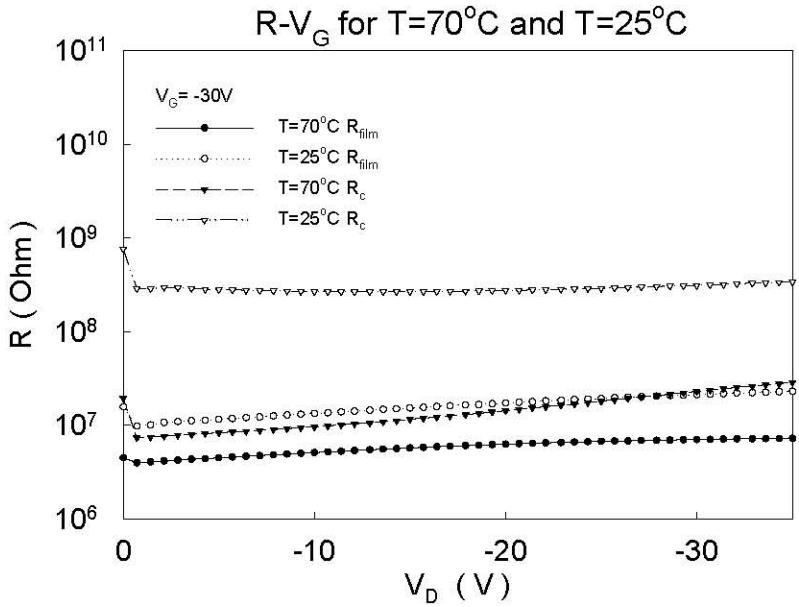



(a)

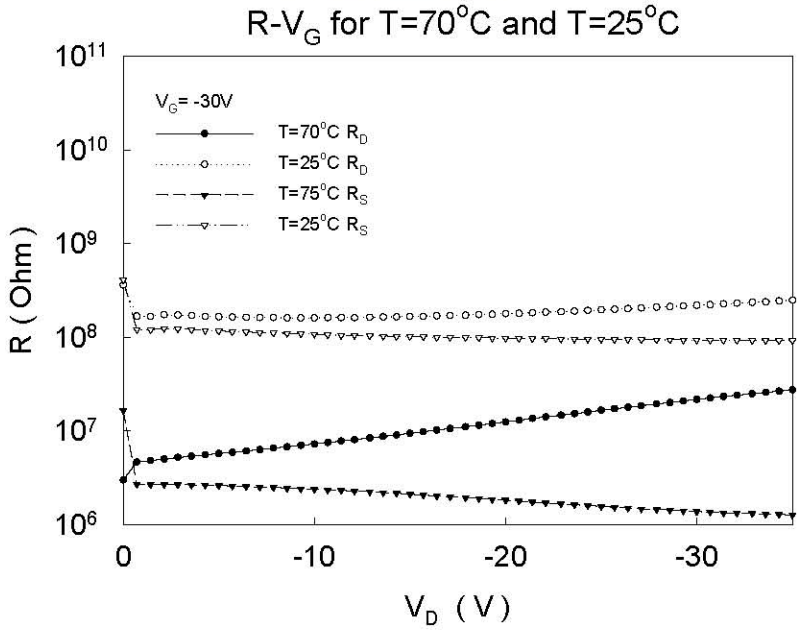



(b)

Figure 2-22: Comparison of (a)film resistance, (b)source resistance and drain resistance as a function of drain voltage at $V_D$= -10V with different deposition temperature of 25°C and 70°C for an operating OTFT . The data correspond to the device in Figure 2-20(b) operating at room temperature

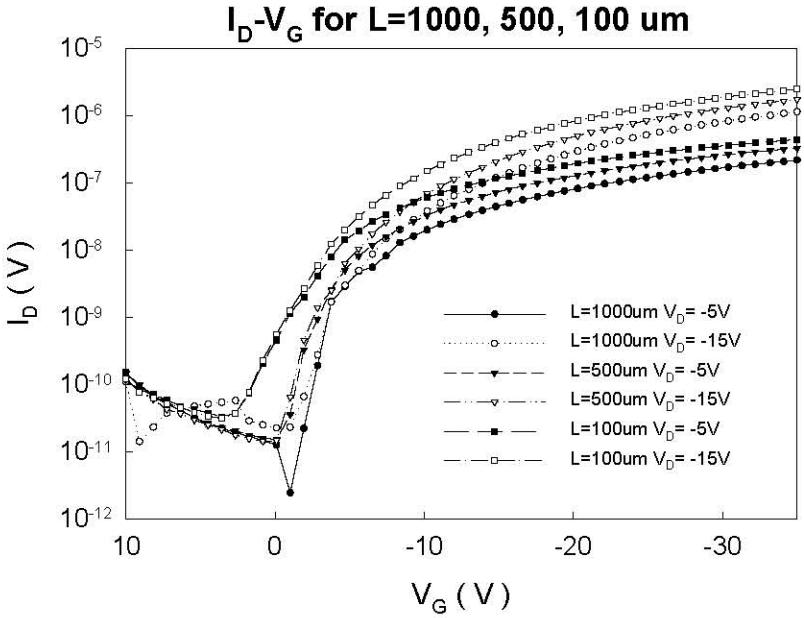



(a)

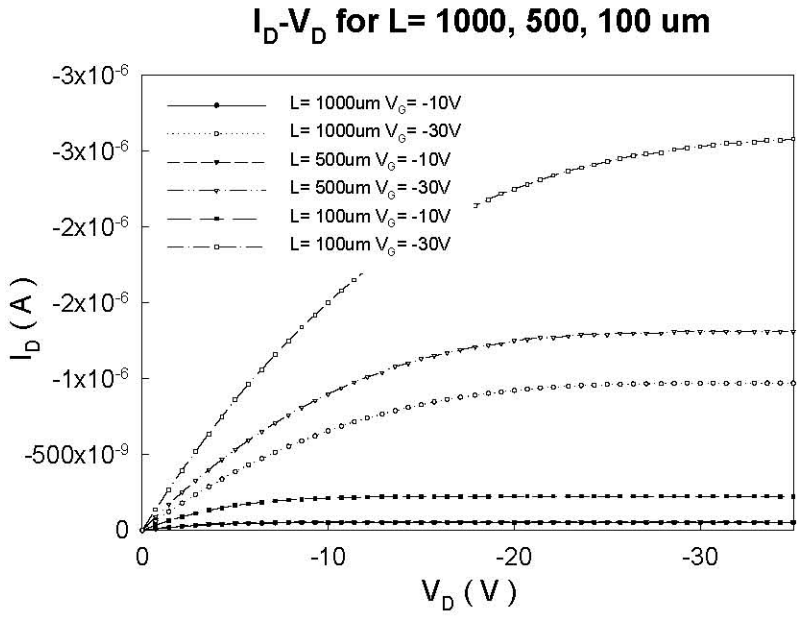



(b)

Figure 2-23: Comparison of (a)film resistance, (b)source resistance and drain resistance as a function of drain voltage at $V_D$= -30V with different deposition temperature of 25°C and 70°C for an operating OTFT. The data correspond to the device in Figure 2-20(b) operating at room temperature




(a)




(b)

Figure 2-24: (a)The transfer characteristics of the device at drain voltages $V_D$= -5V and $V_D$= -15V, and (b)the output characteristics at gate voltage $V_G$= -10 and $V_G$= -30V, compared with the length of 1000um, 500um and 100um.

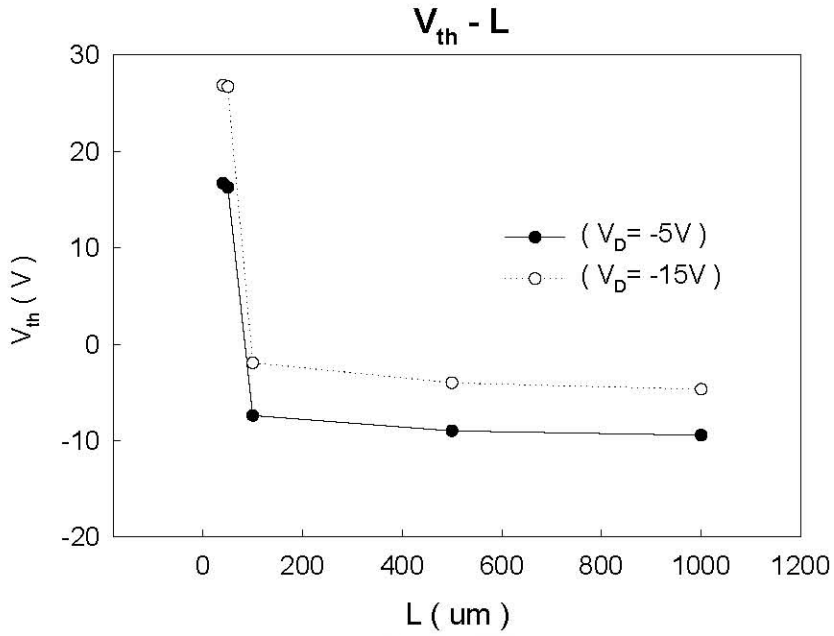



Figure 2-25: The threshold voltage versus length under drain bias ($V_D$= -5V and -15V), in linear and saturation region respectively.

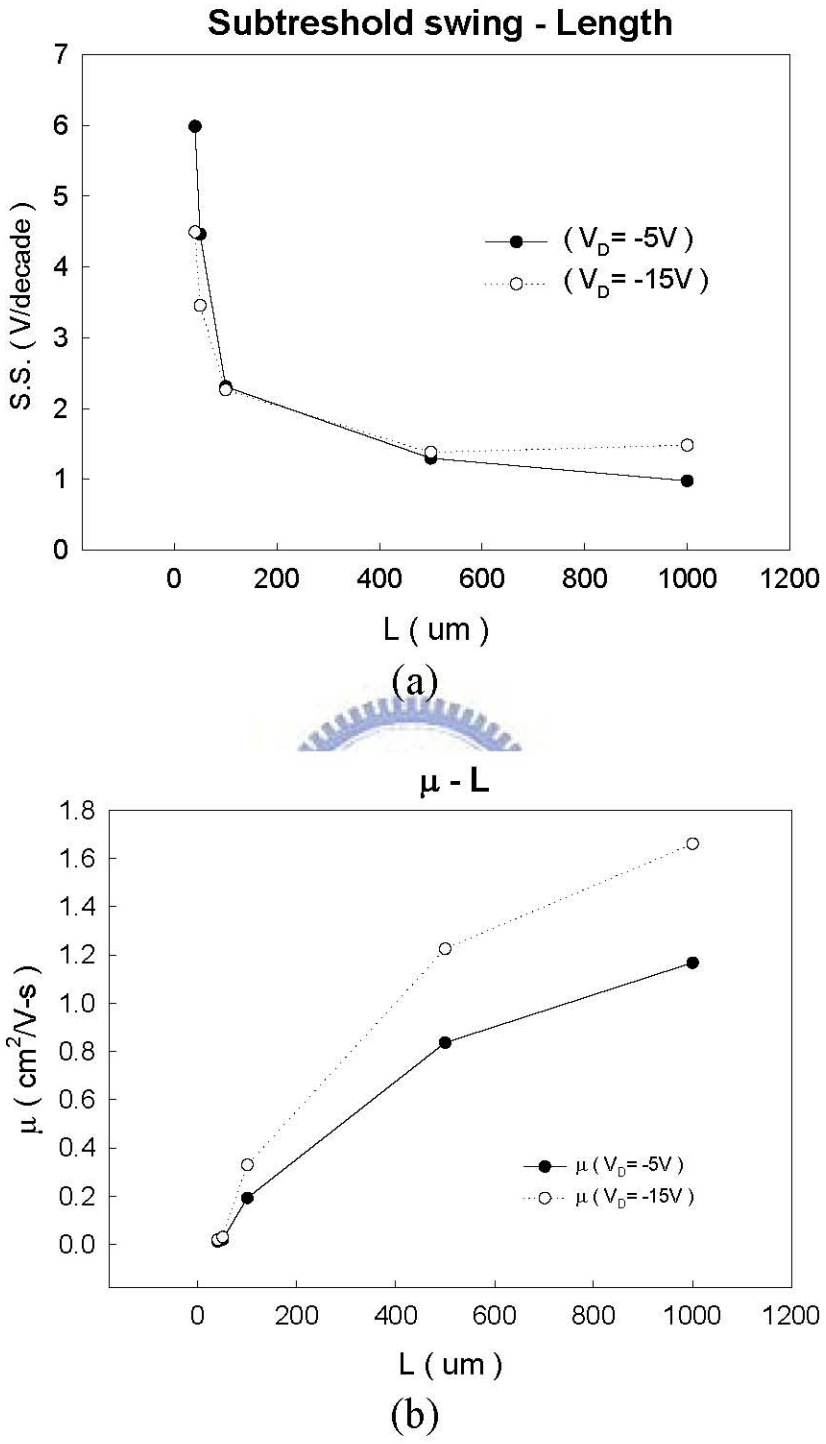
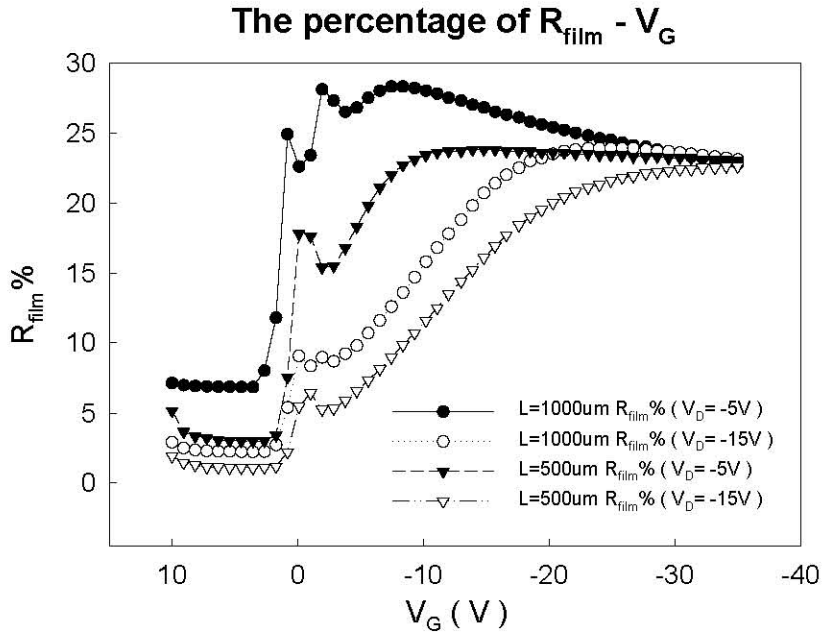
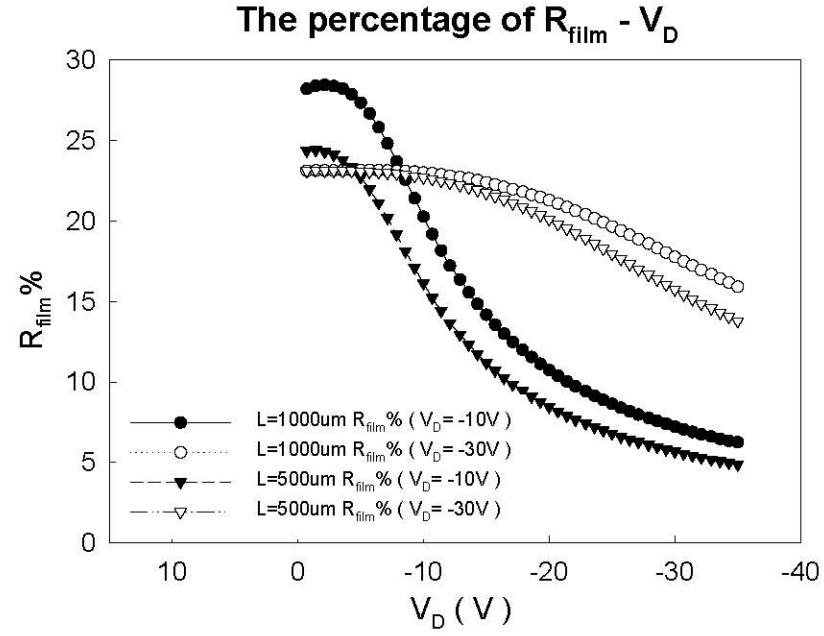



Figure 2-26: (a)The subthreshold swing versus length under the drain voltage of -5V and -15V, and (b)the linear and saturation mobility versus length under drain bias ($V_D$= -5V and -15V).

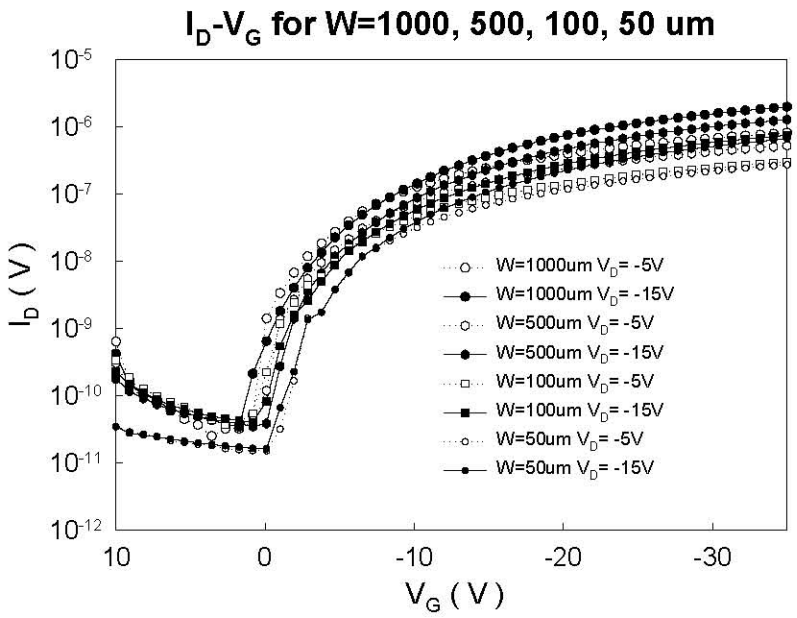



(a)

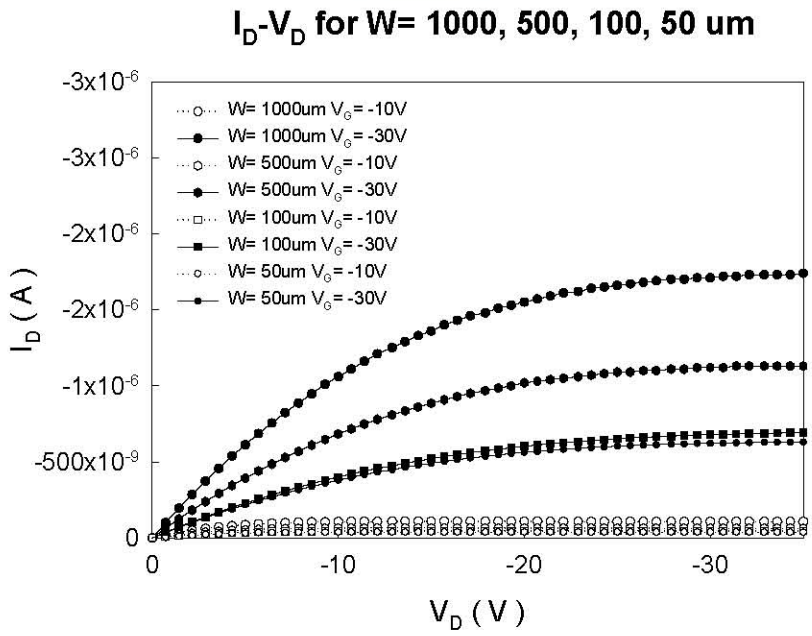



(b)

Figure 2-27: (a)The percentage of the film resistances as a function of gate voltage under drain bias ($V_D$= -5V and -15V). (b)The percentage of the film resistances as a function of drain voltage under gate bias ($V_G$= -10V and -30V). Two different kinds of devices with length (1000 um and 500 um) would be compared with.

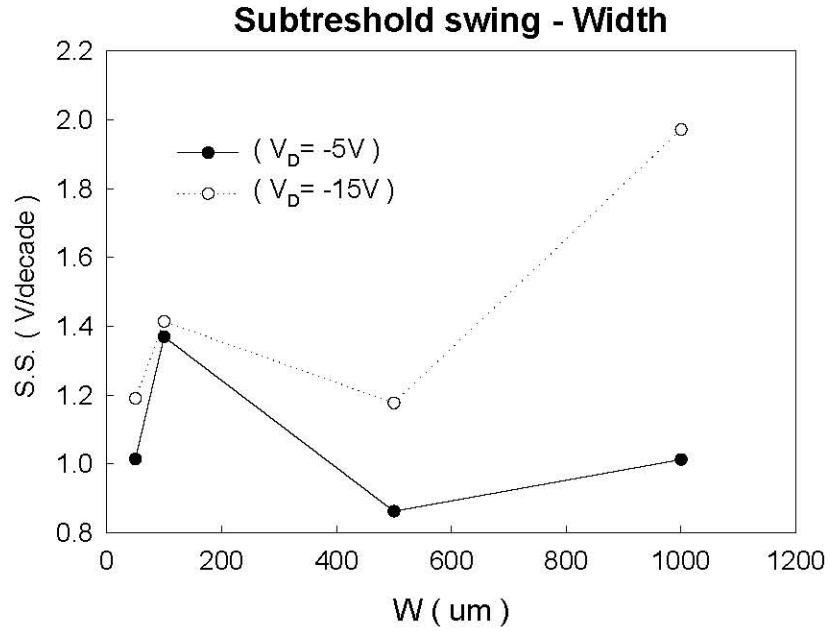



(a)

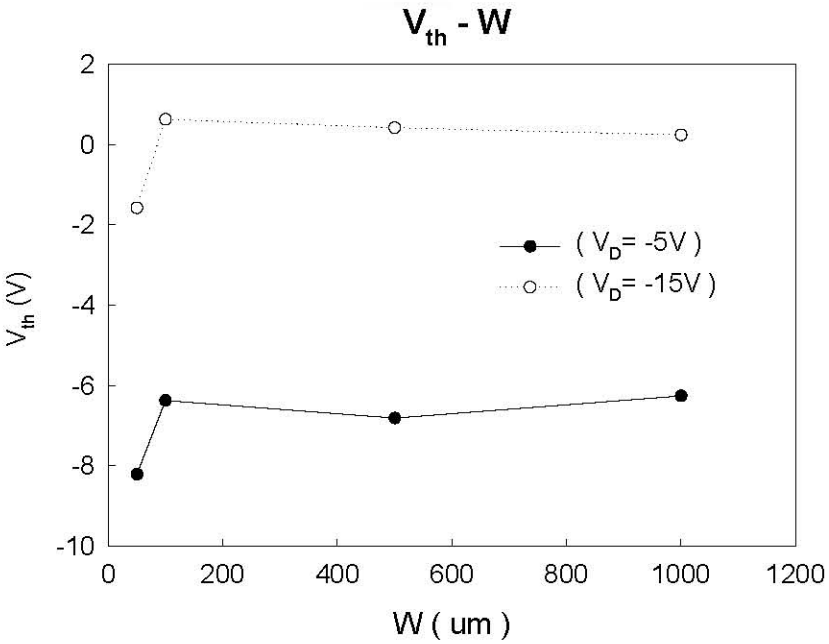



(b)

Figure 2-28: (a)The transfer characteristics of the device at drain voltages $V_D$= -5V and $V_D$= -15V, and (b)the output characteristics at gate voltage $V_G$= -10 and $V_G$= -30V, compared with the width of 1000um, 500um ,100um and 50um.




(a)




(b)

Figure 2-29: (a)The subthreshold swing versus width under the drain voltage of -5V and -15V, and (b)the threshold voltage versus width under drain bias ($V_D$= -5V and -15V), in linear and saturation region respectively.

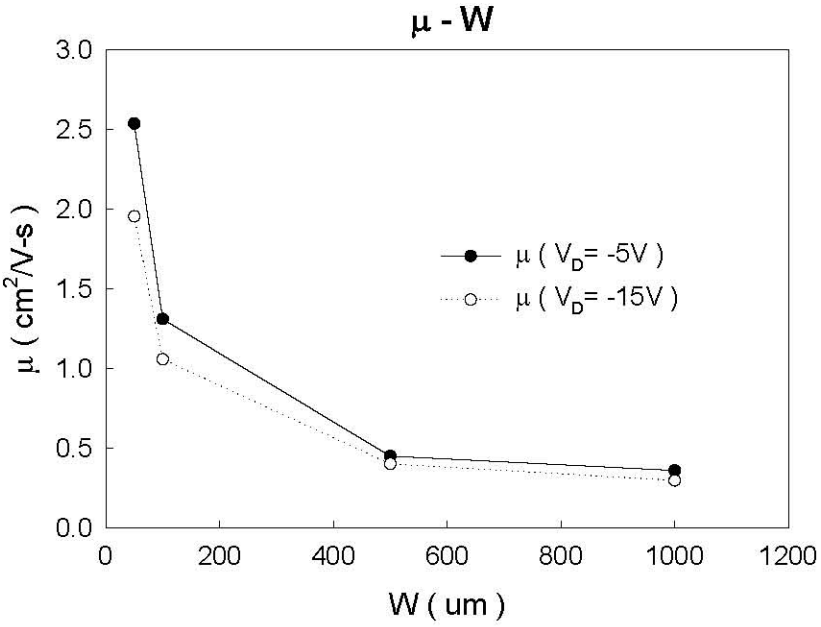
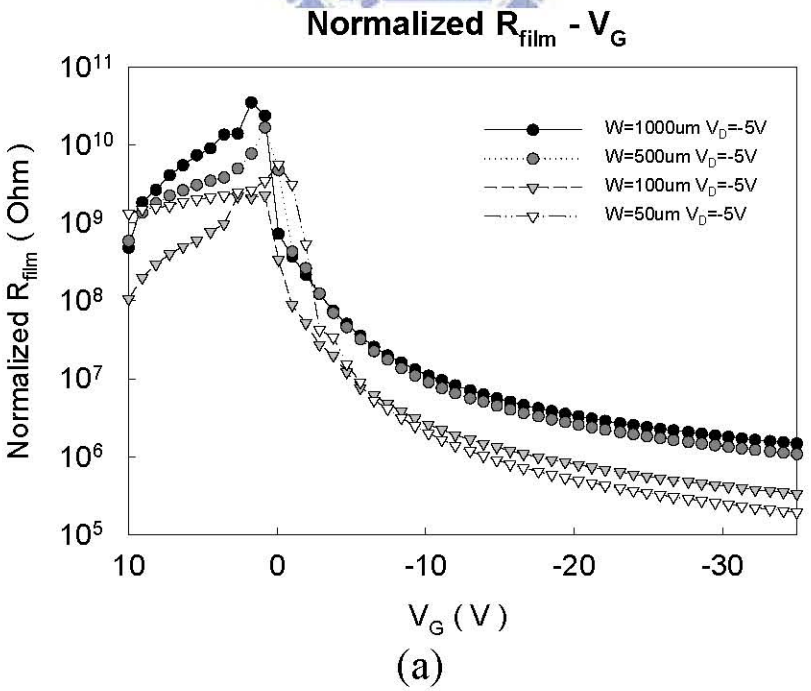
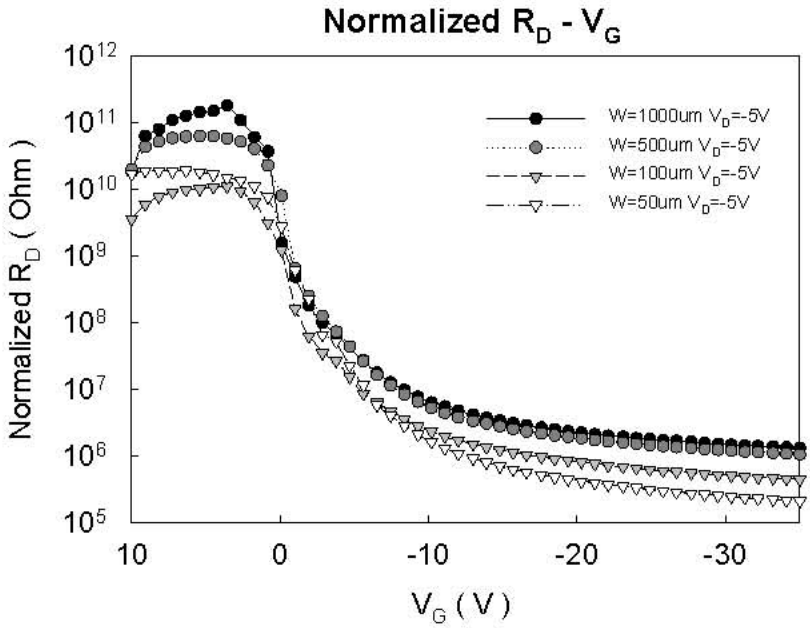



Figure 2-30: The mobility of OTFTs for linear and saturation region as the function of width .




(a)




(b)

Figure 2-31: (a)The normalized film resistances and (b)the normalized resistances at drain side as a function of gate voltage under drain bias $V_D$= -5V and -15V, taken with the different width of 1000um, 500um, 100um and 50um.

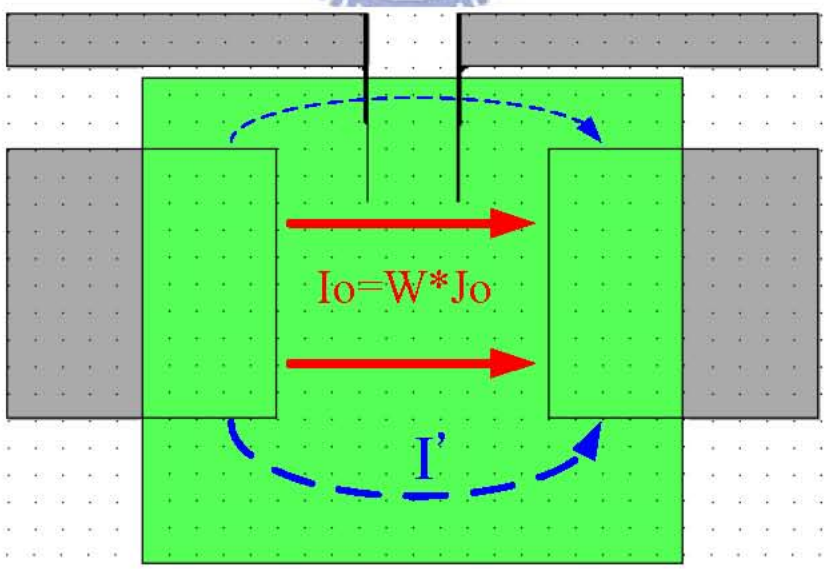



Figure 2-32: The border effect for device, which result from active region fabricated by shadow mask

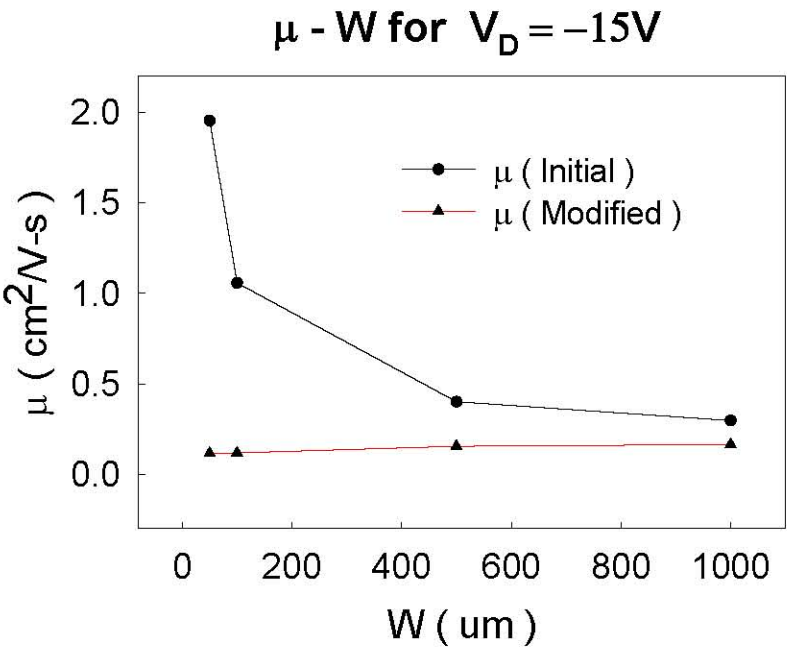



Figure 2-33: Comparison with initial mobility and modified mobility, modified by additional width.

# Chapter 3

# Variable temperature measurements

## 3.1 Introduction

The observed charge carrier mobility in organic semiconductors spans greater than ten orders of magnitude. As a consequence, there are a host of different models for explaining the microscopic mechanism of charge transport over such a huge range. We present a quick overview of the transport models relevant to OTFTs with particular attention to the temperature dependence of the mobility.

***Band transport***

There are large differences between the three-dimensional crystal lattice of most inorganic semiconductors and the amorphous structure of conjugated polymers. Inorganic semiconductor crystalline lattices, such as silicon and germanium, are characterized by long range order and strongly coupled atoms, in which silicon atoms are tightly held together by strong covalent bonds, with energies on the order of 70 kcal/mole for Si-Si bonds. For silicon and germanium, this results in the formation of long-range delocalized energy bands separated by a forbidden energy gap [41]. Charge carriers added to the semiconductor can move in these energy bands with a relatively large mean free path. These materials are very sensitive to chemical impurities, which constitute the principle of doping of these materials, and they are also marked by the presence of dangling bonds at their surface, leading to the high sensitivity of their electrical properties to surface states.

The limiting factor for this band transport is scattering of the carriers at thermal lattice vibrations, i.e. phonons [41-42]. This is depicted schematically in Figure 3-1(a). As the number of lattice vibrations decreases with decreasing temperature, the mobility of the charge carriers increases with decreasing temperature.

***Hopping transport***

Due to the disorder and the localization of charge, the motion of the charge carriers in organic semiconductors is typically described by hopping transport, which is a phonon assisted tunneling mechanism from site to site [43-44]. In Figure 3-1(b), if the carrier is localized due to defects, disorder or self localization, e.g. in the case of polarons, the lattice vibrations are essential for a carrier to move from one site to another. For hopping transport the mobility increases with increasing temperature. This hopping transport takes place around the Fermi level. Many of the hopping models are based on the single phonon jump rate description as proposed by Miller and Abrahams [45]. In this model the hopping rate between an occupied site i and an adjacent unoccupied site j, which are separated in energy by $E_i - E_j$ and in distance by Rij, is described by:

$$\nu_{ij} = \nu_0 \exp(-2\gamma R_{ij}) \begin{cases} \exp\left(-\dfrac{E_i - E_j}{KT}\right) \cdots\cdots\cdots E_i > E_j \\ 1 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots E_i < E_j \end{cases} \qquad (3\text{-}1)$$

where $\gamma$ quantifies the wave function overlap between the sites, $\nu_0$ is a prefactor, and K is Boltzmanns constant. The Miller-Abrahams model addresses hopping rates at low temperatures between shallow three-dimensional impurity states, assuming that the electron lattice coupling is weak. When the Miller-Abrahams model is applied to

polymeric semiconductors, it is assumed that the conjugated segments of the polymers play the role of nearly isolated impurity states, and that equation is still valid at high temperatures [45]. Depending on the structural and energetic disorder of the system, it can be energetically favorable to hop over a longer distance with a low activation energy (energy difference between sites), than over a shorter distance with a higher activation energy. This extension to the Miller-Abrahams model is called variable range hopping [45]. Monroe developed a model describing hopping transport around the Fermi level in an exponential density of states [46]. He found that this hopping description is analytically very similar to a model in which charge carriers are thermally activated to a transport level.

***Multiple trapping and release model***

For polycrystalline organic semiconductor layers, the temperature dependent transport data is often interpreted in terms of a multiple trapping and release model [47]. In this model, the organic semiconductor film consists of crystallites which are separated from each other by amorphous grain boundaries. In the crystallites the charge carriers can move in delocalized bands, whereas in the grain boundaries they become trapped in localized states. The trapping and release of carriers at these localized states results in a thermally activated behavior of the field-effect mobility, which depends on the gate voltage. The description of trapped, i.e. localized, charges which can be thermally activated to a transport level, in this case the band is very similar to hopping in an exponential density of states [46] as stated in the previous section. As the grain boundaries in a polycrystalline system determine the DC charge transport and typically an exponential trap distribution is used to model the experimental data, no clear

distinction can be made between hopping transport and multiple trapping and release, on the basis of the temperature dependence of the mobility. One should be able to separate a trap-limited mobility from a hopping mobility if the Hall mobility in a Hall effect experiment could be determined, since in a magnetic field, there will be no Lorentz force on trapped charges [48]. Unfortunately, due to the low charge carrier mobilities, the Hall effect is very difficult to measure experimentally.

***Polarons***

Next to the disorder-induced localization of charge, the strong electron-phonon coupling in organic materials results in localization of charge. An excess charge carrier on a conjugated polymer chain can minimize its energy by a local lattice deformation. This quasi particle consisting of charge and a lattice deformation, or phonon cloud, is called a polaron. As polarons represent a local distortion of the lattice, the associated energy levels must split off from the HOMO level and the LUMO level. These energy levels, which reside in the energy gap, have often been observed in optical absorption experiments on charged conjugated polymer films [49-51]. In polaronic charge transport, not only the charge moves under an applied electric field but the lattice deformation moves with it.

In this chapter, variable temperature electrical measurements are well-established means for determining the conduction mechanism in semiconductors. In amorphous and polycrystalline silicon, for example, temperature dependent measurements have been used to determine whether charge transport occurs in extended states, by variable range hopping (VRH) or by multiple trapping and release (MTR).

Each of these models predicts a specific temperature dependence of the charge carrier mobility that can be used to identify the underlying conduction mechanism. Variable temperature measurements also provide information about trap states and their distribution in the semiconductor.

## 3.2 Variable Temperature Measurements

### 3.2.1 The Multiple Trapping and Release (MTR) Model and The Meyer–Neldel Rule (MNR)

Variable temperature TFT measurements can be used to determine the temperature dependence of the mobility in a semiconductor thin film. The temperature dependence of the mobility can yield information about the conduction mechanism and trap states in the semiconductor. Several models have been proposed to explain thermally activated mobility in crystalline organic semiconductor films, but the multiple trapping and release (MTR) model is the most widely accepted [52]. MTR supposes that charge transport in the semiconductor is dominated by recurrent trapping into localized band-tail trap states below the conduction band edge followed by thermal release.

Thus, the effective mobility ($\mu_{eff}$) of a TFT is the free carrier mobility ($\mu_0$) reduced by the concentration of trapped electrons ($N_T$). We take n-type organic semiconductor for example.

$$\frac{\mu_{eff}}{\mu_o} = \frac{N_c}{N_c + N_T} = \frac{1}{1 + \frac{N_T}{N_{co}} \exp(\frac{E_c - E_F}{KT})} \tag{3-2}$$

where $N_C$ is the density of free electrons defined by

$$Nc = N_{CO} \exp(\frac{-(E_C - E_f)}{KT}) \tag{3-3}$$

$N_{CO}$ is the effective density of states at the conduction band edge ($E_C$), and $E_f$ is the Fermi energy. For simplicity's sake, we assume a discrete trap state at energy $E_T$ which captures electrons according to Fermi–Dirac statistics. Hence, integrating the delta function yields

$$N_T = N_{TO} \exp(\frac{-(E_T - E_f)}{KT}) \tag{3-4}$$

where $N_{TO}$ is the density of trap states (#/cm$^2$). Combining Equation (3-2) and (3-4) yields an Arrhenius-like form for the temperature dependence of the effective mobility

$$\mu_{eff} \approx \mu_o \exp(\frac{-E_a}{KT}) \tag{3-5}$$

where $E_a$ is the difference in energy between the discrete trap state and the conduction band edge ( $E_C$ - $E_T$ ), and we have assumed that $E_a$>>KT and $N_{CO}$~$N_{TO}$ . This simple interpretation of the MTR model predicts activated behavior for the effective mobility, with an activation energy which is the difference in energy between the trap state and the conduction band edge.

Typically, an exponential distribution ($n_T$) of traps is assumed to be a better representation of the trap states in the band-tail

$$n_T = N_{to} \exp(\frac{-(Ec - E)}{KT_o}) \tag{3-6}$$

where $N_{to}$ is the energy density of traps states at E=$E_C$ (#/cm$^2$-eV), and $T_o$ characterizes the width of the distribution. In this case, the activation energy in a TFT is a convolution of both trap depth and distribution. The applied gate voltage in the TFT moves the Fermi level through the trap distribution, closer to the band edge, which

increases the effective mobility. This creates a gate voltage dependence of the activation energy.

A consequence of assuming MTR model with an exponential distribution of trap states is that the Meyer–Neldel rule should hold. The Meyer–Neldel rule relates

$$G = G_o \exp(\frac{-E_a}{KT}) \tag{3-7}$$

$$G_o = G_{oo} \exp(\frac{E_a}{KT_o}) \tag{3-8}$$

between an electrical property G, its activation prefactor ($G_o$) and the activation energy, where $KT_o$ is the width of the trap distribution and is often called the Meyer–Neldel energy ($E_{MN}$).

### 3.2.2 Experiment Detail

The bottom-contact OTFTs in this experiment are fabricated by conventional process as described in chapter 2. The organic TFTs are prepared by evaporated pentacence on a transistor test substrate in thermal coater at temperature of 70°C. The transistor test substrate consists of dummy silicon wafer of low resistivity (1-100 Ω-cm) as gate electrode, a 200nm-thick $SiO_2$ insulating layer ( $C_i$=17 nF/cm$^2$ ) thermally grown in furnace and a patterned gold layer formed ohmic contacts as the gate four probe structure, including of the source, drain electrodes, sense probe1 and sense probe 2. The cross section of gate four probe structure is show in Figure 2-8.

After fabrication, the electric characteristics are measured by semiconductor parameter analyzer of HP4156 on a hot stage in atmosphere around dark environment. The semiconductor parameter analyzer of HP4156 equips with a hot plate for variable temperature measurement. At first, we controlled the measurement temperature at 20°C .

The drain current of the transfer curve measured as a function of gate voltage at drain voltage of -5V and -15V. The output characteristics was taken at gate voltage $V_G$= -10 and $V_G$= -30V. The $V_1$ and $V_2$ between channel were sensed by probe1 and probe 2 at the same time. Furthermore, we use the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon.

Then, we repeat the different variable temperature measurements at different temperature of 40°C, 60°C, 80°C, and 100°C. The transfer curve, the output characteristic and four probe measurements were all taken in different measurement temperatures respectively.

Finally, the sample would be stored carefully in dry cabinet to avoid moisture and pollution after measurement.

## 3.3 Results and Discussions

### 3.3.1 The Existence of Meyer–Neldel Rule (MNR)

Figure 3-2 show the transfer characteristics $I_D$-$V_G$ of OTFT with $V_D$= -5V and $V_D$= -15V, measured at the temperature of 20°C, 40°C, 60°C and 80°C. They can be taken as the extraction of the mobility and transconductance at different temperature. Some variation of the phenomenon at different temperature in the plot can be observed. That is, on-current increased and threshold voltage shifted toward positive with the rising temperature. The result of increasing current is similar to the saturation current of the output characteristics for pentacene-based OTFT at the gate voltage drop of -30V, taken at the substrate temperature of 20°C, 40°C, 60°C and 80°C as shown in Figure 3-3. They would be further discussed in next section.

Figure 3-4 and 3-5 show the temperature dependence of the saturation and linear regime mobility for the device described in Figure 3-2. The mobility is thermally activated from room temperature up to 375 K, with activation energies of 140.75 and 98.64 meV for the saturation and linear regime respectively. The mobility drops by a factor greater

than 2 from 0.15 $cm^2$/V-s at room temperature to 0.4 $cm^2$/V-s at 355 K. The reduced activation energy for linear compared to saturation regime data is interesting, because it hints at the dependence of activation energy on gate voltage. Indeed in the MTR model, the activation energy is predicted to decrease with increased gate voltage because the Fermi level is moved towards shallower band-tail states. This has been observed in amorphous silicon and other organic semiconductors [53-54]. In order to investigate the gate voltage dependence of he activation energy, we use a transconductance ($G_m$) in chapter 2:

$$G_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=connst} = \frac{WC_{ox}}{L}\mu V_D \cdots for \cdot\cdot linear \cdot\cdot region \qquad (2\text{-}2)$$

The $G_m$ is proportional to the device mobility in the linear regime. Figure 3-6 shows activation plots of $G_m$ for several gate voltages; the least-squares fits used to extract the activation energy. In Figure 3-7, the activation energy is shown a function of gate voltage. The activation energy is the greatest just above conduction onset and falls monotonically towards the linear regime value about 25 meV. Further analysis reveals a Meyer–Neldel rule between the transconductance prefactor ( $G_{m,o}$ ) and film activation energy, as shown in Figure 3-8. A Meyer–Neldel relationship was observed for electrical transport ,using a transconductance. There is a Meyer–Neldel relationship between the activation energy and the prefactor with a Meyer–Neldel energy ($E_{MN}$) of 30.03 meV, which corresponds well with the isokinetic temperature of 348.48 K.

Thereby, the Meyer–Neldel energy of 30.03 meV is similar to the value of the Meyer-Neldel energy on paper (see Table 3-1) and consistent with the isokinetic temperature of about 355 K shown in Figure 3-6. In the MTR model, the TFT turns on when the Fermi level moves into mobile states in the band tail. As the Fermi level moves closer to the band edge with increasing gate voltage, it moves through the distribution of band-tail states, thus the measured activation energy for a device is integrated over the distribution of band-tail states.

### 3.3.2 Sensitivity to Variable Temperature during Measurement

We took effort on the variable temperature measurement at different temperature of 20°C, 40°, 60°C, 80°C, and 100°C. The transfer curve, the output characteristic and four probe measurement were all taken in different measurement temperatures. The drain current of the transfer curve measured as a function of gate voltage at drain voltage of -5V and -15V. The output characteristics was taken at gate voltage $V_G$= -10 and $V_G$= -30V. The $V_1$ and $V_2$ between channel were sensed by probe1 and probe2 at the same time. Furthermore, we use the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon.

Figure 3-9 show the plots of film resistance as a function of gate voltage at the drain voltage of $V_D$= -5V and $V_D$= -15V for an operating OTFT at different temperature of 20°C, 40°C, 60°C and 80°C. It can be found that the film resistance between probe1 and probe2 decrease with the rising temperature. It is similar to the the resistance in channel as a function of drain voltage under gate bias $V_D$= -20V and $V_G$= -30V , taken at the temperature of 20°C, 40°C, 60°C and 80°C as shown in Figure 3-10. The reason for the reduced film resistance is that the trapped carriers in pentacene is thermally

activated so that the film resistance is reduced. It attributes to the mobility increasing as shown in Figure 3-4 and 3-5. Therefore, corresponding to the Figure 2-2 and 2-3, the on-current is higher. On the other hand, the more carriers in the deep traps could be activated and released to hopping at the higher temperature. There are relatively less positive carriers trapped in trap states at higher temperature, comparing to at lower temperature, as shown in Figure 3-13 and 3-14. The relative less carriers at traps lead to the threshold voltage shift toward positive, as shown in Figure 3-11. The threshold voltage versus temperature under drain bias ($V_D$= -5V and -15V), in linear region and saturation respectively are corresponded to Figure 2. For the same reason, the subtreshold swing (see Figure 3-12) can be better.

In short, the carriers in pentacene is affected by thermal activation. Samples with higher temperature during measurement were observed to have better mobility, higher on-current and lower resistance, which agrees well with the multiple trapping and release model proposed to explain the conduction mechanism in small molecule OTFTs.

## 2.4 Summary

In this chapter, we properly use the multiple trapping and release model to explain the thermally activated phenomenon .

The Arrhenius relationship illustrates the activated nature of mobility for electrical transport, using a transconductance. There is a Meyer–Neldel relationship between the activation energy and the prefactor with a Meyer – Neldel energy of 30.03 meV, which corresponds well with the isokinetic temperature of 348.48 K.

Therefore, the carriers with exponential distribution of trap states in pentacene is affected by thermal activation. Samples with higher temperature during measurement

were observed to have better mobility, higher on-current and lower resistance, which agrees well with the multiple trapping and release model proposed to explain the conduction mechanism in small molecule OTFTs.

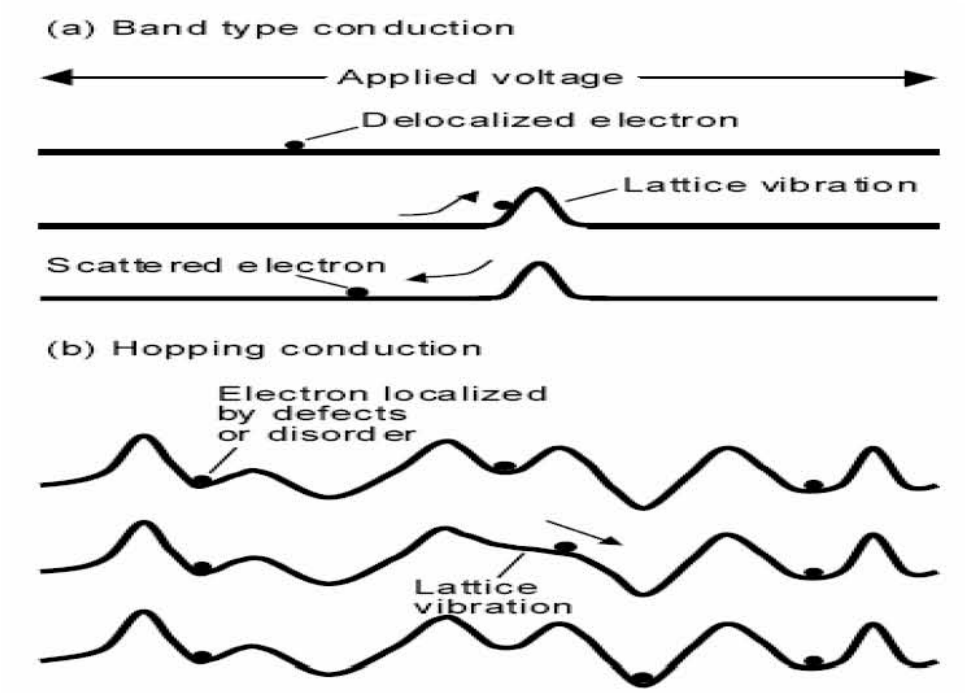



Figure 3-1: Charge transport mechanisms in solids. (a)Band transport. In a perfect crystal, depicted as the straight line, a free carrier is delocalized. There are always lattice vibrations that disrupt the crystal symmetry. Carriers are scattered at these phonons, which limit the charge carrier mobility. The mobility for band transport increases with decreasing temperature. (b) Hopping transport. If the carrier is localized due to defects, disorder or self localization, e.g. in the case of polarons, the lattice vibrations are essential for a carrier to move from one site to another. For hopping transport the mobility increases with increasing temperature. (M. Matters et al. Synth. Met. 1999 [42])

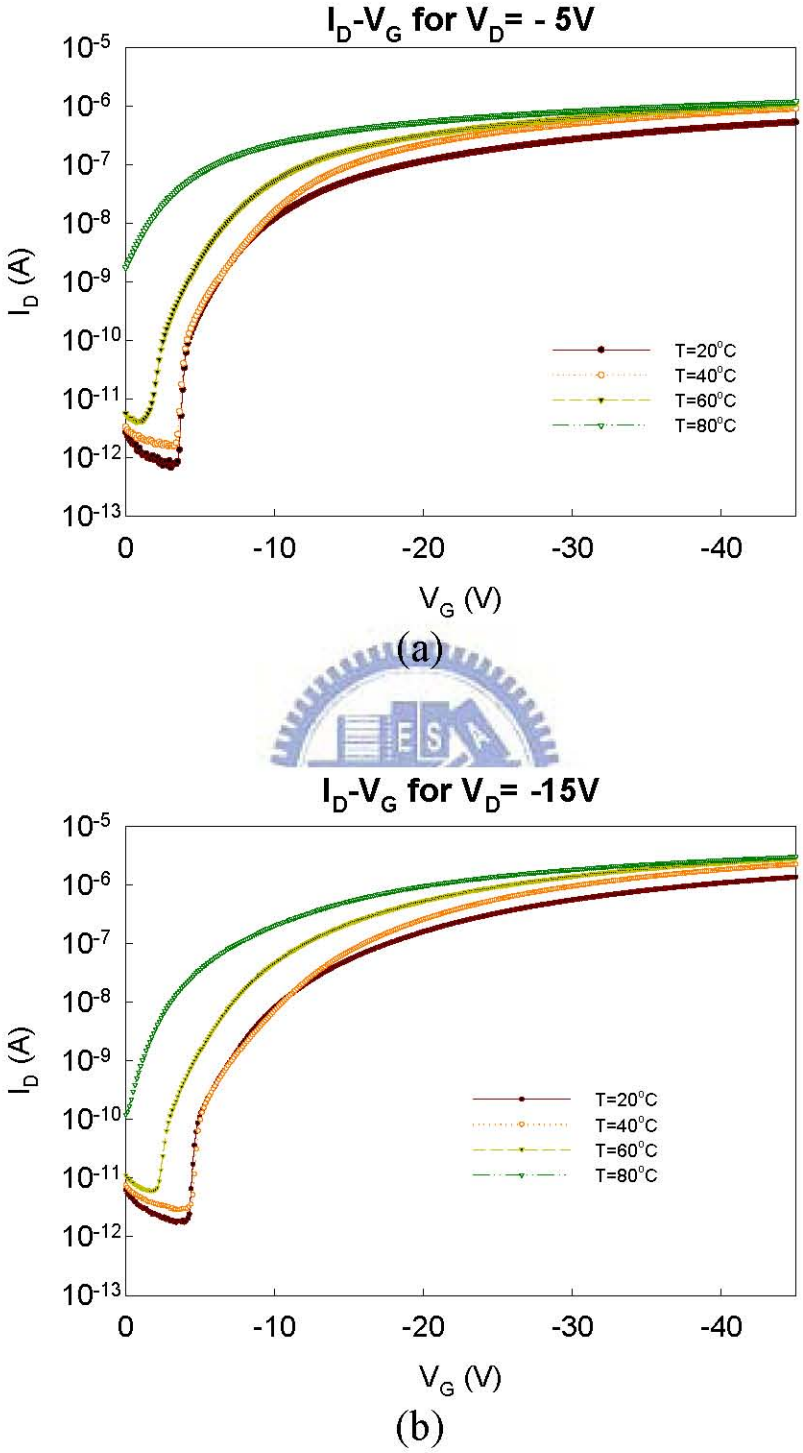



Figure 3-2: The Transfer characteristics $I_D$-$V_G$ of OTFT with (a)$V_D$= -5V and (b)$V_D$= -15V, measured at the temperatures of 20°C, 40°C, 60°C and 80°C.

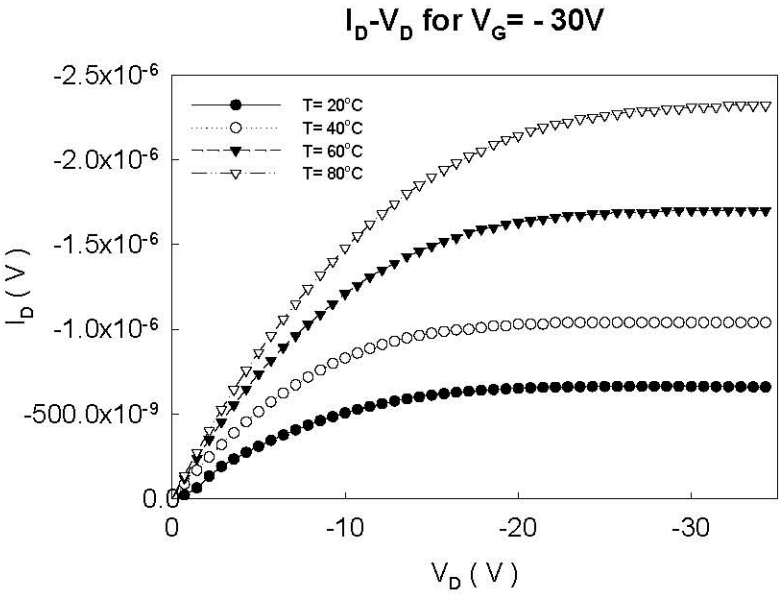



Figure 3-3: The output characteristics for pentacene-based OTFT with four probe structure at the gate voltage drop of -30V, taken at the substrate temperatures of 20°C, 40°C, 60°C and 80°C.

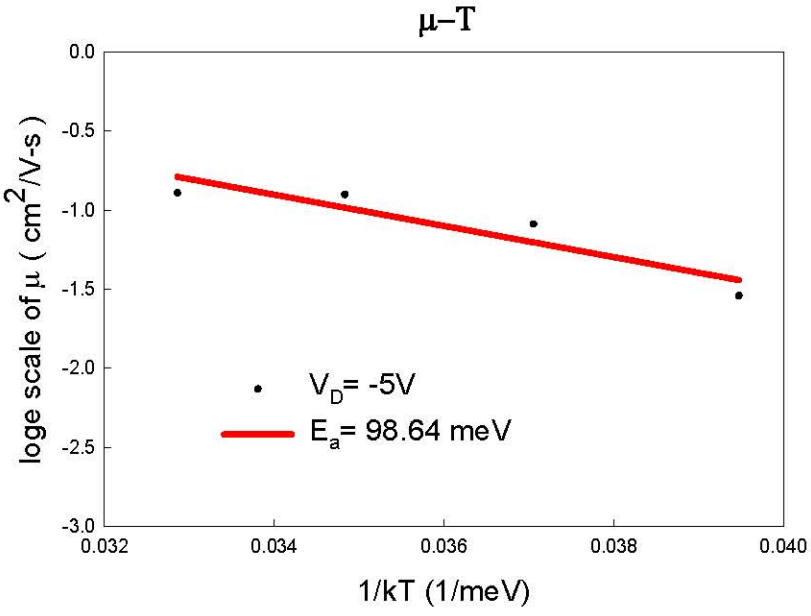



Figure 3-4: Arrhenius plot of linear regime mobility illustrating the activated nature of mobility in pentacene-based OTFT over a

temperature range (293-375K).

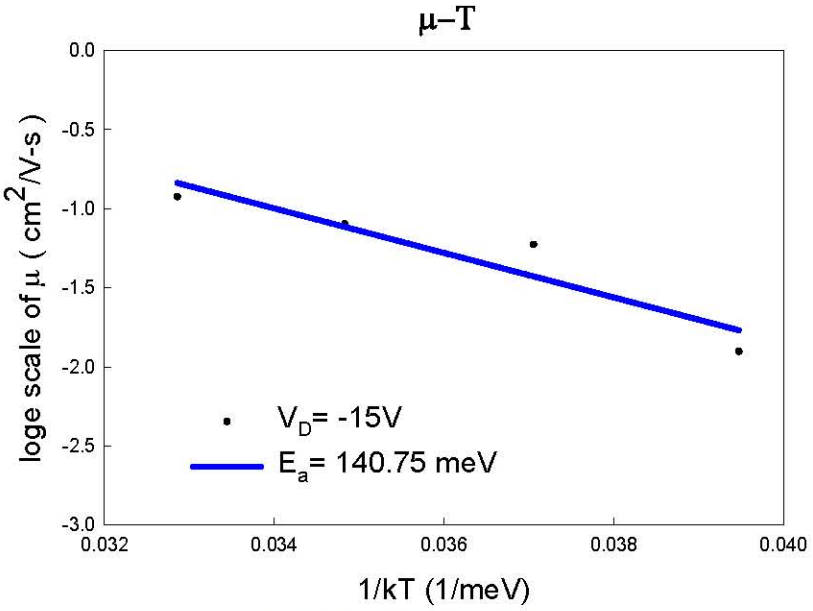



Figure 3-5: Arrhenius plot of saturation regime mobility illustrating the activated nature of mobility in pentacene-based OTFT over a temperature range (293-375K).

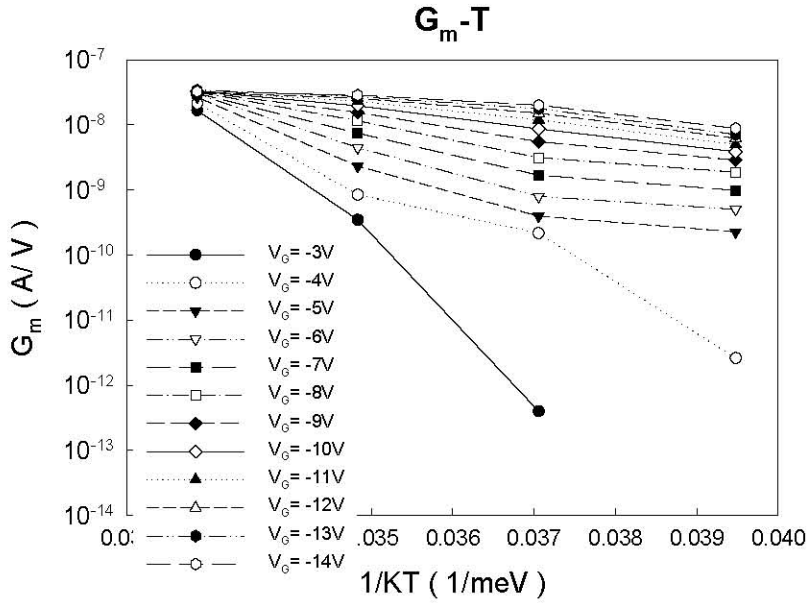



Figure 3-6: Activation plots of transconcutance for different gate voltages for the device corresponding to Figure 3-1. The activation fits appear to intersect at 355 K approximately, which is the isokinetic temperature.

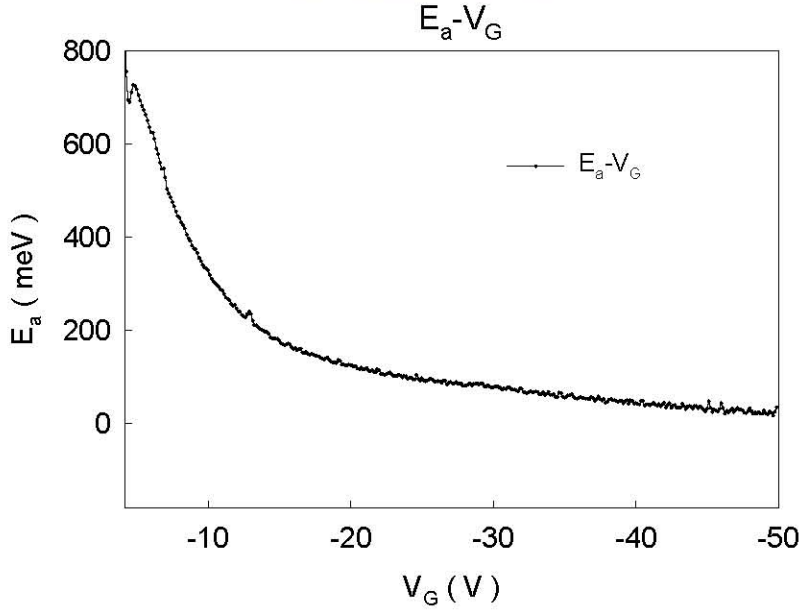



Figure 3-7: Plot of activation energy derived from the transconductance as a function of gate voltage.

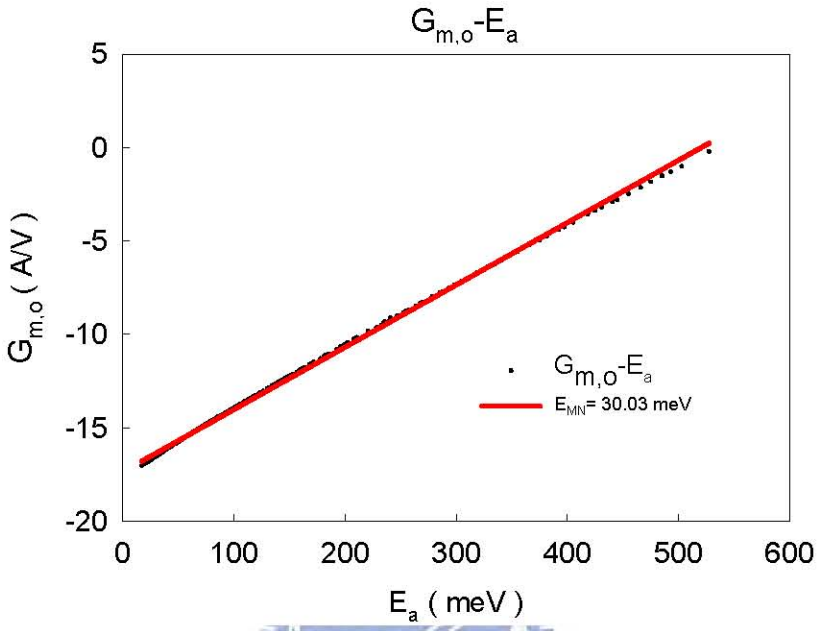



Figure 3-8: A semilog plot of the transconductance prefactor versus activation energy. There is a Meyer–Neldel relationship between the activation energy and the prefactor with a Meyer–Neldel energy of 30.03 meV, which corresponds well with the isokinetic temperatures of 348.5 K.

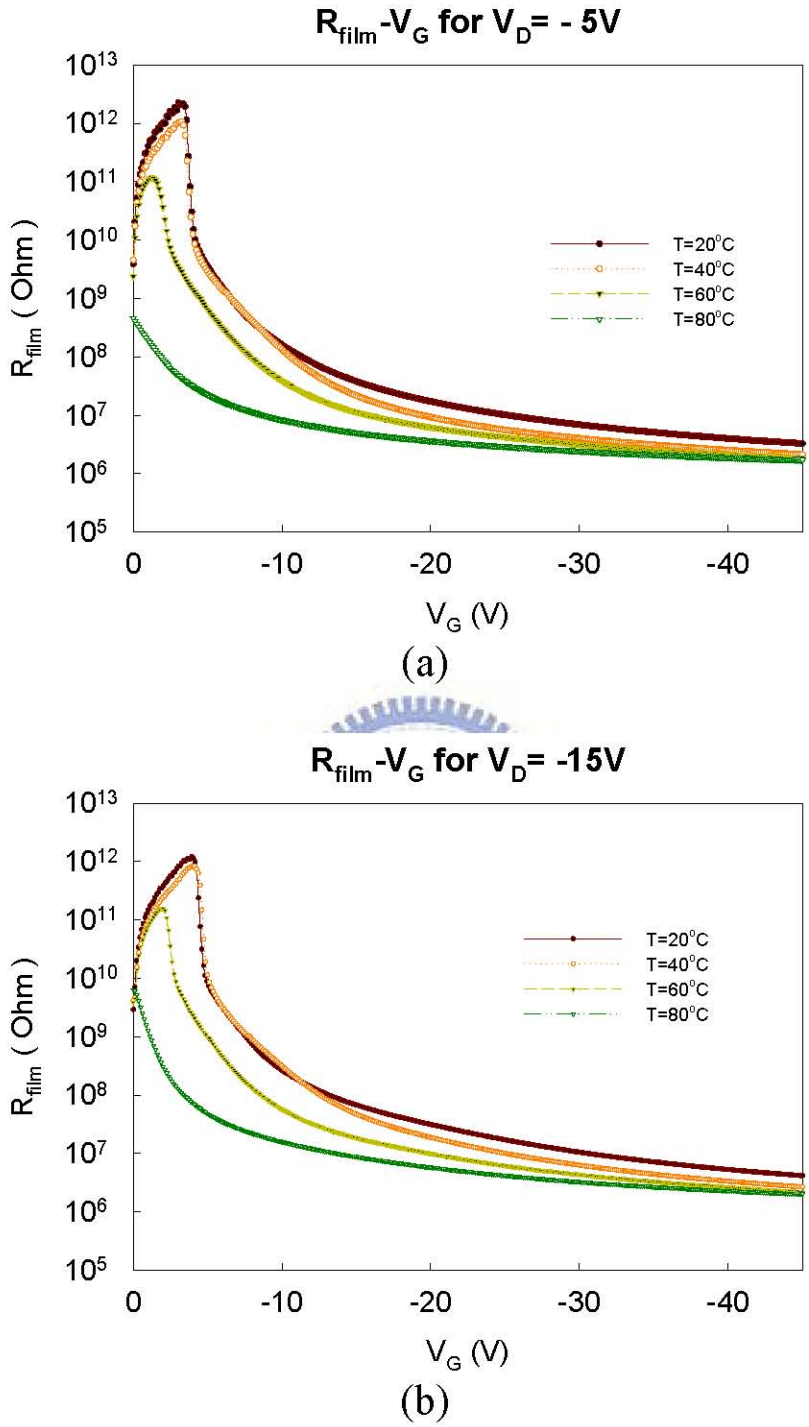



Figure 3-9: Plots of film resistance as a function of gate voltage at the drain voltage of (a)$V_D$= -5V and (b)$V_D$= -15V for an operating OTFT at different temperatures of 20°C, 40°C, 60°C and 80°C.

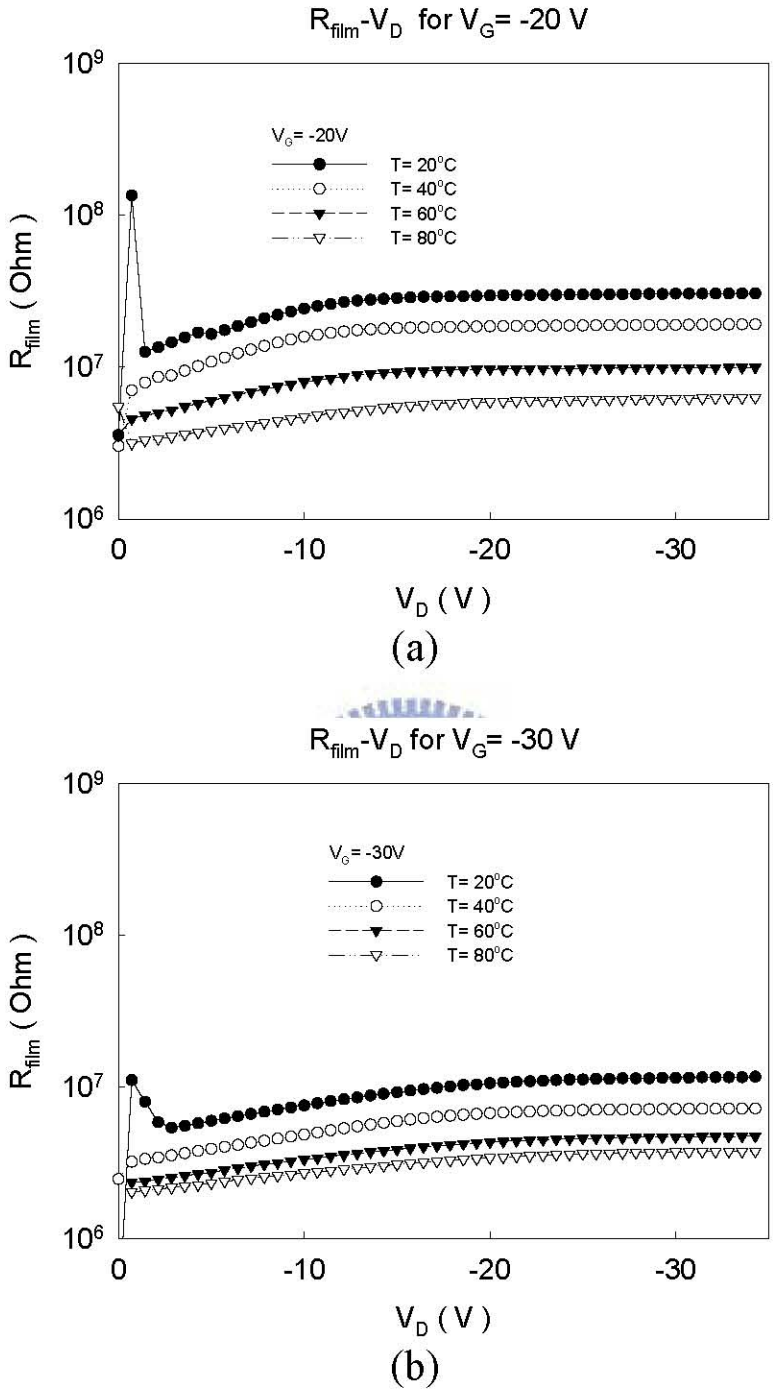



Figure 3-10: The resistance in channel as a function of drain voltage under gate bias of (a)$V_D$= -20V and (b)$V_G$= -30V, taken at the temperatures of 20°C, 40°C, 60°C and 80°C.

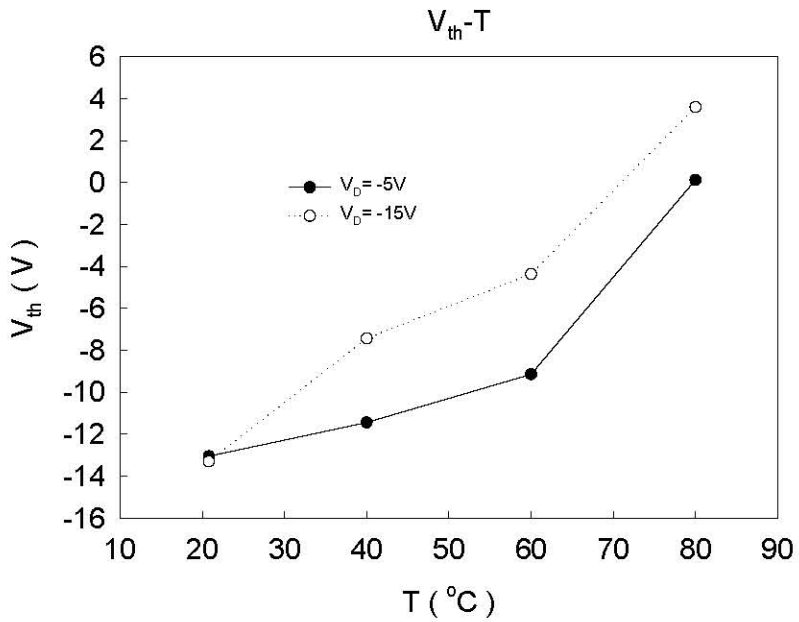



Figure 3-11: The threshold voltage versus temperature under drain bias ($V_D$= -5V and -15V), in linear and saturation region respectively.

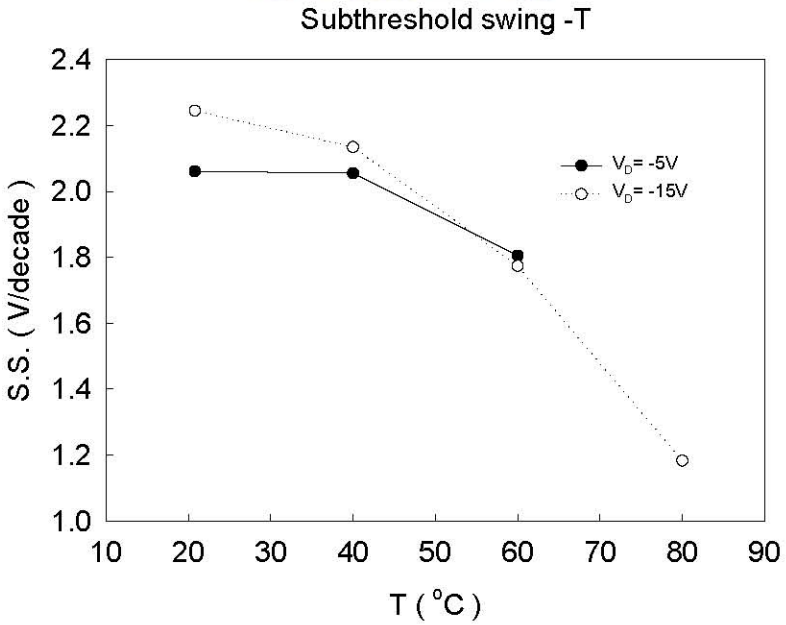



Figure 3-12: The subthreshold swing versus temperature under the drain voltage of -5V and -15V

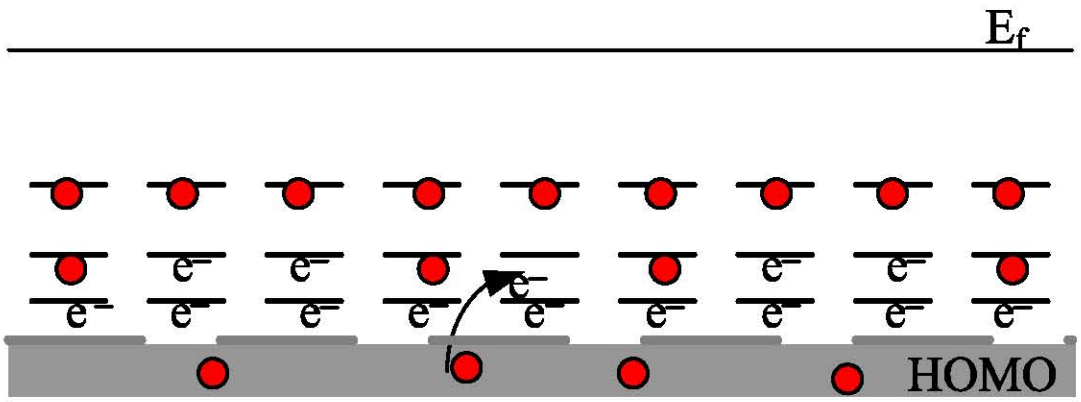



Figure 3-13: Schematic illustration of conduction by multiple trapping and release at lower temperature.

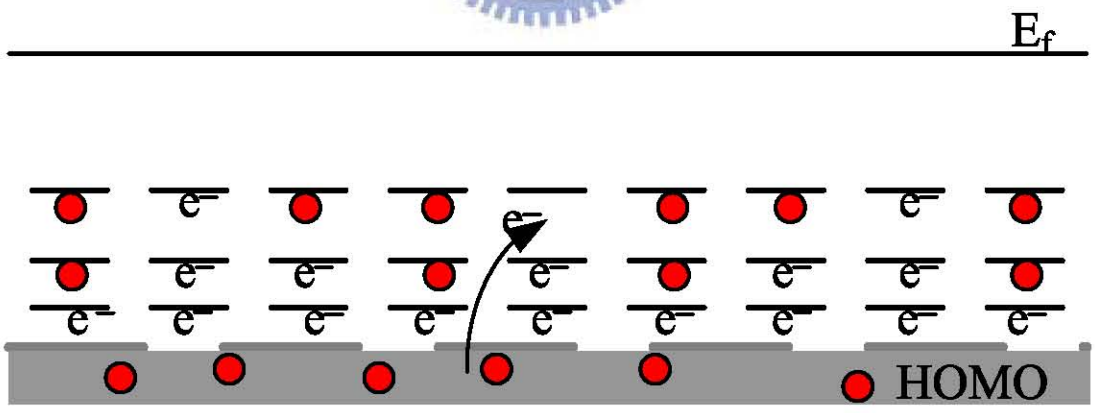



Figure 3-14: Schematic illustration of conduction by multiple trapping and release at higher temperature.

Table 3-1: The relative list of Meyer–Neldel Energy

| Data reported in literature | |
|---|---|
| Materials | **Meyer – Neldel Energy** |
| dihexyl-sexithiophene | 43 meV |
| $C_{60}$ | 36 meV |
| PTV | 35 meV |
| pentacene | 34 meV |
| PTCDI-$C_5$ | 20 meV |

# Chapter 4

# Electric Instability of Pentacene-Based OTFTs

## 4.1 Introduction

Organic semiconducting materials used as active layer in thin film transistors have received considerable interesting [55-58] and organic thin film transistors (TFTs ) have been the subject of investigation for several years [59-60]. Mobility as hlgh as 2 $cm^2$/V-s have been reach in evaporated pentacene transistors [61] and 0.1$cm^2$/V-s in solution-process pentacene [62] and poly-3-hexylthiophenephene [63]. These mobilities are comparable to those in amorphous silicon TFTs [64-65]. Additionally, OTFTs exhibit great potential for special application such as flexible display, RF tags, and smart cards. In this respect, there is no obstacle for a real application of organic TFT [62]. However, an important aspect of the organic TFT is the stability both in ambient atmosphere and under device operation.

Comparing to inorganic semiconductor, the stability of OTFTs is poor with time evolution while different environmental ambient such as nitrogen, oxygen or moisture would affect the performance of organic device [68-70]. Organic materials are more sensible and weaker than inorganic materials. Therefore, stability issues of these organic devices is another challenge which should be kept in mind. Besides, electric stability of OTFTs during long time operation is another important needed subject of research.

Typically, the instabilities are observed as a shift of the threshold voltage ($\Delta V_{th}$) accompanied by a possible change in the charge carrier mobility, which is due to charge

trapping at the gate – dielectric interface or at defect sites in the active layer itself [64]. Both of them are found in pentacene-based TFTs. Also the origin of the changing threshold voltage is not known, which complicates the analysis of the transport properties and depredates potential use of organic TFTs in applications. Therefore, we attempted to analysis instability phenomenon and explain trapping charge mechanism during stress. The studies of the operational lifetime would be adapted and we investigate the behavior of OTFTs during stress

In this chapter, we found the instability of electrical characteristics in a continue series measurements and investigated the characteristics of bottom-contact pentacene-based OTFTs under drain current stress conditions. Here, we understand that polarization phenomenon play an important role during stress, and thus we provide the rough energy band figure to depict these special properties of OTFTs. The effect of these charge trapping instability on the measured threshold voltage and mobility on the transport studies will be discussed. However, more practical issues have to be taken into accountant. The influence of the atmosphere ( i. e. water and oxygen ) around the organic TFT should be concerned at the same time.

## 4.2 Instability of OTFTs during current stress

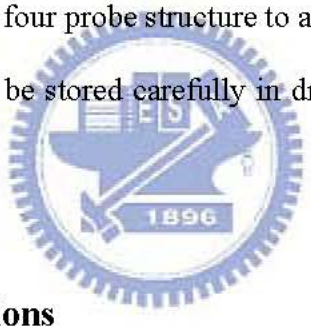
### 4.2.1 Experiment Detail

The bottom-contact OTFTs in this experiment were fabricated by conventional process as described in chapter 2. The organic TFTs were prepared by evaporated pentacence on a transistor test substrate in thermal coater at temperature of 70°C. The transistor test substrate consists of dummy silicon wafer of low resistivity (1-100 Ω-cm)

as gate electrode, a 200nm-thick $SiO_2$ insulating layer ( $C_i$ = 17 nF/cm$^2$ ) thermally grown in furnace and a patterned gold layer formed ohmic contacts as the four probe structure , including of the source electrode, drain electrode, sense probe1 and sense probe 2. The cross section of four probe structure is show in Figure 4-1.

After fabrication, the electric characteristics were measured by semiconductor parameter analyzer of E5270B at room temperature in atmosphere around dark environment. The drain current of the transfer curve measured as a function of gate voltage at drain voltage of -5V and -15V. Later, the output characteristics were taken at gate voltage $V_G$= - 10 and $V_G$= -30V. The $V_1$ and $V_2$ between channel was sensed by probe 1 and probe 2 at the same time. Furthermore, we use the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon.

Finally, the sample would be stored carefully in dry cabinet to avoid moisture and pollution after measurement.



### 4.2.2 Results and Discussions

We monitored the transfer characteristics while applying a current stress of -2× $10^{-7}$ A at gate voltage of -20V. As shown in Figure 4-2, the transfer characteristics $I_D$-$V_G$ of OTFT with $V_D$= -5V and $V_D$= -15V respectively after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s. The on-current gradually decay with time and the threshold voltages have shift toward more negative. At first, the subthreshold swing is unstable and have the perturbation between 1 V/decade and1.5 V/decade (see Figure 4-3). The one reason for perturbation phenomenon was artificial extraction error in measurement and another was that unstable property of OTFT. In spite of the instability in subtrashold swing (see Table 4-3), the threshold voltage shift tended toward more

negative and the shift was obviously as shown in Figure 4-4 and Table 4-1. In Figure 4-5 and Table 4-2, we can find the field effect mobility was about 0.4 $cm^2/V$-s in linear region and 0.3 $cm^2/V$-s in saturation region and decay slightly with stress time. The major change in lower drain current as shown in Figure 4-2 was converted back to a threshold voltage shift.

From the literature [22], the shift in threshold voltage under bias stress and its recovery, are very similar for thermal oxide and PECVD silicon nitride dielectrics. These results suggest that the pentacene material, rather than the dielectric, determines the TFT properties. We would also discuss further about degradation of material later according to four probe measurement. Therefore, the negative threshold shift would be concerned about trapping positive charge in semiconductor directly. The two reasons would likely be concerned about negative threshold voltage shift as shown in Figure 4-6, First, the dangling bonds in grain boundary would be considered for the reason of the mixed phase in thin film. The accumulated carriers hopping in channel through $\pi$ bond facilitate charge trapping in the dangling bonds after a long operational period. Second, due to molecular extending structure in electrical field, $\pi$ bonds happened to out of control so that the hopping behaviors was temporally abnormal and the less mobile states formed. If the stress is operated for a long time, the defect sites are more likely to form and trapping charges appear. All of them ( see Figure 4-6 ) would trap carrier charges in semiconductor during operation. In Figure 4-7, the energy band diagram show the formation of the positive trapping charges between LUMO and HOMO. Figure 4-7(a) is the energy band diagram of a metal and a semiconductor with an oxide layer between them, and Figure 4-7(b) is the energy level of pentacene.

In Figure 4-8, 4-9 and 4-10, they indicate that the current stress lead to the

degradation of material for $R_D$, $R_{film}$ and $R_S$. Comparing them, they can be found that the magnitude of degradation for $R_D$ is rather than $R_{film}$ and $R_S$. From Figure 4-8, it depicts the difference between $R_D$ in linear region and saturation region. Because the less carriers due to trapping more charges at drain side gradually lead to the more formation of depletion region, the resistance at drain side in saturation region would increase more obviously than in linear region with stress time. The Figure 4-11, 4-12 and 4-13, the resistances as the function of $V_D$, double checks the reason mentioned above. The current stress lead to the degradation of material for $R_D$, rather than $R_{film}$ and $R_S$, and the less carriers due to trapping charges at drain side gradually lead to the more formation of depletion region.

It is interesting to observe that the voltage drops of channel between probe1 and probe2, drain side, and source side in linear region as a function of gate voltage unchanged with the increase of current stress time as shown in Figure 4-14. They depict the uniform degradation for the same voltage percentage in channel when current stress time increase. Additionally in Figure 4-15, the voltage drop or the percentage of the voltage drop at drain side in saturation region become larger due to less carriers and more depletion region. In contrast, the voltage drops of channel between probe 1 and probe 2 or the percentage of voltage drop in channel reduced at the same time. In Figure 4-17 and 4-18, the voltage drops of channel between probe 1 and probe 2, drain side, and source side at gate bias ($V_G$= -10V and -30V) as a function of drain voltage double check the mentions above. In the linear region, voltage drops are the same but change in saturation region. They depicted the uniform degradation with the same voltage percentage in linear region when current stress time increase and the percentage of the voltage drop at drain side become larger due to less carrier and more depletion region in

saturation region. The Figure 4-17 and 4-18 is the voltage drop as the function of drain voltage, corresponding to the output characteristic in Figure 4-16.

## 4.3 The Recovery after Current Stress and Polarization Phenomenon

### 4.3.1 Experiment Detail

The bottom-contact OTFTs of four probe structure in this experiment were fabricated by conventional process as described above. After the current stress time of 20000s, the sample was left unstressed for 45 minutes.

Then, the electric characteristics were measured by semiconductor parameter analyzer of E5270B at room temperature in atmosphere around dark environment again. The drain current of the transfer curve measured as a function of gate voltage at drain voltage of -5V and -15V. Later, the output characteristics were taken at gate voltage $V_G$= -10 and $V_G$= -30V. The $V_1$ and $V_2$ between channel was sensed by probe 1 and probe 2 at the same time. Furthermore, we used the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon.

Finally, the sample would be stored carefully in dry cabinet to avoid moisture and pollution after measurement.

### 4.3.2 Results and Discussions

After leaving the sample unstressed for a period time of 45 minutes, the characteristic of degradation was gradually recovered as shown in Figure 4-19.

Comparing with after stress and after release, the transfer characteristics of the device at drain voltages $V_D$= -5V and $V_D$= -15V show the shift in thresholed voltage. The shape of the curves does not seem to change [60].

The output characteristics at gate voltage $V_G$= -10 and $V_G$= -30V indicated that the off-current recover to on-current at $V_G$= -10V after release. This indicates that , after stressing , an equal amount of charge per unit area was being accumulated ,but later , up to $\Delta V_{th}$, the accumulated charge is significantly less mobile and even trapped. However, they could be released through a unstressed time. The recovery process can be enhanced by applying a positive gate bias stress. Schematic of organic field transistor as shown in Figure 4-20 provide an idea that the recovered characteristic was oringinated from the formation of dipole during the current stress.

We found the polarization properties of pentacene-based OTFTs affected the threshold voltage shift enormously in various stress condition. Next, we try to investigate the properties further. A paper reported some self-assembled monolayers have built-in dipole field of 1 MV/cm [66-67]. To produce the same field as applying a voltage across the 100 nm-thick $SiO_2$ gate insulator, gate voltage of 10V is necessary.

Thereby, we can confirm that the polarization effect was caused by the pentacene film itself through stress. When the gate bias applied, the electric field established and expended the structure of molecular to form a dipole and twirled the direction of dipoles in organic active layer. The dipole built a field that direction opposite to that established by gate bias. The larger voltage bias established stronger electric field and induce more dipoles in organic active material that result in larger threshold voltage shift. The dipole built-in field would reinforce with the stress time and ease the net electric field in organic active layer.

During the current stress, the stretched dipole contributed to the trapping carrier charges in pentacene due to the formation of less mobile states and defect sites. After leaving the sample unstressed for a period time of 45 minutes, the stretched dipole would gradually recovered and trapping charges in less mobile states would release. Therefore, after release, the accumulated carrier trapped in less mobile states would reduced and the threshold voltage shift recovered.

Figure 4-21 show that the energy level of flat band with the positive charges induced by dipole, and diagram of band bending of a MOS structure after the current stress. Smooth band bending due to the energy level of interface was pined down by the positive charges. According to the equation of current-voltage deduced from charge sheet model in saturation region below from (2-3)

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_G - V_{th})^2 \cdots for \cdots saturation \cdots region \quad (2\text{-}3)$$

The change which resulted in drain current was later converted back to a threshold voltage shift, leading to the on-current decreasing.

Figure 4-22 show that the energy level of flat band, and diagram of band bending of a MOS structure after its recovery. Because the pined energy level recovered, the band bending could be more winding and induced more accumulated carriers.

The resistances as a function of gate voltage under drain bias of $V_D$= -5V and $V_D$= -15V at drain side, source side and channel between probe1 and probe2 in Figure 4-23 depict just the effect of threshold voltage shift toward positive after release of 45 minutes and the resistance reduced due to recovered dipole.

The resistances shown in Figure 4-24(a) as a function of drain voltage under gate bias ($V_G$= -30V) for drain side, source side and channel between probe 1 and probe 2 describe that the resistances reduced after release of 45minutes. The reason is that the

dipole recovered, the traps reduced and the depletion region can become smaller.

In Figure 4-24(b), the voltage drops or the percentage of the voltage drop at drain side become smaller due to more carriers and less depletion region. In contrast, the voltage drops of channel between probe 1 and probe 2 or the percentage of voltage drop in channel increased at the same time.

The less mobile states can be located in the organic semiconductor at the semiconductor-interface so that trapping charges and polarization phenomenon appear. It notes that polarization phenomenon plays an important role during stress. The dipoles built-in field will reinforce with time and decrease the net electric field in organic active layer, so that threshold voltage shift will form. They will slowly recover after release from stress.

## 4.4 Transient Stress Phenomenon in Measurements

### 4.4.1 Experiment Detail

The bottom-contact OTFTs of four probe structure in this experiment are fabricated by conventional process as described above.

When we measured $I_D$-$V_G$ and $I_D$-$V_D$ repeatedly, it was boring to find the instability during each measurements. Thereby, a continue series measurements with no break were operated for a purpose of distinguishing from variations. The electric characteristics were measured by semiconductor parameter analyzer of E5270B at room temperature in atmosphere around dark environment. It was not obvious and regular for phenomenon, therefore it is not suggested to use the data of voltage drops and resistances between channel by four probe structure to analyze phenomenon.

Finally, the sample would be stored carefully in dry cabinet to avoid moisture and pollution after measurement.

### 4.4.2 Results and Discussions

In Figure 4-25, comparing with the transfer curve for the first, third, and fourth measurements, the shift in threshold voltage was gradually toward negative for each measurement. The shape of curve did not seem to change. The detail data of mobility and threshold voltage are presented in Table 4-4. At the same time, comparing with the output characteristics for first, third and fourth measurement, the lower on-current was converted back to a threshold voltage shift during the transient stress from each measurement. It is easy to find that the life time of recovering dipole induced by stress in OTFT are significantly longer than inorganic TFT. The behavior of induced dipole matched the phenomenon mentioned above.

## 4.5 Summary

In this chapter, the electric reliability of OTFTs is tested. We understand the instability of electrical characteristics in a continue series measurements and investigated the characteristics of bottom-contact pentacene-based OTFTs under drain current stress conditions.

The current stress lead to the degradation of material for $R_D$, rather than $R_{film}$ and $R_S$. The magnitude of degradation for $R_D$ in linear region is rather than in saturation region. The degradation in linear region is uniform with the same voltage percentage when current stress time increase.

The field-effect mobility, subthreshold swing and threshold voltage were extracted to analyze the phenomenon and the obvious variation from current stress is the shift in threshold voltage.

Reports of instabilities in OTFTs have been rare. However, Knipp et al. recently observed reversible threshold voltage shift in pentacene OTFTs. They concluded that gate bias induced structural changes in the pentacene film, which produced trap states and led to the threshold voltage shift [22].

Here, we find that polarization phenomenon play an important role during stress. The built-in field from the induced dipole is originated from the pentacene film in the applied field. Thus, we provide the rough energy band figure to depict these special properties of OTFTs and Figure 4-26 provide the summary for threshold voltage shift after stress and release.

The studies of the transport and trapping charges are discussed. However, more practical issues have to be taken into accountant. The influence of the atmosphere ( i. e. water and oxygen ) around the organic TFT should be concerned at the same time.

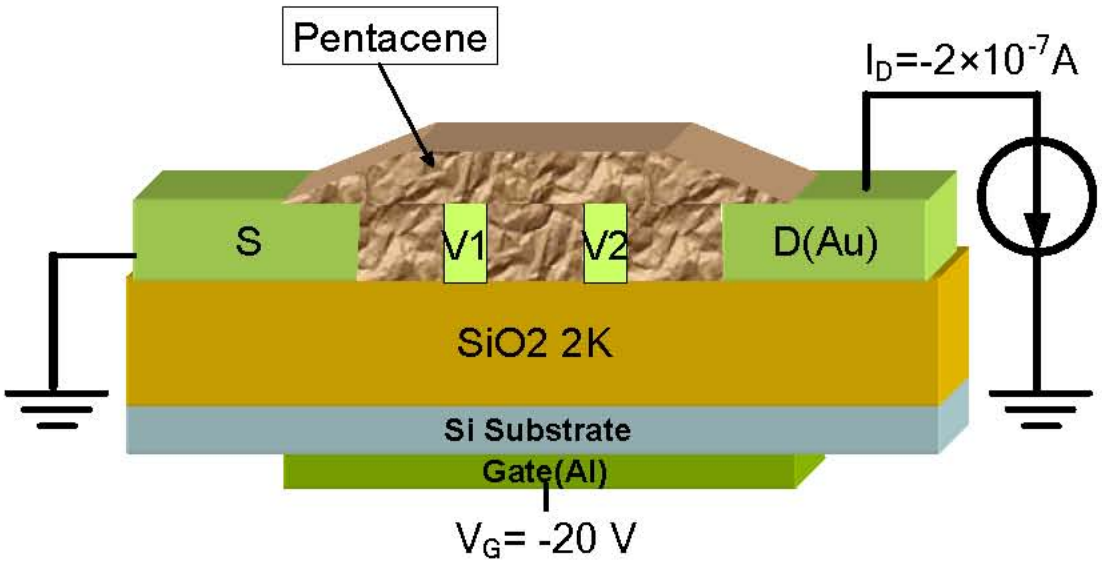
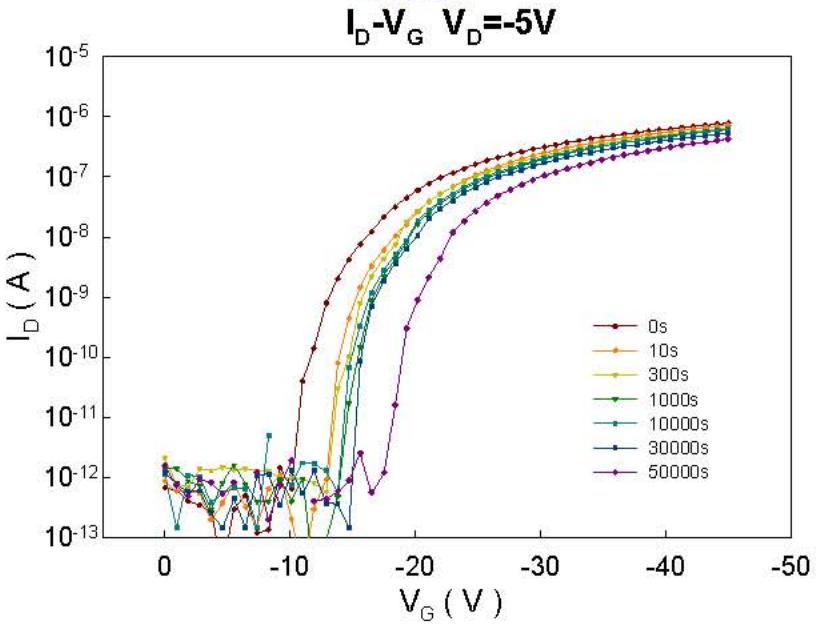
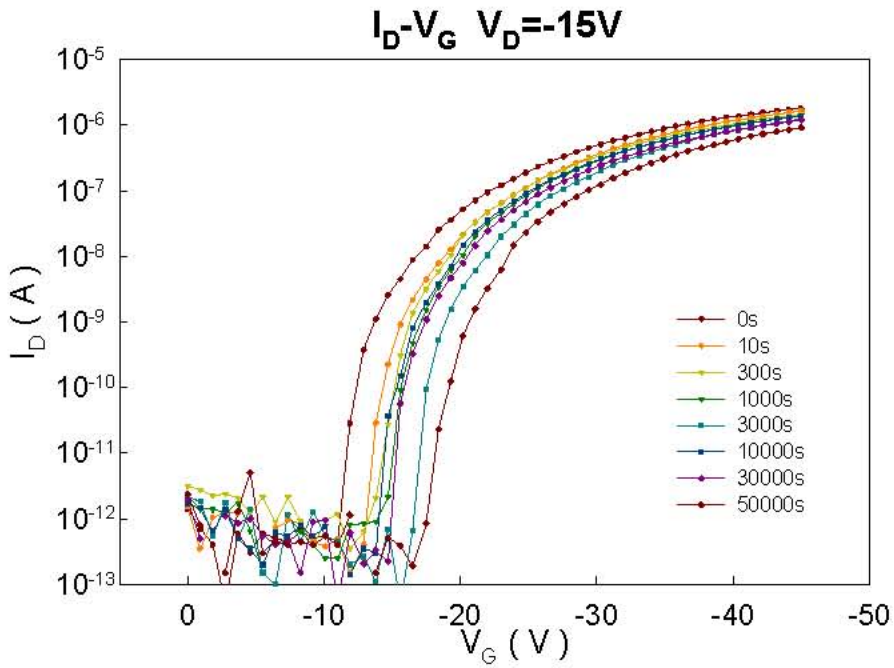



Figure 4-1: The schematic diagram of the bottom-contact OTFT with four probe structure. The applied current source is $2\times10^{-7}$A with DC gate bias ( VG= -20V ) to induce a channel of accumulated carriers .




(a)




(b)

Figure 4-2: The transfer characteristics $I_D$-$V_G$ of OTFT with (a)$V_D$= -5V and (b)$V_D$= -15V after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

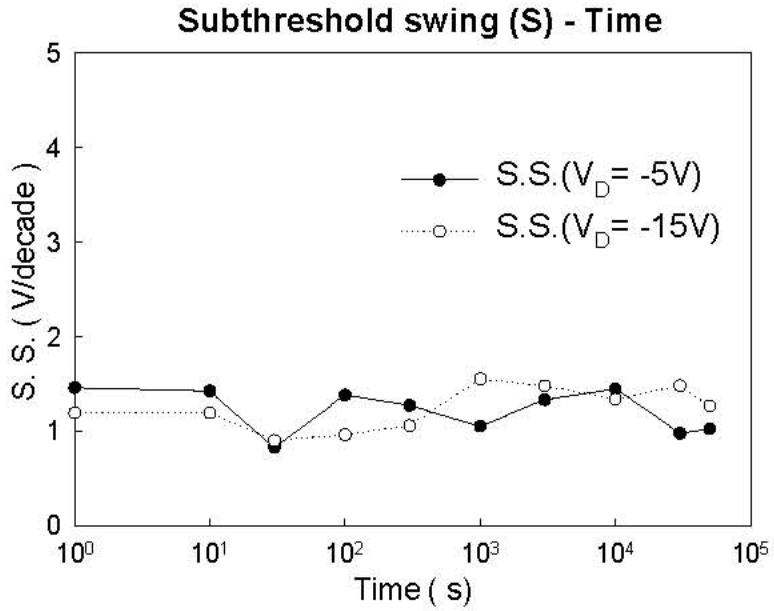



Figure 4-3: The subthreshold swing versus time under drain bias ($V_D$= -5V and -15V), taken after 0s, 10s, 1000s, 10000s, 30000s and 50000s current stress.

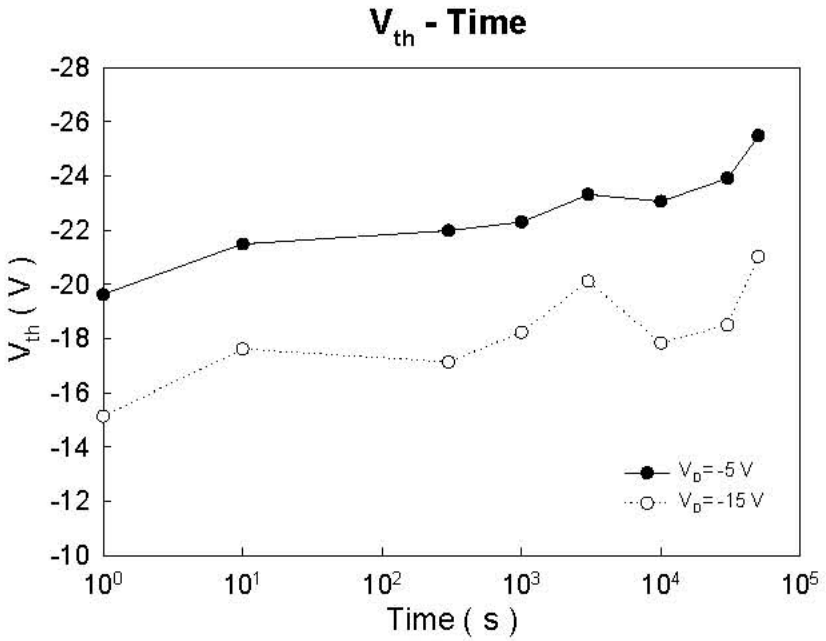



Figure 4-4: The threshold voltage versus time under drain bias ($V_D$= -5V and -15V) taken after 0s, 10s, 1000s, 10000s, 30000s and 50000s current stress.

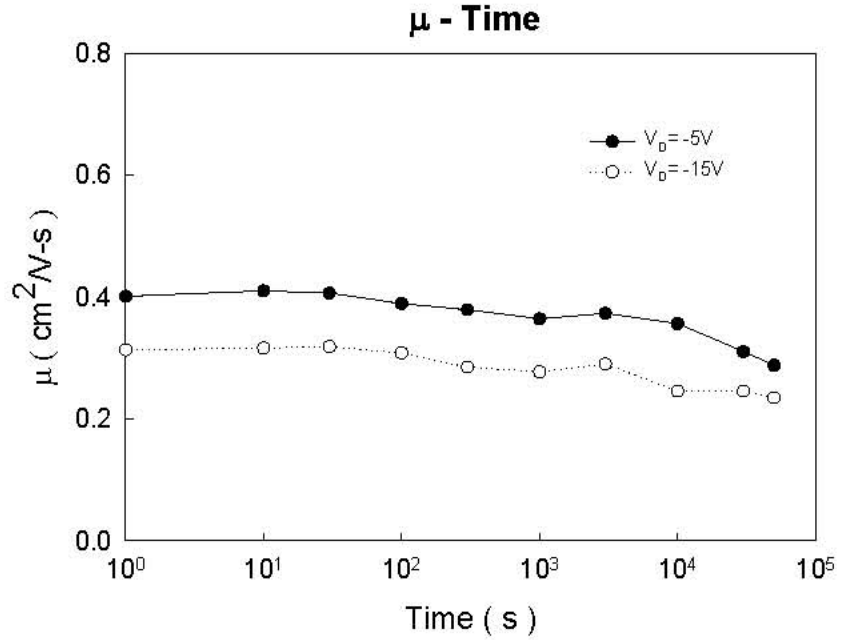
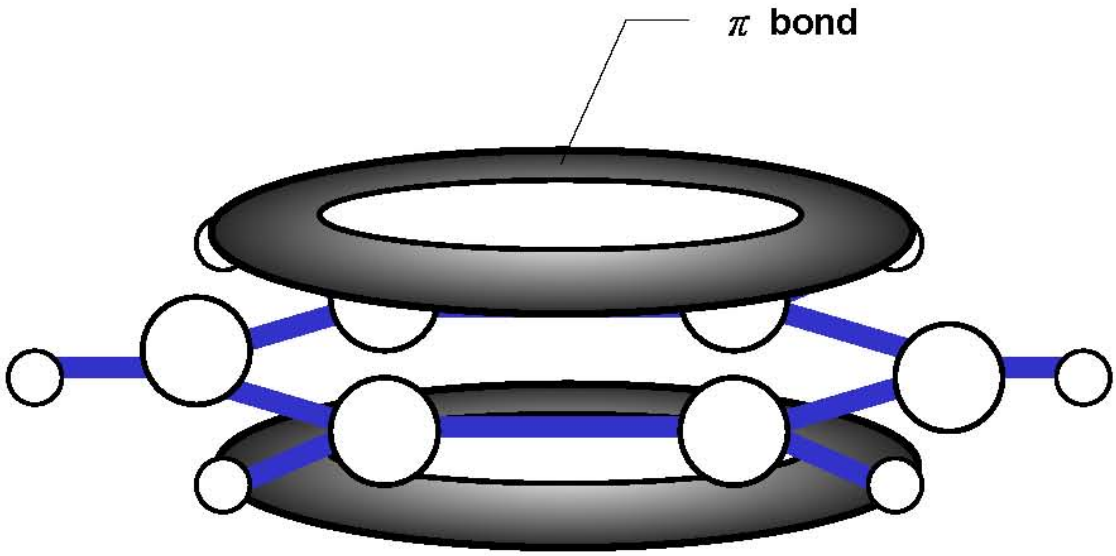
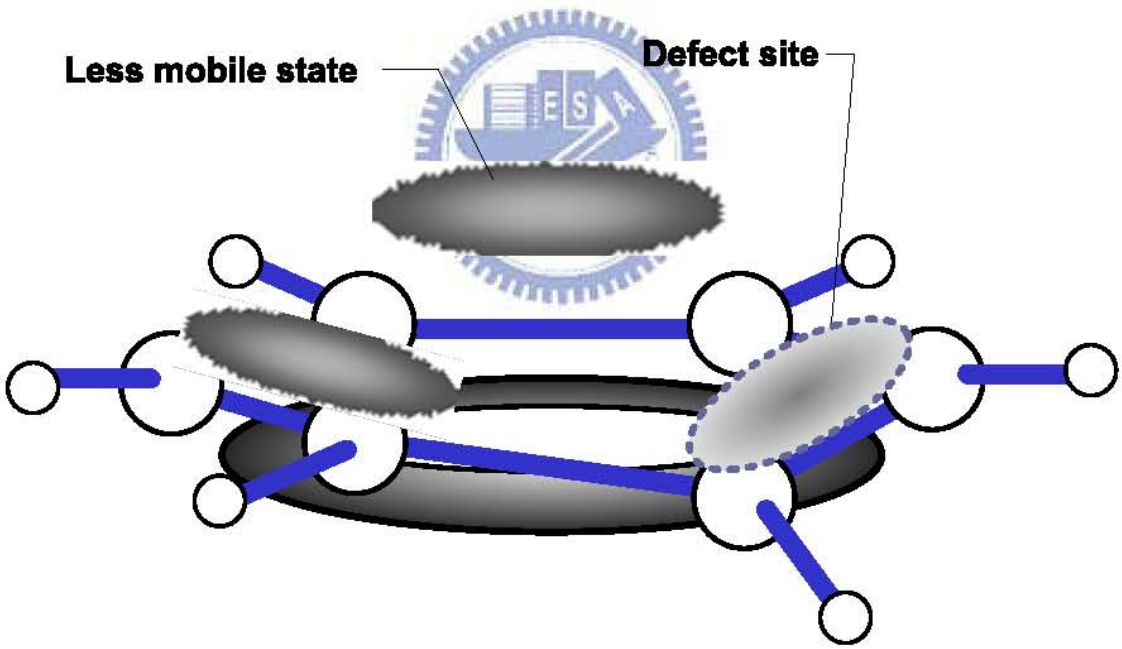



Figure 4-5: The linear and saturation mobility versus time under drain bias ($V_D$= -5V and -15V) taken after 0s, 10s, 1000s, 10000s, 30000s and 50000s current stress.




(a)




(b)

Figure 4-6: The structure of benzene in pentacene. Comparing the degradation of $\pi$ bond (a)before current stress, and (b)after current stress.

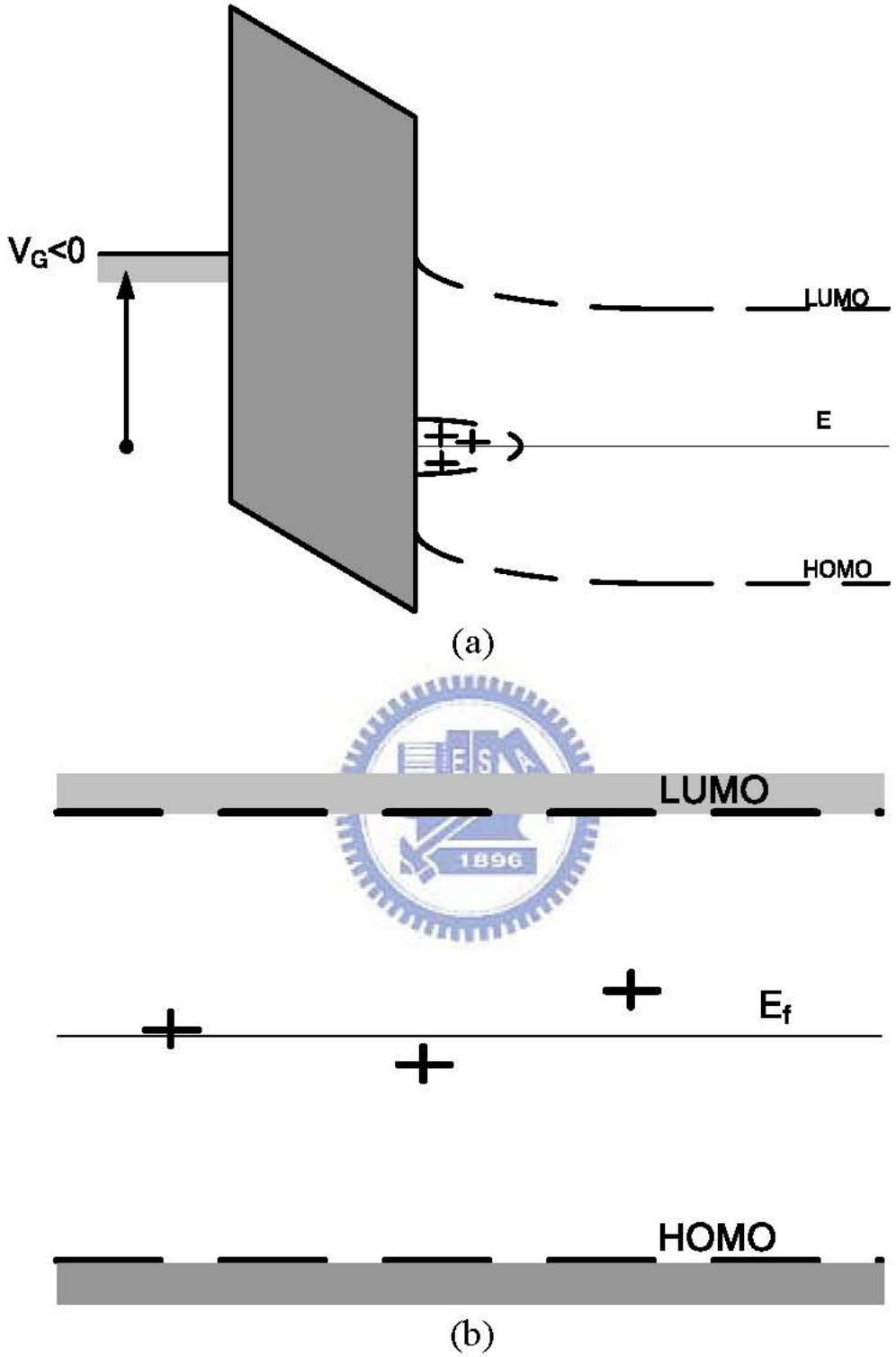
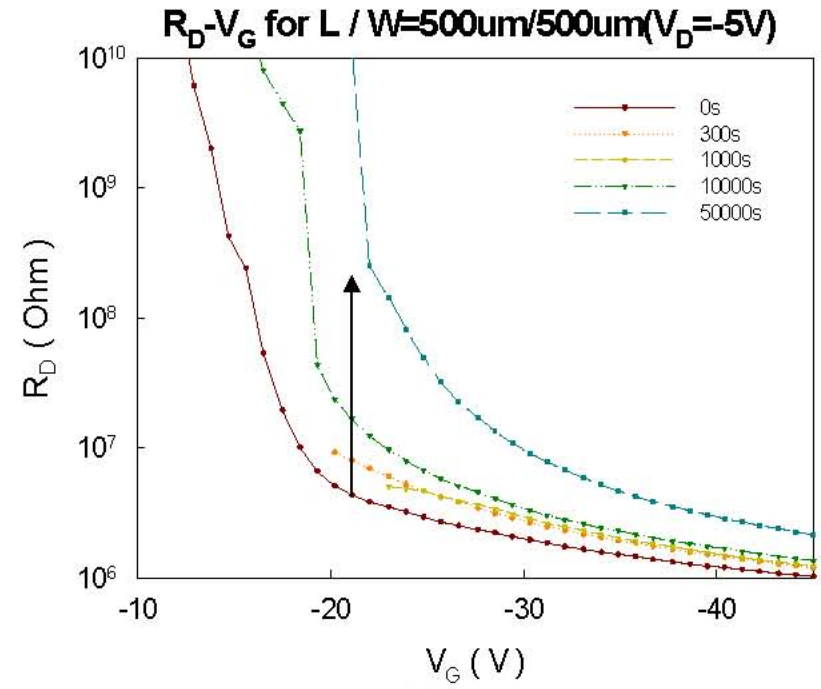
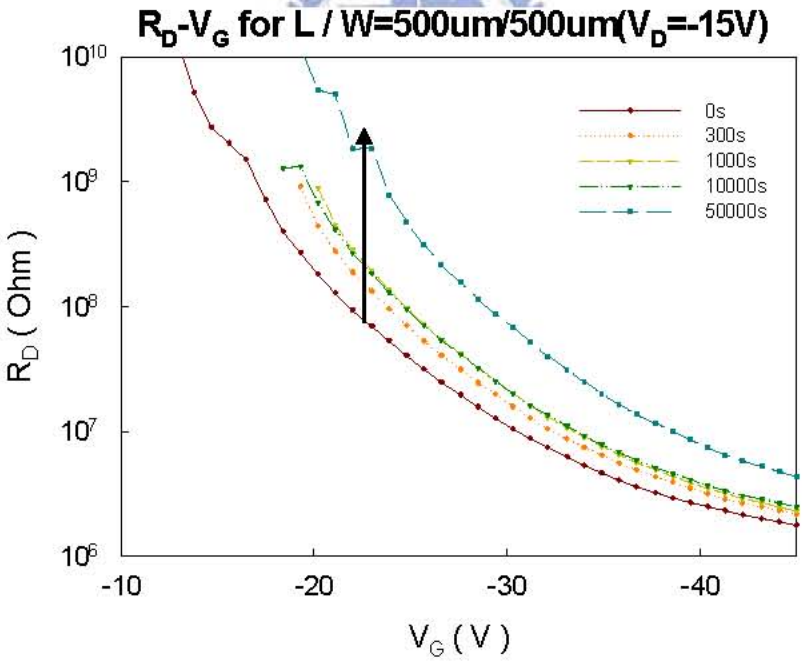



Figure 4-7: The energy band diagrams show the formation of the positive trapping charges between LUMO and HOMO. (a)The energy band diagram of a metal and a semiconductor with an oxide layer between them, and (b)the energy level of pentacene.

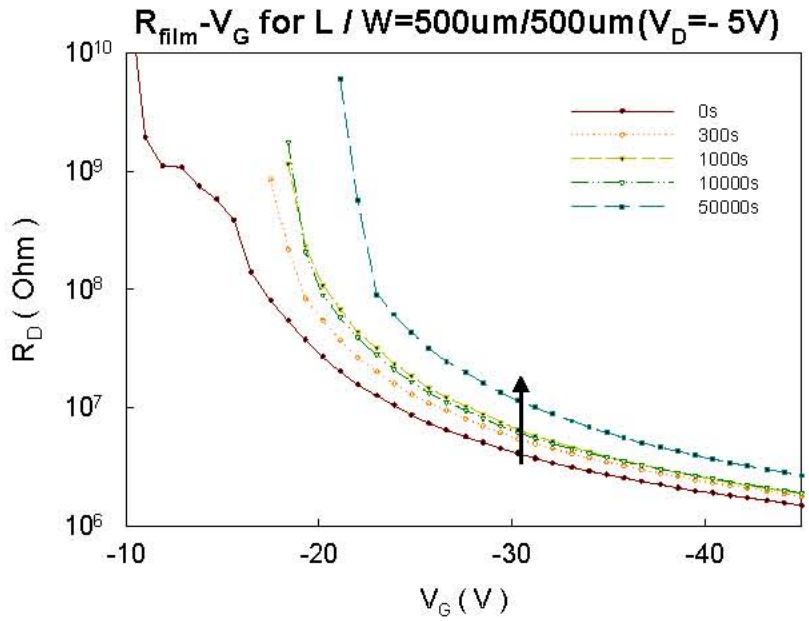



(a)




(b)

Figure 4-8: The resistance at drain side as a function of gate voltage under drain bias (a)$V_D$= -5V and (b)$V_D$= -15V taken after current stress of 0r, 10s, 1000s, 10000s, 30000s and 50000s.

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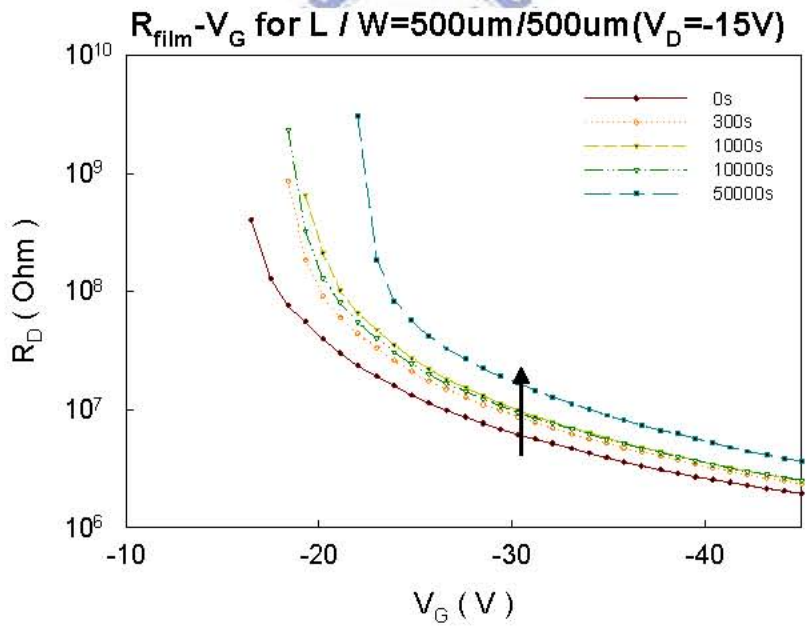
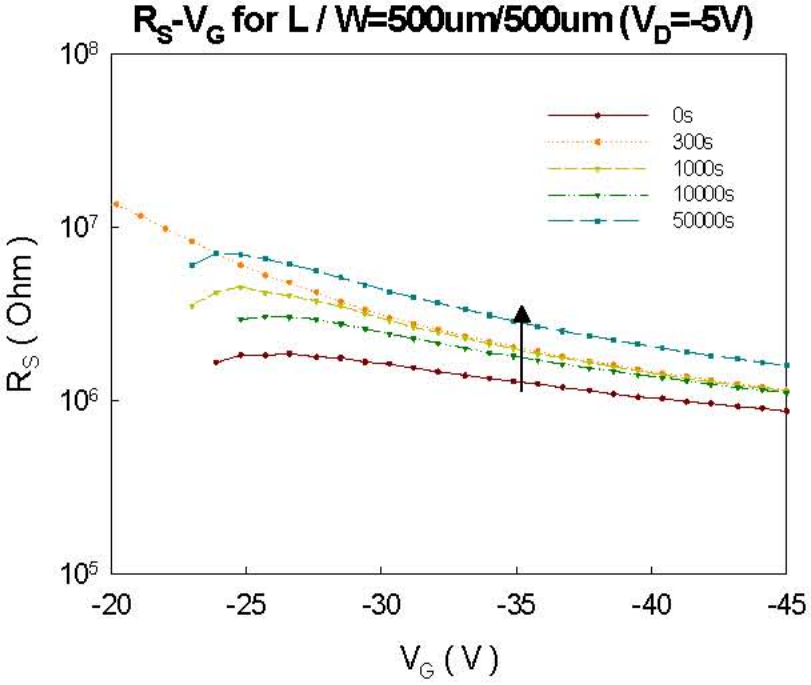
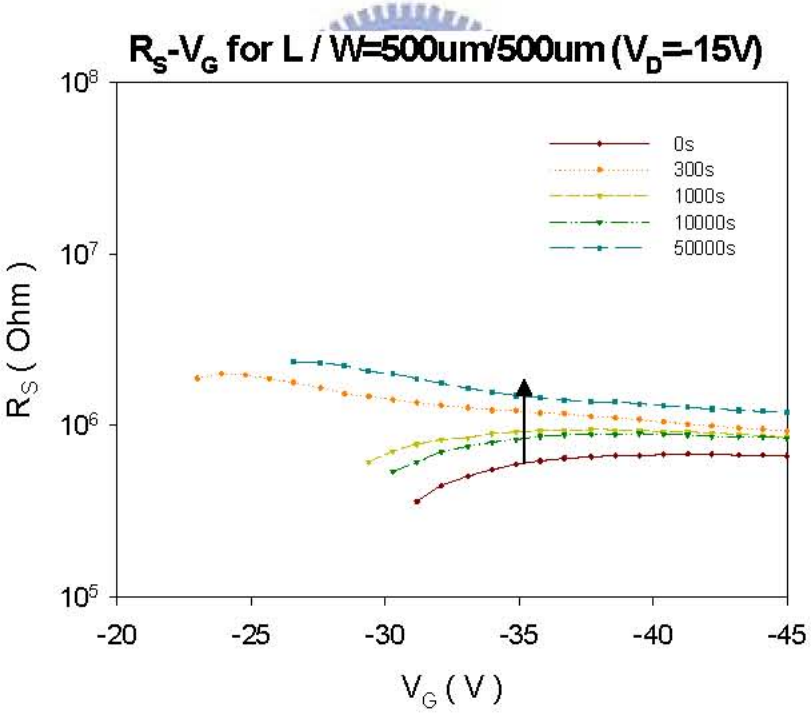



(b)

Figure 4-9: The resistance in channel as a function of gate voltage under drain bias (a)$V_D$= -5V and (b)$V_D$= -15V taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

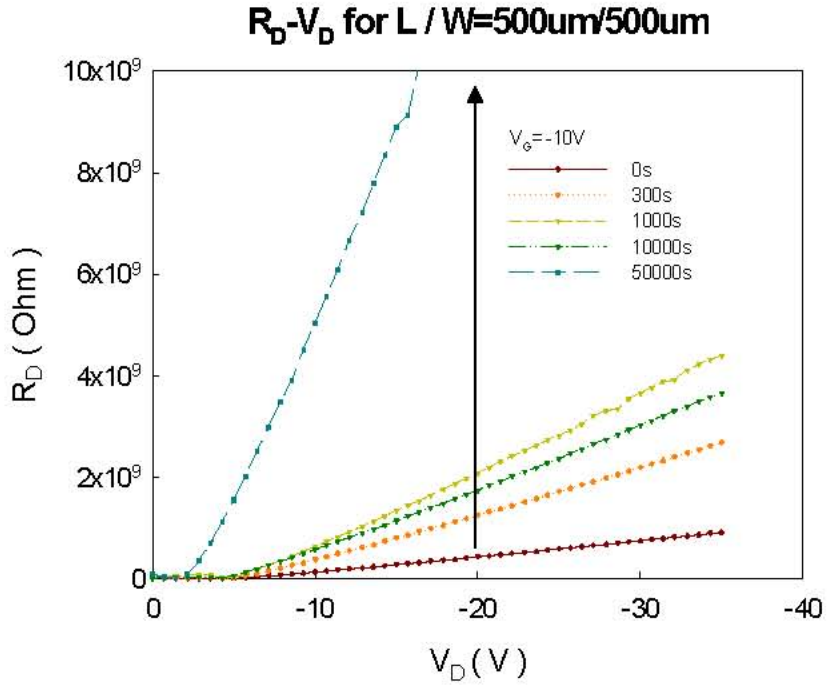



(a)




(b)

Figure 4-10: The resistance at source side as a function of gate voltage under drain bias (a)$V_D$= -5V and (b)$V_G$= -15V taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

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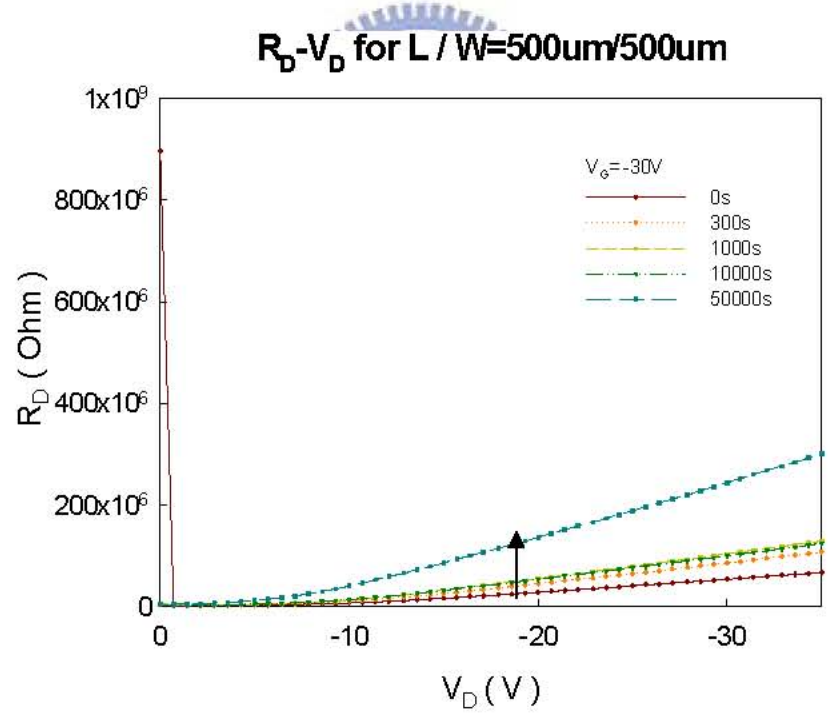
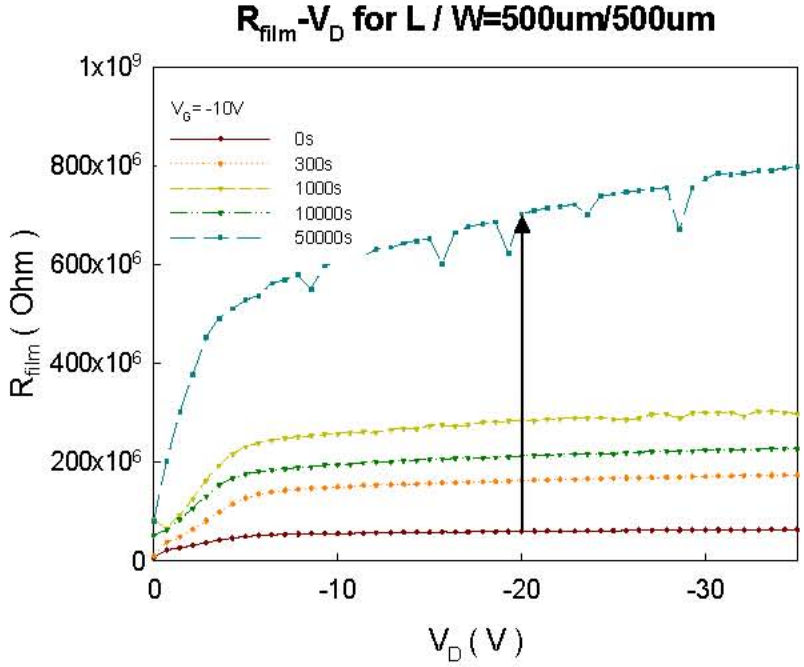
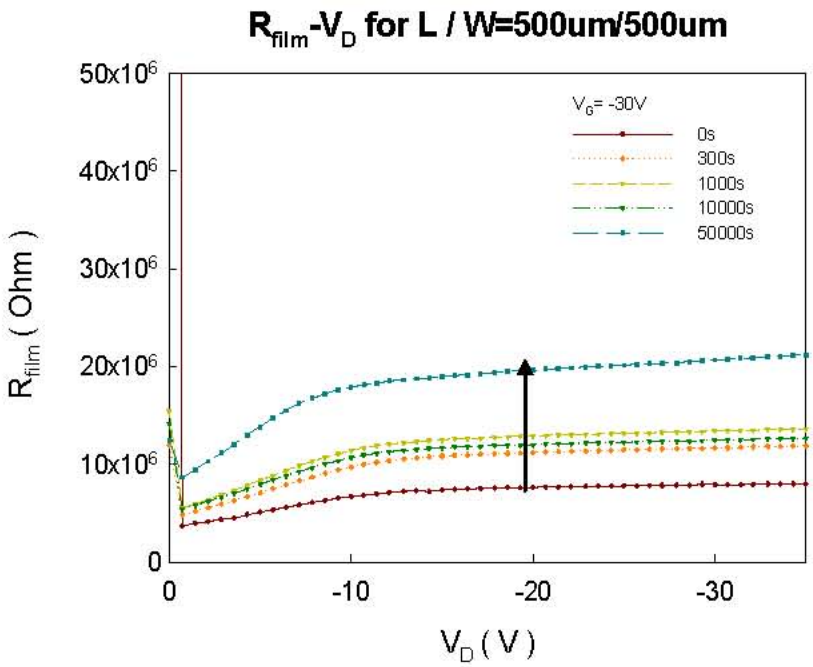



(b)

Figure 4-11: The resistance at drain side as a function of drain voltage under gate bias (a)$V_G$= -10V and (b)$V_G$= -30V taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

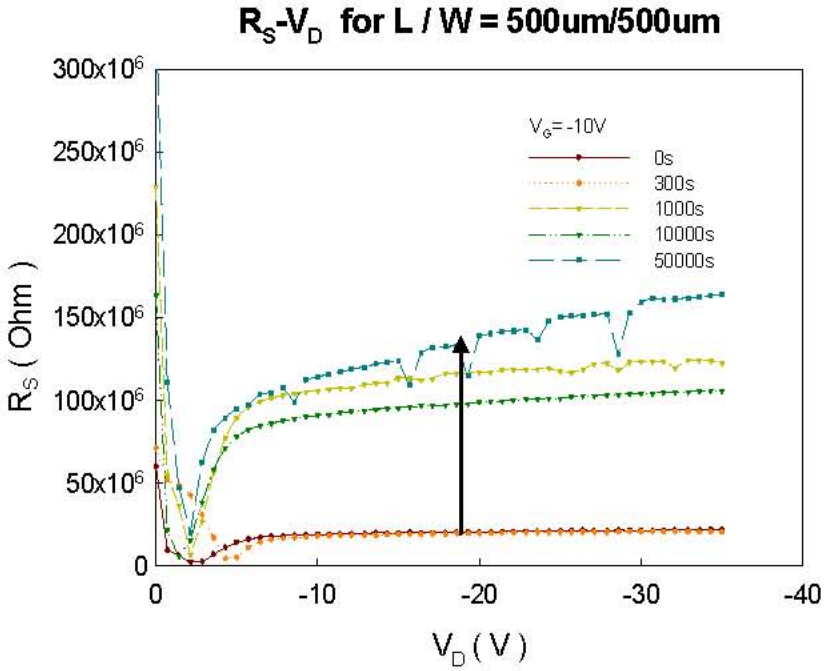



(a)

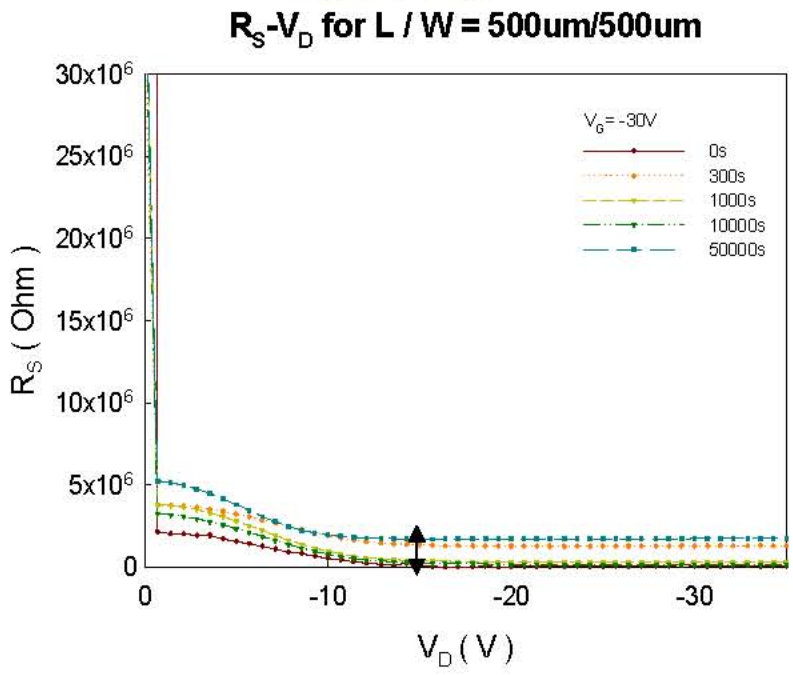



(b)

Figure 4-12: The resistance at drain side as a function of drain voltage under gate bias (a)$V_G$= -10V and (b)$V_G$= -30V taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

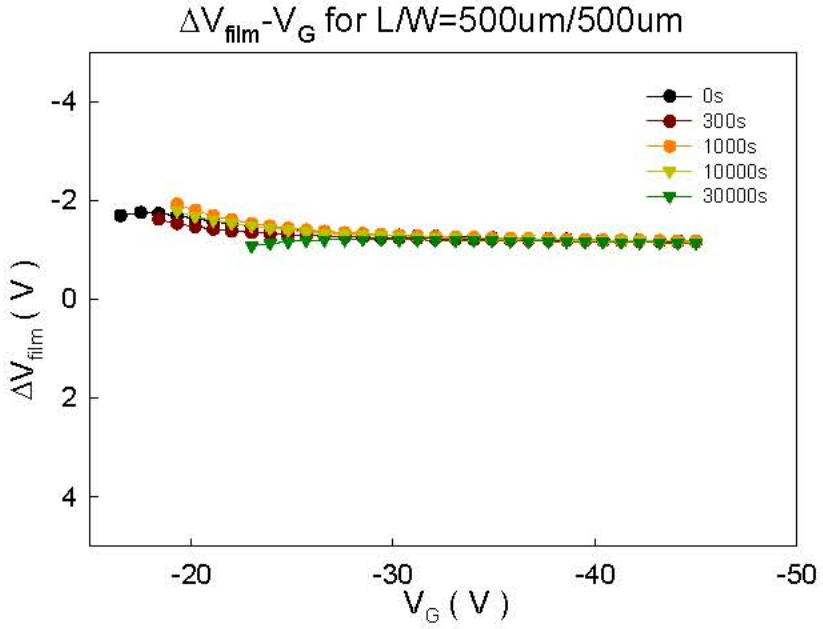



(a)



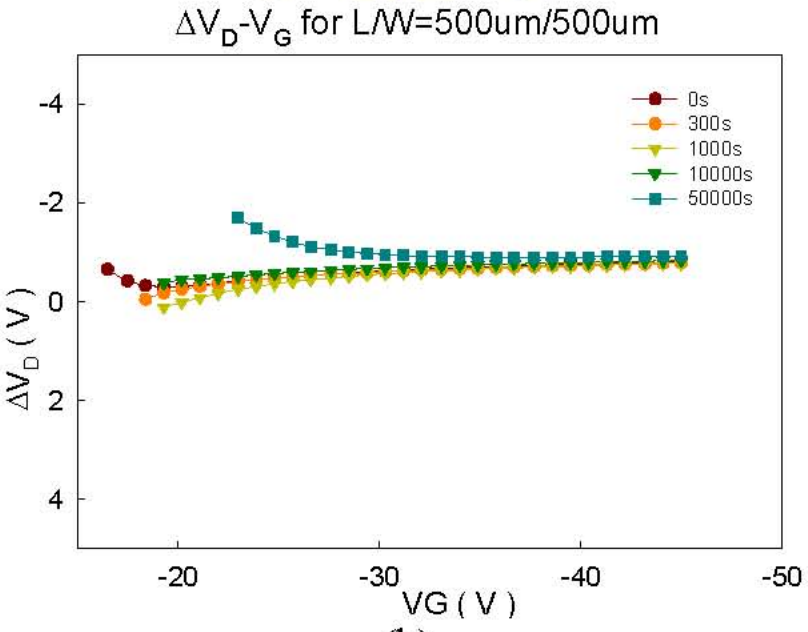

(b)

Figure 4-13: The resistance at source side as a function of drain voltage under gate bias (a)$V_G$= -10V and (b)$V_G$= -30V taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



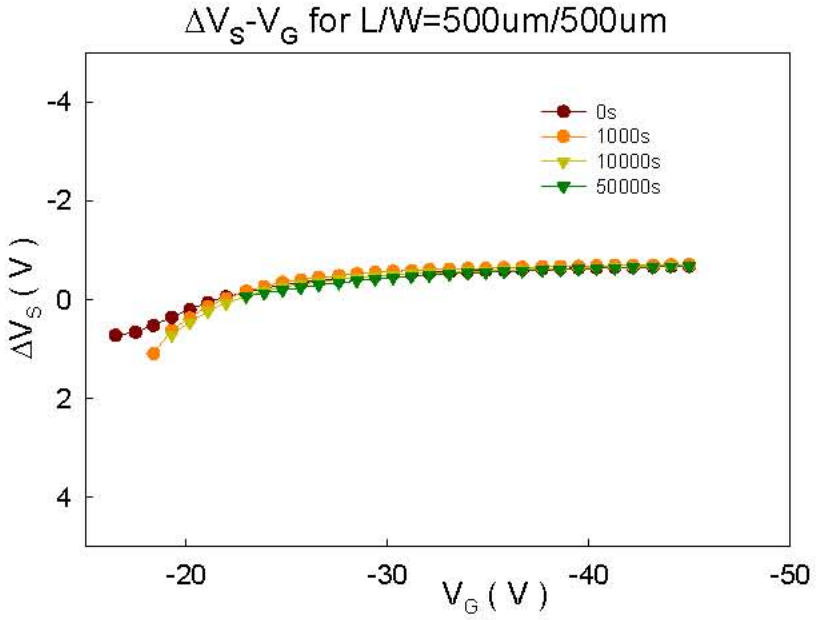

(a)

Figure 4-14: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side in linear region as a function of gate voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



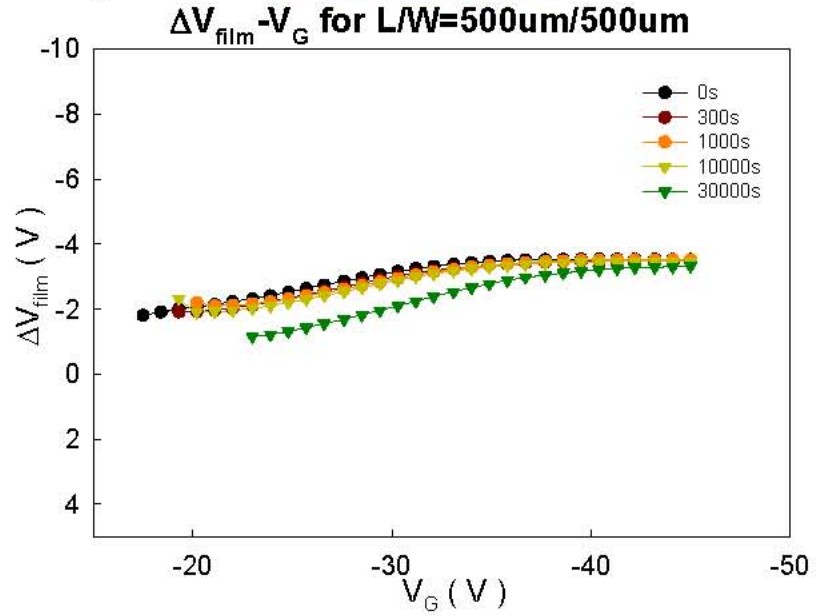

(b)

Figure 4-14: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side in linear region as a function of gate voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



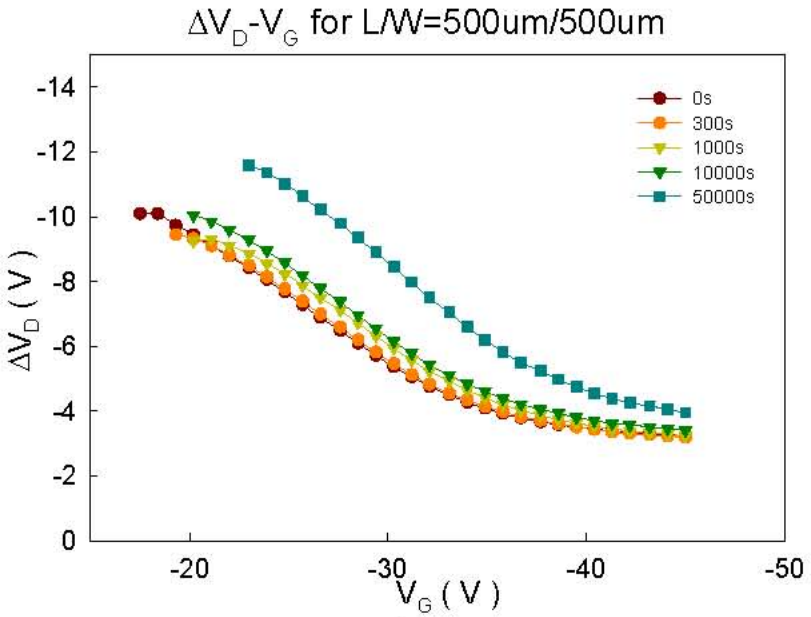

(c)

Figure 4-14: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side in linear region as a function of gate voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



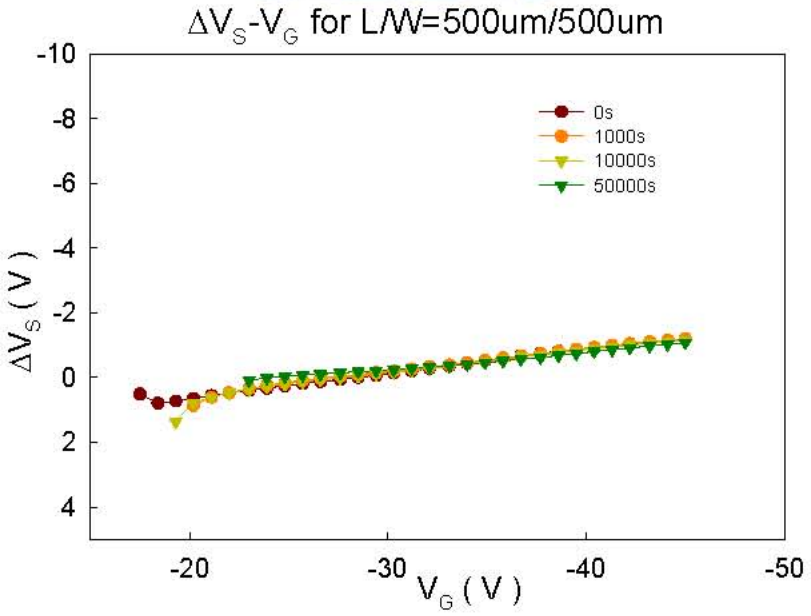

(a)

Figure 4-15: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side in saturation region as a function of gate voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



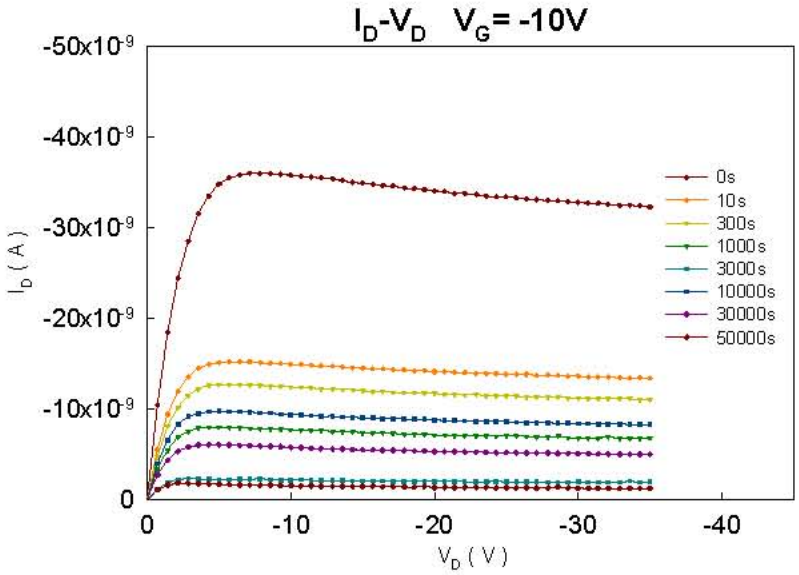

(b)

Figure 4-15: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side in saturation region as a function of gate voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

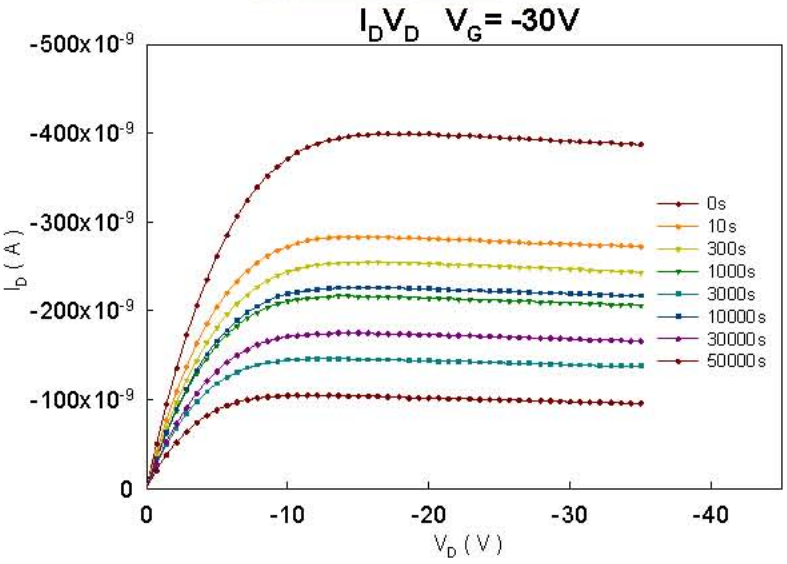



(c)

Figure 4-15: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side in saturation region as a function of gate voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

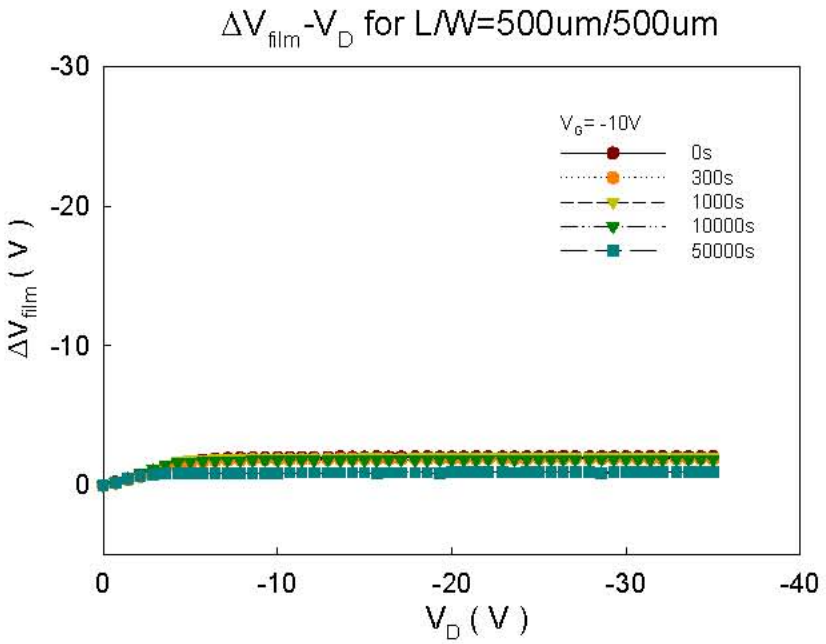



(a)



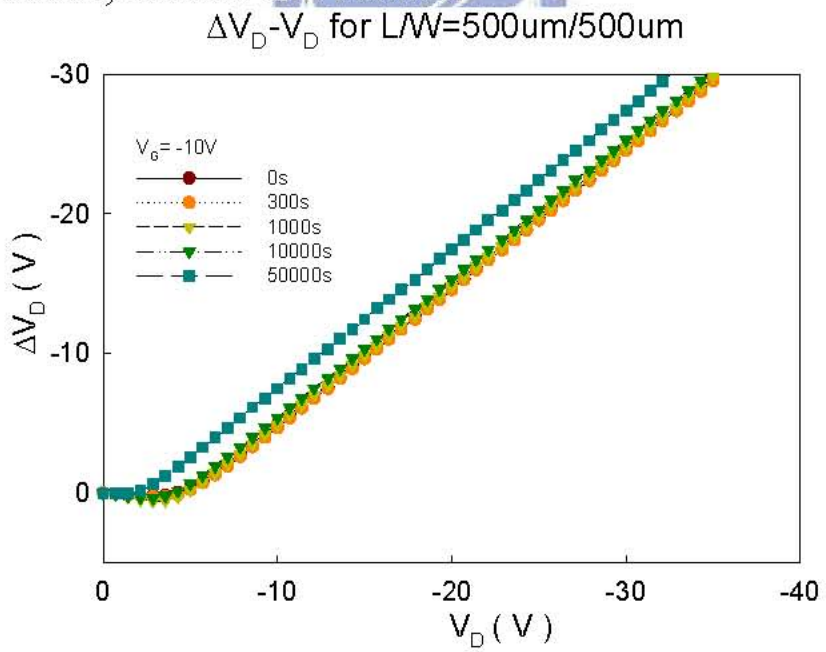

(b)

Figure 4-16: The output characteristics for pentacene-based OTFT with four probe structure (a) at $V_G$= -10V and (b) at $V_G$= -30V



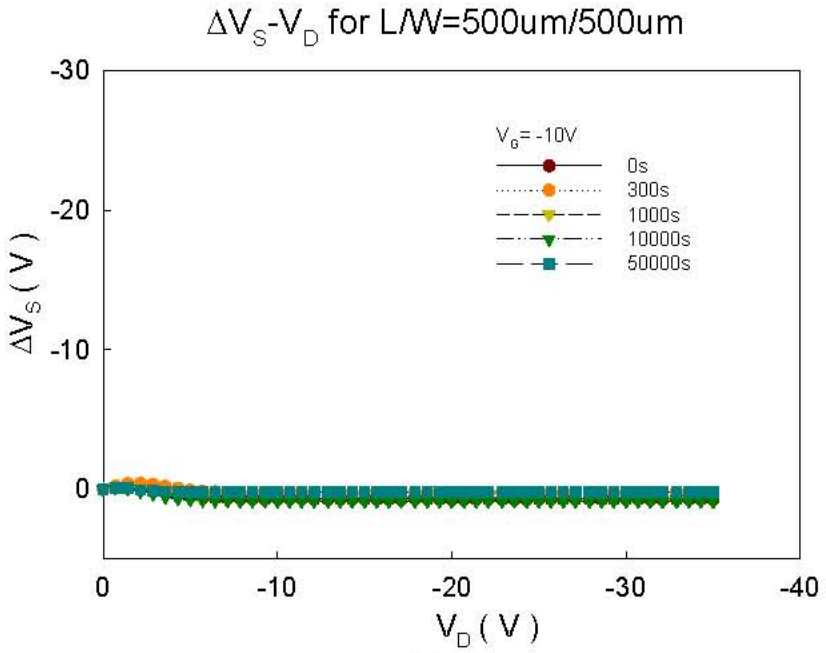

(a)

Figure 4-17: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side at gate bias ($V_G$= -10V) as a function of drain voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



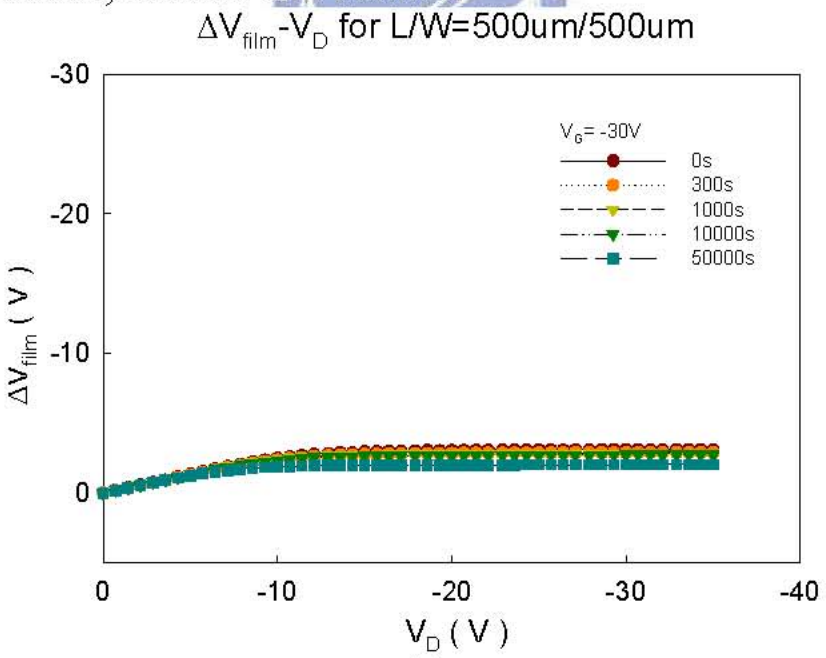

(b)

Figure 4-17: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side at gate bias ($V_G$= -10V) as a function of drain voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



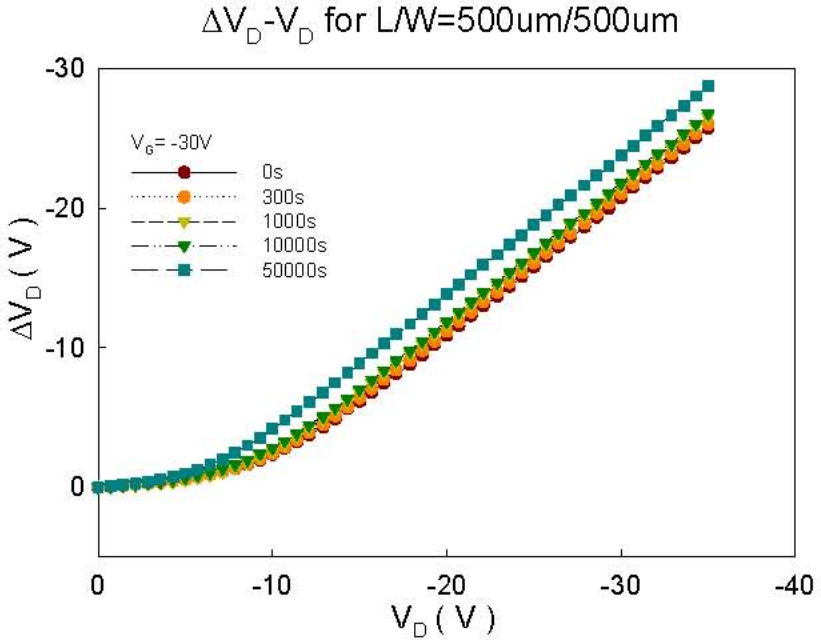

(c)

Figure 4-17: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side at gate bias ($V_G$= -10V) as a function of drain voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



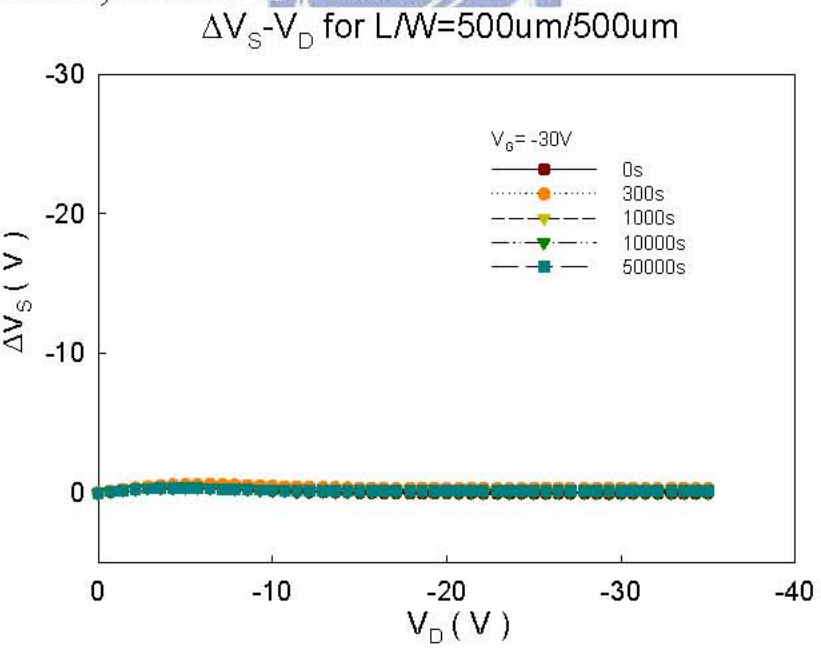

(a)

Figure 4-18: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side at gate bias ($V_G$= -30V) as a function of drain voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.



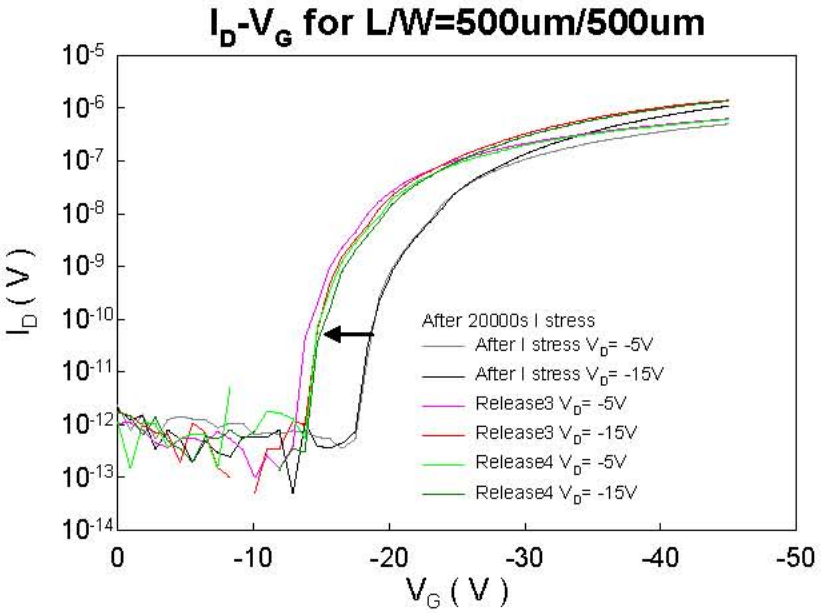

(b)

Figure 4-18: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side at gate bias ($V_G$= -30V) as a function of drain voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.

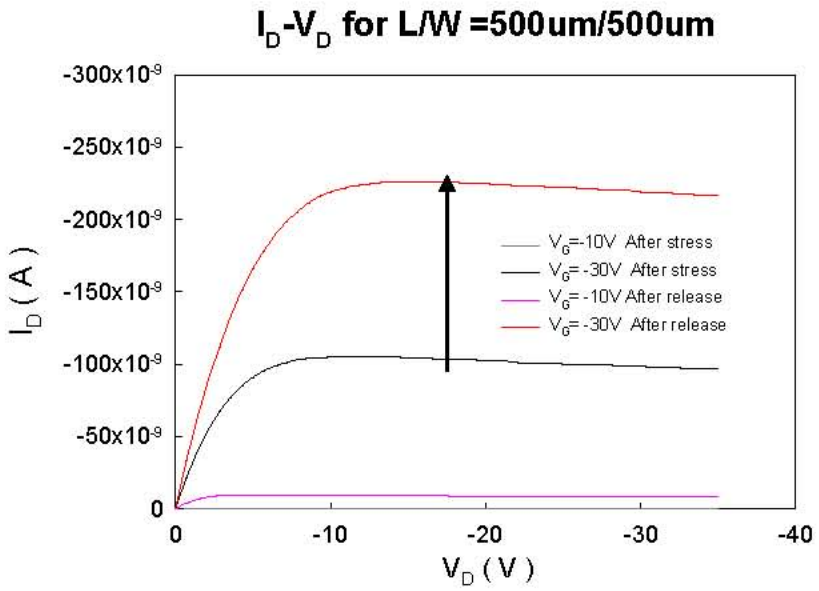



(c)

Figure 4-18: The voltage drop of (a)channel between probe1 and probe2, (b)drain side, and (c)source side at gate bias ($V_G$= -30V) as a function of drain voltage taken after current stress of 0s, 10s, 1000s, 10000s, 30000s and 50000s.




(a)




(b)

Figure 4-19: (a) The transfer characteristics of the device at drain voltages $V_D$= -5V and $V_D$= -15V, and (b)the output characteristics at gate voltage $V_G$= -10 and $V_G$= -30V, compared with after stress and after release.

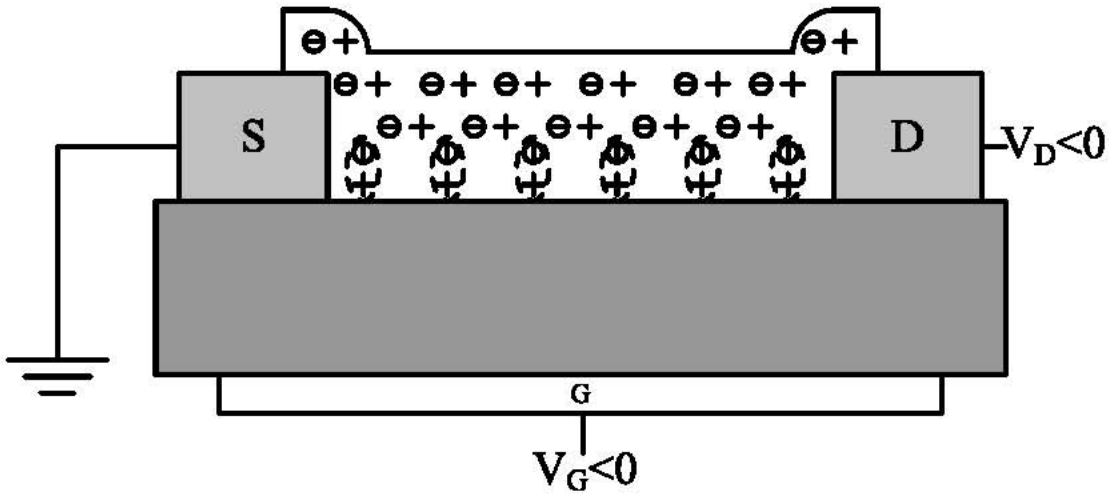



Figure 4-20: Schematic of organic field transistor, showing the formation of dipole during the current stress.

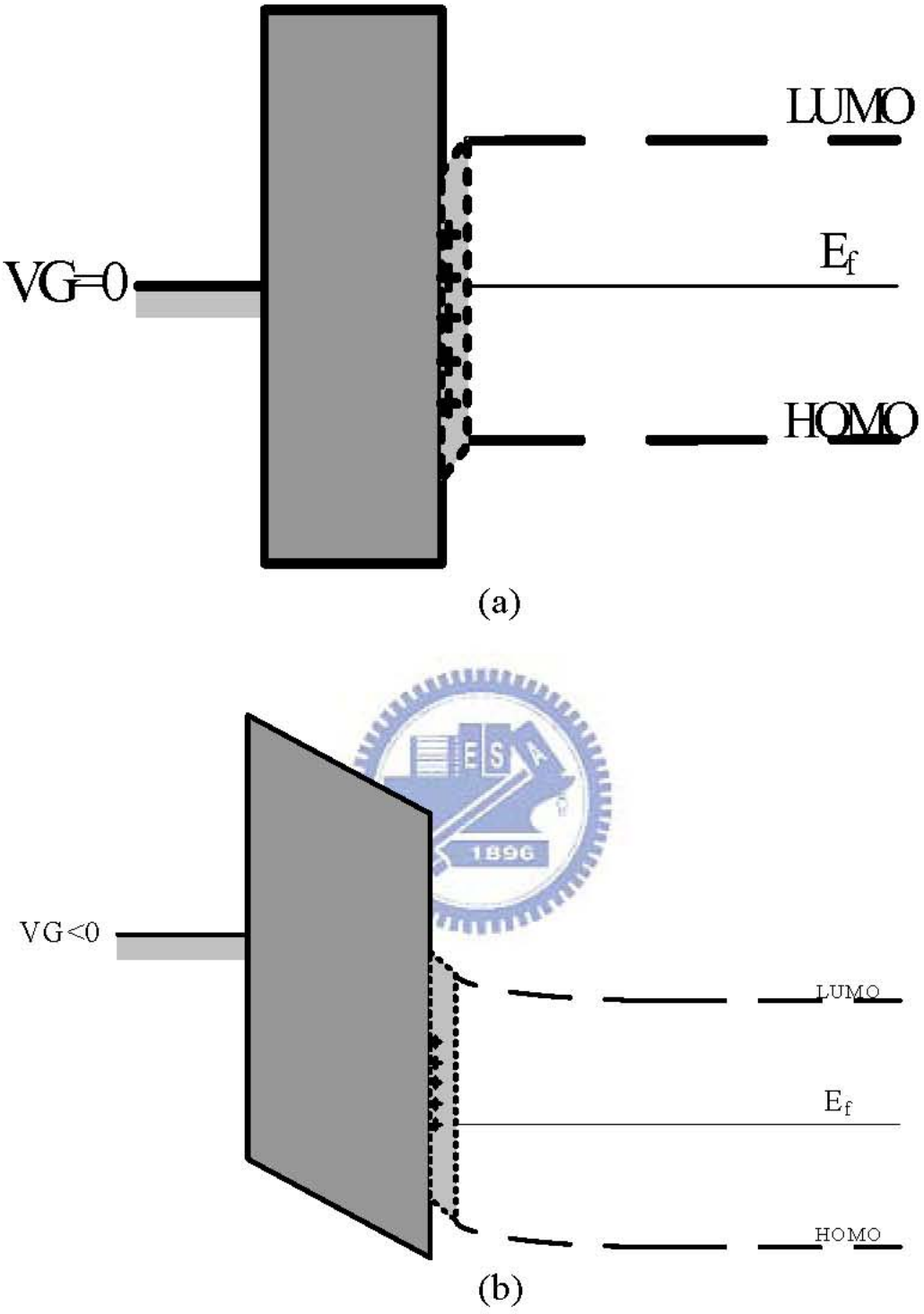



Figure 4-21: (a)The energy band diagram of flat band with the positive charges induced by dipoles, and (b)energy band diagram through the MIS structure with a positive gate bias. Smooth band bending due to the energy level of interface, pined down by the positive charges.

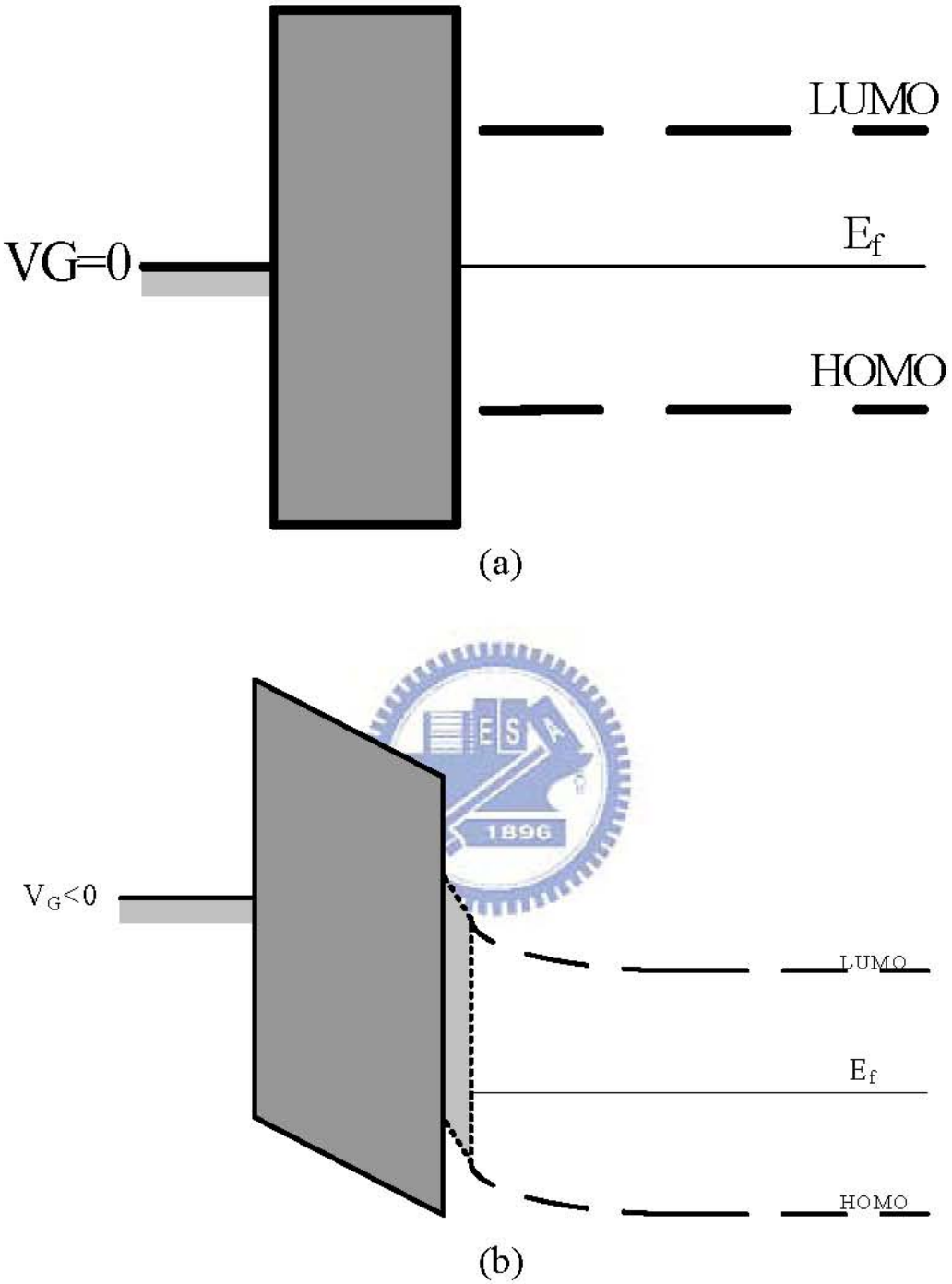
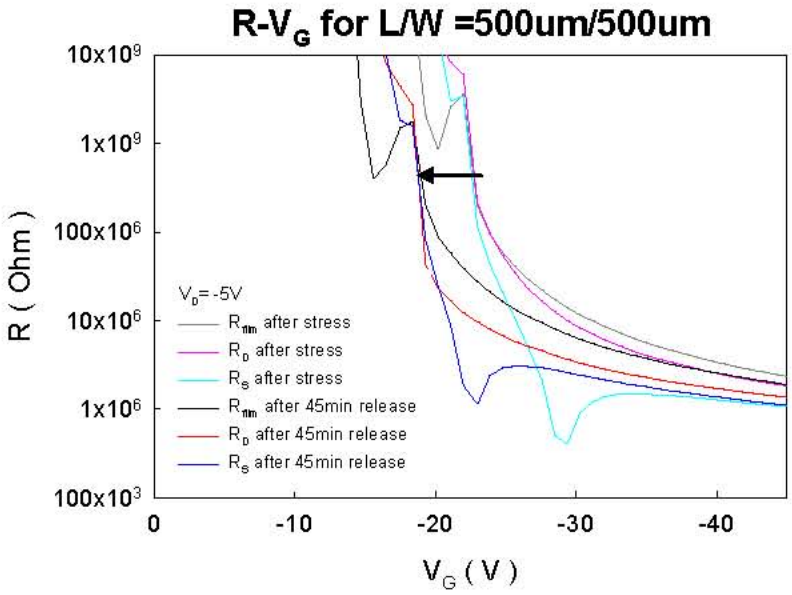
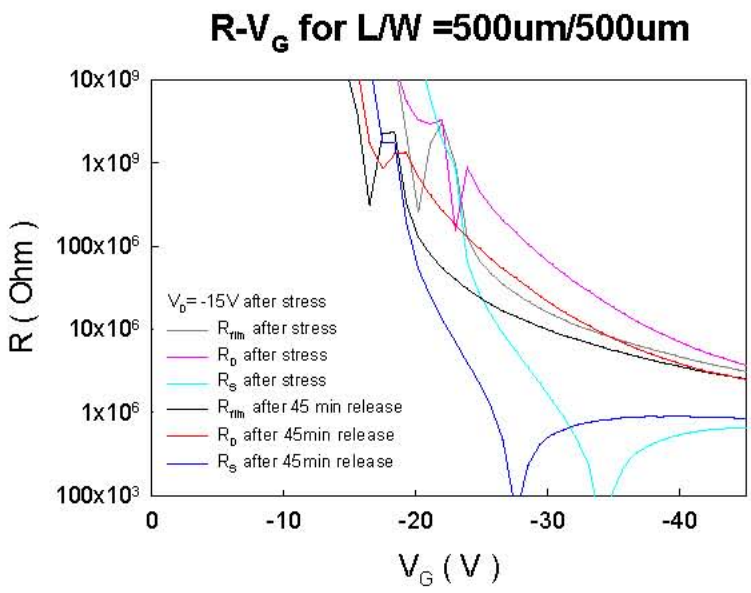



Figure 4-22: (a)The energy band diagram of flat band, and (b)energy band diagram through the MIS structure with a positive gate bias after its recovery. The band bending is more winding.

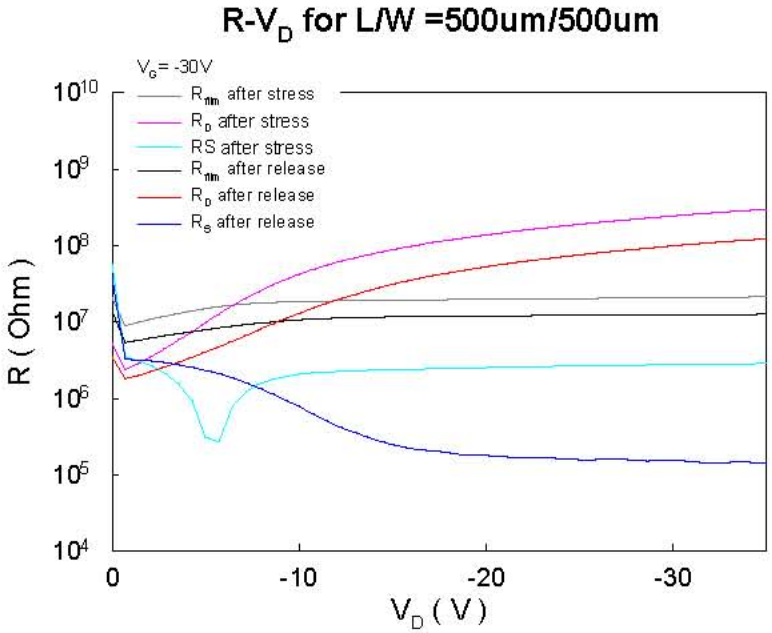



(a)

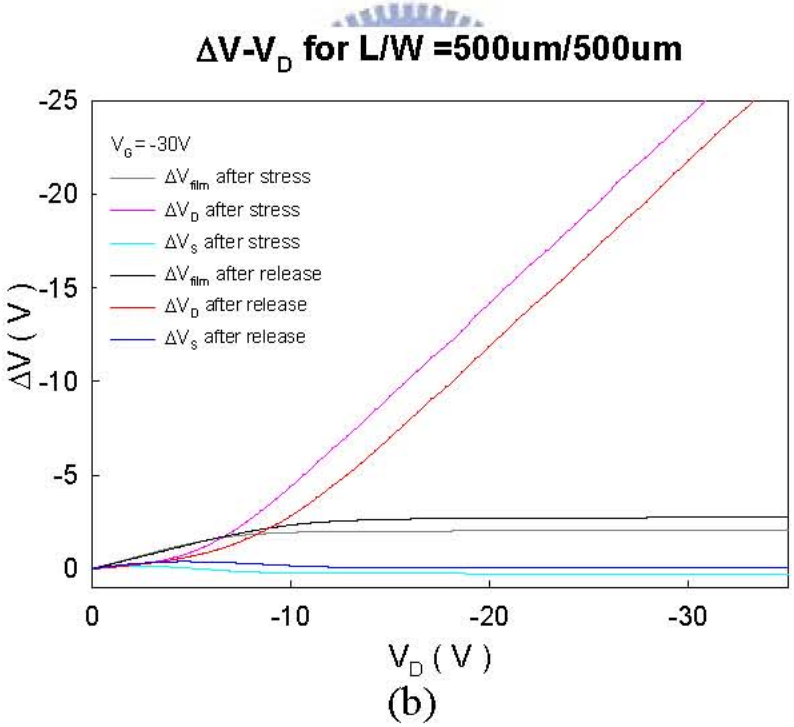



(b)

Figure 4-23: The resistances as a function of gate voltage under drain bias of (a)$V_D$= -5V and (b)$V_D$= -15V for drain side, source side ,and channel between probe1 and probe2. They after stress and after release would be compared.

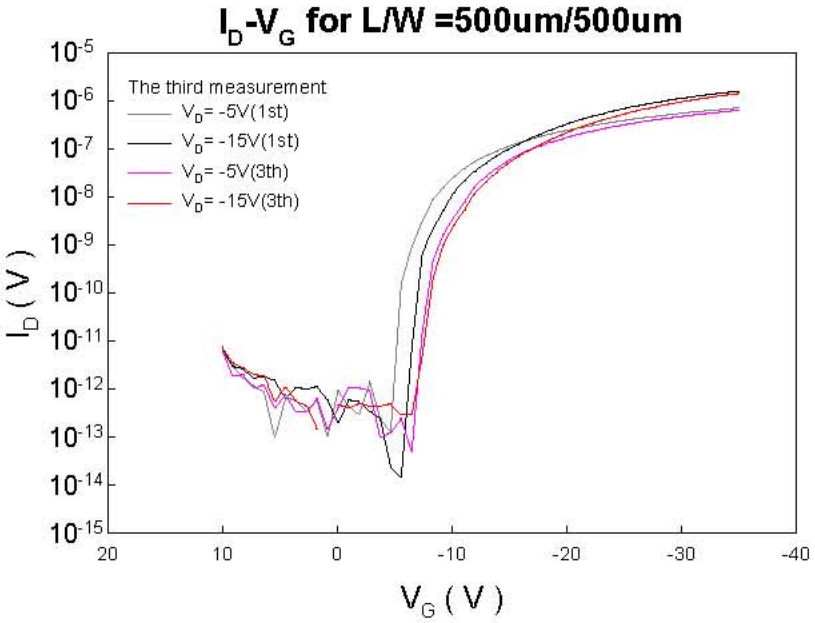



(a)

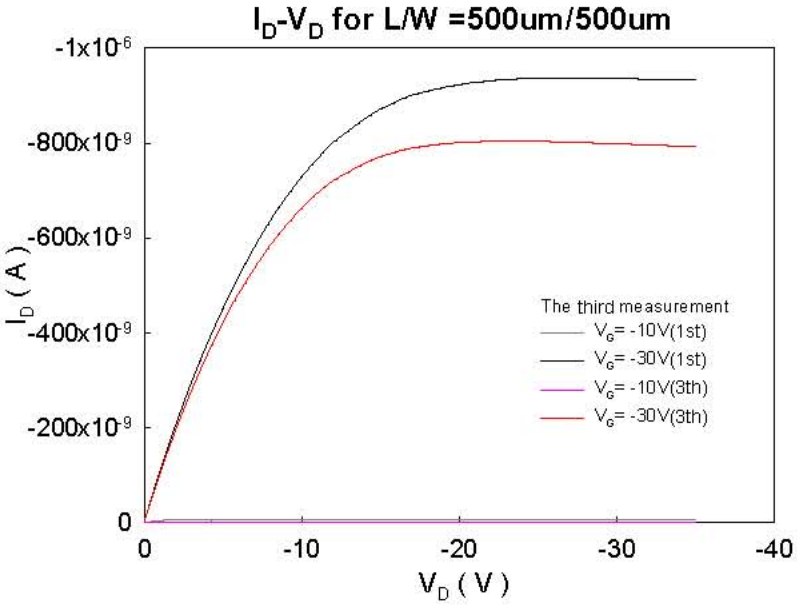



(b)

Figure 4-24: (a)The resistances as a function of drain voltage under gate bias ($V_G$= -30V) for drain side, source side and channel between probe1 and probe2. (b)The voltage drop of channel between probe1 and probe2, drain side, and source side as a function of drain voltage. They after stress and release would be compared.

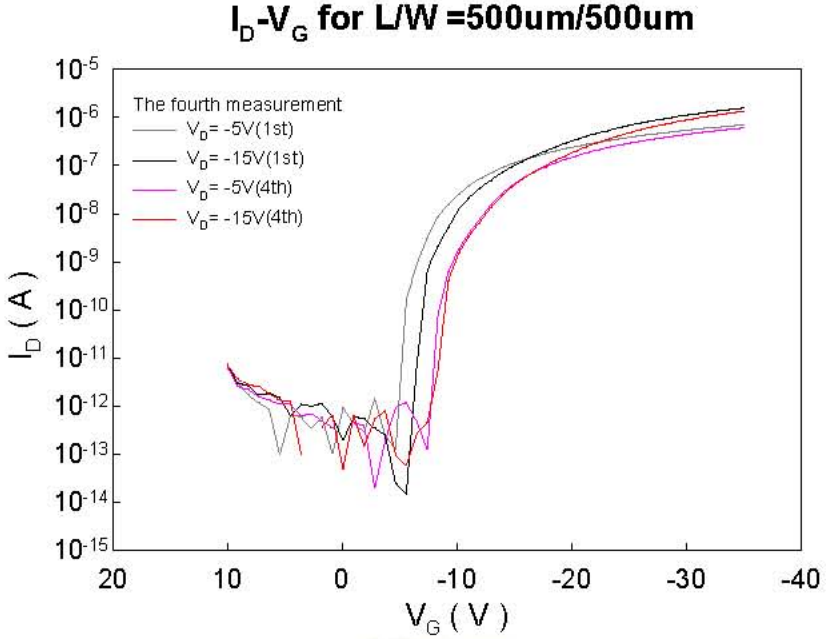



(a)

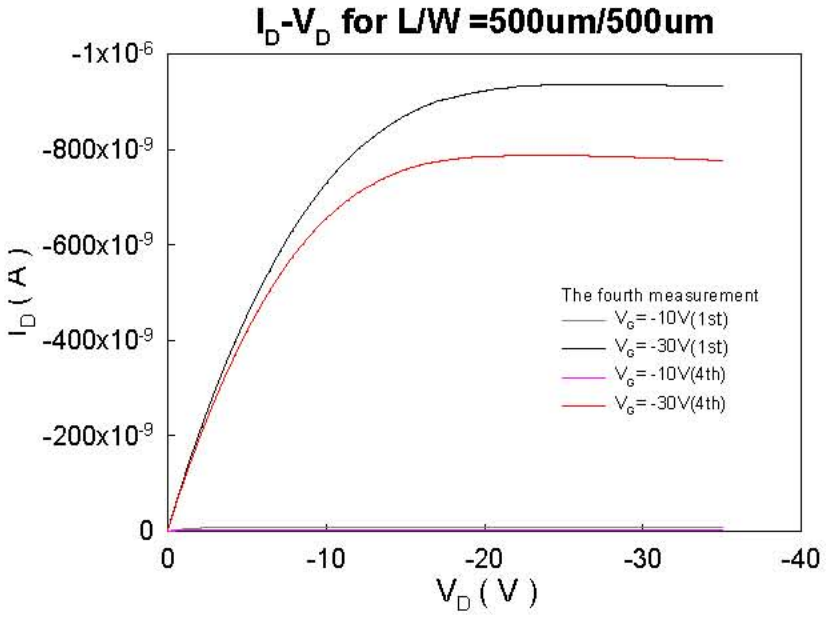



(b)

Figure 4-25: Comparison with (a)the transfer curve, and (b)the output characteristic for the first and third measurement. At the same time, comparison with (c)the transfer curve, and (d)the output characteristic for the first and fourth measurement. (continue)




(c)




(d)

Figure 4-25: Comparison with (a)the transfer curve, and (b)the output characteristic for the first and third measurement. At the same time,comparison with (c)the transfer curve, and (d)the output characteristic for the first and fourth measurement.

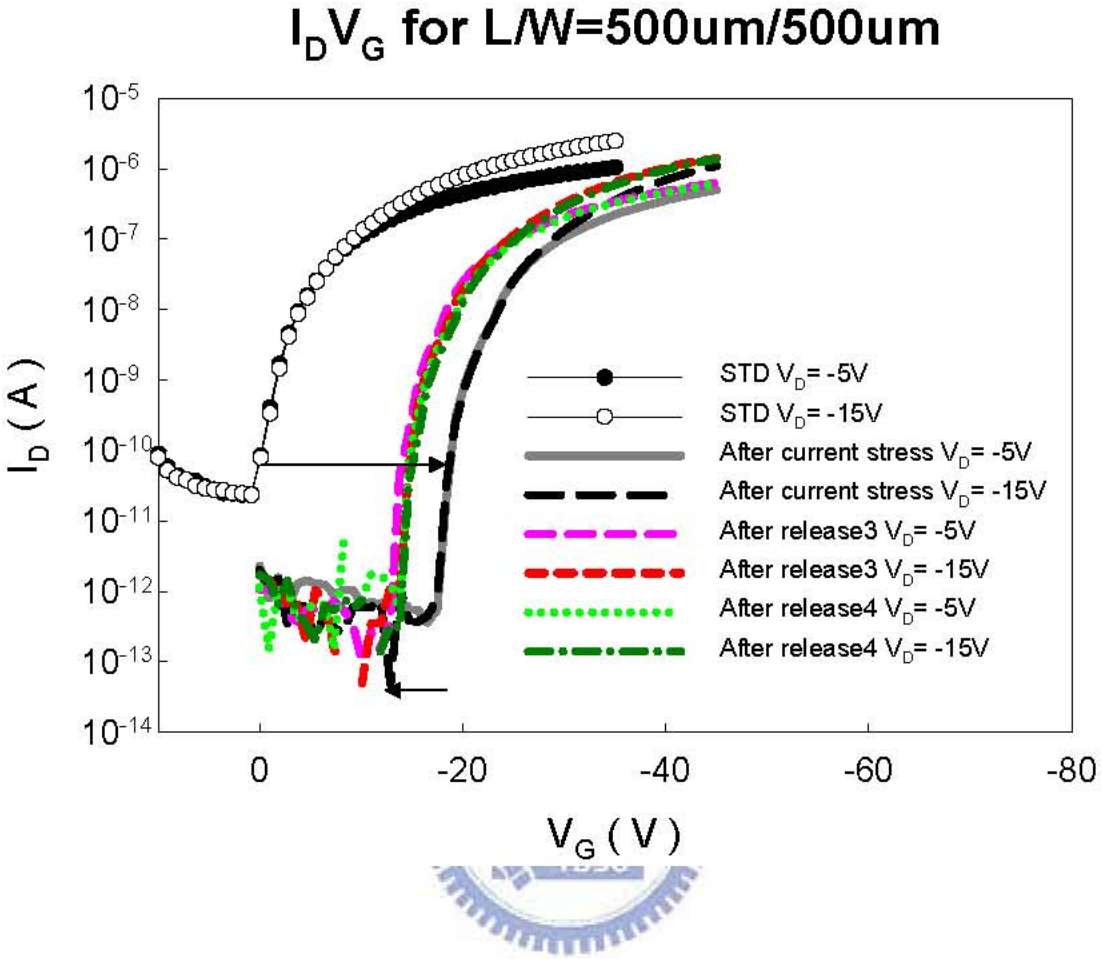



Figure 4-26: The summary for threshold voltage shift after stress and release.

Table 4-1: Threshold voltage shift during current stress

| $I_D$= -2x10$^{-7}$A<br>$V_G$= -20V | L=500($\mu$m)<br>W=500($\mu$m) | |
|---|---|---|
| Time<br>(s) | $V_{th}$(lin)<br>(V) | $V_{th}$(sat)<br>(V) |
| 1 | 0.401 | 0.313 |
| 10 | 0.41 | 0.316 |
| 30 | 0.406 | 0.3185 |
| 100 | 0.389 | 0.308 |
| 300 | 0.3789 | 0.2849 |
| 1000 | 0.364 | 0.277 |
| 3000 | 0.373 | 0.29 |
| 10000 | 0.356 | 0.2453 |
| 30000 | 0.3101 | 0.2453 |
| 50000 | 0.2877 | 0.2347 |

Table 4-2: Instability of mobility during current stress

| $I_D$= -2x10$^{-7}$A<br>$V_G$= -20V | L=500($\mu$m)<br>W=500($\mu$m) | |
|---|---|---|
| Time<br>(s) | $\mu$(lin)<br>(cm$^2$/Vs) | $\mu$(sat)<br>(cm$^2$/Vs) |
| 1 | -19.63 | -15.14 |
| 10 | -21.49 | -17.62 |
| 300 | -21.99 | -17.143 |
| 1000 | -22.31 | -18.235 |
| 3000 | -23.321 | -20.122 |
| 10000 | -23.072 | -17.842 |
| 30000 | -23.924 | -18.508 |
| 50000 | -25.492 | -21.03 |

Table 4-3: Instability of subthreshold swing during current stress

| $I_D$= -2x10$^{-7}$A<br>$V_G$= -20V | L=500($\mu$m)<br>W=500($\mu$m) | |
|---|---|---|
| Time (s) | s.s.(lin) (V/decade) | s.s.(sat) (V/decade) |
| 1 | 1.4640 | 1.1960 |
| 10 | 1.4300 | 1.1980 |
| 30 | 0.8360 | 0.9060 |
| 100 | 1.3860 | 0.9670 |
| 300 | 1.2770 | 1.0620 |
| 1000 | 1.0570 | 1.5570 |
| 3000 | 1.3370 | 1.4830 |
| 10000 | 1.4500 | 1.3430 |
| 30000 | 0.9820 | 1.4850 |
| 50000 | 1.0300 | 1.2710 |

Table 4-4: Transient stress phenomenon

| | L=500($\mu$m)<br>W=500($\mu$m) | |
|---|---|---|
| Times | $\mu$(sat) (cm$^2$/Vs) | $V_{th}$(sat) (V) |
| first | 0.324 | -8.263 |
| third | 0.327 | -10.303 |
| fourth | 0.327 | -10.981 |

# Chapter 5

# Conclusions and Further Recommendations

## 5.1 Conclusions

The pentacene-based OTFT with four probe structure were fabricated. We study on the physical and electrical characteristics of OTFT, including of material analysis, four probe measurement, conduction mechanism and electrical instability. They are concluded in the folling.

The pentacene crystallization as a continuous film is influenced by substrate temperature, morphology and the difference phase. Although many approaches were proposed to enhance pentacene grain growth, however, larger poly grains do not mean better electrical properties. In material, a single phase of pentacene crystal is preferred for carrier transport due to the lack of interference between two kinds of orientation of pentacene molecules.

The four probe structure are proposed to analyze the voltage drop and the resistance for devices. The voltage drops are further discussed and the increasing carrier concentration with the rising gate voltage attributed to the reduced resistances. In four probe measurements, we can further understand more information of an operating device. The higher substrate temperature not only improves the thin film growth, but also helps the connection of the contact between metal and semiconductor.

As expected for OTFTs, the extracted mobility decreases at the shorter channel length

device. This is due to a large drain-source voltage drop at source/drain series resistance in comparison to the channel resistance for a shorter channel-length OTFT (the channel resistance is smaller); this results in a lower extracted mobility. For a longer channel-length OTFT, e.g., L=1000um, the channel resistance is much larger than source/drain series resistances, and the extracted mobility approaches its intrinsic mobility value (1.17 cm /Vs). In addition, mobility is also sensitive to width. We can find that the narrower width is significantly affected by the border effect. The additional current at the edge of active area would be an important portion of drain current as the width decreases. Hence, the extracted mobility increases at the narrower channel width device and should be modified. The normalized resistances reduce due to addition drain current, too.

We properly use the multiple trapping and release model to explain the thermally activated phenomenon for the variable temperature measurement. The Arrhenius relationship illustrates the activated nature of mobility for electrical transport, using a transconductance. There is a Meyer–Neldel relationship between the activation energy and the prefactor with a Meyer–Neldel energy of 30.03 meV, which corresponds well with the isokinetic temperature of 348.48 K. Therefore, the carriers with exponential distribution of trap states in pentacene is affected by thermal activation. Samples with the higher temperature during measurements were observed to have better mobility, higher on-current and lower resistance, which agrees well with the multiple trapping and release model proposed to explain the conduction mechanism in small molecule OTFTs.

The electric reliability of pentacene-based OTFTs is tested. We understand the

instability of electrical characteristics in a continued series measurements and investigated the characteristics of bottom-contact pentacene-based OTFTs under drain current stress conditions. The field-effect mobility, subthreshold swing and threshold voltage were extracted to analysis the phenomenon and the obvious variation from current stress is the shift in threshold voltage. After sample had released, the reversible threshold voltage was observed. Reports of instabilities in OTFTs have been rare. However, Knipp et al. concluded that gate bias induced structural changes in the pentacene film produced trap states, which led to the threshold voltage shift. Here, we also think that polarization phenomenon play an important role during stress. The dipole built-in field is originated from the pentacene film due to the applied field. Thus we provide the rough energy band figure to depict these special properties of OTFTs. The studies of the transport and trapping charges are discussed. However, more practical issues have to be taken into accountant. The influence of the atmosphere ( i. e. water and oxygen ) around the organic TFT should be concerned at the same time.

## 5.2 Further Recommendations

From the investigation in this thesis, we provide some further recommendations for future studies.

**Passivation**

The OTFT affected by moisture is well known and lead to the degradation of device. Thus, when we fabricate our device, time is an important factor. When the

samples keep the proper electrical performance, we must soon take measurements in order to get ride of interference from degradation. The data must be chosen from measurements for many times. It is unfortunate that there are many passivation methods provided but the performance is not better. It will be a big problem for OTFT to develop a proper passivation to avoid the degradation.

**The effect of contact resistance**

As we know, the organic and metal contact is shottky contact. It depends on the fabrication condition and the interface with different material. It is always an obstacle to further analysis in this thesis. The uncertainty for interface between petacene and metal would lead to a challenge to investigation on the property of OTFT. The practical conditions are still under study to date.

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## Publications

五環素有機薄膜電晶體可靠度之研究

**Study on the Reliability of Pentacene-Based Organic Thin Film Transistor**