Chapter 1

Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are widely investigated, have drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1], and organic light-emitting displays (OLEDs)[2]. Except large area displays, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs) [3], static random access memories(SRAMs) , electrical programming read only memories(EPROM) [4], electrical erasable programming read only memories (EEPROMs) [5], linear image sensors[6], photo-detector amplifier [7]. Lately, some superior performances of poly-Si TFTs also have been reported by scaling down device dimension or utilizing novel crystallization technologies to enhance poly-Si film quality [8-9]. This provides the opportunity of using poly-Si TFTs into three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary trend, leading to rapid developing of poly-Si TFT technology.

The major attraction of applying polycrystalline silicon thin-film transistors (poly-Si TFTs) is in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility in poly-Si film and the capability of integrating the pixel switching elements and the capability to integrate sophisticated digital and analog driving circuit on the glass substrates[10-12]. For the poly-Si active layer, carrier mobility

larger than 10 cm^2/Vs can be easily achieved, that is enough to use as peripheral driving circuit including n-and p-channel devices (or p-channel only). Such performance brings the era of system-on-panel (SOP) technology. The process complexity can be greatly simplified to lower the cost (which save the IC and FPC BOM cost). In addition, the mobility of poly-Si TFTs much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high driving current and high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that device channel width can be scaled down while meeting the same pixel driving requirements as in α-Si TFT AMLCDs.

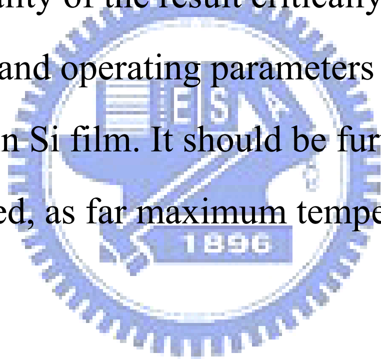
Nevertheless, some problems still exist in applying poly-Si TFTs on the large-area displays. In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to the ON current seriously [13]. Moreover, the relatively large leakage current is one of the most important issues of conventional poly-Si TFTs under OFF-state operation [14-15]. The dominant mechanism of the leakage current in poly TFTs is field emission via grain boundary traps due to the high electric field near the drain junction. To solve these problems, some crystallization methods such as excimer laser annealing (ELA) have been introduced to enlarge the grain size [16]. A dual gate device or lightly-doped drain (LDD) region is used to

effectively lower leakage current by decreasing drain electric field [17]. Up to date, some studies of poly-Si TFTs also focus on developing new technologies to lower the maximum fabrication temperature, which enables the use of low-quality glass and therefore reduce production cost [18]. Some reported papers focus on the fabrication and characterization of small-dimensional poly-Si TFTs [19], which has driving ability and high resolution and can be applied on AMLCD peripheral circuitry or the high-resolution projectors. In summary, it is expected that the poly-Si TFTs will becomes more and more important in future technologies, especially when the 3-D circuit integration era is coming. More researches study the related new technologies and the underlying mechanisms in poly-Si devices with shrinking dimensions are therefore worthy to be indulged in.

The fabrication of polycrystalline-silicon TFTs (poly-Si TFTs) encompasses many of the steps commonly in MOSFET fabrication for integrated circuits. Despite the similarities, however, a number of key differences exist. These differences emerge primarily from the fact that the substrate of TFTs is no longer a single-crystal silicon wafer, but rather a typically heat-sensitive material such as glass. This means that, unlike MOSFET devices, the TFT active layer needs to be formed on such amorphous host material and, furthermore, that the temperature of all associated processing has to be constrained within the allowable range prescribed by the maximum processing temperature needs to be kept below~650˚C. Even after considering possible exceptions to this maximum temperature (typically encountered during rapid thermal processing), the temperature range for fabrication on glass is severely

constrained with respect to that on Si. This limitation affects critical process steps, such as the gate-insulator formation and the activation of the doped regions of the device. These Processes have to be reconsidered and optimized for TFT fabrication on glass.

The substrate dissimilarity, however, has an even more immediate impact on the process flow of TFTs. Unlike MOSFETs, Where the device active layer is part of the substrate, in the case of TFTs the active layer needs to be separately formed on the host substrate. The common way of doing that, for poly-Si TFTs, is by deposition of an amorphous Si (a-Si) film on host substrate and the annealing step. Both of these steps affect the micro-structural quality of the result critically affected by the selection of techniques and operating parameters for the deposition and crystallization of the thin Si film. It should be further noted that these steps are also constrained, as far maximum temperature, per our earlier discussion.



1.2Motivation

The market for liquid crystal displays has been rapidly expanding in recent years. The demand for a high luminance and a high contrast ratio in liquid crystal displays (LCDs), such as small-medium LCDs for projection device, mobile displays and displays for cars, is continuing to grow and seems insatiable. However, high luminance would increase photo leakage current (PLC) in the TFTs, which diminishes the voltages that are held across the pixel electrodes or affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. For instance, the off current of poly-Si TFTs exposure at the 3000nits

backlight is higher that in the dark, which is about higher one order, shows as the Fig.1.1. and Fig.1.2. Not only low drain voltage but also high ones. It is suffer the On/Off ratio of device and will affect the TFTs operating. It goes without saying for the application of brightness about 8000nits in car. Consequently, it is necessary to suppress the PLC in LCDs with high luminosity.

In this thesis, there are three schemes to suppress the PLC. First scheme is to vary the center of generated / recombined between the buffer layer and poly-Si active layer [20] so that the electron-hole pairs which were excited by back light, the electron-hole pairs were generated at the bottom of the poly-Si layer. Second one is using the light-absorption structure sot that less light can reach the active layers of TFTs [21]. The last one is using light-shielding structure, here we employ the opaque Material to shield the light, it is the most effective to cut-off the light from the backlight source. Unfortunately, this method still has some side effect that we will have detail discuss later. In this thesis, we focus upon those methods and have examined how the PLC changes depending upon structural parameters of TFTs and pursuit a desirable device structures of the TFTs. This work has been done for the TFTs with low-temperature poly-Si (LTPS).

1.3 Thesis outline

The goal of this thesis is to study how to suppress the photo leakage current (PLC) when the TFTs exposure the backlight in simply methods and do not suffer the through put under the fabrication. The arrangement of chapters follows the generally principles.

First, detailed poly-Si TFTs fabrication process flow in array is present. Before the poly-Si active layer forming, all the key experimental structures and procedures in the chapter2.

Section2.1 presents the first experiment of reduce PLC, the interface between buffer layer and poly-Si layer treatment which including NH3 and O2 plasma treatment by PECVD and Argon ion treatment by ion implanter.

Section2.2 presents the second experiment of reduce PLC, we use silicon rich film to be a absorbed layer to lessen the light to reach the active poly-Si layer.

Section2.3 presents the third experiment of reduce PLC, here we use a opaque film, e.g. Mo、W、MoW and aSi:H etc..., the Mo is employed to shield the backlight in our experiment. Then we also discuss some side effect that unexpected.

Section2.4 presents the way for extracting the parameters of device. Those parameters are important for semiconductors.

Second, we are aimed at our experimental result and giving a discussion to each experiment, i.e. buffer/poly-Si interface treatment, metal shielding and silicon-rich film absorption, respectively. Then we have a summary for this experimentation. In this chapter, four sections are arranged.

Section3.1 discusses the interface of buffer/poly-Si treatment result, and we refer to a PLC model which derived by Kunihiro Suzuki at 2004 [20].

Section3.2 discusses the silicon rich absorbed film result; it is the most feasible method in thesis that does not need any extra process.

Section3.3 discusses the metal shielding result and proofs floating body effect by the simulating data. Of course, we bring up an idea to solve the problem.

Section3.4 does some summary of our experiments.

Third, the last chapter in the thesis, we give a conclusion to make up for the integrity of thesis.

Chapter 2

Device Fabrication and Experiment

Second, detailed poly-Si TFTs fabrication processes and experimental procedure, such interface treatment, shielding metal forming and silicon-rich film absorption, were described.

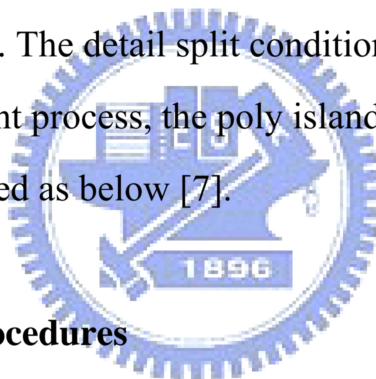
2.10 Process flow of our standard control sample

The top gate p-channel and self align light drain doping (LDD) TFTs were fabricated on Corning1737 glass substrate [1]. First, the buffer SiNx/oxide layer and 50 nm thickness a-Si:H film were deposited by plasma enhanced chemical vapor deposition (PECVD) at 380℃, we dehydrogenated aSi:H film in a furnace at 450℃. Then the poly silicon channel was formed by 308nm XeCl excimer laser irradiation at 350mJ/cm2. In this work, 95% laser overlap ratio was adopted to obtain large grain size and better uniformity of active layer. As the SEM Fig.2.1, the average grain size of polycrystalline silicon was found to be 280~300nm [3]. The island was patterned by plasma dry etching Fig.2.2. The 100nm thickness gate insulator was deposited by TEOS (Tetra-Ethyl-Ortho-Silicate)-base oxide. The source/drain and LDD region were formed by the mass-separated ion implanter technique. The doping activation was performed at 530℃/1hr thermal furnace and RTA irradiation Fig.2.3~Fig.2.4. Finally, the interlayer oxide and inter-connection metal were deposited and pattern. The H2 plasma hydrogenation was performed in a commercial RF parallel-plate plasma

reactor at 100W, 480℃ 15min in H2 and Argon gas mixture. The SiO2/SiNx with 300nm and 100nm interlayer film and source/drain contact holes etching and S/D metal patterning Fig.2.5. Finally, the planer layer (UHA2) and ITO were employed on our device Fig.2.6 [4-6]; the device electrical measurements were finished by HP4156C.

2.11 Devices Structure of interface treatment

Fig.2.7 was shown the treatment structure of our device, in this experiment, we treated the interface between buffer oxide and poly-Si active layer. We employed the NH3 and O2 plasma by PECVD and Argon by ion implanter. The detail split condition, please referred to the table 2.1. After treatment process, the poly island forming and the others procedures was described as below [7].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2.12 Experimental Procedures

The top gate p-channel and self align light drain doping (LDD) TFTs were fabricated on Corning1737 glass substrate [ ].First, the buffer SiNx/oxide layer and 50 nm thickness a-Si:H film were deposited by plasma enhanced chemical vapor deposition (PECVD) at 380℃, we dehydrogenated aSi:H film in a furnace at 450℃. The treatment step, NH3 (300w/10min) and O2 (2kw/10min) plasma by PECVD and Argon (1~2mins) by implanter, was interrupted before 50nm aSi:H deposited. After treatment, refer the process as 2.10. Check to Fig.2.7.

2.21 Devices Structure of Si-Rich Film

This experiment did not add extra thin film deposited or photo process. In our work, we employed silicon rich oxide and silicon rich SiNx film to replace the buffer layer of the conventional TFTs. Fig.2.8a is shown the 200nm silicon-rich SiNx to replace the buffer SiNx; Fig.2.8b is shown the 200nm silicon-rich oxide to replace the buffer oxide. Table2.2 was our split condition [8]. Besides the properties silicon rich film, the other crucial point for display was etching back the transparent area of array pixel essentially. The following is the detail procedure.

2.22 Procedures of light absorption by silicon rich film.

A 100nm silicon-rich SiNx and SiOx were deposited by PECVD respectively, then buffer oxide and a-Si:H were on the silicon-rich film, as the Fig.2.8a and Fig.2.8b. The following detail procedure as referring to 2.10. The Full structure figures were shown in Fig.2.9a and Fig.2.9b.

2.31 Devices Structure of Metal Shielding

Fig.2.10 was shown the shielding structure with molybdenum (Mo), it was oversimplification and directly perceived way to suppress or cutoff the backlight to reach the poly-Si active layer. The section2.32 specified how the process to be implemented.

2.32 Experimental Procedures

First of all, a thin and opaque film was sputtered on the glass substrate, here we used 80nm molybdenum to be a shielding layer, shown in the Fig.2.11 [9]. After the shielding process, the conventional process liked the standard structure sample we had mentioned in section 2.10.The

device as shown in Fig.2.11.

2.4 Electrical Characterization Measurement and Analysis

2.41 Output characteristics

The typical TFT output characteristics are shown in Fig.2.12. They represent the dependence of the Drain-Source current (I_{DS}) on the Drain-Source voltage (V_{DS}) at different gate voltage (V_{GS}). The Drain-Source current increase linearly at low Drain-Source voltage (Linear regime/operation) and saturates at high Drain-Source voltage (Saturation regime /operation). The saturation values of I_{DS} depend on the applied gate voltage. When the low gate voltage is applied, the thickness of the induced channel is small and current is low. On the other hand, thicker channel is induced at high gate voltage and the saturation current is higher. Well-separated output characteristics are an indication of good ohmic contact at drain and source. The transistor enters in saturation regime when $V_{DS} > V_{SAT}$, where $V_{SAT}=V_{GS}-V_T$. In Id_Vd curve, the points corresponding to $V_{DS} = V_{SAT}$ are connect the blue line described the following equation:

$$I_{DS} = \frac{1}{2} \times \mu_{fe} \times Cox \times \frac{W}{L} \times \left[(V_{GS} - V_T)^2 \right] \quad \text{.................................} \quad (2\text{-}1)$$

When W and L are the width and length of the transistor channel, μ_{fe} is the field-effect electron mobility and C_{ox} is the gate insulator capacitance. The threshold voltage and the field mobility effect mobility can be determined from measuring the saturation current, plotting the

square root of the measured I_{DS} vs. V_{GS} in saturation ($V_{DS} \geqq V_{GS}-V_T$).

Of course, the poly-Si TFTs are not perfect device as the single crystalline; it is since the grain boundary [10]. The region of operation in poly-Si TFT roughly:

a. Cut-off : Current is due to reverse-bias drain junction leakage trap-assisted mechanisms.

b. Subthreshold : Current is due to carrier diffusion. Limited by source junction potential barrier.

c. Pseudo-subthreshold : Current is due to carrier drift. Inversion-charge density Q_{inv} increases ~linearly with V_G-V_T. The field mobility μ_{fe} increases ~ exponentially with V_G ➔ I_D increases ~ exponentially with V_G.

d. Above threshold : Current is due to carrier drift, Qinv V_G-V_T; μ_{fe} ~ constant➔ I_D increases linearly with V_G

Refer to the Fig.2.13.

2.42 Method of device parameter extraction

In this section, we will introduce the methods of typical parameter extraction such as threshold voltage V_T , field-effect mobility μ_{FE} , subthreshold swing SS and the transconductance Gm. Those essential parameters of device characteristic are always be employed to monitor the process status in the mass production.

Set up instruments for IV measurement

Apparatus

(1) Microscope and probe station in Fig14.

(2) Agilent4156C and E5250A are shown in Fig15.

(3) Software of measurement Sagittarius (人馬座) which is created by STARs Tech. Co....Fig.2.16.

Then we use the software to get follows:

1. I_{DS}_V_{GS} (Linear region)
2. I_{DS}_V_{GS} (Saturation region)
3. I_{DS}_V_{DS}
4. G_m_V_{GS}

Where

V_{DS} : Drain voltage

I_{DS} : Drain current

V_{GS} : Gate voltage

G_m: I_{DS}_V_{GS} max slope

2.43 Determination of the field-mobility

The field-effect mobility (μ_{fe}) is determined from the Transconductance Gm at low drain voltage. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si MOSFETs, which can be expressed as

$$I_D = \mu_{fe} \times Cox \times \frac{W}{L} \times \left[(V_{GS} - V_T)V_D - \frac{V_D{}^2}{2} \right] \quad \text{..............................} \ (2\text{-}2)$$

Where

Cox is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

Vth is the threshold voltage,

If V_D is much small than V_G-V_{TH} (i.e. << V_G-V_{TH}) and $V_G > V_{TH}$, the drain current can be approximated as :

$$I_D = \mu_{fe} \times Cox \times \frac{W}{L} \times [(V_{GS} - V_T)V_D] \quad \text{......................................} \text{ (2-3)}$$

The Transconductance is defined as Fig.2.16

$$Gm(i) = \partial I_D / \partial V_G(i) = \mu_{fe} \times Cox \times \frac{W}{L} \times V_D \quad \text{..............................} \text{ (2-4)}$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{fe}(i) = Gm(i) \Big/ \left(Cox \times \frac{W}{L} \times V_D \right) \text{.......................................} \text{ (2- 5)}$$

Then μ_{fe} is:

$$\mu_{fe} = \max.(\mu_{fe}(i)) \text{...} \text{ (2-6)}$$

2.44 Determined the threshold voltage

Threshold voltage (V_T) is the most important parameter of semiconductors device, of course, there are lots of ways to determine the parameter, for example, constant current method or G_m max. etc. Here we use the familiar method, I_D_V_{GS} insert, as the Fig.2.17, and then we can get the simple equation as follow:

$$V_{T_{lin}} = \left(Id(i)\times Vg(i-1) - Id(i-1)\times Vg(i)\right) / \left(Id(i) - Id(i-1)\right) \ldots\ldots\ldots\ldots \text{(2-7)}$$

Where i is the Gm_{max} position, thus, the V_T is easy to be determined.

2.45 Determined the Sub-threshold Swing

Subthreshold swing S.S (V/dec) is a typical parameter to describe the control ability of gate toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punch through-like effect. The subthreshold swing is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this study, S.S parameter is got from I_D_V_G curve, it can be express as the follow equation:

$$S.S._{min}(i) = \left[V_G[i] - V_G[i-1])/\log_{10}(I_D[i]/I_D[i-1])\right] \ldots\ldots\ldots\ldots \text{(2-8)}$$

The S.S. parameter is calculated by excel of Microsoft or the other calculated software easily [11].

Chapter 3

Result and Discuss

Third, in this chapter, we would report three kinds of experimental results we had done. Electrical properties are discussed and we did material analysis for silicon rich films, respectively. Following were the results and discussion for each suppressed method.

3.1 Interface between buffer layer and active poly-Si layer treatment

3.11 Result of the interface treatment

First, shown in Fig. 3.1, the device size is W=6um and L=12um. I want to show that the fundamental electric characterization of our experimental TFTs is as good as the standard ones'. It is meant that devices performance is not affected during the treatment process and we are also concerned about that.

The reduction the PLC for the TFTs with interface treatment is shown as Fig. 3.2a and Fig. 3.2b. We had also fabricated a conventional sample (without any treatment) for a comparison. The trend chart of the low drain voltage is conspicuous that we proposed treatment process improves considerably (~50% than w/o any treatment) due to the trap trapping which creating by interface treatment. Because we assume that electron-hole pairs are generated when backlight is absorbed near the buffer/poly-Si interface. These electron-hole pairs either recombine at the buffer/poly-Si interface or diffuse to the gate insulator/poly-Si interface and recombine there [1]. The 3rd sample is not effective as the other one's due to the treatment time, it is well known that Argon process by the ion implanter is very short, about 1or 2 minutes only. If we want to get the

better result we can increase the parameters of implanter. Fig. 3.3 was shown the subthreshold Swing different from dark and illuminated. It was a powerful evidence to explain the effect.

3.12 Mechanism of Trapping

As we mention last section, the photo leakage current analysis model has been derived by Kunihiro Suzuki at 2004 [1]. The Fig. 3.4 shows the distribution in the poly-Si of our TFTs. The balance of flow at both interfaces is given by

$$Q = s_b N_m + D\frac{N_m - N_s}{t_{Si}}, \quad D\frac{N_m - N_s}{t_{Si}} = s_f N_s \qquad \text{.......... (3-1)}$$

Where

Sb: recombination speeds at the glass/poly-Si interface

Sf: recombination speeds at the poly-Si/gate oxide interface

Nm: the electron-hole pair concentration at the glass/poly-Si interface

Ns: the electron-hole pair concentration at the poly-Si/gate oxide interface

After derive and the ΔV_0 be determined experimentally as table 3.1

$$I_{Dchan}(Photo) = I_{dark0}\exp\left[\frac{q(\Delta V_0 + (1-\kappa)(V_G - V_{G0}))}{n_{dark}k_B T}\right]$$

$$\Delta V_0 = \ln\left(\frac{1}{k(1 + h_{FE})}\right) \qquad \text{............................ (3-2)}$$

Finally, the drain current during backlight exposure can be expressed by

$$I_D(Photo) = I_{dark0}\exp\left[\frac{q(\Delta V_0 + (1-\kappa)(V_G - V_{G0}))}{n_{dark}k_B T}\right] + a\frac{1+2h_{FE}}{1+h_{FE}}\frac{Q}{\Gamma s_p}t_{Si} \quad \text{…………….. (3-3)}$$

The Fig 3.5 was shown that the IV curve of model and experiment the author provided.

Thus, we created lots of the recombined (trapping) center by plasma treatment in the bottom of the poly-Si. The electron-hole pairs were excited by the light source, the excited pairs would die out before reaching the drain/source regions due to the trap fig.3.6. Consequently, the PLC was reduced efficaciously.

3.2 The Silicon Rich Film Shielding

The second way to suppress the PLC which we provided was to absorb the backlight with silicon rich SiNx and silicon rich SiOx film; we want to decrease the light to reach to the poly-Si active layer, then the electron-hole pairs got lower energy, the photon was decreased [2].

3.21 Result of the absorption

Fig. 3.7a and Fig. 3.7b showed the PLC result with silicon rich film, not only silicon-rich SiNx but also silicon-rich oxide was significant effect to reducing the PLC. Of course, the ΔSS of Si-Rich film was shown in Fig. 3.8, to prove this method work. According to our data, silicon-rich oxide seems to own better absorption, we thought that was due to the thicker thickness. The absorbed efficiency vs. the thickness of silicon-rich film would be shown later, undoubtedly, it was strong related. Fig. 3.9 was the

thickness vs. transmittance, it was clearly the transmittance with 1k Si-R SiNx was about 80%, but the drop of transmittance in 3kA was 45%.

3.22 Material analysis

To proceed with the procedure, we would take to some physical analysis for the silicon-rich SiNx film. In the Fig. 3.10a and Fig. 3.10b, the transmittance of standard structure was about 90%, in the Si-rich film SiNx structure was much lower than STD, especially in the 350nm~600nm. It was important that Si-rich SiNx film could absorb majority visual light of human. Therefore, the less light pass to the active poly-Si layer, the lower photo leakage current was produced. Fig.3.11

3.3 The Shielding Method

To use a shielding method, the shielding material could be non-transparent film, especially metal. The follow result was employing the molybdenum (Mo) to shield the backlight [3].

3.31 Result of the metal shielding with molybdenum

For a start, the Fig. 3.12, was the device cross-section of shielding layer by SEM, this etching profile was patterning with the same mask by dry machine. According to the picture, the thin Mo film which was large than active poly-Si layer, it could cut-off the light from back light source. Proceeding to the step, the electrical properties of device was not as good as the control sample without shielding, but the PLC result was the best, referred to the Fig. 3.13. The electrical result was due to the Mo layer under the poly-Si layer would share the crystalline energy of ELA

process. That is easy to fine tune the optimum energy of ELA process. Another undesired effect was floating body effect (FBE), which was caused by the drain terminal of device coupling to the shielding metal. This phenomenon would be explained in the following section.

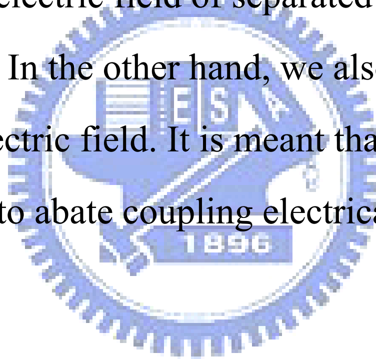
3.32 Floating-Body Effect (FBE)

In bulk silicon device, the channel region is grounded to the silicon substrate. On the other hand, in SOP/SOG devices as with SOI devices, the shielding metal layer under the active poly-Si layer which is not electrically connected to the terminal with fixed potential. Under the TFTs operating, the shielding metal would be coupled a potential. This is called the floating body. During operation, this shielding layer would be induced a potential and causes several undesired effects, for example, the kink effect. There undesired effects are called the floating-body effect. Because the body potential of a TFT depends on its biasing history and the carrier generation and recombination mechanism, the floating-body effect also depends on the device history and the recombination mechanism [4].

To investigate the FBE, for out device, observed in Fig 3.14, in more detail, a measurement was done which was changing V_{DS}. Fig 3.14, showed I_{DS} vs. V_{GS} with different V_{DS}. The I_{DS}_V_{GS} curves were shift dependence on V_{DS}, the higher $|V_{DS}|$, the I_{DS}_V_{GS} curves were shift seriously. It was resulted from the drain terminal coupling, shown as Fig 3.15. Under the operating, the drain terminal voltage was Vd=-9.1v and the shielding metal was coupled as a floating potential, then negative charge was be induced in the bottom channel. Finally, the initial barrier

height was lower than standard structure. Shown in Fig. 3.16. The phenomenon was like the double channel [5]. Besides these, I use simulating tool to simulate this metal shielding structure. As we predict that there is a potential in the shielding layer which was induced by the drain terminal. The higher drain voltage, the much charge was induced.

To solve and decrease the floating body effect, we provided the new metal shielding structure, as the Fig. 3.17, the key point is to separate the full shielding layer (we had used) which under the active poly-Si layer. My purpose is to reduce the coupling potential caused by drain terminal of the TFT, and then the FBE is reduced. According to the simulation result, it is obvious the electric field of separated type is much lower than the full shielding ones'. In the other hand, we also can use thicker buffer layer to decrease the electric field. It is meant that separate the shielding metal layer is effective to abate coupling electrical field. Then the TFTs could work normal.



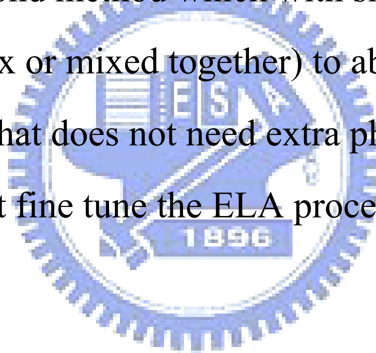
3.4 Summary

We used the compared table 3.2 to check the merits of the three ways. It is obvious that the red frame marked is better way we have done.

Chapter 4

Conclusion

We have provided three effective ways to reduce the photo leakage current and implement to poly-Si TFTs. The first one is bottom interface of poly-Si treatment; second: silicon rich film replace buffer layer; third: shielding metal. All the methods are not in good shape that could implement to fabricate the TFTs device for mass production directly. For example, the high BOM cost of plasma treatment by PECVD; the silicon rich film absorption in long visible wave and the floating body effect of metal shielding method etc…, those items we need to conquer. Finally, I want to suggest the second method which with silicon rich film (silicon-rich oxide, SiNx or mixed together) to absorb the light source. The key of this way is that does not need extra photography process or film deposition. We just fine tune the ELA process energy and so on.



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Chapter 1

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Table Caption

Table2.1 Split table of Interface Treatment Experiment

Split table	By PECVD		By I/I	
	#1	#2	#3	#4
Buffer layer_2kA				
Pre aSi treatment	NH3_300W/10min	O2_2kW/10min	Ar_30kev/1min	W/O
aSi dep.				
ELA				

Table2.2 Split table of Si-rich film Experiment

	#1	#2	#3
Buffer SiNx	Buffer SiNx_500A	x	x
Si-rich SiNx		Si-R(SiOx) 2kA	Si-R(Nitride) 1kA
Buffer SiOx	Buffer SiO2_1.5kA	x	Buffer SiO2_1.5kA
Si-rich Oxide			
aSi dep.	aSi_500A	aSi_500A	aSi_500A

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Table3.1 The extraction table

t_{si} (nm)	n_{dark}	ΔV_0(V)	κ	I_{dark0}(A)
50	3.2	0.45	0.35	6.50E-14
100	3.5	0.5	0.35	6.50E-14
150	5.7	0.7	0.35	6.50E-14

Table3.2 Compared table of suppressing methods we had provided.

實驗方法 / 比較項次	Interface Treatment	Si-Rich Film	Metal Shielding
PLC抑制效果	抑制30~50%	抑制30~50%	抑制~100%
邊際效應	無	無	有FBE
製程便利性	時間較長	方便	多一道鍍膜
成本考量	電漿成本高	OK	多一道鍍膜

Figure Caption

Chapter 1

Fig. 1.1 Id_Vg Curve of Dark and Illuminated at linear region.

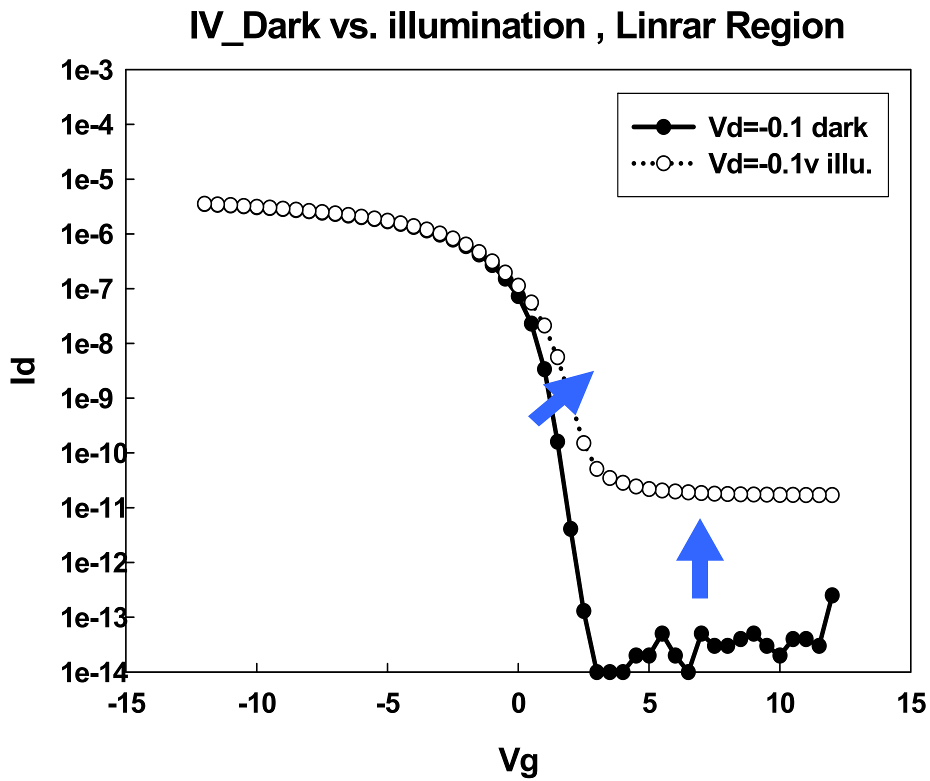
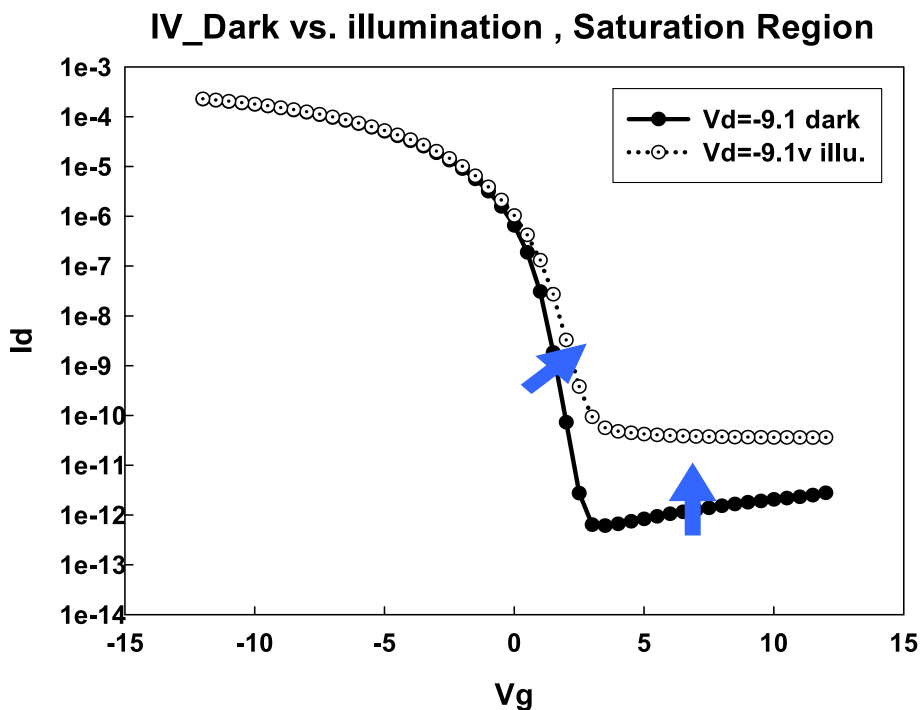


Fig. 1.2 Id_Vg Curve of Dark and Illuminated at saturation region.



Chapter 2

Fig.2.1 SEM of Grain Size

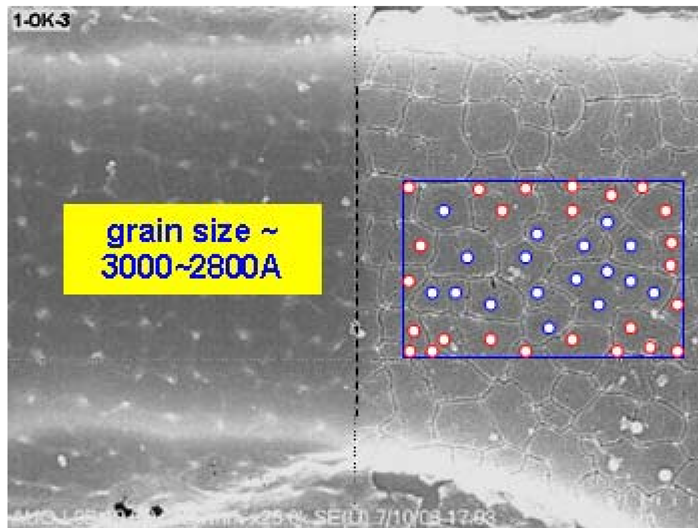


Fig.2.2 Pep1 Process Flow of LTPS PMOS TFT

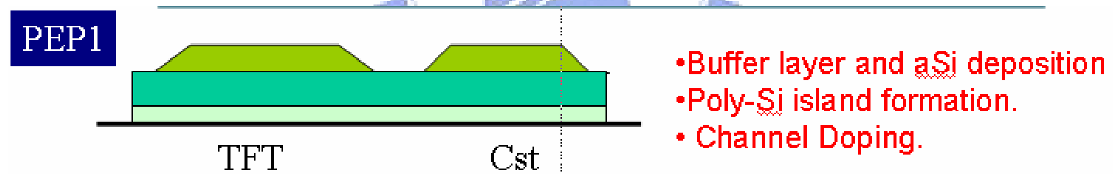


Fig.2.3 Pep2 Process Flow of LTPS PMOS TFT

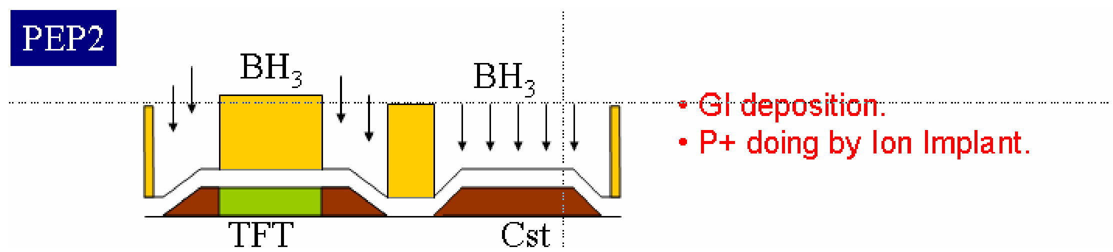


Fig.2.4 Pep3 Process Flow of LTPS PMOS TFT

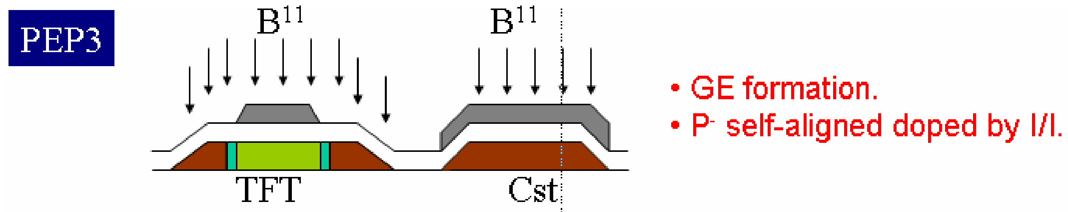


Fig.2.5 Pep4 Process Flow of LTPS PMOS TFT

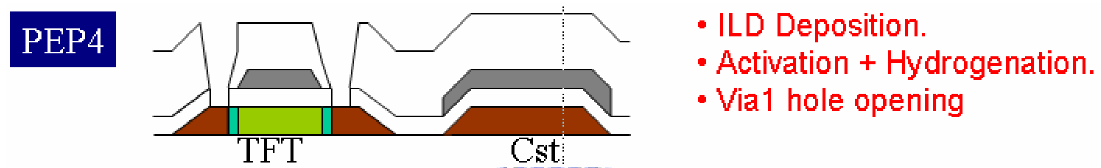


Fig.2.5 Pep5 Process Flow of LTPS PMOS TFT

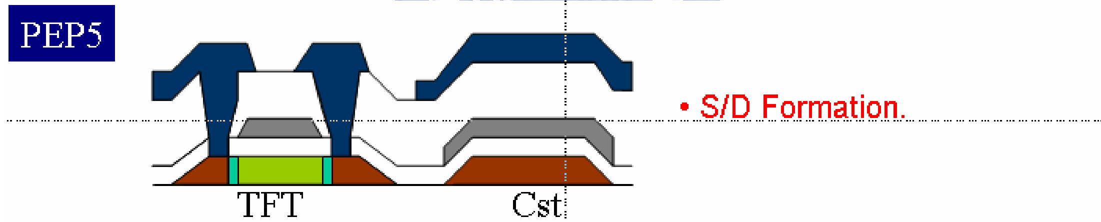


Fig.2.6 Pep6,7 Process Flow of LTPS PMOS TFT

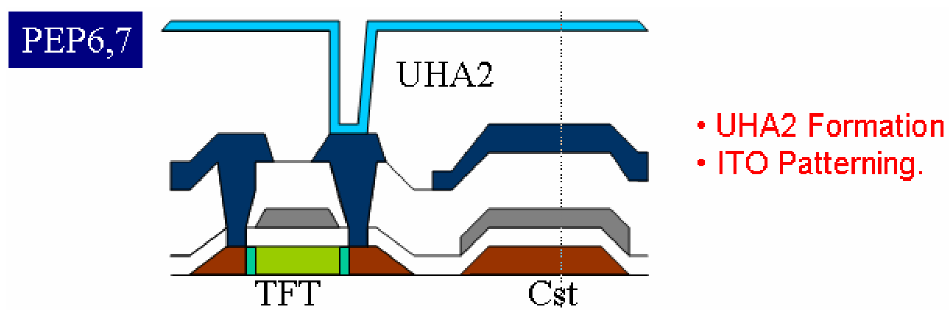


Fig.2.7 Structure of interface treatment

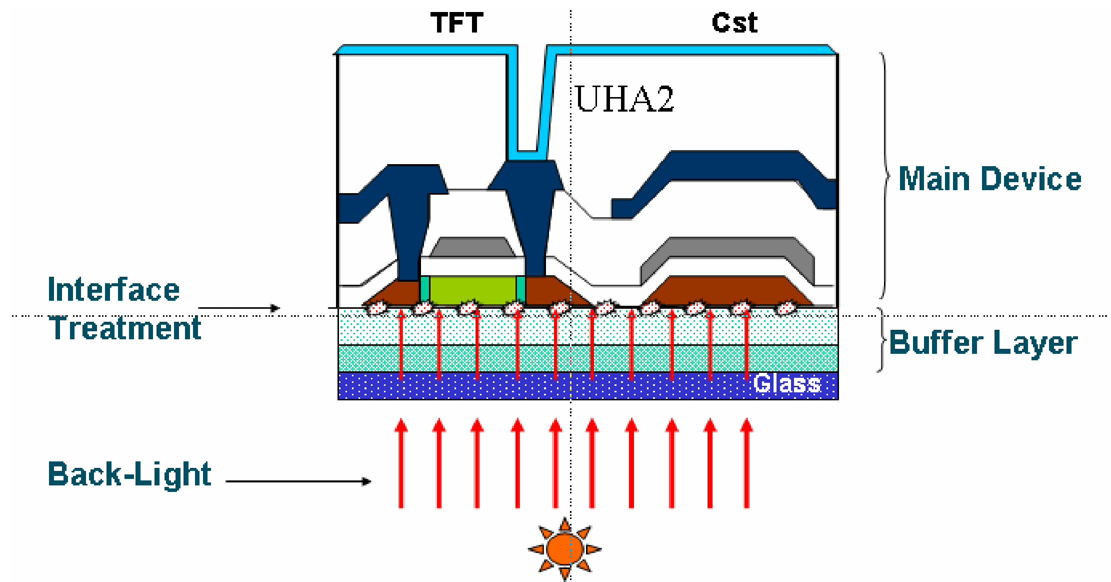


Fig.2.8a and 2.8b Structure of Si-rich Film replace buffer layer

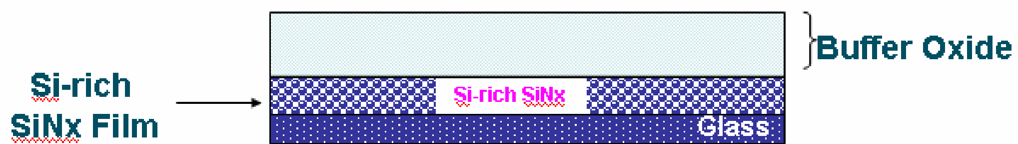


Fig.2.8a

Fig.2.8b

Fig.2.9a and Fig.2.9b were shown the full structure of Si-rich film replaced the buffer layer.

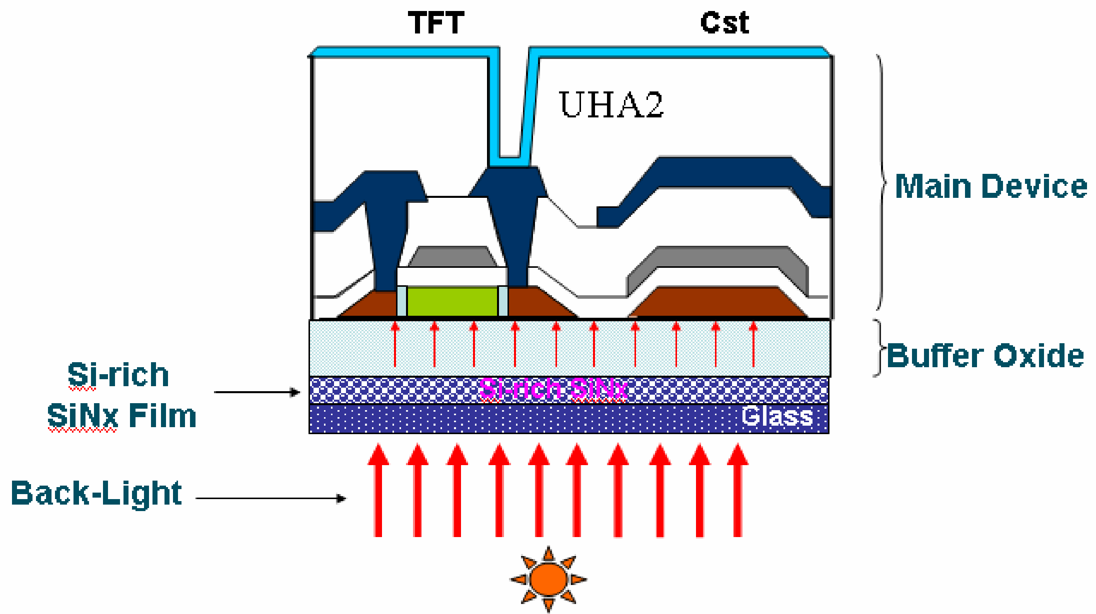


Fig.2.9a

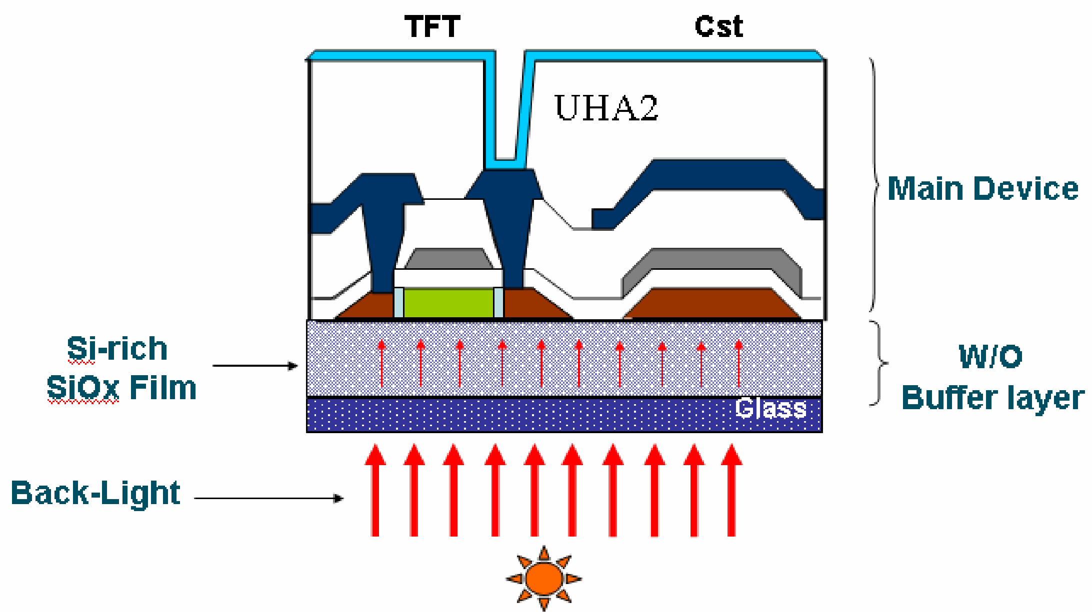


Fig.2.9b

Fig.2.10 Structure of shielding metal which was employed Molybdenum.

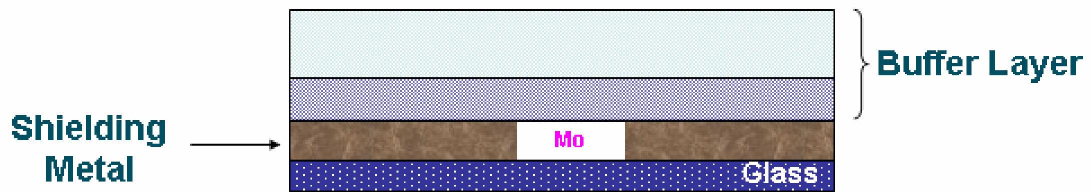


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Fig.2.11 Full structure of metal shielding

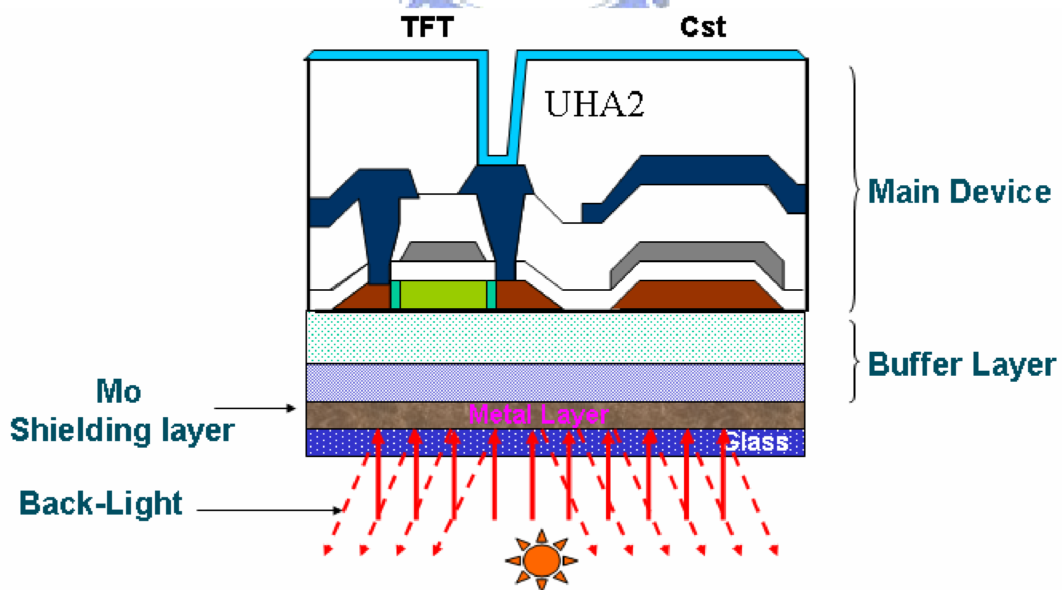


Fig.2.12 Id_Vg of Linear (Vd=-0.1v) and Saturation (Vd=-9.1v) Mode

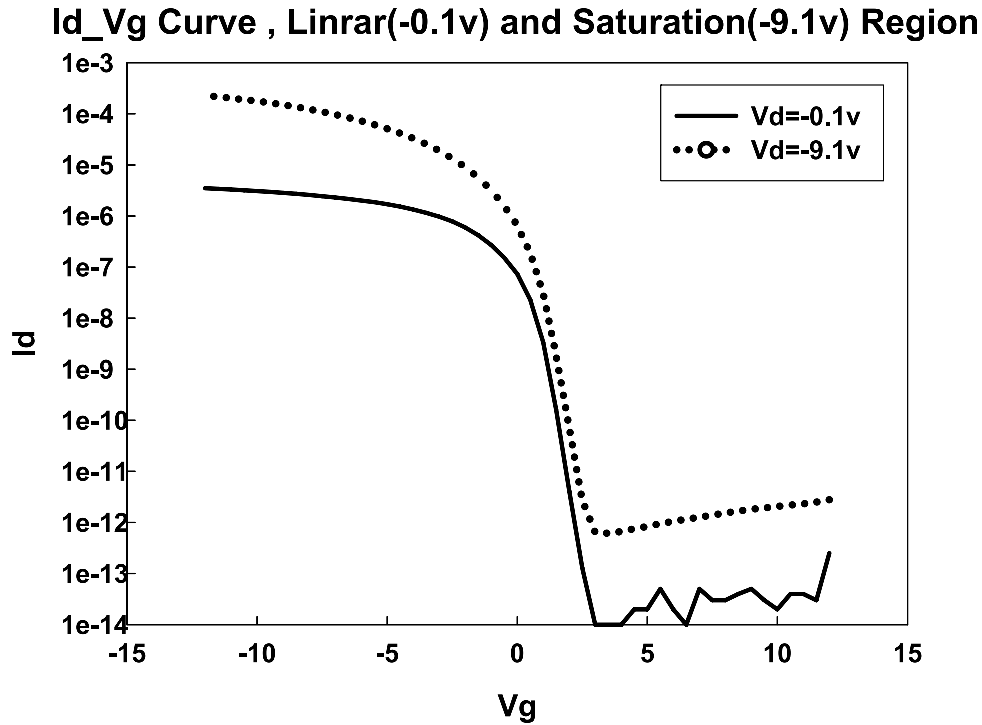


Fig.2.13 Poly TFT Transfer Characteristics (Id_Vg Curve)

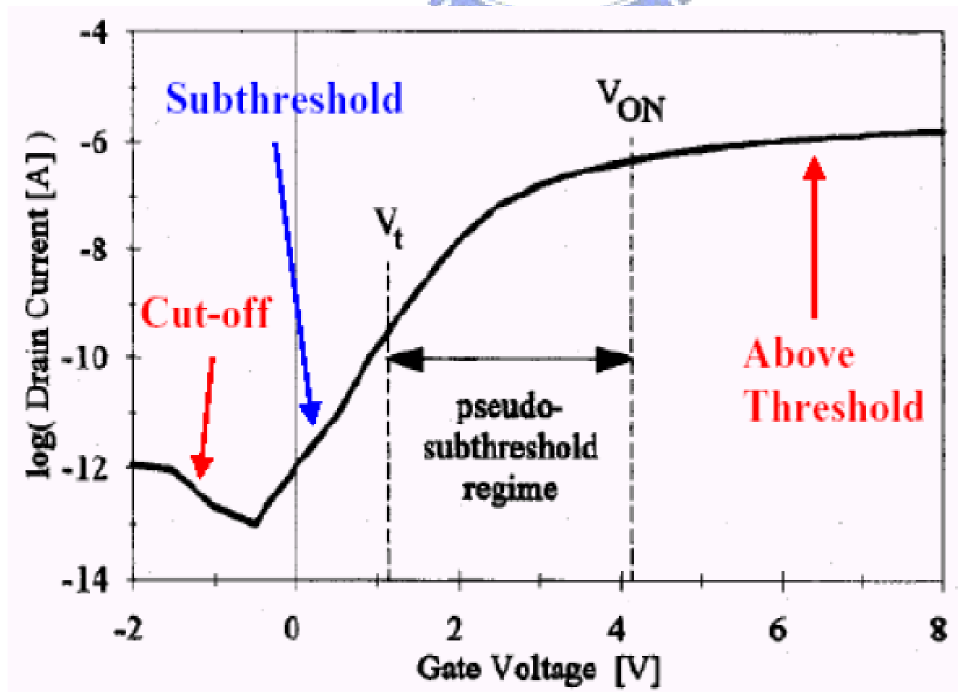


Fig.2.14 Measurement System➔Microscope and Probe Station

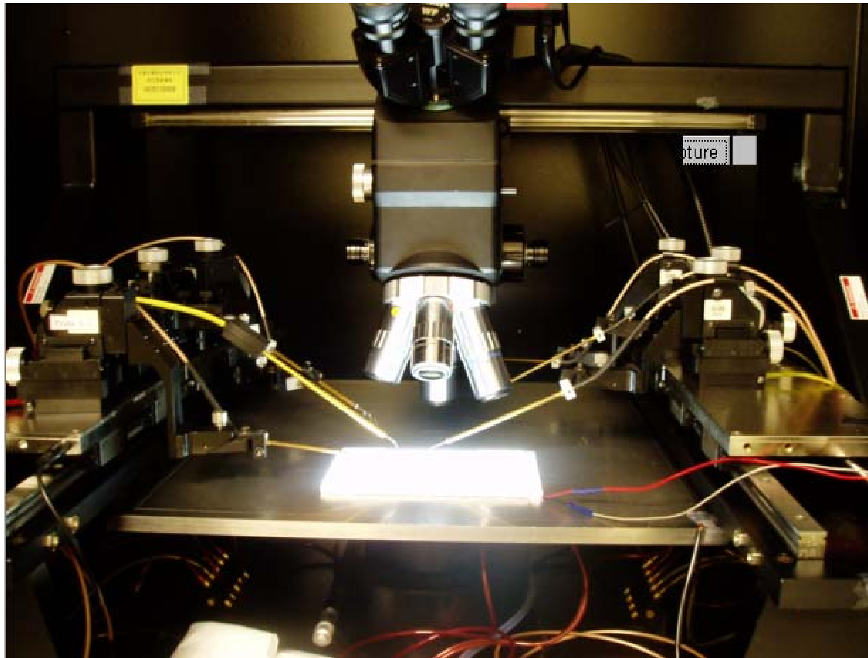


Fig.2.15 Measurement System➔ Agilent4156C

Fig.2.16 Measurement System➔Sagittarius Integrated Parameter Test Solution.

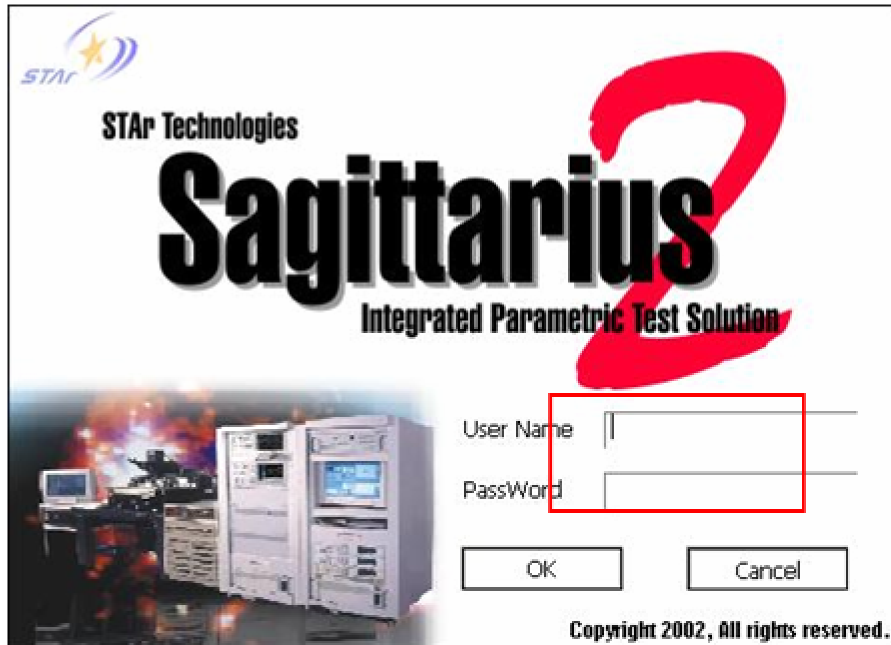


Fig.2.17 Id_Vg Curve and Transconductance (Gm)

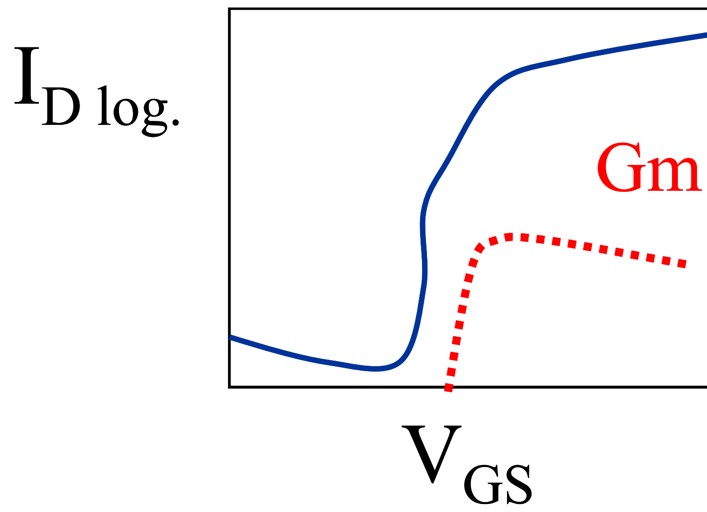
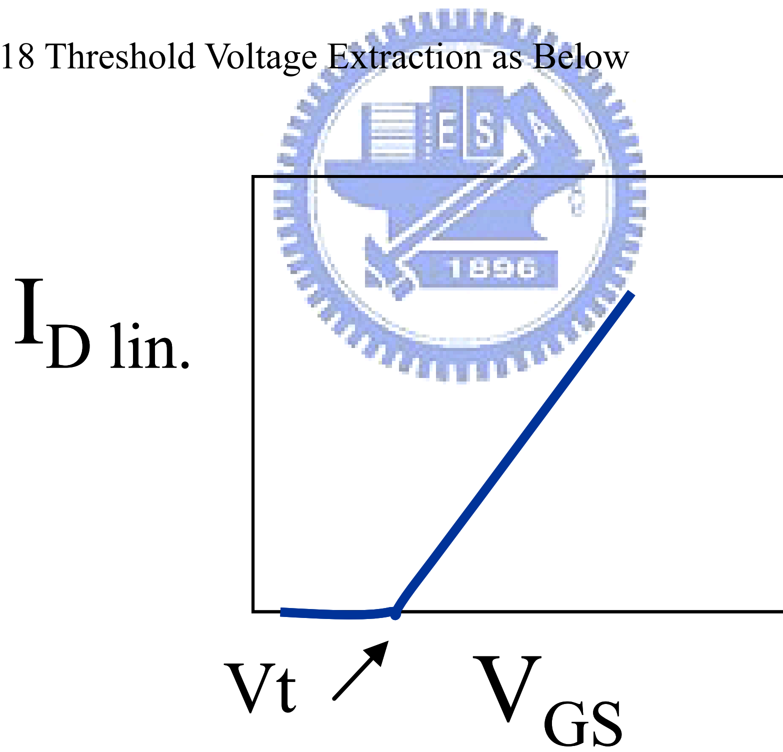


Fig.2.18 Threshold Voltage Extraction as Below



Chapter 3

Fig. 3.1 Electric Characterization of Treatment

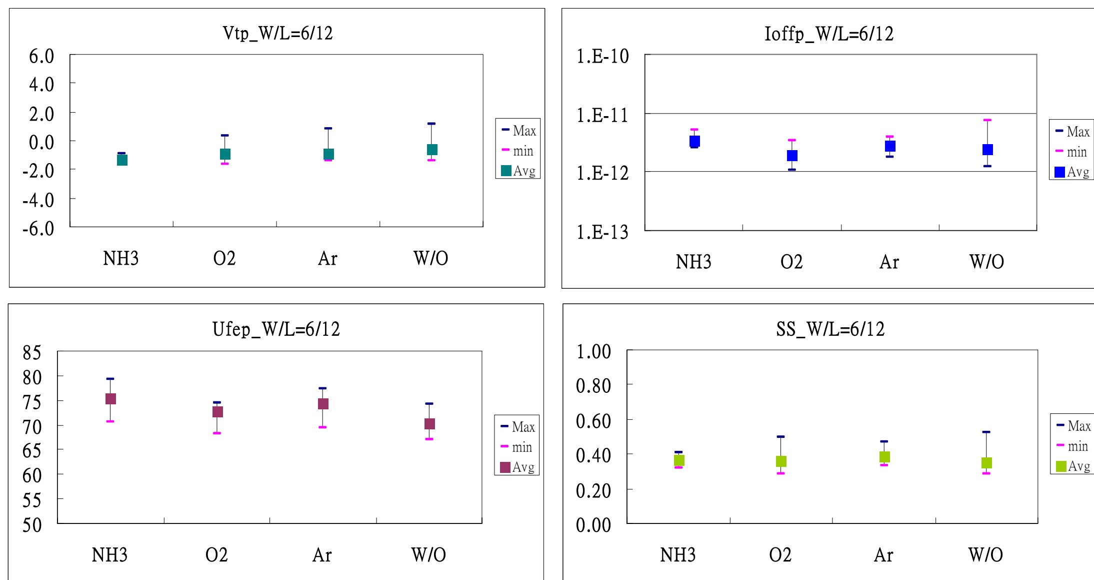


Fig. 3.2a PLC Result of Interface Treatment at Linear Region

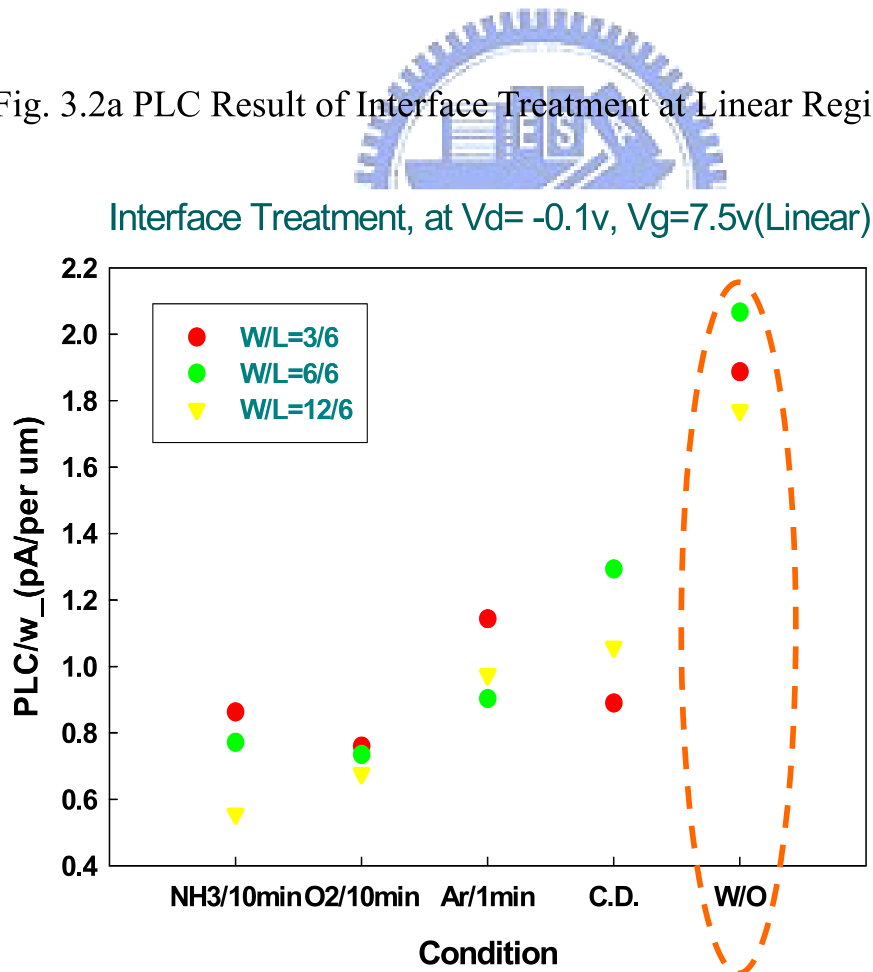


Fig. 3.2b PLC Result of Interface Treatment at Saturation Region

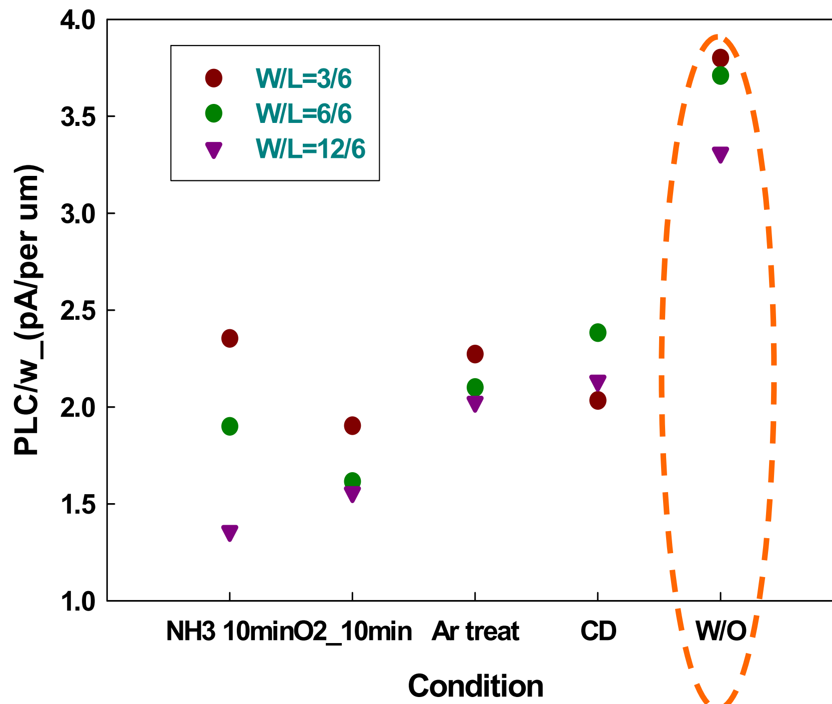


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Fig. 3.3 ΔSS of Interface Treatment

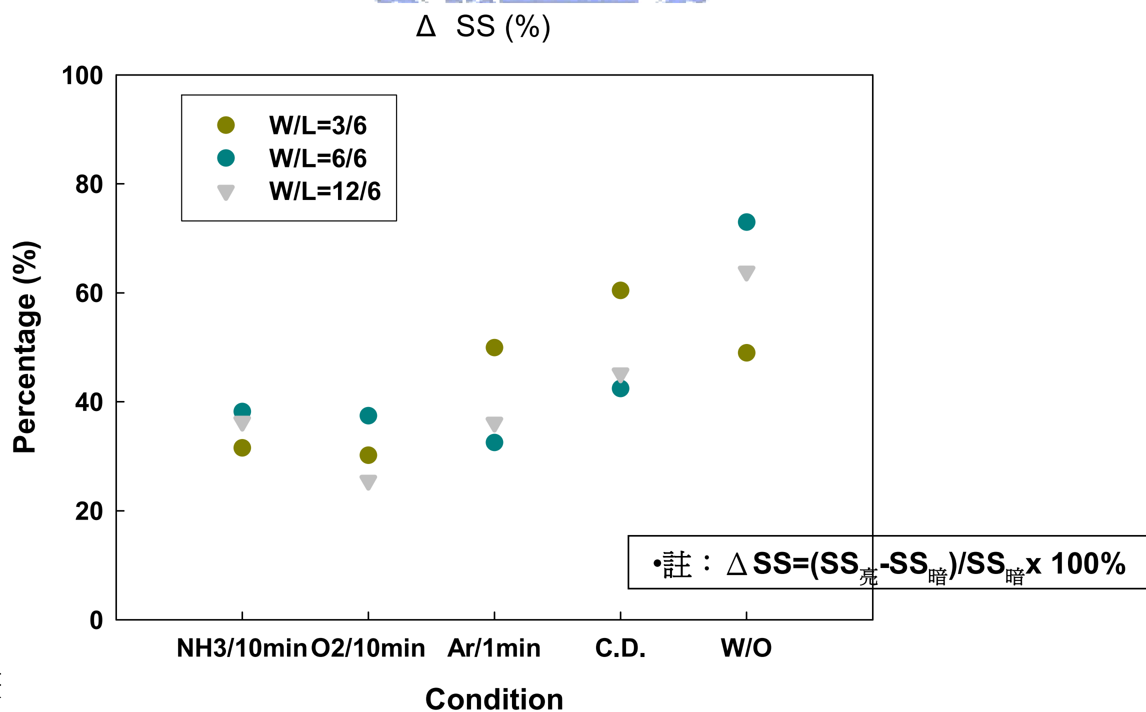

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Fig. 3.4 Distribution of electron-hole pairs in the poly-Si of TFTs.

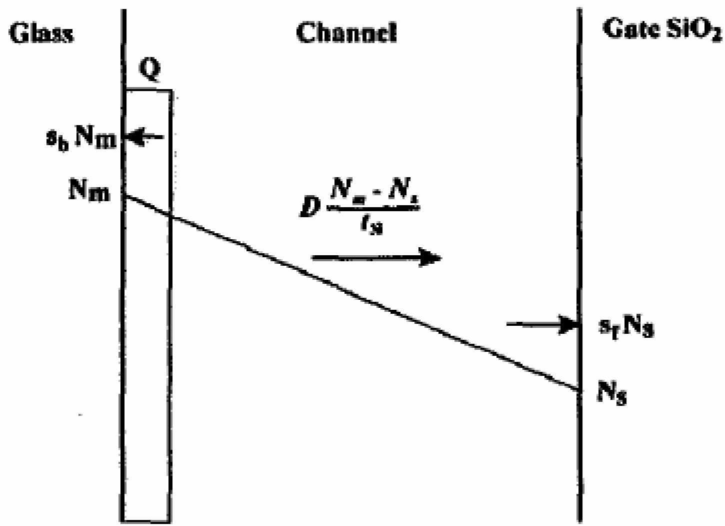

Fig. 3.5 IV Curves were shown the experiment and theory was matched.

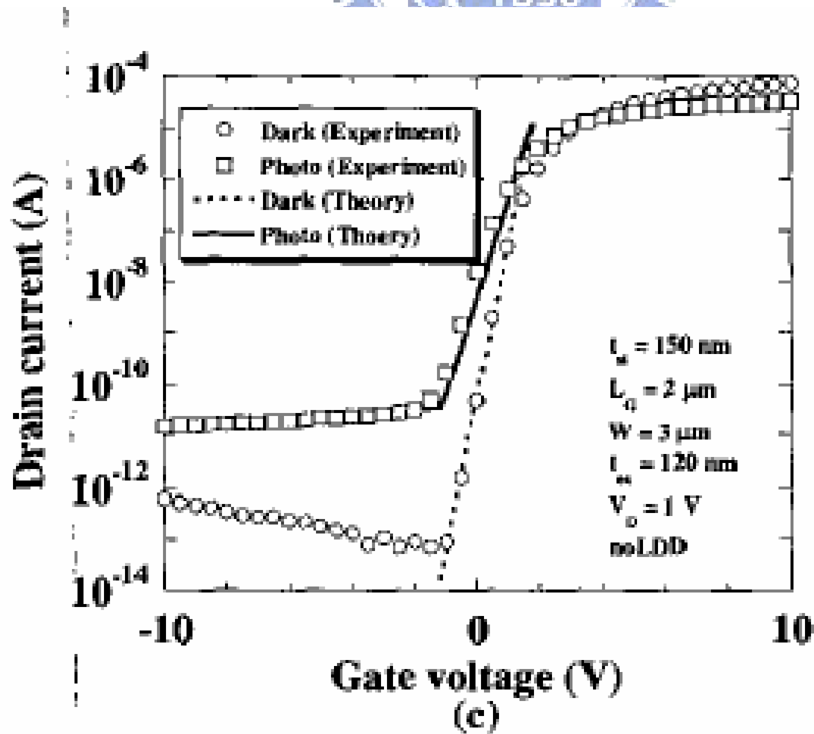

Fig. 3.6 Illustration of Recombination Center

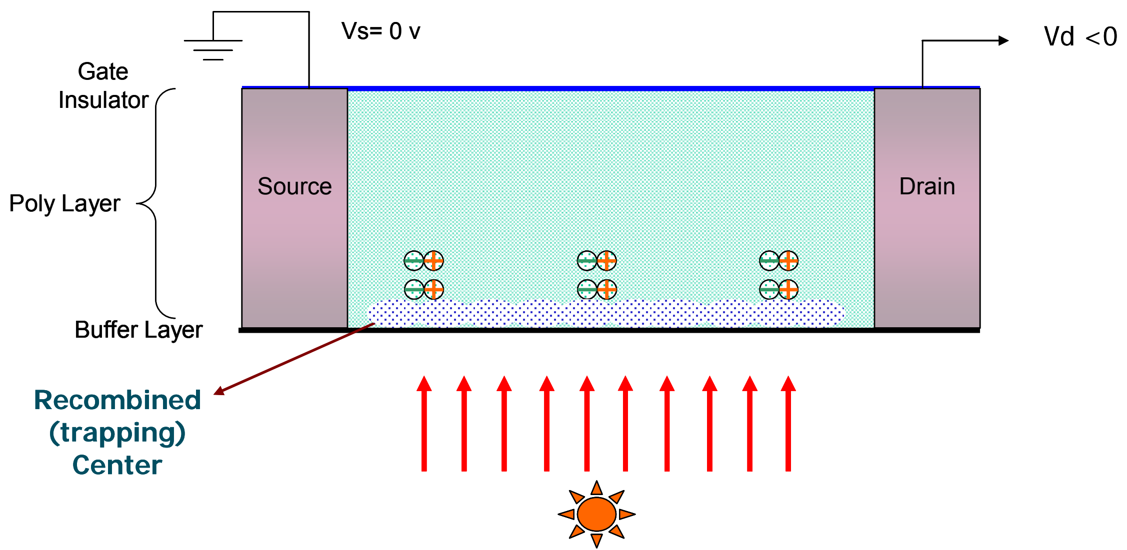

Fig. 3.7a PLC Result of Si-Rich Film in Linear Region.

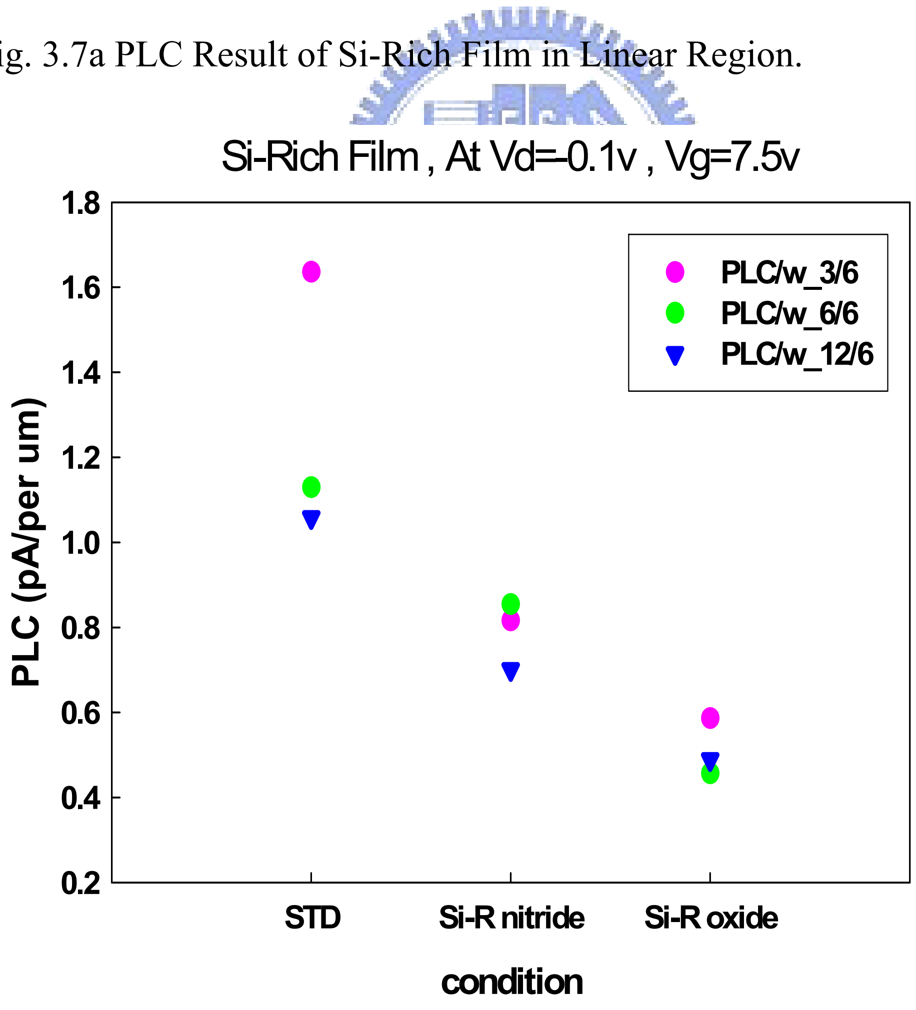

Fig. 3.7b PLC Result of Si-Rich Film in Saturation Region.

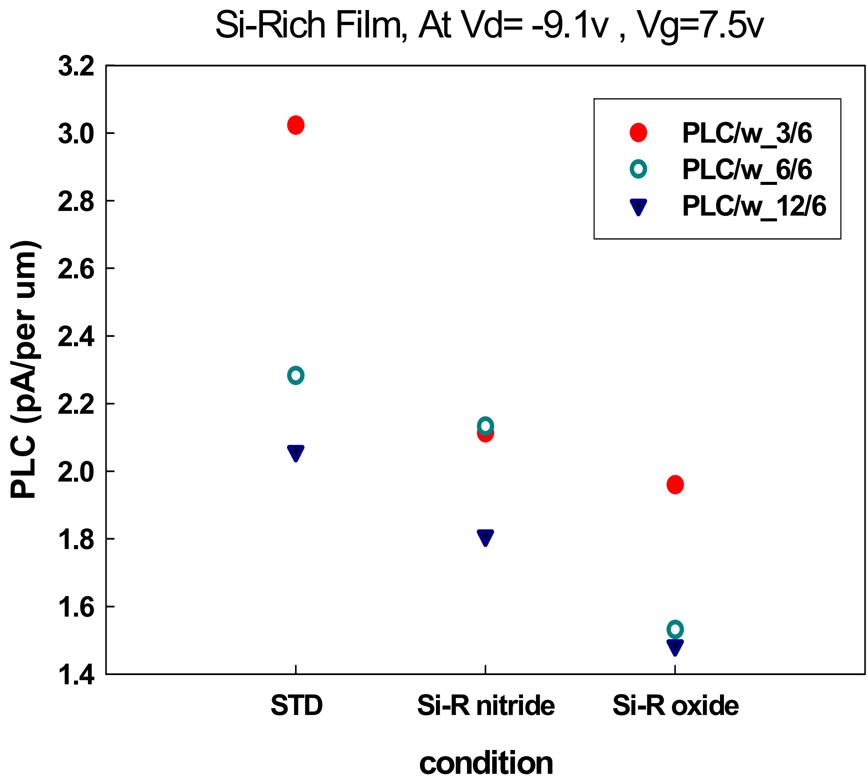

Fig. 3.8 ΔSS of Si-Rich Film

SubThreshold Swing Difference (%) Between Dark and Illumination

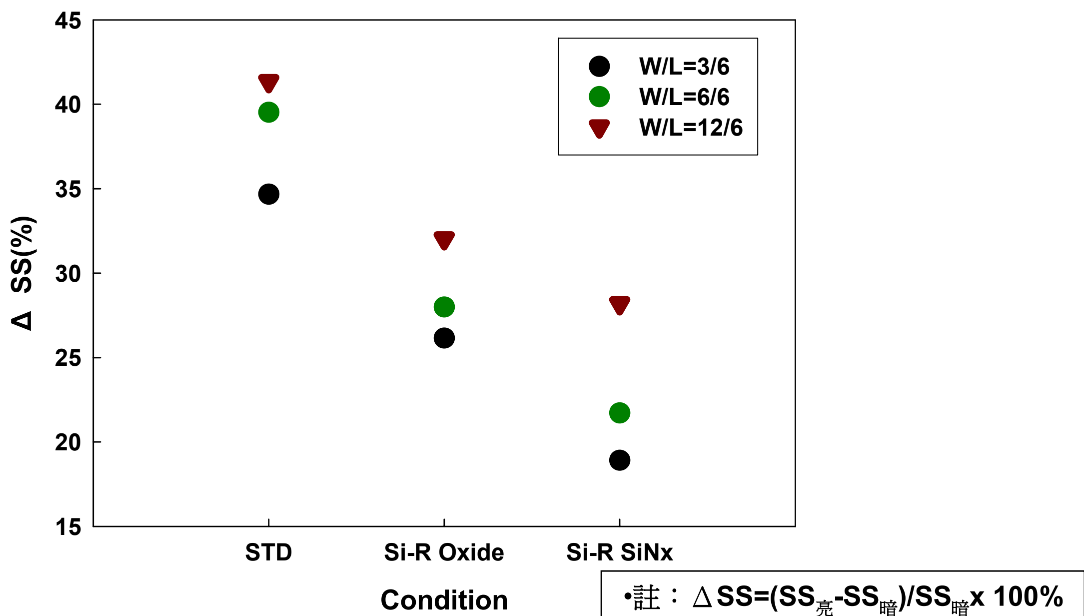

Fig. 3.9 Transmittance of Si-rich (SiNx) film with different thickness.

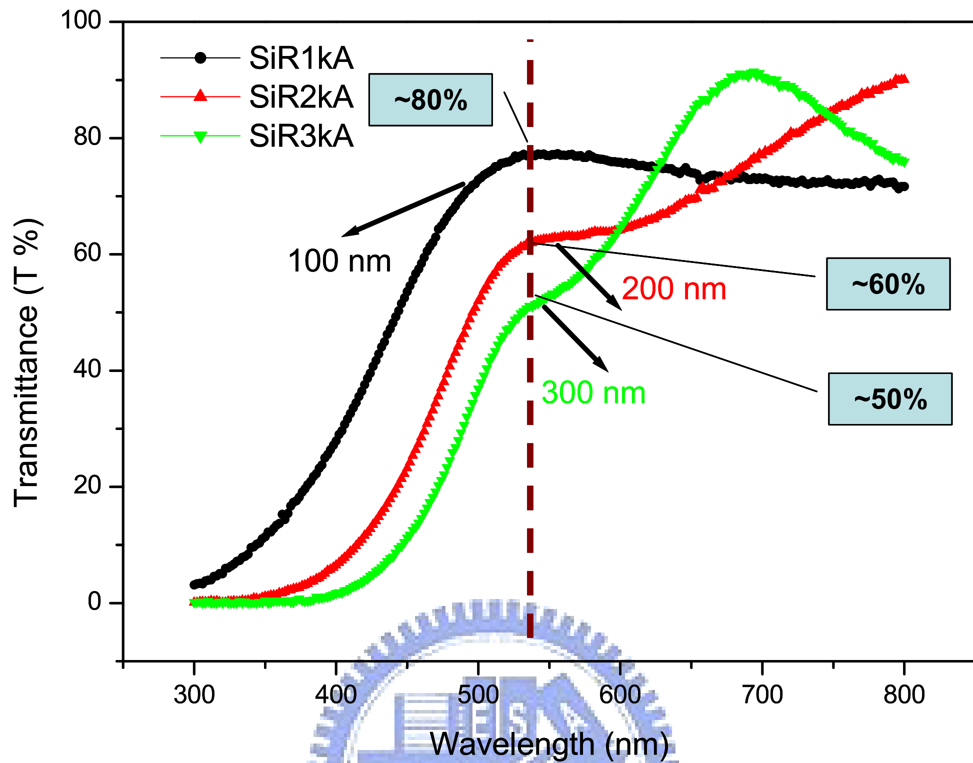

Fig. 3.10a Transmittance of STD and Si-rich film.

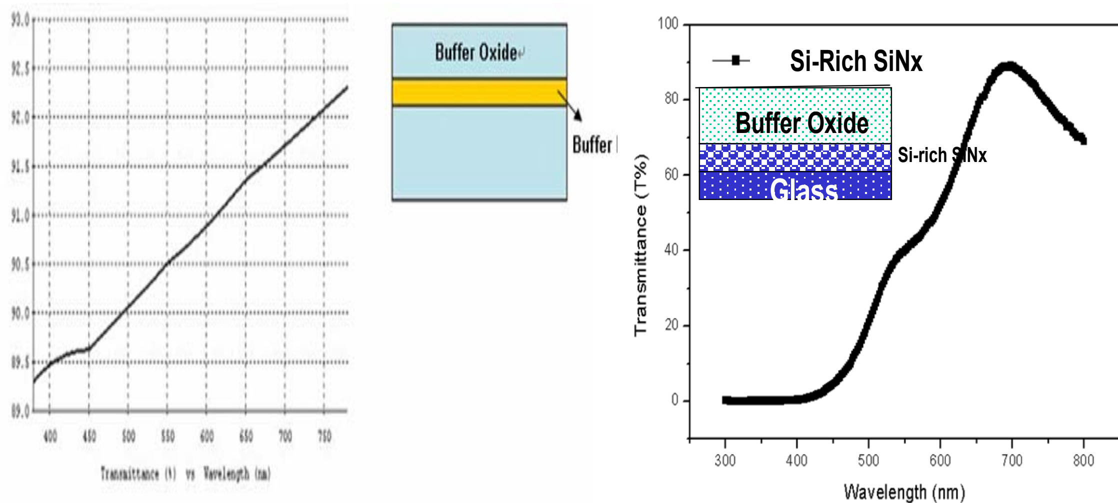

Fig. 3.10b Transmittance Compared : STD with Si-rich Film (2000A).

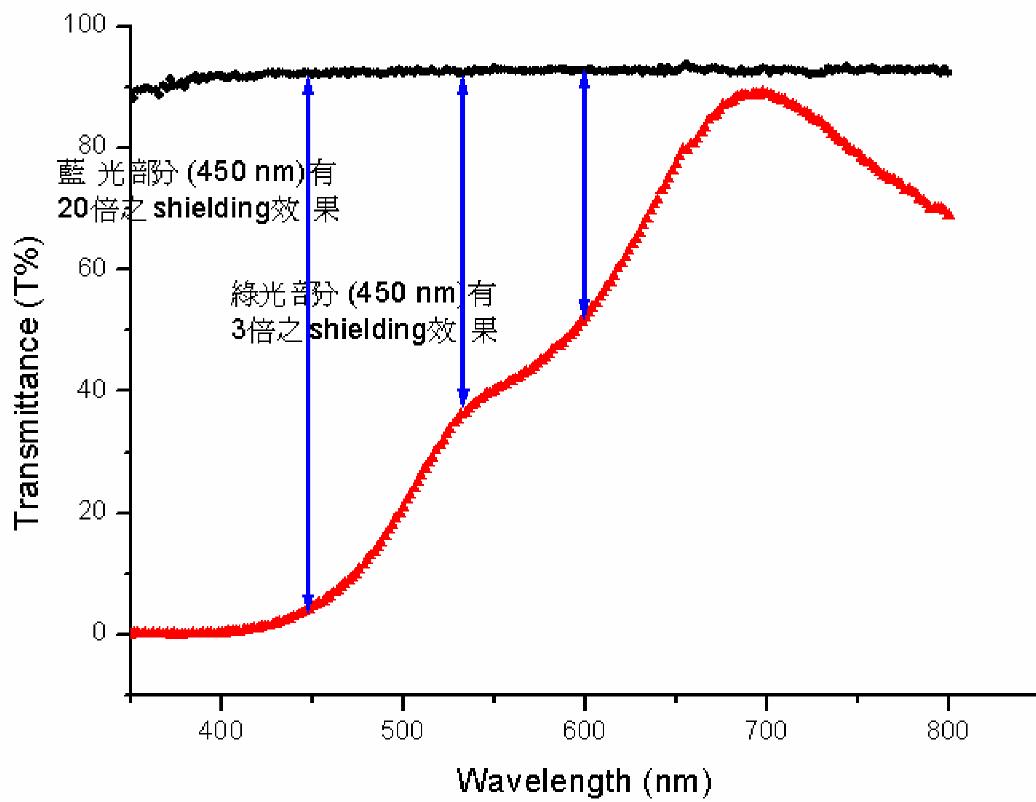

Fig. 3.11

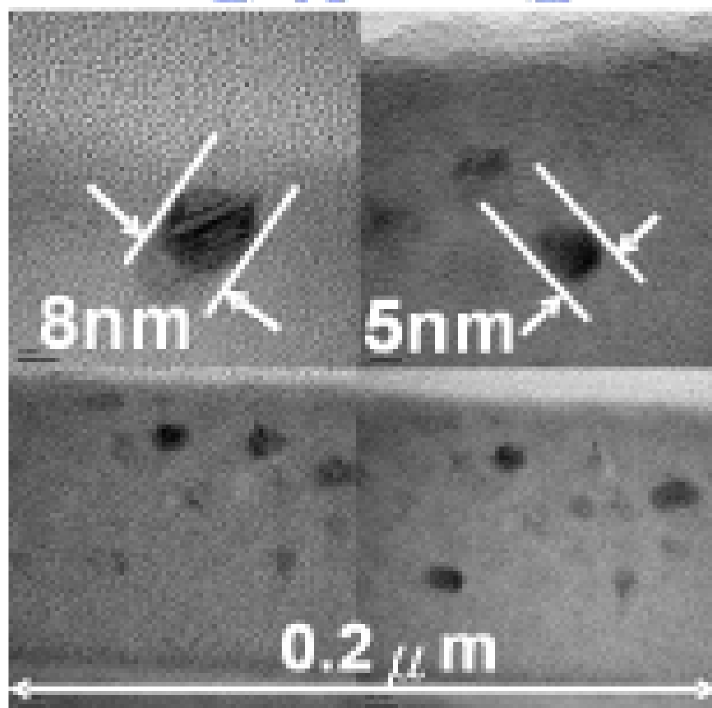

Fig. 3.12 The Etching Profile of Shielding Metal by SEM.

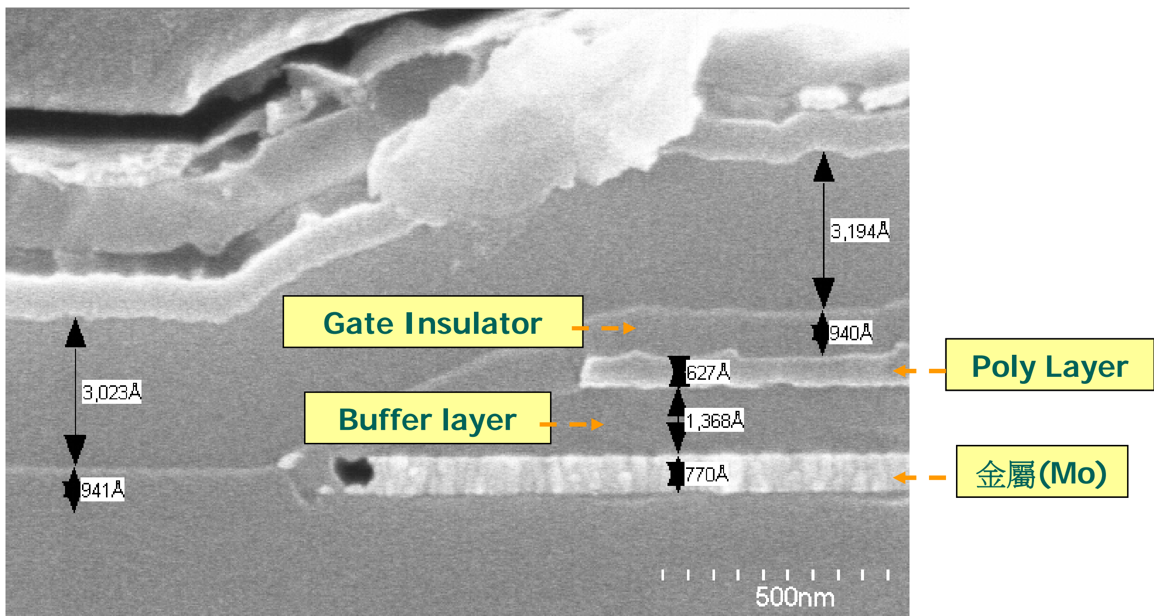

Fig. 3.13 The transfer characterization of shielding metal device.

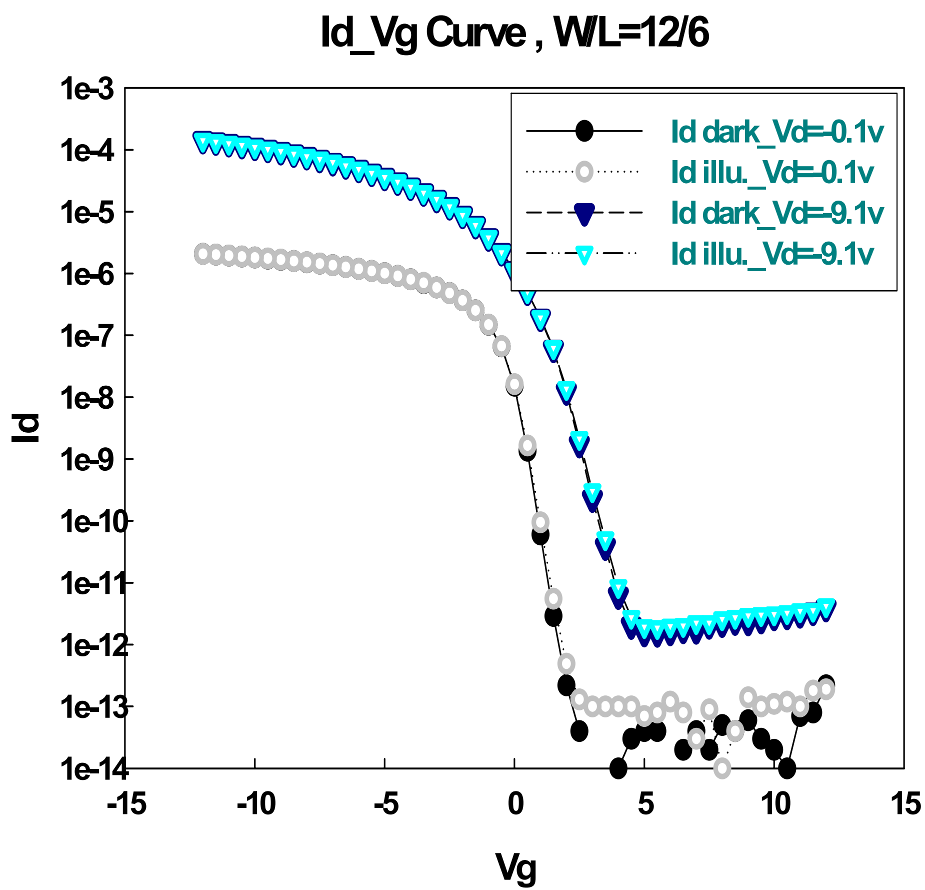

Fig. 3.14 Id_Vg Curve depended on |Vd|.

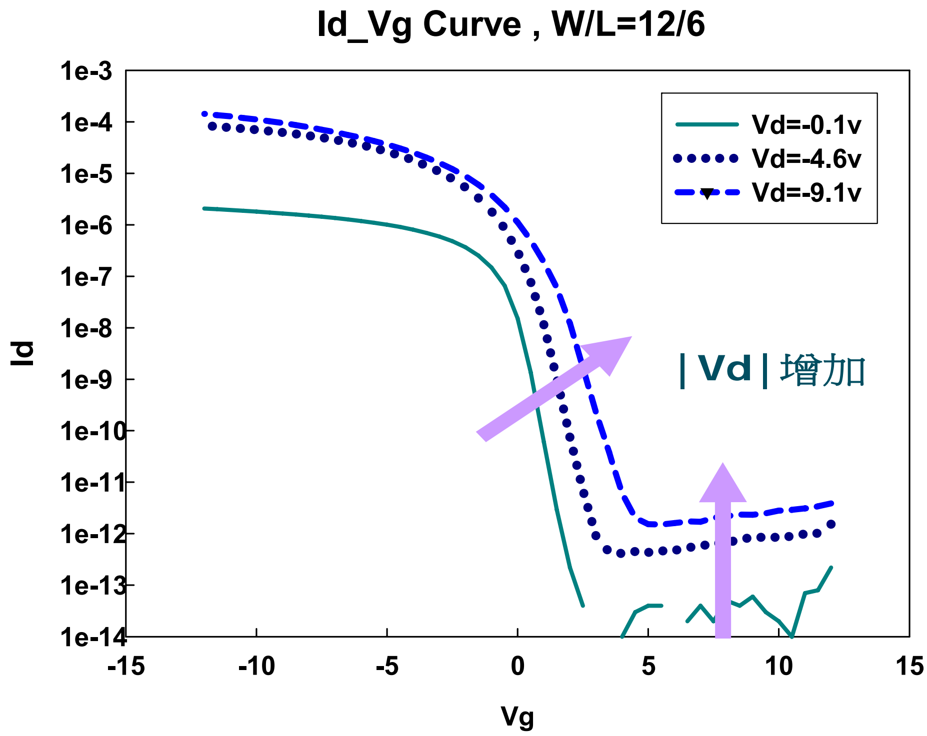

Fig. 3.15 Drain terminal coupling illustration.

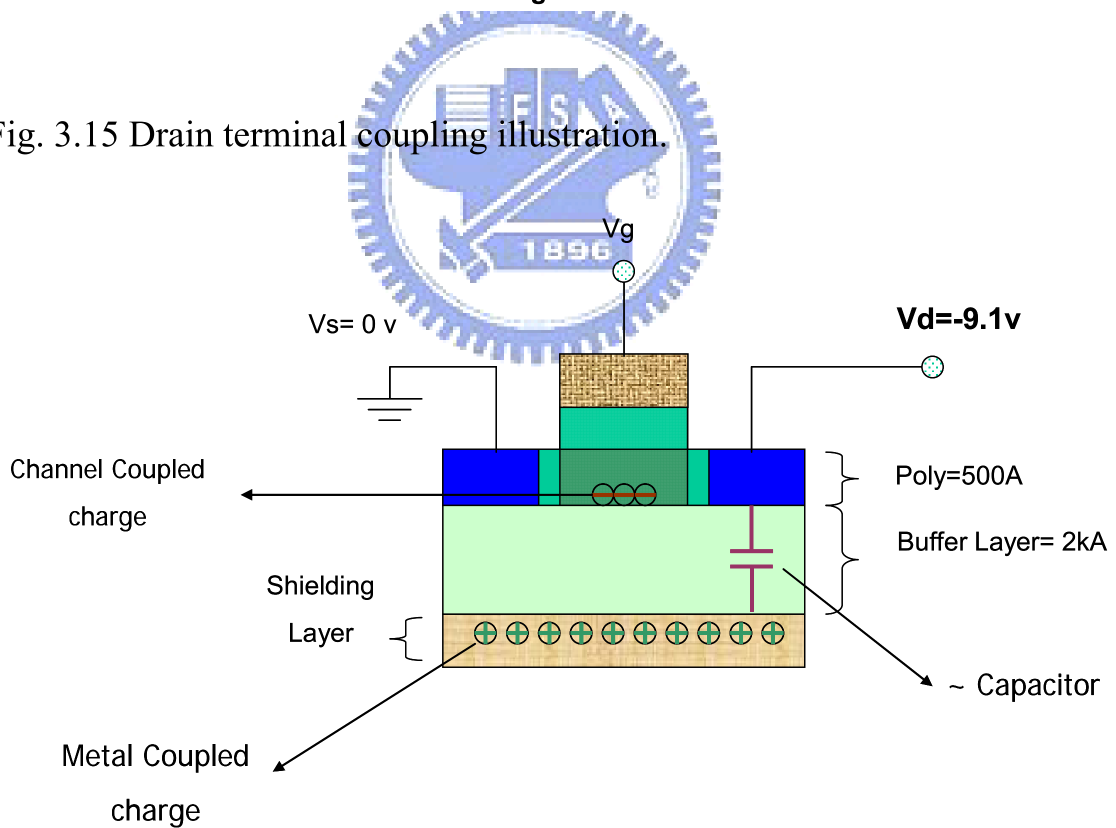

Fig. 3.16 Energy Band Diagram of Coupling Charge

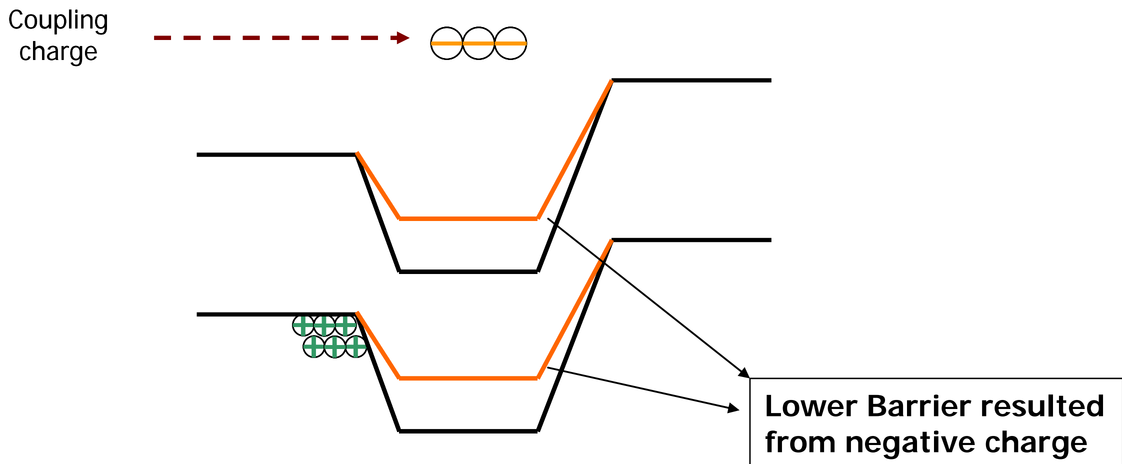

Fig. 3.17 The structure of separating shielding layer