# 國　立　交　通　大　學

## 電子工程學系電子研究所

## 博　士　論　文

# 可移植性數位控制式振盪器及動態頻率計數迴路之研究

# The Study of Portable Digitally Controlled Oscillator and Dynamic Frequency Counting Loop

研究生　：　陳寶龍

指導教授　：　李鎮宜 教授

中華民國九十四年十一月

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研 究 生：陳寶龍　　Student：Pao-Lung Chen

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電子工程學系電子研究所

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# 國　立　交　通　大　學

## 博碩士論文全文電子檔著作權授權書

（提供授權人裝訂於紙本論文書名頁之次頁用）

本授權書所授權之學位論文，為本人於國立交通大學 電子工程 系所 系統 組， 94 學年度第 1 學期取得博士學位之論文。

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## 博碩士紙本論文著作權授權書

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本論文為本人向經濟部智慧局申請專利(未申請者本條款請不予理會)的附件之一，申請文號為：____94119599_____，請將論文延至____年____月____日再公開。

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# 推 薦 函

主旨：推薦電子工程學系博士班研究生陳寶龍，舉行博士班學位口試。

說明：本人所指導之博士班學生陳寶龍，業已通過資格考試，並完成本校電子工程學系電子研究所博士班規定之學科課程及論文研究訓練。陳君主要從事全數位控制式振盪器(DCO)及控制迴路演算法之研究工作，其論文題目「可移植性數位控制式振盪器及動態頻率計數迴路之研究」(The Study of Portable Digitally Controlled Oscillator and Dynamic Frequency Counting Loop) 利用數位控制式壓控變容器來設計 DCO，同時提出動態頻率計數迴路來控制振盪器，及其在高倍數的應用中探討分析，並透過矽晶片驗證改善效能。相關研究成果如下：

期刊論文:

[1] Pao-Lung Chen, Ching-Che Chung and Chen-Yi Lee, "A Novel Digitally-Controlled Varactor for Portable Delay Cell Design," *IEICE Trans. Fundamentals,* Vol. E-87A, pp. 3324-3326, Dec. 2004.

[2] Pao-Lung Chen, Ching-Che Chung and Chen-Yi Lee, "A Portable Digitally-Controlled Oscillator Using Novel Varactors," *IEEE Trans. Circuits and Syst. II, Express Briefs,* Vol. 52, No. 5, pp. 233-237, May 2005.

[3] Pao-Lung Chen and Chen-Yi Lee, "A Standard Cell-Based Frequency Synthesizer with Dynamic Frequency Counting," *accepted and to be published on IEICE Trans. Fundamentals,* Vol. E-88A, Dec. 2005.

研討會論文:

[4] Pao-Lung Chen, and Chen-Yi Lee, "A Novel Structure for Low Power and High Performance Multimedia Processor," *in Proc. DMS'01, The 2001 International Workshops on Multimedia Technologies, Architecture, and Applications,* Sep. 2001, pp. 295 ~ 298.

[5] Pao-Lung Chen, and Chen-Yi Lee, "A Compact Software-Controlled Clock Multiplier for SoC Applications," *in Proc. IEEE 45th MWSCAS,* Aug. 2002, pp. I499-I502.

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投出待審之論文：

[13] Pao-Lung Chen, Ching-Che Chung, Jyh-Neng Yang, and Chen-Yi Lee, "Clock Generation with Cascaded Dynamic Frequency Counting Loops for Wide Multiplication Range Applications," submitted to *IEEE Journal of Solid-State Circuits*.

目前尚有一篇期刊論文正在審查當中。總言之，陳君在過去的研究期間，已滿足本所在課業及研究上的要求，並在團隊研究方面，獲致肯定，因此特以推薦之。

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李 鎮 宜

中 華 民 國 九 十 四 年 十 月

# 國 立 交 通 大 學

## 論文口試委員會審定書

本校電子工程學系電子研究所博士班 陳寶龍 君

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合於博士資格標準、業經本委員會評審認可。

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Date : 2005-11-29

We have carefully read the dissertation entitled The Study of Portable Digitally Controlled Oscillator and Dynamic Frequency Counting Loop

submitted by Pao-Lung Chen in partial fulfillment of the requirements of the degree of DOCTOR OF PHILOSOPHY and recommend its acceptance.

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# 可移植性數位控制式振盪器及動態頻率計數迴路之研究

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## 摘要

現代的系統單晶片(SoC)需要晶片內在的時脈產生器以及產生許多不同的頻率，來提供給其他子系統使用，一般常用鎖相迴路為基礎的時脈產生器來達成此任務。然而，鎖相迴路的迴路參數為了減少抖動量以及保持迴路的穩定度，因而必須依照輸出頻率以及頻率產生倍數來調整，現有類比電路的方式需要較長的設計週期。

本論文從可移植性數位控制式振盪器，動態取樣的迴路控制器，到利用串接式迴路來達成高倍數，提供一個實用的解決方式。具體而言，此種所提出架構的數位控制式振盪器利用反或閘/反及閘的寄生電容差值作為數位控制式壓控變容器，不同型式的數位控制式壓控變容器也加以討論比較。數位控制式壓控變容器能夠提升傳統標準細胞單元中單一緩衝器的時間延遲的極限，在微調上時間解析度能夠依照使用驅動細胞單元的能力及數位控制式壓控變容器的電容差異，作不同的選擇。同時具有較線性的時間解析度相對於使用 OAI-AOI 細胞單元或三態緩衝器矩陣，除此之外，電路佈局圖可以利用自動繞線及擺放的軟體工具完成。

本論文接著提出低成本的動態頻率計數迴路使用變動時間來估算及調整數位控制式振盪器的頻率，傳統相頻器以及可程式化除頻器被數位式比較器及數位控制式振盪器計數器取代，數位控制式振盪器計數器的值可再細分為商數向量及餘數向量，同時，使用臨界值的設立及動態性的取樣時間來解決計數器的取樣量化問題以及提高頻率偵測的解析度，提出的動態頻率計數迴路透過模擬比較及晶片功能驗證。

本論文最後發展串接式動態頻率計數迴路應用在高倍數及低輸入頻率的應用中，所提出的時脈產生器其倍數可從 4 ~ 13888 (其中 5122 cases)，其抖動量值小於輸出時脈週期的 2.8%，最低的輸入頻率為 19.26 仟赫茲到最高輸入頻率為 60 百萬赫茲，其核心面積為 0.16 平方毫米($mm^2$)，當工作在 1.8 伏、378 百萬赫茲時其消耗功率為 15 毫瓦，以上所提出的設計均使用高階應體描述語言，再使用標準細胞單元件庫來合成。提出高解析度之可移植性數位控制式振盪器、態頻率計數迴路和串接式動態頻率計數迴路在 0.35 微米或 0.18 微米的標準元件庫中驗證，此所提出的可移植性數位控制式振盪器、動態頻率計數迴路和串接式動態頻率計數迴路，十分適合在系統整合的應用及系統單晶片中。

# The Study of Portable Digitally Controlled Oscillator and Dynamic Frequency Counting Loop

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# ABSTRACT

Modern system-on-a-chip (SoC) processors often require on-chip clock generation and multiplication to produce several unrelated frequencies for other sub-systems. PLL-based clock generator is a common way of frequency multiplication to accomplish the task. However, the loop parameters must be adjusted to minimize jitter performance and insure stability for each output frequency and multiplication factors. Conventional analog skills suffer from long design cycle.

This dissertation provides a practical solution, from portable digitally controlled oscillator (DCO), dynamic sampling algorithm for loop controller, and a cascaded loop for wide multiplication range. Specifically, the proposed DCO with novel digital controlled varactors (DCV) based on parasitic capacitance difference of NOR/NAND gates can enhance the timing limitations as compared with a single buffer cell. Different types of NOR/NAND gates (2-input or 3-input) for DCV are also investigated. The timing resolution in fine-tuned stage can be decided from different driving cells and capacitance difference of each DCV cell. Thus, a high resolution DCO with better timing linearity as compared with OAI-AOI cell or

tri-state matrix is achieved. The final circuit layout can be generated using an auto placement and routing (APR) tools.

We next propose a dynamic counting loop (DFC) with low cost that uses variable time period to estimate and tune the frequency DCO. Conventional phase-frequency detector (PFD) and programmable divider are replaced with a digital arithmetic comparator and a DCO timing counter. The value in the DCO timing counter is separated into quotient and remainder vectors. Also, a threshold region is set and by using dynamic sampling period to solve the quantization effect of counter sampling and enhance resolution of frequency detection. The proposed algorithm was simulated and verified with test chips.

Finally, we develop a cascaded DFC loops that can be applied in wide multiplication ranges applications with low input frequency. The proposed clock generator achieves a multiplication ranges from 4 to 13888 (with 5122 cases) with output peak-to-peak jitter less than 2.8% of clock period. The lowest input frequency is 19.26KHz and the maximum input frequency is 60MHz. A test chip for the proposed clock generator is fabricated in 0.18 μm CMOS process with core area of 0.16 $mm^2$. Power consumption is 15 mW @ 378 MHz with 1.8 V supply voltage. The above designs are designed in gate-level Hardware Description Language (HDL) codes and synthesized for a target cell library. The proposed portable DCO, DFC loop, and a cascaded DFC loops have been verified on silicon using 0.35-μm or 0.18-μm CMOS cell library. As a result, the proposed portable DCO, DFC loop and cascaded DFC loops are well-suited for system-level integration and SoC applications.

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# Chapter 1

# Introduction

## 1.1 Thesis Background

Traditionally, phase locked loops (PLL) based clock generators for microprocessor are the common way of frequency multiplication from a low-frequency reference clock, typically from quartz oscillator [1-13]. As VLSI technology grows up rapidly, the advance of semiconductor process enables the successful realization of system-on-a-chip (SoC) [14-17,21,23-24]. Modern SoC processors integrate both analog and digital real-time functions, such as a digital signal processor (DSP), digital-to-analog converter (DAC), audio, video, and I/O interface protocols. An off-chip clock costs power to generate and to distribute on the PC-board. In addition, the ability to oscillate at different frequencies reduces costs by eliminating the need for additional oscillators to a system. Such applications often require on-chip clock generation and multiplication to produce several unrelated frequencies for digital signal processing, I/O interfaces, as well as sampled analog sub-systems [18-19].

One solution is to create one PLL-based clock generator running at a high frequency that can then be divided down to obtain all the desired frequencies [20]. The disadvantage of this approach is the high power consumption and stringent jitter requirements. Another approach is to have a dedicated PLL for each clock domain [21]. This solution is very costly in term of power and area.

The diversity of SoC applications has led to diversity in operating frequencies and

multiplication factors required from PLLs. The loop parameters must be adjusted to minimize jitter performance and to insure stability for each PLL output frequency and multiplication factors. Providing ample flexibility for a variety of applications is a big challenge for PLL design. The design of PLL-based clock generator is a trade-off among jitter performance, frequency/phase resolution, lock-in time, power consumption, area-cost, circuit complexity and design time. It often needs to redesign the PLL for target applications. If a wide-range PLL is designed for SoC applications, it can be used in more modules without modify it. However, this scheme may waste unnecessary area cost and power consumption due to the requirement of wide-range operation. Thus, it is a challenge task to design it based on conventional analog skill.

In addition, most PLL design use mixed signal and full custom design techniques, which can not be fully integrated in digital environment. Due to time-to-market issue, the design cycle remains the same or even shorter. Thus in System-on-a-Chip (SoC) designs [22], each module had better to be reusable and process portable, so that the total design time can be reduced. As a result, how to design a synthesizer clock generator in an efficient way becomes more important.

## *1.2 Thesis Motivation*

The all-digital PLLs have several advantages over their analog counterparts. Firstly, traditional analog loop filter costs a lot of chip areas. Using digital loop filters gives benefits such as robustness against noise, and also the ability to design higher order filters without much extra power consumption and area penalty. Secondly, analog component are vulnerable to DC offset and drift phenomena that are not present in equivalent digital implementations [35]. Furthermore, the loop dynamics of analog PLLs are quite sensitive to process technology scaling, whereas the behavior of digital logic remains unchanged with scaling; this

requires much more significant redesign effort to migrate analog PLLs to a new technology node than is required for all-digital PLLs.

Moreover, power consumption is extreme concern for portable, battery-powered, computing system, as power dissipation relates directly to battery life. As a result, many manufactures are reducing the power supply voltage requirements of the integrated circuits, particularly those that are especially adapted for portable computing system [36]. However, reduction in power supply voltage applied to analog circuitry, such as analog and digital PLLs, does not reduce the power dissipated by these circuits. Additionally, reduction in power supply voltage to analog circuits renders the design of robust circuit much more difficult.

For these reason, PLLs in which digital techniques are used in not only the phase detector, but also in the loop filter and the controllable oscillator, are very attractive to designers. All-digital cell-based approach is preferred for SoC applications [44-50]. It can reduce significantly both design time and design complexity by using Verilog (or VHDL) hardware-description language and the final circuit layout to be generated by using an auto placement and routing (APR) tools.

A production SoC with high-performance audio/video media networking processor as shown in Fig 1.1 has successfully applied four standard cell-based digitally controlled oscillators (DCO) [57] to replace two external analog audio PLLs and two external quartz oscillators [23-24]. By saving two external analog PLLs, 4 I/O pins (2 per PLL) are saved. Another two I/O pins for connecting quartz oscillators are also reduced. However, due to the limitations of standard cell-based design, it is difficult to achieve a low jitter, low-power, and high resolution all-digital cell-based clock generator [45-50,57]. Thus, how to overcome the limitations of standard cells to build up a high resolution DCO with better linearity and less power consumption, and propose new control algorithm for clock generator are the important design challenges for our research.

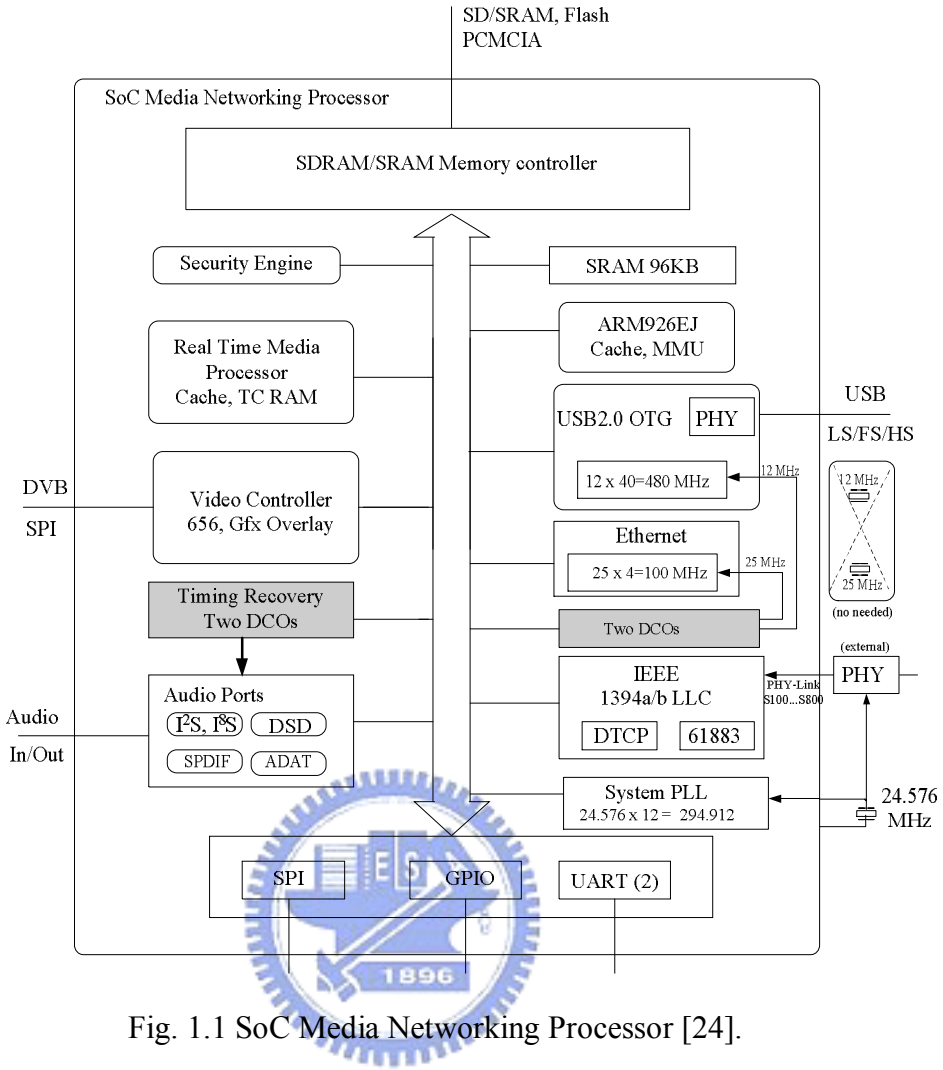



Fig. 1.1 SoC Media Networking Processor [24].

## *1.3 Thesis Contribution*

In this dissertation, we address the issue of portable digitally controlled oscillator (DCO) and propose dynamic sampling period algorithm to enhance frequency detection. In addition, a cascade dynamic frequency counting loops for wide multiplication application is developed. The contributions are listed as follows:

- **Portable Digitally Controlled Oscillator with Novel Varactors**

In this thesis, we first present a portable digitally controlled oscillator (DCO) by using two-input NOR gates as a digitally controlled varactor (DCV) in fine-tuning delay cell design.

This novel varactor uses the parasitic capacitances difference of NOR gates under different digital control inputs to establish a digitally controlled varactor. Thus proposed DCO can improve delay resolution 256 times better than a single buffer design. This study also examines different types of NOR/NAND gates (2-input or 3-input) for DCV. The final circuit layout can be generated using an auto placement and routing (APR) tools. A test chip demonstrates that LSB resolution of the DCO can be improved to averaged 1.55 ps with standard 0.35-μm 2P4M CMOS digital cell library. The proposed DCO has good performance in terms of fine resolution, testability, and short design turn-around cycle compared with conventional DCO designs.

## ■ A New Algorithm with Dynamic Frequency Counting Loop

Second, a new algorithm with dynamic frequency counting (DFC) that multiplying input reference frequency by N times is presented. The DFC loop which uses variable time period to estimate and tune the frequency of digitally controlled oscillator (DCO) enhances the resolution of frequency detection. One up counter serves as variable timer and another DCO timing counter acts as frequency estimator. Conventional phase-frequency detector (PFD) thus is replaced with a digital arithmetic comparator to yield a simple circuit structure. The proposed algorithm was simulated and compared with other method. Then, the performances were measured from 0.35-μm and 0.18-um chips.

## ■ Cascaded DFC Loops for Wide Range Multiplication Applications

Finally, a clock generator with cascaded dynamic frequency counting (DFC) loops for wide multiplication range applications is presented. The loop stability can be retained by cascading two DFC loops when multiplication factor (N) is large. The design complexity is tremendously reduced without using the analog component. The proposed clock generator is fabricated in 0.18-μm CMOS process with core area of 0.16mm$^2$. Experimental results of the

clock generator are given in this chapter.

## *1.4 Thesis Organization*

The organization of this thesis is as follows: In chapter 1, we introduce that different clock domains are required in a SoC chip. Using portable clock generator to replace conventional PLL is feasible. For the rest of this dissertation is organized as follows.

In chapter 2, we give an overview of PLL related techniques for clock generator. Properties of analog, digital PLL as well as charge-pump PLL are addressed. Then, all-digital PLL with different DCO approaches are discussed. The design trade-off of clock generator with different PLL architecture is also investigated.

In chapter 3, we first introduce the fundamentals of digitally controlled oscillator. We also introduce different approaches to enhance the fine tune solution of DCO. Then, we focus on the operation of digitally controlled varactors with two-input or three-input NOR/NAND gates designs. Then, we apply the DCV as fine tune cell to build high resolution digitally controlled oscillator. A detailed description of the circuits and experimental results are given.

In chapter 4, we describe a dynamic sampling technique to enhance the resolution of frequency detection by using simple structure. Detailed algorithm and structure of the loop are then discussed. Then, the proposed algorithm was verified in 0.35-um and 0.18-um.

In chapter 5, we utilize the dynamic sampling techniques for wide range multiplication applications by cascade loops. The multiplication factors range from 4 to 13888 (224 x 62). The peak-to-peak jitter is less than 2.8% of output clock period. Then, we talk how to design the DCO in each loop as well as the loop parameters. Finally, we discuss the experiment results and the overflow issue.

In chapter 6, some concluding remarks will be derived from this research. Finally, we describe several design issues that needed to be further explored in the near future.

# Chapter 2

# Overview of Clock Generators with Phase Locked Loop (PLL)

As shown in chapter 1, numerous applications, such as video graphics card, microprocessor and telecommunication system, require a clock synthesizer. Quartz oscillators frequently require conversion when operating at low frequency. Several methods exist for realizing frequency multiplication: phase locked loop (PLL) [1-13], delay locked loop (DLL) [25-32], and direct digital synthesis (DDS) in [33]. The basic concept of DLL is similar with PLL. The major difference is the voltage controlled delay line (VCDL) in DLL and voltage controlled oscillator (VCO) in PLL [68]. Each of these methods has advantages and disadvantages for frequency multiplication. DLL approach may offer better jitter performance than PLL approach because the noise induced by the power supply or substrate noise disappears at the end of the delay line. However, DLL-based method is not suitable for wide multiplication range applications. The direct digital synthesis (DDS) in [33] applied accumulator and D/A converter mechanism for frequency synthesis. Therefore, we only focus on the PLL approach in this work.

The organization of this chapter is as follows. Section 2.1 describes the preliminary knowledge of analog PLL and charge pump PLL. Basics of all-digital PLL and standard cell-based approach are discussed in section 2.2. Design trade-off in different PLL architecture is discussed in section 2.3.

## 2.1 PLL Basics

PLL-based clock generator has been widely used in the industry. In addition, PLL-based approach is the most suitable for integrating into a standard CMOS process. Phase-locked loops are originally of analog nature [1-3]. The operation principle is summarized in this section and the steps towards charge pump PLL are described in the subsequent sections.

### 2.1.1 Analog PLL

The PLL's characteristics are determined by the characteristics of phase detector, voltage controlled oscillator and low pass filter. In [1-3] indicated two factors will influence the performance, one is the phase error – the difference between the input phase and output phase, and another is the frequency range – what range over which it will acquire lock. As a result, PLL can be regarded as a tracking phase system. An analog PLL consist of the three main building blocks as shown in Fig. 2.1.

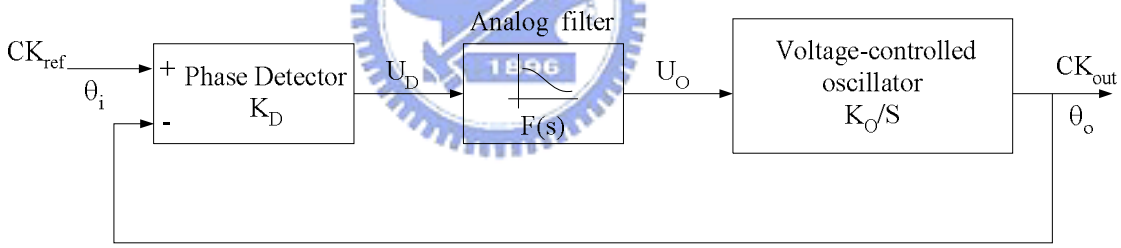



Fig. 2.1. Block diagram of an analog PLL.

- Phase detector: It compares the phase of the input signal (reference signal) with the phase of the feedback signal. The output of the PD is ideally proportional to the phase difference $\theta_e$ .

$$U_D(s) = K_D(\theta_i(s) - \theta_o(s)) = K_D\,\theta_e(s) \qquad (2.1)$$

where $K_D$ is the phase detector gain in [V/rad] and $\theta_i$ and $\theta_o$ are the phase of the input and output signals respectively. If the analog phase detector like multiplier is replaced with three-state phase frequency detector (PFD) as shown in Fig. 2.2 (a), then it is defined as digital PLL in [3]. Fig. 2.2 (b) illustrates the PFD state diagram including

Down, Zero, and Up states. The PFD detects not only the phase difference but also the frequency difference between its two inputs. During the phase-locking process the relative time that the PFD remains in `Down' or `Up' state represents the phase error. If the PLL is locked, the output of '$Q_A$' and '$Q_B$' are activated only during extremely short time spans. However, the practical PFD circuit suffers from the dead-zone problem [3].

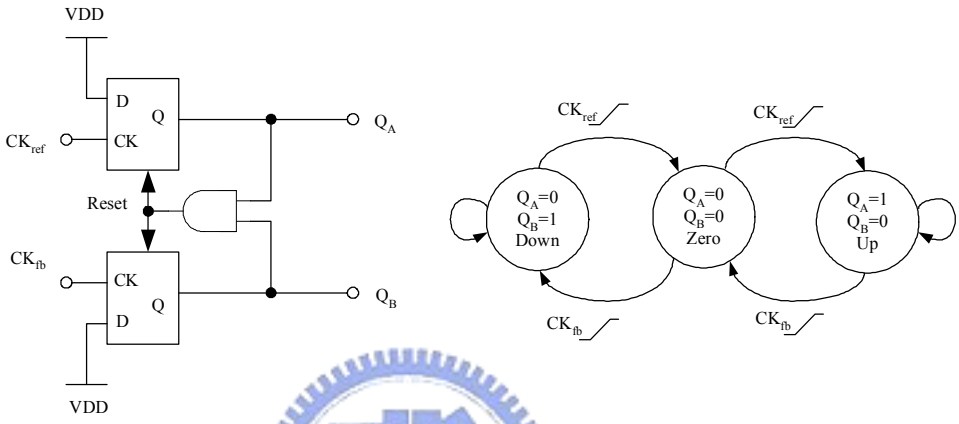



Fig. 2.2. (a) Three state phase frequency detector. (b) PFD state diagram.

- Voltage controlled oscillator (VCO): Translates the filter output into a frequency. Due to the transformation of phase information into a frequency, it has the characteristic of an integrator with gain $K_0$ [rad/sV].

$$\theta_o(s) = \frac{U_O(s) \cdot K_o}{s}. \tag{2.2}$$

- Low pass filter (LPF) : Filters the output voltage of the phase detector with the transfer function F(s) can be expressed in

$$U_o(s) = U_D(s)F(s). \tag{2.3}$$

The loop filter reduces the AC loop gain and the loop bandwidth to remove the frequency that we do not want in the loop. The overall transfer function of the closed loop becomes

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_D K_o F(s)}{s + K_D K_o F(s)}. \tag{2.4}$$

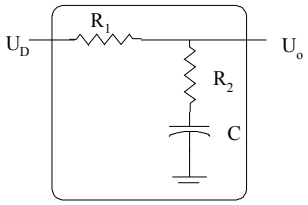



Fig. 2.3. A first order loop filter with RC implementation.

The characteristics of the LPF are important which they determines lot of parameters of the loop. Three parameters for engineer to choice: (1) the loop gain, (2) the placement of the zeros, and (3) the placement of the poles that we need. A first order loop filter is depicted in Fig. 2.2 that has the following transfer function:

$$F(s)= \frac{1+sR_2C}{1+s(R_1C+R_2C)}. \tag{2.5}$$

The overall loop transfer function is a second order loop with low-pass characteristic. The natural frequency is

$$\omega_n = \sqrt{\frac{K_D K_O}{R_1C+R_2C}} \tag{2.6}$$

and the damping factor becomes

$$\zeta = \frac{\omega_n}{2}(R_2C+\frac{1}{K_D K_O}). \tag{2.7}$$

A PLL uses a first order loop filter is therefore a second order system. Figure 2.4 shows the transfer functions of a second order loop for various damping factors $\zeta$.

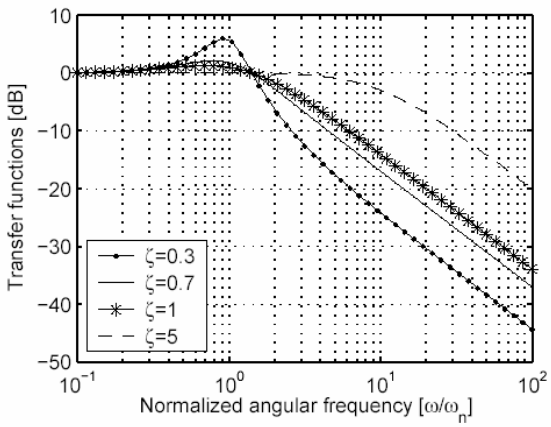



Fig. 2.4. Magnitude response of a second order loop transfer function.

## 2.1.2 Charge Pump PLL

To trade-offs between $\zeta$, $\omega_n$, and the phase error, the analog/digital PLLs suffer from a critical drawback: limited acquisition range. A charge pump (CP) PLL was proposed in [34] to solve this problem as shown in Fig. 2.5. A charge pump consists of two switched current sources that pump charge into or out of the loop filter according to two logical inputs. The three state PFD detects phase or frequency differences, and activates the charge pump accordingly. The gain of PFD/CP combination is infinite, which can not achieved by the digital PLL. When in lock, the PLL generates the output frequency that is N times the reference frequency. The system is second order closed loop response because the integration of charge on the loop filter and the integration of phase.

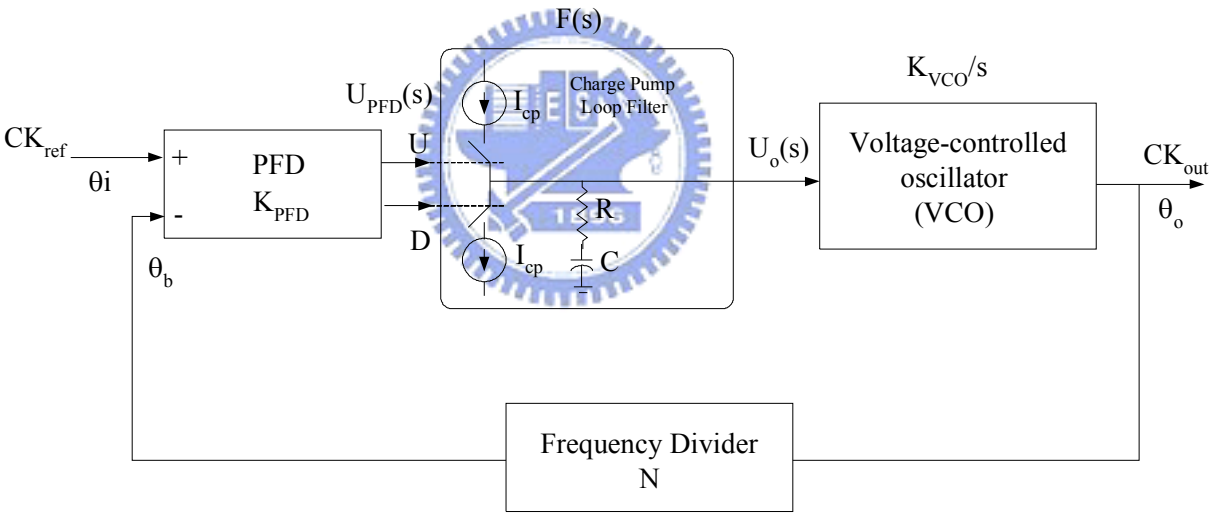



Fig. 2.5. Block diagram of a charge pump PLL.

The loop bandwidth (rad/s) of a CP-PLL is given by

$$\omega_n = \sqrt{\frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot N \cdot C}} \tag{2.8}$$

and the damping factor can be described in

$$\zeta = \frac{1}{2} \cdot \omega_n \cdot R \cdot C \,. \tag{2.9}$$

The loop bandwidth characterizes the response rate of the system and the damping factor characterizes its stability. Ideally, $\omega_n$ should scale with the $CK_{ref}$ to handle a wide frequency range. However, the $\omega_n$ is influenced by the divider ratio as indicated in (2.8). This creates a challenge for PLL with wide range N.

## *2.2 All-Digital PLL*

The all-digital phase lock loop (ADPLL) has gained increased attention in recent years. All analog building blocks are replaced with digital representations in all-digital PLLs (ADPLL). The term "all-digital PLL" is used for a particular reasons: all signals within this PLL are digital values; no analog level is used. Many different ADPLL are discussed in the literature [69]. In general, there are two types of ADPLL depending on the DCO clock source: (1) to use fixed high-speed clock as indicated in [2,15,43,57] to form a DCO, (2) to synthesis clock internal based on a DCO circuit as [37-39, 42]. Furthermore, the standard cell-based implementation of DCO will also be discussed because of its popularity [50].

### 2.2.1 DCO with Fixed High-Speed Clock

Fig. 2.6 shows the proposed ADPLL with fixed high-speed clock and output accumulator in [3].

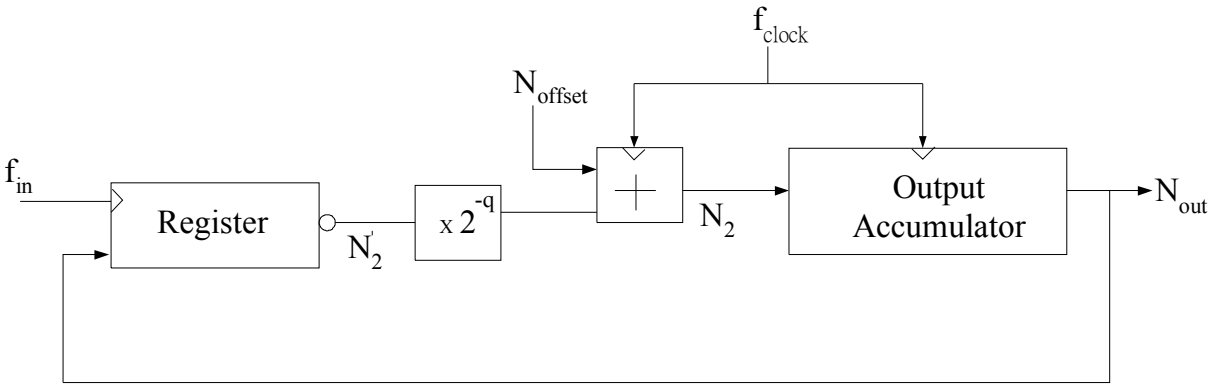



Fig. 2.6. ADPLL with fixed high-speed clock to form DCO in [3].

The input is a binary $f_{in}$, and the output is to be a number that has an average repetition rate of $f_{in}$ but follows the input with a closeness that depends on the loop parameters. The DCO consists of an accumulator and high speed clock $f_{clock}$. Its output is a number that changes each clock cycle by an amount equal to its input $N_2$. Each time the output accumulator reaches its capacity $N_{max}$, it recycles to 0. Thus, one cycle is represented by $N_{max}$, and the output phase of the output accumulator is

$$\Phi_{out} = (N_{out} / N_{max}) \text{ cycles} \tag{2.10}$$

The output frequency is

$$f_{out} = \Delta\Phi_{out} / \Delta t = (N_2 / N_{max}) \cdot f_{clock} \tag{2.11}$$

since the output is incremented by $N_2$ each cycle of the output accumulator. The register stores the value of $N_{out}$ at each cycle of the input signal $f_{in}$. The register thus functions as a phase detector and zero-order hold. Then, the phase error will be inversed and multiply with $2^{-q}$. There are two sampling processes occurring in the simple loop, one in the register at $f_{in}$ and one in the output accumulator at $f_{clock}$. The stability of this simple loop can be represented by using z-transform. The closed loop of Fig. 2.6 is

$$H(z) = \frac{K}{z - 1 + K}, \tag{2.12}$$

where

$$K = 2^{-q} (f_{clock} / f_{in}). \tag{2.13}$$

The open and closed loop poles for this loop are shown Fig. The closed loop pole locus begins at the open loop pole when K=0 and moves along the real axis as K increases. The beset response will be in the center of the unit circle where K=1. The closed loop is unstable when K is larger than 2.

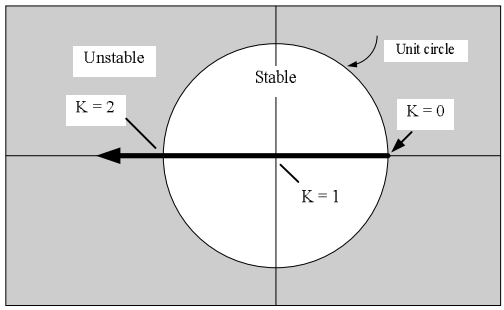



Fig. 2.7. Z-plane representation of the loop [3].

## 2.2.2 Direct DCO Synthesis Clock

If the high-speed clock is available, such as in SoC, and the target operation's speed is not very high, then DCO with fixed high-speed clock can be the choice. However, it may consume large power due to high-speed clock operation. The external high-speed clock is not always feasible which require extra pin and another high-speed quartz oscillator when the target application is for on-chip clock multiplication (factor > 1). In recent years, ADPLL of type (2) is more popular and even applied frequency synthesis for RF wireless application [40-41,54]. An ADPLL with high resolution DCO as shown in Fig. 2.8 was first proposed in [37] as clock generator for microprocessor that did not require external fixed high-speed clock as compared with Fig. 2.6.

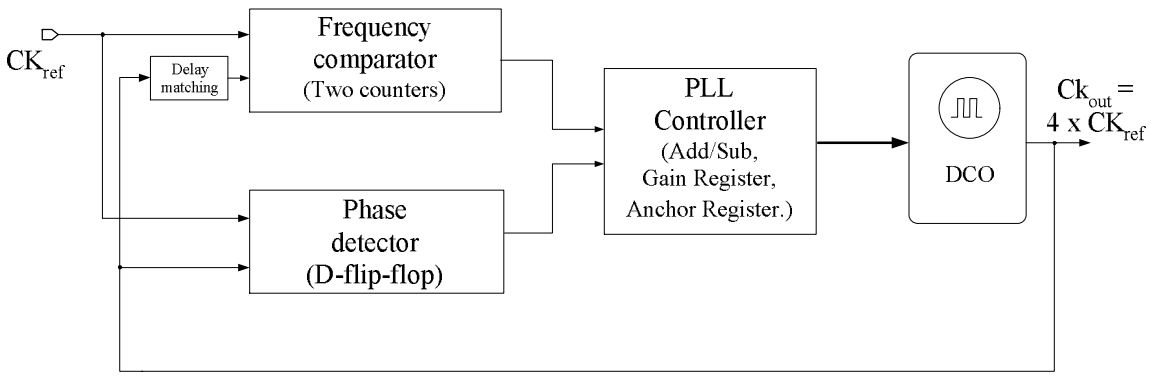



Figure 2.8. ADPLL with direct DCO synthesis clock [37].

This ADPLL achieved fast locking within 50 reference clock cycles as compared with conventional charge pump PLL-based clock generator. The fast locking time was achieved with modified binary searching algorithm. It separated the frequency acquisition and phase acquisition that did not utilize the three-state PFD and frequency divider. A high-resolution frequency comparator with matching delay line was utilized to achieve frequency accuracy under 0.1% error ratio. A high-resolution ring oscillator with 16-bit control word was implemented to generate the accurate frequency output. The DCO will be turn-on and disable after 30-40 iterations for frequency comparison. An anchor register is needed to store the baseline frequency. After frequency acquisition is completed, the PLL starts to trace the phase of the reference clock. The phase tracking process was performed with a phase control algorithm and a phase detector. It contains phase gain controller and two series-connected, edge-triggered D flip-flops. The phase acquisition process can be finished within 10 reference clock cycles. After the frequency acquisition and phase acquisition, the ADPLL enters phase and frequency tracking process. Many ADPLL variants follow this ADPLL approach, such as [38-39]. However, the cost of this chip area is extremely high due to DCO. Another small area DCO was proposed in [38]. Those DCO designs were required to be with full-custom layout. The specific transistor sizing of DCO comes to be with changes in design specifications.

### 2.2.3 Standard Cell-Based DCO

A standard cell-based implementation of all-digital clock generator [50] based on structure of digital PLL that can be divided into five main parts: PFD, loop controller, loop filter, DCO, and programmable divider as shown in Fig 2.9. The key issue is that all of the elements are designed form standard cell library without any fully-custom layout.

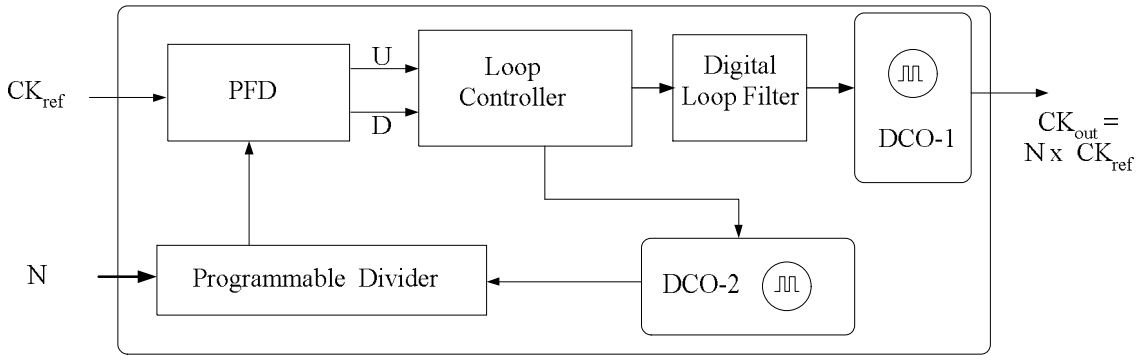



Fig. 2.9. Functional block of ADPLL in [50].

The function of the programmable divider is simply to slow the DCO output frequency for comparison. The loop controller generates the digital commands to track the DCO output clock based on the results from PFD. Two extra digital pulse amplifier circuits are required to minimize the dead zone of PFD, as indicated in [50]. However, the control code may have small variations due to the following factors: PFD's dead zone, DCO's finite resolution. An average loop filter is necessary to filter out the rippling and produce a smoother digital controlled word with less jumping. Additionally, two DCOs are required for low output jitter to reduce the noise and jitter associated with input reference. This requirement leads to a highly complex and expensive design. Therefore, this structure was effectively creating a frequency locked loop. The cell-based ADPLL of Fig. 2.9 can be modeled as shown in Fig. 2.10.

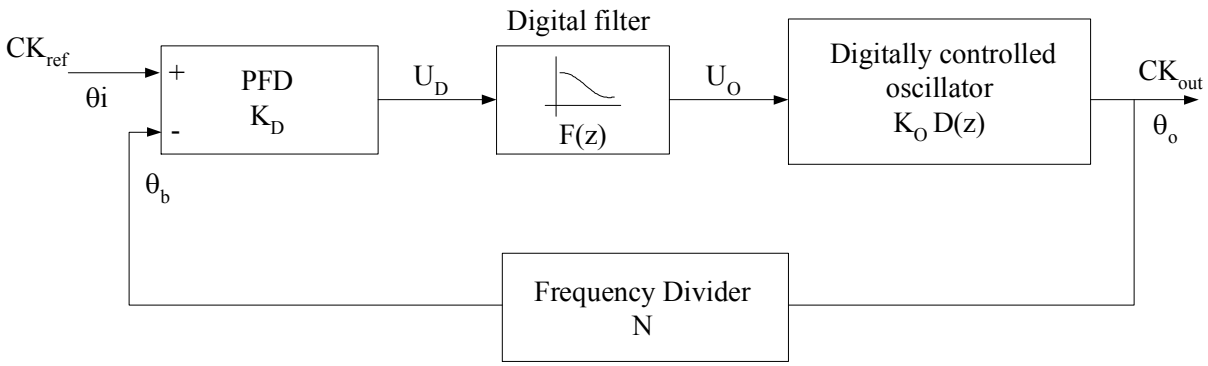



Fig. 2.10. Signal block diagram of standard cell-based all-digital PLL.

The closed-loop transfer function of Fig. 2.10 is

$$H(z)=\frac{\theta_o(z)}{\theta_i(z)}=\frac{N\cdot K_D\cdot K_O\cdot F(z)\cdot D(z)}{N+K_D\cdot K_O\cdot F(z)\cdot D(z)} \quad (2.12)$$

The stability of the closed loop transfer function depending on $K_D$, $K_O$, N and $F(z)$. Different types of loop filter are discussed in [49].

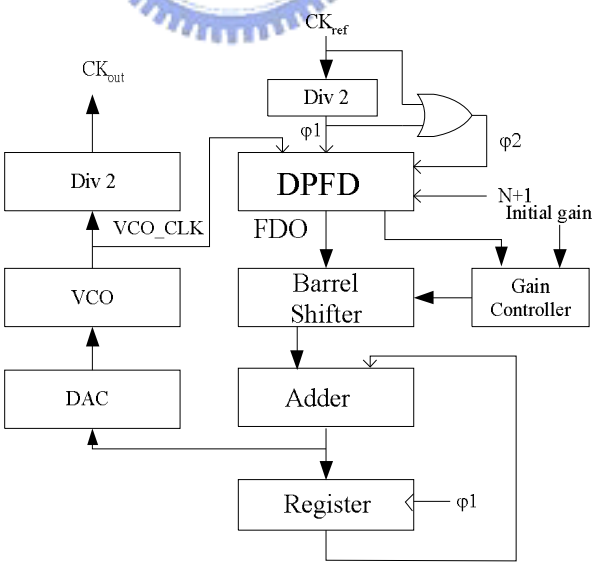
## 2.3 Clock Generator Trade-off with Different PLL Architectures

PLL-based clock generator is a trade-off lock-in time, area cost, power consumption, jitter performance, circuit complexity and design time. Thus, it is very challenge to design one PLL clock generator for all applications. The conventional charge pump PLL-based clock generators for microprocessor as indicated [6,8-10] that can accomplish good jitter performance as well as low power consumption. However, the on-chip loop filter occupied a lot of chip area and slow lock-in time. Furthermore, it required long design time due to circuit complexity. Therefore, those clock generators are also only suitable specific application which can not be applied a variety of multiplication ranges. In order to handle wide multiplication range, Ref. [11] utilized a scalable charge-pump current to compensate for the damping factor and bandwidth dependence of the multiplication factor. The multiplication factor (N) of [11] can range from 1 to 4096. However the proposed architecture leads to design complexity and also has large die area due to the 12-bit programmable 1/N current mirror.

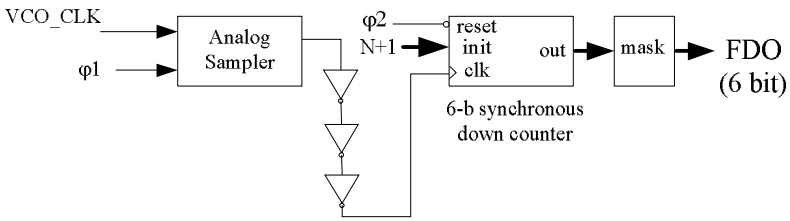
In conventional PLL-based clock generator design, fast acquisition requires tuning the free-running frequency near the desired frequency in advance or to increase the loop bandwidth. The exact VCO tuning range is not easy to be achieved since there always has

process variations, voltage variation, and temperature variations (PVT variations). A Discriminator-Aided Phase Detector (DAPD) in [64] can be applied to reduce the PLL pull-in time and enhance the switching speed. This makes the charge pump circuits more complex, and the loop filter is off-chip.

A Digital Phase-Frequency Detector (DPFD) as indicated in Fig. 2.11 is proposed in [62] to convert the frequency directly to the digital value, and then change the gain for VCO control adaptively. It required a complex D/A converter that occupied a lot of chip area and power consumption. A different way to achieve fast-lock is proposed in [70] as shown in Fig. 2.12. It uses a digital hybrid PLL with Digital Look-up Table (DLT) to directly adjust VCO output to the desired frequency, and the use a traditional analog PLL to fine-tune the output frequency. However, this digital look-up table is still dependent on PVT variations. As a result, acquisition time increases in proportion to the initial frequency difference.




(a)




(b)

Fig. 2.11. PLL frequency synthesizer with DPFD [62]. (a) Functional block diagram. (b) Structure of DPFD.

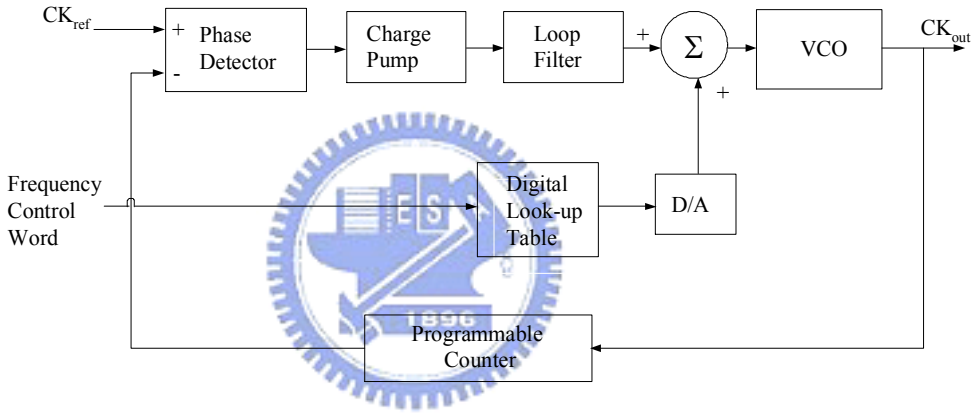



Fig. 2.12. Hybrid PLL frequency synthesizer with DLT table [70].

To further speed up lock time, a Time-to-Digital (TDC) circuit as shown in Fig. 2.13 can be used to quantize the reference clock period ratio into multiple of inverter delay times as indicated in [51]. This all-digital PLL replaces the DLT with TDC to against PVT variations and speed up the frequency acquisition process. However, the area cost for the TDC processing unit is large if a small chip area is required.

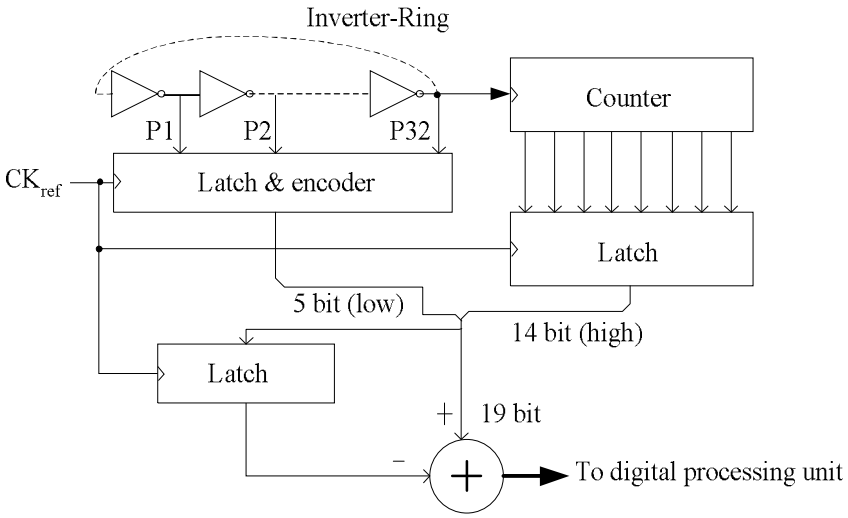



Fig. 2.13. Time-to-Digital conversion circuit [51].

An all-digital PLL as indicated in section 2.2.2 that uses the modified binary search which can achieves 50 cycles lock-in time for clock multiplier applications (multiplication factor: 4). This ADPLL can keep tracking the phase of the reference clock by using an anchor register to store the baseline frequency and a complex phase/frequency tracking algorithm. The phase error of this ADPLL may become worst when multiplication ratio is increased. In addition, its DCO needs to be full-custom design, making it difficult for porting to different process as design specification to be changed.

Thus, efforts at the physical design level remain unsolved. A complete clock generator design using standard cell only as the IP block with portability in [44-50] can partially solve the problem. A portable clock multiplier generator using digital CMOS standard cells based is presented in [44]. However, its multiplication factor is limited to 4~20. Additionally, three large register files are required for storing the history of previous 256 cycles. The chip area also is very big and dependent on multiplication factor.

The standard cell-based DCO with delay matrix architecture to improve the resolution in the fine-tuning is developed in [47-48]. But, the proposed fine-search delay matrix also occupies large silicon area and high power consumption. Also, two DCOs are required to

reduce the output clock jitter effectively. From the above discussions, a better DCO with high resolution and a new loop control algorithm has to be explored for different SoC and low cost applications.

# Chapter 3

# Digitally Controlled Oscillator with Novel Varactors

Traditional analog circuit design, such as voltage-controlled oscillator (VCO), shifts the design paradigm towards more digitally-intensive techniques, easier testability and less parameter variability because of process migration. Digitally controlled oscillator is the key component of all-digital PLL. Thus, this chapter attempts to propose a high resolution DCO by using NOR/NAND gates as novel varactor.

The organization of this chapter is as follows. Section 3.1 describes the preliminary concept of DCO, basic DCO design and fine tune methods. The novel digital controlled varactor is discussed in section 3.2. Section 3.3 describes the structure of DCO. Summary is in section 3.4.

## *3.1 Basic Concepts of Digitally Controlled Oscillator*

The fundamental function of a DCO is to provide an output waveform, typically in the form of square wave, which has a frequency of oscillation $f_{DCO}$ that is a function of a digital input word D, as follows:

$$f_{DCO} = f(D) = f( d_{n-1} 2^{n-1} + d_{n-2} 2^{n-2} + \cdots + d_1 2^1 + d_0 2^0). \quad (3.1)$$

Typically, the DCO transfer function $f(\cdots)$ is defined so that either the frequency $f_{DCO}$ or the period of oscillation $T_{DCO}$ is linear with D, generally with an offset. For example, a DCO transfer function that is linear in frequency is typically expressed as:

$$f(D) = f_{offset} + D \cdot \Delta f \quad (3.2)$$

where $f_{offset}$ is a constant offset frequency and $\Delta f$ is the frequency quantization step. Similarly, a DCO transfer function that is linear in period is typically expressed as:

$$T(D) = 1/f(D) = T_{offset} + D \cdot \Delta T \quad (3.3)$$

where $T_{offset}$ is constant offset period and $\Delta T$ is the period quantization step. It is evident that, since the DCO period T(D) is a function of quantized digital input D, the DCO can not generate a continuous range of frequencies. In this regard, the quantization granularity of the DCO period sets some fundamental limits on the achievable jitter of an all-digital PLL. It is of course desirable to have a fairly small quantization step size (e.g. period quantization step $\Delta T$).

### 3.1.1 Basic DCO Design Approaches

One simple method to implement DCO in [53] is directly utilized digital-to-analog (DAC) converter and conventional voltage (current) controlled oscillator (VCO, ICO) as shown in Fig. 3.1. However, to design a high resolution DAC (e.g. 16 bits) is extremely difficult. In addition, the VCO is an analog block that is easy to be influence by power and substrate noise. It also requires extensive design efforts when specifications are changed or transfer into other technology processes. The chip area cost is very high due to DAC and VCO.

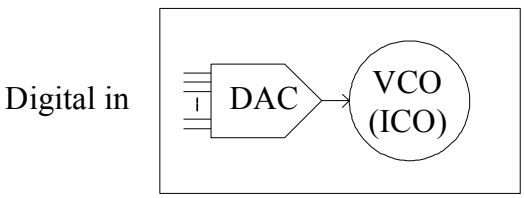



Fig. 3.1. DCO constructed with DAC and VCO (ICO).

Another common type of conventional DCO includes a high frequency oscillator in combination with a programmable frequency divider. Figure 3.2 shows the DCO. A

programmable frequency divider receives an n-bit digital control word D which indicates the divisor values. The output DCO (CLK) signal is to be divided from a high speed oscillator (HFCLK).

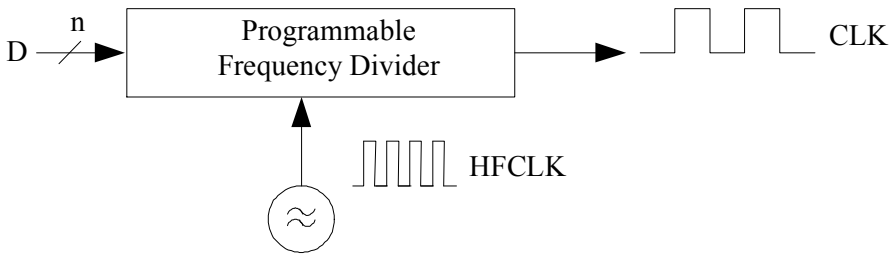



Fig. 3.2. DCO constructed with high-speed clock and divider.

The period quantization step ΔT is limited by the high frequency oscillator (HFCLK) in this arrangement. Low jitter operation thus requires oscillator to operate at an extremely high frequency; for example, a 100 ps step between periods require high frequency oscillator and programmable counter to operate at 10 GHz. This will consume a lot of power consumption.

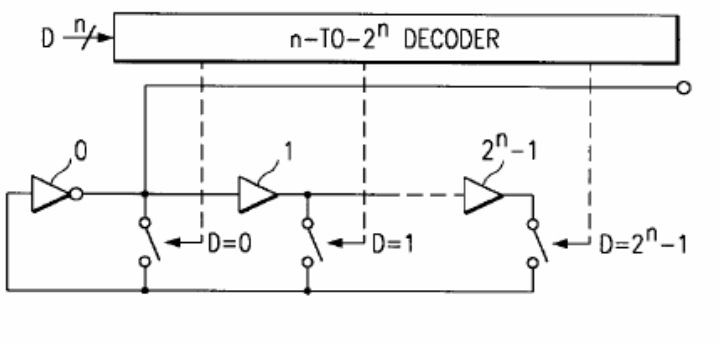



Fig. 3.3. DCO constructed with variable length ring oscillator.

Because of the speed limitation, other conventional DCO approaches directly synthesis a signal, rather than dividing down from a high frequency source. Figure 3.3 shows a variable length ring oscillator. In this example, $2^n$ delay buffer are connected in series. A decoder

decodes n-bit digital control word D into $2^n$ control lines. If the propagation delay time of each buffer stage is $T_{buffer}$, then the period quantization step is thus $2 \cdot T_{buffer}$, which is typically an improvement over Fig. 3.2's design. However, the period quantization step still may be too coarse for many applications.

### 3.1.2 Enhance Fine Resolution of DCO design

The basic skill to enhance the fine resolution of DCO is to enhance overall driving capability. The methods are to adjust the overall resistance (R), or to adjust capacitance (C), or to adjust inductance (L) as shown in Fig. 3.4.

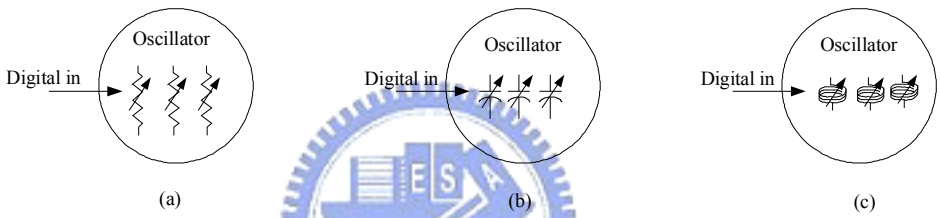



Fig. 3.4. General mechanism for enhance of fine tune in DCO.

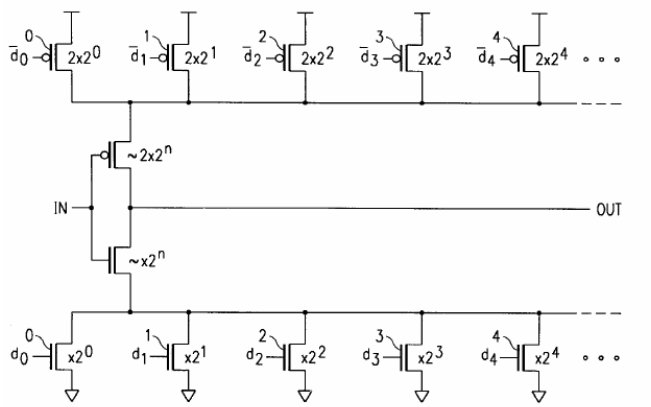



Fig. 3.5. DCO with fine resolution constructed with current starved ring oscillator.

A well-known DCO is indicated in [37], the desired output frequency is directly synthesized through the operation of an eight-stage current-starved ring oscillator, on such stage is

illustrated in Fig. 3.5. Each inverting stage includes a pull-up leg of parallel binary-weighted transistors, and pull-down leg of parallel binary-weighted transistors each of the transistor on the pull-up leg or pull-down leg is controlled by a corresponding bit $d_i$ of the control word D. While acceptance frequency resolution is provided, the amount of integrated circuit chip area is extremely large. In addition, the layout of the DCO has to be full custom, which is very time consuming.

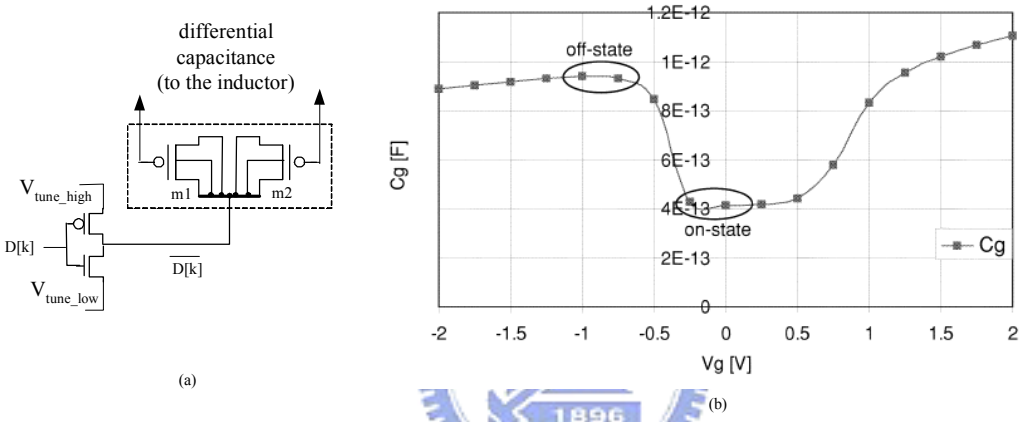



Fig. 3.6. DCO with differential capacitance for fine resolution (a). circuit structure. (b). Gate capacitance v.s. gate voltage for PMOS varactor (L=0.5 μm, W=0.6 μm) when source and drain tied to GND.

Another DCO has significant resolution using a switched-capacitor bank for RF application is indicated in [54]. The LC tank DCO achieves very fine frequency resolution (23KHz) by using advanced 0.13-μm CMOS process. The switchable capacitance of the finest PMOS varactor is 38 attofarads as shown in Fig 3.6 where the D[k] is the digital control word. The differential capacitance is formed by transistor M1 and M2. However, this DCO suffers from one fundamental drawback. Due to the extremely small size of varactor, it requires intensive circuit layout and needs advanced lithography technology. It also needs to overcome Process variations, Voltage variations, and Temperature variations (PVT variations) before an acceptable performance can be achieved. And because of these complicated factors, they

often result in a long design cycle as the design product transfers to different process or design specifications are changed.

### 3.1.3 Fine Tune in Standard Cell Library

For most digital applications, a standard cell description of the digitally controlled oscillation simplifies the design, and it can be easily ported to different processes in a very short time period. One simple DCO design directly using an inverter as delay cell is reported in [46], but its resolution is not fine enough for most applications. The other example, a DCO consists of a bank of tri-state inverter buffers was proposed in [47-49] as shown in Fig. 3.7. The resolution of DCO can be controlled by enabling the numbers of tri-state buffers. The advantage of this structure is very simple and easy to implement. However, this DCO design for fine tune has disadvantages in large area and high power consumption. In addition, the resolution of time step is not easy to be uniform.

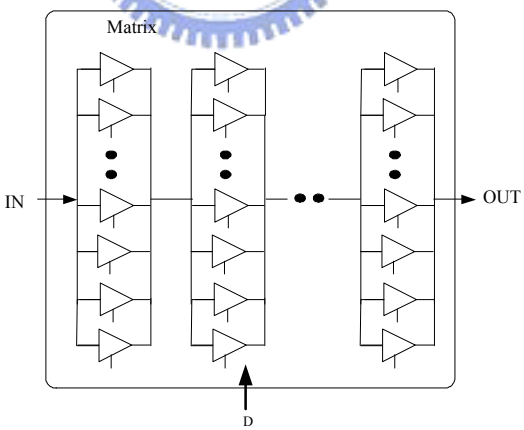



Fig. 3.7. DCO with tri-buffer matrix.

Another example of DCO implemented by an and-or-inverter (AOI) cell and or-and-inverter (OAI) cell with two parallel tri-state inverters was proposed in [50]. The basic method is to adjust the driving capability with resistance control. This fine tune method of DCO cell has less area and power consumption than [47-49]. However, its resolution step is

non-uniform and sensitive to power-supply variation because it is based on AOI-OAI cell to change the delay resolution. In addition, this technique also requires an additional decoder for mapping AOI-OAI cell control inputs.

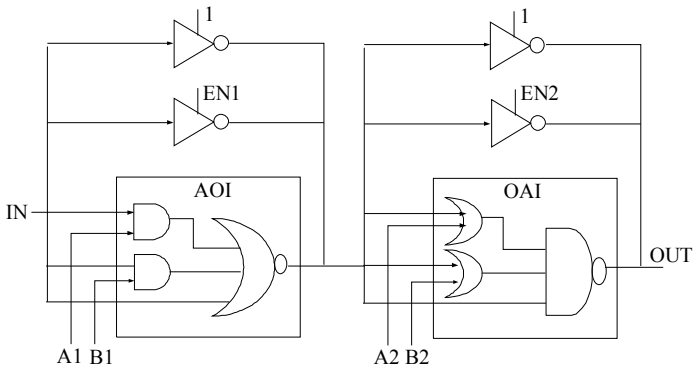



Fig. 3.8. DCO with AOI-OAI as fine tuning cell.

The concept of timing vernier has been utilized in measurement [58]. A fine tune method in [59] uses the delay difference of NAND between different paths. For example, the capacitances and output strengths of different pins are approximately close for a NAND gate in standard-cell library. The timing delay difference from different input pins to the same output pin approximates to the intrinsic delay difference. The advantage is that the delay difference can be check directly from the standard-cell data sheet. However, the real routing, placement, and loading of the NAND gate in the chip will also influence the intrinsic delay difference. In addition, the on/off each switch will also cause fluctuation of timing difference.

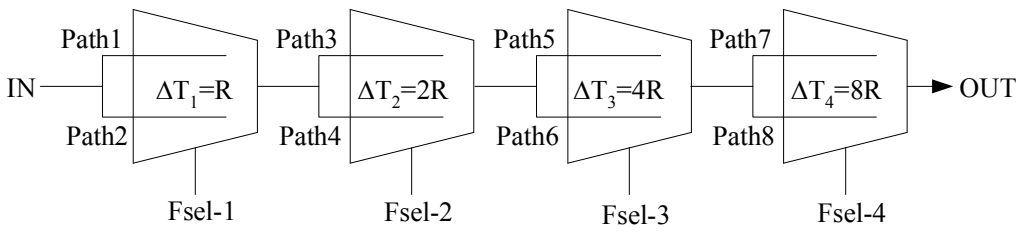
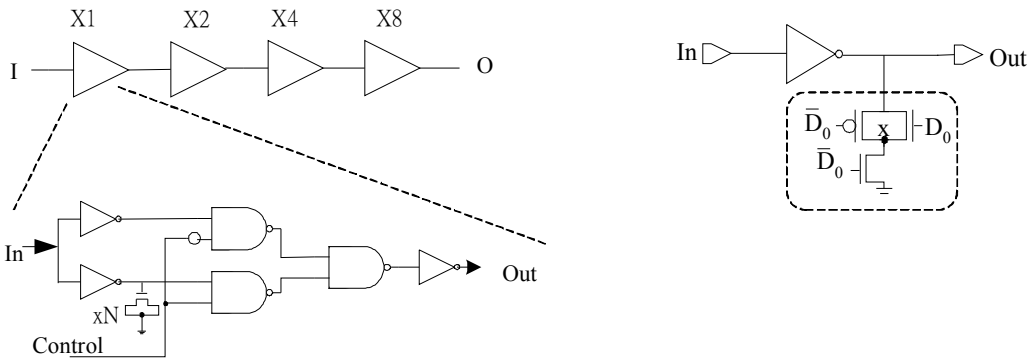



Fig. 3.9. Fine tune cell of DCO with delay difference.

## *3.2 Digital Control Oscillator with DCVs*

A delay control method has been successfully applied in delay locked loop as indicated in [71] based on path difference. The other similar concept was based on single path delay as indicated in [56].




(a) (b)

Fig. 3.10. (a). Delay control in [71]. (b). Delay control in [56].

The proposed DCO, like most voltage-controlled oscillators or delay control, employs a frequency control mechanism located inside an oscillator block. Two parameters are used to modulate the output frequency of a ring oscillator, namely the propagation delay time of each delay cell, and the total number of delay cells in the closed loop. Generally, delay time resolution is more difficult to achieve than total delay time, because the transistor width/length (W/L) is fixed in a cell-based design. To deal with this problem, we developed a novel DCV using NOR/NAND gate in the fine-tuning cell design of DCO. The proposed DCO improves delay resolution and demonstrates monotonic delay behavior with respect to digital control codes. The proposed technique has been successfully verified on a test chip fabricated in a 0.35-μm 2P4M CMOS process.

Basically, two main techniques exist for designing a fine resolution in DCO with shunt capacitor. One technique changes the MOS driving strength dynamically using a fixed capacitance loading and achieves a fine resolution [55]. Meanwhile, the other uses the shunt

capacitor technique to fine-tune the capacitance loadings and achieves high resolution [54,56]. Figure 3.11 shows the conventional control mechanism with the shunt capacitor circuit. In Fig.3.11, $M_C$ serves as a capacitor. The gate of transistor $M_{ctrl}$ (that is, $D_{ctrl}$) controls the discharge/charge current. Consequently, $D_{ctrl}$ can control the delay resolution from In to Out.

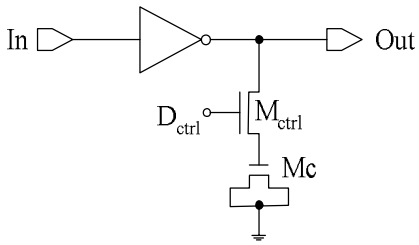



Fig. 3.11. Conventional digitally controlled mechanism with shunt capacitor.

### 3.2.1 Digitally Controlled Varactors

Figure 3.12(a) illustrates a novel varactor cell using a two-input NOR gate. As described in [60], the gate-to-channel capacitance contributes to total gate-capacitance. The proposed method controls the capacitance between gate and source or between gate and drain. In Fig. 3.12(a), the NOR gate-capacitance at node $C_L$ depends on control node D's value. The total gate-capacitance of transistors M2 and M3 varies with D input states. Figure 3.12 (b) shows the equivalent circuit of Fig. 3.12(a), an initial capacitance ($C_I$) parallels with a capacitance difference ($\Delta C$). The D input controls the capacitance ($\Delta C$) in the output (Out) node.

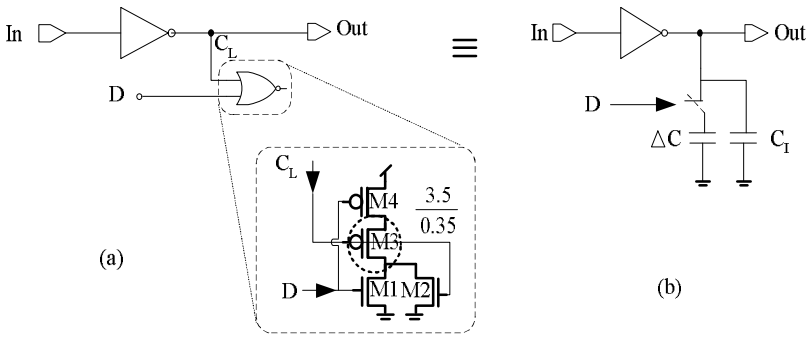



Fig. 3.12. Proposed DCV with two-input NOR gate. (a) Circuit with digital control. (b) Equivalent circuit with $\Delta C$ capacitance.

Figure 3.13 shows the gate-capacitance difference characteristic which is simulated using the HSPICE circuit simulator. The swing-averaged capacitance $C_{average}(D)$, as D-node is in the 0 state or in the 1 state, is given by

$$C_{average}(D)=\frac{1}{V_{dd}}\int_0^{Vdd} C(V_{gate}, D)\, dV_{gate} \tag{3.4}$$

where $C(V_{gate}, D)$ denotes the simulated gate capacitance shown in Fig. 3.12. Based on Eq. (3.4), ΔC denotes the capacitance difference between $C_{average}(0)$ and $C_{average}(1)$. Consequently, the variable delay (ΔT) of the proposed DCV in different D states can be calculated easily using the following linear equation,

$$\Delta T = K_{load} \times \Delta C \tag{3.5}$$

where $K_{load}$ denotes the delay factor of driving inverter. The $K_{load}$ value of the driving inverter is 0.535 (ns/pF) in target 0.35-μm 2P4M CMOS cell library. The ΔC of Fig. 3.13 is estimated to be around 2.8 fF. Therefore, ΔT of 1.49 ps (=0.535 * 2.8) is easily obtained. If N NOR gates are attached to the $C_L$ node, the max delay time variation becomes N*ΔT. Moreover, different ΔT can be achieved as needed by changing the cell type of the driving inverter (i.e., change the $K_{load}$ ).

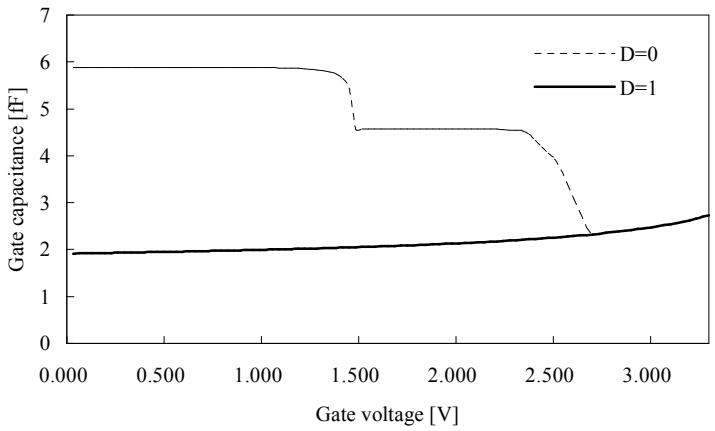



Fig. 3.13. Variation of two-input NOR gate's capacitance when D=0 and D=1.

A NAND gate can also be applied to DCV design. Figure 3.14 illustrates three different DCVs: (a) two-input NAND gate, (b) three-input NOR gate, and (c) three-input NAND gate. For the three-input NOR and three-input NAND gate, an extra input pin is fixed to 1 and 0, respectively. The marked transistors (M5, M6, M7) produce a large capacitance difference under different D states.

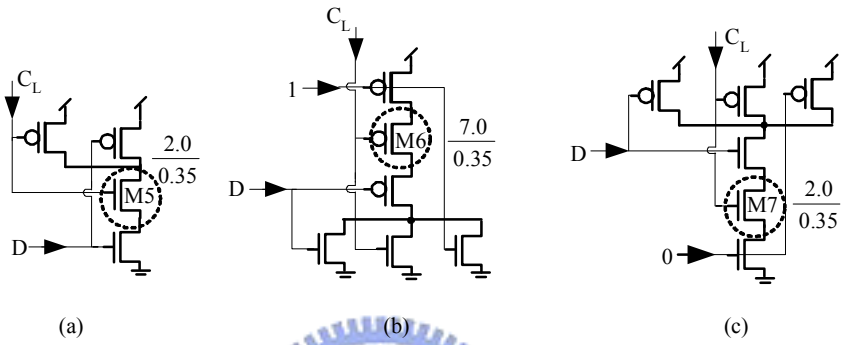



Fig. 3.14. Three different types of DCV cell. (a) Two-input NAND, (b) Three-input NOR, (c) Three-input NAND.

Table 3.1 lists the comparisons among these DCVs. The three-input NAND/NOR gate varactor consumes less power than the 2-input NAND/NOR gate varactor, but it costs more area. Generally, the finer delay resolution can be obtained by decreasing MOS width of (M5, M6, M7).

Table 3.1. Comparisons among different types of proposed DCV cells

| Item \ Type | Two-input NOR | Two-input NAND | Three-input NOR | Three-input NAND |
|---|---|---|---|---|
| Transistors | 4 | 4 | 6 | 6 |
| Size of transistors (W/L) unit: μm | 3.5 / 0.35 | 2.0 / 0.35 | 7.0 / 0.35 | 2.0 / 0.35 |
| Resolution | 1.43 ps | 0.80 ps | 3.2 ps | 0.80 ps |
| Power Consumption | 15.5 μw/MHz | 18.1 μw/MHz | 14.5 μw/MHz | 14.3 μw/MHz |

### 3.2.2 Performance of the Digitally Controlled Varactors

HSPICE circuit simulation is performed for estimating the performance of different type fine-tuning delay cell including the proposed DCV, pass transistor [56], and OAI cell [50] on a standard 0.35-μm CMOS 2P4M process. In this simulation, a series of 97 inverters are used in the coarse-tuning stage of the ring oscillator, and the proposed DCV serves as the fine-tuning delay cell. Totally, 32 DCVs are used in the fine-tuning delay cell (N=32).

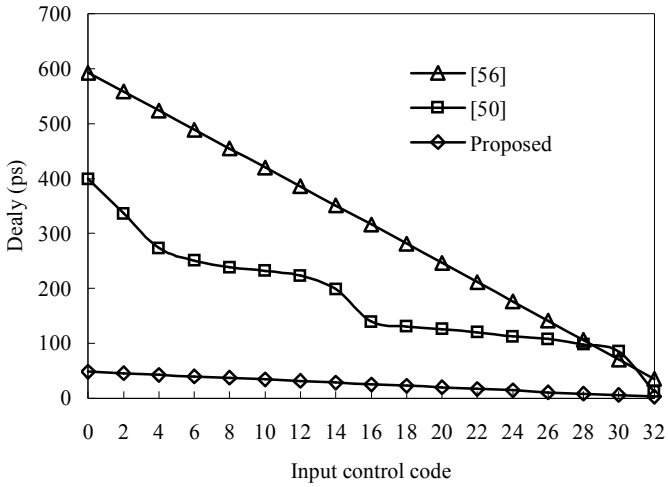



Fig. 3.15. Comparisons among the proposed DCV and other approaches.

Figure 3.15 shows the delay resolution of the fine-tuning stage and the proposed delay cell has finer resolution (about 1.43ps) than other circuits [50,56]. The delay cell proposed by [56] has very good linearity but poor resolution and it also has large transistor counts. Oppositely, OAI cell [50] has less transistor counts and less power consumption, but it has non-uniform linearity.

Figure 3.16 shows the proposed DCV under different PVT conditions: (Best: FF, 3.6V, 0 $^0$C), (Typical: TT, 3.3V, 25 $^0$C), and (Worst: SS, 3.0V, 125 $^0$C). The delay resolution of the proposed DCV ranges from 1.28 ps in the best case to 1.61 ps in the worst case. It demonstrates the effectiveness of the proposed DCV to overcome PVT variations.

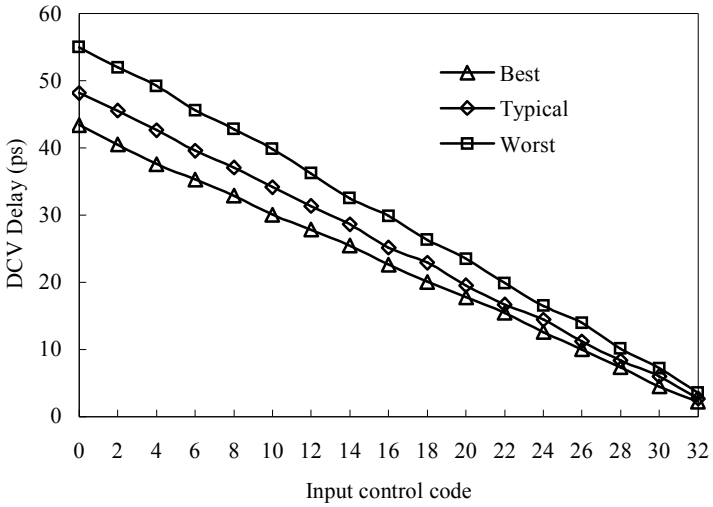



Fig. 3.16. The proposed DCV using two-input NOR under different PVT conditions.

## *3.3 Structure of the Proposed DCO*

### 3.3.1 Structure of DCO and Design Guide

Fig. 3.17 illustrates the structure of the proposed cell-based DCO with 15 bits binary weighted control ($0000_{16}$ ~ $7FFF_{16}$). The proposed DCO structure is separated into two stages: the coarse-tuning stage and the fine-tuning stage. The higher seven bits of the control code are for coarse-tuning stage, and lower eight bits are for the fine-tuning stage. The coarse-tuning stage uses a 128-to-1 path selector for delay-chain selection. This selector is implemented by multistage tri-state buffers to reduce the loading effects of coarse-tuning buffers. The coarse decoder of the DCO decodes the 7 (=$\log_2(128)$) bits control code into 128 control signals. This architecture has the advantage that operating frequency of DCO can be easily modified according to different specifications. The $T_{PHL}$ + $T_{PLH}$ ( = $T_{buffer}$) of one coarse delay cell is about 385 ps in target 0.35-μm 2P4M CMOS standard cell library.

To increase the frequency resolution of the DCO, the fine-tuning stage is divided into fine1 and fine2 stages which are added after the coarse-tuning stage. The fine1 stage consists of 32

digitally-controlled varactors (DCVs) with capacitance difference ΔC. 32 identical NOR gates with ΔC are used to build one ΔC2 DCV. The total capacitance difference equals to 256 ΔC DCVs. The proposed NOR gate varactors for fine-tuning stage thus can improve delay resolution by 256 times compared to a simple buffer design.

The period of DCO's output signals equals

$$T_{period} = T_{coarse} + T_{fine} + T_{constant} \quad (3.6)$$

where $T_{coarse}$ denotes the propagation delay time of coarse buffers, $T_{fine}$ represents the fine-tuning delay time, and $T_{constant}$ is the constant factor for delay time because of one extra NAND gate, a multi-stage tri-state buffer and the intrinsic delay caused by capacitance ($C_I$) of fine-tuning cells in the DCO ring.

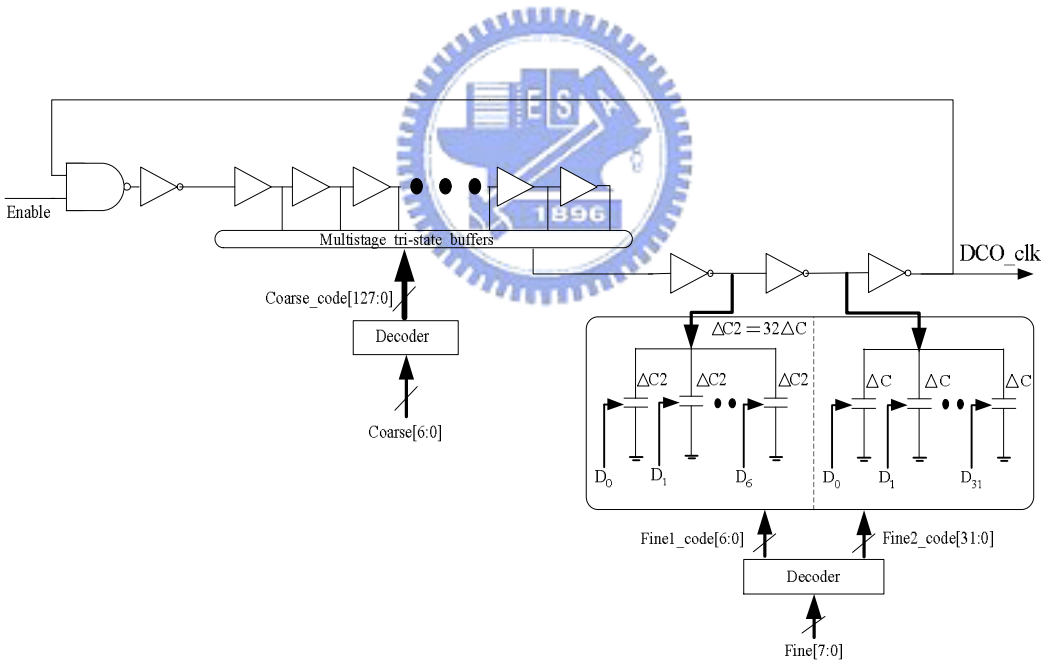



Fig. 3.17. Proposed digitally-controlled oscillator with DCV in the fine-tuning stage.

Equation (3.6) can be rewritten as follows:

$$T_{period} = M \times T_{buffer} + N_2 \times \Delta T_2 + N_1 \times \Delta T_1 + T_{constant} \quad (3.7)$$

where M denotes the number of selected coarse buffers. $N_1$ and $N_2$ represent the number that

DCVs are turned on in fine1 and fine2 stages, respectively. Meanwhile, $\Delta T_1$ and $\Delta T_2$ are variable delay which can be calculated from Eq. (3.5). Therefore, Eq. (3.7) provides an easy method of calculating the timing period of DCO output.

When design a DCO, the target frequency ($T_{period}$) range will be specified at first. Second, the coarse delay buffer with $T_{buffer}$ can be selected from a target standard cell library. Third, the resolution of DCO is defined by DCVs with $T_{fine}$ based on Eq. (3.5) as discussed in the previous section. In order to simplify the DCO decoder, the relationship of $T_{fine}$ and $T_{buffer}$ has better to be approximately power of 2 (i.e. $2^n$). This can be achieved by iteration of second and third steps. If the number of fine tune ($2^n$ ) is large, then different driving cells and different types of DCVs can be applied to save chip area. Finally, the number of coarse buffer M can be decided.

### 3.3.2 Design of DCVs

The proposed DCO with novel digitally controlled varactors is applied to all-digital frequency synthesizer design. The test chip is fabricated using a standard 0.35-μm 2P4M CMOS process. The designed DCO consists of two major functional blocks as illustrated in Fig. 3.16, namely the ring structure and decoder. Moreover, the decoder part is described by Verilog-HDL. The ring structure with DCVs is described at the gate-level. A Verilog-HDL model of DCVs is first built from HSPICE simulation results for co-simulation with other digital blocks. Next, source codes are synthesized to gate-level netlists and schematics for further simulation and verifications. Once the functions have been correctly verified, an automatic placement and routing (APR) tool is used to complete the physical layout.

In APR process, the designed DCO must be grouped in a restricted region to minimize the induced capacitance and the ring structure of DCO had to be placed regularly rather than randomly. Furthermore, the post-layout simulation is performed to ensure the monotonic response of DCO and timing resolution. The APR process will be refined until the target

specification is achieved.

### 3.3.3 Laboratory Test Result

Figure 3.18 is a microphotograph of the all-digital frequency synthesizer. The proposed DCO is located in the upper-left corner of the test chip and occupies 0.04 $mm^2$ of chip area (i.e., 200 um x 200 um). This DCO has been measured for different settings. Initially, the DCO output frequency is directly measured using LeCory LC584A at 3.3V/25 $^0$C, and the measured results demonstrate that the operating frequency of the DCO ranges from 18 to 214 MHz (i.e., 55.555ns to 4.673ns). Moreover, the average step resolution is 1.55ps. In Fig. 3.19, the measured results are compared to linear delay Eq. (3.7). Figure 3.19 also reveals that linear delay Eq. (3.7) can be used to estimate DCO timing period.

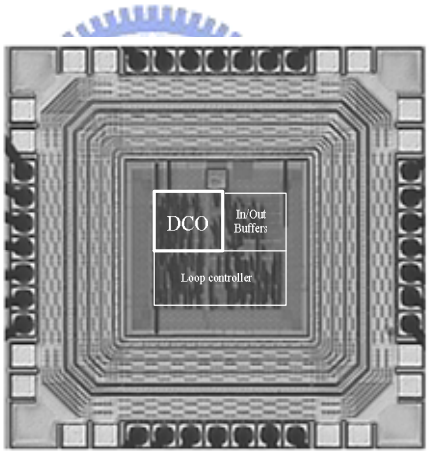



Fig. 3.18. Microphotograph of DCO test chip.

Table 3.2 lists the chip measurement results compared with conventional approaches [50,56-57]. The proposed DCO with 15 bits control codes achieves the finest LSB resolution and best portability. Additionally, the proposed DCO also consumes less power as compared with [50,57].

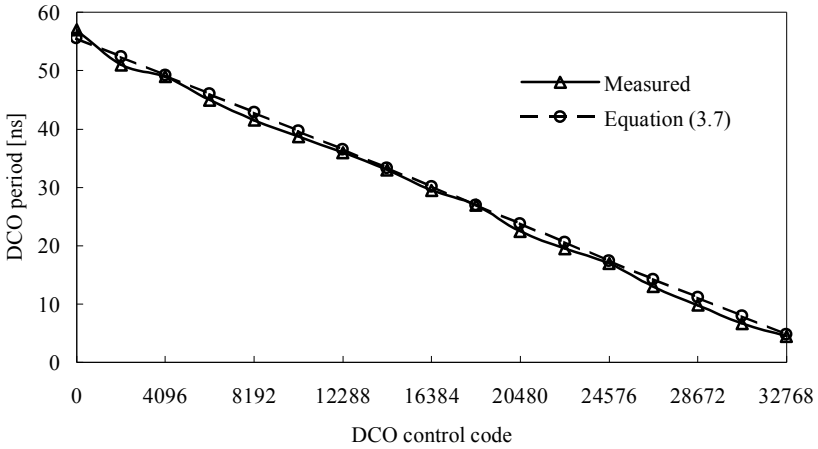



Fig. 3.19. Chip measured results compared to linear Eq. (3.7) under 3.3V/25 $^{0}$C.

Table 3.2. Comparison with existing DCOs

| Items / Function | This work | ISQED'02 [56] | ISSCC'03 [57] | JSSC'03 [50] |
|---|---|---|---|---|
| Process | 0.35μm@3.3V | 0.5μm@1.65V | 0.6μm@5V | 0.35μm@3.3V |
| DCO word length | 15 bits | 8 bits | 10 bits | 12 bits |
| LSB resolution | 1.55 ps | 40 ps | 10 ps | 5 ps |
| DCO output range | 18 ~ 214 MHz | 150 MHz | 10 ~ 12.5 MHz | 45 ~ 450 MHz |
| Power Consumption | 18mW@200MHz | 1mW@150MHz | 164mW@100MHz | 100mW@450MHz |
| Portability | Yes | No | Yes | Yes |

## 3.3.4 Porting DCO to Different Processes

The proposed DCO structure with novel DCV as shown in Fig. 3.17 is simulated under standard 0.35-μm, 0.18-μm, and 0.13-μm CMOS process. The DCO structure and the netlists are the same for these three processes, only cell name is replaced with according to each library. The control code of fine-tuning stage is 8 bit. The $T_{buffer}$ is 140 ps for selection in the 0.18-μm cell library. Similarly, the $T_{buffer}$ is 99.5 ps in 0.13-μm cell library. The resolution of DCV with NAND (3-input) gate as varactor is 0.55 ps/LSB and 0.40 ps/LSB in the 0.18-μm

and 0.13-μm CMOS process as shown in table 3.3, respectively.

Table 3.3. Resolution of $T_{buffer}$ and $T_{fine}$.

| $T_{buffer}$ and $T_{fine}$ Resolution (unit: ps) (Typical, 25 °C) | | | | | |
|---|---|---|---|---|---|
| 0.35 μm (3.3V) | | 0.18 μm (1.8V) | | 0.13 μm (1.2V) | |
| $T_{buffer}$ | $T_{fine}$ | $T_{buffer}$ | $T_{fine}$ | $T_{buffer}$ | $T_{fine}$ |
| 385 | 1.49 | 140 | 0.55 | 99.5 | 0.40 |

Table 3.4. DCO output frequency range for different processes under typical conditions.

| DCO Control word | | DCO Output Frequency Range (unit: MHz) (Typical, 25 °C) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0.35 μm (3.3V) | | 0.18 μm (1.8V) | | 0.13 μm (1.2V) | |
| coarse | fine | Min. | Max. | Min. | Max. | Min. | Max. |
| 7 | 8 | 18.68 | 236.56 | 48.98 | 392.78 | 66.37 | 450.96 |
| 8 | 8 | 9.72 | 236.56 | 26.04 | 392.78 | 35.94 | 450.96 |

Table 3.4 lists the DCO output frequency range for different processes under typical condition. The coarse-bit means the bit width of the coarse-tuning control code. For example, coarse = 7 means there are 128 (=$2^7$) paths in the coarse-tuning stage of DCO. The total control word of DCO is 15 bit. The maximum operating frequency is dependent on the gate delay of the cell libraries. And the minimum operating frequency is dependent on how many coarse-tuning delay cells are used in the DCO's coarse-tuning stage. Figure 3.20 shows the simulation results of different processes under typical condition. The DCO period is linear with the input DCO control code.

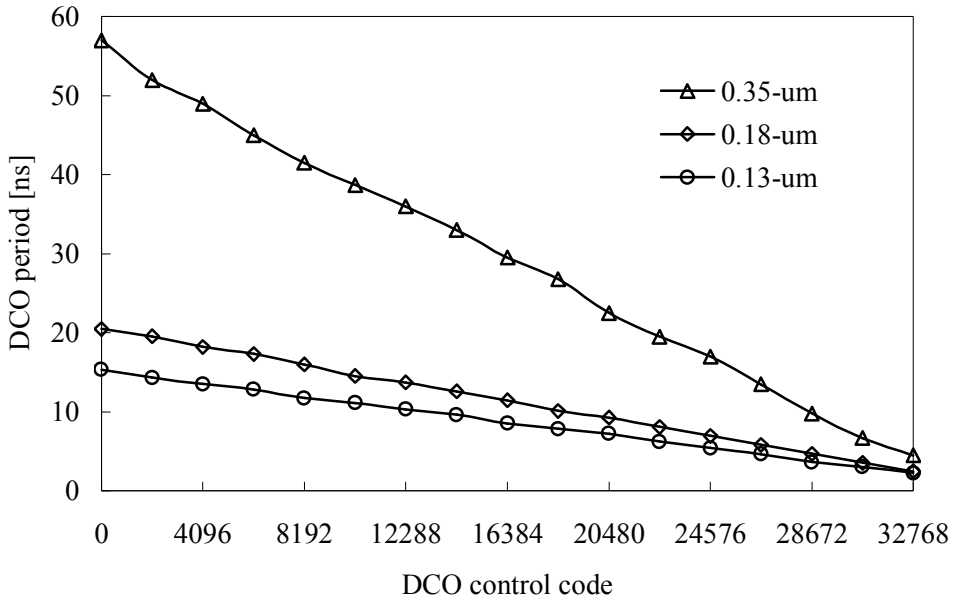



Fig. 3.20. Circuit simulation with DCO 15-bit under different process (typical, 25 $^{0}$C).

## *3.4 Summary*

In this chapter, basic DCO concept is discussed at first. Then, a portable digitally controlled oscillator using two-input NOR gate as digitally controlled varactor is presented. Different configurations based on NOR/NAND (2-inputs and 3-inputs) gates have also been investigated using HSPICE circuit simulator. The delay resolution of the proposed DCO can be determined using a simple linear equation, and the design guidelines are also gievn. Test chip measurement results show the average delay resolution of the proposed DCO is 1.55 ps. The LSB resolution of DCO is enhanced 256 times as compared with single buffer stage. Therefore, the proposed digitally controlled oscillator reduces the circuit complexity and also improves testability. Compared to conventional approaches, design time can also be reduced significantly by using Verilog hardware-description language and APR CAD tools. Furthermore, the proposed DCO is suitable for SoC design, and has an excellent chance of first-time silicon success.

# Chapter 4

# Dynamic Frequency Counting Loop for All-Digital Clock Generator

In this chapter, we proposed dynamic frequency counting (DFC) loop with low gate count for an all-digital clock generator. The DFC loop which uses variable time period to estimate and tune the frequency of digitally controlled oscillator (DCO) enhances the resolution of frequency detection. One up counter serves as variable timer and another DCO timing counter acts as frequency estimator. Conventional phase-frequency detector (PFD) thus is replaced with a digital arithmetic comparator to yield a simple circuit structure. Also, a threshold region is set and by using dynamic sampling period to solve the quantization effect of counter sampling. The proposed DFC loop for all-digital clock generator was verified with 0.35-um and 0.18-um complementary metal oxide silicon (CMOS) process.

The organization of this chapter is as follows. Section 4.1 describes the introduction. The proposed algorithm and architecture is described in section 4.2. Analysis of proposed DFC algorithm is discussed in section 4.3. Then, summary is given in section 4.4.

## *4.1 Introduction*

Clock generator has many applications in today's commercial electronic and telecommunication system. Some techniques exist as described in chapter 2 [1-13, 26-32, 37-39, 43-53, 64], which can be used to generate a frequency that is an integer multiple of a

reference frequency. The design of clock generator is a trade-off among area cost, power consumption, jitter performance, circuit complexity and design time. Therefore, in this chapter, we only focus on the loop control algorithm for all-digital design.

The loop control algorithm of [50] was based on traditional charge pump PLL and directly replaces the digital circuits as discussed in section 2.2.3. [49] also applied similar method. The only difference is that a Time-to-Digital (TDC) converter to measure the phase difference. Both [49] and [50] use the phase-frequency-detector and programmable divider.

An all-digital PLL (ADPLL) as discussed in section 2.2.2 did not use the PFD and programmable divider. The locking process includes how to perform frequency detection, frequency acquisition, frequency tracking, and phase tracking. However, the multiplication factor is limited to 4. The phase error of this ADPLL may become worst when multiplication factor is increased.

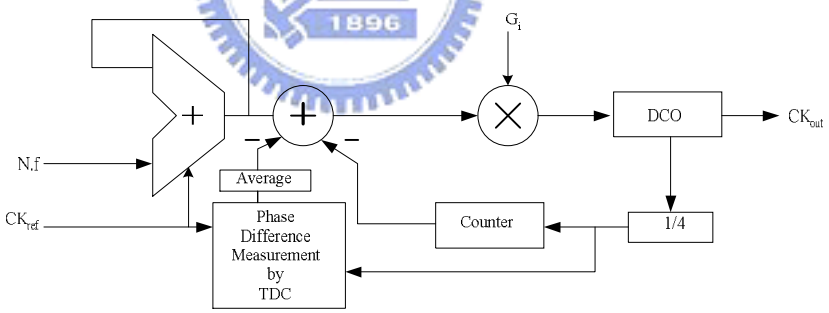


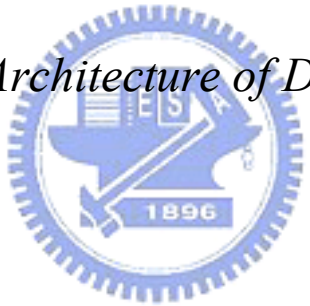

Fig. 4.1. Functional block diagram of [41].

The ADPLL of [41] is successfully applied in the wireless applications for fractional frequency synthesizer, such as Bluetooth and GSM. The functional block diagram of the architecture is shown in Fig. 4.1. The counter was applied to accumulate the phase. The TDC only calculate the phase difference. The TDC is only enabled near the rising edge of reference clock, which can save power. The cost of TDC is very high. In addition, an average unit is

also required to enhance the average resolution of phase measurement. Those units had better to be eliminated for low cost application.

The above structures are all time invariant system. The averaged process unit can be eliminated using the time accumulation. Therefore, we propose a DFC loop control algorithm for frequency search to simplify the hardware cost and enhance frequency detection's resolution. The proposed method can reduce the noise and jitter associated with input reference by dynamic frequency counting. Rather than using a PFD, a programmable divider, and loop filter as in conventional approaches, a DFC loop controller and two digital frequency estimators are applied. No additional need exists for another loop filter in the proposed structure because the DFC loop controller has achieved similar functionality. This demonstrates the effectiveness of the proposed mechanism.

## *4.2 Algorithm and Architecture of Dynamic Frequency Counting Loop*



One common problem exists as described in chapter 2 when the loop's order of PLL or ADPLL is greater than one owing to a phase difference detected in the phase frequency detector. The main reason to this problem is the integral of frequency, which implies that there is a 90 degree shifted response from the DCO control word (DCW). It implies mathematically a pole in the loop response created by the action of measuring phase in the PFD. Thus, it needs a zero to remove the inherent pole to make the loop to be at least second order control system [49,53,55]. This makes the designs to be very complex.

### 4.2.1 Algorithm of Dynamic Frequency Counting Loop

The dynamic frequency counting loop is a first order system that uses variable time

period to estimate and tune frequency of DCO. Fig. 4.1 shows the loop control algorithm of the proposed DFC loop. The reference timing counter (REF_timing_counter) operates at reference clock rate. The counter initially from zero counts up at every rising-edge of reference clock. Similarly, the DCO timing counter (DCO_timing_counter) operates at the speed of the DCO output clock. The quotient and remainder vectors in the DCO timing counter are compared with the input multiplication factor (N) when the reference timing counter is power-of-2 reference clock cycles.

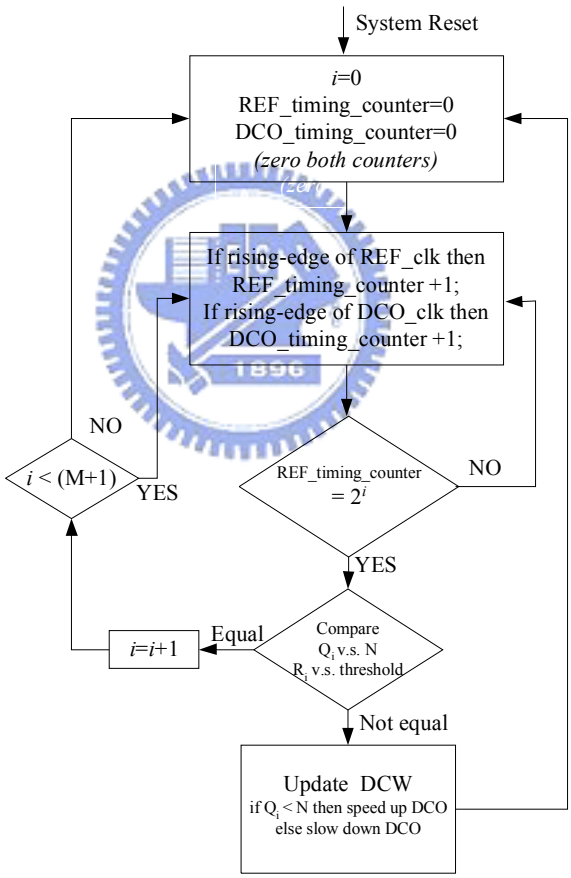



Fig. 4.2. The loop control algorithm for proposed DFC loop.

The sampling cycle time of the DFC loop control is defined as

$$C_i = 2^i \cdot T_{REF} \tag{4.1}$$

where $i$ represents the $i$-th DFC sampling state and $T_{REF}$ is the cycle time of the input reference clock ($CK_{ref}$). The sampling cycle time $C_i$ is the timestamp performing the frequency comparison of DCO clock output and M is the maximum number of DFC sampling state, which is shown in Fig. 4.3. If the result of frequency comparison remains unchanged and the maximum number of DFC sampling state is less than M+1, both counters will continue frequency accumulation. Otherwise, the frequency error signal will be asserted to update current DCO control word (DCW) to adjust the DCO output frequency. Meanwhile, both the reference timing counter and DCO timing counter are reset to zero. Therefore, the reset and accumulation of both counters move according to frequency sampling period and frequency comparison result.

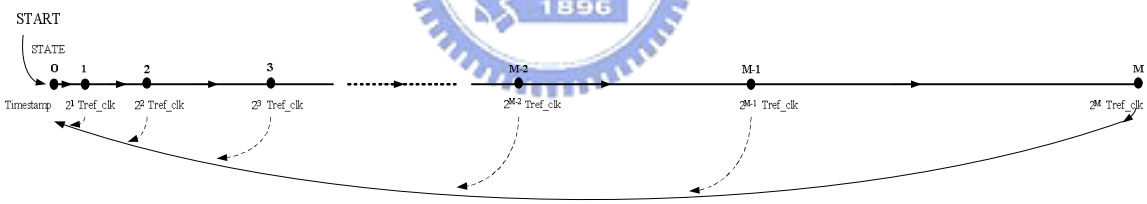



Fig. 4.3. Timestamp of frequency comparison.

Fig. 4.4. shows the basic structure of dynamic frequency counting loop. It consists of four main functional units: a reference timing counter, DCO timing counter, DCO and DFC loop controller. The reference timing counter serves as a variable timer for decision unit to estimate and control the DCO. The DCO timing counter performs as a frequency estimator of DCO output frequency. The DFC loop controller performs loop control, frequency error accumulation and gain control based on measured frequency values in DCO timing counter. The DFC loop is a discrete-time sampled system implemented with all digital components.

Consequently, the z-domain representation is the succinct method instead of using damping factor as indicated in chapter 2 for analog PLL.

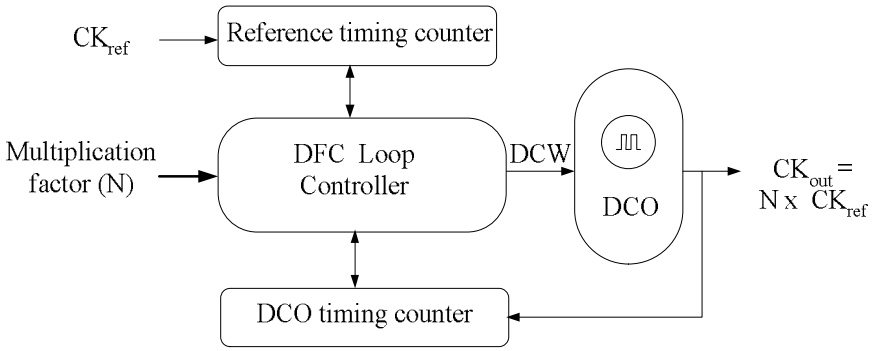



Fig. 4.4. Basic structure of dynamic frequency counting loop.

Fig. 4.5 illustrates the signal model of the proposed clock generator with the DFC loop control. The transfer function of Fig. 4.5 is given by

$$H[z(t)]= \frac{K(i)\cdot[z(t)]^{-1}}{1-(1-K(i))\cdot[z(t)]^{-1}} \qquad (4.2)$$

where K(i) is the loop gain (i.e., $K_i \cdot K_{DCO} \cdot 2^i / F_{REF}$ ), $F_{REF}=1/T_{REF}$ and $t = 2^i \times T_{REF}$, i=0,1,2..M.

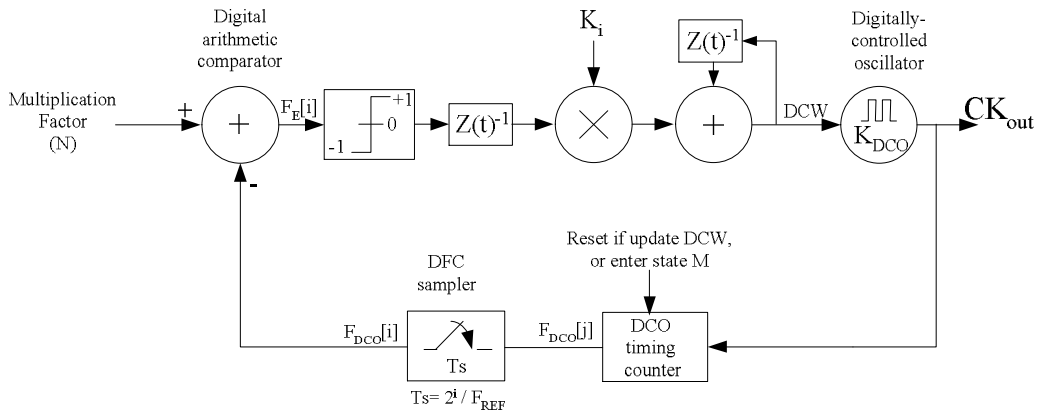



Fig. 4.5. Signal model of the proposed dynamic frequency counting loop.

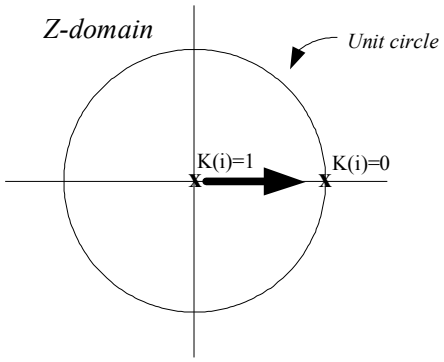



Fig. 4.6. Pole displacement by gain variation.

From (4.3), it should be noted that K(i) should be placed in the range 0 ~ 2 for loop stability. Fig. 4.6 illustrates the pole displacement with gain variation, and the maximum value of M is bounded by the loop gain K(i). The DFC loop control is a first-order time varying system. It only accumulates the frequency error thus generally features faster dynamics and greater stability than higher order loop. The digital arithmetic comparator replaces conventional PFD conversion mechanisms. The variable frequency $F_{DCO}[j]$ is determined by counting the number of rising-edge clock transitions of the digitally controlled oscillator. The sampled $F_{DCO}[i]$ is compared with multiplication factor (N) in a digital arithmetic comparator. If the comparison is equal, the comparator outputs 0; otherwise, it outputs +1 (-1) if reference frequency is faster (slower) than the DCO frequency. The result is then multiplied by gain $K_i$. Then, the DCO's output frequency is adjusted.

Fig. 4.7 shows the step response of the proposed clock generator with DFC algorithm as compared with the sequential search. The step size of the sequential search is 1/128 (i.e. DCO is 8 bits) and the initial condition is set to 0.5 of normalized frequency to improve visualization. The proposed all-digital clock generator with DFC loop achieves fast locking in less than 10 iterations as illustrated in Fig. 4.7 (a). In contrast, the sequential search requires at least 50 iterations to achieve frequency acquisition as shown in Fig. 4.7 (b). Furthermore, if

the fine resolution of the DCO is inadequate, jitter variations will occur as indicated in Fig. 4.7 (c).

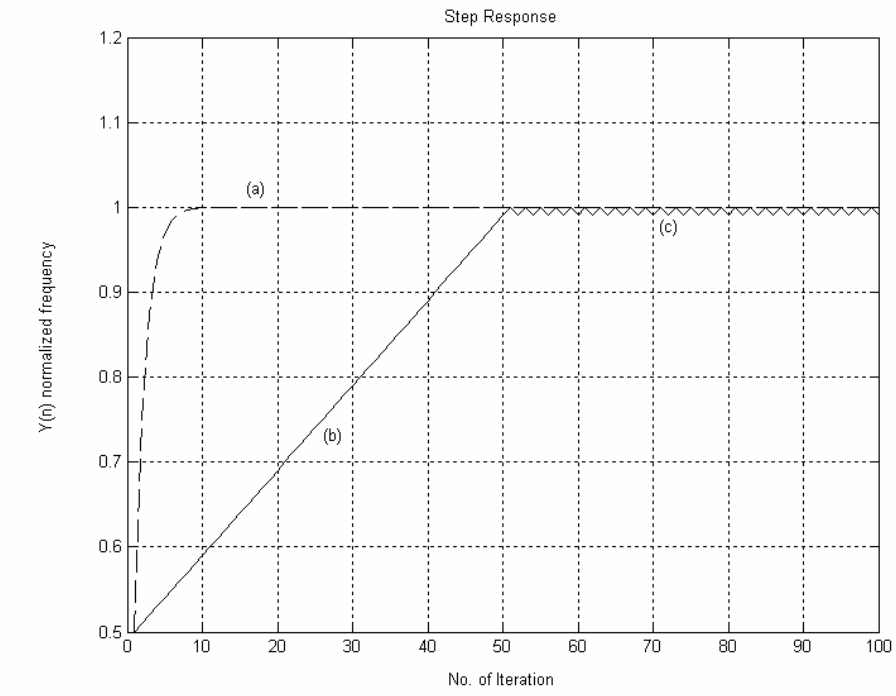



Fig. 4.7. Step response of the proposed clock generator with DFC loop control v.s. sequential search (a). Proposed. (b). Sequential search. (c). Jitter variation.

### 4.2.2 Structure of reference and DCO timing counters

The structure of reference timing counter is a ripple counter with reset function. The length of reference timing counter is dependent on the maximum DFC state of estimating DCO frequency. The structure of DCO timing counter is also a ripple counter with reset function. Therefore, most bits of the DCO timing counter are working in the low clock rate that can save power consumption. The length of the DCO timing counter is related to the multiplication factor (N) and the length of reference timing counter. If the maximum value of multiplication factor is P, L is formulated as

$$L = \lceil \log_2 P \rceil \tag{4.3}$$

where $\lceil X \rceil$ represents the least integer greater than or equal to X. If the length of the

reference timing counter is M, which is equal to the maximum number of DFC sampling state, the length of the DCO timing counter equals L+M. Fig. 4.8 shows the block diagram of quotient and remainder vectors in DCO timing counter with ($A_{L+M-1}$ $A_{L+M-2}$ ····· $A_2$ $A_1$ $A_0$) bits. The values of the quotient and remainder vectors in the *i-th* sampling state are

$$Q_i=( A_{L+i-1} \cdots\cdots A_{i+1} A_i), \tag{4.4}$$

and

$$R_i=(A_{i-1} \cdots\cdots A_1 A_0) \tag{4.5}$$

where $A_i$ denotes the *i-th* bit of DCO timing counter. The measured values of $Q_i$ and $R_i$ in the DCO timing counter then can be calculated as follows:

$$[Q_i \cdot 2^i + R_i] = \left\lceil \frac{C_i}{T_{DCO}} \right\rceil \tag{4.6}$$

where $T_{DCO}$ denotes the cycle time of DCO generated frequency.

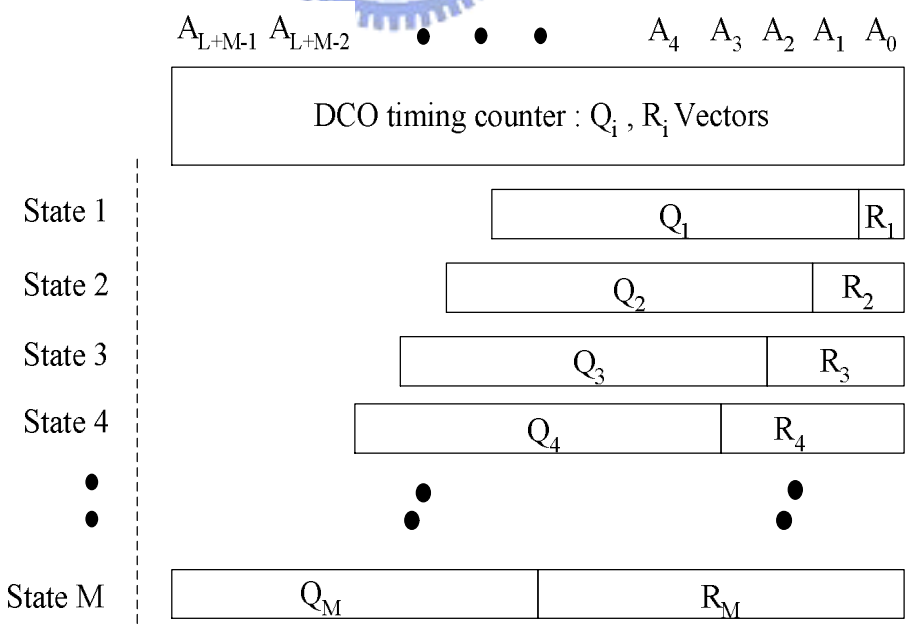



Fig. 4.8. Structure of quotient and remainder vectors in the DCO timing counter.

### 4.2.3 Structure of DFC Loop Controller

The structure of the DFC loop controller is shown in Fig. 4.9. The decision unit performs the digital arithmetic comparisons and updates the DCO control word (DCW). The decision unit compares the DCO timing counter based on frequency sampling period with power-of-2 input reference clock cycles as shown in Fig. 4.3. The decision unit also controls the frequency acquisition process and fine-tuning process. During the acquisition, loop gain control with binary search is applied to achieve fast locking. A multiplexer is used to select the DCO control code. Fig. 4.10(a) illustrates the state transition diagram of the DFC loop controller for frequency search.

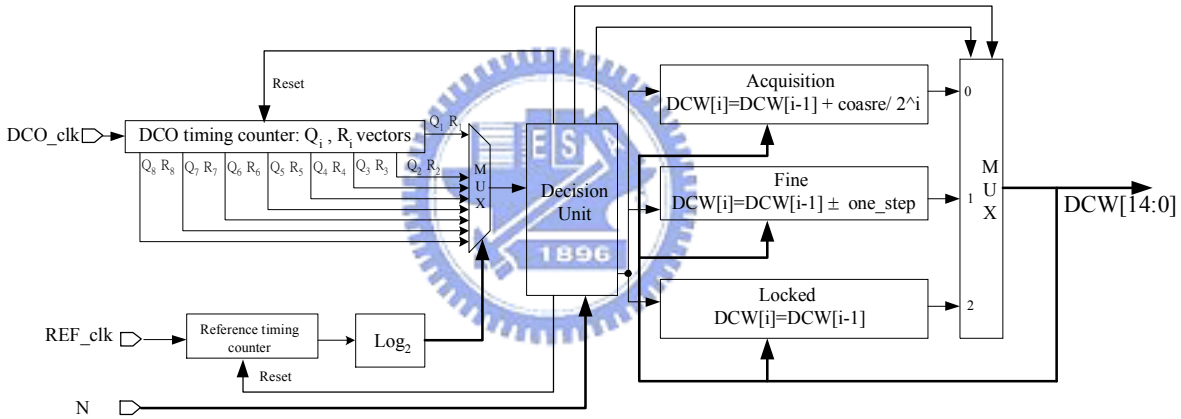



Fig. 4.9. Structure of the proposed DFC loop controller.

Figure 4.10(b) illustrates the state transition diagram of the DFC loop controller. Sampling state 0 is the initial state, and both reference timing counter and DCO timing counter are reset in this state. After a sampling period of $2^1 \times T_{REF}$, the DFC loop controller will switch from sampling state 0 into sampling state 1 for frequency comparison. If the quotient vector in DCO timing counter equals multiplication factor (N) and the frequency error in remainder vector is below the threshold region, state 1 enters into state 2 until $2^2 \times T_{REF}$ sampling period and the DCO control word is left unchanged. Otherwise, the DFC loop controller changes the

DCW depending on the frequency comparison result. Then, it also switches back to sampling state 0 and reset both reference and DCO timing counters. The other DFC sampling states also perform similar operation as well except the maximum DFC sampling state. When the DFC loop controller enters the maximum DFC sampling state M, it will automatically switch back to sampling state 0.

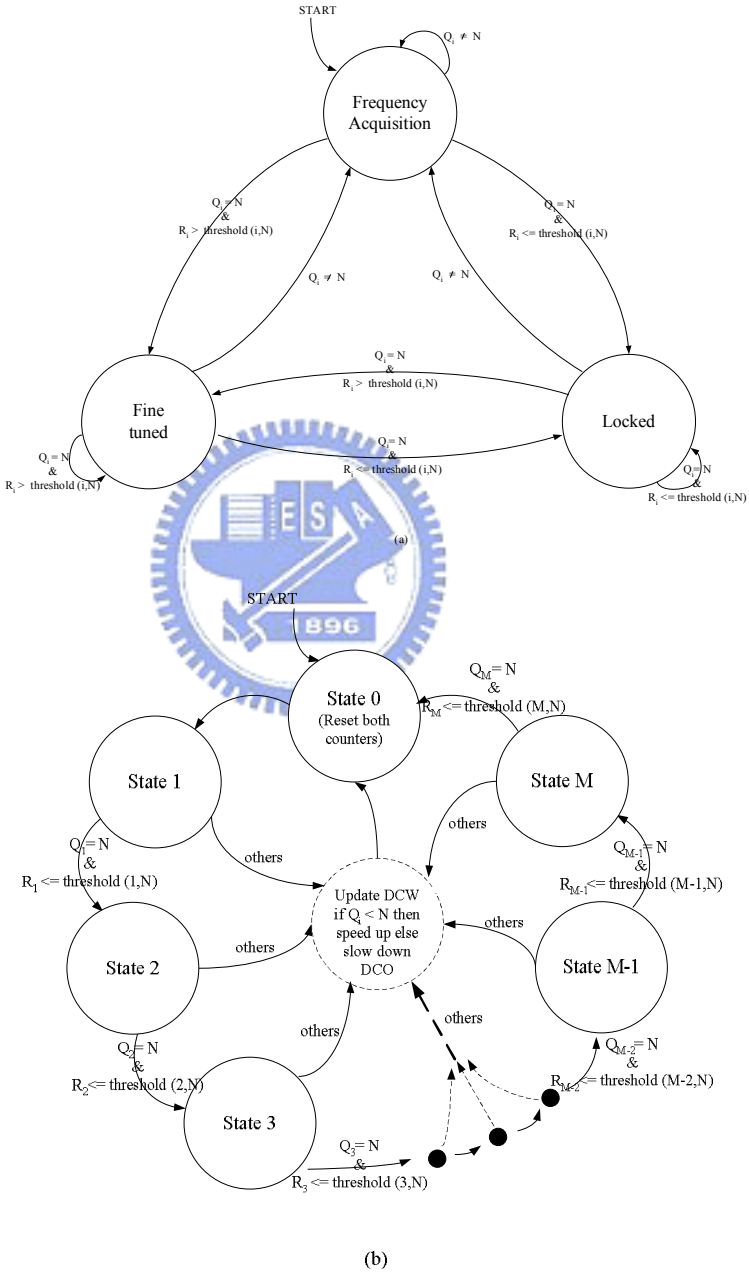



Fig. 4.10. State transition of the proposed DFC loop controller (a). State of frequency search. (b). State of sampling period.

## *4.3 Analysis of the Proposed DFC Algorithm*

### 4.3.1 Error of Frequency Detection

The frequency error rate must be evaluated for the proposed DFC loop control algorithm. If target frequency is N times of reference clock and *i* is *i*-th state, the $Q_i$ vector will be N and the $R_i$ vector will be zero. This is related to

$$C_i = (2^i \cdot Q_i + R_i) \cdot T_{DCO} \quad (4.7)$$

which is based on the ideal condition without jitter variation. Under normal operation, a timing offset error of $\varepsilon_1$ and $\varepsilon_2$ occurs when the $Q_i$ vector is N and the $R_i$ vector is zero based on the DFC method. The time of $C_i$ is expressed as follows:

$$C_i - \varepsilon_1 < C_i < C_i + \varepsilon_2. \quad (4.8)$$

Consequently, the timing error ratio of $C_i$ equals $\{(\varepsilon_1+\varepsilon_2) / C_i\}$, and the maximum value of $(\varepsilon_1+\varepsilon_2)$ is equal to $(2 \cdot T_{DCO})$. Consequently, the maximum frequency error ratio in percentage term can be expressed as:

$$\text{Frequency error ratio} = \{1/[2^{i-1} \cdot N]\} \cdot 100\ \%. \quad (4.9)$$

If the maximum number of DFC sampling state set to 8 (that is *i*=8) and the multiplication factor N is set to 2, the frequency error ratio is less than 0.39 %. The frequency error ratio then varies inversely with input multiplication factor N. Consequently, the proposed mechanism performs better frequency detection for large multiplication factor N under the ideal condition.

### 4.3.2 Jitter Variation and Threshold Decision

Considering the influence of jitter variation on frequency detection, an average processing and a threshold region scheme can be applied to solve such imperfection. For simplification and without losing generality, the average frequency period following *n* cycles can be represented as

$$\overline{T} = T_{ideal} + \frac{\sum_{j=0}^{n-1} T_{jitter(j)}}{n}. \quad (4.10)$$

The $T_{ideal}$ denotes the period of the jitterless clock or the named perfect frequency period, while $T_{jitter(j)}$ represents the frequency jitter in the *j-th* cycle. All of jitters are assumed to be independent and identically distributed (i.i.d) in statistics. The jitter factors can be reduced to an acceptable range when average *n* is large. Therefore, Eq.(4.6) can be rewritten by using (4.10):

$$[2^i \cdot Q_i + R_i] = \left\lceil \frac{2^i \cdot \overline{T_{REF}}}{\overline{T_{DCO}}} \right\rceil = \left\lceil \frac{2^i \cdot \left( T_{REF\_ideal} + \frac{\sum_{j=1}^{2^i} T_{REF\_jitter(j)}}{2^i} \right)}{T_{DCO\_ideal} + \frac{\sum_{j=1}^{N*2^i} T_{DCO\_jitter(j)}}{2^i \cdot N}} \right\rceil$$

$$\approx 2^i \cdot N + \text{threshold}(i, N). \quad (4.11)$$

Both $T_{DCO\_ideal}$ and $T_{REF\_ideal}$ denote the ideal period of DCO output and input reference frequency. Similarly, $T_{DCO\_jitter(j)}$ and $T_{REF\_jitter(j)}$ represent the frequency jitter of the DCO generated clock output and reference frequency in the *j-th* individual cycle. Therefore, a threshold value can be defined to solve the jitter variation. The value of threshold(*i*,N) can be set based on different state *i* and input multiplication factor N. The value of threshold(*i*,N) can not be too large; or else the frequency detection error will be too large. To simplify the hardware cost of the threshold decision unit in the DFC loop controller, threshold(*i*,N) is set to 8 for all input multiplication factor N and states. The average frequency threshold ratio

(AFTR) is the threshold value over the total accumulated frequency value in the DCO timing counter. It can be expressed as follows:

$$\text{AFTR}(i) = \frac{Threshold(i,N)}{2^i \cdot N} = \frac{8}{2^i \cdot N}. \quad (4.12)$$

The average frequency threshold ratio reduces with increasing state and multiplication factor N. Therefore, dynamic frequency error with variable frequency sampling period can be accomplished using the proposed DFC loop control.

## *4.4 Simulations*

Figure 4.11 shows the gate level simulation of proposed DFC loop. The control bit of the DCO is 15-b. The finest resolution is 1.55ps. The reference clock is 1MHz with standard deviation 1ns, and the multiplication factor is 127. Thus, the output frequency is 127 MHz(=1MHz *127). When RESET=0, the DFC loop starts to work. The DCW is changed according to the result of frequency comparison following 2 $T_{REF.}$ Next DCW is DCW[14:0] + step[14:0] or DCW[14:0] – step[14:0], and initially the step is 4000H. The cycle period is 7.85 at the 28 the reference cycle as indicated in Fig. 4.11. By using binary search step for frequency acquisition, the worst-case time complexity of the frequency synthesizer is equal to

$$\begin{aligned} T(n) &= T_{fine}(n) + T_{coarse}(K) \\ &= T_{fine}(n/2) + P(n) + O(\log_2 K) \\ &= T_{fine}(n/2) + O(1) + O(\log_2 K) \\ &= T_{fine}(n/2^K) + k + O(\log_2 K) \\ &= O(\log_2 nK) \end{aligned}$$

where K is total number of steps in a coarse search, P($n$) is the time complexity of the last step, and $T_{fine}(n)$ and $T_{coarse}(K)$ is the time complexity of binary search algorithm for fine and

coarse searches, respectively. So the lock-in time is equal to (A*$\log_2$ $n$K), where A is a constant for frequency lost.

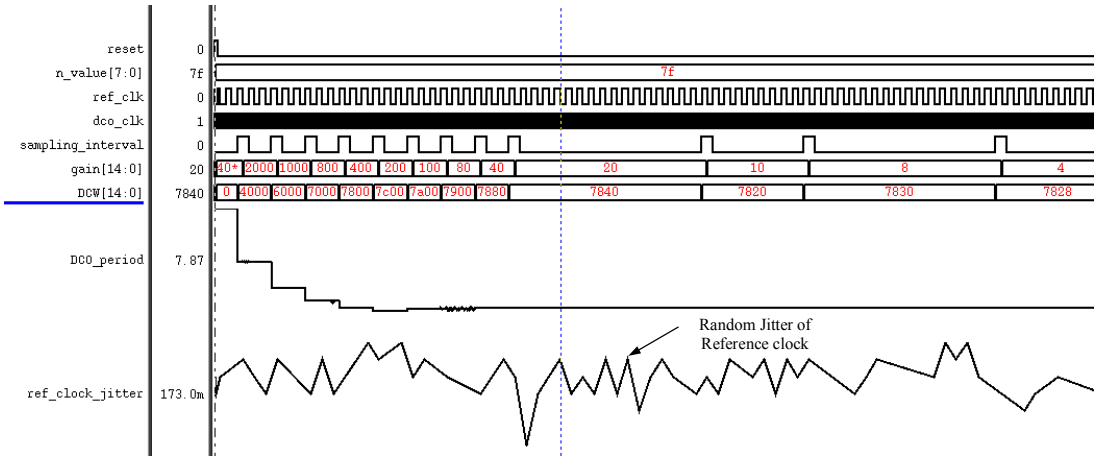



Fig. 4.11. Verilog simulation of the proposed DFC loop control, reference clock=1 MHz, N=127.

Figure 4.12 shows the simulation of proposed DFC loop as compared with fixed sampling period with 8 reference clock cycles, where N=2, reference clock=20MHz (50ns) with 1 ns standard deviation. The target clock period is 25ns. The fixed sampling period with 8 reference clock periods could not lock correctly. Table 4.1 shows the simulation with other sampling periods. The final locked clock period is 24.9ns for both sampling period with 128 and 256 in table 4.1.

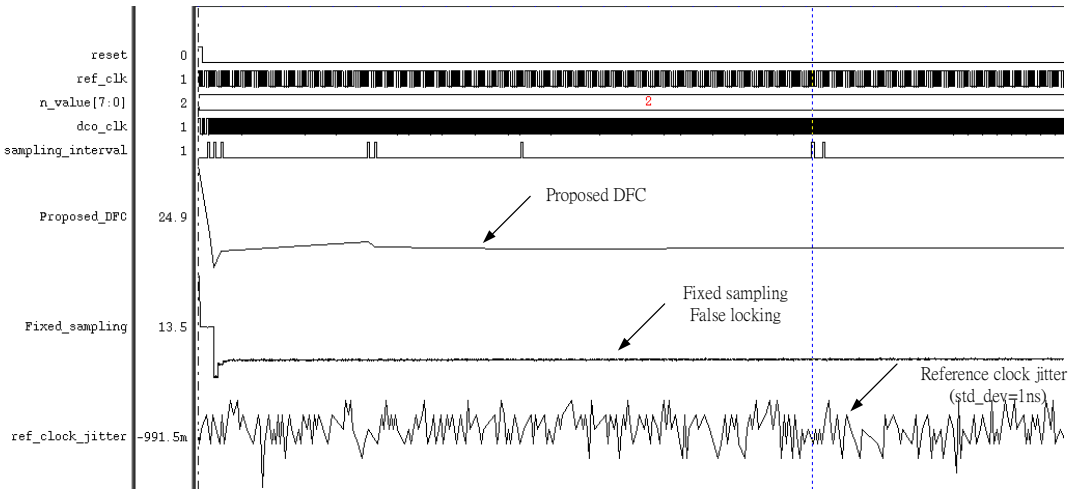



Fig. 4.12. Proposed DFC loop V.S. fixed sampling clock = 8 when N=2, reference clock=20MHz.

Table 4.1. Fixed sampling period V.S. locked cycle period.

| Fixed sampling period | Locked cycle period (ns) |
|---|---|
| 8 | 13.4 |
| 16 | 23.7 |
| 32 | 23.9 |
| 64 | 24.5 |
| 128 | 24.9 |
| 256 | 24.9 |

Figure 4.13 shows the simulation of proposed DFC loop with input 10MHz, N=10 and peak-to-peak jitter 27ns (27%). The output clock is 100MHz with peak-to-peak 8.96% of output clock period. It is 9.58dB improvement without using the TDC circuit. Other simulations were also performed with different multiplication factors N=20 and N=40. Simulations with different input frequencies were also performed in table 4.2. In addition, our proposed DFC can reduce the input jitter.

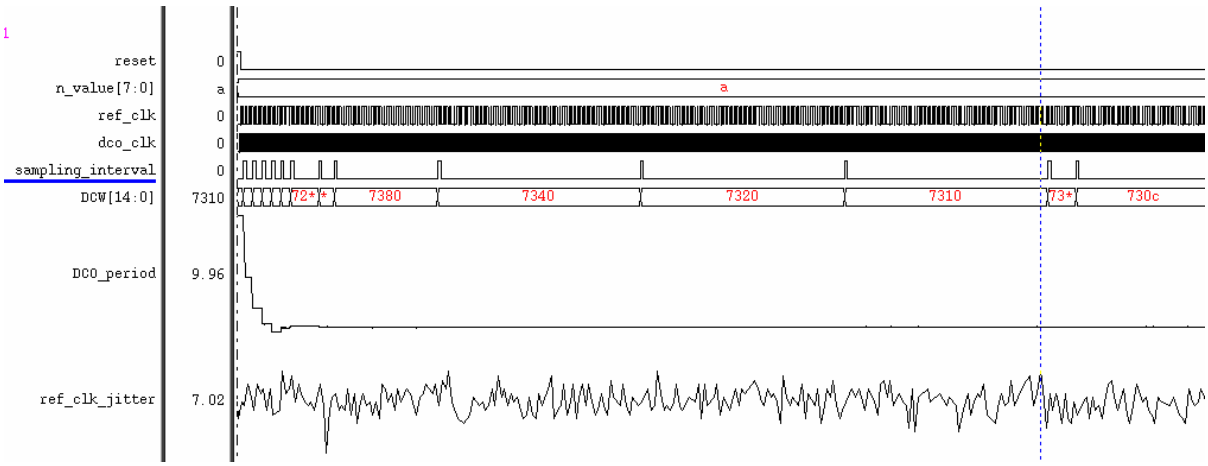



Fig. 4.13. Proposed DFC loop with reference clock at 10MHz with peak-to-peak jitter 27% over clock period and N=10, output frequency at 100MHz with peak-to-peak jitter 8.96% over output clock period.

Table 4.2. Simulations with different input frequencies and multiplication factors.

| Input Frequency | Input Jitter (clock period) | N | Output Jitter (clock period) | Jitter improvement |
|---|---|---|---|---|
| 10MHz | 27% | 10 | 8.96% | 9.58dB |
| 10MHz | 27% | 20 | 10.8% | 7.95dB |
| 10MHz | 27% | 40 | 17.48% | 3.77dB |
| 20MHz | 54% | 10 | 8.66% | 15.03dB |
| 20MHz | 54% | 20 | 19.76% | 8.73dB |
| 2MHz | 5.4% | 10 | 0.998% | 14.66dB |

## *4.5 Experimental Results*

The proposed dynamic frequency counting (DFC) loop was verified at first in 0.35μm 2P4M CMOS. The microphotograph is as shown Fig. 3.17. The gate count of DFC loop is 1458. The chip provided frequency measurement around 48MHz in closed loop mode because the design constraint in logic synthesis was set to 50MHz. Then, the DFC loop was verified in the 0.18-μm 1P6M CMOS by the chip of cascaded loops in Fig. 5.10.

Fig.4.14 was measured from 0.35μm chip. Fig. 4.14(a) shows the test result with N=48, external reference clock at 1MHz with peak-to-peak jitter 260ps, and test output at 24.07MHz with peak-to-peak jitter 70ps. Fig. 4.14(b) shows the test result with N=192, external reference clock at 250KHz with peak-to-peak jitter 300ps, and test output at 24.02MHz with peak-to-peak jitter 60ps (DCO output at 48.04MHz). It has shown that the input jitter can be reduced by the proposed DFC approach.

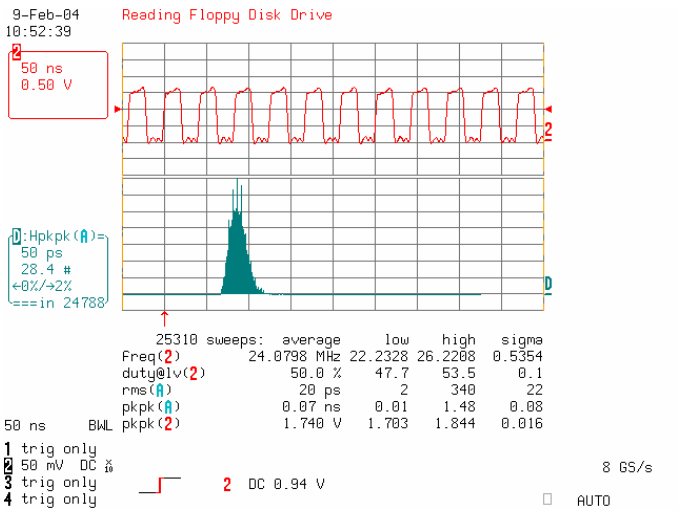



Fig. 4.14(a). Measured result with multiplication factor N=48, reference clock = 1MHz with peak-to-peak jitter 260ps, and test output=24.07MHz with peak-to-peak jitter 70ps (DCO output at 48.14MHz).

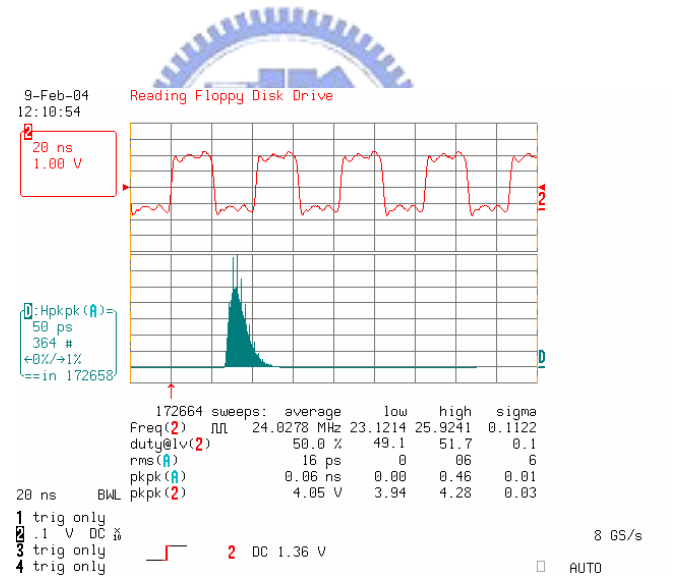



Fig. 4.14(b). Measured result with multiplication factor N=192, reference clock = 250KHz with peak-to-peak jitter 300ps, and test output=24.02MHz with peak-to-peak jitter 60ps (DCO output at 48.04MHz).

Fig. 4.15 shows the test result with N=128, external reference clock at 2.4MHz with peak-to-peak jitter 220ps, and test output at 153.9MHz with peak-to-peak jitter 70ps (DCO

output at 307.8MHz). Fig. 4.15 was measured from 0.18-µm chip in Fig. 5.10.

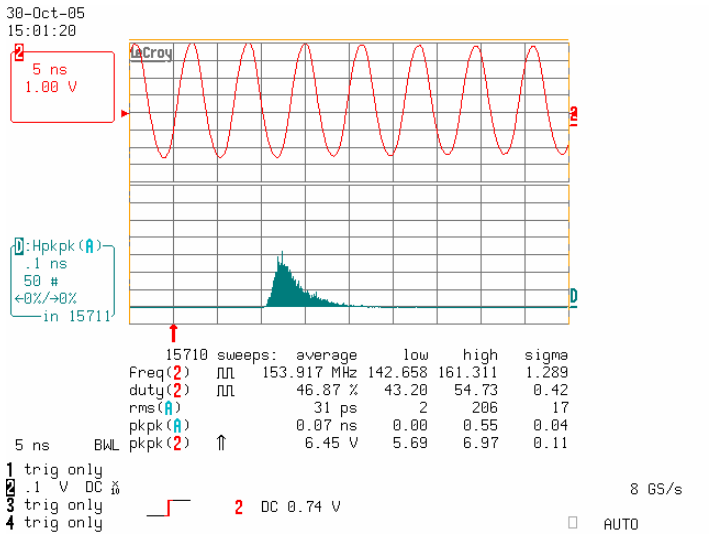



Fig. 4.15. Measured result with multiplication factor N=128, reference clock = 2.4MHz with peak-to-peak jitter 220ps, and test output=153.9MHz with peak-to-peak jitter 70ps (DCO output at 307.8MHz).

Figure 4.16 compares the measured error ratio of DCO output at 48MHz based on 0.35-µm chip with that for (4.12), for which $i$ is set to 8. Better frequency accuracy can be achieved by using larger multiplication factor N. The measured results are consistent with the above analysis in section 4.3.1.

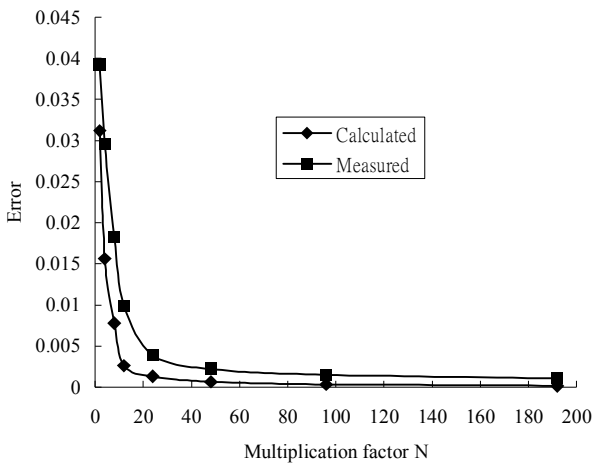



Fig. 4.16. Measured average frequency error v.s. calculated by (4.12) (Output test at 24MHz, internal DCO at 24MHz x 2 =48MHz).

## *4.6 Summary*

In this chapter, a DFC control algorithm for clock generator is presented. The proposed dynamic frequency counting process can eliminate the jitter and noise associated with the input reference clock. The proposed novel mechanism is implemented with a reference timing counter, DCO timing counter and DFC loop controller. Additionally, the frequency error ratio and threshold are also derived. Simulation has been performed to compare different sampling techniques or structure. Based chip measurement, the error of measured frequency is consistent with the analysis. The results achieved by using larger multiplication factor N will be better. This proves the effectiveness of proposed dynamic frequency counting loop.

# Chapter 5

# Clock Generation with Cascaded DFC Loops for Wide Multiplication Range Applications

In this chapter, clock generation for wide multiplication range applications with cascaded dynamic frequency counting (DFC) loops is proposed [66]. The DFC loop as described in chapter 4, which uses variable time period to estimate and tune the frequency of digitally controlled oscillator (DCO) enhances the resolution of frequency detection. A simple up counter can operate faster and with lower cost than a programmable divider [67]. However, the loop stability is deteriorated when divider ration N is increasing. In order to retain the loop stability, we proposed cascading two DFC loops in series. The proposed all-digital clock generator is designed on 0.18-μm complementary metal oxide silicon (CMOS) process.

The rest of this chapter is organized as follows. Section 5.1 is the introduction. Section 5.2 addresses the loop design issues in cascaded DFC loops for wide multiplication range. Session 5.3 then describes the structure of DCO 1 and high resolution DCO 2 with digitally controlled varactors (DCV). Subsequently, chip measurement results of the proposed clock generator with cascaded DFC loops are discussed in section 5.4. Finally, section 5.5 offers a summary and conclusions.

## *5.1 Introduction*

Programmable multifunction unit clock generator is getting more interests for system-level integration, including processors and video/chip interfaces [15,19]. In conventional approaches [1-10] as described in chapter 2, PLL is used to generate different high frequency output with low frequency crystal clock by setting the multiplying factor (i.e. divider ratio N). When in terms of lowering cost and improving stability as indicated in [51], a CR-oscillator can be built in the IC to realize a stable clock in a low-frequency around 10 KHz. Thus the external reference clock such as crystal can be eliminated. However, high speed clock output is still required (e.g. 100 MHz). In this situation, frequency multiplication ratio becomes very large (e.g. 10000). The multiplication ratio is also over 6000 for a signal generator with input frequency of 32.768 KHz as indicated in [52]. As the input to output multiplication factor increases, the prior art PLL [7-10,12] became more sensitive to noise sources and result in additional jitter in the output. Thus, this work attempts to propose an all-digital cell-based clock generator for wide multiplication range frequency synthesis by using the proposed cascaded dynamic frequency counting loops.

While charge pump PLL as illustrated in Fig. 2.5 offers flexible frequency multiplication, the loop parameters, such as damping factor, loop bandwidth, must be adjusted to minimize jitter and to guarantee stability simultaneously for each output frequency and multiplication factor. The loop bandwidth should be about 1/20 of the reference frequency as indicated in [34]. To minimize period jitter, the third-order pole should be set about 1/2 of reference frequency. Furthermore, the damping factor $\zeta$ is given (2.9). The damping factor influences the loop stability and the loop bandwidth has a great impact on the response rate of the system. The damping factor should be about 1 in second-order PLL loop [2], which creates challenge for wide multiplication ranges according to (2.9).

In order to handle wide multiplication range, in [12] utilized a current mode filter and [13] decomposed the capacitor C into smaller $C_1$ and $C_2$ with cascaded loop. However, both multiplication factors (N) are under 255. In [11] a scalable charge-pump current as shown in Fig. 5.1 can be used to compensate for the damping factor and bandwidth dependence of the multiplication factor. The multiplication factor (N) of [11] can range from 1 to 4096. Figure 5.2 shows the structure of 12-bit programmable 1/N current mirror. However the proposed architecture leads to design complexity and also has large die area. A signal generator in [52] used a frequency multiplier in the first stage then follow by an analog PLL to achieve multiplication factor over 6000. It required a D/A converter with another high-speed oscillator for frequency multiplier. The approach of [52] also suffers from complex circuits design efforts and has a high cost of chip area.

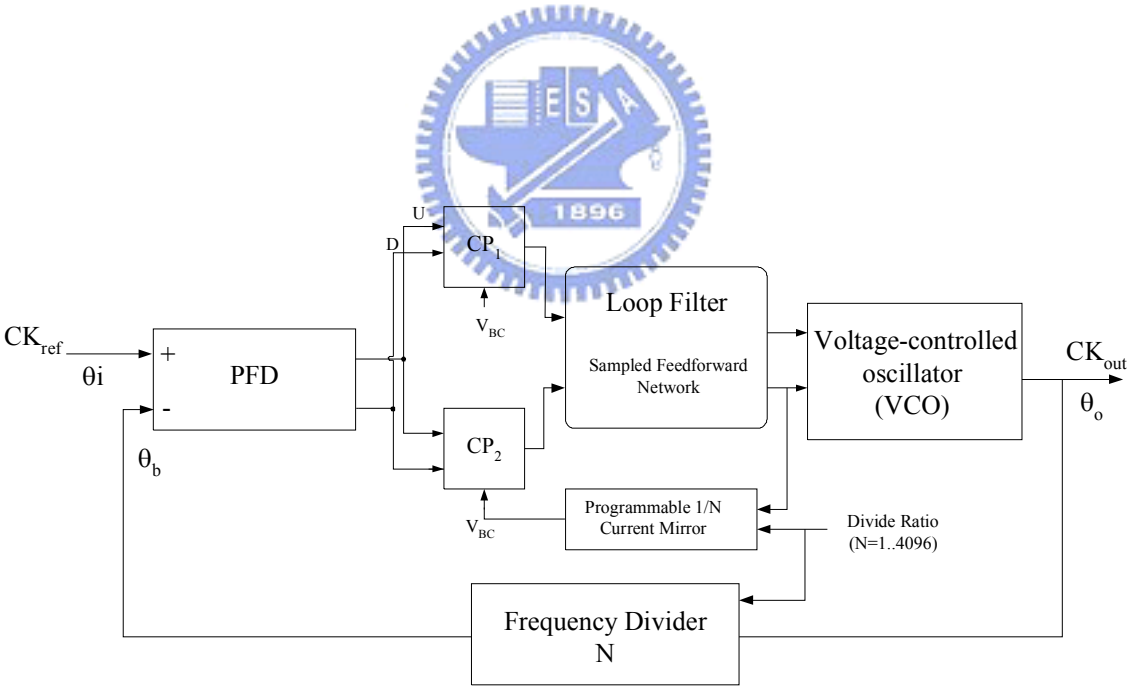



Fig. 5.1. A CP-PLL clock generator with programmable 1/N current mirror [11].

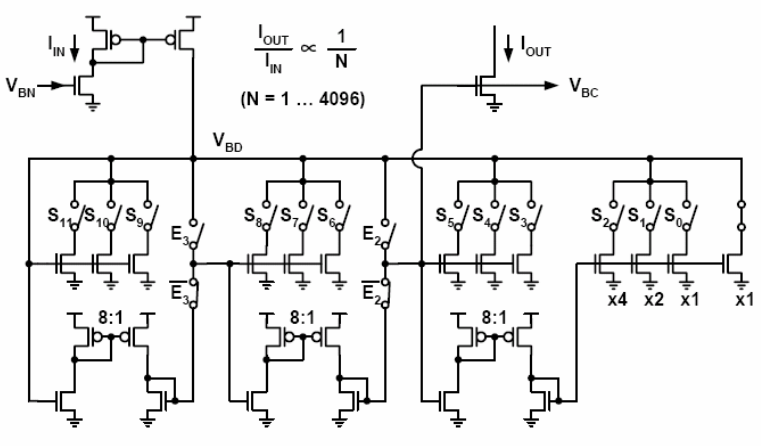



Fig. 5.2. Structure of programmable 1/N current mirror in [11].

This work proposes a cascaded DFC loops for wide multiplication range over 10000 and the lowest input frequency is 19.26KHz. The cascaded DFC loops is formed by two DFC loops in series. Each DFC loop has similar first order transfer function as described in Chapter 4. However, each DFC loop has different loop parameters and requirements of DCO. In order to enhance the resolution of frequency detection, the DFC loop uses variable period to measure and control the DCO output frequency. The variable sampling period is $2^n$ reference clock cycles, where n ranges from 1 to M. The proposed dynamic frequency counting loop can simplify the frequency calculation, and also significantly reduce circuit complexity. The first DFC loop is for generating an intermediate frequency for next DFC loop. This enhances the overall loop stability because the loop gain is reduced by using cascaded DFC loops as compared with a single loop.

The proposed all-digital clock generator for wide multiplication range has been verified in the 0.18-μm 1P6M CMOS process with a frequency range of (2.4~378) MHz at 1.8V. When multiplication factor is less than 13888 with input reference frequency 19.26KHz, the peak-to-peak ($P_k$-$P_k$) jitter is less than 2.8% of output clock period. This demonstrates the effectiveness of the proposed mechanism for wide multiplication range applications.

## *5.2 System Block Diagram and Loop Parameters Design*

### 5.2.1 Issues in DFC Loop When Multiplication N is large

The dynamic frequency counting loop uses variable sampling period to estimate and tune the DCO frequency which enhances the resolution of frequency detection as explained in chapter 4. However, the loop gain K(i) is given by

$$K(i)= K_i \cdot K_{DCO} \cdot 2^i / F_{REF} \quad (5.1)$$

where $F_{REF}$ is the input frequency of reference clock ($CK_{ref}$) and i=0,1,2..M. M is the maximum sampling value. Increase the M value will enhance the resolution of frequency detection as indicated (4.12). However, the stable region of K(i) is 0 ~ 2. It is easy to understand from (5.1) that increasing M value will enlarge the loop gain K(i). Therefore, the M value is in a limited range. In order to describe the impact on multiplication factor (N) on loop gain K(i), (5.1) can be approximately rewritten in the following form

$$K(i) \cong \frac{K_i \cdot \frac{\Delta T}{T_{out}} \cdot F_{out} \cdot 2^i}{F_{REF}} = K_i \cdot \frac{\Delta T}{T_{out}} \cdot N \cdot 2^i . \quad (5.2)$$

The $F_{out}$ is the output frequency and $T_{out}$ is the timing period of output frequency, the $\Delta T$ is the fine tune delay of DCO in (5.2). The loop gain K(i) will be enlarged when multiplication factor (N) increased. For example, $K_i$=1, N=4096, *i*=3, and the target output is 200MHz (T=5 ns), the value of $\Delta T$ should be less than 0.305 ps. If the N is over 10000, then, the resolution of $\Delta T$ should be improved. However, it is very difficult to achieve it.

Another problem is that the length of DCO timing counter will be increased when multiplication factor (N) is increased. This will increase the metastability of DCO timing counter. It will also enlarge the length of comparator. A prudent design procedure to decide the DCO operating range, DCO resolution ($\Delta T$), multiplication factor (N), and maximum

sampling value M as well as the threshold value is listed in the following.

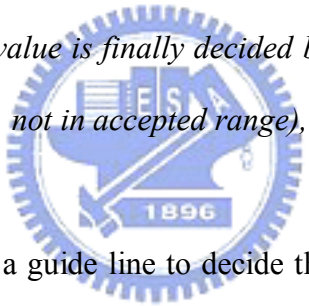
- ***Design Procedure for Loop Parameters***

*Step 1: First decide the basic requirements of input frequency range and output frequency range, then the range of multiplication factor N can be decided (i.e. $N_{min} \sim N_{max}$).*

*Step 2: Decide the resolution of DCO ($\Delta T$), then the number of digital control bit and $K_{DCO}$ can be selected and calculated. If the ($\Delta T$) is less than the timing resolution that can not be achieved by DCV method, then go to step 1.*

*Step 3: The maximum sampling value M can be set by the stability constraint in (5.1). If the value of M is less than 1, then go to step 2.*

*Step 4: The average threshold value is finally decided by (4.12). If the threshold value is less than 2 or too large (i.e. not in accepted range), then go to step 2.*



The design procedure provides a guide line to decide the loop parameters based on proposed dynamic frequency counting method.

## 5.2.2 Cascaded DFC Loops

The basic concept of cascaded DFC loops is similar with design in multistage amplifier. In order to maintain the loop stable for wide multiplication range applications, the transfer function (4.2) can be decomposed into

$$H[z(t)]= \frac{K_1(i)\cdot[z(t_1)]^{-1}}{1-(1-K_1(i))\cdot[z(t_1)]^{-1}} \cdot \frac{K_2(i)\cdot[z(t_2)]^{-1}}{1-(1-K_2(i))\cdot[z(t_2)]^{-1}} . \quad (5.3)$$

Here $K_1(i)$ is the loop gain of the first stage which is equal to ($K_{i1} \cdot K_{DCO1} \cdot 2^i / F_{REF}$), $t_1 =$

$2^i \cdot T_{REF}$, i=0,1,2..$M_1$. Similarly, $K_2(i)$ is the loop gain of the second stage which is equal to ($K_{i2} \cdot K_{DCO2} \cdot 2^i / F_{DCO1}$) and $t_2 = 2^i \cdot T_{DCO1}$, i=0,1,2..$M_2$. Both $M_1$ and $M_2$ are the maximum numbers of DFC sampling state in each loop.

The first stage's DFC loop is for generating an intermediate frequency for next stage. The output frequency range of single DCO can be further divided into two DCO ranges. Therefore, the loop gain $K_1(i)$ and $K_2(i)$ in each DFC loop will have smaller value as compared with single loop. Using cascaded DFC loops makes $K_1(i)$ and $K_2(i)$ easy to be controlled in the stable region instead of using only K(i) in (5.3). In addition, this will not only reduce the length of DCO timing counter and reference timing counter, but also reduce the complexity of DCO design. The proposed cascaded loops generate average output frequency in each stage. Therefore, the output frequency of second stage's DFC loop is still stable due to noise influence or jitter variation in the first stage's DFC loop.

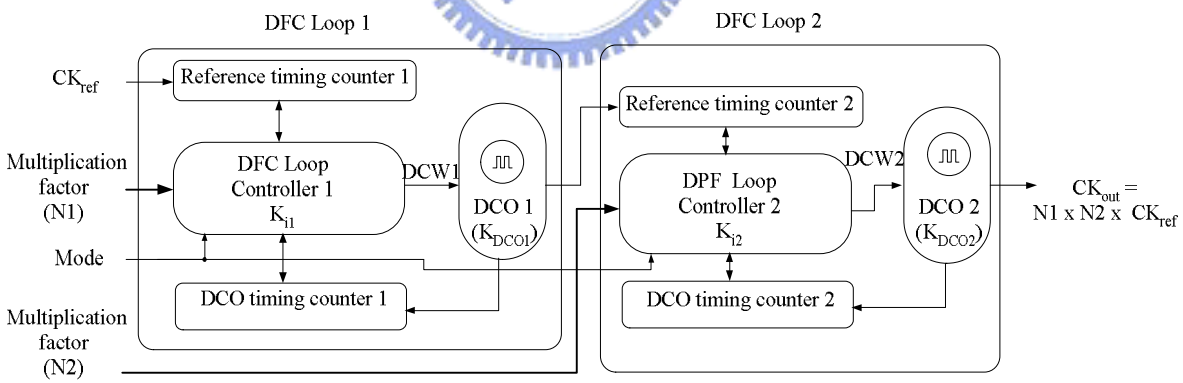



Fig. 5.3. Structure of proposed clock generator with cascaded DFC loops.

Figure 5.3 shows system block diagram of the cascaded dynamic frequency counting loops for wide multiplication range applications. The system consists of two DFC loops in series, called DFC loop 1 and DFC loop 2. The first DFC loop 1 generates low-frequency

output, or intermediate frequencies for the DFC loop 2. DFC loops 1 and 2 have different loop parameters and DCO requirements. DFC loop 1 only requires a low-frequency DCO 1 and a low-frequency detector.

By contrast, the second stage is a high-resolution DCO 2, and also requires a high-resolution frequency detector. Both DFC loops 1 and 2 can be disabled, depending on output requirement, by the mode control. To prevent false locking, the DFC loop 2 is enabled after DFC loop 1 is locked in the acquisition process when two loops are employed. Because the DCO is divided into two DCO ranges, DCO 1 has a smaller control code than the DCO of a single loop, thus shortening the locking time.

To produce the maximum multiplication factor range over 10000 and the lowest input frequency around 10KHz, the multiplication factor (N) needs to be evenly distributed in the first and second stages. Therefore, the multiplication factor (N1) in the first stage's DFC loop is in the range 2~255, and the multiplication factor (N2) in the second stage ranges 2~128. However, the lengths of the reference timing and DCO timing counters are different because of differences between $K_1(i)$ and $K_2(i)$ in (5.11). The variable sampling period in DFC loop improves frequency detection as indicated in (4.12), but also affects the loop stability. After trade-off of (4.12) and (5.3) with simulations, the length of reference timing counter is 4 bits in DFC loop 1 (i.e. $M_1$=4), and is 8 bits in DFC loop 2 (i.e. $M_2$=8). Therefore, the DCO timing counters are 12 and 16 bits long in the first and second stages, respectively. The value of threshold(i,N) is set to 8 in DFC loop 1, and 2 in DFC loop 2. Additionally, the LSB resolutions of DCO 1 and DCO 2 are 65ps and 0.55ps, respectively.

## *5.3 Design of DCOs for Cascaded DFC Loops*

### 5.3.1. Structure of DCO 1

The gain of DCO 1 is 65ps/LSB and the output frequency of DCO 1 is ranging from 2 ~

34 MHz (i.e. 29.4 ~ 500 ns) in the proposed design. It only requires 13 binary weighted control bits and achieves LSB resolution under 65 ps. The LSB resolution of DCO 1 is easy to be implemented by connected two buffers parallel because one buffer delay cell is about 125ps in target 0.18-μm 1P6M CMOS standard cell library. The basic structure of DCO 1 is shown in Fig 5.4, which is controlled by three cascading stages: range selection stage, coarse-tuning stage, and fine-tuning stage. They are controlled by the range selection control code (DCW1[12:7]), coarse-tuning control code (DCW1[6:1]), and fine-tuning control code (DCW1[0]), respectively. The range selection and coarse-tuning stages are implemented using path selector. The difference between these two stages is that the unit delay in range-tuning stage has larger delay than in the coarse-tuning stage. To reduce chip area and power consumption of DCO 1, the unit delay in range-tuning stage is implemented with delay cell provided in the cell library. In those delay cells, the MOS channel length is longer than normal cells. Therefore, they have an extremely larger delay than normal cells. The coarse-tuning cell is simply one buffer delay cell. The fine-tuning stage is 1 bit to control two buffer delay cells connected in parallel. Therefore, DCO 1 is easy to be implemented in standard cell-based design.

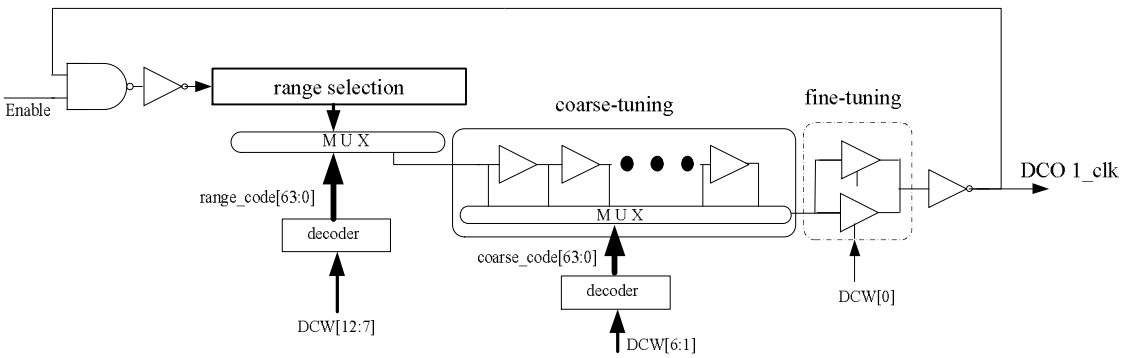



Fig. 5.4. Structure of DCO 1.

### 5.3.2 High Resolution DCO 2 with Digitally Controlled Varactors

High resolution DCO 2 is the key component in the proposed low jitter clock generator for wide multiplication range. To deal with this problem to achieve 0.55ps/LSB, novel DCV using three-input NAND gates for DCO design is proposed in [65]. It uses the parasitic capacitance difference of NAND gates under different digital control inputs to establish a digitally controlled varactor as shown in Fig 5.5. To improve the frequency resolution of the DCO, 256 digitally controlled varactors (DCVs) with different types of NAND gates are used to achieve high resolution. Therefore, DCO 2's LSB resolution for fine-tuning stage can be improved by 256 times as compared with a simple buffer design.

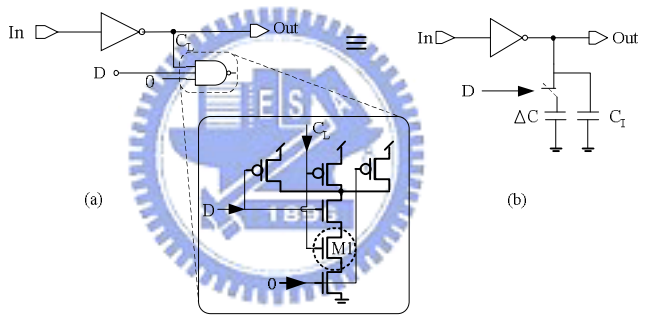



Fig. 5.5. Using three-input NAND gate as DCV. (a) Circuit with digital control. (b) Equivalent circuit with ΔC capacitance.

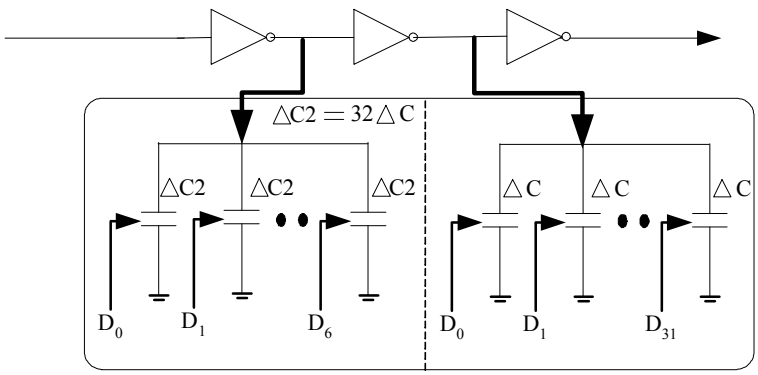



Fig. 5.6. 256 DCVs in the fine-tuning stage of DCO 2.

The structure of DCO 2 is similar with Fig. 5.4. It is also separated into three stages: a range selection, a coarse-tuning stage and a fine-tuning stage. The coarse-tuning stage is the same as in DCO 1. However, DCO 2's range selection cell is smaller than DCO 1's. In addition, the fine-tuning stage is replaced with 256 DCVs as shown in Fig. 5.6. The fine-tuning stage consists of 32 digitally-controlled varactors (DCVs) with capacitance difference ΔC. 32 identical NAND gates with ΔC are used to build one ΔC2 DCV. The total capacitance difference equals to 256 ΔC DCVs. DCO 2 has 16 bits of binary weighted control code ($0000_{16}$ ~ $FFFF_{16}$). The higher three bits of the control code are for the range selection stage and five bits for coarse-tuning stage, while the lower 8 bits are for the fine-tuning stage. The coarse-tuning stage includes 32 buffer stages for delay-chain selection. The output frequency of DCO 2 ranges from 32 ~ 378 MHz This architecture enables the operating frequency of DCO 2 to be easily modified to meet different specifications.

Both DCO 1 and DCO 2 are designed in gate-level Hardware Description Language (HDL) codes. The DFC loop controller is also designed in HDL code and synthesized by a target library. The final circuit layout is generated by auto placement and routing (APR) tools. As a result, the design cycle time is tremendously reduced during process migration.

## *5.4 Experimental Results*

Figure 5.7 show the gate level simulation of proposed cascaded DFC loops for wide multiplication ranges. The reference clock is 500KHz, and the multiplication factor (N1) is 40 and (N2) is 8 as shown in Fig. 5.7 (a). The loop achieves frequency lock after 65 reference clock cycles. And, the reference clock is 10KHz, and N1 is 200 and N2 is 64 is indicated in Fig. 5.7 (b). The DCO 2 is enabled when DCO 1 is locked in order to prevent false lock. The loop is locked after 74 reference clock cycles.

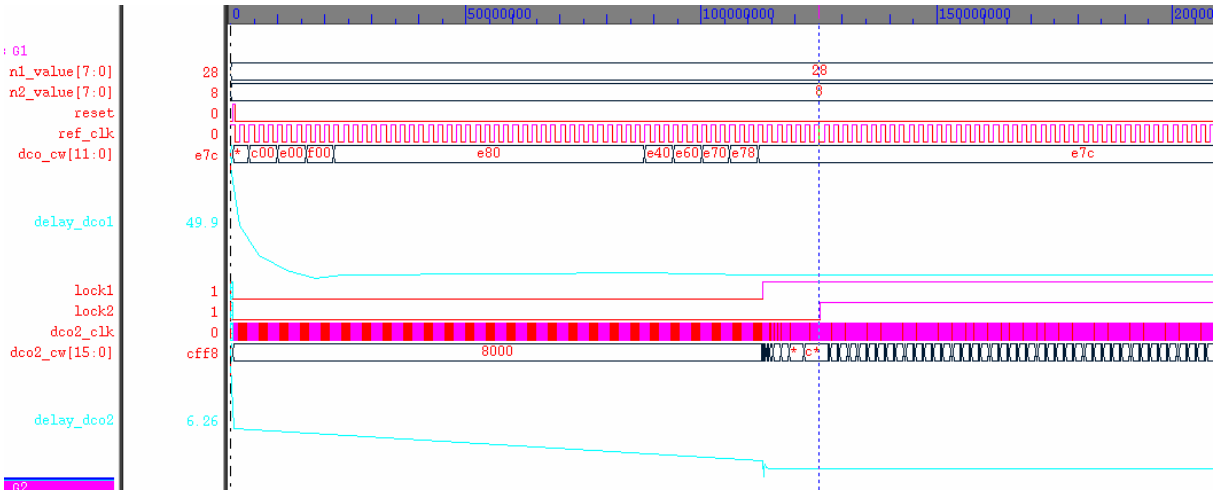



Fig. 5.7 (a). Simulation result with (N=320) N1=40, N2=8, $CK_{ref}$=500KHz, and output=160 MHz.

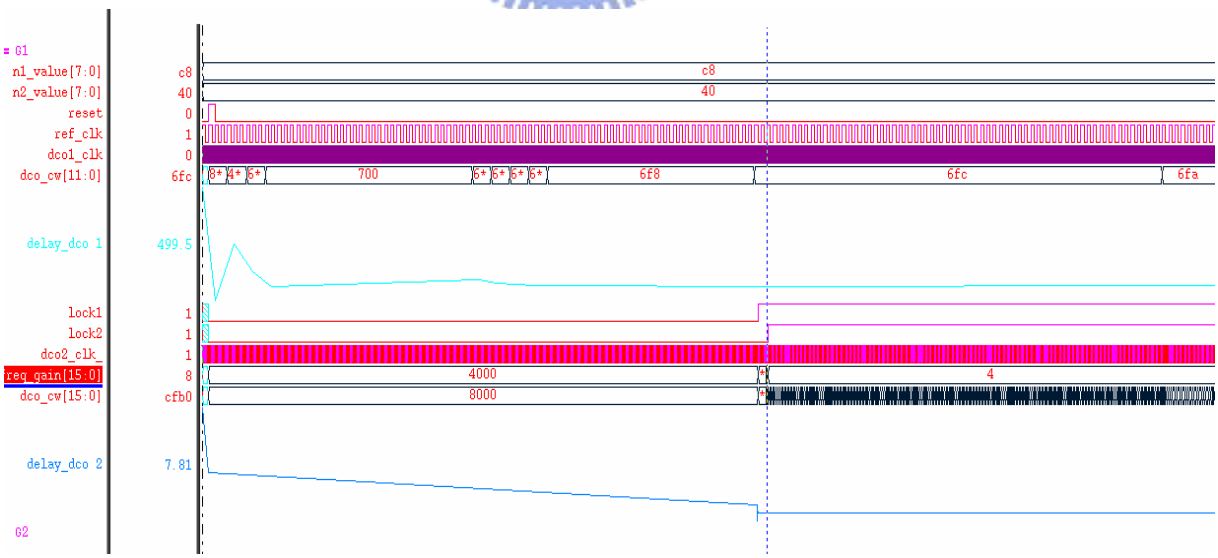
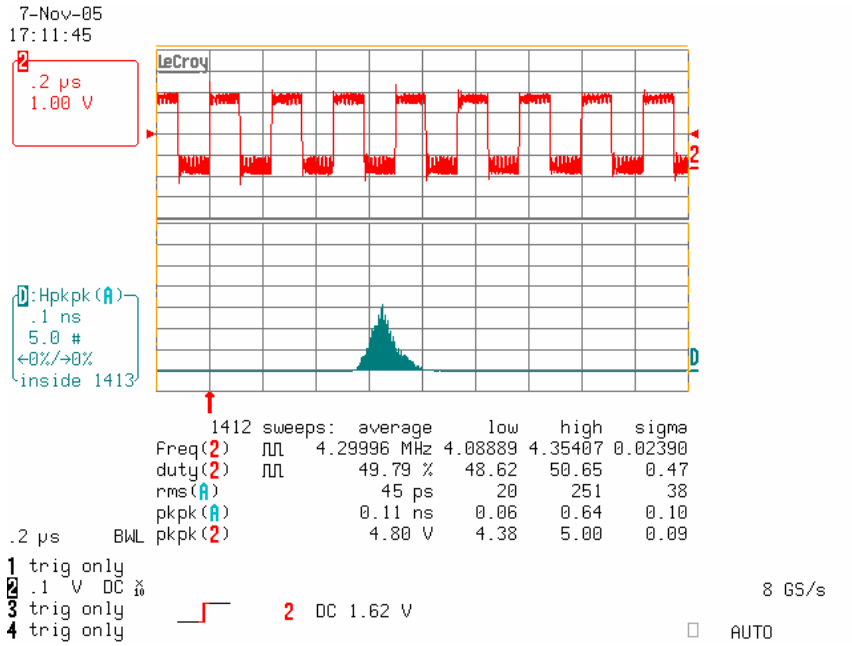



Fig. 5.7 (b). Simulation result with (N=12800) N1=200, N2=64, $CK_{ref}$=10KHz, and output=128MHz.

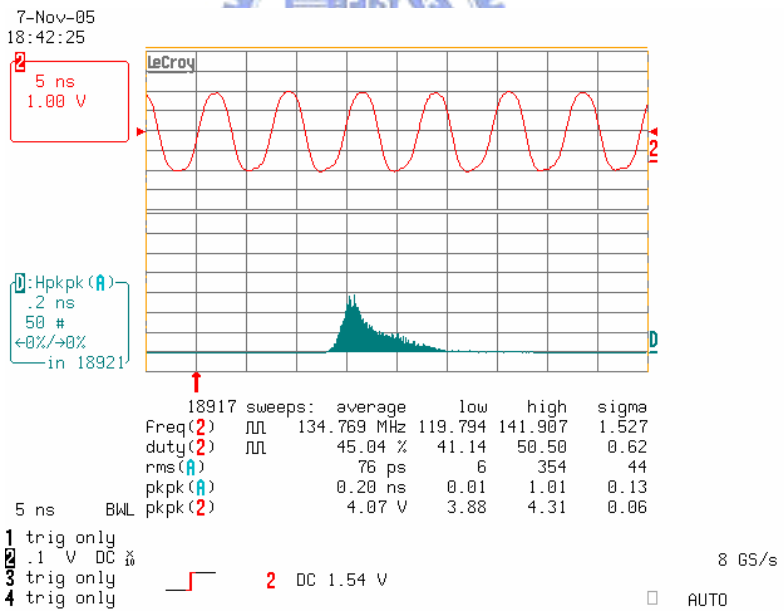
The proposed clock generator with cascaded DFC loops has been laboratory tested under different inputs reference frequencies and multiplication factors. This work uses LeCory LC584A to measure the output frequency given noisy digital circuitry. Fig. 5.8 illustrates the measured results with an input reference frequency of 19.26KHz from an HP-3312 signal generator, multiplication factor N=13888 (i.e. N1 = 224, N2=62) and test output divided by 2 at 134.7MHz under a supply voltage of 1.8V. The signal at Channel 2 displays the DCO generated test output signal (1/2 DCO2), while Channel D shows the long-term cycle-to-cycle jitter histogram. The measured rms jitter and peak-to-peak ($P_k$-$P_k$) jitter of DCO 1 shown in Fig. 5.8(a) are 45ps and 110ps, respectively, and, the measured rms jitter and $P_k$-$P_k$ jitter of DCO 2 shown in Fig. 5.8(b) are 76ps and 200ps, respectively. Fig.5.9 shows the measured long-term cycle-to-cycle jitter of clock output versus multiplication factor (N). The dashed line indicates the output jitter with the input reference clock set to 19.26KHz and different multiplication factors. The solid line shows the output jitter with the test output clock fixed at 134.76MHz and both multiplication factor (N) and input reference clock are changed. The $P_k$-$P_k$ jitter ratio is represented as the percentage of the output clock period, and is always less than 2.8% when multiplication factor (N) is less than 13888. The output clock frequency limits the performance owing to noise induced by the I/O pad transition. When the input clock frequency is set to 19.26 KHz, the $P_k$-$P_k$ jitter ratio increases with the multiplication factor (N), and remains less than 2.8% of output clock period. The output clock period dominates the $P_k$-$P_k$ jitter ratio as output frequency is increased.

The maximum multiplication factor of N1 is 224 instead of 255 owing to the overflow in the DCO timing counter 1, which causes false frequency locking. In addition, the overflow also limits the lowest input frequency of DCO 1. Similarly, overflow also restricts the multiplication factor of N2. To prevent overflow, one more bit has to be extended in the most significant bit (MSB) of (4.4), as well as the DCO timing counter. Bit 0 is added to both

the MSB of multiplication factors N1 and N2 for comparison.




(a)




(b)

Fig. 5.8. Measured results with N=13888 (N1=224, N2=62), REF_clk=19.26KHz. (a) DCO 1 output @ 4.30 MHz (peak-to-peak jitter 110ps). (b). DCO 2 test output @ 134.7 MHz (peak-to-peak jitter 200 ps, DCO 2 output at 269.4MHz).

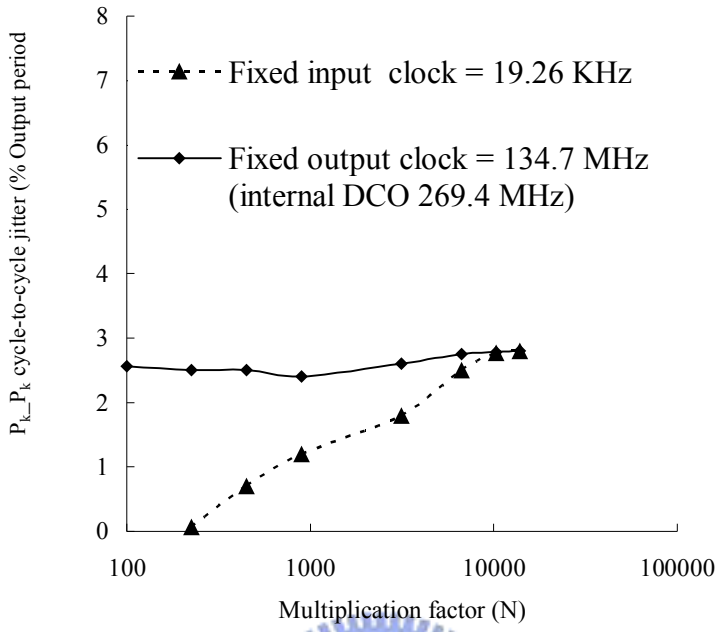



Fig. 5.9. Measured output cycle-to-cycle jitter V.S. multiplication factor (N) for fixed input clock=19.26KHz and fixed output clock=134.7MHz (internal DCO at 269.4 MHz).

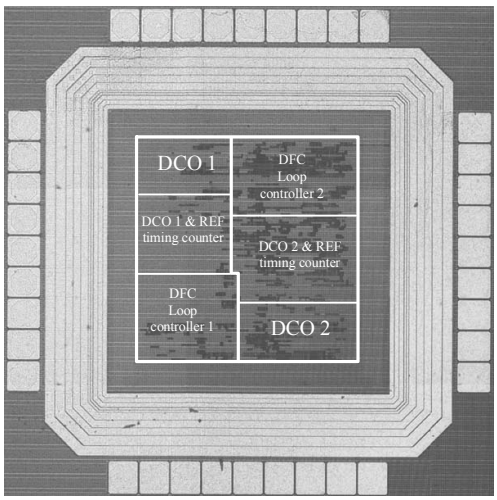



Fig. 5.10. Microphotograph of the proposed clock generator with cascaded DFC loops.

Table 5.1.
Summary of Chip Features
with Cascaded DFC loops

| Items | Specification |
|---|---|
| Technology | UMC 0.18μm CMOS |
| Function | Cell-based clock generator |
| Loop Bandwidth | Dynamic |
| Frequency Range | 2.4 MHz ~ 378 MHz |
| Multiplication Factor | 4 ~ 13888 (5122 cases) |
| Lock-in Time | $A*\log_2(n) <$ 75 cycles |
| Power Consumption | 15 mw @ 378 MHz |
| Power Supply | 1.8 V |
| Gate Count | 6400 gates (700 for testing) |

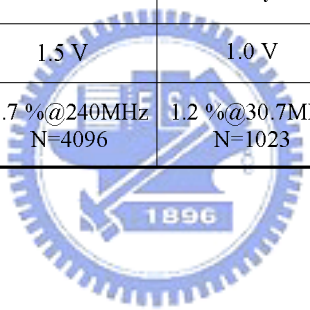
Figure 5.10 displays a chip microphotograph of the proposed design. Table 5.1 lists the summary of chip features. The total gate count is 6400 including 700 gates for scan chain. The gate count of DFC loop 1 and DFC loop 2 is 2540 and 2860, respectively. The core area is 400 x 400 $\mu m^2$. In order to reduce interference of DCO 1 and DCO 2, DCO 1 and DCO 2 are located at left top and right down corners, respectively.

Table 5.2 compares different clock generators with charge pump PLL [11] and all-digital PLLs [50-51,55]. The proposed all-digital clock generator with cascaded DFC loops has wider multiplication range over 10000 among the published PLLs. Furthermore, the chip area is also the smallest among them since neither analog loop filter nor voltage controlled oscillator are used. Although [11,55] had less power consumption because the supply voltage is less than 1.8V. And, their maximum multiplication factors (N) are still less than 5000. Ref. [51] achieves fast locking, but it has poor jitter performance, small multiplication range and its design costs exceed those for the proposed design. The proposed clock generator with cascaded DFC loops is the simplest and has the lowest hardware cost among them.

Additionally, it exhibits better flexibility than other designs in Table 5.2.

Table 5.2. Performance comparison of all-digital clock generator

| Performance Parameter | This work | JSSC 03 [11] | ISSCC 04 [55] | JSSC 03 [51] | JSSC 03 [50] |
|---|---|---|---|---|---|
| Process | 0.18μm CMOS | 0.13μm CMOS | 90nm CMOS | 0.65μm CMOS | 0.35μm CMOS |
| Area | 0.16mm$^2$ | 0.182mm$^2$ | 0.18mm$^2$ | 1.17mm$^2$ | 0.71mm$^2$ |
| Power | 15 mW@378MHz | 7 mW@240MHz | 1.7mW@520MHz | | 100 mW@500MHz |
| Approach | DFC Cascaded loops | 12-b DAC Analog filter | PFD+TDC Digital loop | TDC Digital loop | PFD Digital loop |
| Input Range | 19.26 KHz ~ 60 MHz | | 30 KHz ~ 65 MHz | 11.2 ~ 339.7 KHz | 0.5 ~ 60 MHz |
| Output Range | 2.4 ~ 378 MHz | 30 ~ 650 MHz | 0.18 ~ 600 MHz | 0.0449 ~ 61.3 MHz | 40 ~ 510 MHz |
| Multiplication Factor | 4 ~ 13888 (5122) | 1 ~ 4096 | 1 ~ 1023 | 4 ~ 1022 | 2 ~ 255 |
| Max. Lock time | A*O ($\log_2 n$) < 75 cycles | | > 150 cycles | < 7 cycles | < 46 cycles |
| Supply V*dd* | 1.8 V | 1.5 V | 1.0 V | 5 V | 3.3 V |
| Output Jitter ($P_k$-$P_k$) (% output period) | 2.8 %@134MHz N=13888 | 1.7 %@240MHz N=4096 | 1.2 %@30.7MHz N=1023 | 4.8 %@30.4MHz N=1022 | 3.2 %@450MHz N=137 |



## 5.5 *Summary*

In this paper, a clock generator with cascaded dynamic frequency counting loops for wide multiplication range is presented. The DFC loop is constructed with ripple counters and digital comparator which replaces conventional programmable divider and phase frequency detector. A threshold region is set for jitter variation on frequency detection. Different DCO requirements and loop parameters have been investigated in each DFC loop to maintain loop stability for wide-range multiplication factor (N). A test chip demonstrates that the proposed cascade DFC loops achieves the lowest input reference frequency at 19.26KHz, and the corresponding $P_k$-$P_k$ jitter is less than 2.8 % of the output clock as the multiplication factor (N)

changes from 4 to 13888 with 5122 cases. Hence, the proposed cell-based clock generator with the cascaded DFC loops lowers circuit cost and improves testability. The design can accelerate turnaround time, making it suitable for system-on-chip and low cost applications.

# Chapter 6

# Conclusions and Future Works

## 6.1 Conclusions

Basic concepts of different types of PLL-based clock generator are briefly introduced in this thesis. Then, different DCO structures as well as the resolution-enhancing skills are discussed. A high-resolution DCO based on novel varactors of NAND/NOR gates (2-input or 3-input) has been designed and investigated. The main novelty of the digital controlled varactors is based on capacitance difference of NAND/NOR gates with digital control input. Different configurations of DCV have investigated by using HSPICE circuit simulator under different simulation corners. A simple linear equation can be used to determine the delay resolution. In addition, the delay time can be adjusted by the capability of driving cell and the number of DCVs. The DCVs structure also can be applied in all-digital delay locked loop (DLL) or other applications, such as time-to-digital converter (TDC). A DCO design guide is provided. The operation range of the DCO can be flexible expanded with conventional coarse delay stage and tri-state selection unit. In addition, the final circuit can be generated using an auto placement and routing (APR) tools. The proposed DCO has been designed and fabricated in 0.35μm standard cell library. The DCO operates from 18 ~ 214MHz with average 1.55ps LSB resolution.

Secondly, an algorithm with dynamic frequency counting loop (DFC) has been proposed to enhance the resolution of frequency detection and reduce the jitter associated from reference frequency. The resolution of frequency detection is improved by using two simple

counters with variable sampling scheme to replace conventional phase/frequency detector (PFD) and programmable divider. The sampling period of dynamic frequency counting loop is based on power-of-2 reference clock cycles. The DFC also applied dynamic mean process that can reduce reference input jitter by setting threshold region. The error of frequency detection is investigated. The proposed DFC loop has been simulated and verified both in 0.35μm and 0.18μm chips.

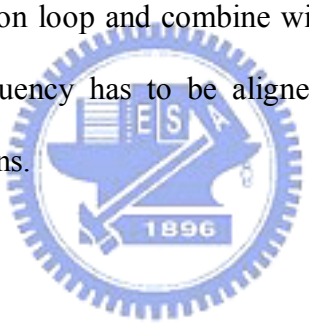
To exploit the DFC loop to be applied in wide multiplication ranges application, a cascaded DFC loops is presented. The loop stability can be easy maintained when two loops are connected in series with different loop parameters. A prudent design procedure for loop parameter is revealed. The DCO range has been divided into two small DCO ranges. This makes the DCO design to be simple, and with fast lock-in time as compared with a single loop. The proposed cascaded DFC loops has been fabricated in the 0.18-μm 1P6M CMOS process with a frequency range of (2.4~378) MHz at 1.8V. The proposed clock generator achieves multiplication factor up to 13888, and the $P_k$-$P_k$ jitter is less than 2.8% of the output clock. The chip area and design complexity is tremendously reduced since no any analog component is need. The total gate count is 6400 including 700 gates for scan chain test.

The above proposed DCO, DFC loop, and a cascaded loop all have been verified with silicon. The all-digital methodology provides a high system-integration efficiency and a short system turnaround time during process migration. As a result, the proposed portable DCO, DFC loop, and cascaded DFC loops are suitable for on-chip clock generation as demanded in current SoC design.

## 6.2 *Future Works*

The following topics to extend the work can be proposed.

- Enhance the resolution of frequency detection by continuing phase accumulation [41] instead of by time accumulation, then, average the phase accumulation to achieve higher resolution. This can be achieved easily by adding another adder to the proposed DFC loop. This will enhance the loop stability.
- To design an all-digital multi-phase clock generator based proposed DCO with modification. Multi-phase clocks are useful in many applications such as high-speed serial link as indicated in [30,43].
- Add another phase detection loop and combine with the DFC loop for phase alignment. The phase of output frequency has to be aligned with the input reference clock for synchronization applications.



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# Publication Lists

## Journal Papers

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