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Series Resistance and Mobility Extraction Method in Nanoscale MOSFETs

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This paper presents a BSIM-based method for source/drain series resistance and mobility extraction in nanoscale strained-silicon metal oxide semiconductor field effect transistors (MOSFETs) with halo implants. This method is more accurate than the conventional channel-resistance and shift and ratio method because it considers the gate-length dependence of mobility caused by local uniaxial stress and laterally nonuniform channel doping. We have verified this method using samples with different stressor/doping conditions and good agreement with experimental data has been obtained. The accuracy of the Berkeley Short-channel IGFET model (BSIM) R_{sd} extraction method is also proven by simulated current–voltage characteristics with different external resistant values. Significant mobility degradation in the short-channel regime has been observed for various uniaxial stressors. This method may serve as a suitable process monitor tool for ultrashallow junction and strained process development.
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As strained-silicon and ultrashallow junction (USJ) techniques are widely used to optimize the carrier velocity and parasitic resistances in metal oxide semiconductor field effect transistors (MOSFETs), an accurate determination of the parasitic source/drain series resistance (R_{sd}) for these nanoscale MOSFETs becomes a crucial issue. Because the series resistance may counteract the mobility enhancement in these strained devices, an accurate R_{sd} value has to be used in the extraction of intrinsic effective mobility (μ_{eff}) during process development. Furthermore, the R_{sd} parameter is critical to evaluate the performance of USJ engineering works.

Among several studies regarding R_{sd} extraction in the past,[1-4] Kim et al.[1] proposed an integrated methodology to separate R_{sd} components and utilized the conventional channel-resistance method in the determination of R_{sd}. Although the channel-resistance method has been widely used,[1,2] it is no longer suitable to nanoscale strained-silicon MOSFETs with halo implants because the laterally nonuniform channel doping as well as uniaxial stress may result in a total resistance (R_{tot}) which does not scale linearly with gate length (L_{TEM}).[5] It is difficult to determine R_{sd} accurately from the nonlinear R_{tot} vs L_{TEM} characteristics.

Another popular method, shift and ratio, is also unsatisfactory because its basic assumption that μ_{eff} is independent of L_{TEM} is no longer valid.[3] The uniaxial stress that may increase as L_{TEM} decreases tends to increase the mobility of short-channel devices, while the halo overlapping profile may degrade the mobility of short-channel devices.[6] Therefore, an adequate method that may accurately determine R_{sd} for nanoscale strained-silicon MOSFETs with halo implants is sorely needed.

In this work, we tackle this problem by a BSIM-based method.[7] Using this method, R_{sd} and μ_{eff} (L_{TEM}) can be extracted well in nanoscale strained devices. The extracted μ_{eff} (L_{TEM}) may also serve as a process monitor for future strain engineering techniques.

Devices

The devices used in this experiment were fabricated by state-of-the-art integrated circuit manufacturing technology,[8] which provides transistors with gate lengths ranging from 4 μm down to 41 nm with the same channel width (W = 1 μm) on 300 mm bulk substrate. A 1.2 nm nitrided gate oxide was used as a gate dielectric. Processes with ultralow highly doped extension energy and unique spike rapid thermal annealing conditions were used to maintain good short channel effect control and high activation rate simultaneously. In this study, devices with different extension dosage and various stressors (tensile/compressive/neutral) in n-channel metal oxide semiconductor (NMOS) were adopted to verify this extraction methodology. The test keys constituted by the transistor arrays and calibration patterns are designed for capacitance–voltage (C-V) measurement. Transistor arrays with source/drain tied together can provide enough area to characterize the capacitance in nanoscale devices. Moreover, we have used a high-frequency probing system to improve the accuracy and stability of C-V characterization results.

Methodology and Discussion

Figure 1 shows the main procedure of our proposed BSIM-based R_{sd} and μ_{eff} extraction methodology. Table I provides the related information for key parameters. Please note A_{bulk} is one parameter in BSIM3 which is used to take into account bulk charge effect. As the drain bias is large or the channel length is long, the depletion width

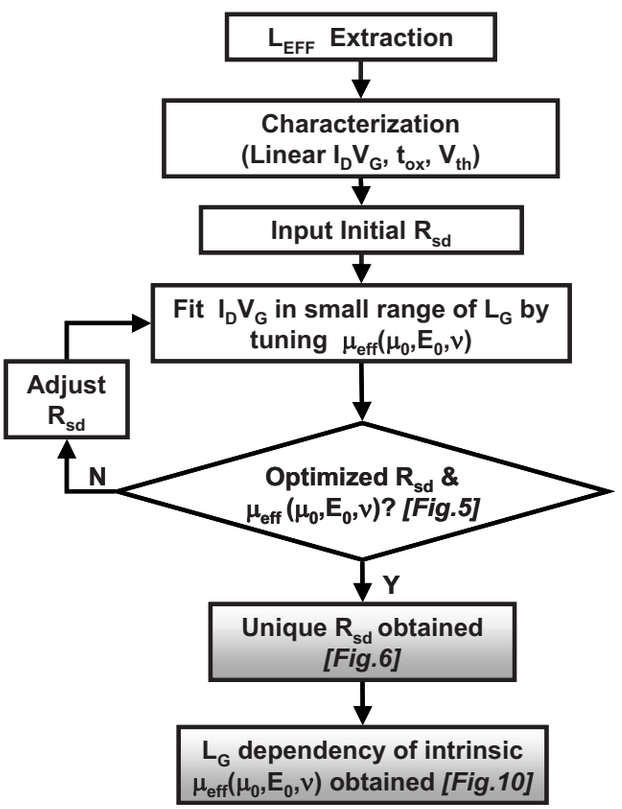

Figure 1. Flow chart of the BSIM-based R_{sd} and μ_{eff} extraction method.

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Table I. Definition of key parameters.

Parameter table	Symbol	Definition
Input parameter	I_D	Drain current in linear region
	C_{gc}	Gate oxide capacitance
	L_{ov}	Gate-extension overlap distance; extracted from C_{gc} and C_{ov}
	L_{TEM}	Obtained from L_{SEM}-ΔL. L_{SEM} is from in-line measurement. ΔL is a constant offset between L_{TEM} and L_{SEM}
	L_{eff}	L_{TEM}-2 * L_{ov}
	μ_{eff}	Effective mobility; need to calibrate with R_{sd} by iterations
	V_{th}	Threshold voltage from measurement
	A_{bulk}	Bulk charge parameter; $A_{bulk} \approx 1$ in short channel region
	E_{sat}	Saturation electrical field; set $E_{sat} \approx \infty$ so that $V_{ds}/E_{sat} * L_{eff} \ll 1$
Fitting parameter	μ_0	Mobility fitting parameter
	E_0	
	v	
	R_{sd}	Source/drain series resistance

is not uniform. This will cause a nonuniform distribution of the threshold voltage along the channel. This effect is the so-called bulk charge effect. A_{bulk} is very close to 1 if the channel length is short. Because the effective channel length (L_{eff}) plays a crucial role in the extraction of R_{sd}, it needs to be adequately determined first. L_{eff} can be calculated by ($L_{TEM} - 2L_{ov}$), as depicted in Fig. 2. L_{TEM} may be obtained from the in-line scanning electron microscopy measurement (with accuracy within ± 2 nm) at polypatterned stage and the etching-induced length bias (ΔL). L_{ov} represents the overlap distance between the source/drain and gate and can be extracted from *C-V* measurement.[9,10] Figure 3 shows the *C-V* curves of different L_{TEM} values in NMOS. C_{ge} and C_{ov} can be extracted at gate bias equal to 1.0 and −0.5 V, respectively.[9] The gate length dependency of extracted C_{gc} and C_{ov} is shown in Fig. 4. L_{ov} can be easily obtained from the intercept of C_{gc} and C_{ov}.[9,10]

Because the conventional R_{sd} extraction methods, which do not consider the gate length dependency of μ_{eff}, need to conduct the R_{sd} extraction using devices with gate length ranging from short to long channel, their extraction errors are significant. Therefore, in this work we carried out the R_{sd} extraction based on the nanoscale devices with L_{TEM} from 50 to 83 nm.

For these short-channel devices, the impact of R_{sd} on the drain current (I_d) in the linear region ($V_d = 20$ mV) can be modeled by Eq. 1

$$I_d = \mu_{eff} C_{ox} \frac{W}{L_{eff}} \frac{(V_g - V_{th} - V_d/2)V_d}{1 + R_{sd}\mu_{eff} C_{ox} \frac{W}{L_{eff}} (V_g - V_{th} - V_d/2)} \quad [1]$$

Note that Eq. 1 can be derived from the BSIM drain current model[7] under the assumption that the carrier velocity saturation and the bulk-charge effect are negligible. The effective mobility (μ_{eff}) in Eq. 1 can be modeled by[7]

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^{\nu}} \quad [2]$$

where μ_0, E_0, and ν are model fitting parameters. E_{eff} represents the average electric field experienced by the carriers in the inversion layer and is given by $(V_g + V_{th})/6T_{ox}$ for an NMOS transistor with n-type polysilicon gate.

Because the accuracy of Eq. 1 in fitting the experimental data strongly depends on R_{sd}, we propose to determine R_{sd} by the following objective function

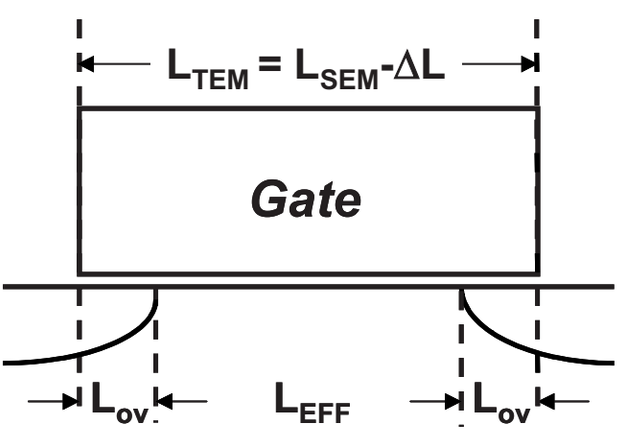

Figure 2. Schematic profile of MOSFET. L_{eff} can be obtained by ($L_{TEM} - 2L_{ov}$).

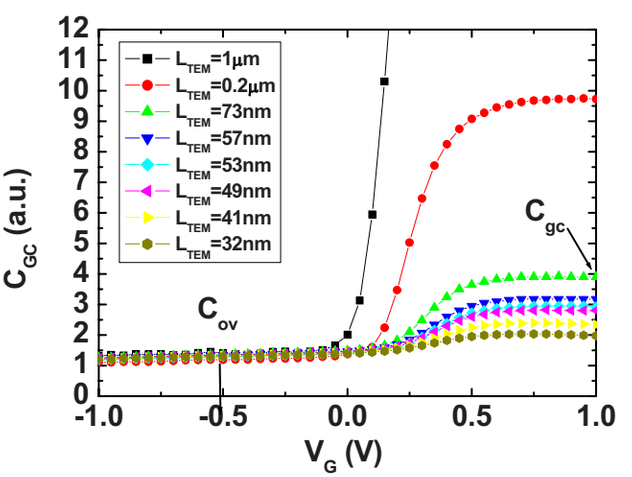

Figure 3. (Color online) The measured *C-V* curves in NMOS with various L_{TEM}. C_{gc} and C_{ov} are extracted at V_G equal to 1.0 and −0.5 V, respectively.

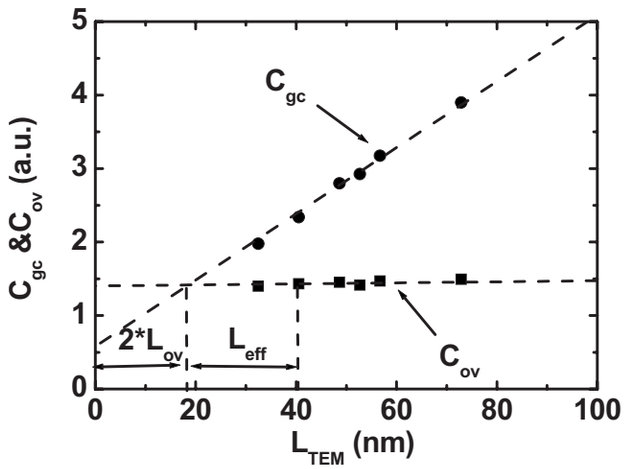

Figure 4. Plot of C_{gc} and C_{ov} vs various L_{TEM}. L_{ov} and L_{eff} can be obtained from the intercept points from C_{gc} and C_{ov}.

$$\delta_{min}(\mu_0', E_0', \upsilon', R_{sd}') = \sum_{L_{TEM}=50-83\ nm} \left\{ \left| \frac{[Id_{Si}(L_{TEM}) - Id_{model}(L_{TEM}, \mu_0', E_0', \upsilon', R_{sd}')]}{Id_{model}(L_{TEM}, \mu_0', E_0', \upsilon', R_{sd}')} \right| \right\} \quad [3]$$

where Id_{si} and Id_{model} represent the measured drain current and the calculated I_d by Eq. 1, respectively. μ_0', E_0', and υ' are the optimized model parameters that may result in a minimum model-hardware discrepancy (δ_{min}) for a given R_{sd}'. The correlation of δ_{min} and R_{sd}', shown in Fig. 5, indicates that δ_{min} is sensitive to the change in R_{sd}' and we may therefore determine the true R_{sd} value by finding the local minimum, i.e., $\partial\delta_{min}(R_{sd}')/\partial R_{sd}' = 0$. For our NMOS devices, the extracted R_{sd} value based on this method is $\sim$165 Ω μm, which follows the International Technology Roadmap for Semiconductors (ITRS) projection for this technology generation.[11] Note that if the R_{sd} value is not accurate, the drain current ratio of devices with different L_{TEM} values will not be correct, as shown in Fig. 6. Figure 7 provides the R_{sd} sensitivity with variations on different key parameters, where R_{sd} is the most sensitive to L_{eff}, but this can be overcome by careful in-line measurement. The variation in μ_{eff} has to be limited to within $\pm$5% if $\pm$4% R_{sd} variation is the maximum tolerance level. In this work, we carried out the R_{sd} extraction based on

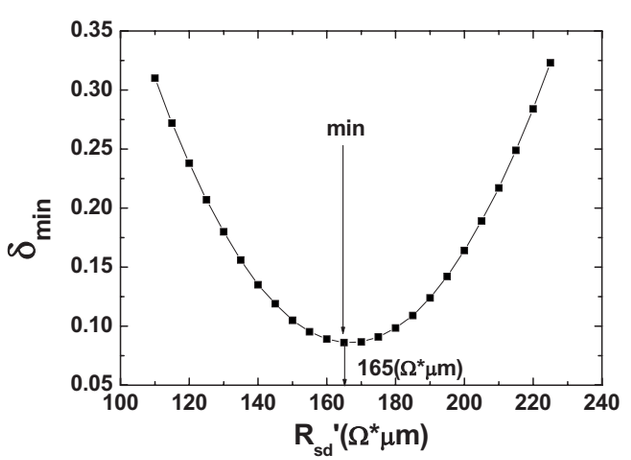

Figure 5. The objective function, δ_{min}, vs R_{sd}'. Optimized R_{sd} (165 Ω μm) can be obtained from the minimum of δ_{min}.

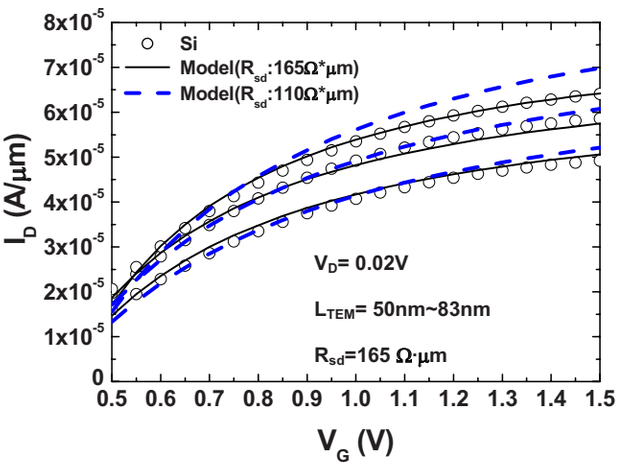

Figure 6. (Color online) I_d-V_g modeling results using various R_{sd} values. The three groups of curves correspond to different gate lengths ranging from 50 to 83 nm. If the R_{sd} value in the model is not accurate (e.g., R_{sd} = 110 Ω μm), the drain current ratio of devices with different L_{TEM} values will not be correct.

the devices with L_{TEM} from 50 to 83 nm, where the variation of μ_{eff} is within $\pm$5%.

To test our R_{sd} extraction methodology, NMOS and p-channel metal oxide semiconductor (PMOS) transistors with various extension conditions have been used. Figure 8 shows the relationship between R_{sd} and the measured overlap capacitance (C_{ov}) for these devices. It can be seen that when we increase the extension dose and hence, the overlap distance (L_{ov}), the extracted R_{sd} indeed decreases as C_{ov} increases. The R_{sd} values of PMOS are around two times those of NMOS.

We assume R_{sd} is independent of L_{TEM} due to the following observations: (*i*) In Fig. 8, R_{sd} is very sensitive to overlap capacitance (C_{ov}). However, Fig. 4 shows that C_{ov} is independent of L_{TEM}. (*ii*) Based on our Tsuprem4 simulation results incorporated with halo implants, L_{ov} (extension overlap distance under the poly) is independent of L_{TEM}, as shown in Fig. 9.

Once R_{sd} is accurately determined, the intrinsic μ_{eff} may be obtained using Eq. 1. Figure 10 shows the gate-length dependency of mobility [$\mu_{eff}(L_{TEM})$] in our NMOS devices with various stressors. Although the extracted R_{sd} values for both tensile and compressive

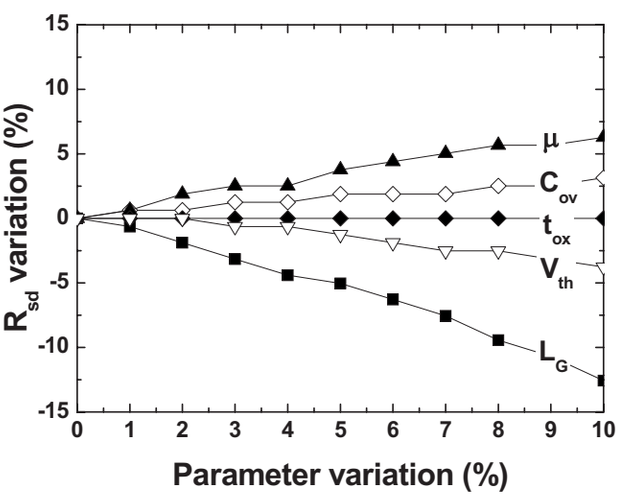

Figure 7. R_{sd} sensitivity plot with different key parameters.

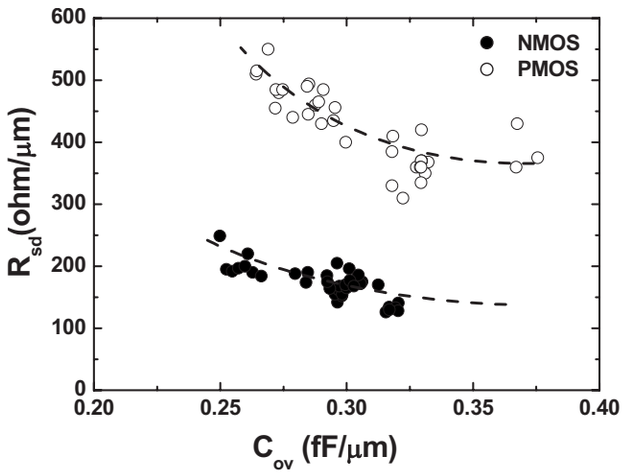

Figure 8. Relationship between R_{sd} and overlap capacitance (C_{ov}).

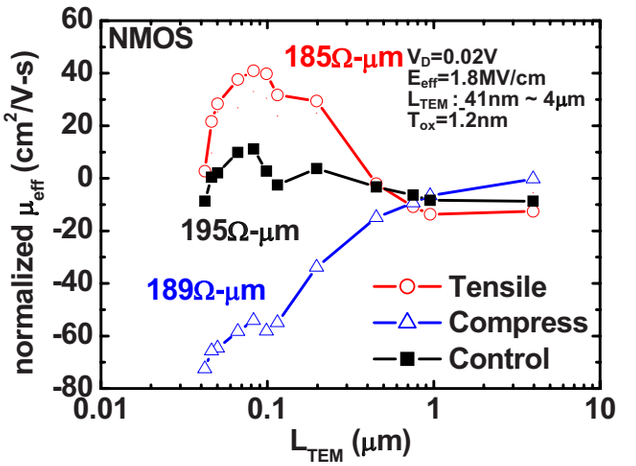

Figure 10. (Color online) $\mu_{eff}(L_{TEM})$ for NMOS devices with halo implants and various stressors (Tensile/0 stress/compressive). The mobility is subtracted by a positive constant for normalization purposes.

stressors are almost identical to the sample with zero stress (difference <10 Ω μm), the local tensile stressor enhances the mobility as L_{TEM} decreases, while the compressive stressor degrades the mobility. For devices with L_{TEM} shorter than 90 nm, however, the mobility shows significant degradation with L_{TEM} for all of the stressors. Several explanations regarding the mobility degradation behavior in the short-channel regime were proposed in the past, including halo implants and quasi-ballistic transport characteristics performed in these nanoscale devices.[2,12] This issue, nevertheless, deserves further study in the future. Using the extracted $\mu_{eff}(L_{TEM})$ in Eq. 1, good agreement with the silicon data over a wide range of L_{TEM} (41 nm to 4 μm) can be seen, as shown in Fig. 11.

Verification

To verify the proposed BSIM R_{sd} extraction method, we extract R_{sd} values from simulated I_d-V_g curves by a Medici simulator[13] and compare them with R_{sd} values obtained from the ohmic drop in the source region of the simulated device structures. The drain bias condition is set to 50 mV. Three values of specific resistivity (7×10^{-8}, 1×10^{-7}, and 1.3×10^{-7} Ω cm^2) are input to modify R_{sd} values and then the related I_d-V_g characteristics are generated for the BSIM fitting method.

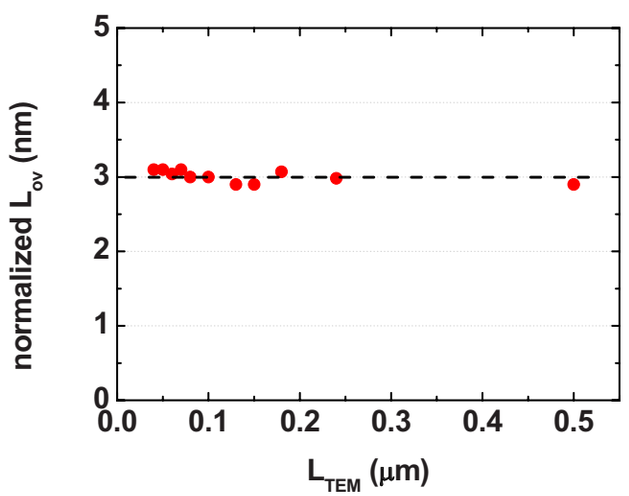

Figure 9. (Color online) L_{ov} (extension overlap distance under poly) vs L_{TEM} from Tsuprem4 structure simulation. L_{ov} is subtracted by a positive value for normalization purposes.

The inset of Fig. 12 shows simulated device structure with potential contour. The voltage drop in the source region is extracted directly from point A on the silicide region (V_A) and point B on the extension boundary (V_B). By using Ohm's law, R_{sd} can be easily obtained and R_{sd} offset (ΔR_{sd}) in different specific resistivity values can be extracted directly. ΔR_{sd} here is defined as $R_{sd}(\rho_c) - R_{sd}$ ($\rho_c = 1 \times 10^{-7}$ Ω cm^2). As shown in Fig. 12, ΔR_{sd} extracted from potential contour with different specific resistivity values shows the consistent trend with ΔR_{sd} extracted by the BSIM fitting method. It indicates that the proposed BSIM method can accurately quantify the difference of R_{sd} and be a suitable monitor tool for USJ and strained process development.

Conclusions

We have proposed a BSIM-based method for R_{sd} and μ_{eff} extraction which applies to nanoscale strained-silicon MOSFETs with halo implants. This R_{sd} extraction method may serve as a suitable process monitor tool for USJ and strained process development. This method is more accurate than the conventional channel-resistance and shift and ratio method because it considers the gate-length dependence of mobility caused by local uniaxial stress and laterally nonuniform channel doping. We have verified this method using

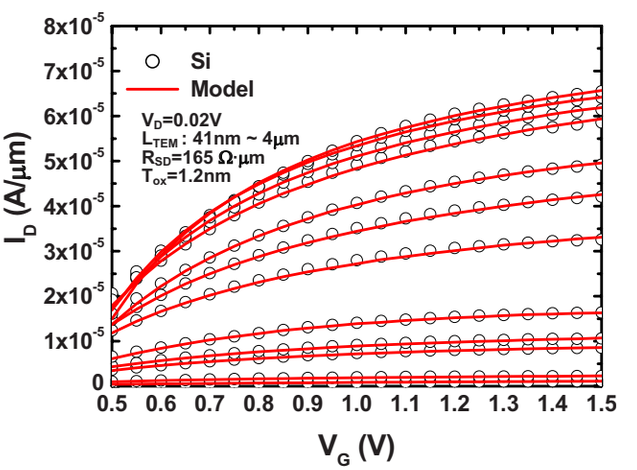

Figure 11. (Color online) I_d-V_g modeling results for a wide range of L_{TEM} using the extracted $\mu_{eff}(L_{TEM})$.

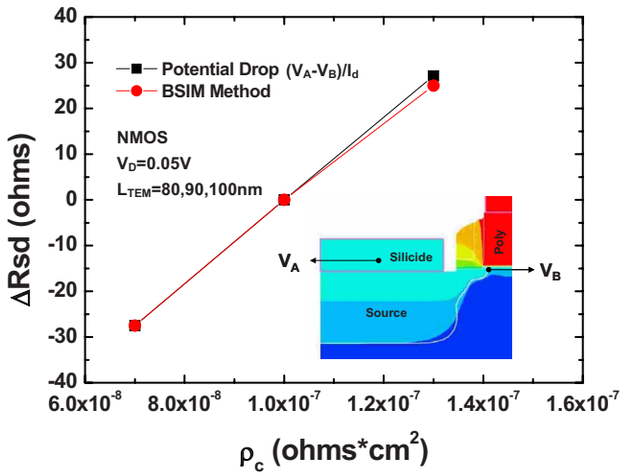

Figure 12. (Color online) A comparison plot of ΔR_{sd} vs ρ_c (specific resistivity) with two R_{sd} extraction methods, the BSIM fitting method and Medici potential contour method. ΔR_{sd} equals $R_{sd}(\rho_c)$-R_{sd} ($\rho_c = 1 \times 10^{-7}$ Ω cm^2). [Inset: potential contour of simulation MOSFET profile. R_{sd} is extracted by Ohm's law: $(V_A$-$V_B)/I_d$].

samples with different stressor/doping conditions and good agreement with experimental data has been obtained. Significant mobility degradation in the short channel regime was observed for various uniaxial stressors. The accuracy of BSIM R_{sd} extraction method is also proven by simulated current–voltage characteristics with different external resistant values in the short-channel regions. Therefore, this method may serve as a suitable process monitor tool for USJ and strained process development.

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