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The Annihilation of Threading Dislocations in the Germanium Epitaxially Grown within the Silicon Nanoscale Trenches

Guang-Li Luo,[a,z] Shih-Chiang Huang,[a] Chih-Hsin Ko,[b] Clement H. Wann,[b] Cheng-Ting Chung,[c] Zong-You Han,[c] Chao-Ching Cheng,[c] Chun-Yen Chang,[c] Hau-Yu Lin,[b] and Chao-Hsin Chien[a,c]

[a]*National Nano Device Laboratories, Hsinchu 300, Taiwan*
[b]*Taiwan Semiconductor Manufacturing Company, Limited, Hsinchu 300, Taiwan*
[c]*Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan*

We investigated the selective growth of germanium into nanoscale trenches on silicon substrates. These nanoscale trenches, the smallest size of which was 50 nm, were fabricated using the state-of-the-art shallow trench isolation technique. The quality of the Ge films was evaluated using transmission electron microscopy. The formation of threading dislocations (TDs) was effectively suppressed when using this deposition technique. For the Ge grown in nanoscale Si areas (e.g., several tens of nanometers), the TDs were probably readily removed during cyclic thermal annealing predominantly because their gliding distance to the SiO_2 sidewalls was very short. Therefore, nanoscale epitaxial growth technology can be used to deposit Ge films on lattice-mismatched Si substrates with a reduced defect density.
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Because of the higher mobility of its carriers and its narrower bandgap relative to that of silicon (Si),[1] germanium (Ge) is now emerging as a viable candidate to supplement Si in complementary metal oxide semiconductor (CMOS) devices and 1.3–1.55 μm optoelectronic applications;[2] therefore, it is essential to develop new methods for the heteroepitaxial growth of Ge on Si. This growth process is not straightforward, however, because the large lattice mismatch (4%) between Ge and Si limits the quality of the epitaxially grown layers. After reaching a critical thickness, the Ge layer usually contains many misfit dislocations (MDs) and threading dislocations (TDs), making it unusable for any practical applications. Although several techniques have been proposed to alleviate this problem,[3] the TD densities in the grown Ge layers remain too high for device applications. Using patterned growth and cyclic thermal annealing (CTA), the dislocation density in Ge can be reduced to ca. $10^6/cm^2$ as a result of thermally induced dislocation gliding.[4] Any further reduction remains a big challenge because the dislocations cannot glide over the long distances in large patterns. Based on the selective growth of Ge in narrow, deep SiO_2 trenches of several hundreds of nanometers, it was recently reported that the generated TDs in Ge could be effectively trapped to the sidewalls of SiO_2 through an aspect ratio trapping (ART) mechanism;[5] the resulting top area of Ge was claimed to be dislocation free. In Ref. 5, the authors considered that the TDs formed at a 45° angle to the underlying Si(001) surface. Thus, for trenches having an aspect ratio greater than unity, the TDs meet the SiO_2 sidewalls and terminate there when they penetrate up in the Ge film. In such a case, the surface of Ge would be dislocation free, with TDs being confined only to the bottom of the trenches.

In this study, following the similar process scheme, we selectively grew Ge layers in SiO_2 trenches having dimensions as low as 50 nm. After CTA, the formation of TDs in the Ge layers grown in these ultrasmall trenches was further suppressed. Our results are slightly different from those expected for the ART mechanism,[5] where there are still a few TDs at the bottom of the Ge layer. In our case, the dislocations at the bottom of the trenches were also suppressed, quite advantageous for the fabrication of Si-based Ge-channel devices, such as Ge fin field effect transistor (FinFET) devices. For our Ge films grown in ultrasmall SiO_2 trenches, the TD reduction was readily achieved because the TDs did not have to glide very long distances in the nanoscale patterns.

[z] E-mail: glluo@ndl.org.tw

Experimental

The state-of-the-art shallow trench isolation (STI) technique was used to fabricate the patterns on p-type (100)-oriented Si wafers having resistivities of 15–25 Ω cm. The Si area was recessed using reactive ion etching to form trenches for the selective epitaxial growth of Ge. The trenches were aligned along the [110] direction; they were formed with dimensions of 50 nm × 600 nm and 320 nm × 1.4 μm, respectively. The narrowest width of the trenches was 50 nm, a reasonable dimension for 22 nm technology nodes. The finished 50 nm trenches are displayed in Fig. 1. After trench fabrication, the Si substrates were subjected to standard wet cleaning and dipping in dilute HF for 30 s to remove the native oxide on the exposed Si surface; they were then loaded into an ultrahigh vacuum chemical vapor deposition chamber. After thermal prebaking at 900°C for 10 min, Ge layers having thicknesses of 150–200 nm were selectively grown inside the trenches at 400°C under a germane flow rate of 10 sccm and a growth pressure of 0.5 mTorr. Finally, the wafers were in situ annealed over three cycles; each cycle included high temperature annealing at 900°C for 5 min and low temperature annealing at 400°C for 5 min. Because the thermal expansion coefficients of Ge and Si are different, annealing can generate extra thermal stress that can cause movement of the TDs in the grown Ge layer. For CTA, an increase in the number of cycles results in a greater dislocation reduction.[4,6] In this study, considering the trade-off between the thermal stress effect and the experimental efficiency, a three-cycle annealing was adopted. Cross-sectional transmission electron microscopy (XTEM) and plan-view transmission electron microscopy (TEM) samples were prepared through mechanical polishing and perforation by Ar-ion milling. For the plan-view TEM samples, only the top 70 nm Ge layer remained

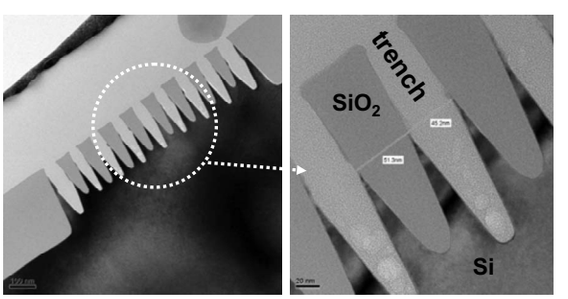

Figure 1. XTEM images of the 50 nm SiO_2 trenches fabricated using the STI process.

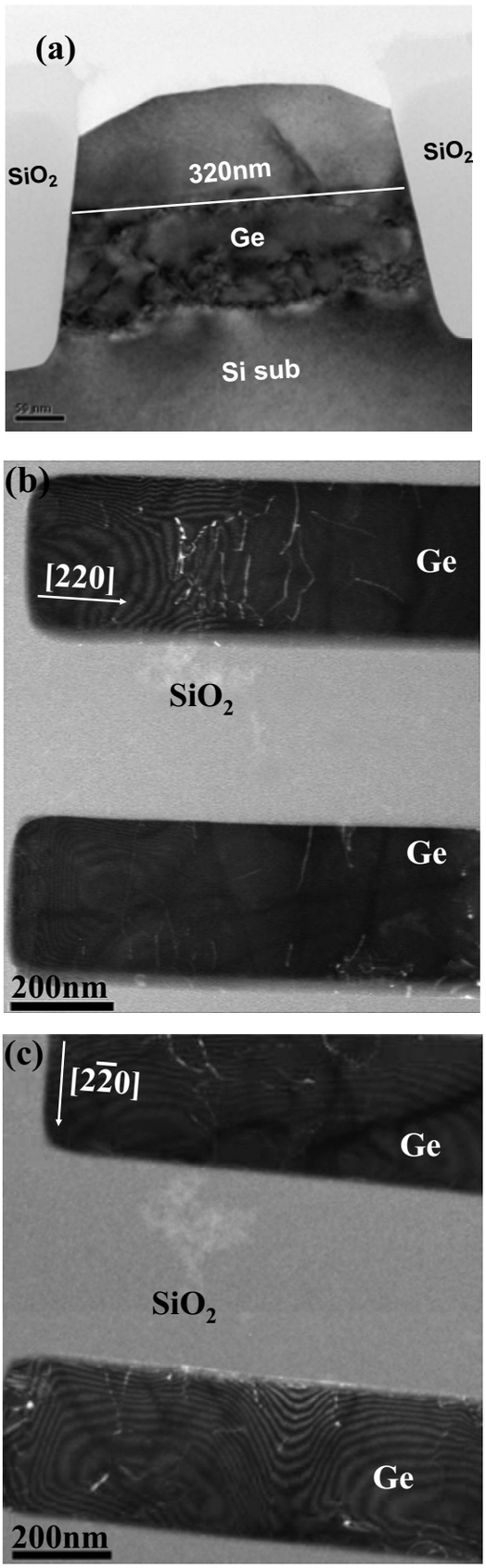

Figure 2. (a) XTEM image of Ge in trenches having a width of 320 nm, revealing unremoved dislocations. Plan-view TEM images of Ge in trenches having a width of 320 nm: (b) $\mathbf{g} = [220]$; (c) $\mathbf{g} = [2\bar{2}0]$.

after Ar-ion milling, making sure that the Ge/Si interface region was removed. TEM images were recorded using an FEI Tecnai F20 microscope operated at 200 kV.

Results and Discussion

TDs are associated with MDs at an interface; they are necessary to accommodate the lattice mismatch between Ge and Si. The MDs can terminate at the film surface via TDs. For diamond and zinc-blende semiconductors, there are generally two types of MDs at the interface: 60° dislocations, which are glissile and have a Burgers vector **b** out of the interface plane, and 90° dislocations, which are sessile and have **b** lying in the interface plane. The 60° MDs can change their length during plastic relaxation through the gliding of their threading segment. The 90° MDs are very effective in relieving a lattice mismatch, but their threading segments can hardly glide.[7,8] For face-centered cubic semiconductors, gliding on the close-packed {111} glide planes of a 60° dislocation is preferable to that on the {100} glide planes of a 90° dislocation; therefore, a direct formation of 90° dislocations is difficult.[7] This type of dislocation can be formed, however, through the reaction of two 60° dislocations.[9,10] For example, if two 60° dislocations had Burgers vectors such that a strong attraction existed between the two threading segments ($\mathbf{b}_1$ and $\mathbf{b}_2$), an attractive interaction would generate a TD having a Burgers vector $\mathbf{b}_3$, namely, a 90° dislocation. In terms of Burgers vectors, a typical reaction may be written as

$$(a/2)[01\bar{1}] + (a/2)[101] = (a/2)[110]$$

Figure 2a displays an XTEM image of the Ge film in a trench having a width of 320 nm; it reveals that the TDs could not be removed completely through CTA. Figure 2b and c presents two-beam dark-field plan-view TEM images that were recorded on the same area of the sample by using $\mathbf{g} = [220]$ and $[2\bar{2}0]$ reflections, respectively; TDs also appear in these two images. The dislocations that display a clear contrast in Fig. 2b are invisible in Fig. 2c, and vice versa. The Burgers vector of these dislocations can be easily identified by the invisibility criterion because dislocations lose contrast if **g** is perpendicular to the Burgers vector (i.e., $\mathbf{g} \cdot \mathbf{b} = 0$).[11] Based on this criterion, the dislocations in Fig. 2b and c are all 90°. The 90° dislocations in Fig. 2b must have a Burgers vector of $a/2[110]$ because they are invisible in Fig. 2c; in contrast, the 90° dislocations in Fig. 2c must have a Burgers vector of $a/2[1\bar{1}0]$ because they are invisible in Fig. 2b. We observe no 60° dislocations in these two figures; therefore, they must have been removed during CTA through the glide and annihilation mechanisms.[12] The Ge/Si interface was somewhat undulated. The high temperature CTA process was the likely cause of this roughness because high temperature annealing can result in severe interdiffusion of Ge and Si. The high gliding ability of the 60° dislocations in the grown Ge layer can be understood in terms of their velocity. We estimated the maximum in-plane thermal stress caused by CTA treatment in our case to be on the order of 10^9 dyn/cm^2. The glide velocity of the 60° dislocations is on the order of 10^{-3} cm/s, according to the data in Kabler's early report.[13]

Figure 3 presents XTEM and plan-view TEM images of Ge grown in 50 nm trenches. In Fig. 3a to c , no TDs are evident in Ge, even at its bottom; only MDs appear at the interface of Ge/Si (see Fig. 3b and d). From these results, we conclude that the TDs glided out the Ge during CTA, and only MDs remained along the Ge/Si interface. A comparison of Fig. 1 and 3 reveals that the Si along the SiO_2 sidewalls at the bottom areas of trenches disappeared after the Ge growth presumably because intense interdiffusion occurred between Si and Ge during the CTA process. That is, Si on both sides of each trench completely diffused into the Ge film during annealing. For comparison, we observed TDs when the Ge layers grown inside the 50 nm trenches were not subjected to CTA (see Fig. 4), confirming that CTA was essential for the removal of TDs.

According to Speck et al.[10] and Romanov et al.,[14] the TD densities can be reduced either through the annihilation of threading seg-

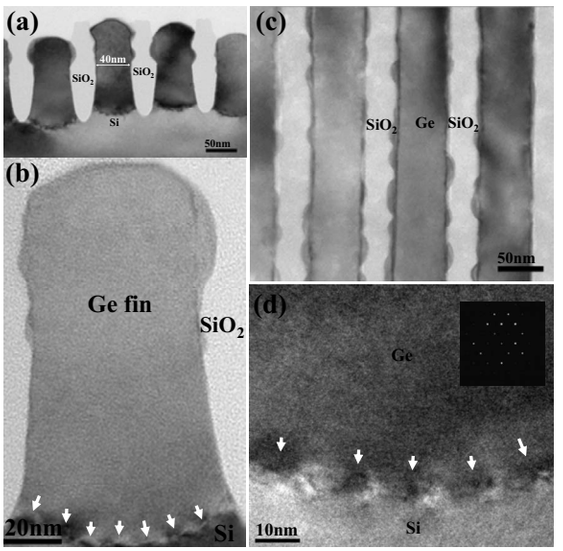

Figure 3. (a) XTEM image of Ge in trenches having a width of 50 nm. (b) Magnified XTEM image. (c) Plan-view TEM image. (d) Magnified XTEM image. The MDs at the Ge/Si interface are indicated by arrows.

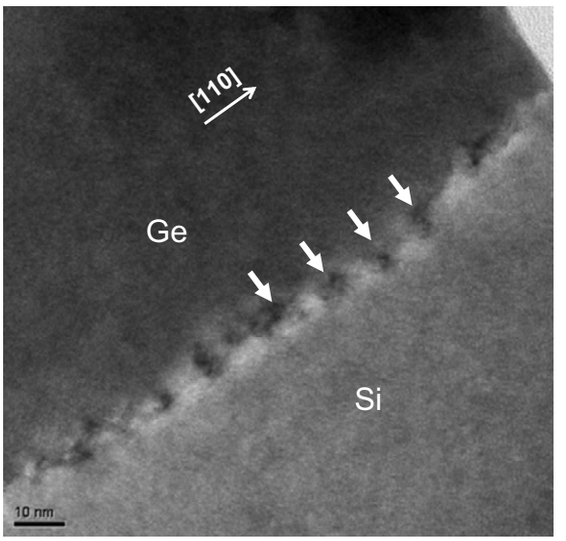

Figure 5. XTEM image of Ge in 50 nm trenches, recorded along the direction of the length of the trenches. MDs are clearly evident at the Ge/Si interface (some are indicated by arrows).

ments having antiparallel Burgers vectors or through reactions in which two TDs combine to form one TD. There are four possible annihilation processes for TDs in a dislocated epitaxial film: (*i*) Loops can self-annihilate through gliding; (*ii*) threading segments from different sources on the same slip lane can annihilate or combine to form another one through gliding; (*iii*) threading segments from different sources on the parallel slip systems can annihilate or combine to form another one; (*iv*) threading segments from different sources on intersecting slip systems can annihilate or combine to form another one through gliding, climbing, or a combination of the two. Because Ge and Si have a 4% lattice mismatch, the original TD density should be the same for any pattern size. Here, the major factor determining the TD density should be the propagation distance. In the nanoscale patterns, many of the dislocations could readily glide to the sidewalls of the trenches with a low probability of being blocked or combined to form a sessile dislocation because of the very small propagation length; in contrast, dislocations in larger patterns had greater difficulty arriving at the sidewalls, and, therefore, they tended to become trapped in the Ge film. Although the trench was aligned along the [110] direction and had a length of 600 nm, the TD density still remained low. Because the TDs in the $(\bar{1}\bar{1}1)$ and (111) slip planes along the width direction of the trench (i.e., [110] direction) have glided to the SiO_2 sidewalls, the interactions between TDs from different sources on intersecting slip systems [e.g., between $(\bar{1}\bar{1}1)$ and $(1\bar{1}1)$ slip planes] are suppressed. This case facilitates the annihilation of TDs on the same slip plane or on the parallel slip systems [e.g., the (*ii*) and (*iii*) annihilation processes of TDs described above] to work better along the direction of the length of the trench. As a result, the TD density in 50 nm trenches can still be reduced, albeit the length of the trenches is long.

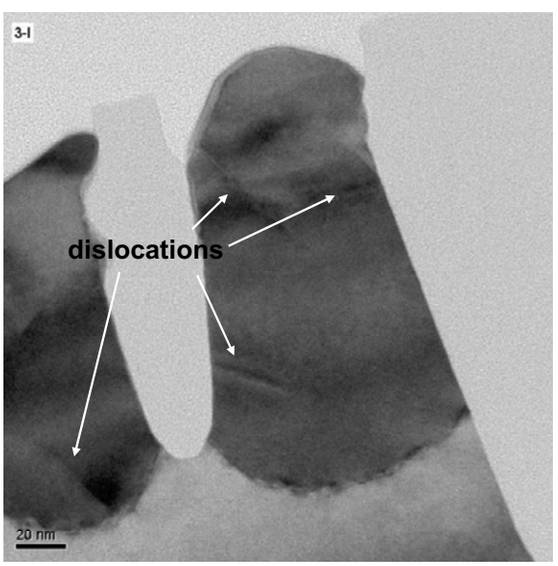

Figure 4. XTEM image of Ge in 50 nm trenches without CTA.

Recent publications[15] suggest that for SiGe films grown selectively on recessed Si, a decrease in the trench width causes the strain of the SiGe film to be released preferably through elastic relaxation in the direction of the width of the trench. However, the strain in our Ge film was released mainly through plastic relaxation in the directions of both the width and the length. In Fig. 3b and d, uniformly distributed MDs appear at the Ge/Si interface. For comparison, we also present a magnified XTEM image of the 50 nm sample along the direction of the length of the trenches. Similarly, the MDs are clearly observable at the Ge–Si interface in Fig. 5. The distances between the MDs in Fig. 3b and d are almost the same as that in Fig. 5, indicating that the strain in Ge was relaxed biaxially and plastically. This result differs from that reported by Ref. 15 most likely because we applied a high temperature CTA process to the Ge layer, causing the Ge layer to relax adequately.

Conclusions

We have performed the heteroepitaxial growth of Ge into nanoscale trenches on Si substrates. Through mechanisms involving gliding and annihilation, the TDs in nanoscale Ge were readily removed through CTA. The strain in the Ge films grown using this technique was released mainly through plastic relaxation in the directions of both the width and the length of the trenches. This heterostructural Ge on Si probably has potential applications in the integration of Ge-channel devices onto Si CMOS platforms.

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