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The Characteristics and Control of Body-to-Body Leakage Current in PD-SOI

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Body-to-body leakage (BBL) current in a partially depleted silicon-on-insulator (PD-SOI) device is increased significantly as polyspacing (PS) is reduced in technology scaling. We found out that the BBL has a great impact to Vt variation. We have demonstrated that the BBL can be minimized drastically by implant optimization. The dependence of the BBL on silicon film thickness, e-SiGe structure, and dopant diffusivity is also discussed in this paper. The layout effect of the BBL current in PD-SOI devices has been characterized with different PSs, device widths, and polylengths. Finally, we have demonstrated that the BBL current can be reduced below junction leakage level.
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Silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) has been widely used recently due to its better device performance and scalability. Partially depleted silicon-on-insulator (PD-SOI) has a similar device structure to a bulk device. As a consequence, the PD-SOI can be fabricated in a standard bulk CMOS process. SOI devices have better circuit performance and lower power consumption due to lower channel doping and smaller parasitic capacitances. However, PD-SOI devices possess several unique behaviors that do not exist in bulk devices such as kink effect,[1-3] self-heating effect,[4-6] history delay effect,[7,8] and pass-gate leakage.[9,10] Those effects have been actively studied and modeled. For the two stack PD-SOI devices sharing a common diffusion area, the bodies of the two devices are isolated by a common source/drain (S/D) junction. If the common S/D junction does not abut the buried oxide (BOX), a leakage path is formed between the two bodies. The body-to-body leakage (BBL) induces body potential change and Vt shift, as reported in Refs. 11 and 12. Besides, ac performance is degraded because of the increase in the S/D junction capacitance. In an advanced SOI technology, aggressive scaling of the junction depth leads to a significant increase in the BBL current. The BBL can have the following adverse effects on circuit operation: (*i*) Higher junction capacitance due to the larger junction area, (*ii*) Vt shift due to the change in body potential, and (*iii*) failure of circuit function if device Vt is significantly changed. As a result, the BBL effect must be taken into consideration when optimizing the S/D junction profile in PD-SOI devices.

The accuracy of device modeling becomes increasingly important in modern circuit design. Although several attempts have been made on the modeling and simulation of the BBL, very few experimental results have been reported. The BBL effect also depends on the device geometries such as polygate spacing. The geometry effect must also be taken into consideration when optimizing the S/D junction profile.

This paper presents the experimental and simulation results of the BBL effect and its dependences on back-gate bias, polygate spacing, device width, silicon layer thickness, and S/D implant conditions. The impact of the Vb shift to circuit function caused by the BBL in stack PD-SOI devices has been simulated by using a simulation program with integrated circuit emphasis (SPICE) circuit simulator. Finally, experimental results are presented to demonstrate that the BBL current can be reduced to below junction leakage current by process optimization and device geometry techniques.

Device Fabrication and Measurement

The PD-SOI metal-oxide-semiconductor field-effect transistors (MOSFETs) used in this study were fabricated in a 45 nm SOI process. This process utilizes several advanced strained techniques to boost device performance like its counterpart bulk process, including embedded SiGe (e-SiGe),[13,14] dual contact-etch-stop-layer,[15,16] and stress memorization technique.[17-20] The structure used to characterize the BBL effect is composed of two stack body-tie devices sharing a common well. The measurement setup is shown in Fig. 1. Body bias (Vb2) is applied to the body region b2. The BBL current is the body current of device no. 1, in which the S/D-to-body junction bias is zero to exclude the S/D junction diode leakage. The polyspacing (PS) and SOI thickness are 140 nm and 550 A, respectively. The bodies of two devices are isolated by the common S/D junction. If the common S/D junction does not abut the BOX, a leakage path is formed between the bodies of the two devices. The BBL is characterized by measuring the leakage current between the bodies of the two stack devices. The BBL is also a function of back-gate bias, as shown in Fig. 2. When a positive Vbg is applied to the back gate, the BBL current is smaller because the depletion layer width of the S/D junction is wider. When a negative

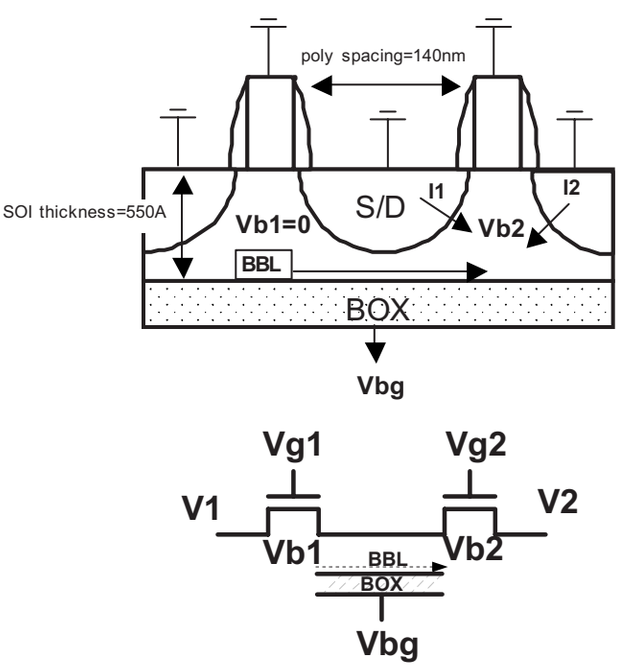

Figure 1. Structure used to characterize the BBL is composed of two stack devices sharing a common well.

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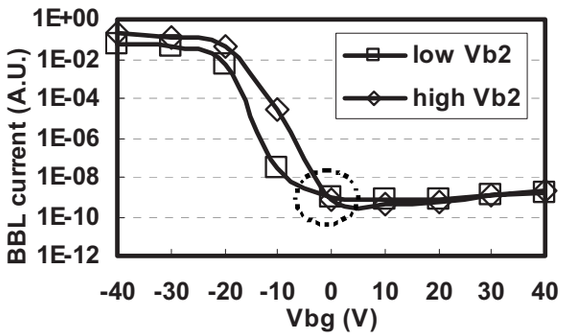


Figure 2. The BBL is a function of back-gate bias. When a positive Vbg is applied, the BBL is smaller because the depletion layer width of the S/D junction is wider. When a negative Vbg is applied, the BBL becomes larger and the isolation between the two stack devices becomes worse because the junction depth is reduced.

Vbg is applied, the BBL current becomes larger and the isolation between the two stack devices becomes worse because the junction depth is reduced. The BBL current becomes insensitive to Vbg when the S/D junction abuts the BOX. The BBL effect has been characterized in different body bias conditions (Vb2). The BBL increases with increasing Vb in negative Vbg because the junction depth is reduced if Vb is increased.

Results and Discussion

BBL simulation.— The BBL can cause body potential change, device Vt shift, and circuit functional failure. The impact of the BBL on device characteristics can be studied by using the SPICE simulation. A two-step SPICE simulation is used to evaluate the Vt shift caused by the BBL current. The first step is to obtain the Vt change caused by the Vb variation. The second step is to obtain the Vb change caused by the BBL current. Figure 3 shows SPICE simulation results of Idsat and Vtsat characteristics as functions of Vb. For nMOSFETs, when Vb is decreased by 50 mV due to BBL, Vtsat is increased by 13 mV and Idsat is decreased by 2.25%, as shown in Fig. 3. The BBL induces Vb change that could cause variations in Vt and Idsat. From the results, it is important to minimize the BBL current in PD-SOI devices to below the S/D junction leakage current; otherwise, Vt and Idsat of stack devices might become unpredictable during circuit operation.

In a PD-SOI technology, each device is isolated from its neighboring devices by BOX and shallow trench isolation. Only stack devices can be affected by the BBL. Figure 4 illustrates the schematic circuit diagram of the two stack devices used for the BBL characterization. The BBL current is denoted as Ib2. If the BBL does not exist, the body potentials, Vb1 and Vb2, are 0.432 and 0.055 V, respectively. If the BBL exists between the two stack devices, the BBL current can affect the body potentials (Vb1 and Vb2) and Vt1, as shown in Fig. 5. As Ib2 increases, the changes in Vb and Vt become more noticeable. Vb2 is less sensitive to the BBL compared to Vb1 because of its higher forward junction leakage compared to the BBL. The impact of Vb2 is not significant until the BBL current is high enough to about forward junction level. To prevent circuit failure caused by the Vb shift, the BBL current must be minimized.

Dependence of BBL on layout effect.— To fully characterize the BBL behavior in PD-SOI devices, the layout effect must be taken into consideration. The BBL has been measured on a set of test structures with variations in the PS, device width, and device length.

The BBL current increases exponentially as the PS is decreased, as shown in Fig. 6a. The BBL current is basically independent of polywidth and length, as shown in Fig. 6b and c. The S/D junction becomes shallower for a smaller PS device due to the shadowing effect of implants. When the technology migrates from 45 nm (PS is 140 nm) to 32 nm (PS is 100 nm), the PS and the S/D junction depth

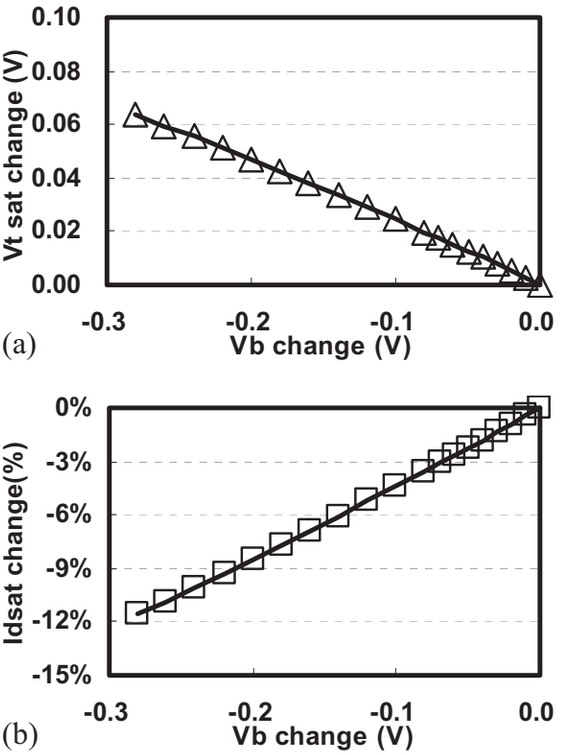


Figure 3. (a) SPICE simulation results for nMOSFET. When Vb is decreased, Vtsat is increased. (b) When Vb is decreased, Idsat is decreased.

are scaled down proportionally with the gate length. The BBL current shows a drastic increase of more than 1000 times when the polyspace is decreased from 180 to 108 nm. The BBL issue becomes one of the scaling limitations for PD-SOI devices.

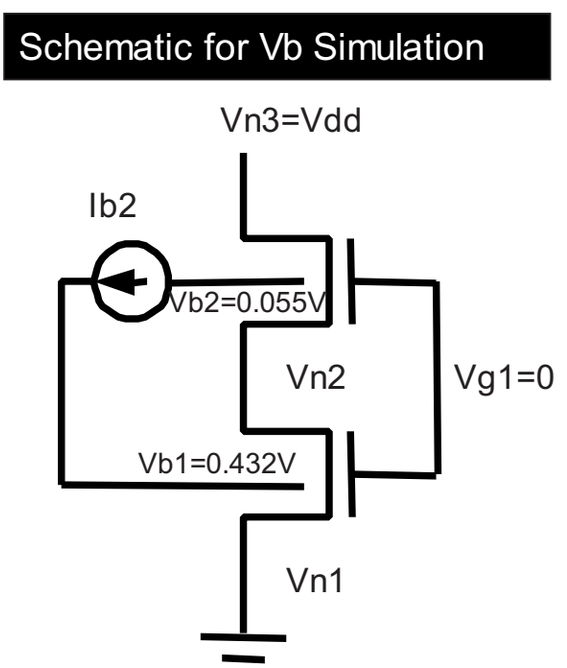


Figure 4. Schematic circuit diagram of the two stack devices. The BBL current is denoted as Ib2. The body potentials, Vb1 and Vb2, are 0.432 and 0.055 V, respectively, when the BBL does not exist.

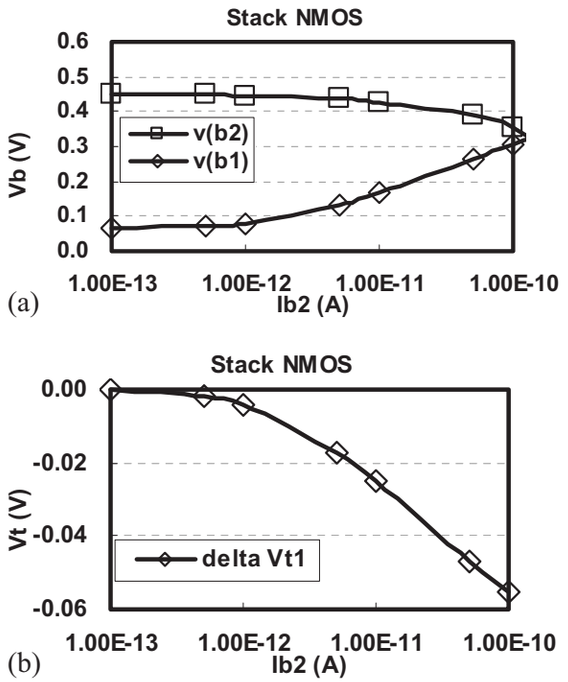


Figure 5. (a) When the BBL exists between two stack devices, Vb1 and Vb2 are changed. As Ib2 increases, the Vb change becomes more noticeable. (b) Ib2 leads to device Vt change.

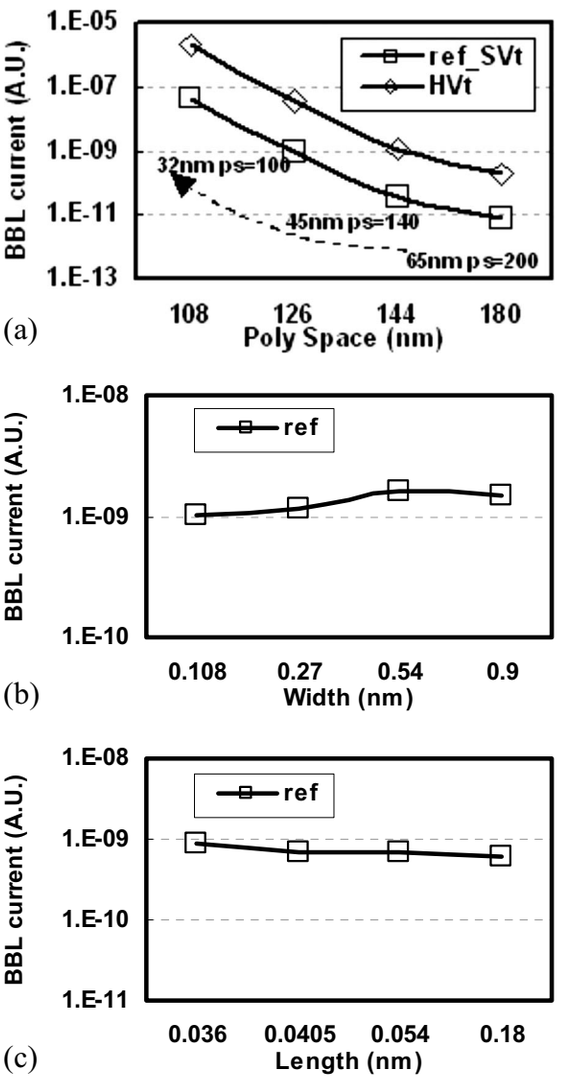


Figure 6. (a) The BBL increases exponentially as the PS decreases. When the technology migrates from 45 to 32 nm, the BBL current shows a drastic increase of more than 1000 times. The BBL current of the HVt device is about 25 times higher than that of SVt devices. (b) The BBL is not a function of device width. (c) The BBL is not a function of device length.

For our technology having multiple Vt devices, the BBL current of high threshold voltage (HVt) devices is about 25 times higher than that of standard threshold voltage (SVt) devices. The higher well doping in HVt devices creates a leakage path under the S/D junction; therefore the BBL current is higher.

BBL minimization.— Figure 7 shows the optimization flow to reduce the BBL current. Physical dimensions of a device are generally reduced to 70% from 65 to 45 nm node by following the scaling rules. When scaling down PD-SOI devices, the BBL becomes a serious concern because we scale up well doping and scale down the PS (from 200 to 140 nm), but the SOI layer thickness is barely changed to maximize mobility enhancement from the e-SiGe stressor. We have demonstrated that the BBL current could be minimized through implant optimization. If the S/D junction abuts the BOX, the BBL current can be greatly reduced. Figure 8 shows that the BBL current can be reduced by optimizing the implant conditions of the S/D, halo, and well implants. Design A shows that the BBL current can be reduced by increasing the S/D junction depth. Design B shows that the BBL current can be reduced by reducing the halo implant energy. The BBL current can be further reduced in Design C by optimization of the halo, well, and S/D implants. By implant optimization, the minimum allowable PS can be reduced from 540 to 108 nm.

The BBL effect is highly dependent on the SOI thickness, as shown in Fig. 9. Wafers were fabricated using three different SOI thicknesses (Reference, 70 Å less, and 140 Å less). The thinner SOI layer allows shallower S/D junctions to abut the BOX and has a weaker dependence on the PS.

The dopant diffusivity also plays an important role in the BBL effect. In an advanced technology, shallow junctions are typically formed with dopant with low diffusivity. However, the BBL issue becomes more severe for a shallower junction. For pMOSFETs, the BBL effect shows less dependence on the PS because boron has a higher diffusivity than phosphorus. S/D junctions of pFETs formed by boron implant are easier to abut the BOX than the S/D junctions of nFETs formed by phosphorus implant, as shown in Fig. 10. In an advanced technology with e-SiGe S/D stressors, pMOSFETs commonly have raised the S/D to increase the SiGe volume to boost the device performance and reduce the S/D series resistance. The raised S/D produces shallower junctions even using the same implant energy. Figure 11 illustrates PS dependence of the BBL current using raised S/D e-SiGe. After optimizing the e-SiGe profile and implant condition, the dependence of the BBL current on the PS can be further reduced. From the experimental results, we have demonstrated that PS dependence of the BBL current at 45 nm node can be reduced by implant optimization, e-SiGe profile improvement, and SOI thickness reduction.

Conclusions

The BBL becomes significant and affects the overall circuit performance in PD-SOI as the polypitch is scaled continuously to 32 nm and beyond technology. A methodology for BBL extraction has been demonstrated in this paper. The impact of BBL can be minimized by optimizing well, halo, and S/D implantation. The Si thick-

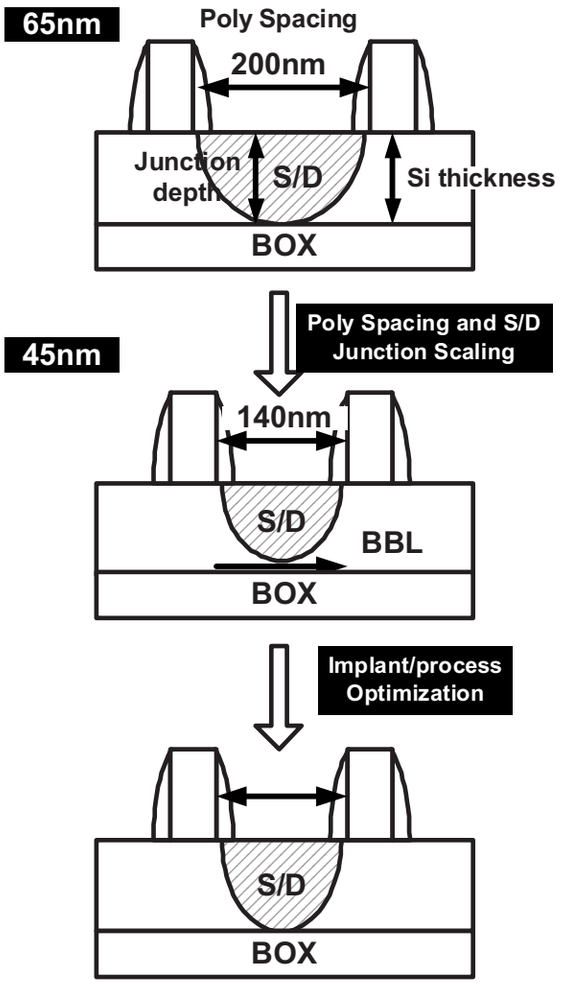
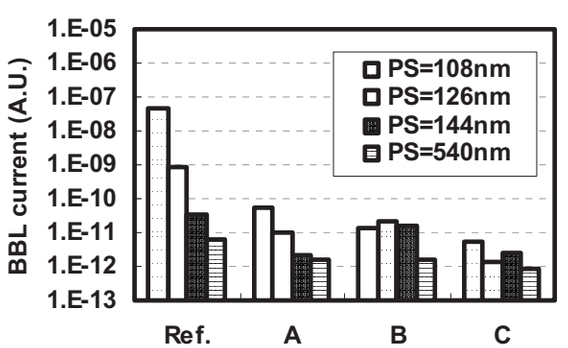


Figure 7. When scaling PD-SOI devices from 65 to 45 nm technology, the BBL becomes a concern because we scale up well doping and scale down the PS, but the SOI layer thickness is barely changed to maximize mobility enhancement from the e-SiGe stressor. The BBL could be minimized through implant optimization to make the S/D junction abut the BOX.



Design	Ref.	A	B	C
Well	-	-	-	Lower dose
Halo	-	-	Shallower	Shallower
S/D	-	Deeper	-	-

Figure 8. The BBL is reduced by optimizing the implant conditions of the S/D, halo, and well implants. After implant optimization, the minimum allowable PS is reduced from 540 to 108 nm.

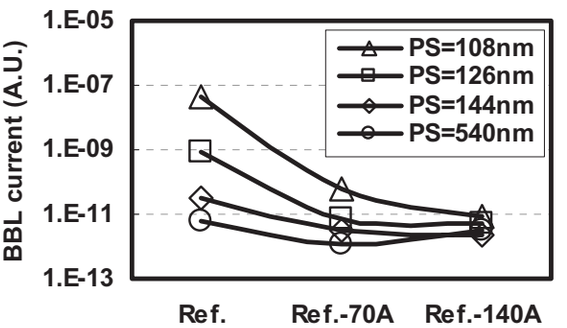


Figure 9. The BBL is dependent on the SOI thickness. The thinner SOI layer allows shallower S/D junctions to abut the BOX and decouple the BBL PS dependence.

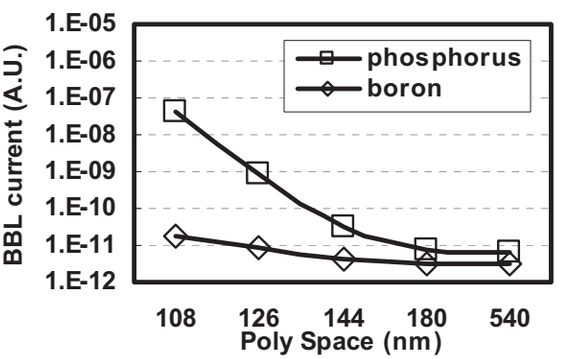


Figure 10. The dopant diffusivity plays an important role in the BBL. For the pMOSFETs, the BBL shows less dependence in the PS because boron has higher diffusivity than phosphorus and is easier to abut the BOX.

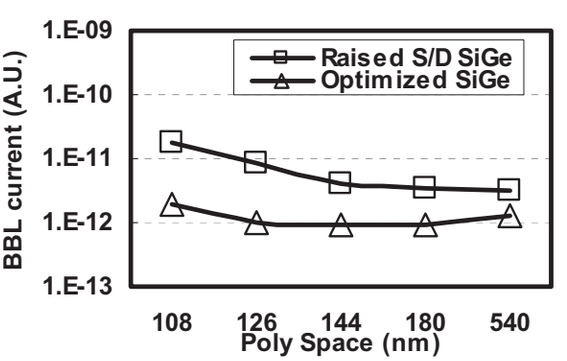


Figure 11. The PS dependence of the BBL is significant using the raised S/D e-SiGe. After optimizing the e-SiGe profile and implant condition, the dependence of BBL on PS is minimized.

ness of the SOI should be reduced after shrinking the S/D junction depth in future technology. Additionally, higher BBL is also observed if a raised S/D structure is employed.

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