Chapter 2

Literature Review

2-1 Overview of electronic packaging

The IC revolutionized the life of humans in the 20th century since the first integrated circuit (IC) was invented by Jack Kilby and Robert Noyce in 1958. With unremitting demand for better performance, the electronics industry has been forcing on smaller device. As the circuit density increases on the chip, the speed and functions it performs increases; however, a chip is not an isolated system, it must communicate with the other IC chips in a device from side to side in input/output (I/O) system of interconnects. Furthermore, the IC chips and its embedded circuitry are delicate, requiring a package both to carry and protect it. The integrated circuit chip alone is functionless if we don't have electronic packaging.

A characteristic microelectronic package is designed to provide the following functions:

(1) Connections for signal lines leading onto and off the silicon chip.

(2) Connections for providing electrical current that powers the circuits on the chip.

(3) A means of removing the heat generated by the circuit.

(4) A structure to support and protect the chip.

(5) A wiring structure for signal and power interconnections within a system and for input/output [4].

Fig.2.1 illustrates microelectronic package conventional hierarchy [2]; the layers of packaging are described as follows,

Level 0: chip level connections, i.e., gate to gate interconnections on the chip.

Level 1: chip-to-module connections, i.e., single-chip module or multi-chip module.

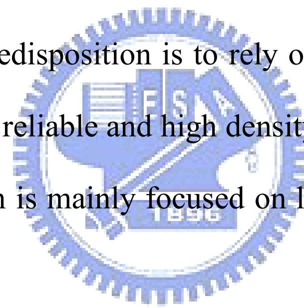
Level 2: module-to-board connections.

Level 3: board-to-board connections, i.e., board to motherboard.

Level 4: connections between sub-assemblies.

Level 5: connections between systems, i.e., computer to printer.

Over the past ten year, academia and industry have paid enormous attention to level 0, which resulted in a rapid increase of interconnections; the same degree of attention has not been paid to level 1, 2, and 3. The rapid growth of the IC density inside the Si chip has posted increasing challenge towards electronic packaging. The vital point to maintain this predisposition is to rely on the development of electronic packaging to provide durable, reliable and high density input/output system in the first level packaging. This research is mainly focused on level 1, which is of most current importance.



2-2 Chip level connections

The objective of chip level connections (1st level packaging) is to provide the requirement of chip-to-module connections. The methods of achieving first level packaging are (a) wire bonding, (b) tape automated bonding (TAB), and (c) flip chip bonding.

Wire bonding is used to attach a fine wire, from one connection pad to another, completing the electrical connection in an electronic device. The pads can be bond sites on the semiconductor chip or metallization bond sites on interconnection substrates. Semiconductor die can also be wire bonded to metal lead frames as is done in plastic encapsulated devices. The methods presently used to wire bond include

thermo compression, ultrasonic and thermo sonic. Figure 2-2(a) shows the scanning electron microscopy (SEM) micrograph of a wire bonding, and figure 2-2(b) is a side view, showing that only the edge is used for bonding purpose. With 20μm wire bonding, only 1000 input/output can be provided on a 1cm^2 chip. Although two rows of alternating bonding pads are used along the perimeter in the higher number of input/output chip, the total number of input/output provided by wire bonding is still limited.

Tape automated bonding (TAB) is a technique where the chip is attached to a polyimide tape prepared with copper conductors. This attachment also called the inner lead bond. The copper wires are connected to the presumed chips by thermo compression bonding; in the assembly plant, the tape is cut in such way that the outer part of the conductors (leads) is exposed. The chip/film assembly is then aligned and soldered or glued to the substrate using conductive adhesive. Figure 2-3 (a) shows the scanning electron microscopy (SEM) micrograph of a TAB inner lead bonding. A single inner lead with bump is shown in Figure 2-3 (b). The principle limitation of TAB is that TAB tapes have to be custom-matched to a particular chip. Today, TAB is only used in a very small portion of the interconnections [3].

Excluding the above two packaging technologies, flip chip packaging utilizes area array technology instead of employing only the peripheral region. If the bump diameter and pitch are reduced to 50μm, the input/output number on a 1 cm^2 chip area can reach to 10000 bumps. As mentioned above, wire bonding uses only ambient area of a Si chip; it cannot satisfy the requirement of a higher number of I/O in the near future. To meet the future requirement for the next 10 years [4], flip chip technology can satisfy the requirement of high density input/output. The solder bump flip chip was introduced by IBM in the early 1960s for their solid logic technology (SLT), which became the logical foundation of the IBM system/360 computer line.

The so-called C4 (controlled-collapse chip connection) technology utilized solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate [5]. Metal were usually Ni or Cu. The solder bump flip chip was aligned to the substrate, and all solder joints were made mean time by reflowing the solder.

A two level flip chip packaging is utilized in the mainframe computers. The chip side is bonded to ceramic module by high Pb solder (Sn5Pb95) with melting temperature of 320℃. Afterwards, the ceramic module is bonded to polymer printed circuit board (PCB) by eutectic SnPb solder and 90Pb10Sn solder ball. The schematic diagrams of two level flip chip packaging and its solder bump used for flip-chip bonding with the interface structure at both the Si side and substrate side are shown in Figures 2-4 (a) and (b).

In large-volume and low-cost consumer electronics, chips are bonded directly to polymer board, with ceramic module removed to reduce cost. In this process, high Pb solder no longer be used since polymers have low glass transition temperature(Tg) and can not sustain the high melting temperature of high Pb solder. Therefore, the high Pb solder was replaced by the eutectic SnPb solder. Nevertheless, eutectic SnPb has wetting problem with Au/Cu/Cr UBM, hence a low melting point eutectic solder to join the high Pb solder which called “composite solder” was applied to utilize in joining material. Figure 2-5 shows the schematic diagram of the composite solder joint. The thin eutectic solder can be deposited on the organic substrate before joining. Also it can be coated on the high-Pb. The key advantage is that the reflow temperature is low and it only needs to melt the low melting point solder [8].

2-3 Under Bump Metallization (UBM)

The ball-limiting metallurgy (BLM) or under bump metallization (UBM) usually

consists of three layers: (1) an adhesion layer such as Cr or Ti, capable of forming a strong bond with the passivation and with the terminating aluminum pad; (2) a solder wetting layer, such as Ni or Cu, which must remain at least partially intact through all the high temperature cycles-wafer reflow, card joining and possible reworks; and (3) a protective layer, Au or other noble metal, to retain wet ability for the wetting layer when vacuum is broken. As we know Ni reaction with Sn not faster than Cu.

The most popular UBM is phased-in Cu-Cr/Cu/Au used in IBM, Al/Ni(V)/Cu in Delco, Flip Chip Technologies, Amkor, Intel and AMD (Advanced Micro Devices), electrolytic Cu in Unitive and Amkor, and electrolytic Ni and electroless Ni in Motorola.

Cu-Cr/Cu/Au and Al/Ni(V)/Cu are thin film UBM, which are about 1μm thick. Electrolytic and electroless Cu and Ni are thick UBM and about 10μm in thickness.

The choice of UBM metals depends on the choice of solder materials. The reactions between molten solder and under bump metallization are a very challenging issue for the flip chip assembly. The details of this issue will not be discussed in this dissertation [9]-[12].

2.4 Electromigration theory

Electromigration is a phenomenon of a combination of thermal an electrical effects on mass motion. It is a diffusion phenomenon under an external0 driving force. 0-For a bulk metal, electromigration occurs at about three-quarter of its melting point (in absolute temperature). For a metallic polycrystalline thin film, electromigration occurs at about half of its melting point (in absolute temperature). A large number of atoms at this temperature would undergo random walk processes in the lattice and grain boundaries for the bulk and the thin film, respectively.

When a thin film stripe is stressed under a high current density, the electrons

would hit the atoms at the cathode side and the momentum would be exchanged between electrons and diffusing atoms. This phenomenon is formed by the interaction of two different types of force:

1. Coulombic force: the force between the electrostatic force and metal ion, when an external electric field is applied.
2. Electron wind force: the force made by the momentum exchange between electrons and diffusing atoms.

The atomic diffusion flux in a solid can be written as[17]:

$$J = -D\frac{\partial C}{\partial X} + \sum_i CM_i F_i \quad (2.1)$$

Where the first term represents the chemical potential gradient, and the second term represents the sum of different forces. For a pure metal, there is no chemical potential gradient between the atoms, so the first term is zero. The second term is what we discussed above, the combination of direct action of the electrostatic field and the momentum exchange of electrons and diffusing atoms. For simplicity, the second term can be written as[17]:

$$\sum_i CM_i F_i = F_{el} + F_{wd} \quad (2.2)$$

By comparing the magnitude between the electrostatic field force and the electron wind force, we can know that the electron wind force is much higher than the electrostatic field force so that the atoms would be pushed from the cathode side to the anode side. Besides, the dominative term F_{wd} can be written as[13]:

$$F_{wd} = EZ^* e \quad (2.3)$$

where E is the electric field, Z* is the effective charge number. Z* is a parameter to express how the atoms would migrate when they are effected by electromigration. So,

the Z* value would vary from different metal atoms. We can find solder have higher Z* than Al and Cu in table 2.2.Then, we can combine equation (2.1) and (2.2) [17]:

$$J = CMF_{wd} \quad (2.4)$$

where M is the mobility of the atoms and C is the atomic concentration. By using the Einstein equation, the mobility of atom can be written as:

$$M = \frac{D}{KT} \quad (2.5)$$

where D is the diffusivity, K is the Boltzmann's constant, T is the absolute temperature. Now, we can combine equation (2.3), (2.4) and (2.5), so we can obtain the following equation: $J_{em} = CMF_{wd} = C\frac{D}{KT}Z^{*}eE$ (2.6)

1896

2.5 Mean-time-to-failure (MTTF)

Electromigration is a diffusion behavior driven by the electrons. When the phenomenon is occurred, the resistance of the circuit would increase and cause the joule heating to increase the temperature of the integral circuit. So, mean-time-to-failure is a reference for the semiconductor industry to test the reliability of the device.

Mean-time-to-failure is able to predict the life time of electric device stressed under a certain current density and certain temperature. The equation that used for predicting the life time is called Black's equation.

$$MTTF = \frac{A}{j^{n}}\exp\left(\frac{Q}{KT}\right) \quad (2.7)$$

where A is a constant, j is the current density that we applied, n is an order parameter, Q is the activation energy for the broken of the device. However, when electric

current is applied into solder bumps, there must be a current crowding region that happens at the entrance of solder bumps, so the current density would increase largely between the solder bumps and the circuit than we calculate. At this time, the high current density would lead to joule heating so that the temperature would increase dramatically. If we don't modify the equation 2.7 properly or correctly, the mean-time-to-failure we predict by the information we have would have great difference with the correct time. So, the equation should be modified as following:

$$MTTF = \frac{A}{(Cj)^n} \exp\left(\frac{Q}{K(T+\Delta T)}\right)$$

where C is the modification of the current density, the ΔT is the modification of the extra temperature increase due to joule heating[15].

2.6 The electromigration behavior in solders

These years, due to the trend of miniaturization and the high performance, the dimension of integrated circuit keeps decreasing and the current that the circuit needs to carry keeps increasing, which causes the current density in the circuit to increase dramatically, and so do solder bumps. Therefore, there's more and more electromigration studies toward solder bumps. In solder stripe experience we can know Sn is more easily have electromigration effect than Al and Cu line as shown in the follow express

$$(j\Delta x)_c = \frac{\Delta \sigma \Omega}{Z^* e \rho}$$

$\Delta\sigma = Y\Delta\varepsilon$, $\Delta\varepsilon = 0.2\%$ at elastic limit

$$(j\Delta x)_c = \frac{Y\Delta \varepsilon\Omega}{Z^* e\rho}$$

where j is current density, ΔX is stripe distance, Ω is resistance, ρ is resistivity, Z^* is effect charge number, Y is Young's modulus.

Because solder have higher Z^* and lower Y than Al and Cu as shown in table2.2. So at the constant ΔX, the current density needed to fail solder is 2-3 orders smaller than that needed to fail Al or Cu. If Al or Cu fails at 10^5 A/cm^2 to 10^6 A/cm^2, solder will fail at 10^3 A/cm^2 or 10^4 A/cm^2.

The degradation mechanism of the solder bumps by electromigration is very similar with that of Al circuit. In 1999, Liu *et al* found electromigration in Sn-Pb solder bumps by sandwich structure[9]. After stressing under the current density of 1×10^5 A/cm^2 at room temperature for 19 days, they found that there were voids at the cathode side. There were some hillocks formed at the anode side as shown in Figure 2.7. Because most of the solders constitute at least 2 different metals, the diffusion mechanism of solder bumps is something different from that of the circuit, which is pure Cu or pure Al. Figure 2.8 show SEM images of hillocks formed in the pure Sn, $Sn_{80}Pb_{20}$, $Sn_{70}P_{b30}$, eutectic $Sn_{63}Pb_{37}$, $Sn_{40}Pb_{60}$, Sn_5Pb_{95}, which are stressed under the current density of 10^5 A/cm^2 for 40 hr [16].

In SEM images, we can find that hillocks grew more easily at grain side. Besides, we also find that the diffusion behavior is more active when the alloy is at eutectic composition, because they provide more diffusion interface in this region, so hillocks are more easily found in the eutectic phase region in Sn-rich alloy, as shown in figures 2.8 (b) and (c). If we compare figures 2.8 (a) to (f), it is not difficult for us to find that the Pb-rich alloy resists the eletromigration more readily than Sn-rich does. That is to say, for the Sn-Pb alloy, although Sn is the dominative factor for diffusion, the resist to electromigration still depends on the microstructure of the solder.

Besides, Lee *et al* found the movement of the Pb-phase in eutectic SnPb solders by flip chip solder bumps. Figure 2.9 is the cross-sectional view of the eutectic SnPb solder stressed under the current of 1.5 Amp amd 120℃. We can find that Pb-composition moved to the anode side and left voids at the cathode side due to electromigration phenomenon and the Ni layer in under bump metallization would melt due to the increase of temperature by joule heating. The reason is Pb is the dominative diffusion species that when temperature is above 100℃[18].

2.7 The melting phenomenon in solder bumps

From the discussion above, we know that in general, the failures usually starts from the interface of the solder bumps and the circuit. Due to this phenomenon, Yeh contributed the reason for this failure mechanism to the current crowding.

So, the current crowding phenomenon is another key point to determine how severe the device is affected by the electromigration. Current crowding usually happens at the corner when electrons go from the circuit to the solder bumps. That means the current density at this point would increase largely, due to current crowding phenomenon.

Figure 2.10 shows the Cu UBM on the top of the solder bump has asymmetric melting phenomenon after stressing by current[19]. Hu pointed that the Cu UBM would melt into solder bumps when stressing under the current of 1.27 Amp at 100℃, due to the local joule heating at the contact window. The Cu UBM on the chip side would be pushed into solder bumps to form intermetallic compound after stressing for 15mins, as shown in figure 2.10. Few minutes later, the Cu layer of the UBM would be consumed gradually and the solder replaced the location which is occupied by Cu originally. Finally, the solder would be filled with in the Cu circuit and the device would be broken.

M.O.Alam also point that when bump under 2A 20℃ i.e. current density is 3×10^4. Its average life time is 10s as shown in Fig. 2.11 [20]. It is mean joule heating is to large for bump to resistance and Localized dissolution of the Cu pad was found at the anode side, where the Cu trace was connected to the Cu bond pad. Because of this localized Cu dissolution, the electrical circuit become open. So enhance the IMC region which between solder and Cu may prevent Cu dissolution in solder.

2.8 Current crowding effect

In S.W. Liang, J. Mater. Res., Vol. 21, No. 1, Jan 2006 work, current density distribution in a solder joint was thoroughly studied by a three-dimensional finite element simulation. It was found that the maximum current density in a solder bump can be much higher than the average one that was previously projected. It locates itself near the solder/underbump metallization (UBM) interface, which serves as a vacancy flux divergence plane and favors electromigration occurring at that location. Consequently, the solder joint is more prone to electromigration. The cause of such locally high current density is a result of the current crowding effect. Current crowding occurring in the solder joints is due to the current flow experiencing a dramatic geometrical and resistance transition from the thin on-chip metal line to the solder bump. Because the cross-section of the Al trace on the chip side is about two orders smaller than that of the solder joints, the majority of the current will tend to gather near the Al/UBM entrance point to enter the solder bump instead of spreading uniformly across the opening before entering the bump. The materials near the entrance point experience a current density of about one order of magnitude higher than the average value. Current crowding plays a critical role in the electromigration failure of the solder joints.

2.9 Motivation of this steady IMC character

IMC is high electrical resistivity materials as shown in table2.1. Pure Ni electrical resistivity is 6.2 μΩ-cm and its IMC formed with Sn is Ni_3Sn_4. Its resistivity is 28.5 μΩ-cm at 298K. The electrical resistivity of Cu electrical is 1.58 μΩ-cm and its IMC formed with Sn is Cu_6Sn_5. Its resistivity is 17.5 μΩ-cm at 298K. The electrical resistivity of Sn is 11.5 μΩ-cm and Pb is 19.3μΩ-cm. And Sn-37Pb just is 14.5 μΩ-cm [21] [22] [23]. We can easily find Ni_3Sn_4 resistivity is higher than solder bump more about two times. The electrical resistivity of Cu_6Sn_5 also higher than solder. In addition, Chen and co-workers [24-32] have studied IMC formation in several diffusion couples such as Sn/Ni, Sn/Ag, Sn/Cu, and other solder, etc., with a DC current density of 10^2-10^3A/cm^2. They observed a directional effect of electric current on the IMC thickness at the interface at a current density of 5×10^2A/cm^2.

H.L.Chao et al. points that IMC may induce local concentration of tensile stresses and drive interfacial crack formation[32]. Min Ding also point that the morphology of the cracks form under EM in the Cu and Ni UBM bumps is different in that the crack are sharp and more confined to the interface in the Ni UBM bump in contrast to the blunt and more spreading cracks in the Cu UBM bump. They suggests that the UBM dimension and design can affect the characteristics of IMCs and crack formation, which may well be important in controlling damage evolution and EM reliability [33].

We think its may have interesting result if we make IMC thicker before electromigration test. The most important result maybe is that life time of solder bump change apparent.

Table 2.1 Electrical Resistivity,T_{mp} and TCR of Sn, Pb and alloy

Alloy	T_{mp} (°C)	Temp. (K)	Electrical Resistivity (μΩ-cm)	TCR (10^{-3} K^{-1})
Sn (pure)	232		11.5	
Sn-37Pb	183		14.5	
Aluminum			2.61	
Copper		293	1.58	4.3
Lead		293	19.3	4.2
Nickel		293	6.2	6.8
Tin	293		10.1	4.6
Ni_3Sn_4		298	28.5	
Cu_3Sn		298	8.93	
Cu_6Sn_5		298	17.5	

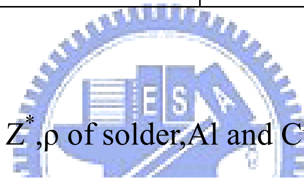


Table 2.2 Y(Yong's modulus), Z^*,ρ of solder,Al and Cu

<table>
<tr><th></th><th>Y(Gpa)</th><th>Z*</th><th>ρ(μΩ-cm)</th></tr>
<tr><td>Solder</td><td>~30</td><td>~30</td><td>~22</td></tr>
<tr><td>Al</td><td>~69</td><td rowspan="2">2~4</td><td rowspan="2">~2</td></tr>
<tr><td>Cu</td><td>~110</td></tr>
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