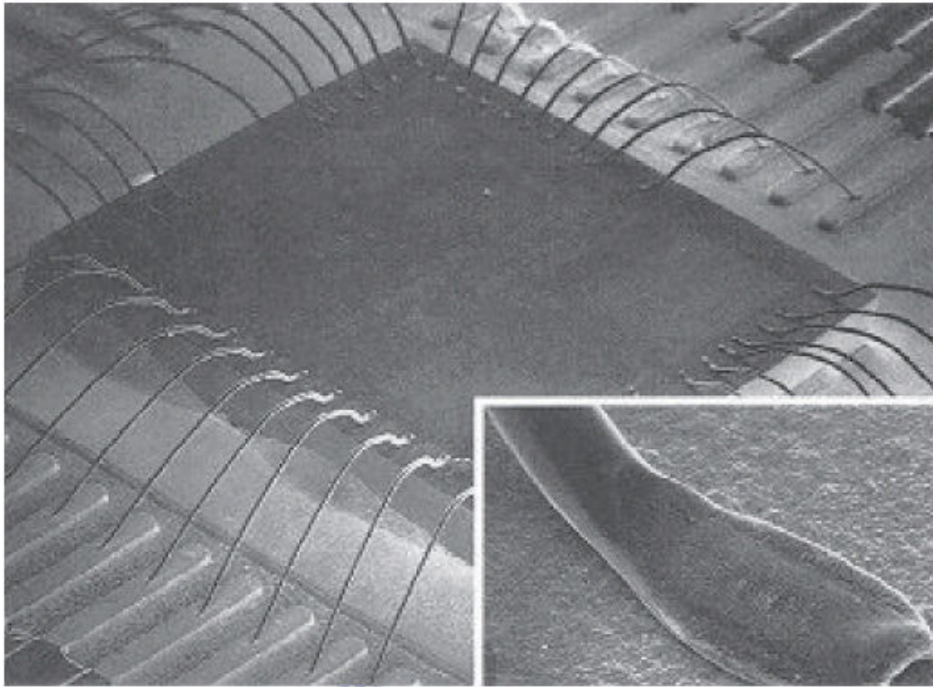


Fig. 2.1 Conventional hierarchy of electronic packaging (first 3 levels)

[2] C. S. Chang, A. Oscilowski, and R. C. Bracken, IEEE Circuits Devices Mag. 14, 45 (1998).

(a)



(b)

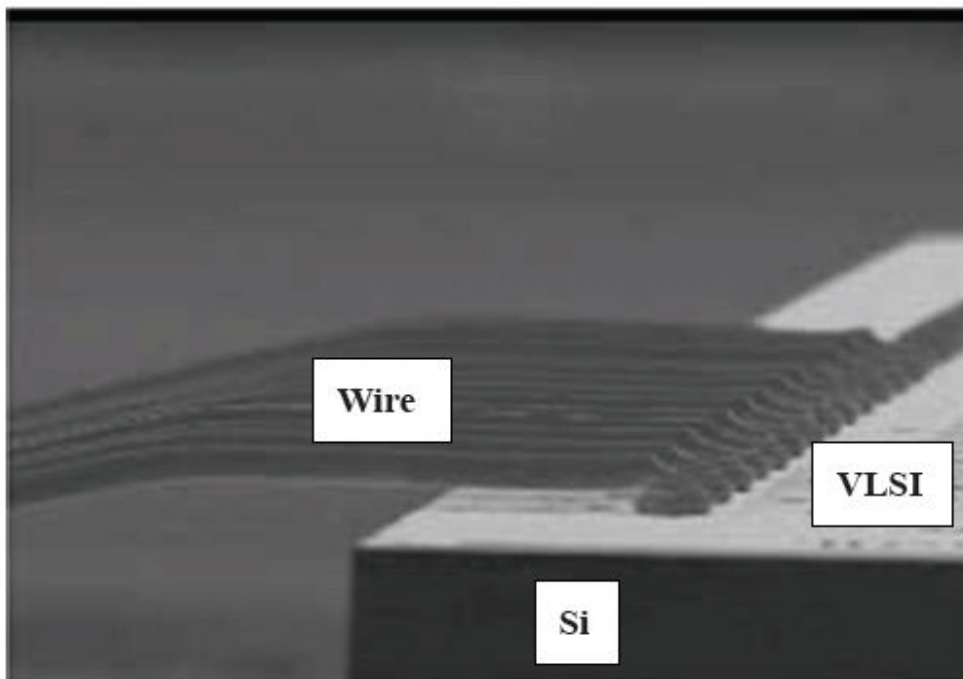
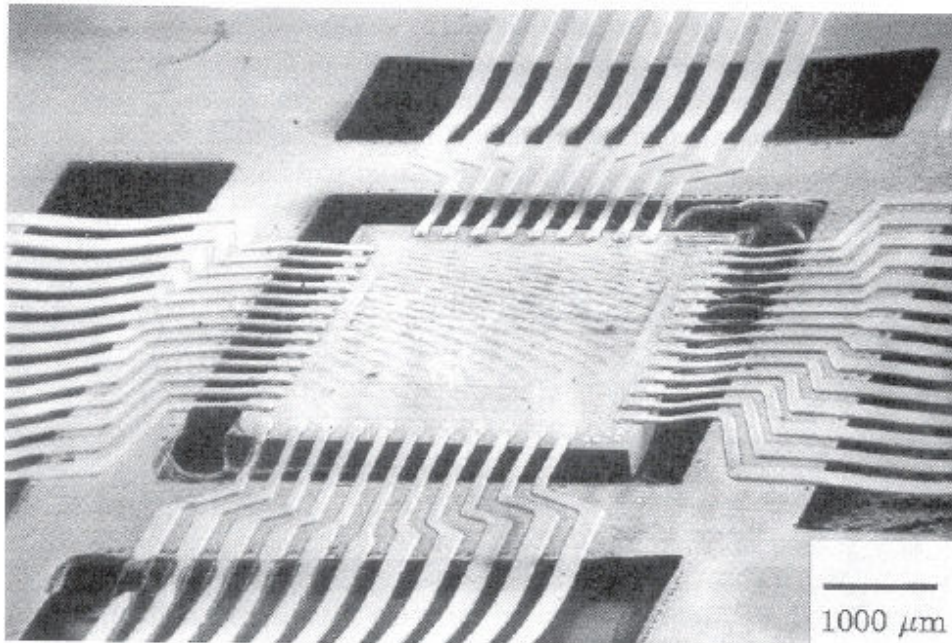


Fig. 2.2 (a) SEM micrograph of a wire bonding (b) Side-view SEM micrograph of wire bonding

(a)



(b)

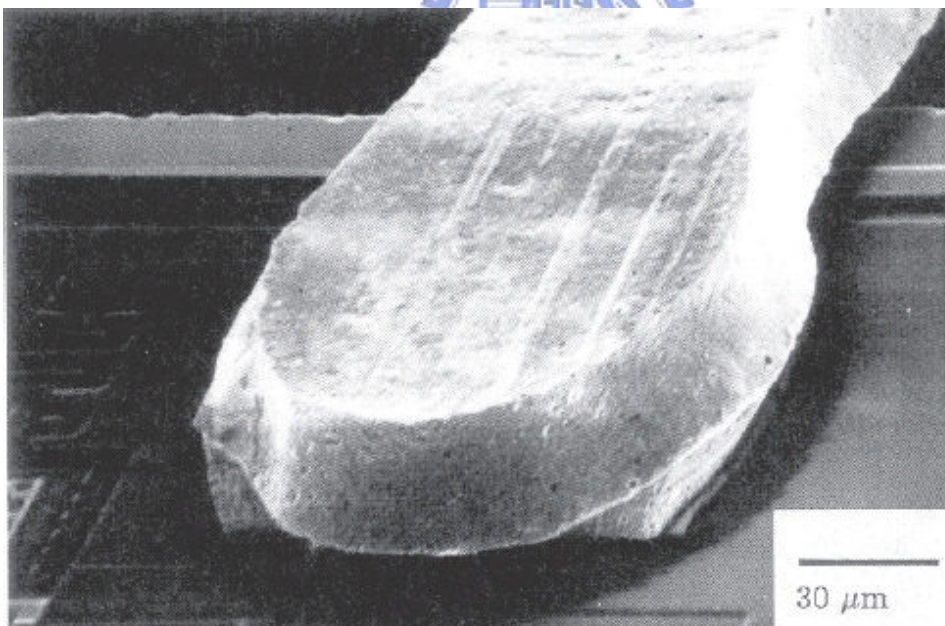


Fig. 2.3 (a) Scanning electron micrograph of a TAB inner lead bonding. (b) Scanning electron micrograph of a single inner lead bonded bumped pad.

[3] The International Technology Roadmap for Semiconductor, Semiconductor Industry Association, 2003.

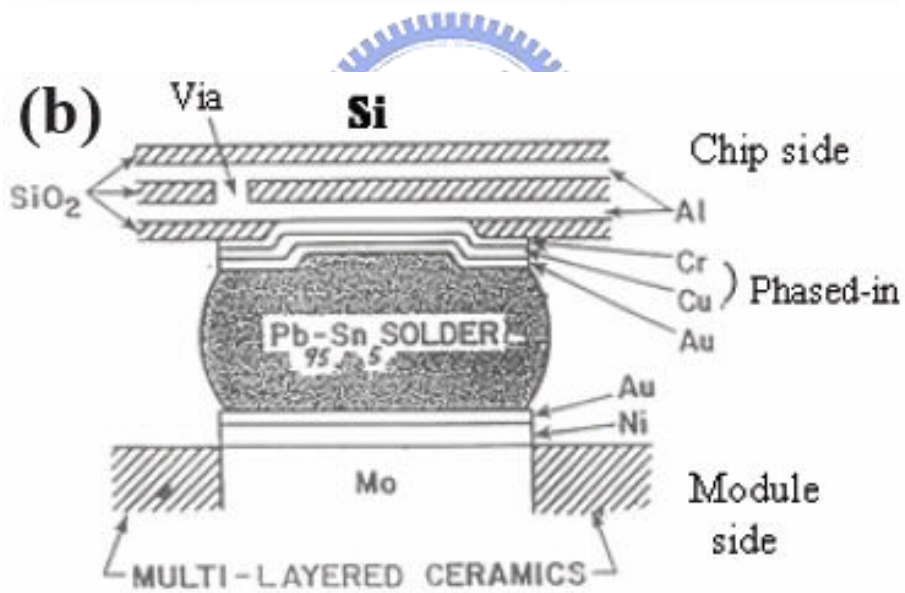
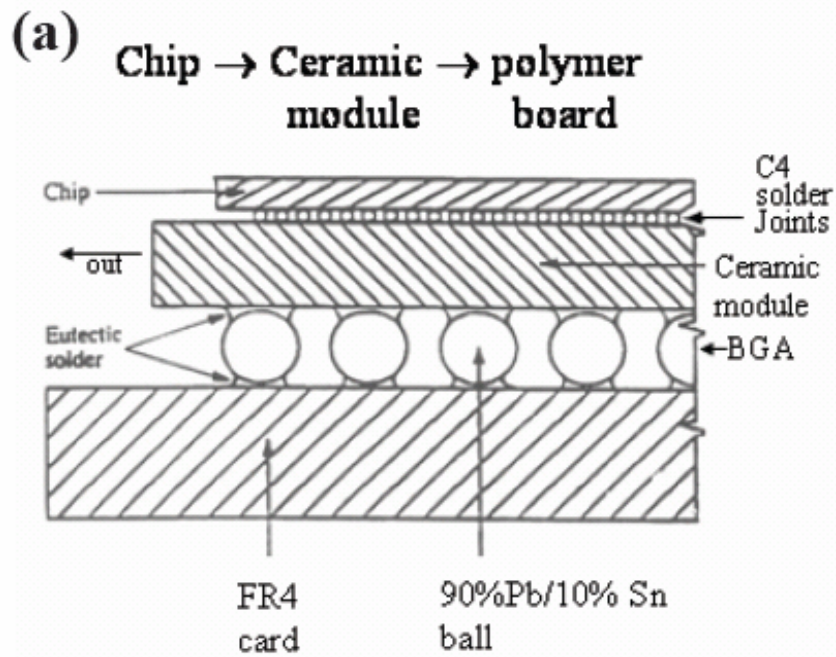


Fig. 2.4 (a) Schematic diagrams of two level flip chip packaging (b) solder bump used for flip-chip bonding with the interface structure at both the Si side and substrate side.

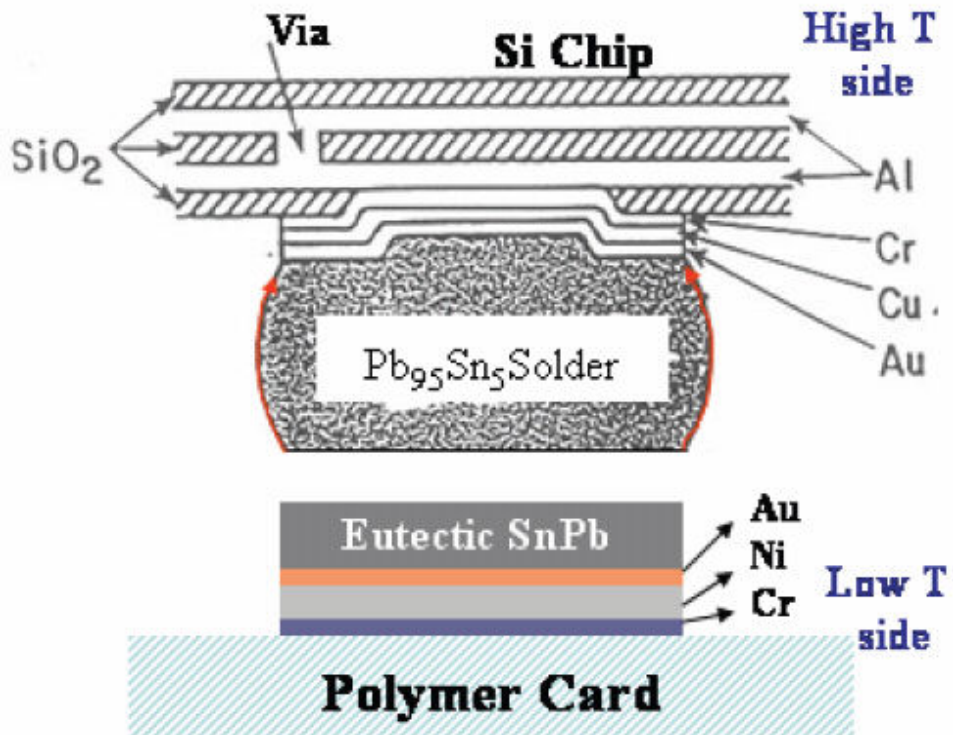


Fig. 2.5 Schematic diagram of the composite solder joint. The thin eutectic solder can be deposited on the organic substrate before joining.

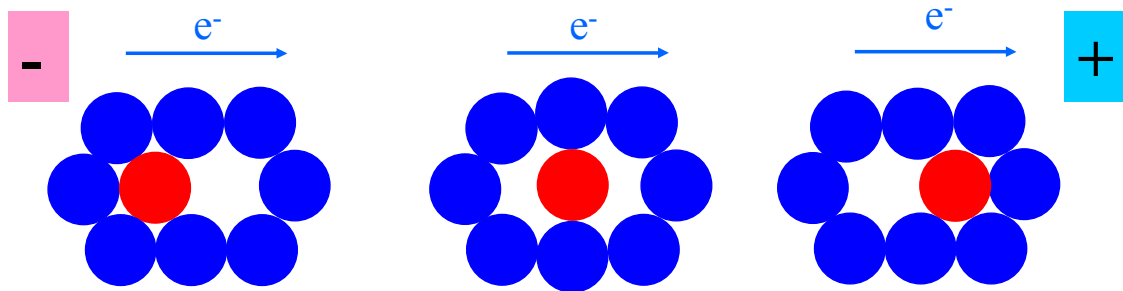


Fig. 2.6 Schematic diagram of Electromigration behavior

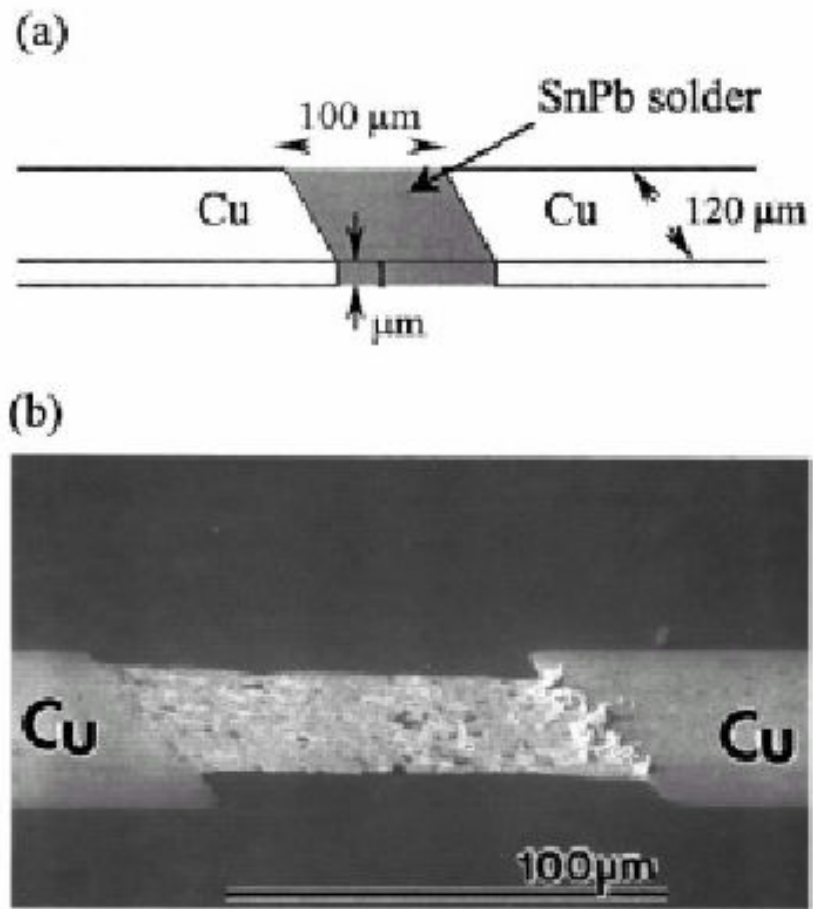


Fig. 2.7 (a) schematic illustration of Sandwich structure (b) SEM image of Sn-Pb solder stressed at  $1 \times 10^5\ \text{A/cm}^2$  at room temperature for 19 days.

[16] C. Y. Liu, Chih Chen, and K. N. Tu, J. Appl. Phys., 88, 5703 (2000).

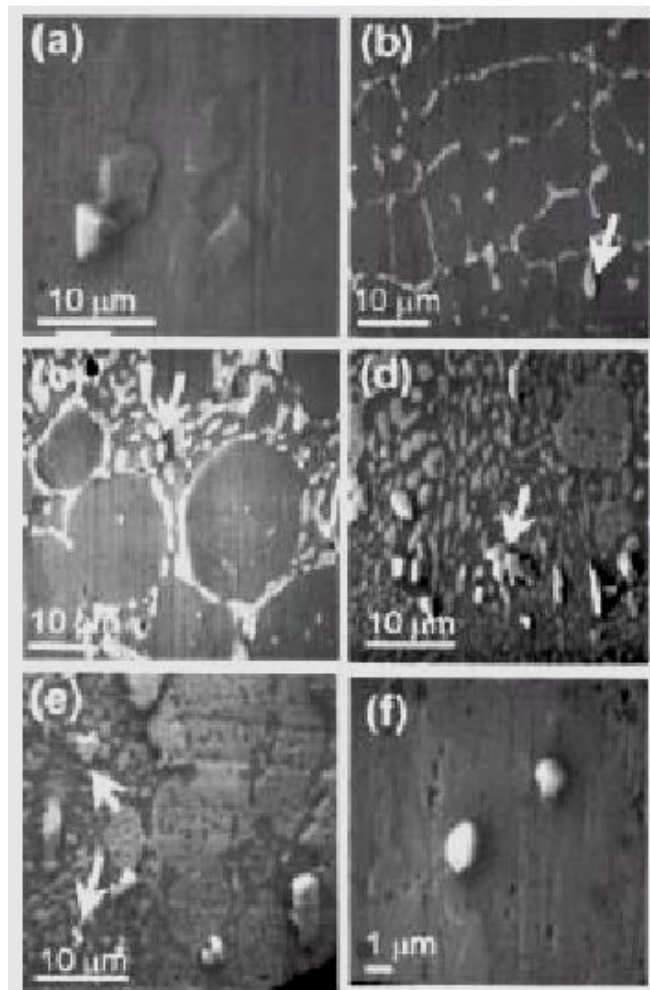


Fig. 2.8 The hillocks formed in the alloy, which has different Sn, Pb composition, stressed at  $10^5$  A/cm<sup>2</sup> for 40 h (a) pure Sn; (b) Sn<sub>80</sub>Pb<sub>20</sub>; (c) Sn<sub>70</sub>Pb<sub>30</sub>; (d) eutectic Sn<sub>63</sub>Pb<sub>37</sub>; (e) Sn<sub>40</sub>Pb<sub>60</sub>; (f) Sn<sub>5</sub>Pb<sub>95</sub>.

[16] C. Y. Liu, Chih Chen, and K. N. Tu, J. Appl. Phys., 88, 5703 (2000).

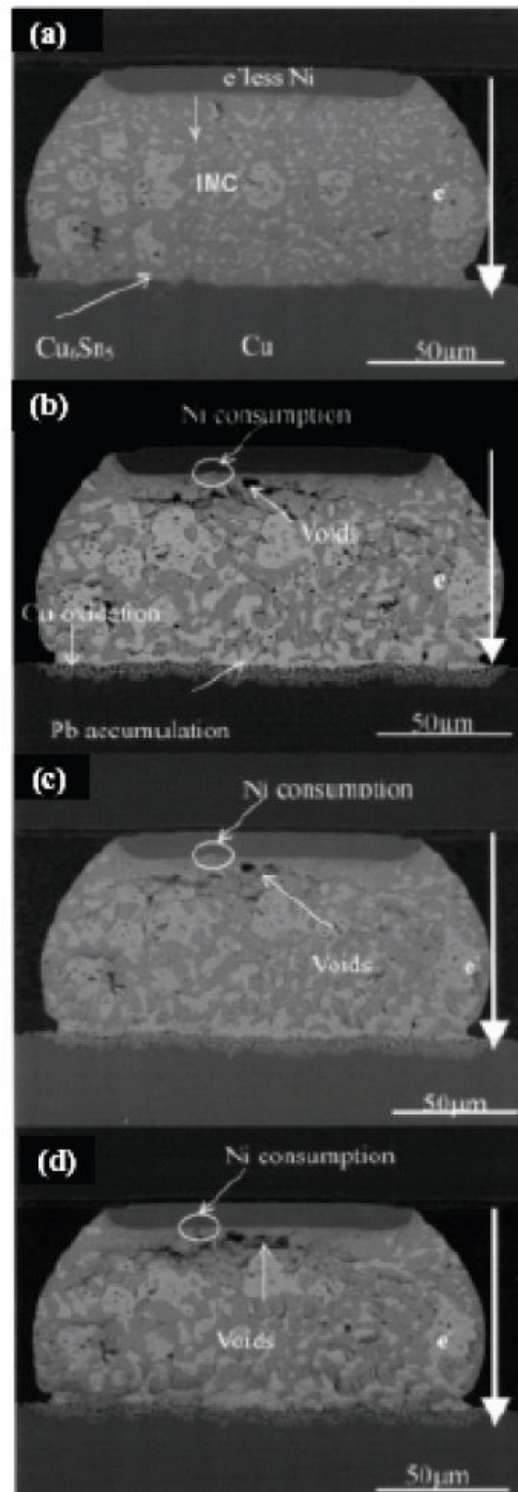


Fig. 2.9 Cross-sectional-view of SEM images of eutectic SnPb solder bumps stressed under the current of 1.5 Amp and 120°C. (a) 0 h; (b) 20 h; (c) 30 h; (d) 39.5 h. [18] T.Y. Lee, K.N. Tu, and D.R. Frear, J. Appl. Phys., 90, 4502 (2001)



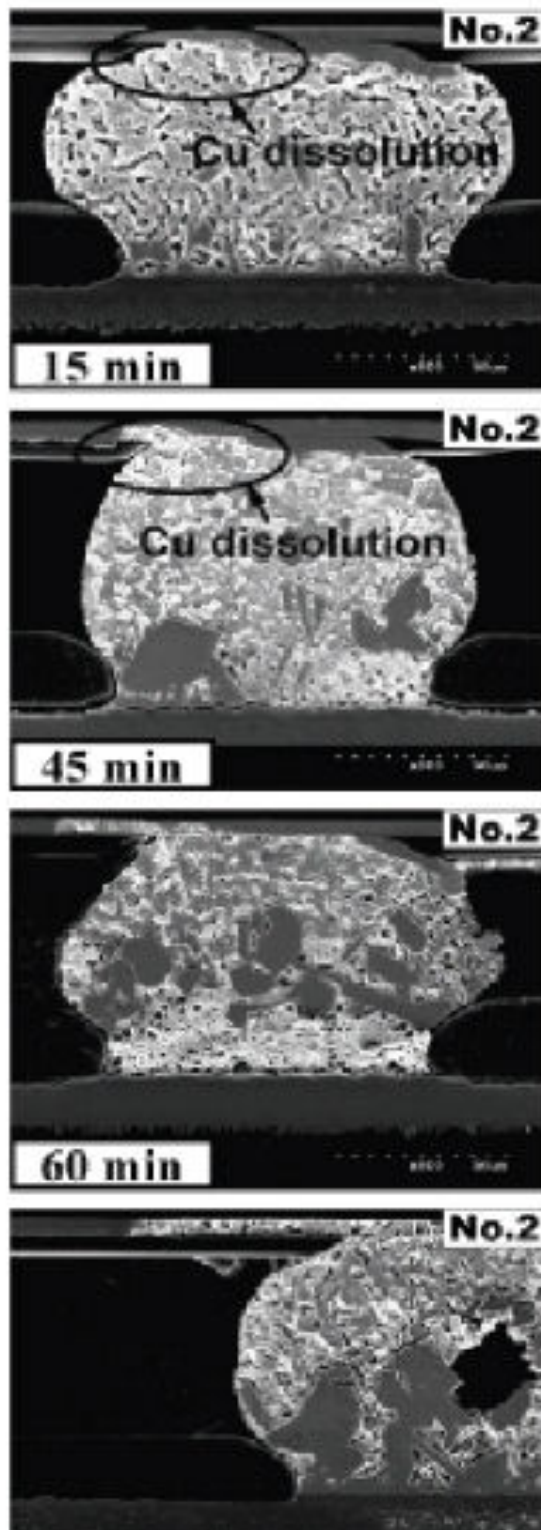
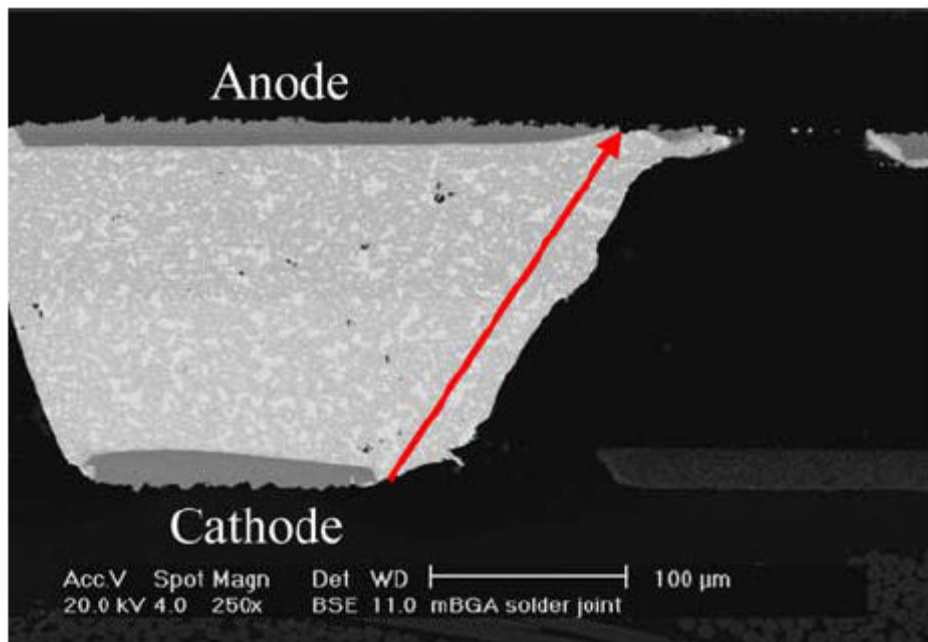
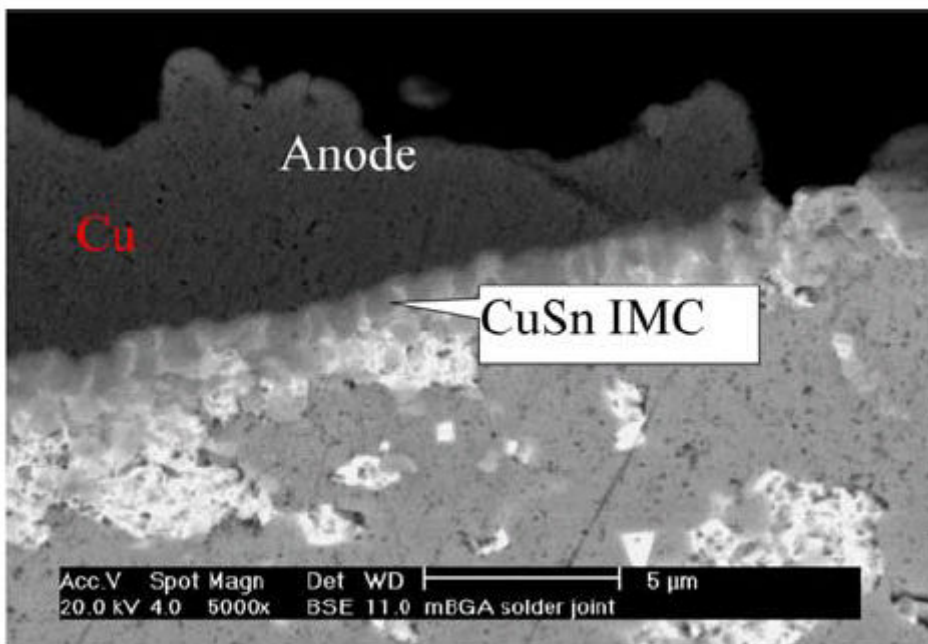


Fig. 2.10 The Cu UBM melted asymmetrically due to current crowding.  
[19] Y. C. Hu, Y. H. Lin, and C. R. Kao, *J. Mater. Res.*, 18, 2544, (2003).



a



b

Fig. 2.11 Cross-section SEM image of typical failed joint which failed at 10s of 2A current stressing at room temperature (a)Whole solder joint (b) magnified view of the dissolved area at the component side.

[20] M.O.Alam, B.Y.Wu, Y.C.Chan, K.N.Tu. Acta Materialia, 54(2006)613-621