國立交通大學

材料科學與工程學系

博士論文

覆晶封裝銲錫接點在電遷移效應下之熱與電特性

Thermo-electrical characterizations in flip-chip solder joints during electromigration

研究生：梁世緯

指導教授：陳智　教授

中華民國九十八年七月

覆晶封裝銲錫接點在電遷移效應下之熱與電特性

Thermo-electrical characterizations in flip-chip solder joints during electromigration

研 究 生： 梁世緯　　Student： Shih-Wei Liang

指導教授： 陳智　　Advisor： Dr. Chih Chen

國立交通大學

材料科學與工程所

博士論文

A Thesis

Submitted to Department of Materials Science and Engineering

College of Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of Ph.D. in

Materials Science and Engineering

July 2009

Hsinchu, Taiwan, Republic of China

中華民國 九十八 年 七 月

覆晶封裝銲錫接點在電遷移效應下之熱與電特性

學生：梁世緯　　指導教授：陳智 博士

國立交通大學材料科學與工程學系

摘　要

覆晶封裝銲錫接點的電遷移與熱遷移是可靠度上的重要議題，是故了解覆晶封裝銲錫接點的熱電效應相當重要。本研究利用實驗與有限元素分析法研究銲錫接點在測試時的熱電特徵。首先利用聚焦離子束製備出具有記號的銲錫接點，驗證出電遷移速率與電流密度呈現正比的關係；再者因為四點量測的結構改用，可以使得凸塊電阻可直接量測出來，並且在不同位置量測到的電阻有所不同；隨著電遷移產生孔洞並成長，使得電流密度與溫度重新分佈的情形都可以利用模擬得知，會發現銲錫接點內部的電流密度與溫度在孔洞生成 50%時，會先些許下降，當孔洞持續成長的時候，電流密度與溫度會改為上升；此外利用不同線寬的導線研究導線寬度對電遷移壽命的影響，發現導線線寬會影響電流集中效應與焦耳熱效應，但主要還是熱的影響，使得線寬比較寬的時候，壽命得以延長；另外還討論銲錫接點在通電後期

造成的熔化，主要是來自於導線的劣化損壞，使得溫度急遽上升達到熔點；最後，因為電流集中效應的關係，使得覆晶封裝銲錫接點內部的溫度呈現非線性分佈。

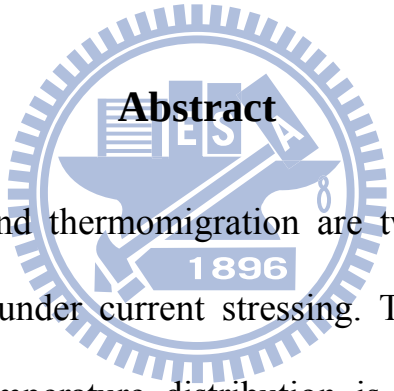
另外利用模擬的結果討論利用變換底部金屬層材料、鋁導線設計、底部金屬層厚度以及接觸窗口大小，設法找出覆晶封裝銲錫接點之最佳化結構，以供後續設計之參考。最後在分析當銲錫接點越做越小時，對溫度與電流密度之影響，並對矽晶片在三度空間堆疊下，將會減薄矽晶片厚度，而當矽晶片變薄之下，對銲錫接點溫度之影響。此些議題將在此研究裡詳細地討論。

Thermo-electrical characterizations in flip-chip solder joints during electromigration

Student：Shih-Wei Liang Advisor：Dr. Chih Chen

Department of Materials Science and Engineering

National Chiao Tung University



Abstract

Electromigration and thermomigration are two important issues in flip-chip solder joints under current stressing. Thus, to investigate the current density and temperature distribution is quite valuable. In this study, the experiments and finite-elements method were used to understand the thermo-electrical characterizations in flip-chip solder bumps under current stressing.

The observation of marker movement made by focused ion beam (FIB) confirmed that the electromigration flux is proportional to the current density. Using the four-point probing, the bump resistance was measured directly. Also, the bump resistance changed due to the change

of measuring position. Due to the void formation and propagation, the current density and temperature re-distributed. Before the voids grew and became 50% of the contact opening, the current density and temperature decreased slightly. When the voids continuously grew, the current density and temperature increased. The width of Al trace affected the current crowding and Joule heating effect in the flip-chip solder joints. The main effect on mean-time-to-failure (MTTF) is the Joule heating effect. Then, the key reason causing the solder melting at the final stressing period is the degradation of Al trace. Rapid increase in Al trace resistance caused the abrupt Joule heating to melt the solder bumps. The non-linear thermal gradient was found in flip-chip solder joints under current stressing due to current crowding effect.

In addition, the simulation study was carried out in order to find the suitable UBM material, Al trace's designation, the thickness of UBM and the size of contact opening, so as to determine the optimal structure of flip-chip solder joints. These results are useful guidelines for later designation. Afterward, to analyze its effects on temperature and electric current density when the size of flip-chip solder joints shrink. When pilling up in three dimensions, Si chip will be thinner, the effect of this change on flip-chip solder joints will thoroughly be discussed as well.

Acknowledgements

感謝我的指導教授**陳智**老師，在我還是應數系的時候可以收我做為專題生，之後鼓勵我攻讀材料所碩博士，老師對我的指導不僅是在專業的研究領域，做人處事方面也是我值得學習的楷模。陳智老師給我有許多參與國際研討會的機會，甚至讓我可以出國執行千里馬計畫一年，眾多的出國經驗不僅讓我體驗各國風情，更重要的是培養我的國際觀，不會只是閉門造車。在 UCLA 的期間，我特別要感謝**杜經寧**院士對我的照顧，杜老師把我當成自己的學生一樣，細心教導，傳授許多平時會忽略的物理觀念，對我的研究有甚多幫助，對我的生活也是關心有加，讓我在 LA 並沒有太嚴重的思鄉情結。在此也要感謝我的口試委員：**高振宏**教授、**謝宗雍**教授、**饒達仁**教授與**賴逸少**博士，對我論文的批評與指教，讓我知道我的學習仍然不足，我必須更嚴謹的態度來面對我的研究。

不能忘記的還有一路上陪我的一起努力，互相砥礪的學長姐與學弟妹們：感謝**穎超**學長，無時不刻對我的耳提面命，常常在人生的道路上指引我；**棟樑**學長與**大鈞**帶領我進入到模擬的領域，讓我得以完成我的博士論文；**慶榮**學長與**章賓**學長教導我對儀器操作與實驗進行，讓我都有莫大的啟發；給我快樂的**書宏**學長與**鈺庭**學長，常常在實驗煩悶之餘，讓我覺得還有溫暖跟開心；謝謝**聖翔**學長與**翔耀**在實驗上的協助，讓我可以能完善的分析；還有**筱芸**學姊與**阿丸**，更是我最無所不聊的好友，謝謝你們的耐心，常常可以讓我發洩；忠厚老實的**詠湟**學長和可愛的**佳凌**學妹，更是讓我永難忘懷，我會常常回來找你們；感謝**阿光**學長、**德聖**學長、**淵明**學長、**宏誌**學長、**程昶**學長與**佩君**學姐，在我剛進實驗室對我的照顧；一起打拼的**哲誠**、**舜民**、**俊宏**和**健民**，發現我們曾經的擁有，卻是那樣的永恆；還有我最喜歡的學弟妹們**宗寬**、**誠風**、**小山**、**宗憲**、**旻峰**跟**明慧**，看著你們畢業的時候，那種離情依依的感覺，自今還感動萬分；新加入實驗室的學弟妹們，**漢文**、**岱霖**、**瑋安**、**建志**、**右峻**、**若薇**跟**曉葳**，祝福你們可以順利的完成之後的實驗，快快樂樂畢業；以及我最愛的系辦小姐們：**蕙馨**、**克瑤**與**麗娟**，有你們的幫忙，才讓我可以順利畢業。有你們的陪伴，實驗室的生活是如此的多采多姿與充滿歡樂。

在 UCLA 的朋友們，我的好室友**居呈**學長、**苡嘉**、**欣蘋**、**汎怡**、**子瑜**學姊、**Peter** 學長，有你們的照顧，我才能夠活在 LA。千里馬俱樂部的**亮雯**、**東耘**、**勝文**、**美杏**、**于鵬**與**政玄**，讓我玩在 LA。

最後要感謝我的家人，爸爸、媽媽、大姐、二姐與我可愛的外甥祐安，謝謝你們可以對任性的我無微不至照顧，沒有你們，就沒有今天的我。畢業真好。

Contents

Figure captions

List of tables

Chapter 1 Introduction

1.1 Flip-chip technology

To meet the relentless drive for miniaturization of portable devices, flip-chip technology has been adopted for high-density packaging due to its excellent electrical characteristic and superior heat dissipation capability [1]. In 1960s, IBM first developed the flip-chip technology, which was named as controlled-collapse-chip-connection (C4) [2-4]. In C4 technology, high-Pb solder with high melting temperature of 320 °C was used as solder joint material [5]. Then the chip was aligned on the ceramic substrate and reflow soldering was performed to form the solder joints. C4 technology gained wide utilization in 1980 since it can provide a great number of advantages in size, performance, flexibility, reliability and cost than other packaging methods. Owing to area array capability in flip-chip technology, the size of entire die, the height of solder bump, and the length of interconnect are effectively reduced, providing higher input/output (I/O) pin count and signal propagation speed in electronic devices.

Before flip-chip assemblies, solder bumps need to deposit onto the under bump metallurgy (UBM) on the chip side. The requirements for UBM are: (1) it must adhere well both to the underlying metal line, like Al or Cu, and to the surrounding IC

passivation layer; (2) it is able to provide a sufficient barrier to prevent the diffusion of other bump metals into the integrated circuit (IC); (3) it needs to be wettable by the bump metals during solder reflow. For example, a thin film Cr/Cu/Au UBM is adopted for the high-Pb solder alloy in C4 technology.

The typical of solder joints on silicon (Si) chip is shown in Figure 1-1 (a). Figure 1-1(b) is the schematic diagram of the cross-section of the flip-chip solder joints. As depicted in Figure 1-1(c), the chip is then placed upside down (flip chip), and all the joints are formed simultaneously between chip and substrate during the reflowing process. In flip-chip process, electrical connections are the array of solder bumps on the chip surface, hence interconnects distance between package and chip is effectively reduced. The density of I/O is limited by the minimum distance between adjacent bonding pads. For high ends device and when size reduction is the main concern, area-arrayed flip-chip technology is the only choice to meet the needs.

However, flip-chip technology has some evolutions due to certain concern. In order to cost down the consumer electronics, the polymer substrates, like bismaleimide triazine (BT) or flame retardant 4 (FR4) printed circuit board, are used to replace the ceramic substrate. For this concern, the high-Pb solder has no longer been used due to its high melting point of 320 °C since polymers have relatively low glass transition temperature. Thus, the eutectic-SnPb solder alloy can be used to solve

this problem for its low melting point of 183 °C. Next, owing to the environment concern, the Pb-free solder alloys replace the Pb-containing solder alloys due to the toxicity of Pb. Then, the thin film UBM will not be suitable for this change. Therefore, the electroplating 5-μm Cu or 5-μm Cu/3-μm Ni was used as the UBM for the lead-free solder joints. Because of these evolutions, several kinds of solder alloys and UBMs are able to select for the flip-chip assembly. This makes flip-chip technology become complex since there are too many combinations. But the key is to find the best solder alloy and UBM so as to provide a lot of benefits to the company.

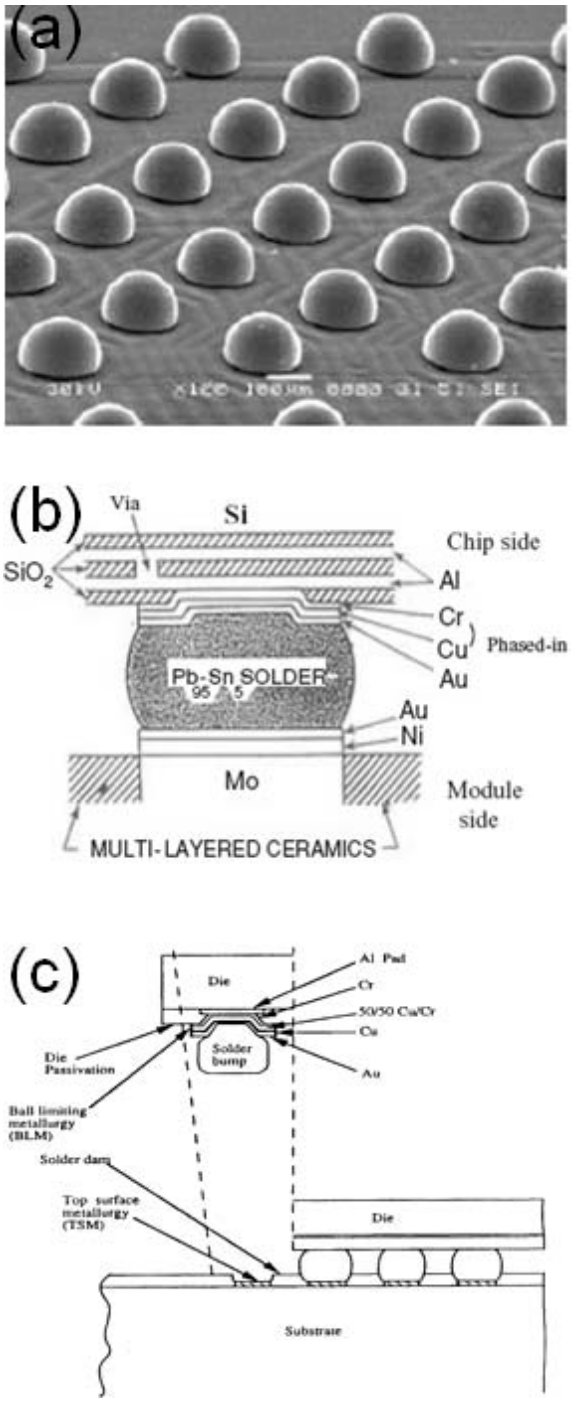


Figure 1-1: (a) Tilt-view of SEM image of arrays of solder bumps on silicon die. (b) A flip-chip solder joint to connect the chip side and the module side. (c) The chip is placed upside down (flip chip), and all the joints are formed simultaneously between chip and substrate by reflow. [??]

1.2 Electromigration

Electromigration (EM) has been the most persistent reliability issue in interconnects of microelectronic devices. Electromigration is defined as mass transport due to momentum transfer between conducting electrons and diffusing metal atoms. For EM in a metal, the driving force acting on a diffusion atom consists two forces: (1) the direct action of the electrostatic field on the diffusing atom, electrostatic force, and (2) the momentum exchange between the moving electrons and the ionic atoms, electron wind force. It can be expressed as [6]:

$$F = F_{direct} + F_{wind} = Z^* eE = (Z^*_{el} + Z^*_{wd})eE \quad (1.1)$$

where Z* is the effective charge number, e is the electron charge, and E is the electric field (E = ρj, where ρ is resistivity and j is current density). The effective charge Z* includes two terms, Z^*_{el} and Z^*_{wd}. Z^*_{el} is nominal valence of the diffusing ions in the metal when the dynamic screening effect is ignored. $Z^*_{el}eE$ is named as direct force, which draws atoms towards the electrode in negative bias. On the other hand, Z^*_{wd}, represents the momentum exchange effect between electrons and the diffusion ions. Generally speaking, the electron wind force, $Z^*_{wd}eE$, is dominant and is found to be on the order of 10 for high conductivity metals such as Ag, Al, Cu, Pb. Sn, etc [7]. Z^*_{wd} can also be positive, but it was found that only in transition elements with complex band structures where electron hole conduction plays a more important role

[8].

The atomic flux is related to the electric field and thus the current density. The flux equation can then be expressed as the following:

$$J = J_{chem} + J_{em} = -D\frac{dC}{dx} + C\frac{D}{kT}Z^{*}eE \tag{1.2}$$

where C is concentration of diffusing species, D is the diffusivity, k is Boltzmann's constant, and T is temperature.

After stressing for extended time, atoms in interconnects accumulate on the anode end and voids appear on the cathode side, resulting in open failure eventually. In general, the average drift velocity of atoms due to EM is given by Huntigton and Grone [6]:

$$v = \frac{J}{C} = \frac{D}{kT}Z^{*}eE = \frac{D}{kT}Z^{*}e\rho j \tag{1.3}$$

In 1976, the mass transport caused by EM was first observed in Al metal interconnects. Figure 1-2 (a) is schematic diagram of Blech structure with a short Al or Cu strip on a base line of TiN [9,10]. Because the resistance of Al or Cu is lower than that of TiN, the current will take the lowest resistance path and go along the strip of Al or Cu when the voltage bias is applied. After some period of time, a depleted region occurs at the cathode and an extrusion occurs at the anode. Figure 1-2 (b) is the top view of scanning electron microscope (SEM) image of a Cu strip tested for 99 hrs at 350 °C with current density of 5×10^5 A/cm^2 [11]. The EM clearly occurred in this

Cu strip. In addition, from the mass conservation point of view, both depletion and extrusion should have the same volume change. Thus, the drift velocity can be calculated from the rate of depletion volume.

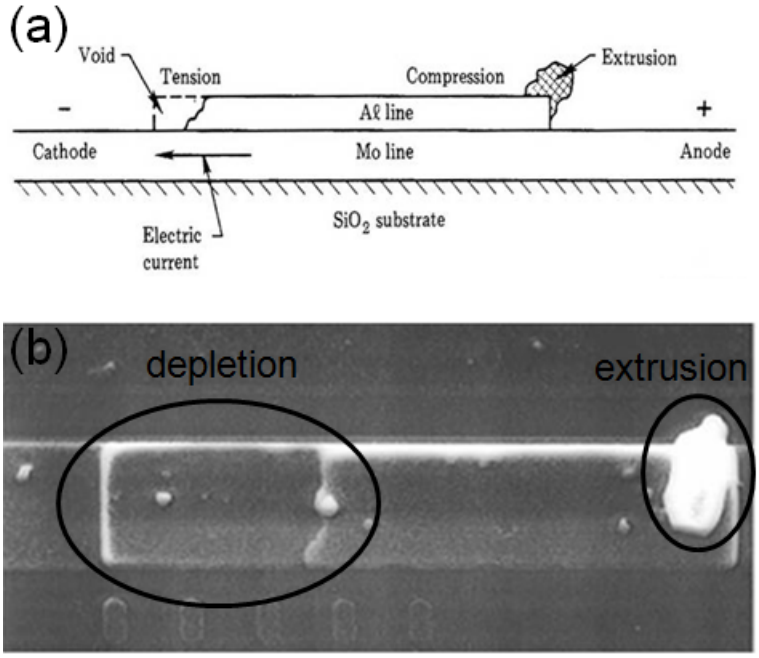


Figure 1-2: (a) A schematic diagram of typical EM behavior in a Al stripe. (b) SEM images of the morphology of a Cu strip tested for 99 hrs at 350 °C with current density of 5×10^5 A/cm^2. [11]

1.3 Electromigration behavior in flip-chip solder joints

In 1998, Brandenburg and Yeh first reported the EM failure in flip-chip solder joints with eutectic SnPb [12]. In their research, some interesting observations were found as follows: (1) the current density inducing in EM failure in the solder joints is two order of magnitude lower than that in the Al; (2) the failure mode is pan-cake type void formation in the cathode end; (3) the redistribution of Pb-rich and Sn-rich phase was observed. Nowadays, to meet the higher demands for device's performance, the I/O numbers is expected to increase while the dimension of each individual joint shrunks accordingly. To date, each bump measures at 100 μm or less in diameter. The design rule of packaging dictates that each bump is likely to carry current of 0.2 to 0.4 A. Due to this requirement, carry-on current density in the solder bumps must be increased over 1×10^4 A/cm^2. This renders EM a daunting reliability issue in flip-chip solder joints under such high current density [13]. In below, the four characteristics for EM in flip chip solder joints will be thoroughly addressed.

1.3.1 Current crowding effect

Current crowding phenomenon is a unique behavior in flip-chip solder joints under current stressing. However, the current crowding cannot be observed directly. The two-dimensional simulation of current crowding effect in flip-chip solder joints is

report by Yeh *et al* as shown in Figure 1-3 [14, 15]. It was found that the maximum current density in a solder bump can be much higher than the average one that was previously projected. It locates itself near the solder / UBM interface. Current crowding occurs in solder joints is due to the current flow experiences a dramatic geometrical and resistance transition from the thin on-chip metal line to the solder bump. Because the cross-section of the Al trace on the chip side is about two orders smaller than that of the solder joints, the majority of the current tends to gather near Al-to-UBM entrance point to enter the solder bump instead of spreading uniformly across the opening before entering the bump. The materials near the entrance point experience a current density of about one order of magnitude higher than the average value.

In previous study, Shao *et al* study the current density distribution in a solder joint by a three-dimensional simulation [16,17]. Figure 1-4 (a) illustrates the typical current density distribution in three-dimensions. From the cross-sectional view along the Al trace of the whole bump, as shown in Figure 1-4 (b), the current crowds in the solder bump near the entrance point of the Al trace. Also, from this study, the current density distributions across six positions of the solder bump have been discussed. Figures 1-5 (a) to (f) show the current density distribution of six layers for the UBM layer, IMC layer, top layer of solder, middle layer of solder, necking layer of solder,

and bottom layer of solder, respectively. The high current region for each layer is close to the left hand side which is current entrance point. That means the current goes from Al trace and through the shortest path in the solder joint, and then leaves through the Cu line. It needs to note that the direction of current is opposite to electron charge flow. Figures 1-6 (a) to (f) are the corresponding three-dimensional profile to Figures 1-5 (a) to (f). According to three-dimensional current density profile, it gives a clear picture how the current distribute inside the solder joints.

"Crowding ratio" was used to define the degree of the current crowding effect. Donation of "crowding ratio" is that the local maximum current density in the solder joints divided by the average current density on the UBM opening.

Also, it is worth to mention that current crowding effect leads to non-uniform current distribution inside a solder joint and in turn leads to non-uniform drift velocity (see Section 1.2). The drift velocity is proportional to the current density and non-uniform temperature distribution inside a solder joint due to local Joule heating effect (see Section 1.3.2) [14]. As a result, EM-induced damage occurs near the contact between the on-chip line and the bump; voids formation for the bumps with electrons downward and hillock or whisker for the bumps with electrons upward. Therefore, current crowding effect plays a crucial role in the flip-chip solder joints under EM.

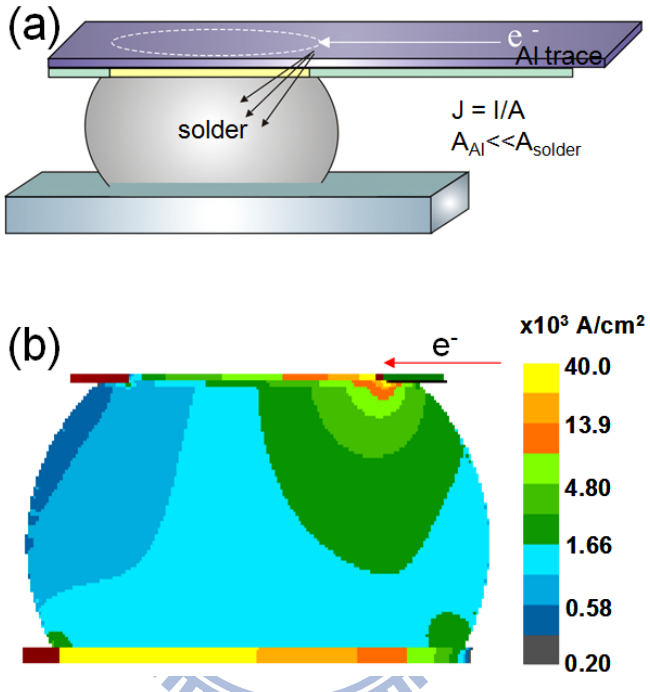


Figure 1-3: (a) Unique line-to-bump geometry of a flip-chip solder bump joining an interconnect line on the chip side (top) and a conducting trace on the board side (bottom). (b) Two-dimensional (2D) simulation of current distribution in a solder joint. [14,15]

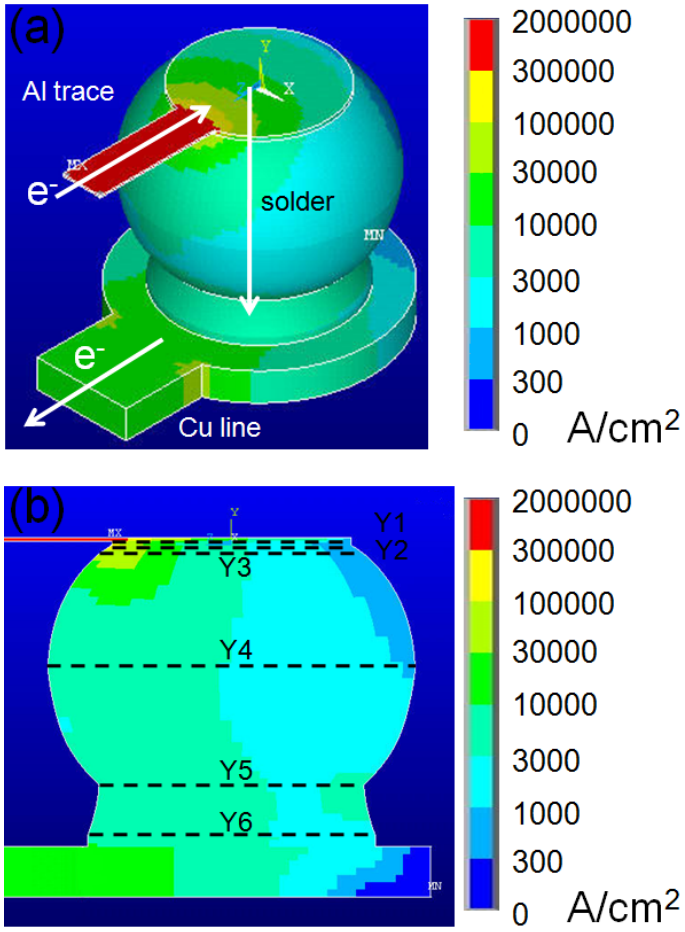


Figure 1-4: (a) 3D current-density distribution in the solder joint with the Ti/Cr–Cu/Cu thin-film UBM. (b) Current-density distribution at the Z-axis cross section in (a). The black dotted lines show the six cross-sections examined in this study. [16,17]

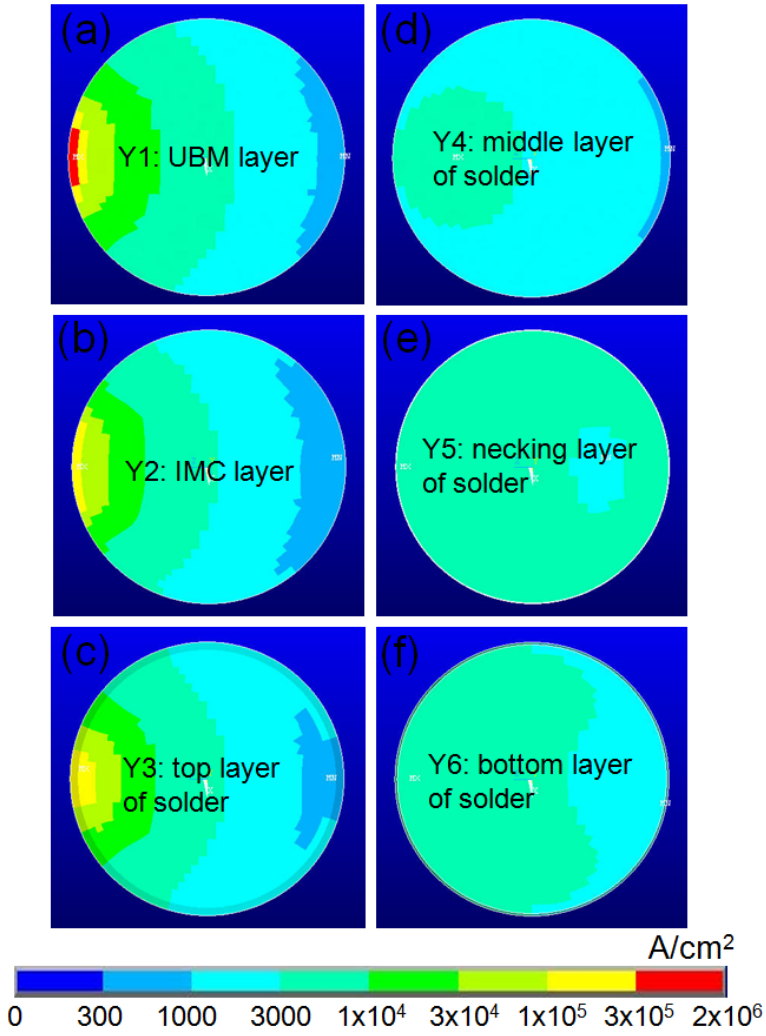


Figure 1-5: The plan-view current-density distribution at different cross-sections: (a) Cross-section Y1, which is located inside UBM. (b) Cross-section Y2, which is IMC layer.(c) Cross-section Y3, which is the top layer of the solder connected to IMC formed between UBM and the solder.(d) Cross-section Y4, which is the largest diameter in the joints. (e) Cross-section Y5, which is a smaller diameter due to solder mask process. (f) Cross-section Y6, which is situated at the bottom of the solder joint. [16,17]

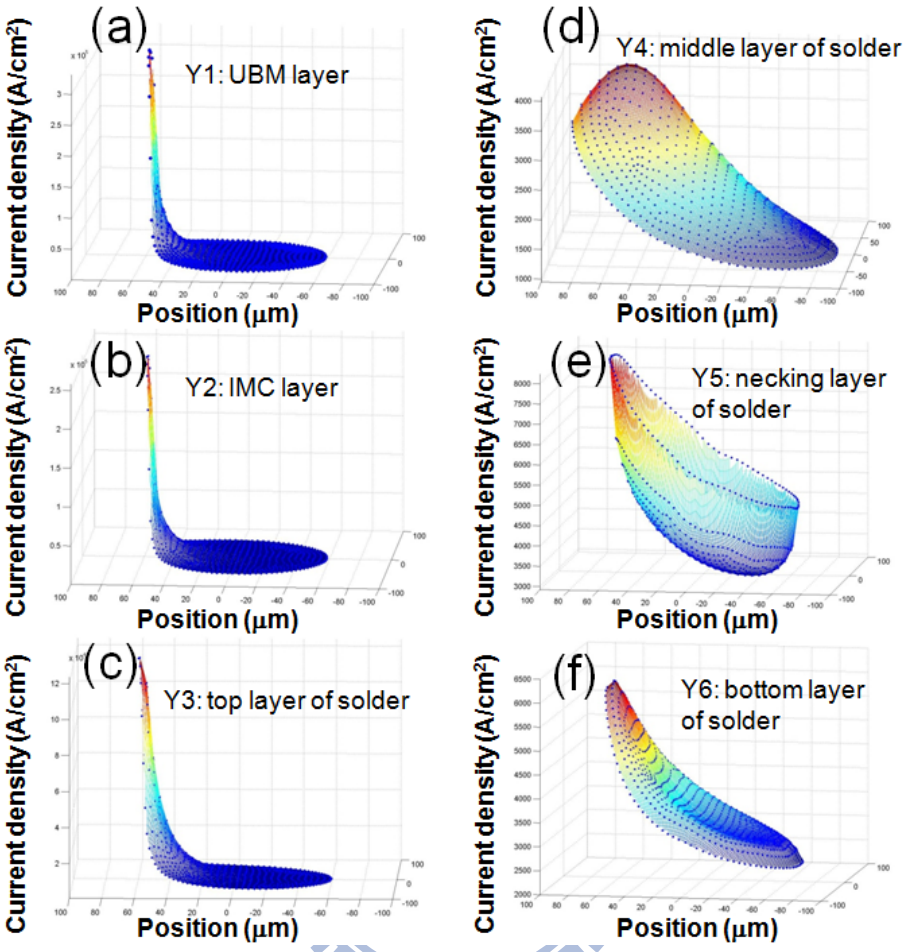


Figure 1-6: The three-dimensional current-density distribution at the different cross-sections: (a) Cross-section Y1, which is located inside the UBM. (b) Cross-section Y2, which is the IMC layer.(c) Cross-section Y3, which is the top layer of the solder connected to the IMC formed between the UBM and the solder.(d) Cross-section Y4, which has the largest diameter in the joints. (e) Cross-section Y5, which has a smaller diameter due to solder mask process. (f) Cross-section Y6, which is situated at the bottom of the solder joint. [16,17]

1.3.2 Joule heating effect

When the current flow pass through a conductor, heat is generated due to the electrons colliding the atoms in the conductor. This is so called Joule heating effect. The heating power can be describe as:

$$P = I^2 R = j^2 \rho V \tag{1.4}$$

where P is the heating power, I is the applied current, R is the resistance of the conductor, j is the current density, r is the resistivity of the conductor, and V is the volume of the conductor. Thus, the heating is influenced by two factors: the applied current and the resistance of the conductor.

When the flip-chip solder joints are applied with high currents, a lot of heat generates. Furthermore, the total length of Al trace is typically about few hundreds to few thousands micrometers, which corresponds to a resistance of approximately few ohms. In contrast, the resistances of the solder bumps and the Cu trace in the substrate are relatively low, typically in the order of few or tens of milliohms. Therefore, the primary contributor for Joule heating in the solder joints is Al trace [18-20]. Al trace is the main heating source. As a result, the temperature in the bumps during accelerated testing is likely to be much higher than that of the ambient because of the Joule heating. Moreover, the current crowding effect leads to the local high current density, and therefore there is induced local Joule heating in the solder joints. The

temperature distribution becomes non-uniform in the flip-chip solder joints. Also, Chiu *et al* reported the "hot spot" exists in the solder bumps at the crowding region [20, 21]. The combination of the Joule heating of Al interconnects on the chip side and the non-uniform current distribution will lead to a temperature gradient across the solder joints. Consequently, Joule heating effect induced the increasing in temperature in the flip-chip solder joints under EM significantly affects the analysis of failure time (see Section 1.3.4).

1.3.3 Void formation and propagation

Voids formation and propagation at the cathode end is the typical EM failure mode of electromigration in flip-chip solder joints. For flip-chip solder joints with a thin film UBM, the current crowding effect leads to a pancake-type of void formation near the entrance point of the current flow and the void propagates along the interface of intermetallic compound (IMC) and solder [13, 14, 22-29]. Figure 1-7 (a) displays the SEM images of eutectic SnPb after EM [13, 14]. After stressing at 125 °C / 2.25 × 10^4 A/cm^2 for 40 h, voids formed in the upper left-hand corner since electron flow entered the bump from the left-upper corner of the joint. Similar phenomena were also observed in Sn-4.0Ag-0.5 Cu Pb-free solder joints as shown in Figure 1-7 (b) [24]. Pancake-type void is clearly seen at the corner of flip-chip solder joints when the cathode is on the chip side. With current stressing time increased, pancake-type voids

propagate across the top of solder joints, resulted in open failure. Later, the re-distribution of current density and temperature due to void formation and propagation will be discussed.

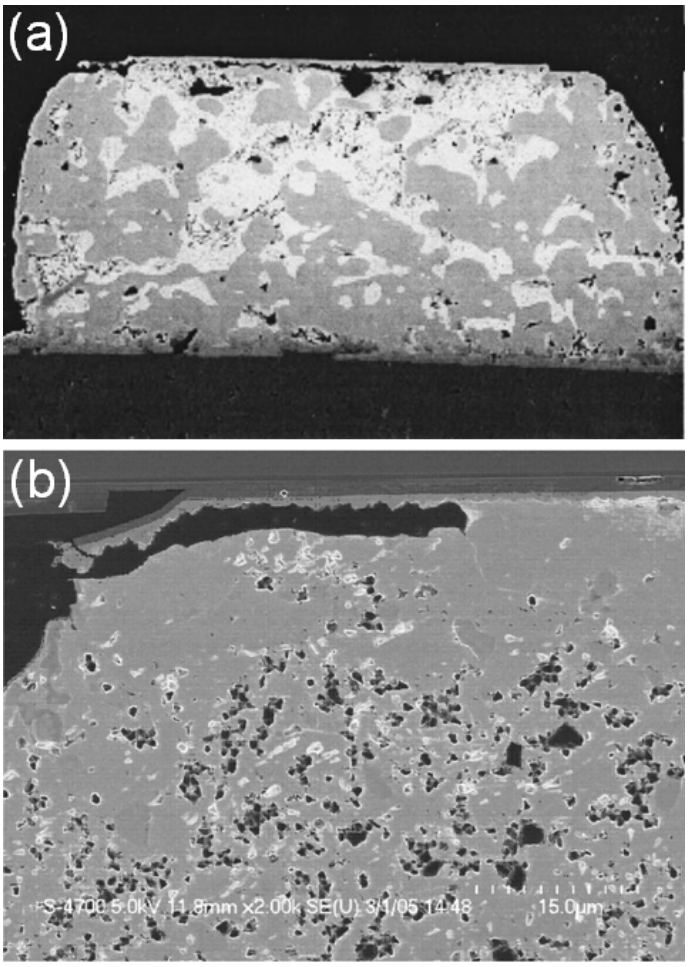


Figure 1-7: (a) SEM images of a sequence of void formation and propagation in a flip-chip eutectic SnPb solder bump stressed on 125 °C at 2.25 × 10^4 A/cm^2 for 40 h. (b) SEM image of void formation in flip-chip 95.5Sn-4.0Ag-0.5Cu solder bump on 146 °C at 3.67 × 10^3 A/cm^2. [24]

1.3.4 Mean-Time-To-Failure (MTTF)

For EM to occur, a non-vanishing divergence of atomic flux is a requirement. Since electromigration damage is cumulative, it affects the failure rate. In statistic study, the test samples should be stressed at the same current and temperature conditions. Then, the failure time or lifetime can be recorded and plot by Weibull or normal distribution. In Weibull distribution, 63.2% of the time of unreliability is denoted as the MTTF [30]. In 1969, J. R. Black explained the MTTF in the presence of EM which was given by the equation [31]:

$$MTTF = A\frac{1}{J^n}\exp\left(\frac{Ea}{kT}\right) \tag{1.5}$$

where A is a constant, J is current density, n is a model parameter, Ea is activation energy, k is Boltzmann's constant, and T is average temperature. There are four parameters, j, n, Ea, and T. All of them need to be examined and analyzed. However, current crowding effect and Joule heating effect in the flip-chip solder joints play important roles under EM. To include these effects in MTTF analysis, Black's equation needs to be modified by multiplying J with a crowding ratio c and add T as an increment of ΔT due to Joule heating [15]:

$$MTTF = A\frac{1}{(cJ)^n}\exp\left[\frac{Ea}{k(T+\Delta T)}\right] \tag{1.6}$$

For the following discussion, the estimated MTTF will be a key result to compare with each other.

1.4 Thermomigration

Thermomigration is defined as a flow of mass driven by a temperature gradient [8,32]. In most metallurgical process, when we anneal an inhomogeneous binary alloy in a furnace at a constant temperature and constant pressure, the alloy tends to become homogenous. On the other hand, if we anneal a homogeneous binary alloy under a temperature gradient, i.e., if one end of it is hotter than the other end, the homogeneous alloy will become inhomogeneous. This phenomenon is named Soret effect or thermomigration, which explains the uphill diffusion for one element and downhill diffusion for another element in a solid solution after being exposed to a temperature gradient. Thermomigration can occur in a pure metal or binary eutectic alloy. For example, Soret effect has been reported to occur in a solid solution of PbIn alloy [33, 34].

When a temperature gradient is established, energy and momentum of the electrons at high temperature side is greater than that at low temperature side. The gradient in the momentum exchange produces a driving force for relative movement of the components [35]. In addition, concentration of equilibrium should also be considered in thermomigration. Since a temperature gradient exists, the concentration of equilibrium at high temperature is higher than that at low temperature side. Thus, this concentration gradient of vacancy will also produce a driving force for relative

movement of the component. Here, the driving force exerted by the temperature gradient can be expressed as

$$F = \frac{Q^*}{T}\frac{dT}{dx} \tag{1.7}$$

where Q* is defined as heat of transport, which is different between heat carried by a moving atom per mole to the heat of atoms per mole at the hot end and T is temperature [36]. Q* can be positive or negative, depends on the direction of component movement. Q* is the positive sign when the flux is from cold to hot region, which means the component gains heat. Q* stand for negative when the component is from hot to cold region. The flux equation of thermomigration is given as

$$J = C\frac{D}{kT}\frac{\left(Q^*/N\right)}{T}\left(-\frac{\partial T}{\partial x}\right) \tag{1.8}$$

where C is concentration, D is diffusivity, N is Avogadro number, and kT is thermal energy. It is worth mentioning that D is the isothermal diffusion coefficient. The jump mechanism or mean jump frequency is not change by the temperature gradient at any temperature. However, it biases the direction of jumps.

Thermomigration of flip chip solder joints under current stressing was first reported by Ye *et al.* [18]. According to their results, several voids were found on these two bumps near the Si chip side. Voids formation on one bump was more serious than that on another bump, as shown in Figure 1-8. EM alone can not explain this phenomenon because EM has a polarity effect. The solder joints with different

current direction would not have void formation near the chip side at the same time. Therefore, thermomigration combined with EM occurred in this pair of solder bumps, as further proved by the marker movement. In Figure 1-9, three-dimensional thermo-electrical finite elements simulation model was used to simulate the temperature distribution from the surface of chip side to the bottom of the solder joints. Their results indicate that a linear temperature gradient of 1500 °C/cm is predicted. This linear temperature gradient of 1500 °C/cm seems sufficient to cause thermomigration in eutectic SnPb solder joints.

Later, thermomigration in SnPb composite flip-chip solder joints at an ambient temperature of 150 °C was observed [37,38]. Figure 1-10 shows the SEM images of composite solder joints before and after thermomigration. The redistribution of Sn and Pb occurs due to a temperature gradient with Sn atoms moved to hot end and Pb atoms moved to cold end. From our previous research [37, 38], we performed the analysis of phase separation mechanism to estimate the driving force of thermomigration assumed 10 °C difference across a solder joint of 100 μm. That means a linear temperature gradient of 1000 °C/cm will induce thermomigration in the solder joints.

From studies above, they assumed that the thermal gradient in the solder joints is linear distribution. However, non-uniform temperature distribution in the solder joints

was found by Chiu *et al.* [20]. More detail studies should be done on this part to confirm the distribution of the thermal gradient. Since there exists the non-linear thermal gradient exists in the solder bumps, it will impact the analysis of the study of thermomigration.

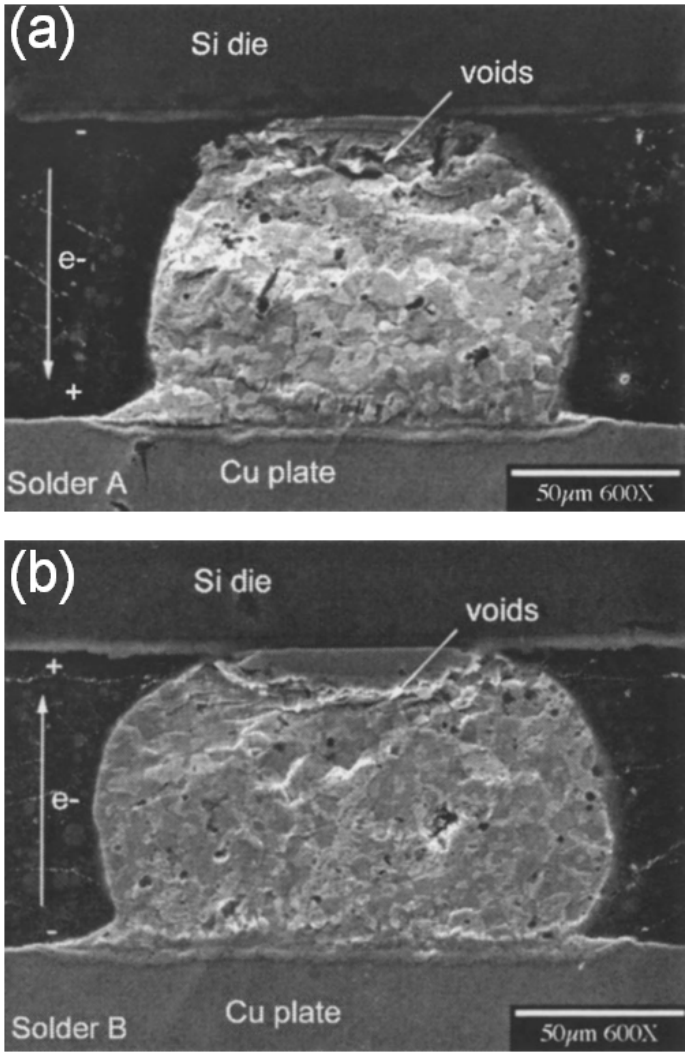


Figure 1-8: The formation of voids on the chip side and accumulation of solder on the substrate side for the solder bump with. (a) Downward electron flow. (b) Upward electron flow. [18]

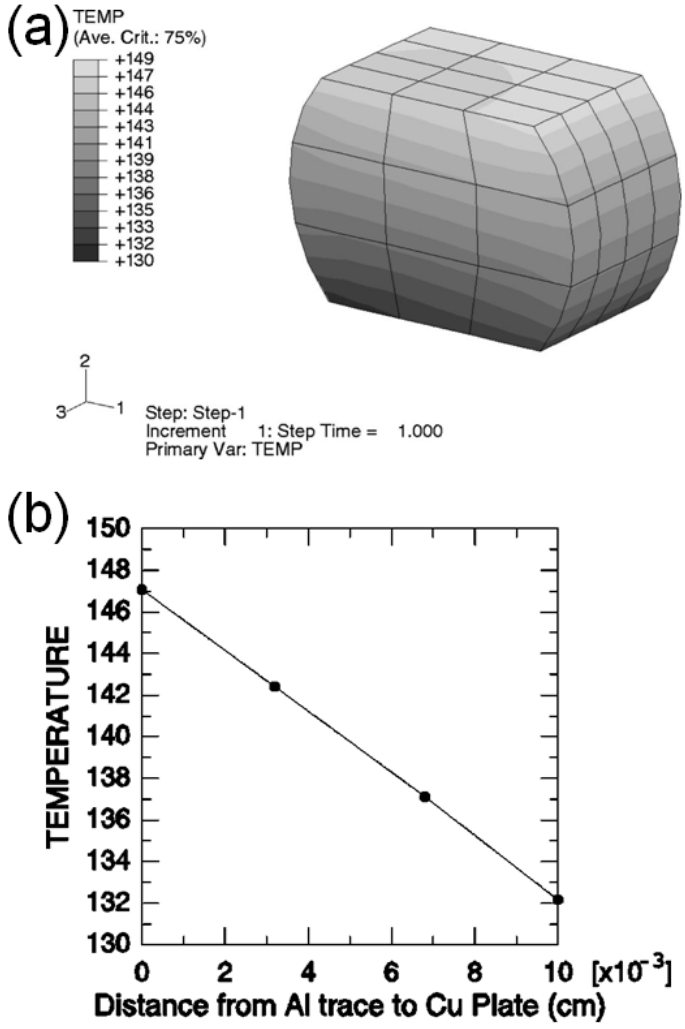


Figure 1-9: (a) Temperature distribution on the solder bump. (b) Temperature distribution along the vertical line across the solder bump. [18]

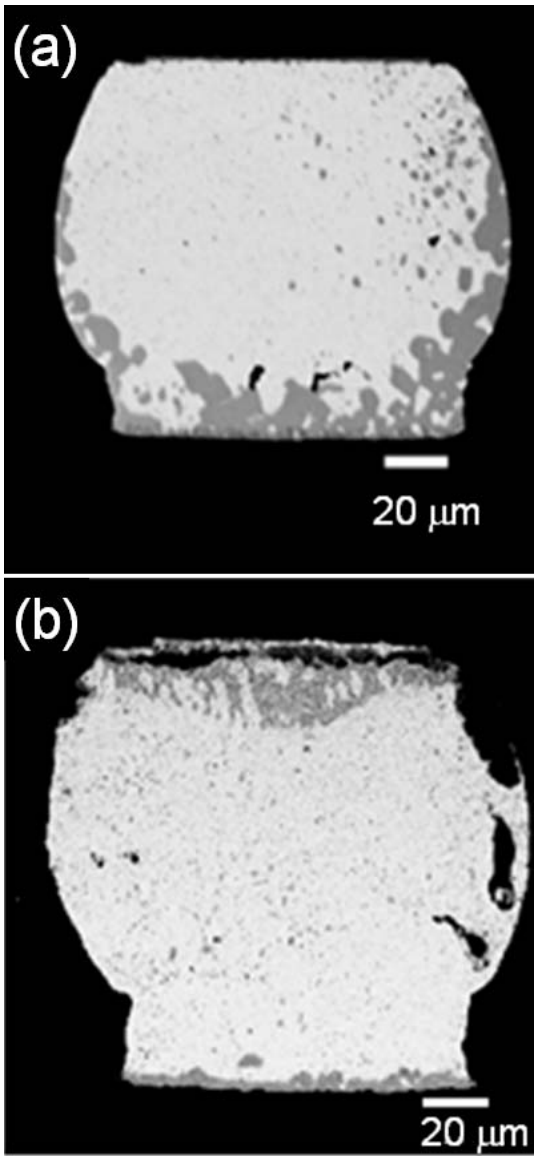


Figure 1-10: SEM image of composite flip-chip solder bump. (a) As prepared. (b) After thermomigration. The Sn-rich phase moved to the chip side. [37,38]

1.5 Motivations

The current that each solder bump needs to carry continually increases. In addition, the miniaturization trend in portable microelectronic products drives the shrinkage of the dimension of solder bumps, which caused in a dramatic increase of current density in solder joints. Therefore, EM has become an important reliability issue of flip-chip solder joints.

The two key issues in flip-chip solder joints under EM are the current density and the temperature distributions inside the solder bumps. However, they are hard to measure directly. In the study, the three-dimensional finite elements method is adopted to analysis the thermo-electrical characteristics in the solder joints. Also, the experiment was performed to confirm the simulation results. The experimental results of thermo-electrical characterization on the EM of the solder joints include the observation of current crowding phenomena by marker movement, the bump resistance by the design of Kelvin probe, the effect of the width of Al trace on MTTF, the effect of Al trace degradation on Joule heating, and non-linear distribution of thermal gradient. In addition, the current density and temperature re-distribution due to void formation and propagation will be discussed. Moreover, by simulation, the prediction to enhance EM resistance, i.e. relieving the current crowding effect and Joule heating effect in the solder joints, is able to be through with by controlling the

UBM materials, solder alloys, Al-trace design, UBM thickness, and size of contact opening. Finally, the shrinkage of solder bump size and die thickness are investigated since the 3D IC packaging becomes more and more important for next packaging generation.

Chapter 2 Experimental procedure

2.1 Sample preparation

Three kinds of flip-chip samples were used in the EM test in this study. The samples prepared by typical bumping process including photolithography, Cu and solder electroplating, flip-chip reflow process and etc. First, the solder joints were eutectic SnPb solder with a tri-layer 0.1 μm Ti / 0.3 μm Cr-Cu/ 0.7 μm Cu UBM provided by APack [39] as illustrated in Figure 2-1 (a). The SEM image of solder joints from APack as prepared is shown in Figure 2-1 (b). Passivation and UBM openings were 85 and 120 μm in diameter respectively. Al trace on the chip side was 34 μm wide and 1.5 μm thick. Cu line on the BT substrate was 80 μm wide and 25 μm thick. The height and pitch of the bump are 145 and 400 μm, respectively. Dimension of Si chip was 7.0 × 4.8 mm^2 and the thickness was 290 μm, whereas the dimension of BT substrate was 5.4 mm wide, 9.0 mm long and 480 μm thick. Second, Lead-free SnAg3.5 solder joints were adopted and the UBM is 0.5-μm Ti-Cu/5-μm Cu. This kind of sample is provided by Megic [40]. The schematics and SEM image of the solder joint samples from Megic is shown in Figures 2-2 (a) and (b), respectively. The 0.5-μm Ti-Cu was sputtered as a Cu seed layer, and then a 5-μm Cu layer was electroplated. The diameter of the UBM opening was 120 μm. Lead-free SnAg3.5 solder bumps were electroplated and joined to FR5 substrates. The bump

height was about 75 μm. The metallization layer on the FR5 substrate was a 5-μm electroless-Ni. The dimension of the Cu pad opening in the substrate was 300 μm in diameter. Al trace on the chip side was 100 μm or 40 μm wide and 1.5 μm thick. Cu line on BT substrate was 100 μm wide and 25 μm thick. The bump height and pitch are 75 and 800 μm, respectively. Third, the test vehicle employed in the EM study was a flip-chip package, that is a Si chip interconnected to the substrate by an array of Pb-free solder joints. In the drawing Figure 2-3 (a), all these samples are FCBGA flip-chip packages provided by ASE [41]. The pitch between adjacent solder joints is 270 μm. The bump height is about 100 μm. Figure 2-3 (b) is a cross-sectional view of a flip-chip solder joint by SEM image. The UBM on the chip side is a tri-layer thin film of Ti/Ni(V)/Cu. The thickness of the Cu thin film is 0.5 μm. The diameter of UBM opening and passivation opening were 110 and 85 μm, respectively. Printing solder of Sn-0.7Cu alloy was used on the chip side. The substrate metallization on Cu bond-pad features the solder-on-pad (SOP) surface treatment, i.e., with printed Sn-3.0Ag-0.5Cu pre-solder on Cu bond-pad surface. Cu bond-pad has a thickness of 15 μm, which is much thicker than Cu thin film UBM on the chip side. The printing solder and the SOP were reflowed together and became the Pb-free bumps. The stress condition will be described in later chapter.

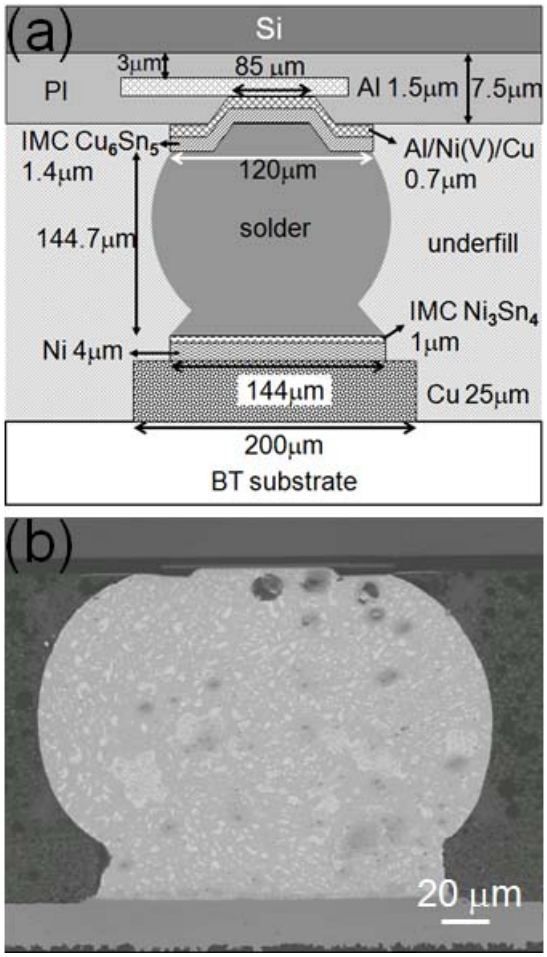


Figure 2-1: (a) The cross-sectional schematic shows the flip-chip solder joints from APack. (b) The cross-sectional SEM image of flip-chip solder joints as prepared by APack.

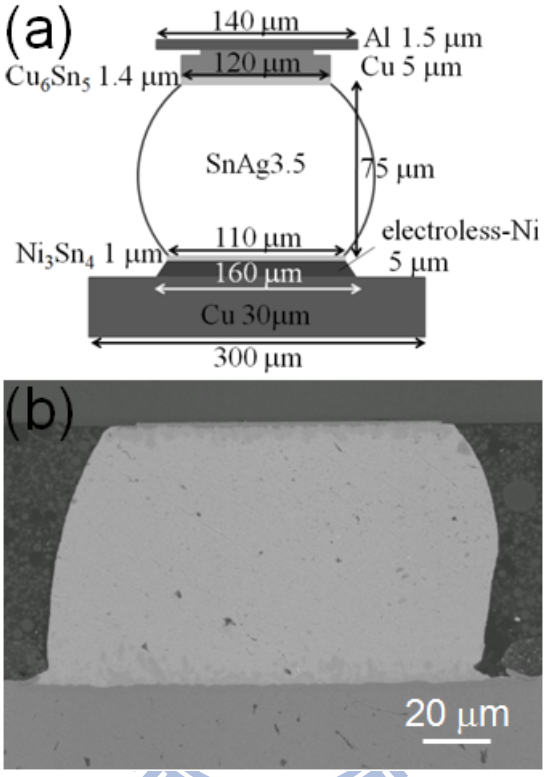


Figure 2-2: (a) The cross-sectional schematic shows the flip-chip solder joints from Megic. (b) The cross-sectional SEM image of flip-chip solder joints as prepared by Megic.

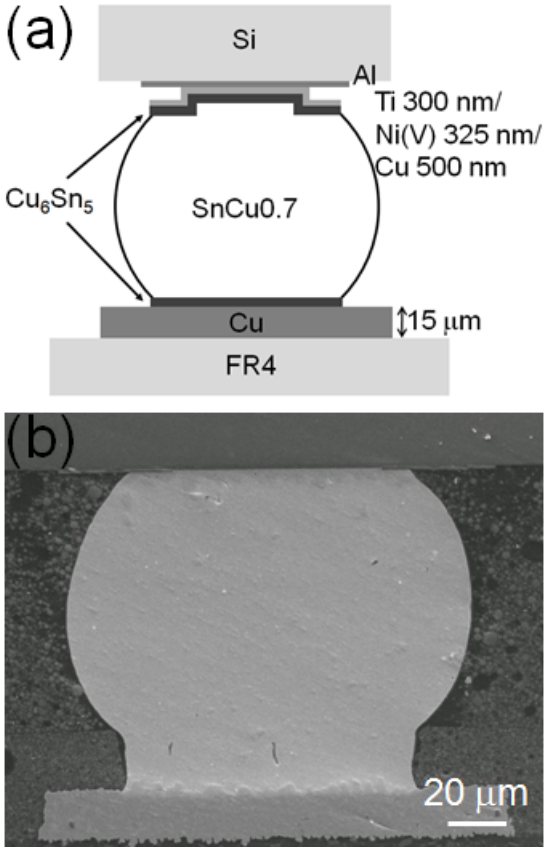


Figure 2-3: (a) The cross-sectional schematic shows the flip-chip solder joints from ASE. (b) The cross-sectional SEM image of flip-chip solder joints as prepared by ASE.

2.2 Automated data acquirement system

In this study, power supply Keithley 2400 [42] and power supply Agilent E3646A [43] are served as the current sources. Data switch Agilent E34970A [43] with three pieces of 20-channels modulus was used to monitor the voltage history. The limitation of the voltage measurement is about 5 μV for the power supply and the data switch. Since the initial EM failure of the flip-chip solder joints may increase several micro-ohm of resistance, this measuring system can provide enough accuracy for our measurement. To fit long time current stressing in EM tests, an in-house controlling software was encoded by LabVIEW [44,45]. Using the software, the stressing current, stressing time and failure criteria can be easily recorded. To link the apparatus and the software, the GPIB card from NI [44] was employed to serve the long time, stable, and precise controller. The measuring system is illustrated in Figure 2-4.

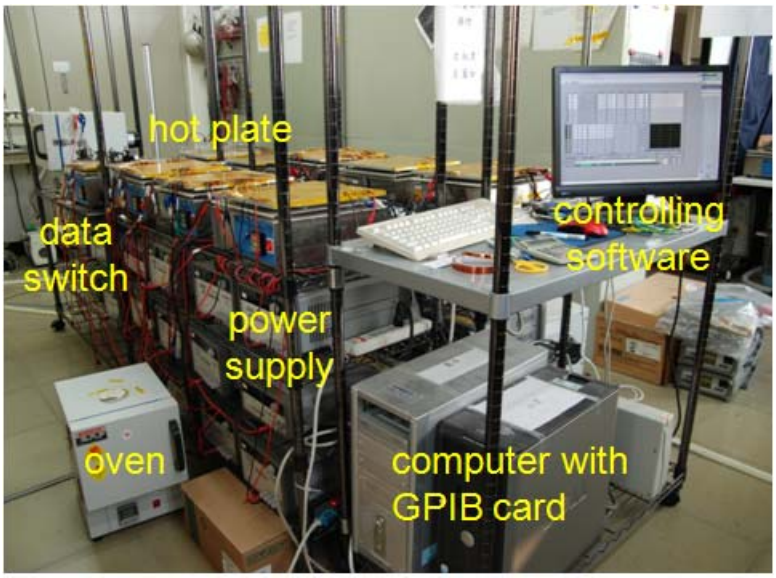


Figure 2-4: The photograph of the automated data auquirment system.

2.3 Microstructure examination

Cross-sectional and whole-bump samples were prepared for the EM test. The cross-sectional samples were first polished to the half solder joints before current stressing. After stressing the whole-bump samples, the samples also need to be ground and polished to certain position. The following apparatus or equipments were used to inspect the morphology and the composition changes of the solder joints.

2.3.1 SEM

In Figure 2-5 (a), JEOL JSM-6500F and JEOL JSM-6700F field-emission scanning electron microscopy (FESEM) were used for the examination of EM damage. The high-voltage electron-beam hits the samples on the stage, and then releases the secondary electrons. By collecting the secondary form the surface of the samples, the secondary electron images (SEI) can be acquired to analysis the surface morphology. On the other hand, backscattered electrons are beam electrons that reflected from the sample by elastic scattering. Backscattered electrons are often used in analytical SEM along with the spectra of characteristic x-rays. Because the intensity of the backscattered electrons signal is strongly related to the atomic number (Z) of the specimen, backscattered electrons images (BEI) can provide information about the distribution of elements in the samples.

2.3.2 Energy dispersive spectroscopy (EDS)

The detector of energy dispersive X-ray spectroscopy (EDS) attached to SEM is adopted to analyze the compositions of the flip-chip solders joints. A detector was used to convert X-ray energy into electrical signals. As the energy of the X-rays is characteristics of the difference in energy between the two shells and of the atomic structure of the element from which they were emitted, this allows the elemental composition of the specimen to be detected.

2.3.3 Focused ion beam (FIB)

Figure 2-5 (b) depicts the dual-beam focused ion beam (DB-FIB) of FEI Nova-200 used for the examination. The FIB can be utilized for precise cutting, selective deposition, selective etching, and TEM samples preparation. In this study, the precise cutting, selective etching, and the ion channeling image were used by FIB. Due to ion channeling effect, the contrast of grain orientation looks different since different grain orientation has different ion channeling. If the orientation is parallel with the ion direction, it looks darker under ion channeling. Otherwise, when the grain orientation against the ion, it looks brighter.

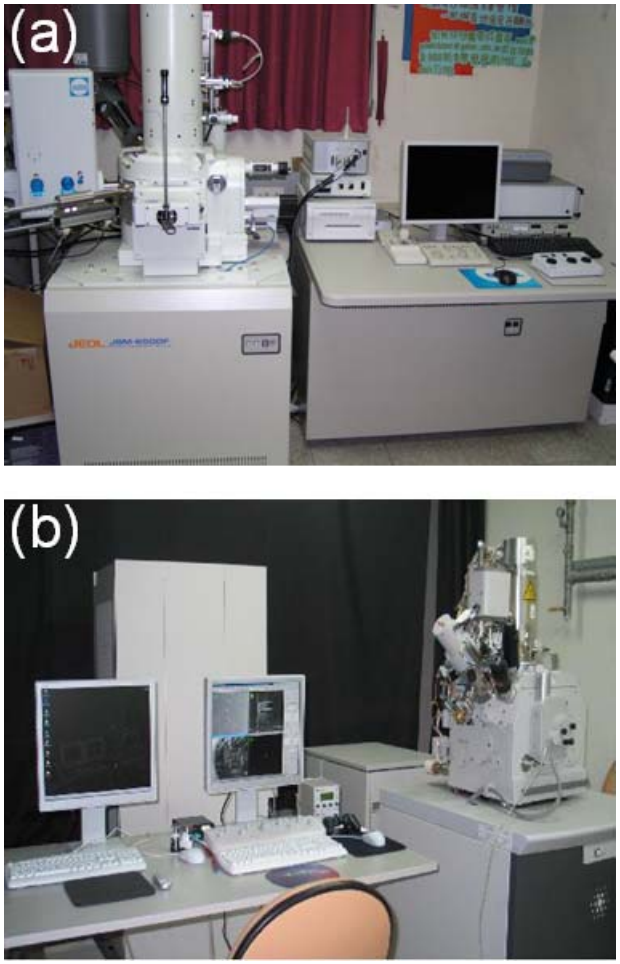


Figure 2-5: The photograph of (a) FESEM. (b)FIB.

2.4 Temperature measurement

Since the Joule heating effect is a major issue in this study, how to measure the accurate temperature distribution is the key problem to be solved. The thermal couple may be used to measure the temperature. However, the contact point of thermal couple is too large to measure the exact temperature in flip-chip solder joints. In this study, the following two methods are employed to obtain the temperature in the flip-chip solder joints without damaging the samples.

2.4.1 Infrared microscopy

An infrared microscope (IR) form Quantum Focus Instrument (QFI) as shown in Figure 2-6 (a) was employed to measure the temperature in the flip-chip solder joints under current stressing [21]. The temperature distribution inside the bumps was detected by a thermal infrared microscope, which the resolution of 0.1 °C in temperature sensitivity and 2.8 μm in spatial resolution per pixel. Before the current stressing, the emissivity of the specimen was calibrated at 100 °C. After the calibration, the bumps were stressed by a desired current condition. Then, temperature measurement was performed to record the temperature distribution after the temperature reached a steady state. Figure 2-6 (b) shows the schematic diagram for experimental setup, in which the Si side faces the infrared microscope. Since the 250 μm Si is transparent to infrared, the corresponding penetration depth is larger than 2

m and much larger than the thickness of the Si wafer. Therefore, the absorption of Si chip can be ignored [46]. Another purpose to use IR is it can be used to detect the materials distribution by the radiance mode. The radiance of a metal is smaller than that of a ploymer. Thus, the metal appears brighter in the image.

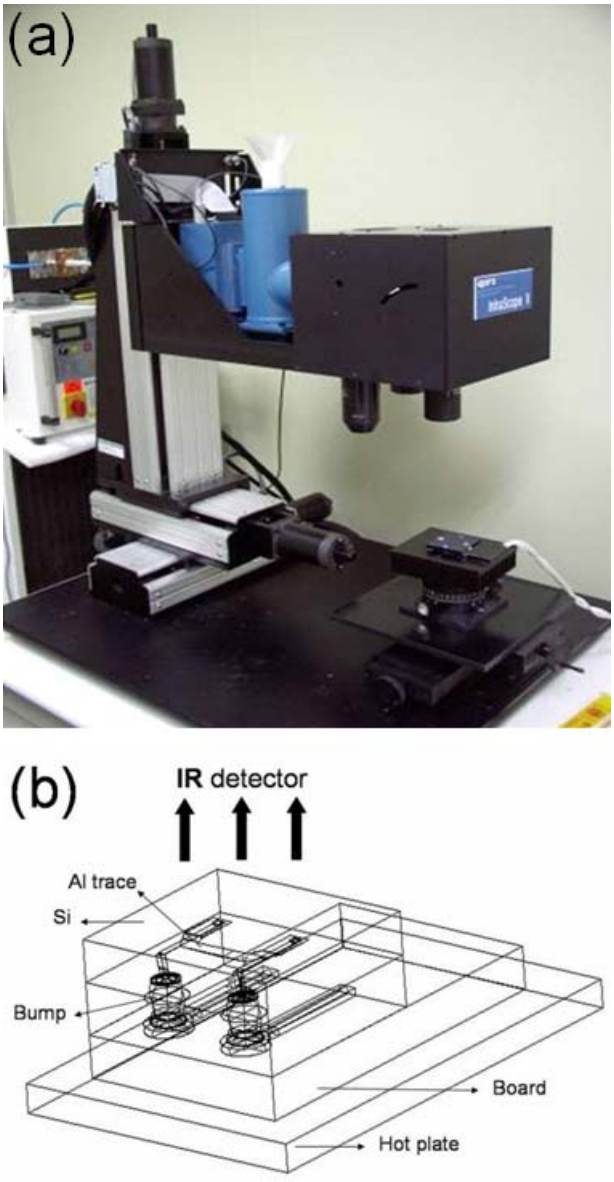


Figure 2-6: (a) The photograph of the IR microscope. (b) The schematic diagram for experimental setup during IR measurement.

2.4.2 Thermal sensors by TCR effect of Al lines

The temperature coefficient of resistance (TCR) is a physical property of metals. Since the electrical resistance of a metal conductor such as a copper wire is dependent upon collision processes within the wire, the resistivity could be expected to increase with temperature since there will be more collisions. An intuitive approach to temperature dependence leads one to expect a fractional change in resistance which is proportional to the temperature change:

$$R = R_o\left[1 + \alpha\left(T - T_o\right)\right] \tag{2.1}$$

where R is the resistance at temperature of interest, R_o was the reference resistance, α is the temperature coefficient of resistance, T is the temperature of interest, and T_o is the reference temperature.

To explore the TCR effect, the layout in Figure 2-7 is designed as a thermal sensor in the flip-chip solder joints. For the TCR calibration, the applied current was 0.2 A through pad 1 to pad 2 in the oven. The voltage drop was monitored through pad 3 and pad 4. Thus, the measured resistance included the resistance of bump 3 and bump 4, some Cu lines, as well as the resistance of the Al trace connecting bump 3 and bump 4. To calibrate the TCR, the resistance was measured in an oven in which the temperature was from 50 to 175 °C. After calibration, the exact bump temperature can be estimated when resistance with a desired current on the hotplate is acquired.

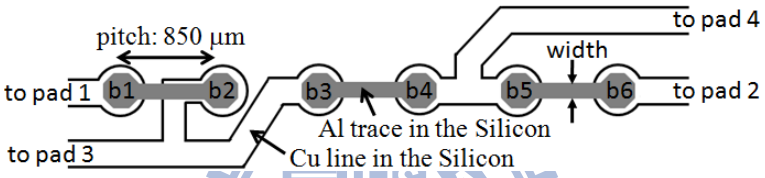


Figure 2-7: Plan-view schematics show the daisy-chain layout for the solder joints served as a thermal sensor.

Chapter 3 Simulation

3.1 Finite-elements method

As the functions and the speed of a computer calculating become better and better, the computer-aided engineering, as known as CAE, has been performed to supply the engineers some important information technology of analysis, design, manufacture, planning, etc. Not only industry but also academia, CAE began played an important role due to its powerful technology on analysis and designing.

In this study, the ANSYS [47] software was used to obtain the thermo-electric simulation in flip-chip solder joints. ANSYS adopts as the finite-elements method (FEM) for the thermal, electrical, stress and the coupling analysis. For the FEM, the model needs to be meshed to form a lot of nodes and elements. By the certain type of elements, the equations in the elements are use to solve the analysis. Next sections present the process of the simulation by ANSYS software individually.

3.2 Simulation process

By using the ANSYS software which was developed by ANSYS Inc., the thermo-electric simulation can be conducted to calculate the current density and temperature distribution in flip-chip solder joints. The simulation processes by ANSYS software include three parts: preprocess, solution and postprocess. In the first part, element type was selected to solve the thermo-electrical problem. The

three-dimensional models were constructed to set materials. And then, the models need to be meshed. In the second part, the boundary conditions are applied to solve the equations. Finally, the results came out in the postprocess.

3.2.1 Element type

The element type of SOLID69 was used in the simulation model. It was suitable for the 8-node hexahedral and 6-node prism, and 4-node tetragonal thermo-electrical coupling elements as shows in Figure 3-1. This element type is very useful for mixed meshization process. Due to the SOLID69, the physically calculations included heat generations, thermal gradient, thermal flux, electric fields, current density, Joule heating generation per unit volume, temperature, heat flow, etc.

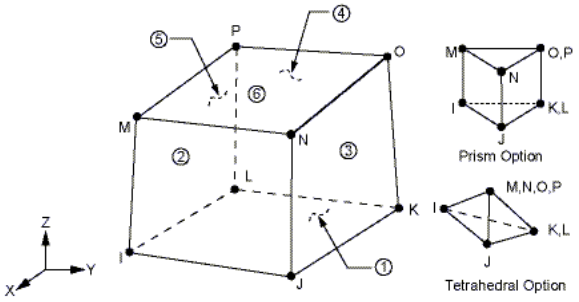


Figure 3-1: SOLID69 Geometry

3.2.2 Materials properties

In the thermo-electrical coupling simulation, the material properties include resistivity, conductivity, temperature coefficient of resistivity of materials. The temperature coefficient of resistivity is especially the linking property for the coupling calculation. Relevant material characteristics of materials in this study are listed in the Table 3-1. However, the thermal conductivity of the electroless Ni could not be found in the literature. The following equation was used to estimate the thermal conductivity [48].

$$\frac{\kappa}{\sigma}\frac{1}{T} = 3\left(\frac{k}{e}\right)^2 \tag{3.1}$$

where κ is thermal conductivity, σ is conductivity, T means temperature, k and e are the Boltzmann constant and electron charge, respectively. When the resistivity of electroless Ni with 10% P is 70 μΩ-cm, the thermal conductivity is estimated to be 9.3 W/m-K by this equation.

Table 3-1: The materials properties used in this study.

Materials	Thermal conductivity (W/m・K)	Resistivity (μΩ・cm)	Temperature coefficient of resistivity (TCR) (K^{-1})
Al	238	2.7	4.2×10^{-3}
Al/Ni(V)Cu	166.6	29.54	5.6×10^{-3}
Cu	403	1.7	4.3×10^{-3}
Ni	76	6.8	6.8×10^{-3}
electroless Ni	9.3	70	6.8×10^{-3}
Pb-5Sn	63	19	4.2×10^{-3}
e-SnPb	50	14.6	4.4×10^{-3}
SnAg3.5	33	12.3	4.6×10^{-3}
Cu_6Sn_5	34.1	17.5	4.5×10^{-3}
Ni_3Sn_4	19.6	28.5	5.5×10^{-3}
Si	147	--	--
BT	0.7	--	--
Underfill	0.55	--	--
PI	0.34	--	--

Note: The materials not given in electric resistivity are assumed to be electrical insulators.

3.2.3 Model construction

Two standard construction methods have been well known as following:

1. Top-down method:

   The creation is starting from the keypoints. The coordination of keypoints needs to be confirmed by the model first. Then use two or more keypoints creates lines. By at least four lines, the areas can be constructed. Since the areas existed, the volumes can be done by areas collection. Brief speaking, top-down method creates models from low dimension to high dimension.

2. Bottom-up method:

   The models create all kinds of volumes first and use Booleans operation to add, subtract, or divide each other to form the models. The models come from high dimension to low dimension.

However, the packaging model of the flip-chip solder joints is very complex. The model construction should use the combination of these methods. In Figure 3-2, the construction process is as following flowchart:

1. Create two dimensional (2D) area of half cross-section of the solder joints.
2. Rotate 360° of the area by the axis.
3. Copy the solder joints.
4. Create Al traces and Cu lines.

5. Create dummy solder joints.

6. Create underfill, passivation, Si die and substrate.

7. Glue the whole package.

8. Set the material properties of the whole package.

9. Mesh the whole model.

In order to overcome the difficulties that may occur during meshing, layered-type both Cu_6Sn_5 and Ni_3Sn_4 IMCs, dummy solder bumps, and shorten Cu lines were used in the model construction.

In addition, three kinds of pattern of Al trace were discussed as illustrated in Figures 3-3 (a) to (c). Al trace of Pattern 1 has two layer layout of Al trace. Al trace of Pattern 2 has one Al trace to connect the two solder bumps. Al trace of Pattern 3 has two segment of Al trace to connect the three solder bumps. In the simulation model of the flip-chip solder joints, the mapped-mesh, which means the hexahedral elements, was provided to cover the whole bump. But the surrounding model was adopted with the free-mesh, which means the tetragonal elements. The solder joints with ball shape are going to be stressed by current, this is so called real solder area. This area of three patterns of Al trace has been well meshed as shown in Figures 3-3 (d) to (f).

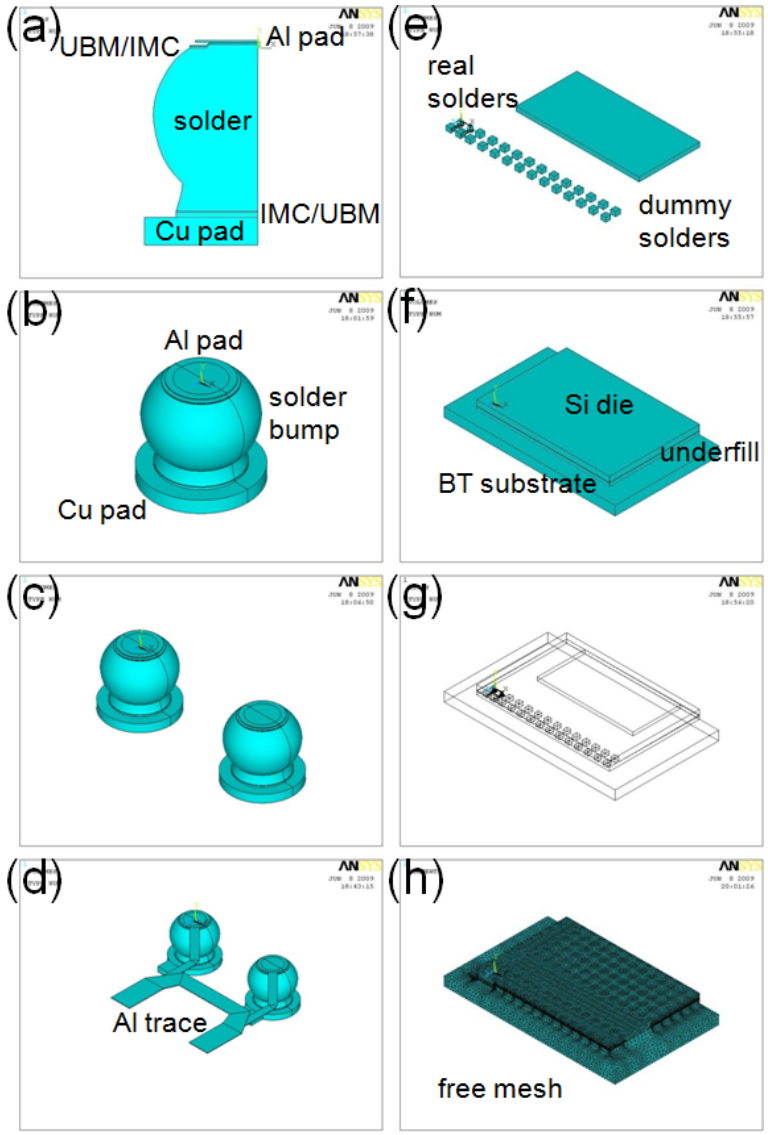


Figure 3-2: (a) Create 2D area of half cross-section of solder joints. (b) Rotate 360° of the area by the axis. (c) Copy the solder joints. (d) Create Al traces and Cu lines. (e) Create dummy solder joints. (f) Create underfill, passivation, Si die, and substrate. (g) A perspective drawing of the whole simulation model. (h) Mesh the whole model.

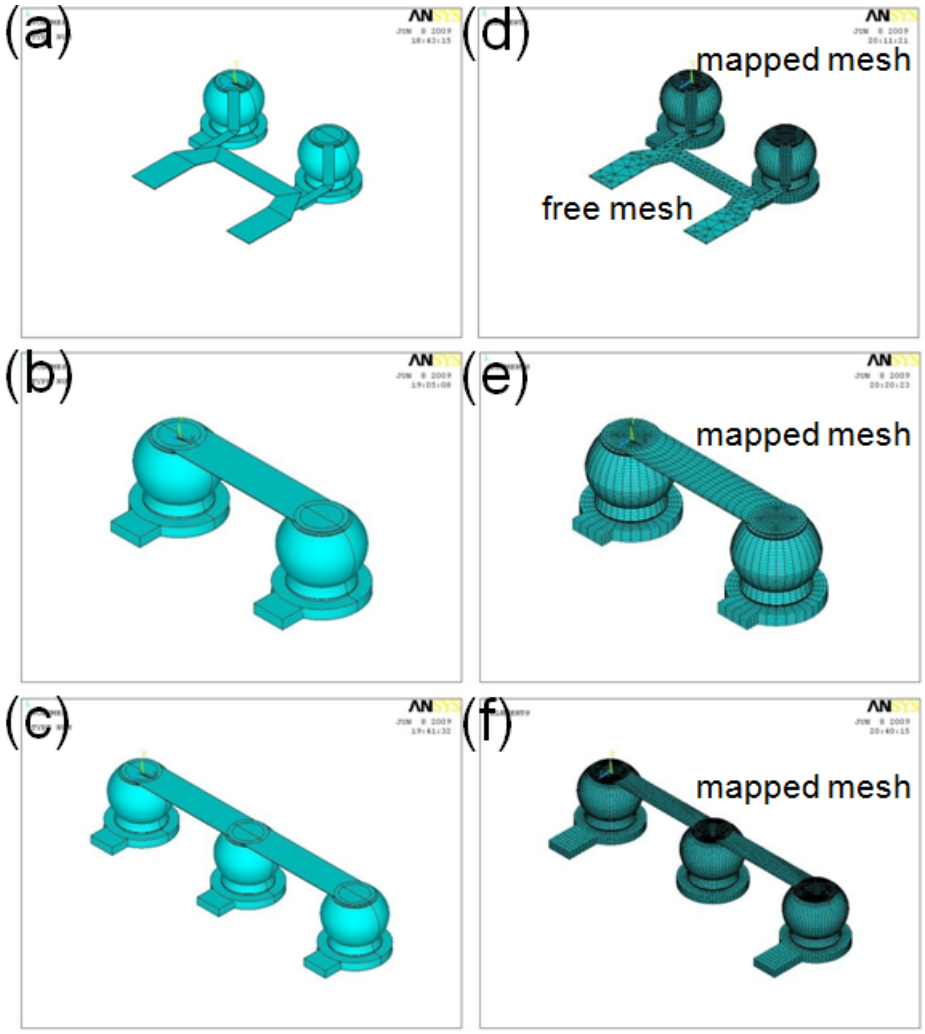


Figure 3-3: (a) The simulation model of solder joints with Al trace of Pattern 1. (b) The simulation model of solder joints with Al trace of Pattern 2. (c) The simulation model of solder joints with Al trace of Pattern 3. (d) The corresponding meshization of Pattern 1. (e) The corresponding meshization of Pattern 2. (f) The corresponding meshization of Pattern 3.

3.2.4 Excitation load and boundary conditions

For the electrical boundary conditions, a constant current was applied through the left-hand side of Cu line in the substrate side. The voltage at the right-hand side of Cu end was set to be zero. The stressing currents ranged from 0.1 A to 0.6 A. For the thermal boundary conditions, the BT substrate kept at 100 °C. Moreover, the convection parameter was in natural convection condition, whose heat convection coefficient in the air is usually between 5 W/m^2-°C and 15 W/m^2-°C. The ambient temperature and convection coefficient were taken as 25 °C and 10 W/ m^2-°C.

Actually, the condition modification needs to adopt the above boundary. First, the flip-chip solder joints are prepared, then use IR microscope to measure the temperature in Al trace. Then construct 3-D model and set material properties and boundary conditions, then the current and temperature distribution in the solder joints can be obtained. By comparing the simulation results to the experimental results, the material properties and boundary conditions can be adjusted to match the experimental results. Then the current density and temperature distributions in the solder joints are able to be analyzed.

3.2.5 Solutions

Since the models have been created and meshed and the boundary conditions have been set, the simulation will be solved by the built-in solver. After certain

running time, the solutions will come out. Then the results are able to be acquired.

3.2.6 Postprocess

In the final step of the simulation, the postprocessor is going to be used to save the contour pictures of current density and temperature distribution. Also, the lists of the results can be received and then use other software, like MATLAB [49], to make transform action and get more simulation information.

3.3 Basic equations

In the finite-elements method, the basic equations have been built in the element type. In this section, the basic equations of electric conduction and heat transfer are going to be discussed since this study is focused on the thermo-electrical simulation.

3.3.1 Electrical conduction

Electrical conduction is the movement of electrically charged particles through a transmission medium (electrical conductor). The movement of charge constitutes an electric current. The charge transport may result as a response to an electric field or as a result of a concentration gradient in carrier density. In electromagnetism, Maxwell's equations are a set of four partial different equations that describe the properties of the electric and magnetic fields and relate them to their sources, charge density and current density. So, the Maxwell’s equations in terms of free charge and current by different form are described as:

$$\nabla \times \{H\} = \{J\} + \{\frac{\partial D}{\partial t}\} \tag{3.2}$$

$$\nabla \times \{E\} = -\{\frac{\partial B}{\partial t}\} \tag{3.3}$$

$$\nabla \bullet \{B\} = 0 \tag{3.4}$$

$$\nabla \bullet \{E\} = \rho \tag{3.5}$$

where {H} is magnetizing field, {J} is current density, {D} is electric displacement field, {B} is magnetic field, t is time, and ρ is charge density. These equations show the theory of the electromagnetism.

But in simulation calculation, Kirchhoff's circuit laws are two equalities that deal with the conservation of charge and energy in electrical circuits, and were first described in 1845 by G. Kirchhoff [50]. First, Kirchhoff's current law (KCL) is based on the conservation of charge whereby the charge is the product of the current and the time. Second, Kirchhoff's voltage law (KVL) is based on the conservation of energy whereby voltage is defined as the energy per unit charge. The total amount of energy gained per unit charge must equal the amount of energy lost per unit charge. This seems to be true as the conservation of energy states that energy cannot be created or destroyed; it can only be transformed into one form to another.

3.3.2 Heat conduction

Heat transfer is the transition of thermal energy or simply heat from a hotter object to a cooler object. There are three methods to transfer the heat: conduction,

convention and radiation [51].

Conduction is the transfer of heat by direct contact of particles of matter. The differential form of Fourier's Law can be used to explain thermal conduction of heat flux:

$$q = -k\frac{dT}{dx} \tag{3.6}$$

where q is heat flux, k is material's conductivity, T is temperature, x is distance, thus, dT/dx means thermal gradient.

3.3.3 Heat convection

Convection is the transfer of heat energy between a solid surface and the nearby liquid or gas in motion. As fluid motion goes faster, the convective heat transfer increases. The presence of bulk motion of fluid enhances the heat transfer between the solid surface and the fluid. The formula for Rate of Convective Heat Transfer can be described [52]:

$$q = hA(T_s - T_b) \tag{3.7}$$

where q is heat flux, h is heat transfer coefficient, A is surface area of transferred heat, T_s is surface temperature, and T_b is temperature of fluid at bulk temperature.

3.3.4 Heat radiation

Radiation is the transfer of heat energy through empty space. This formula is mathematically written as:

$$q = \sigma \varepsilon_i F_{ij} A_i \left(T_i^4 - T_j^4 \right) \tag{3.8}$$

where q is heat flux, σ is Stefan-Boltzmann constant, ε_i is effective emissivity, F_{ij} is radiation view factors, and A is surface area. However, the heat transferred by radiation only under very high temperature difference. Here, the heat radiation was ignored.

3.3.5 Thermo-electrical coupling field

In the simulation, the thermo-electric was sequential. The field equations for the coupled thermoelectric analysis are:

$$\{Q\} = T[\alpha]\{J\} - [K]\{\nabla T\} \tag{3.9}$$

$$\{J\} = [\sigma]\left(\{E\} - [\alpha]\{\nabla T\}\right) \tag{3.10}$$

where Q is heat flux vector, T is absolute temperature, α is Seebeck matrix, J is electric current density, K is thermal conductivity matrix evaluated at zero current density, ∇T is thermal gradient, σ is electrical conductivity matrix evaluated at zero thermal gradient and E is electric field. By the matrix of field equation, the coupling thermo-electrical finite-elements method can use to solve and calculate the current density and temperature distribution.

Chapter 4 Results and discussion

4.1 Effect of current crowding on maker movement

4.1.1 Results and discussion

As discussed in Chapter I, the effect of current crowding on pancake-type void formation at the cathode and whisker growth at the anode of solder joints has been reported [53-55]. However, the effect of non-uniform distribution of electric current on diffusion in the bulk of the solder bump is unclear. No direct measurement of the rate of EM in the current crowding region vs. that in the rest of the solder bump has been reported. In this section, diffusion makers prepared by FIB were used to measure the non-uniform distribution of diffusion flux in the solder joints during EM. The EM vehicles are provided by ASE. The distribution of movement of markers is found to be indirect proportional to the local current density distribution. Yet atomic flow against electron flow in the low current density region has been observed. The product of DZ*, the diffusivity times the effective charge number, in the current crowding region has been estimated.

The sample was polished approximately to the centers of the solder bumps before electromigration test. To avoid thermomigration during EM tests [56,57], a low current density was used to induce void formation. One pair of the solder joints was applied by 0.6 A on a hotplate maintained at 100 °C. In the very beginning of EM, IR

microscopy was used to measure the temperature distribution in the bump. The temperature distribution is illustrated in Figure 4-1. The bump on the left hand side, denoted as Bump 1, was subjected to the downward electron current stressing. The temperature distribution is quite uniform as shown in Figure 4-1 (a). No clear hot spots were found in the bump. Figure 4-1 (b) shows the temperature profile from Point A to Point B as marked in Figure 4-1 (a). No obvious thermal gradient across the bump was exhibited. According to the result by IR microscopy indicated that no large thermal gradient was created under the current stressing of 0.6 A at 100 °C. Therefore, we conclude that thermomigration did not accompany electromigration in the test.

To correlate qualitatively the current crowding to electromigration flux in the solder joints, marker analysis was used to measure the non-uniform distribution of electromigration flux. Twelve markers were fabricated by FIB and each marker was a square of 1 μm × 1 μm and was 200 nm in depth. The pitch in the marker array was 10 μm. The distance between the marker and the contact interface to the Si die was about 11 μm to 12 μm. Figure 4-2 shows the SEM images of the markers after various stressing time. Figure 4-2 (a) shows the image before current stressing. In EM test, the electron flow was coming from the upper right corner of Figure 4-2 (a). After stressing for 150 h, the formation of IMC near the upper-right corner became clear as

shown in Figure 4-2(b). The flux of tin atoms has moved to the anode side due to EM. After stressing for 300 h, when we compared the markers at the right corner with those at the left corner, the movement of marker No. 10 became clearer, as shown in Figure 4-2 (c). It moved closer to the die. After 1632 h of current stressing, voids formed at cathode end as shown in Figure 4-2 (d). Some IMCs disappeared near the anode entrance of Cu trace on the substrate, and voids formed between IMC and solder on the cathode side.

To obtain the quantitative analysis of current density and marker movement, 3D current density distribution was constructed by finite element method and the marker movement was measured from SEM image. In Figures 4-3 (a) (b), current crowding occurred at the upper-right region near the exit point of Al interconnect. The average current density on remained UBM opening is about 1.26×10^4 A/cm^2. But, the maximum current density is 9.53×10^4 A/cm^2 in the solder bump, which is adjacent to UBM. Figure 4-3 (c) shows the current density distribution corresponding to the marker position. Indeed, the current crowding effect is the strongest close to the marker No. 10. The current density on marker No. 10 has reached 4.8×10^4 A/cm^2 which is slightly lower than the maximum current density because it was about 11 μm away from the die. The average current density on the UBM opening is 1.26×10^4 A/cm^2. The current crowding ratio, which is denoted as the maximum current density

divided by the average current density, is about 3.8. The current density away from the current exit point is smaller than 1×10^4 A/cm^2.

To observe the maker movement, the positions of markers were measured by a software, Image-J, before and after the current stressing. It can translate the pixels in SEM image to the length. The uncertainty is about 0.1 μm. The evolution of marker position is shown in Figure 4-4 (a). It was found that the markers near the current crowding region (Markers 6-10) moved close to the Si die. Since the electron flow went from the chip side to the substrate side, the Sn atoms were pushed downward and the vacancies were pushed upward. But the marker movement at the low current density region (Markers 1-5) migrated in the opposite direction against the electron flow. This interesting phenomenon will be discussed later. The markers almost do not move horizontally. We did not measure movement of the marker depth. But we believe that the EM flux will almost pass from the chip side to the board side which is the z-direction. Then other directions can be ignored. To determine the velocity of marker movement, we define it as the difference of distance between the edge of the Si die and the marker before and after current stressing divided by the stressing time. As shown in Figure 4-4 (b), for 150 and 300 h current stressing, it is clear that the largest marker movement is located at marker No. 10. The other markers have lower velocities. These results prove the effect of current crowding experimentally. After

1632 h current stressing, the maximum marker velocity still occurred at the marker No. 10. But the velocity of marker No. 10 decreased from 8.6×10^{-7} μm/s to 3.5×10^{-7} μm/s. Since the current crowding region has the highest atom diffusion velocity, void formation and propagation started from the entrance point of Al interconnect. After the pancake-type void formed, the conducting path was interrupted by the void and forced the conduction to pass the void. Thus, the velocity of marker near the original current crowding region decreased, and the velocity away from the current crowding region increased. We noted that the makers at low current regions (Markers 1-5) possess negative velocities.

It has been reported that the threshold current density for EM in pure Sn is about 8×10^3 A/cm^2 at 100 °C [58]. The local current densities at makers, No. 1 to 5, may be lower than the threshold current densities. Thus, in these regions no EM occurred and no back-stress induced. Yet the negative marker velocities indicate that atomic flow has occurred, but it is against electron flow. Such migration may occur if we assume a constant volume of the solder bump. In the high current density region, atoms are driven to the anode. There back stress develops as accumulation occurs. When the stress is beyond the elastic limit, either plastic deformation or lattice shift occurs to relieve the stress. If we assume a constant volume model, the anode needs to create room for the incoming atomic flux by out-diffusion. The out-diffusion can

occur under a stress gradient going from the high back stress region to the neighboring low back stress region. Then, the lattice shift of atomic back flow occurs in the low current density region because the resistance is lower. As a consequence, we have negative marker motion in the low current density region.

In Figure 4-4 (c), we obtain the direct correlation between current density distribution and marker velocity distribution in the solder joints. For electromigration in Al films, it has been shown that the relationship is linear if the current density is low [9,59,60]. In our results here, both the fitting lines for data of 300 h and 1632 h show linear relationship between current density and marker velocity, indicates that reliable data have been obtained in this study.

Under EM, electron wind force and back stress gradient induced atomic fluxes are given as [61]:

$$J_{em} = C\frac{D}{kT}Z^{*}eE - C\frac{D}{kT}\frac{d\sigma\Omega}{dx} \qquad (4.1)$$

where J_{em} is atom flux in unit of atoms/cm^2-s, C is concentration of atoms per unit volume, D/kT is atomic mobility, σ is hydrostatic stress in the metal, dσ/dx is stress gradient along the direction of electron flux, Ω is atomic volume, Z* is effective charge number of electromigration, e is electron charge, and E is electric field. In this study, the EM was focused on current crowding region in the cathode end. When we take Ω_{Sn} to be 2.71×10^{-29} m^3, Δσ to be about 20 MPa, and Δx to be 75 μm, the back

stress gradient is several orders of magnitude smaller than the electron wind force. The estimated EM and back stress fluxes are about 75 • C and 0.45 • C atoms/cm^{2}s, respectively. Thus, the back stress is negligible here. Equation 4.1 can be simplified as:

$$J_{em} = C\frac{D}{kT}Z^*eE = C < v > \tag{4.2}$$

Where <v> is atomic drift velocity, and E = ρj, ρ is metal resistivity, j is electron current density. Then, the mean atomic drift velocity <v> in EM is given below:

$$C < v >= \frac{eDZ^*}{kT}\rho j \tag{4-3}$$

here, T is 108 °C which is equal to 381 K measured by IR microscopy, ρ is 16 μΩ-cm at this temperature according to the temperature coefficient of resistivity of solder. From the results shown in Figure 4-2, DZ* was calculated from each marker position by this equation. The average of DZ* was calculated to be 3.3 × 10^{-12} cm^2/s. The lattice diffusivities in pure β-Sn along the direction parallel and normal to the c-axis are 1.6 × 10^{-14} cm^2/s and 3.8 ×10^{-14} cm^2/s, respectively [62]. Therefore, the average D of tin in tin is 2.7 × 10^{-14} cm^2/s at 108 °C, the calculating Z* is 125, the value is high but unreasonable. Tsai *et al.* calculated the DZ* for eutectic SnPb to be 5.0 × 10^{-10} cm^2/s [63]. So, DZ* of the lead-free solder is two orders of magnitude lower than that of eutectic SnPb under the same temperature. It is most likely that the diffusivity in the eutectic SnPb is much higher than that in the eutectic SnCu.


E S A
1896

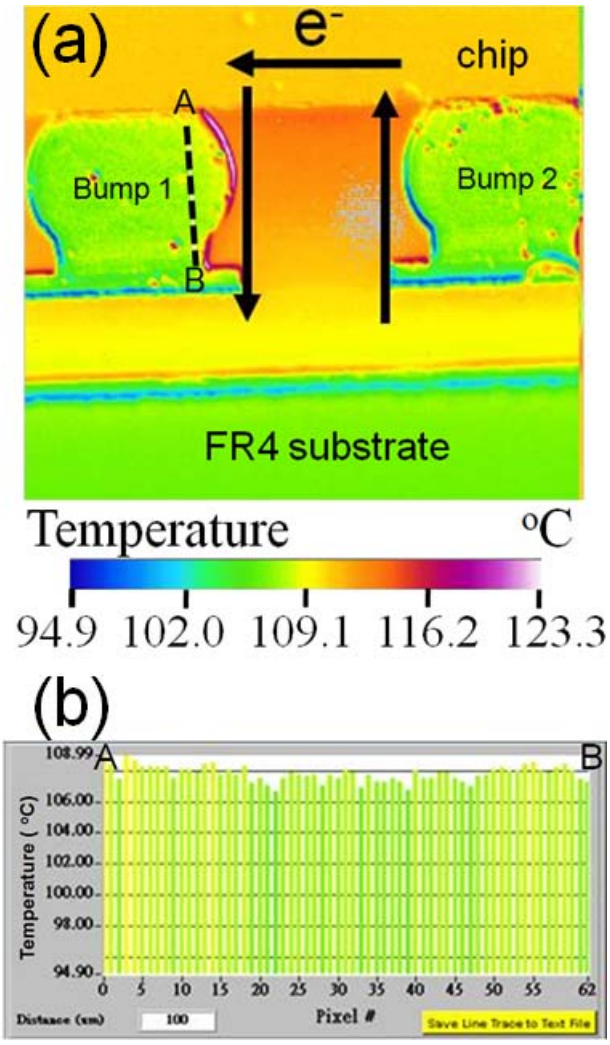


Figure 4-1: (a) IR images showing the temperature distribution in the bump with 0.6 A at 100 °C. (b) The temperature profiles along with dashed lines in the bump.

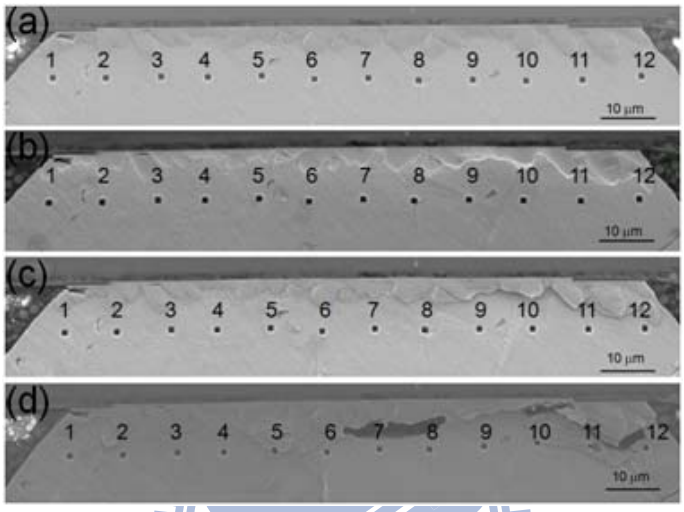


Figure 4-2: SEM image for the solder before and after the current stressing for (a) 0 h. (b) 150 h. (c) 300 h. (d) 1632 h.

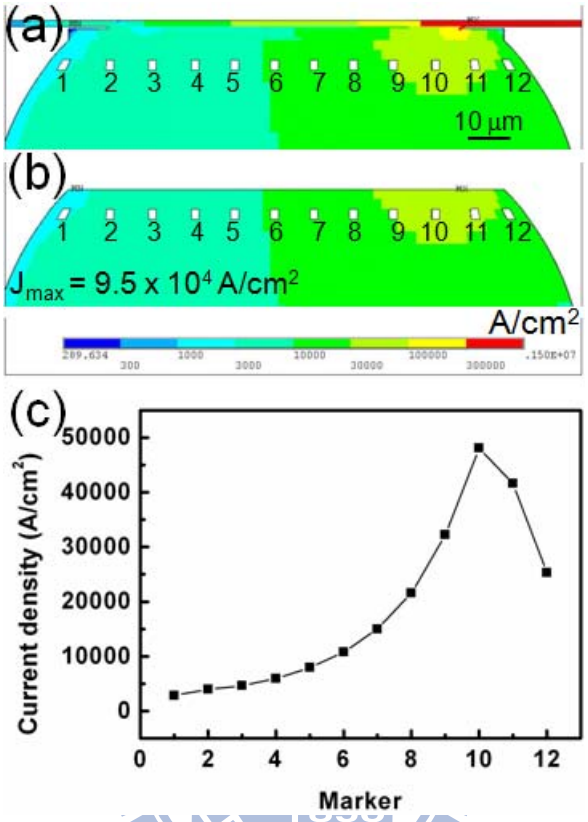


Figure 4-3: Simulation results on current density distribution in the flip-chip solder joints (a) With Al trace and UBM. (b) With the solder bump only. (c) Local current density at the 12 marker positions.

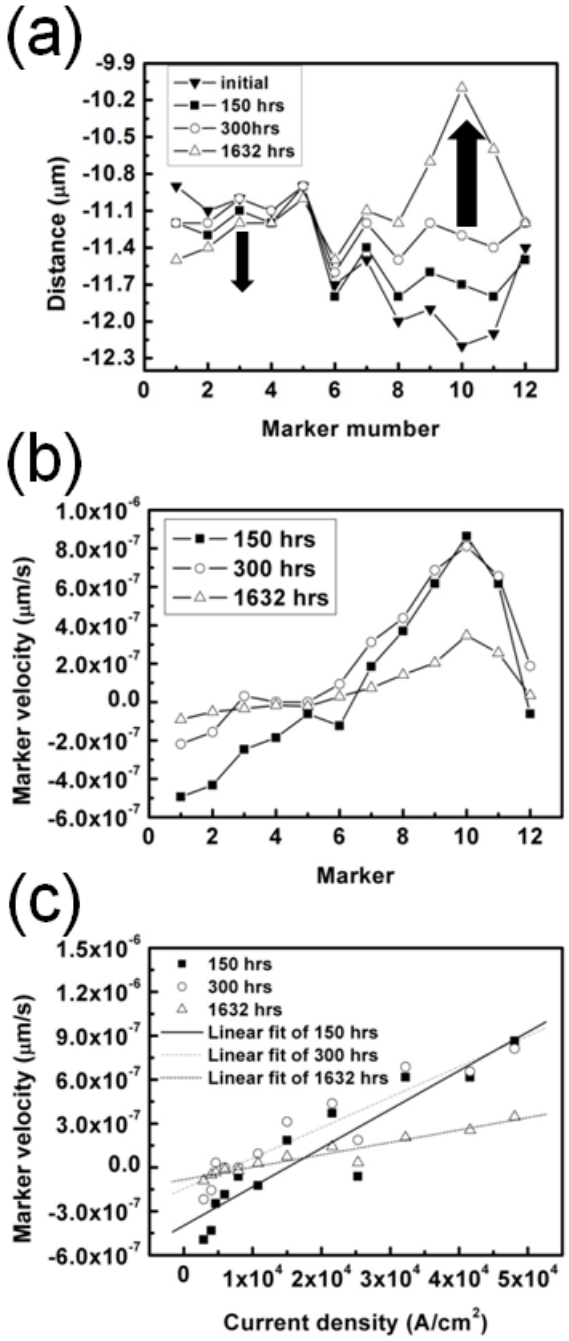
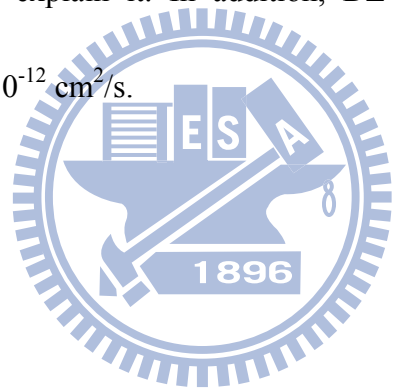


Figure 4-4: (a) The evolution of marker position for 12 markers at various stressing times. (b) Marker velocity at 12 marker positions with different stressing time. (c) Plot marker velocity as a function of local current density with different stressing time. The marker velocity is proportional to the local current density at the marker.

4.1.2 Summary

In summary, the distribution of EM rate in flip-chip solder joints was measured by an array of markers near the cathode end. We found that the EM rate at the current crowding region is much higher than those in the rest of the solder joints, which supports the previous simulation results on the effect of current crowding. The non-uniform EM has resulted in non-uniform and even negative marker motion. The latter indicates a back flow of atomic flux. We have proposed a constant volume model and back stress to explain it. In addition, DZ* for Sn-0.7Cu solder was calculated to be about 3×10^{-12} cm^2/s.



4.2 Blocking whisker growth by IMC formation

4.2.1 Results and discussion

Spontaneous Sn whisker growth is of concern in high reliability devices such as satellites. To understand whisker growth, we need to accelerate the growth. Electromigration can do so in using Blech test structures of pure Sn stripes. However, how to reduce and prevent whisker growth is an important technology and is of wide interest. In this section, EM in Pb-free solder bumps from ASE was conducted to observe the whisker and hillock growth in the anode. We found that the accompanied IMCs in the anode can serve as diffusion barriers to block the diffusion of Sn and to slow down the whisker and hillock growth. The effectiveness of the barrier depends on the amount of IMC formation at the anode, which in turn depends on the supply of Cu from the cathode.

The sample was cut and polished to the center of the solder joints. One pair of the flip chip solder joints was stressed by current density of 1.3×10^4 A/cm^2 on a hotplate maintained at 100 °C. Figure 4-5 (a) depicts the 3-dimensional view of the pair. The cut surface serves as the first cross-sectional surface for in-situ observation in EM, and the arrows indicate the electron flow direction. It enters the right-hand side bump from the middle of the bottom, exits the bump at the upper left corner, enters the left-hand side bump from the upper right corner, and exits it from the rear

of the middle bottom. In right-hand side bump, current crowding occurs at the upper left corner, which is the anode. In the left-hand side bump, current crowding is less at the anode, which is at the bottom rear because the Cu bond-pad is thick. Since the microstructure and IMC formation in the matrix of the solder joints is important, the sample was cross-sectioned a second time as illustrated in Figure 4-5 (b). Either the right-hand or the left-hand side bump was cross-sectioned. Then ion channeling image of focus ion beam (FIB) and secondary SEM images were employed to investigate the surfaces morphology and phase distribution on the second cross-section.

Figures 4-6 (a) to (c) show the evolution of surface morphology on the first cross-section for the right-hand side solder joint with a downward electron flow (from the chip side to the substrate side) of the as-prepared solder bump, after 150 h and after 1632 h of current stressing, respectively. As shown in Figure 4-6 (b), a hillock was extruded near the anode end. In Figure 4-6 (c), a void formed and propagated at the cathode end. Moreover, the hillock grew extensively and almost occupied the entire bottom of the solder bump. However, from the images of the first cross-section, the volume of void is quite small as compared with the volume of the hillock; they seem mismatched. Actually, as illustrated by the second cross-section in Figure 4-6 (d), the surface sank in the middle of the solder bump. Thus, the volume or mass is conserved, and the mass of the hillocks is from both the void and the depression of the

solder joints. The extrusion thickness of the hillock is about 10 μm to 20 μm.

In the left-hand side solder joint with the upward electron flow (from the substrate side to the chip side), smaller hillocks were observed at the anode. Figure 4-7 (a) to (c) show the morphology changes on the first cross-section of the as-prepared solder bump, after 150 h and after 1632 h of current stressing, respectively. Compared Figure 4-7 (a) with Figure 4-6 (a), the phase distribution in the as-prepared state is almost the same before current stressing. After the current stressing for 150 h, much IMC was formed in the cathode near the Si chip side but no hillock formed, as shown in Figure 4-7 (b). After stressing for 1632 h, as shown in Fig. 4-7 (c), the formation of IMCs became more obvious than that in Figure 4-7 (b). Only one small whisker is extruded, as shown in the enlarged image in Figure 4-7 (d).

To investigate the microstructure and IMC distribution in the matrix of the solder joints, FIB ion channeling image was used to analysis the second cross-section. Due to ion channeling effect, the contrast of Sn grains looks darker than that of IMC since IMC has less ion channeling, as shown in Figure 4-8. In Figure 4-8 (a) and (b) show the second cross-section of the right-hand side bump with electron flow downward are shown. The hillock is the Sn grain closest to the substrate to be extruded out when the grain is adjacent to the IMC on the Cu bond-pad. There is no IMC between the hillock and the matrix of the solder. Next to the hillock, there are two columnar-type of Sn

grains along the electron flow. They were dimpled and the Sn atoms that driven to grow the hillock by electromigration, as illustrated in Figure 4-8 (b).

When the electron flow went upward as in the left-hand side bump, not only the Sn but also much of the Cu were driven from the bond-pad to the anode at the upper left corner on the chip side and a large amount of IMC was formed there. During the growth of Sn hillock, IMC grains were distributed along the surface of the first cross-section and accumulated at the chip end as illustrated in Figure 4-8 (c). The high magnification image in Figure 4-8 (d) revealed that the Cu_6Sn_5 IMCs have become a diffusion barrier and blocked the Sn supply to the hillock grain.

It is known that the driving force of hillock growth is to relieve the compressive stress due to IMC formation and the accumulation of Sn atoms at the anode in EM. In the flip chip structure, the current crowding is more serious at the anode on the chip side than at the anode on the substrate side. The flux density at the anode should be quite different between upward and downward electron flows. Thus, we might expect the hillock or whisker should grow faster in the bump with upward electron flow than that with downward electron flow. However, EM drives both Sn and Cu to the anode. For a longer stressing time, the hillock growth will be affected by the IMC formation, in turn the supply of Cu from the cathode to the anode. In Figures 4-7 (b) and (c), with a thick Cu bond-pad, a large amount of Cu atoms was driven from the substrate side

to form IMCs on the chip side. The IMC growth may create the compressive stress to extrude the hillock. However, the excessive formation of IMC blocked the diffusion path of the Sn atoms driven by EM. A typical case is shown in Figure 4-8 (d), where the IMC at the root of the hillock has become a diffusion barrier and hindered the growth of hillock.

In our test samples, SOP process on the substrate side has thick Cu, so in the right-hand side bump under EM with an upward electron flow, a large amount of Cu atoms can be dissolved and driven to the anode on the chip side to have enough IMC to form a diffusion barrier layer to stop the supply of Sn for the hillock growth. On the other hand, in the left-hand side bump with a downward electron flow, the amount of Cu in the thin film UBM on the chip side is not enough to be dissolved and form a diffusion barrier on the substrate side, so the hillock become huge.

Besides the blocking effect of IMC, the difference of the temperature at the chip and the substrate side may also affect the hillock and whisker growing rate. We found that if the hotplate temperature increased to 150 °C, the hillock growth at the substrate side is not as significant as that at 100 °C. Since 150 °C is a high homologous temperature for Sn, the mechanical stress can relax more quickly, so the driving force of hillock or whisker growth is reduced.

On diffusion of Cu, it has been reported recently that due to anisotropic effect,

the diffusivity of Cu in Sn along the c-axis is three to four orders of magnitude faster than that along the a or b-axis [64-67]. Hence, the orientation of the Sn grains in the solder joint matrix will have a profound effect on the diffusion of Cu from the cathode to the anode. The interaction among the anisotropic effect, current crowding, and the supply of Cu from the cathode to the anode requires more study. In present case, since the grain size in the solder joint matrix is about 20 μm, so there were about 5 grains in the solder joint between the cathode and the anode, the change of orientation between grains will reduce the anisotropic effect of diffusion.

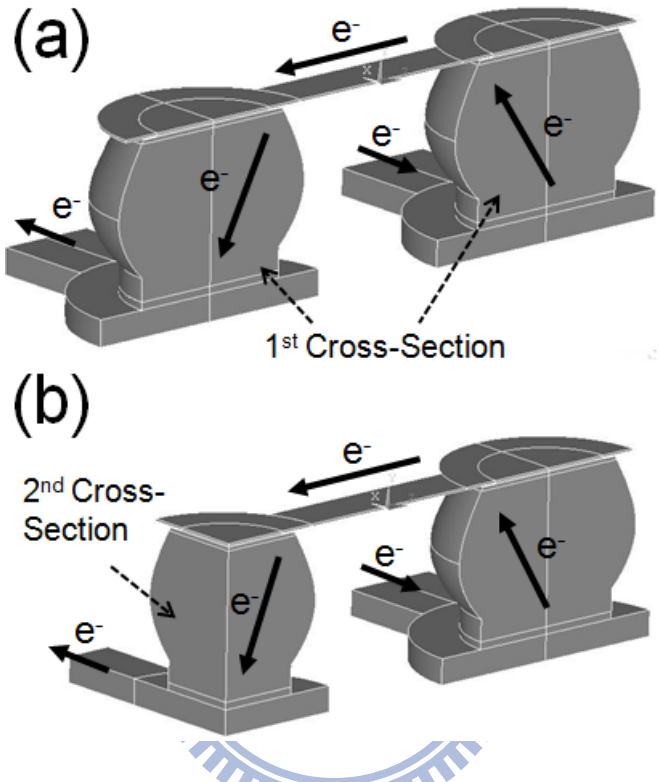


Figure 4-5: (a) Three-dimensional diagram for the solder joints with the direction of electron flow with first cross-section. (b) Three-dimensional diagram for the solder joints with the direction of electron flow with second cross-section.

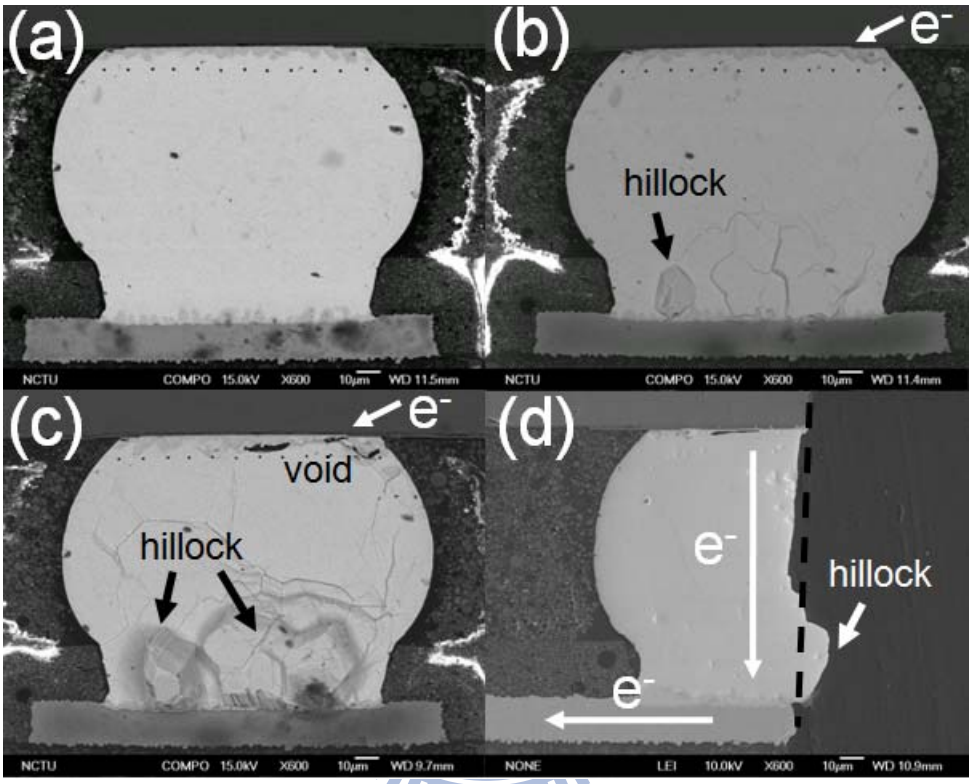


Figure 4-6: Cross-sectional BEI for the solder joints with downward electron flow before and after the current stressing. (a) Before current stressing. (b) After 150 h. (c) After 1632 h current stressing. (d) Second cross-section for the sample in (c).

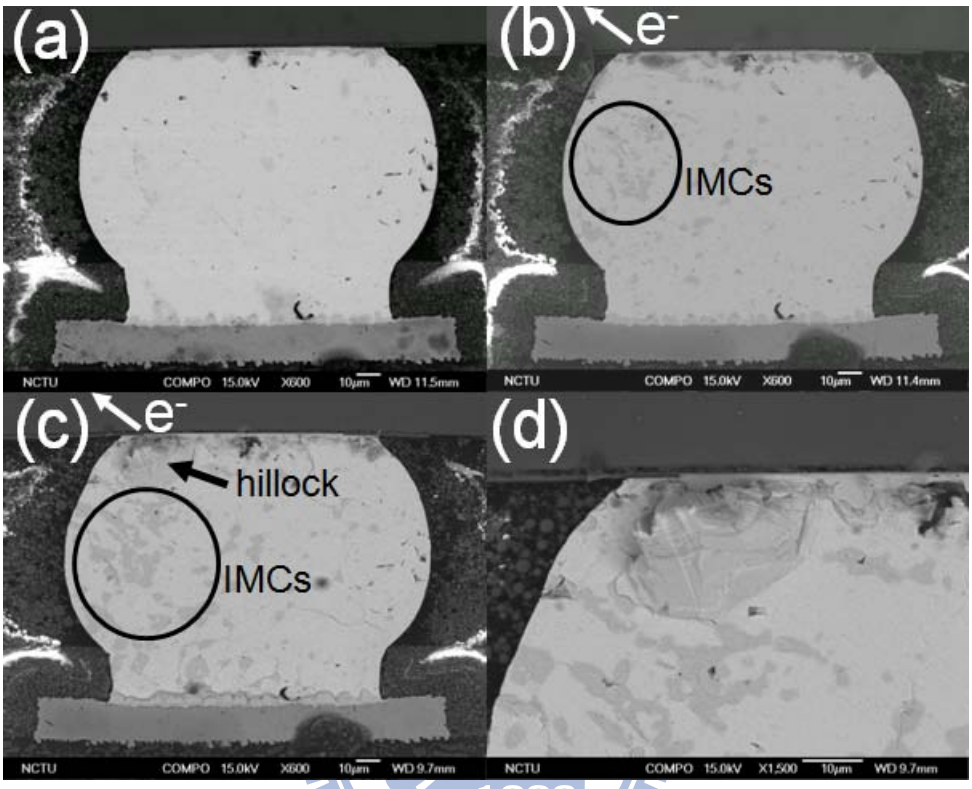


Figure 4-7: Cross-sectional BEI for the solder joints with upward electron flow before and after the current stressing. (a) Before current stressing. (b) After 150 h. (c) After 1632 h current stressing. (d) Higher magnification of the sample in (c) to show a clear image of the whisker.

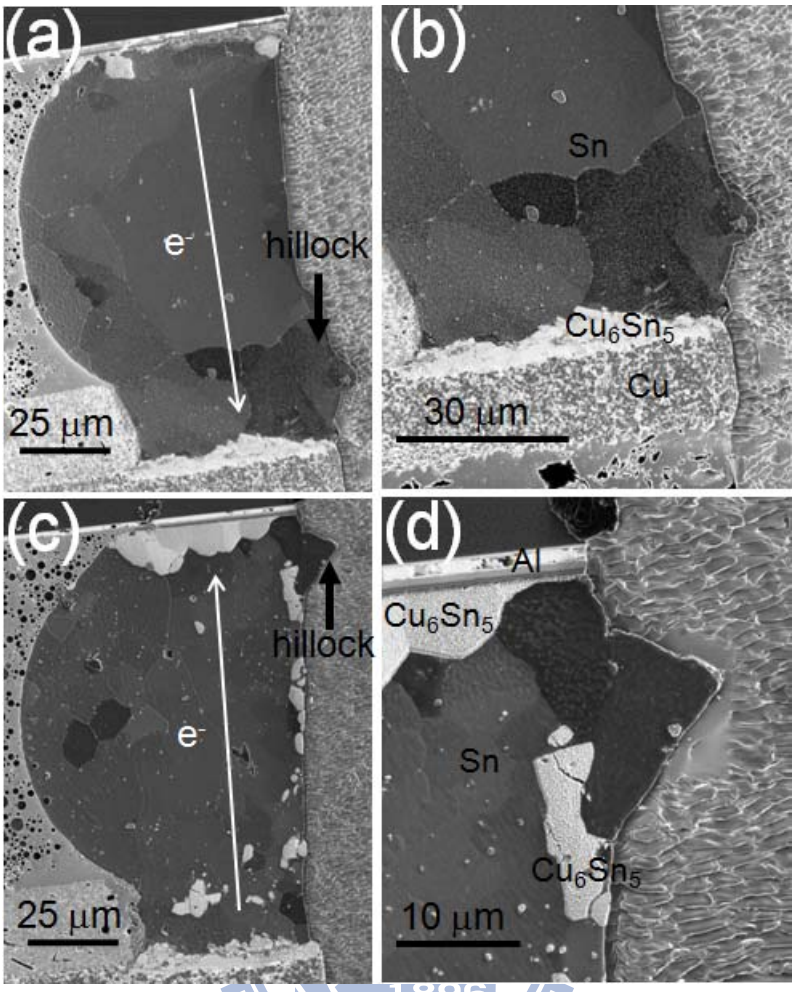


Figure 4-8: FIB image for second cross-section of the solder joints after the current stressing for 1632 h. (a) In the solder bump with the upward electron flow. (b) Higher magnification of (a) to show the grains and IMCs distributions of the bump. (c) In the solder bump with the downward electron flow. (d) Higher magnification of the sample in (c) to show the IMCs formation blocking the tin diffusion path for the whisker growth.

4.2.2 Summary

In summary, hillock and whisker growth occurs at the anode in cross-sectioned Sn-0.7Cu flip-chip solder joints under electromigration. The growth at the anode is accompanied by IMC formation since Cu atoms were driven to the anode together with Sn atoms. IMC formation can become a diffusion barrier to block the supply of Sn to grow the hillock and whisker. It is effective if the supply of Cu is sufficient.

4.3 Design of Kelvin probes to measure the bump resistance

4.3.1 Results and discussion

Kelvin structures have been used to measure via or contact resistance in Al and Cu interconnect for over twenty years, in which four electrical terminals are employed to measure the contact resistance [68, 69]. The geometrical effect of the contact resistance has been investigated by Natan *et al* [70]. Liu *et al.* investigated the electrical resistance of the solder joints, but the current crowding effect was not considered [71]. Electromigration has become an important reliability issue for flip-chip packages due to the continuous shrinking of the solder joints [7,72]. Although the bump resistance may not be a critical issue for signal delay consideration, it can be used to monitor the failure of electromigration test. Recently, many researchers have been using bump resistance changes to monitor electromigration behavior [73-75]. Gee *et al.* has designed this structure to measure bump resistance in ball grid array during EM [73]. Ebersberger *et al.* used it to monitor the failure of electromigration in flip-chip solder joints [75]. However, no literature has been found on measuring the bump resistance.

In addition, from the scientific point of view, the bump resistance may be of interest, since serious current crowding occurs in the solder joints, and the joint comprises several materials. Compared with Al and Cu interconnects, the dimension

of the solder joints is quite large. Therefore, there are several ways to design Kelvin bump structure. However, no significant effort has been made on the measurement and modeling of the bump resistance. The crowding effect on bump resistance has not been studied. In this part of study, we measured the bump resistance by Kelvin structure and employed the 3D finite element modeling to investigate the geometrical effect of bump resistance. This study provides a deeper understanding of the bump resistance in flip-chip solder joints.

We have designed and fabricated Kelvin structure for the flip-chip solder joints which are provided by Megic. Figure 4-9 (a) shows the plan-view schematic for the structure. The test structure consisted of four bumps, in which Al trace connected them together. Al trace was 1.5 μm thick and 100 μm wide. The pitch for the solder joints was 1mm. Six Cu lines in the FR5 substrate connected to the four bumps, and they were labeled as node 1 through 6, as shown in the figure. The dimension of the Cu lines was 30 μm thick and 100 μm wide. The bump connected to the node 3 and node 6 was used to investigate the geometrical effect of bump resistance. Through these six Cu lines, various experimental setups can be performed to measure the bump resistance for Bump 2. In this study, four approaches were adopted to measure the bump resistance. The experimental setup for the first approach was shown in Figure 4-9 (b). The current was applied through nodes 1 and 2, and the voltage drop was

monitored through nodes 4 and 5. This approach measures the voltage drop on the left-hand side of the bump. The second experimental setup is illustrated in Figure 4-9 (c), in which the current was applied through nodes 1 and 4, and the voltage change was examined using nodes 2 and 5. For this approach, the voltage drop across the diagonal of the bump was measured. The third approach is shown in Figure 4-9 (d), current was applied through nodes 1 and 2, and the voltage difference was measured through nodes 3 and 5. The fourth approach measured the voltage drop across nodes 5 and 6 when current was applied through nodes 1 and 2, as depicted in Figure 4-9 (e).

Surprisingly, the measured bump resistance was much lower than that expected for the four approaches shown in Figures 4-9 (b) and (e). Figure 4-10 shows the typical bump resistances as a function of temperature up to 150 °C for the four approaches. For bump resistance measured by approach 1, the value was only 0.89 mΩ at room temperature. The resistance increased with the increase in temperature, and it was attributed to the TCR. If we assume the TCR to be linear, the estimated TCR for the solder joint was 5.1×10^{-3} K^{-1}. The measured bump resistance comprised the contribution from Al, Cu, Ni, Sn and Pb materials. Therefore, the TCR may be the combination of the above materials. The TCR values for the bulk Al, Cu, Ni, Sn, and Pb are 4.2, 4.3, 6.8, 4.6, and 4.2×10^{-3} K^{-1}, respectively. Hence, the measured TCR seems to be quite reasonable. The measured bump resistance for the

same bump was 0.87, 0.96, 0.94 mΩ at room temperature for the second, third, and fourth approaches, respectively. The bump resistances measured by approaches 3 and 4 are slightly larger than those by approaches 1 and 2. The temperature dependence of bump resistance was quite close to that measured by the first approach. The estimated TCR values are 4.4, 4.3, and 4.9 for the three approaches, respectively.

To examine the current and voltage distribution in the solder joints, 3D simulation was performed to provide more understanding of the effect of current crowding on the bump resistance measurement. Figure 4-11 (a) shows the current density distribution in the solder joints upon applying 0.2 A current. The current crowded into the solder bump in the vicinity of the entrance of Al trace, and only a small amount of current flows in the opposite side of the joint. Figure 4-11 (b) illustrates the voltage distribution in the solder joints. Since the resistance of the Al trace was much larger than that of the solder joints due to its smaller cross-section, most of the voltage dropped in the Al trace. Figure 4-11 (c) depicts the cross-sectional view along the YZ plane in Figure 4-11 (b). Apparently, voltage drop mainly occurred at the left-hand side of the bump, which was the current crowding region. The voltage drop on the left-hand side was approximately 9 times larger than that on the right-hand side. This may cause large variation in the measurement of bump resistance. Hence, the measured voltage strongly depends on the layout of the Kelvin

structure.

To investigate the geometry effect of the bump resistance, voltage at various positions were examined in the solder joints. Figure 4-11 (d) shows the voltage distribution in the solder joint, excluding Al trace and Cu line. Two positions, 1 and 5 in the chip side were labeled. On the substrate side, positions 2, 3, 4, and 6 were labeled. The definition of the positions matched the six nodes in Figure 4-9 (a). When the current was applied through nodes 1 and 2, the voltages in the six positions were examined. The results are listed in Table 4-1. The voltages in the chip side were obtained by averaging the voltages in the junction of Al trace and Al pad. The junction area was approximately 110 μm × 1.5 μm. For voltages in the substrate side, they were estimated by averaging the voltages in the junction of Cu line and Cu pad. The junction area was approximately 110 μm × 30 μm. It was found that the voltage drop across positions 1 and 2 was 1.54 mV, whereas it was only 0.15 mV across positions 4 and 5 (First approach), and it was 0.17 mV across positions 3 and 5 (Third approach) as well as positions across 5 and 6 (Fourth approach). Therefore, the simulated bump resistance was 0.77, 0.83, and 0.83 mΩ for the first, third and fourth approaches, respectively. Similarly, the theoretical bump resistance for second approach can be obtained by simulation, and the value was 0.76 mΩ. Table 4-2 summaries the experimental and simulation results on bump resistances for the four

approaches. The measured bump resistance was 0.89, 0.87, 0.96, and 0.94 mΩ, whereas the simulated value was 0.77, 0.76, 0.83, and 0.83 mΩ for the four approaches respectively. The experimental results were approximately 12-14 % higher than the simulated values. The difference may be attributed to the variation in bump height, and the temperature differences between the simulation and the measurement. In the simulation, the resistivity values adopted was at 20 °C, but the measurement was done at temperature range 25-30 °C. Although the experimental values were higher than the simulated ones, geometrical effect shows the same trend for both results. Therefore, the simulation results are in good agreement with the experimental data. These results indicate that serious current crowding effect occurs in the flip-chip solder joints.

On the basis of the simulation results, the real bump resistance should be equal to voltage difference between the current entrance point and the leaving points divided by the current. In the case of first approach as shown in Figures 4-11, the real bump resistance should be 7.7 mΩ. However, the measured bump resistances for the four approaches were less than 0.9 mΩ. The low measured values for bump resistance may be attributed to the serious crowding effect in the solder joints. Our previous 3D simulation shows that the current did not spread uniformly in the UBM opening. Instead, the current crowded into the solder bump in a small volume near the entrance

point of Al trace [16]. Little amount of the current passed through the opposite end of the entrance point of the current. Therefore, the voltage drops measured by the first approaches were much lower. For the third and fourth approaches, Kelvin probes for measuring voltage drops were closer to the current crowding region than those in the first and second approaches. Consequently, the measured values by the third and fourth approaches were larger than those by the first and second approaches.

Three components, Al pad (disc), UBM/solder, and Cu pad (disc), as shown in Figures 4-12 (a) to (c) may contribute to the bump resistance. From the simulation results, the bump resistance was 7.7 mΩ. In this paper, we denoted the bump resistance as the voltage drop across positions 1 and 2 which divided by the applied current. Therefore, the bump resistance included the above three components. Among them, Al disc contributed to the bump resistance most. This is because the cross-section of Al disc was quite small, approximately 1.5 μm × 100 μm. The current needs to flow through part of Al disc adjacent to Al trace in order to enter the solder joints through passivation opening, as shown in Figure 4-12 (a). The resistance of the partial Al disc was estimated to be 5.5 mΩ, which was about 72% of the bump resistance. In addition, since the cross sections for UBM/solder and part of the Cu disc was much larger than that of Al disc, they contributed only the rest of 21% resistance.

This bump resistance of 7.7 mΩ was larger than expected. We assume that the

current flows through the joint uniformly as illustrated schematically in Figure 4-13 (a). The resistance based on this assumption was estimated to be only 1.0 mΩ for our solder joints. In fact, the current path was not uniform, as depicted schematically in Figure 4-13 (b). The current entered the solder joints from Al trace, drifting in the left-hand side of Al disc, crowding into the solder joints from the passivation opening, spreading out gradually as well as drifting toward the substrate side, and leaving the joint from Cu disc. Due to this current path, the bump resistance was about 7.7 times larger than that for uniformly distributed current.

Thermal-electrical effect might affect the measurement of bump resistance. When two materials are joined together and a temperature difference ΔT is applied between two junctions, an open circuit voltage ΔV is established in the circuit when electric current I approaches zero. The Seebeck coefficient, α, is defined as [76, 77]:

$$\alpha = \left(\frac{\Delta V}{\Delta T} \right)_{I=0} \tag{4.4}$$

Therefore, if there is a temperature difference across the solder bump, there would be a voltage drop there. To estimate the magnitude of the voltage drop due to thermal-electrical effect in this measurement, we assumed the temperature difference across the solder bump is 1 °C, which is reasonable since the Joule heating effect in this study was less than 1 °C. The Seebeck coefficients at 300 K for Al, Cu and Sn are -1.66, 1.83, and -1 μV/K. Therefore, the voltage drop due to thermal-electrical effect

is approximately 1.5 μV, which is about 1~2 % of the voltage drop in the solder bump when applied 0.2 A. As a result, the influence of thermal-electric effect could be neglected in this study.

Based on the above results and discussion, a layout for Kelvin structure is proposed to measure the bump resistance, as shown in Figure 4-14. It is denoted as approach 5 in this paper. One voltage terminal is connected near the entrance of Al trace, and the other voltage terminal could be at any position on the substrate side, since the voltage at the substrate was almost constant. However, the measured value is the combination of part of Al trace and the bump resistance. The bump resistance can be obtained by excluding the resistance of Al trace. When the terminal is very close to the bump, the measured value will be near the bump resistance. Gee *et al.* has used this structure to monitor the bump resistance changes during electromigration [73]. The resistance they measured was as high as 26 mΩ. This high value may be mainly attributed to the larger bump height of about 250 μm, and to the resistance comprised part of the resistance of Al trace.

Although the bump resistance may not be a critical issue for signal delay consideration, it has been used to monitor the resistance change due to void formation during reliability test [77,78]. Zhang and Baldwin fabricated the Kelvin bump structure to monitor the bump resistance changes during power cycling, and the

resistance they measured were about 2 to 4 mΩ at room temperature for eutectic solder bumps with 125 μm in diameter [78]. Amagai *et al.* defined the failure of the solder joints during drop test by an increase in bump resistance by 1.2 times [79]. To examine the resistance change due to void formation, a void was inserted in the simulation model, as shown in Figure 4-15. The void depleted approximately 18% of the UBM opening. As the void formed near the entrance of the left Al trace, more current was forced to drift farther in the Al pad and entered the right-hand side of the solder bump, causing the increase in the bump resistance. The resistance increases due to the void formation measured by the four approaches are listed in Table 4-3. It was found the resistance increase was only 0.12 mΩ, which is approximately 15% increase in bump resistance. However, if the Approach 5 in Figure 8 is adopted to monitor the bump resistance, the change was only 6.5%. Therefore, the approaches 1 through 4 are more sensitive to void formation.

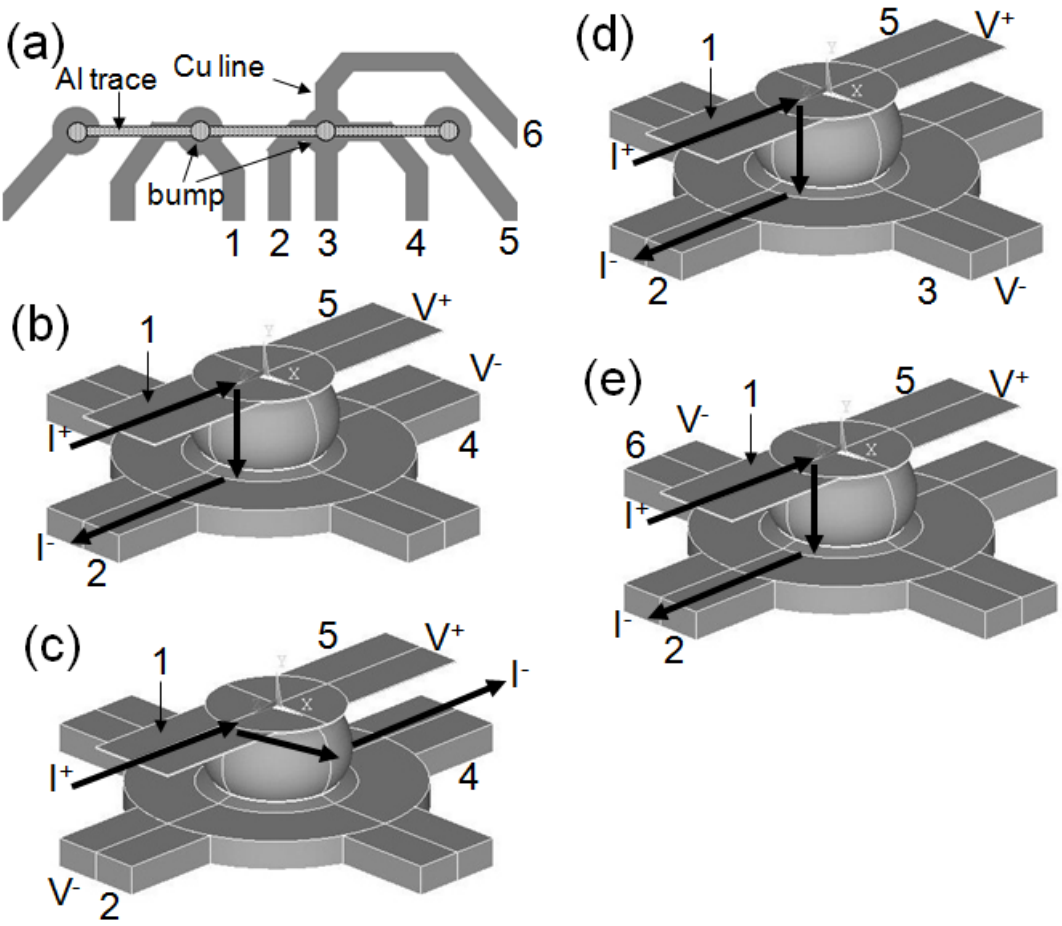


Figure 4-9: (a) Plan-view schematic of the layout design. Al trace connected all the four solder bumps together. Six nodes in the substrate side are labeled. Cross-sectional diagram shows the experimental setup for (b) Approach 1. (c) Approach 2. (d) Approach 3. (e) Approach 4.

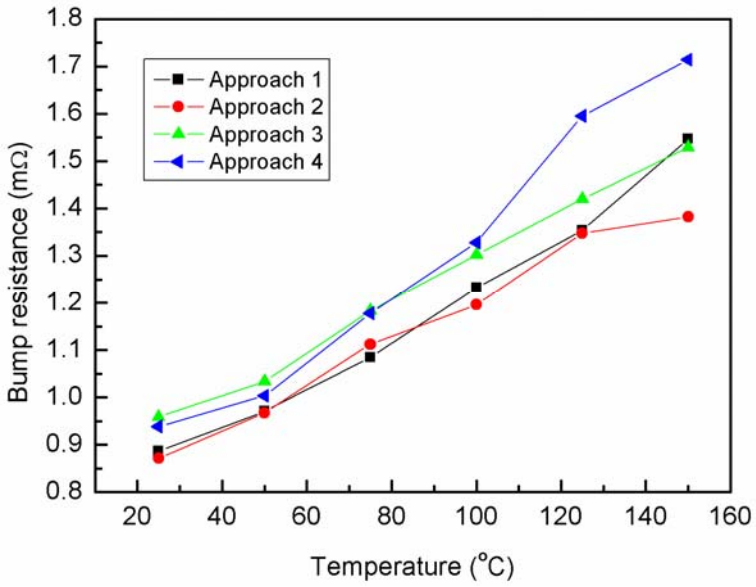


Figure 4-10: The measured bump resistance as a function of temperature up to 150 °C for the four approaches.

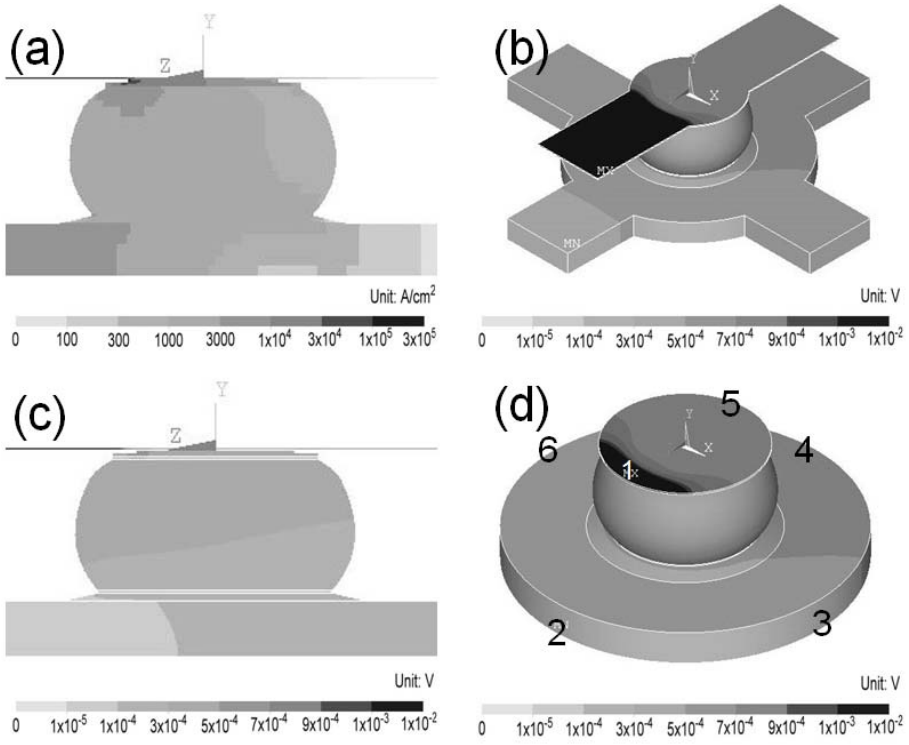


Figure 4-11: (a) Simulation results shows the current density distribution across the solder joints upon applying by 0.2 A. (b) The voltage distribution in the solder joints. Voltage drop mainly occurred in Al trace. (c) Cross-sectional view along the YZ plane in (b) shows that voltage drop inside the solder bump mainly occurred at the high current density region. (d) Voltage distribution in the solder joint, excluding Al trace and Cu line. Six positions were labeled for measuring the voltage drop.

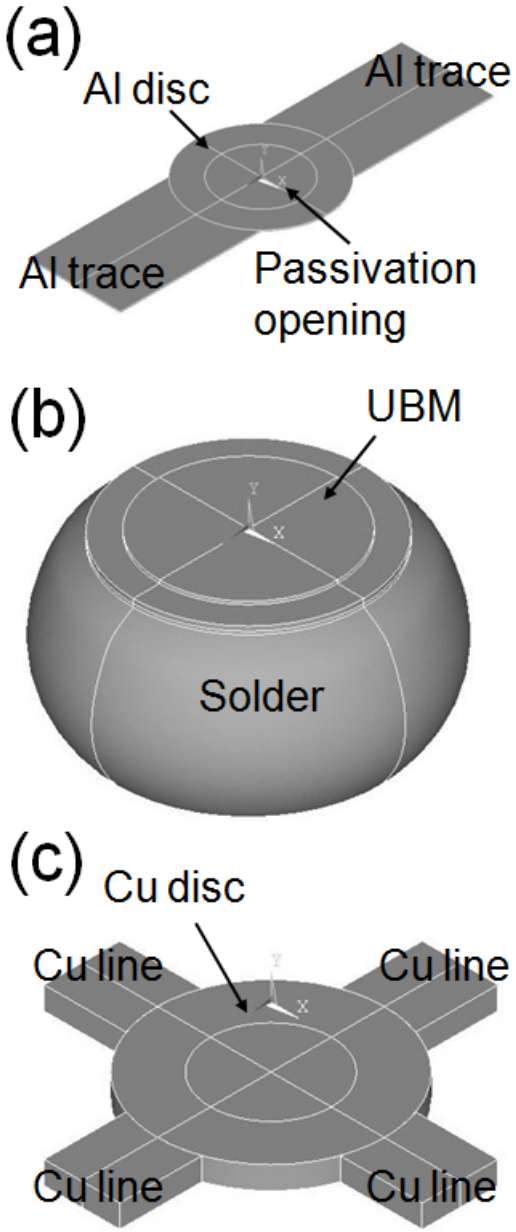


Figure 4-12: Three components contributing to the bump resistance, includ (a) Al disc, (b) UBM/solder, (c) Cu disc. The resistance of Al disc contributed about 79% of the total bump resistance.

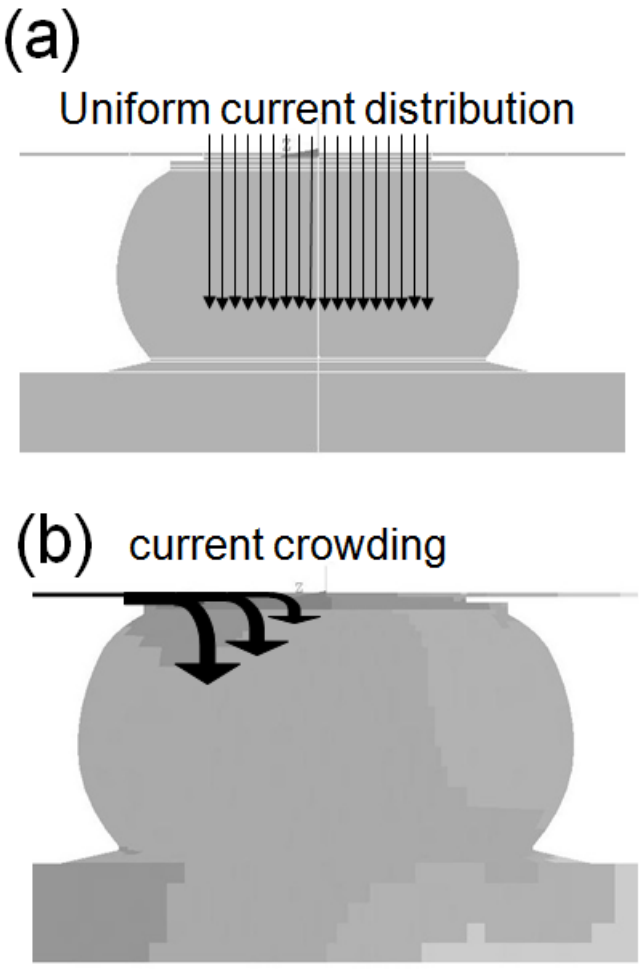


Figure 4-13: Schematic drawings shows (a) the uniform current distribution and (b) the current crowding effect in the solder joints.

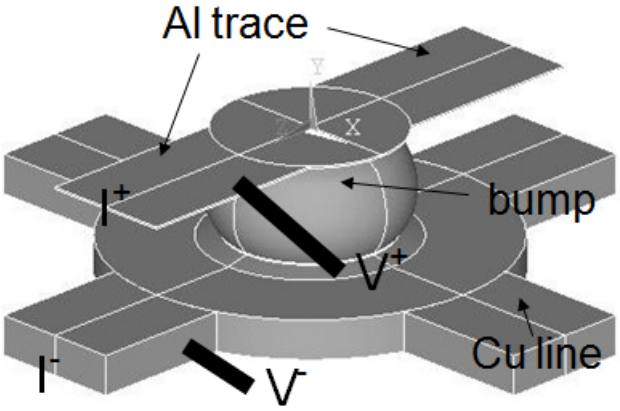


Figure 4-14: Proposed layout of Kelvin structure for measuring bump resistance of the flip-chip solder joint.

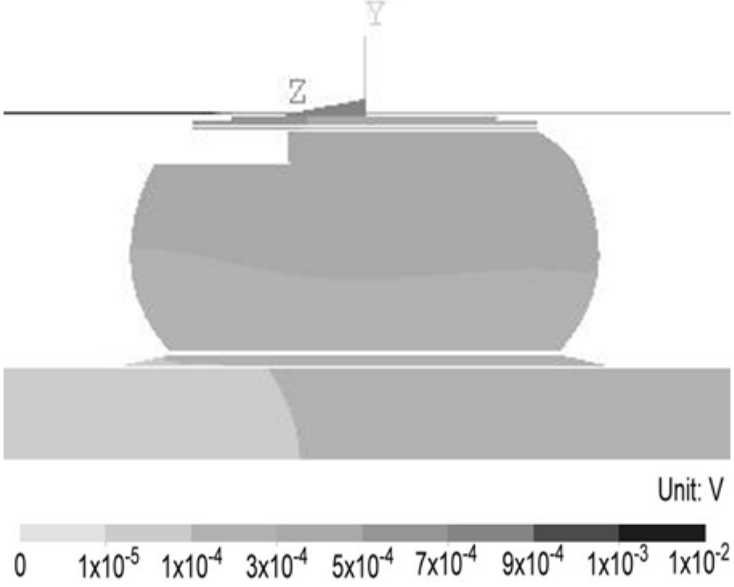


Figure 4-15: The voltage distribution in the solder bump when a void depleted approximately 18% of the UBM opening.

Table 4-1: The simulation voltages at the six positions in Figure 4-11 (b).

	Positions for voltage measurement					
	1	2	3	4	5	6
Voltage (mV)	1.66	0.12	0.36	0.17	0.16	0.17

Table 4-2: Experimental and simulation results on bump resistances for the four approaches.

Approach / Node	1	2	3	4
Experimental (mΩ)	0.89	0.87	0.96	0.94
Simulation (mΩ)	0.77	0.76	0.83	0.83

Table 4-3: The resistance increases due to the void formation measured by the different approaches in this study.

Approach	1	2	3	4	5
R_o (mΩ)	0.77	0.76	0.83	0.83	7.7
R_1 (mΩ)	0.89	0.88	0.95	0.95	8.2
$(R_1 - R_o)/R_o$ (%)	15.6	15.7	14.5	14.5	6.5

4.3.2 Summary

Kelvin structures for flip-chip solder joints were designed and fabricated to measure bump resistance. The measured bump resistance strongly depended on the layout of the Kelvin bump structures. The simulation results indicated that the difference in bump resistance could be as large as 9 times when the voltage drop was measured at different positions. It was found that the serious crowding effect may be responsible for the significant geometrical effect of bump resistance in flip-chip solder joints. The simulation results indicated that the approaches 1 through 4 are quite sensitive to detect the void formation, and thus they are quite suitable for monitoring the resistance change due to void formation.

4.4 Void formation and propagation during various stages of EM

4.4.1 Results and discussion

The mechanism of void nucleation, growth and especially the corresponding change of current distribution in the solder joints due to void formation are unclear. In particular, it is unknown why some voids are formed at the periphery of the UBM opening under the dielectric, where the current density is low [24,73,80]. In Blech structure of Al stripes, Tu *et al.* proposed that resistive vacancy might move to the low current density region to form voids due to the high gradient of current density, which was as high as 10^{10} A/cm^3 [22]. However, for flip-chip solder joints, the gradient of current density is estimated to be only 1.33×10^6 A/cm^3 owing to its large dimension [80]. Therefore, the growth of voids in the periphery of the UBM opening, which is located at the low current density region, may not be driven by the gradient of current density. In this section, three-dimensional finite element method was employed to simulate the effect of void formation on redistribution of current density and temperature in a flip chip solder joint, especially in the periphery area where a low- resistance thin film UBM exists.

Figures 4-16 (a) and 1(b) show the current density distributions before void growth. Figure 4-16 (a) demonstrates the 3D current density distribution inside the SnPb solder bump when 0.28 A was applied to the bump. Al trace, the UBM in the

chip side and the metallization in the substrate were ignored. It was found that the current crowded into the solder bump in the passivation opening. Figure 4-16 (b) shows the corresponding cross-sectional view along the YZ-plane. The current crowding behavior near the entrance of Al trace can be clearly demonstrated. The maximum current density reached 5.42×10^4 A/cm^2, which is about 22 times higher than the average value. The current density distribution in the top layer of the solder was plotted in Figure 4-16 (c). It is proposed that this local high current density was responsible for the initial void formation due to flux divergence [14,53]. Figure 4-16 (d) illustrates the temperature distribution before void formation. The maximum temperature inside the solder bump was 109.6 °C; therefore, the increase in temperature due to Joule heating was only 9.6 °C. The temperature was quite uniform inside the bulk of the solder.

In Stage I, a semi-cylindrical void, 45.5 μm in diameter and 13.0 μm in height, was formed inside the solder near the entrance of Al trace, as indicated by the arrow in Figure 4-17 (a). The current redistributed due to void formation, and the maximum current density occurred in the solder near the upper left corner of the periphery of UBM opening under Al trace. As shown in Figure 4-17 (b), void formation resulted in redistribution of current in two ways. First, current may drift farther along Al trace, passing the void and entered the solder. Second, the current may drain down to the

solder through the surrounding UBM/IMC layer. It is intriguing that the UBM/IMC layers served as a current path, directing the current into the upper left corner of the periphery of UBM opening. Since UBM/IMC layers have much higher electromigration resistance [7], voids are formed mainly inside the solder. Figure 4-17 (c) shows the current density distribution for the solder adjacent to the UBM/IMC layers. It is clear that the solder on the left of the void has higher current density than that under the passivation opening. Therefore, voids may propagate toward the solder in the UBM periphery. Compared with that shown in Figure 1, the maximum current density inside the solder has been reduced to 4.43×10^4 A/cm^2 due to void formation. On the other hand, the temperature inside the solder decreased slightly to 109.5 °C, which was 0.1 °C lower than that before void formation, as illustrated in Figure 4-17 (d). This may be attributed to the smaller crowding effect as a result of void formation.

Since the maximum current density occurred near the periphery of the UBM opening, we assume that the void propagates toward the left-hand-side periphery, as illustrated in Figures 4-18 (a) and (b). The void depleted 50% of UBM opening, which is denoted as Stage II. Figure 4-18 (c) shows the current density distribution for the solder adjacent to UBM/IMC layers as a function of position. Since UBM/IMC layers still serve as a current path, the void may be able to propagate to the edge of the

solder bump. Therefore, we postulate that the growth of void in the low current density region under the periphery of UBM opening is mainly attributed to current redistribution, not gradient of current density. The maximum current density inside the solder bump reduced further to 4.04×10^4 A/cm^2 due to void formation. Figure 4-18 (d) shows the corresponding temperature distribution in the solder bump. The maximum temperature in the solder was 109.3 °C, which was 0.2 °C lower than that in Stage II. Again, this may due to the smaller crowding effect in the solder joints at this stage. Although there was a slight increase in temperature in Al pad, the temperature inside the solder did not alter much at this stage. From the results reported by Gee *et al.*, the shape of the void may resemble a pancake shape for solder joints with thin-film UBM [66]. In addition, due to the limitation of our simulation modeling, semi-cylindrical voids were adopted in this study. However, whether it is circular, semi-circular or irregular remains unclear at this moment, and needs further experimental investigation by X-ray.

The void was then assumed to propagate to fill 80.5% of UBM opening, as shown in Figure 4-19 (a). It is denoted as Stage III. The current entered the joints through a smaller contact area, as depicted in Figure 4-19 (b), caused an increase in maximum current density. As seen in Figure 4-19 (c), it rose to 8.70×10^4 A/cm^2, and almost the whole passivation opening experienced current density higher than $1.0 \times$

10^4 A/cm^2. Therefore, void propagation will expedite in this stage. The maximum temperature in the solder bump increased to 109.4 °C because of the higher current crowding effect at this stage, as shown in Figure 4-19 (d). In the absence of current flowing through the solder in the left-hand side of the joint, the temperature on the right-hand side was higher than that on the left-hand side. However, there was still no obvious temperature increase in the solder close to the entrance point that the current flow into the solder.

The solder in the passivation opening was completely depleted at this final stage, leaving a small amount of solder near the periphery of the UBM opening, as illustrated in Figures 4-20 (a) and (c). There was approximately 4.0% of contact area left for conducting the current at this stage. With further decrease in contact area, the maximum current density became 1.69×10^5 A/cm^2, as shown in Figure 4-20 (c). UBM/IMC layers served as a conducting path to direct the current to the remaining solder. Hence, the remaining solder near the periphery of UBM opening could be completely depleted and caused the failure. Figure 4-20 (d) shows the temperature distribution at this stage. The maximum temperature in the solder bump was 110.4 °C, which was 0.8 °C higher than that before void formation.

Our simulation also shows that bump resistance increased gradually in the first three stages, and then increased rapidly in the final stage, as shown in Table 4-4.

Bump resistance was defined as the decrease in voltage between the entrance point of Al trace into Al pad (disc) and the junction point of Cu line with the solder joint. In Stage I, bump resistance increased from 11.2 mΩ to 14.6 mΩ. It increased to 19.0 mΩ and 25.3 mΩ in Stages II and III, respectively. It rose to 42.9 mΩ in Stage IV. This increase of bump resistance may also enhance the local Joule heating effect. However, no significant local Joule heating was found in the thermal simulation up to Stage IV. This may be attributed to the fact that the major heating source was Al trace [19]. In our model, the total resistance of Al trace was about 1800 mΩ. Consequently, the increase of bump resistance was quite small to compare with that of the Al trace. In addition, the increase in bump resistance was mainly due to the following manner: owing to void formation, the current needed to drift farther in Al pad (disc), and then flowed down to the solder bump. Therefore, the local Joule heating in Al pad (disc) increased when voids were formed. Since there was good heat dissipation in the Si side, the increase in temperature due to void formation was quite small. Nevertheless, the increase might be higher when larger current was applied, since the overall Joule heating would be significantly higher at higher stressing current.

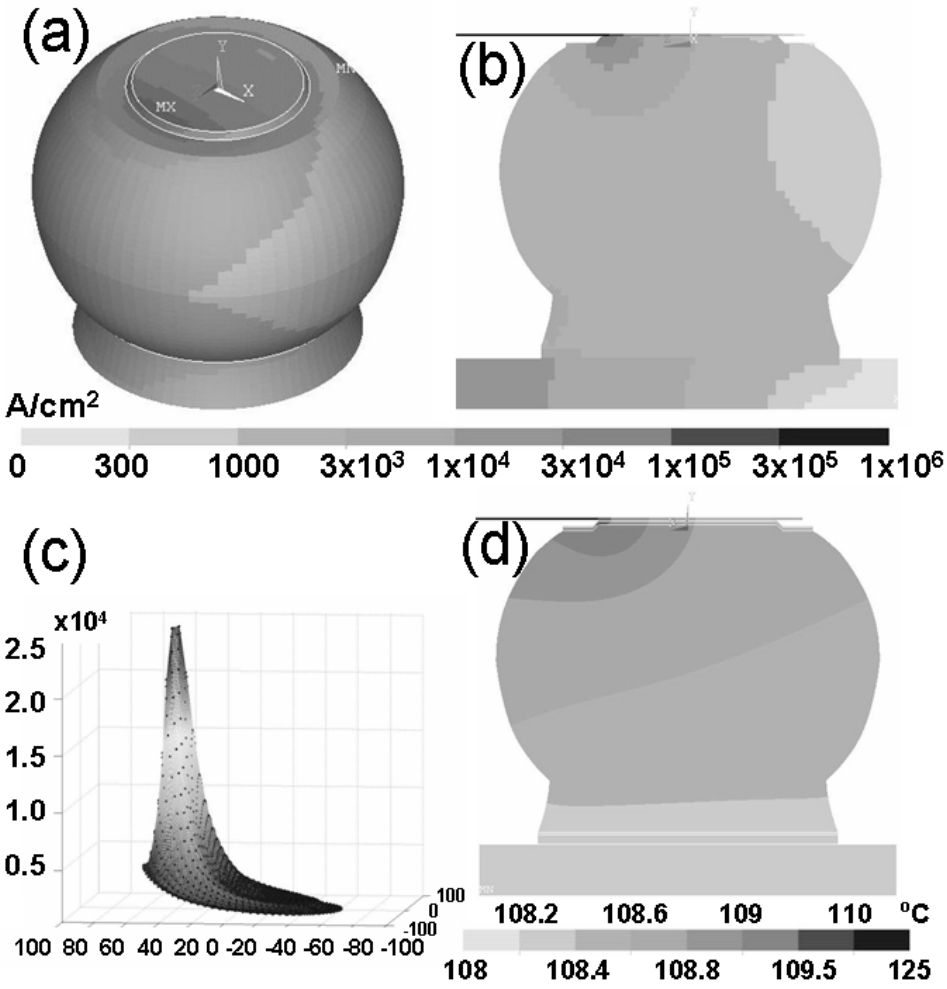


Figure 4-16: Current density distribution in solder joints before void formation. (a) Tilt view, shows solder bump only. (b) Cross-sectional view of (a). (c) Current density distribution in solder adjacent to UBM/IMC layers. (d) Corresponding cross-sectional view for temperature distribution.

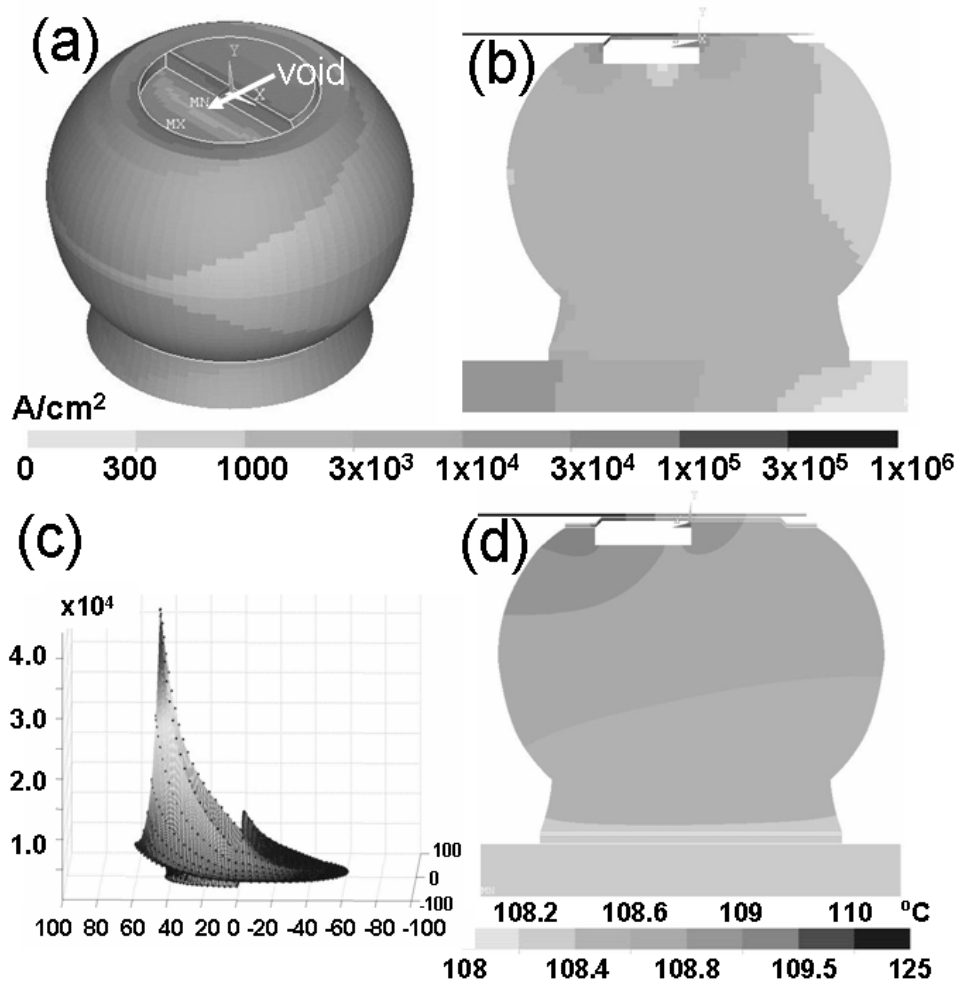


Figure 4-17: Current density redistribution in solder joints at Stage I. (a) Tilt view, shows solder bump only. (b) Cross-sectional view of (a). (c) Current density distribution in solder adjacent to UBM/IMC layers. (d) Corresponding temperature distribution.

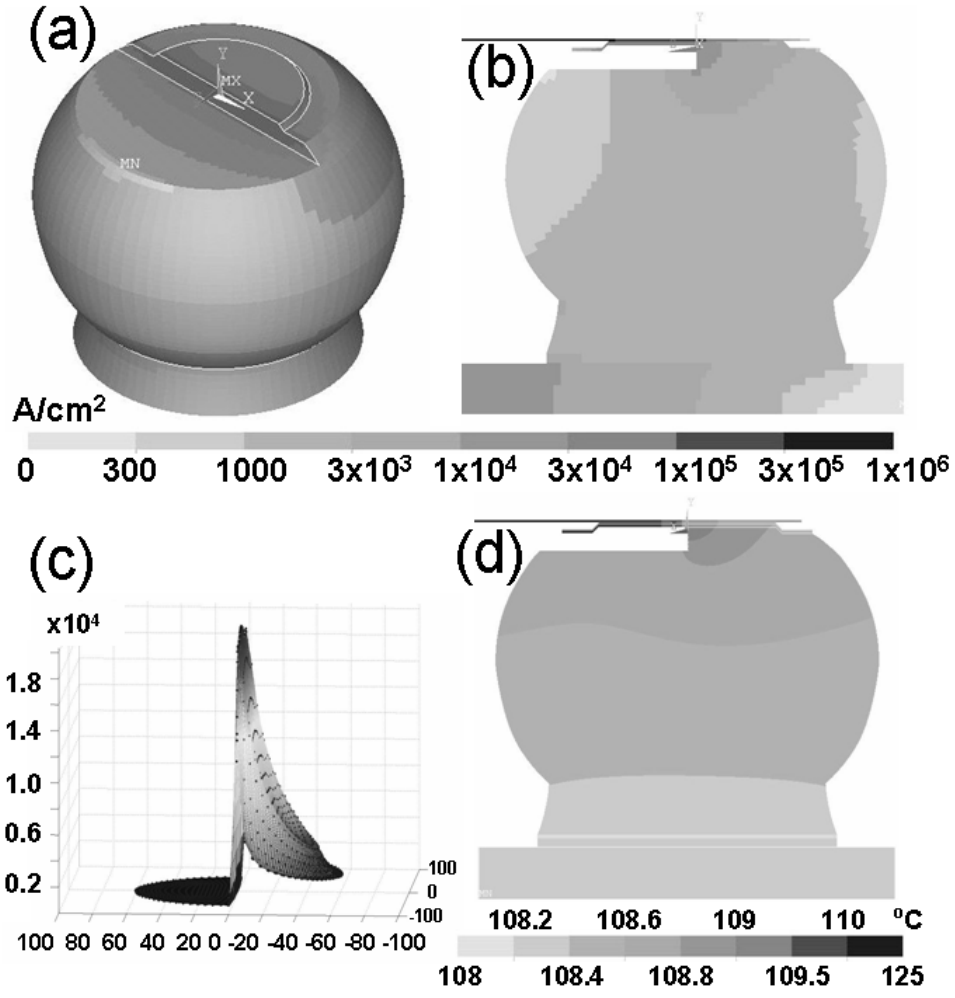


Figure 4-18: Current density redistribution in solder joints at Stage II. (a) Tilt view, shows solder bump only. (b) Cross-sectional view of (a). (c) Current density distribution in solder adjacent to UBM/IMC layers. (d) Corresponding temperature distribution.

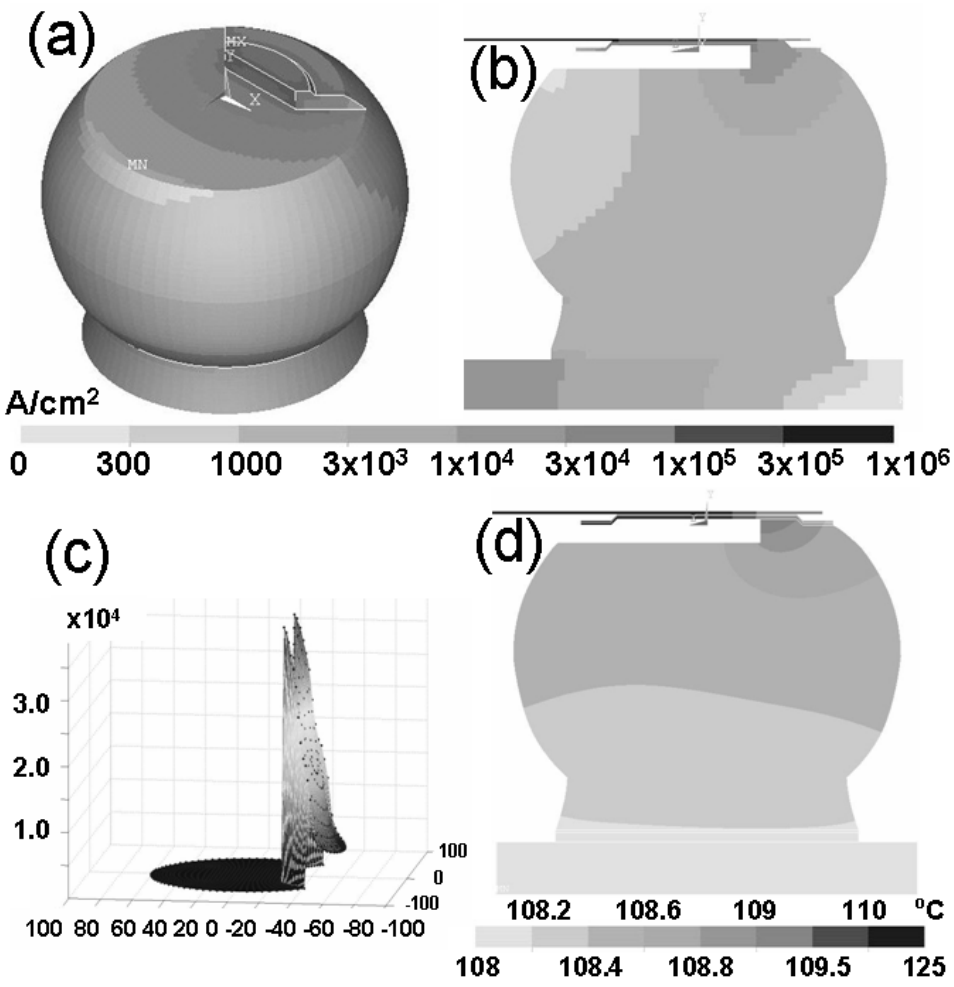


Figure 4-19: Current density redistribution in solder joints at Stage III. (a) Tilt view, shows solder bump only. (b) cross-sectional view of (a). (c) Current density distribution in solder adjacent to UBM/IMC layers. (d) Corresponding temperature distribution.

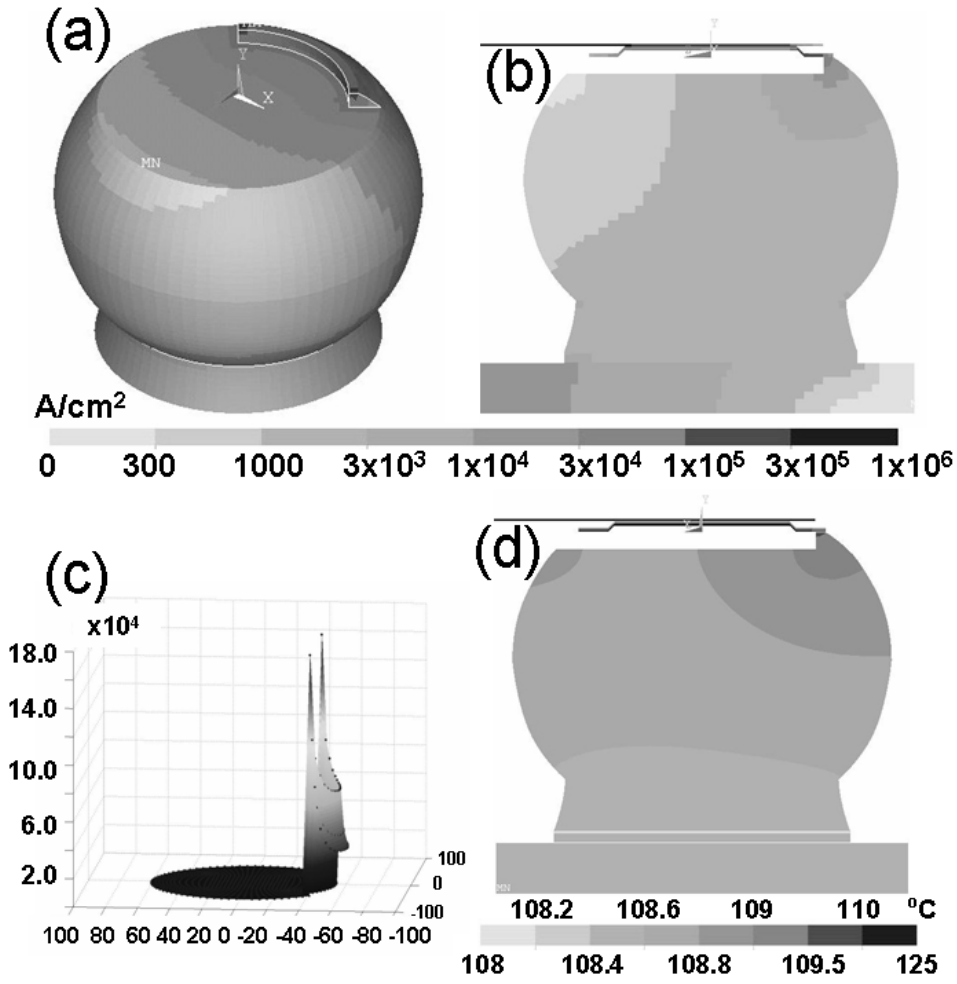


Figure 4-20: Current density redistribution in solder joints at Stage IV. (a) Tilt view, shows solder bump only. (b) Cross-sectional view of (a). (c) Current density distribution in solder adjacent to UBM/IMC layers. (d) Corresponding temperature distribution.

Table 4-4: The simulated maximum current density inside the solder, the corresponding crowding ratio as well as the bump resistance at each stage.

	Original bump	Stage I	Stage II	Stage III	Stage IV
Void proportion (area %)	0	28.8	50.0	80.5	96.0
Maximum current density inside solder (A/cm^2)	5.42×10^4	4.43×10^4	4.04×10^4	8.70×10^4	1.69×10^5
Bump resistance(mΩ)	11.2	14.6	19.0	25.3	42.9
Maximum temperature inside solder (°C)	109.6	109.5	109.3	109.4	110.4

4.4.2 Summary

In summary, we have employed 3-D finite elements method to simulate the current and temperature redistribution due to the formation and propagation of a pancake-shape void in solder joints during EM. It is proposed that current redistribution is the main reason of void formation and propagation, especially the propagation into the low current density region below the contact passivation. It was found that UBM provided a conducting path for current to go below the passivation, and it directed the current to the periphery of the solder joints, which is in agreement with the experimental observation of void formation in those regions. Increasing in temperature due to void formation was not significant since the major heat was from Al trace and the applied current was as low as 0.28 A.

4.5 Effect of the width of the Al trace on EM failure time

4.5.1 Results and discussion

Chiu *et al.* investigated the effect of the length of Al-trace on EM lifetime [81]. It was found that the length of Al-trace affected the Joule heating effect, while the current crowding effect remained the same for solder joints with Al traces of various lengths. They also reported that the length of Al-trace has significant influence on the EM failure time of solder joints. Thus, the width has substantial effect on the failure time of solder joints. It is quite common to use different widths of Al trace in packaging industry. However, such effect has not been verified by experimental results. In this study, we investigated the EM failure in SnAg3.5 solder joints with 40-μm-wide and 100-μm-wide Al-traces. The current crowding effect was calculated by using simulations. In addition, the TCR effect was employed as a temperature sensor to measure the real temperature under current stressing. This helped distinguish the Joule heating effect from current crowding effect in electromigration lifetime.

To investigate the effect of the width of Al-trace on electromigration, two test structures were adopted. The only difference between the two structures was the width of Al traces. One was 40 μm wide and the other was 100 μm wide. They were both 1.5 μm thick. During EM tests, a current of 0.5 A was applied on a 165 °C hot plate. The mean failure time for each structure was obtained by Weibull plot from five

samples. The resistance history was monitored using four point probes at Cu pads on the substrate side. The current was terminated by a computer program when the resistance of the stressing circuit exceeded 5×10^6 mΩ. An infrared microscope was utilized to examine whether there is any damage in Al trace, since Si is transparent to infrared.

The experimental results indicated that the width of Al-trace has significant influence on the failure time of the solder joints. In Figure 4-21, MTTF of the solder joints with 40-μm-wide and 100-μm-wide Al traces was 44.1 hrs and 250.1 hrs, respectively. Other parameters given from Weibull plot are listed in Table 4-5. Resistance history for the two sets of joints show similar behavior under current stressing. Figures 4-22 (a) and (b) illustrate the typical resistance curves of the solder joints with 40-μm-wide and 100-μm-wide Al traces, respectively. The initial resistance was 3210.8 mΩ and 1292.9 mΩ of the joints with 40-μm-wide and 100-μm-wide Al traces, respectively. The resistance included the resistance of six bumps, three segments of Al trace, and Cu lines in the substrate. Thus, the total resistance was higher of the joints with 40-μm-wide Al trace. The resistance increased slowly and almost linearly before 95% of the failure time as shown in the insets of Figures 4-22 (a) and (b). After that, the resistance increased abruptly until open-circuit failure occurred.

After EM failure, IR microscopy was employed to examine whether the damage occurred or not in Al traces. Figures 4-23 (a) through (c) show the plan-view radiance image of the solder joints with 40-μm-wide Al trace. The six bumps were situated directly below six Al pads. The electron flow in Al traces drifted from the left-hand side to the right-hand side. As seen in Figure 4-23 (a), some damages occurred in the Al pad of Bump 2, whereas no obvious damages were found in the Al traces connecting the bumps. However, in other samples, we also found damage in Al pads of Bump 4 or Bump 6, since electrons drifted from the chip side to the substrate side of the even-numbered bumps. Serious damage always occurred in Al pads of the even-numbered bumps in this study. Similar failure modes were found in Al pads for the solder joints with 100-μm-wide Al trace, as shown in Figure 4-24. Serious damage was observed in Al pad of Bump 6.

To observe the failure sites more clearly, the samples were ground and polished laterally for cross-sectional SEM examination. Figures 4-25 and Figures 4-26 show the cross-sectional SEM images for the solder joints with 40-μm-wide and 100-μm-wide Al traces, respectively. The arrows in SEM images indicate the directions of electron flow. For solder joints with 40-μm-wide Al trace, Bump 2 had severe damage and almost became open, which was consistent with the results of the infrared microscopy in Figure 4-23. On the other hand, for solder joints with

100-μm-wide Al trace, Bump 6 had the most serious damage among the bumps, which was also consistent with the infrared results in Figure 4-24. All bumps with electrons drifting down had void formation in the chip side. In addition, SEM results show that IMC was accumulated in the anode side due to the electron flow. When the electron current in the bump drifted downward (from the chip side to the board side), a smooth Cu_6Sn_5 layer was accumulated in the anode side on Cu pad due to polarity effect [82]. Moreover, serious column-type Cu_6Sn_5 accumulated in the anode in the chip side, especially close to the current crowding region. The supply of Cu atoms came from Cu pad on the substrate side. Huang *et al.* reported that Cu migrated in the molten solder under current stressing serious column-type Cu_6Sn_5 [83]. Similar behavior was found in this study. The solder may melt during the final 5% of the stressing time. Abundant Cu atoms would migrate in the melted solder joints. However, there was no serious column-type Cu_6Sn_5 formed in the solder joints with downward electron current. There are two possible reasons. First, the 5-μm Cu UBM in the chip side totally consumed before solder melting. There are not enough Cu atoms to migrate to the board side to form IMCs. Second, the temperature on the substrate side is lower than that on the chip side. The serious column-type Cu_6Sn_5 was formed near the current crowding region with higher temperature [84]. Therefore, IMCs formed in the anode/chip and anode/substrate ends of the solder joints are two

different morphologies.

In order to distinguish the current crowding effect from the Joule heating effect on failure time, the maximum current density and temperature in the solder joints need to be obtained. First, the maximum current densities in the solder bumps with Al traces of two widths were simulated by the finite-elements method. Figures 4-27 (a) and (b) show the cross-sectional view of current density distribution in the solder joints with a 40-μm-wide and 100-μm-wide Al traces, respectively. The current crowding effect occurred in the solder near the entrance point of Al trace. The maximum current density in the solder bump with a 40-μm-wide Al trace was 2.22×10^4 A/cm^2. The maximum value divided by the average current density on UBM opening, which is 4.42×10^3 A/cm^2, was denoted as the crowding ratio. The corresponding crowding ratio for the solder with a 40-μm-wide Al trace was 5.0. For the solder bumps with a 100-μm-wide Al trace, the maximum current density decreased to 1.79×10^4 A/cm^2. Thus, increasing the width of Al trace could reduce the maximum current density in solder bumps. This is because a wider Al trace renders a lower average current density in Al trace. Thus, the current density before going into the contact opening was smaller, leading to a smaller current density in the solder bumps.

To measure the real temperature of the solder bumps during current stressing,

TCR effect of the stressing circuit was used as a temperature sensor in the package. Figure 4-28 shows the relationship of the measured resistance as a function of oven temperature for the two widths. The measured resistance included a segment of Al trace, two solder bumps, and some Cu lines in the substrate. However, most of the resistance came from Al trace due to its small cross-section. Thus, TCR effect had its original mainly from Al traces. Since Al traces were connected to the solder bumps, the real temperature in the solder bumps was close to the temperature in Al trace. The 0.2-A current was chosen because Joule heating under this current increased less than 2 °C as measured by the infrared microscopy. The fitting equations for the two curves in Figure 4-28 are:

$$R_{40} = 563.0 + 2.27\ T \quad (4.5)$$

$$R_{100} = 236.5 + 0.96\ T \quad (4.6)$$

where R_{40} and R_{100} represent the resistance of the stressing circuit with 40-μm-wide and 100-μm-wide Al traces, respectively, and T is the real solder temperature.

By using the fitting equations, the real temperature in solder bumps could be measured when the circuit was applied by 0.5 A on a 165 °C hotplate. The resistances were 1058.2 mΩ and 401.3 mΩ for the solder bumps with 40-μm-wide and 100-μm-wide Al traces, respectively. Thus, the real temperature in the solder was estimated to be 218.2 °C and 172.2 °C of the solder bumps with 40-μm-wide and

100-μm-wide Al traces, respectively.

The different current crowding and Joule heating effects on failure time could be estimated by using Black's equation. We plugged in the simulated maximum current density as j and measured temperature as T in the Black's equation. Moreover, the values of n and activation energy were set to be 2 and 0.7 eV, respectively. The estimated MTTF ratio for the solder joints with 100-μm-wide Al trace to that with 40-μm-wide Al trace was about 8.2, where current-density difference contributed 1.5 times and the temperature variation contributed 5.5 times. The experimental MTTF ratio was about 5.7. Thus, higher Joule heating effect serves as the major reason for the short failure time of solder joints with 40-μm-wide Al traces in this study. Compared with that for solder joints with 100-μm-wide Al trace, the temperature increase in solder bumps was 46 °C higher in the bumps with 40-μm-wide Al trace. Owing to the exponential term in Black's equation, the increase in temperature has pronounced influence on the MTTF of solder joints. On the other hand, the difference in current crowding effect has no substantial influence on MTTF of bumps in the present case. However, if thin-film UBM structure is adopted for the joints, the different current crowding effect may have obvious influence on MTTF of the joints.

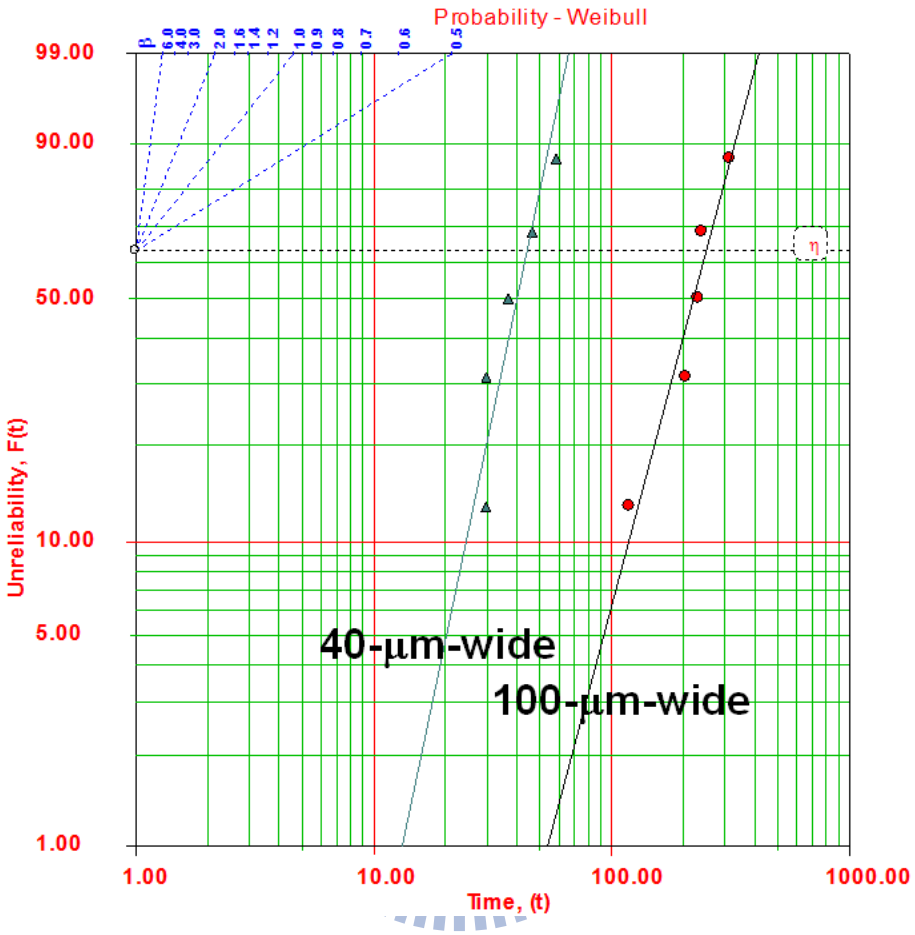


Figure 4-21: Weibull distribution of the flip-chip solder joints with 40-µm-wide and 100-µm-wide Al traces.

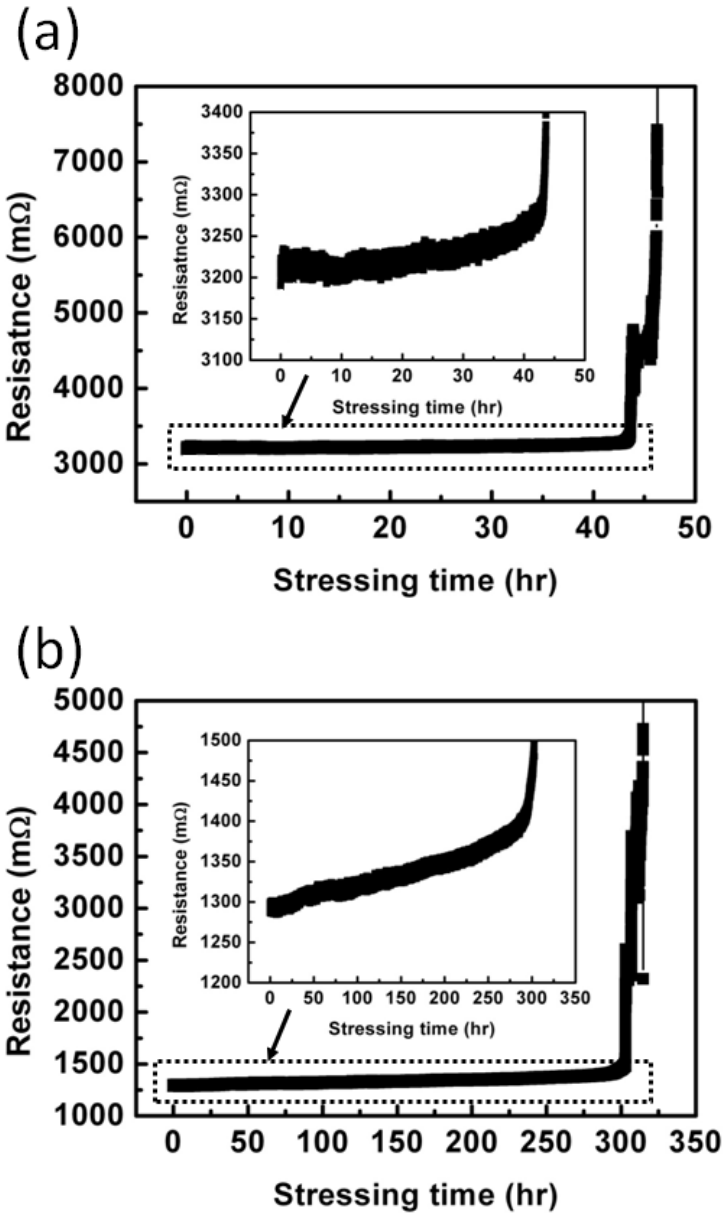


Figure 4-22: (a) Changes in resistance of the six solder joints with 40-μm-wide Al trace during electromigration tests. (b) Changes in resistance of the six solder joints with 100-μm-wide Al trace during electromigration tests. The insets in Fig. 2(a) and 2(b) show the enlargement of the resistance curve up to 95% of the failure times.

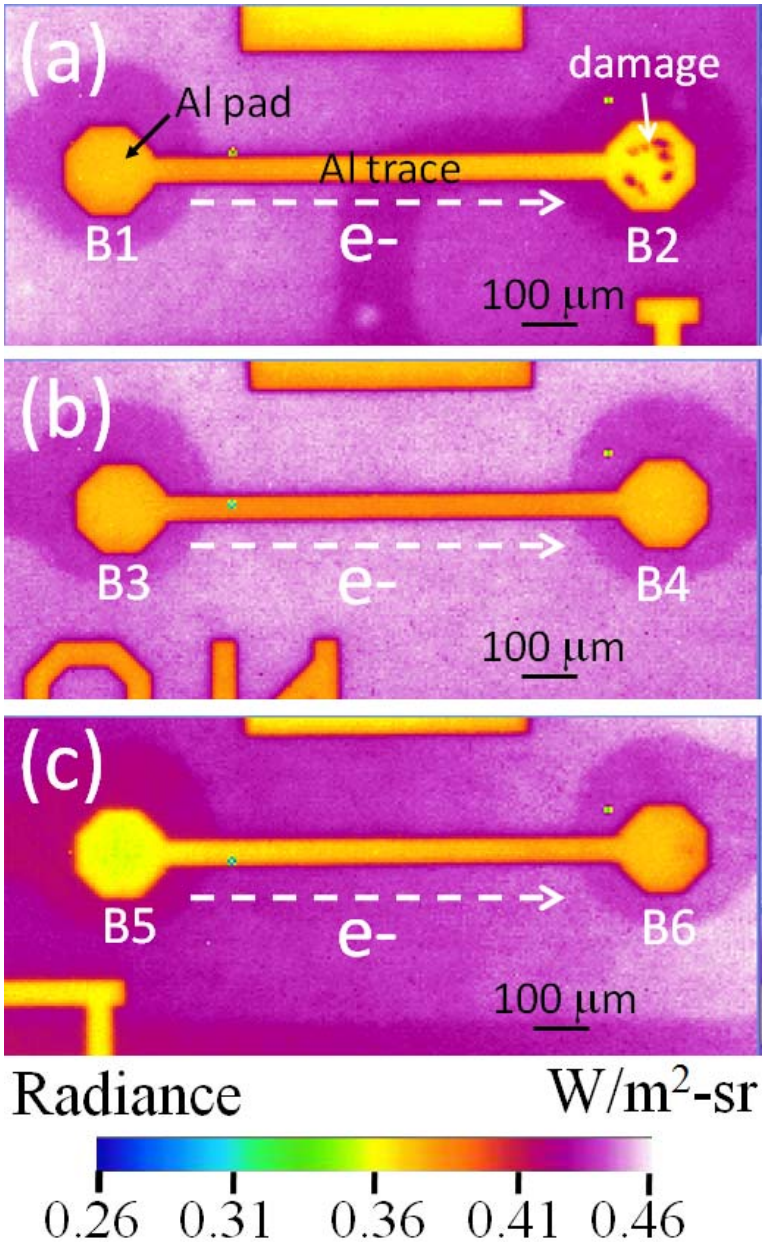


Figure 4-23: Plan-view radiance-mode IR images of 40-μm-wide Al trace after 0.5 A current stressing at 165 °C. (a) First segment of Al trace. A serious damage occurred in Al pad of Bump 2. (b) Second segment of Al trace. (c) Third segment of Al trace.

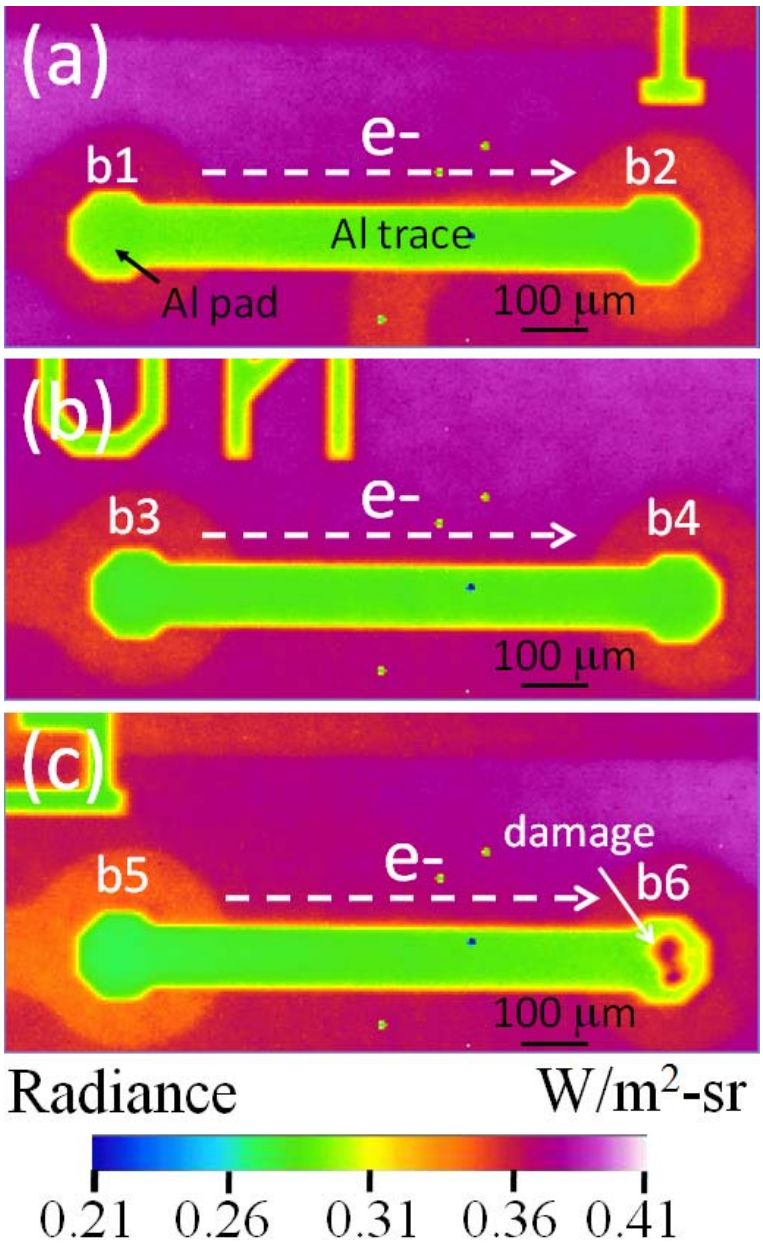


Figure 4-24: Plan-view radiance-mode IR images of 100-μm-wide Al trace after 0.5 A current stressing at 165 °C. (a) First segment of Al trace. (b) Second segment of Al trace. (c) Third segment of Al trace. A serious damage occurred in the Al pad for Bump 6.

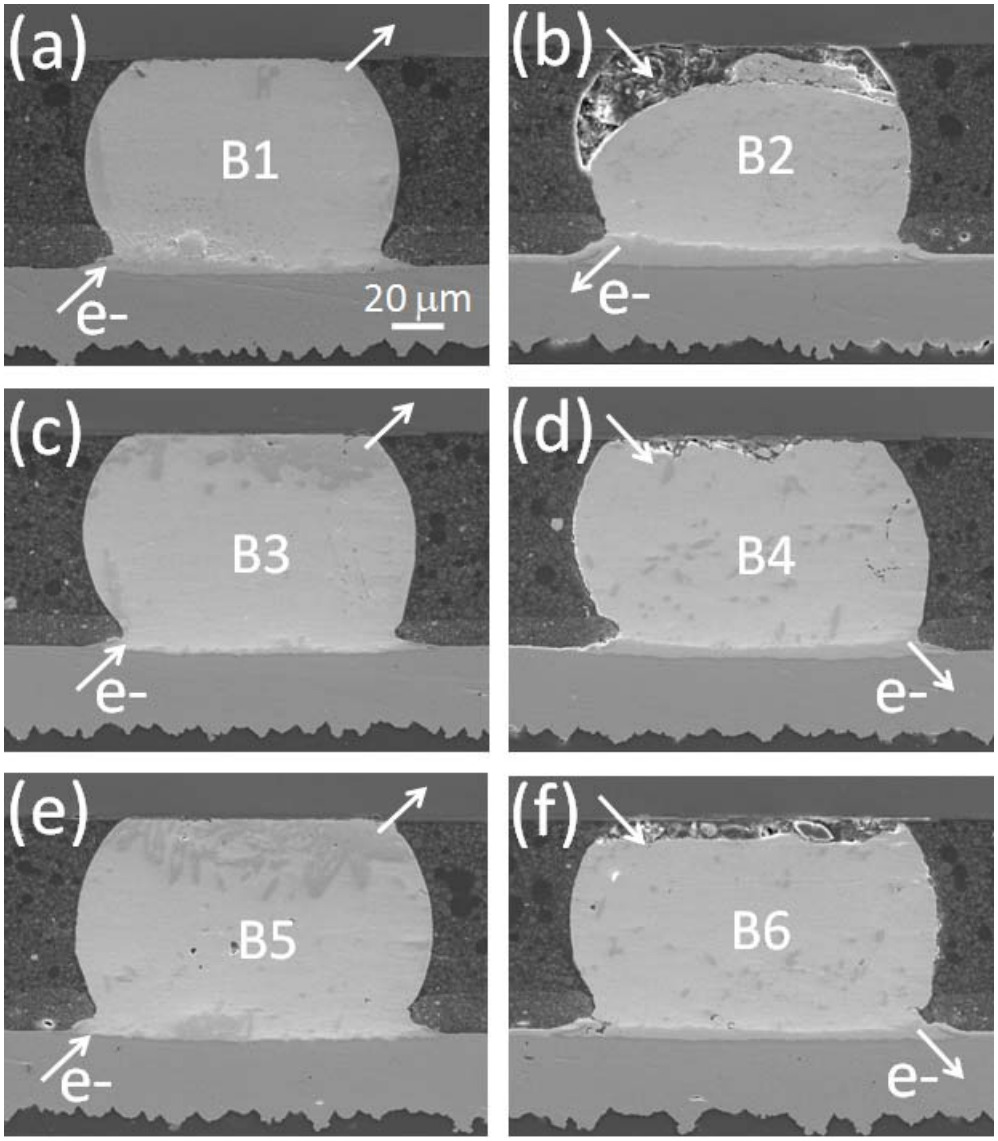


Figure 4-25: Cross-sectional SEM images of six bumps with 40-μm-wide Al trace after 0.5 A current stressing at 165 °C. (a) Bump 1 with upward electron flow. (b) Bump 2 with downward electron flow. Large voids were found in the chip side. (c) Bump 3 with upward electron flow. (d) Bump 4 with downward electron flow. (e) Bump 5 with upward electron flow. (f) Bump 6 with downward electron flow.

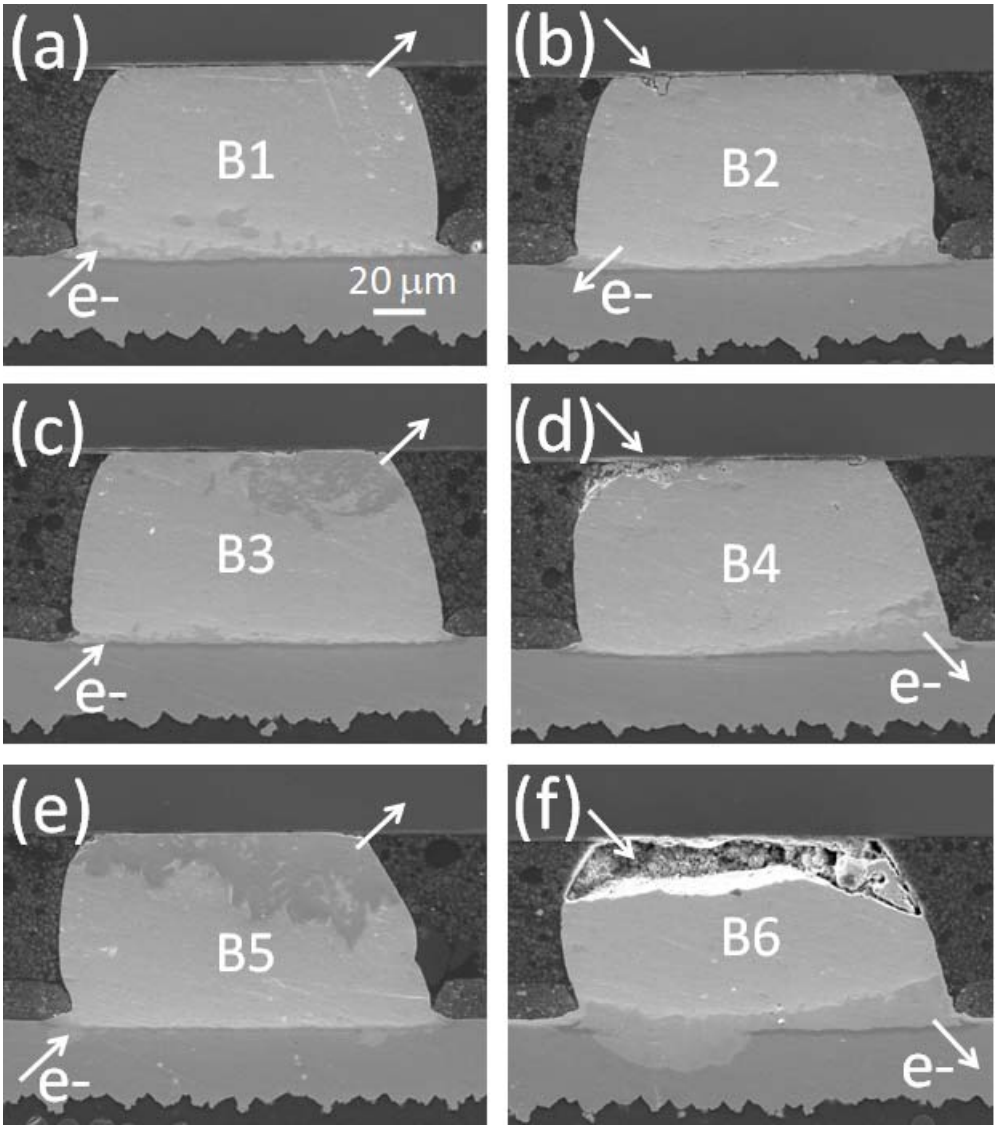


Figure 4-26: Cross-sectional SEM images of six bumps with 100-μm-wide Al trace after 0.5 A current stressing at 165 °C. (a) Bump 1 with upward electron flow. (b) Bump 2 with downward electron flow. (c) Bump 3 with upward electron flow. (d) Bump 4 with downward electron flow. (e) Bump 5 with upward electron flow. (f) Bump 6 with downward electron flow. This bump has the most severe damage among the six bumps.

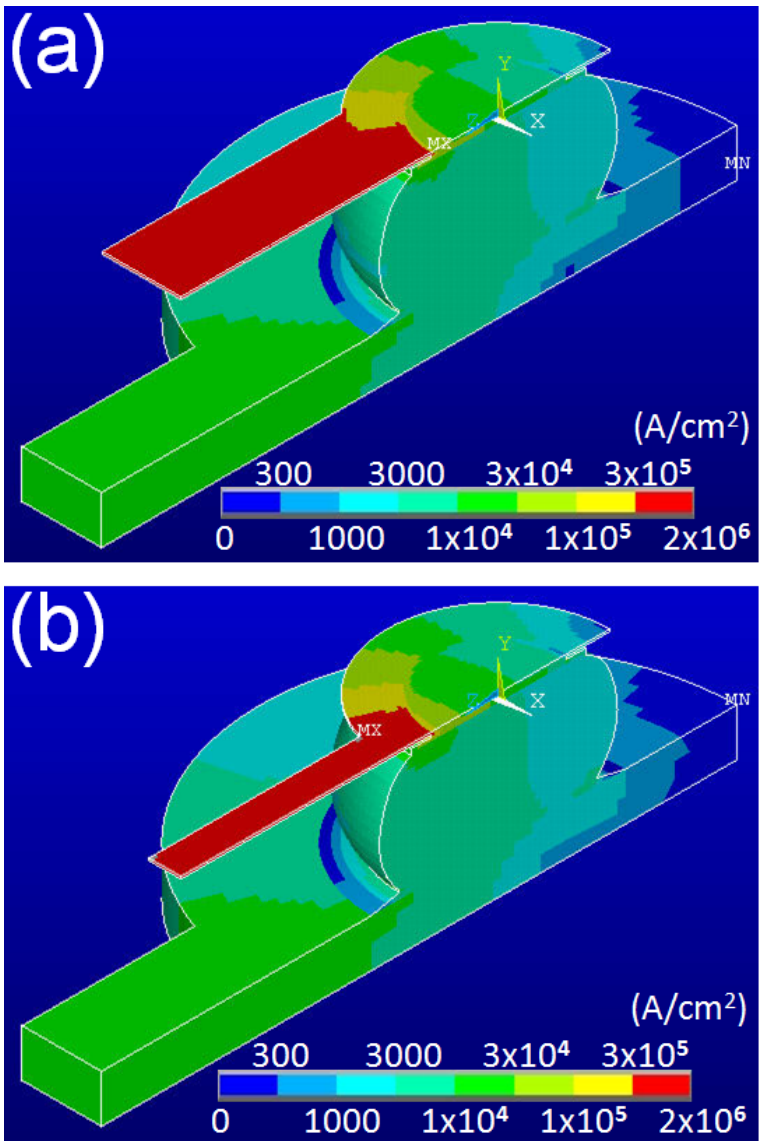


Figure 4-27: Tilted view of cross-sectional current-density distribution in the solder bumps. (a) With 40-μm-wide Al trace. (b) With 100-μm-wide Al trace when they were stressed by 0.5 A.

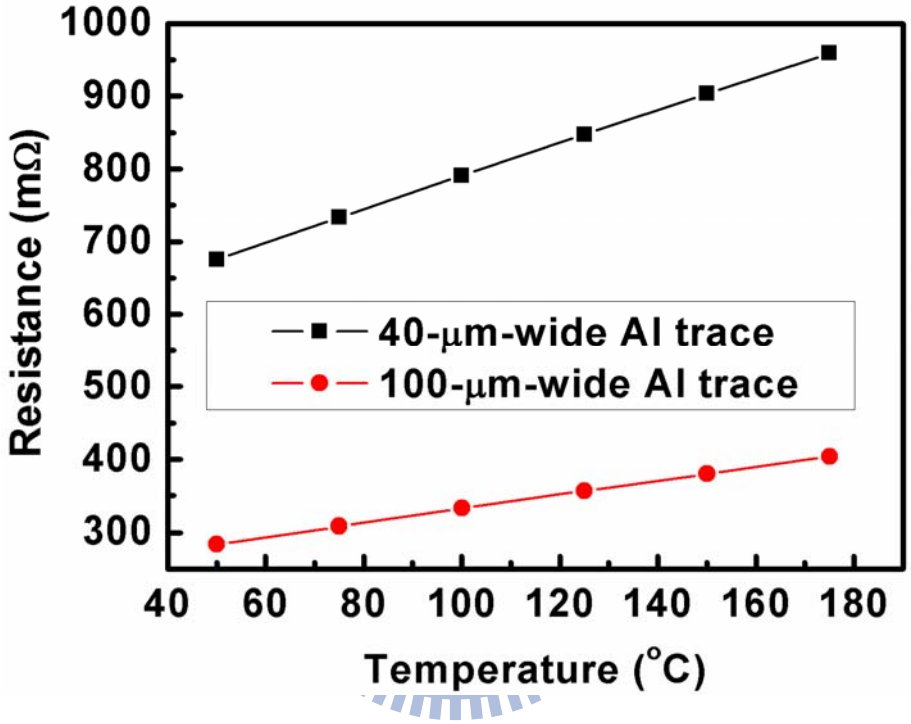


Figure 4-28: Changes in resistance as a function of oven temperature. (a) For solder joints with 40-μm-wide Al trace. (b) For solder joints with 100-μm-wide Al trace.

Table 4-5: Electromigration reliability

Width of Al trace	β (slope)	η (MTTF)	ρ (correlation)
40 μm	3.8	44.1	92.5%
100 μm	3.0	250.1	96.7%

4.5.2 Summary

The effect of Al-trace width on EM of flip-chip solder joints was investigated experimentally in this study. For the same stressing condition, 0.5 A on a 165 °C hotplate, the solder joints with larger width has longer EM lifetime. The average failure time was 44.1 h and 250.1 h for the solder joints with 40-μm-wide and 100-μm-wide Al traces, respectively. It was found that both different current crowding and Joule heating effects contribute to the difference in failure time. As described by Black's equation, these two factors will affect the lifetime of the solder joint. According to the simulation results, slightly higher current crowding effect occurs in solder joints with a 40-μm-wide Al trace than that with a 100-μm-wide Al trace. In addition, higher Joule heating effect occurs of joints with a 40-μm-wide Al trace due to larger resistance of the stressing circuit. By using TCR effect of the stressing circuit, the real temperature in the solder joints can be obtained. It is verified that the different Joule heating effects serve as the main contributor for the different failure times of solder joints with different widths of Al trace.

4.6 Effect of Al-trace degradation on Joule heating during EM tests

4.6.1 Results and discussion

Several studies investigated the failure mechanism in flip-chip solder joints during EM test. It is frequently reported that there is a dramatic increase in temperature at later stages of EM test that caused the melting of the solder bumps [25, 85-87]. Melting may happen in the whole solder bump or in the solder adjacent of Al trace. Tsai *et al.* explained that the solder was melted because of two reasons: one is the increase in resistance due to void formation, and the other is the local current crowding effect [87]. Huang *et al.* proposed that the void formation due to EM would block the heat dissipation of solder joints and the temperature increases as the voids are formed [25]. Yet, in our previous study, the simulation results show that the temperature increases only by a few degree Celsius due to void formation and propagation, even when the voids deplete 95% of the under-bump-metallization (UBM) opening [Section 4.4]. The experimental observation of solder melting revealed that Joule heating occurs seriously in later stages of EM. However, the mechanism of this serious Joule heating remains unclear.

To one's surprise, open failure occurs in Al trace instead of inside solder bumps under this stressing condition. Figure 4-29 (a) shows IR radiant image before current stressing at 100 °C. The radiance of Al trace was smaller than that of the underfill.

Thus, it appeared brighter in the image. Al trace can be clearly seen, and the two solder joints subjected to current stressing were labeled as Bump 1 and Bump 2. The two bumps were directly below the circular Al pads. After stressed by 0.6 A at 100°C for 25 hours, Al trace near Bump 2 shows a discontinuous image, as indicated by the solid arrow in the Figure 4-29 (b). The direction of the electron flow was also indicated by the dashed arrows in the figure. Al trace might become open there. The failure may occur either in the anode or cathode end of Al trace.

The solder bumps melted after failure, as shown in the cross-sectional SEM images in Figure 4-30. The bumps were polished to approximate the center area. Damage was found in Bump 2, where electron drifted from the chip side to the substrate side. In addition, the Pb-rich phase in both bumps became finely dispersed. This microstructure indicated that both solder bumps melted completely upon failure, i.e., the temperature was over 183 °C. This melting behavior demonstrates that serious Joule heating occurred before failure.

To investigate the mechanism of the abrupt rise in temperature before failure, the change in resistance of the whole stressing circuit was also monitored during the EM test as shown in Figure 4-31. The initial total resistance was 3.0 Ω, which included the resistance of Al trace on Si chip, Cu lines on BT substrate, and the external Cu lines added for current stressing. The resistance for Al trace was about 1.5 Ω before current

stressing. As stressing time increased, the total increased slowly to 3.2 Ω at 91500 s, which was about 90% of the failure time. The temperature rose abruptly after 91500 s, and it increased over 4.2 Ω upon failure. Since Al trace was found to be open after failure, it is speculated that EM damage also occurred in Al trace, and degradation of Al trace may be responsible for the abrupt rise in temperature.

To verify if the increase in resistance of Al trace can have substantial influence on Joule heating effect, 3D thermo-electric simulation was carried out with and without considering the increase in resistance in Al trace. Figure 4-32 (a) shows the changes in hot-spot temperature in solder due to void formation when stressed at 0.6 A at 100 °C without considering the damage in Al trace. The hot-spot temperature was 137.5 °C, which means that the Joule heating effect increased the temperature in the solder bump by 37.5 °C. The hot-spot temperature decreased in the beginning as the voids grew, and it increased at later stages. Nevertheless, the increase in temperature was only less than 5 °C even though the voids depleted about 95% of UBM opening, because the increase in bump resistance was less than 100 mΩ. These results are consistent with our previous findings even at a different stressing condition [Section 4.4]. As a result, void formation and propagation cannot explain the dramatic rising temperature in solder at later stages.

It is worth mentioning that the maximum temperature in Al trace was as high as

217 °C at the initial stage of EM. Furthermore, the corresponding current density in Al trace was as high as 1.2×10^6 A/cm^2. Therefore, EM in Al could occur under this stressing condition [72, 88]. On the other hand, the current density in Cu lines was only 3.0×10^4 A/cm^2, and the temperature was about 130 °C. Thus, EM would not initiate in Cu lines in BT substrate [89, 90]. In addition, the stressing circuit outside the package had even larger cross-section than that of Cu line. Thus, damage may not occur in the external circuit. Consequently, it is reasonable to assume that the huge increase in resistance of 1.2 Ω at later stages of EM is mainly attributed to the EM damage of Al trace. Thus, the resistance of Al trace was increased accordingly by adjusting Al resistivity in the simulation model. Figure 4-32 (b) shows the hot-spot temperature in the solder bumps as a function of Al resistance without considering void formation, and it was found that the temperature increased significantly as the resistance of Al trace increased. In particular, the temperature exceeded the melting point of solder when the resistance of Al trace increased from 1.5 to 3.5 Ω. On the other hand, the maximum temperature in Al trace also increased from 217 °C to about 390 °C when the resistance of Al trace increased from 1.5 to 3.5 Ω, which also accelerated the EM in Al trace.

There exists a discrepancy in the change in resistance required for the temperature in solder to exceed 183 °C in the experimental observation and

simulation results. In the experiments, an increase in resistance of approximately 1.2 Ω was detected upon failure as seen in Figure 4-31, and the solder melted after failure. However, in the simulation model, it required an increase in resistance of about 2.0 Ω to do so. This discrepancy may be attributed to the fact that the resistance right before failure was not recorded. In Figure 4-31, the last point of resistance was 4.2 Ω, and it jumped above 1000 Ω for the next point, which was not shown. The time span between the two points was 10 seconds, which implies that the resistance may exceed 4.2 Ω, i.e. the increase in resistance right before failure could be larger than 1.2 Ω.

Aluminum EM may occur quite often during the accelerated EM of flip-chip solder joints. The width of Al trace was only 34 μm for the samples used in this study. Typically, it is 100 μm wide and 1.5 μm thick, and the stressing currents range from 0.5 A to 2.0 A. The current density in Al trace reaches 8×10^5 A/cm^2 with the applied current of 1.2 A. As for the stressing temperature, the ambient temperature may be elevated to 150 °C or higher, especially for Pb-free solders. Thus, the real temperature in Al trace may exceed 200 °C easily if the Joule heating effect is considered. In fact, we also observed similar results for Al trace of 100 μm wide and 1.5 μm thick when stressed by 0.75 A or higher. The above results indicates that EM in Al trace cannot be ignored during the EM test of solder joints, and the testing conditions should be cautiously chosen in order to avoid it.

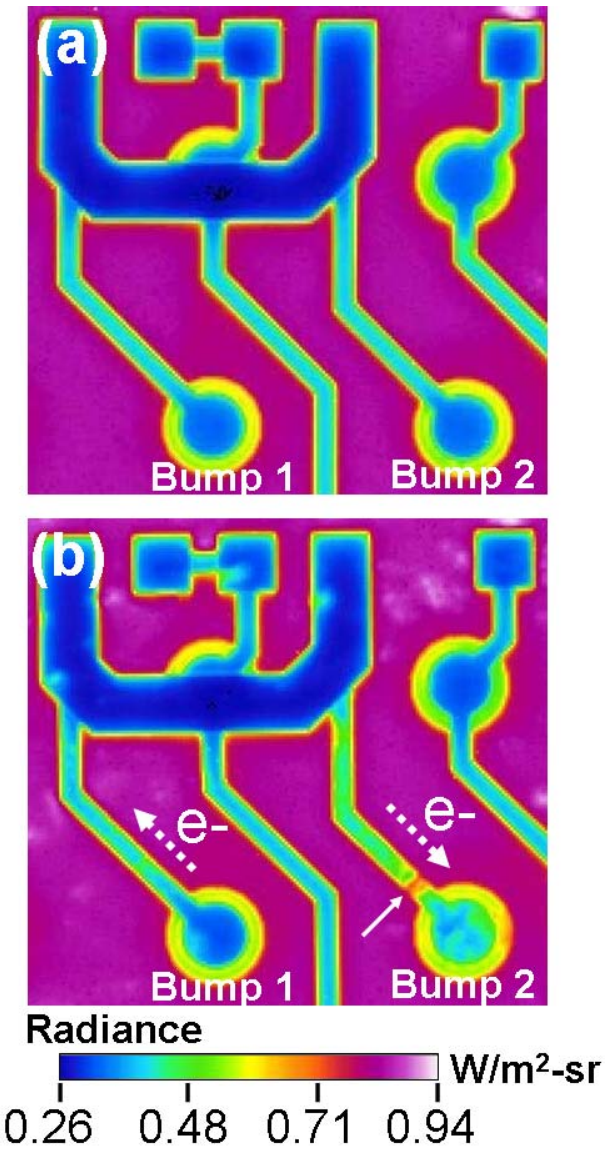


Figure 4-29: Plan-view radiance-mode IR images of Al trace. (a) Before current stressing. (b) After stressing for 25 hours. Open failure was found in Al trace near Bump 2.

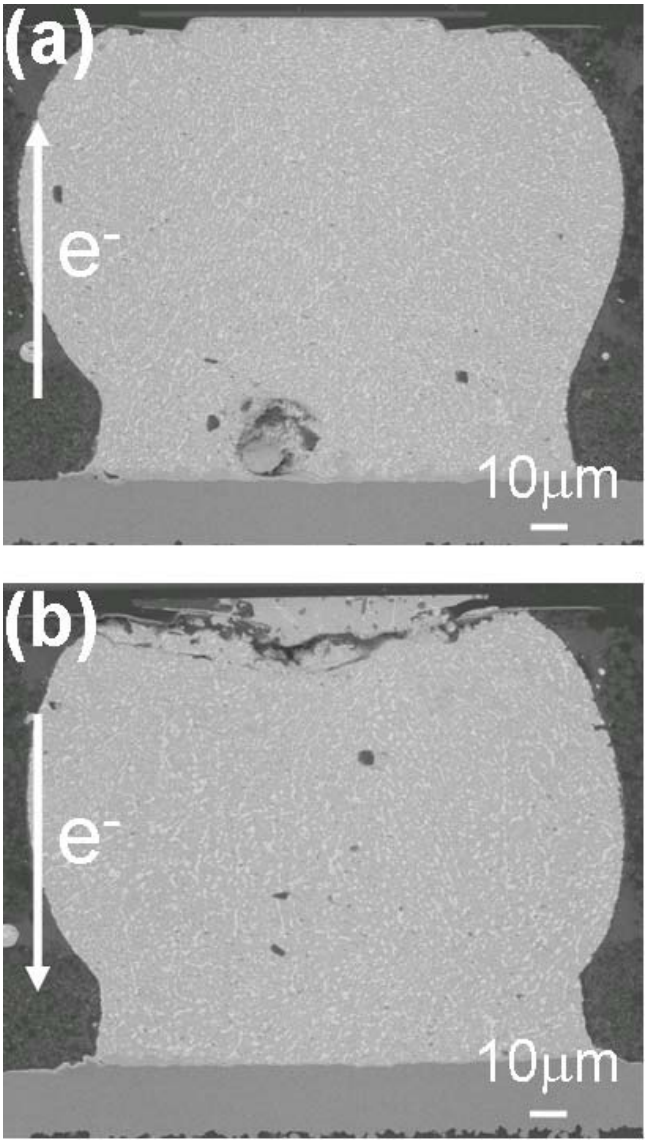


Figure 4-30: Cross-sectional SEM images of the solder bumps after open failure for (a) Bump 1. (b) Bump 2. Melting behavior occurred in both bumps and EM damage was observed at the chip side of Bump 2.

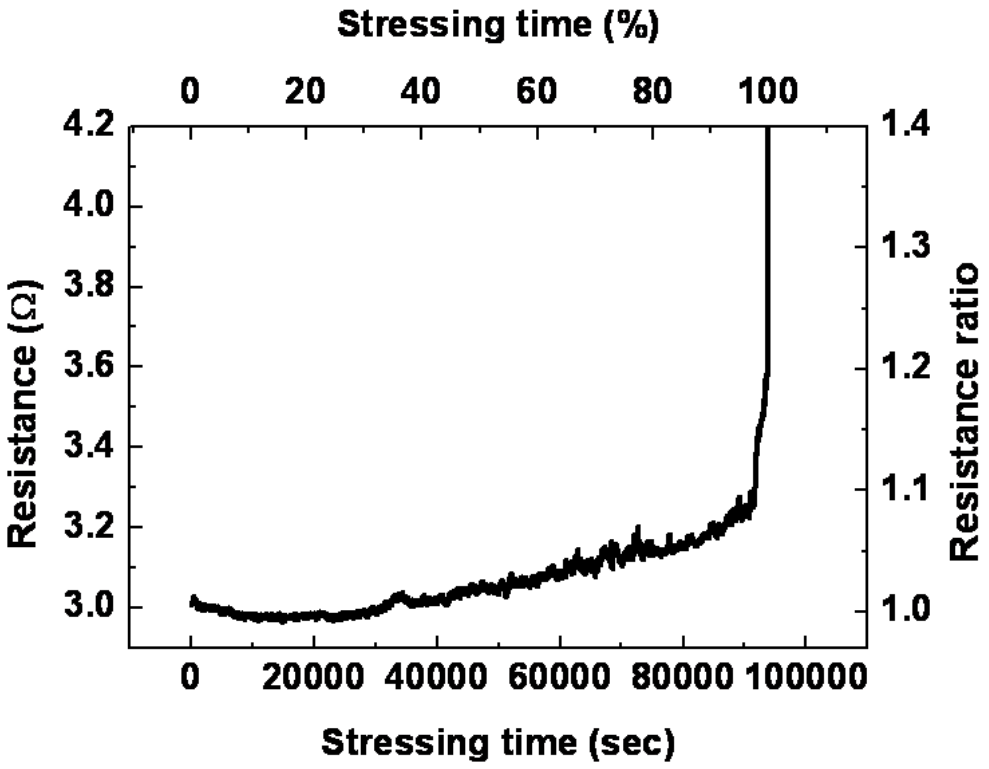


Figure 4-31: The measured resistance of the stressing circuit as a function of stressing time. Abrupt increase in resistance took place at later stages of EM.

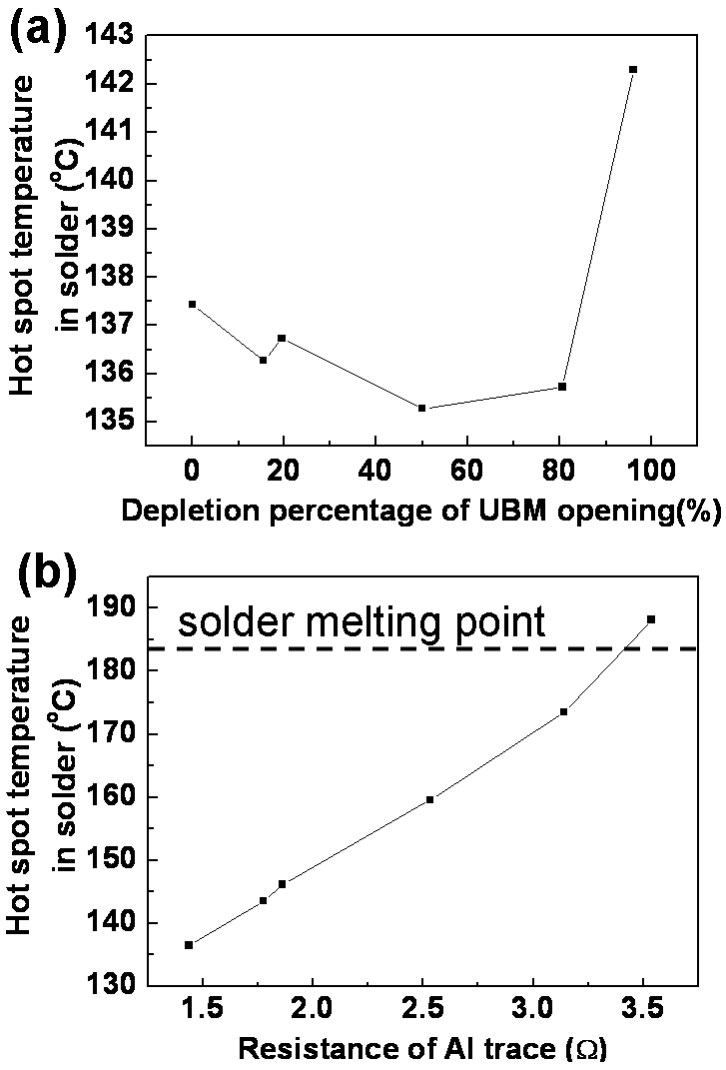


Figure 4-32: (a) The hot-spot temperature in the solder bumps as a function of the depletion percentage of UBM opening due to void formation; (b) The hot-spot temperature in the solder bump as a function of the resistance of Al trace. Formation of voids was not considered in these results.

4.6.2 Summary

The mechanism of dramatic Joule heating effect at later stages of EM in flip-chip solder joints has been studied by using IR microscopy and 3D thermo-electrical simulation. It was found that EM also occurred in the Al trace under stringent stressing conditions, resulting in a resistance in Al trace. Since the major heating source in the stressing circuit is Al trace, degradation of Al trace caused serious Joule heating at later stages of EM. This model can explain the observed abrupt rise in temperature in the solder bumps before failure.

4.7 Non-linear behavior of thermal gradient during current stressing

4.7.1 Results and discussion

In 2003, Ye *et al.* has reported the linear temperature distribution across the solder bumps under current stressing [18]. Later, Lai *et al.* investigated the electrothermal coupling analysis in flip-chip solder joints under current stressing [91]. It was found that the shape of the simulation model is close to the real solder bumps. The temperature distribution was quite non-uniform since scalar bar is linear scale. Also, when the solder become smaller, there exists the hot spot in the solder joints as reported by Wu *et al* [92]. The most important thing is that the temperature distribution across the solder joints can be monitored by IR microscopy [84]. The non-linear distribution of thermal gradient across the solder bumps was found. Moreover, the linear or non-linear distribution of thermal gradient would affect the analysis of the thermomigration. In this section, three-dimension simulation was used to analyze the distribution of thermal gradient and explain how non-uniform temperature distribution occurred in the solder bumps.

To confirm the thermal gradient is non-linear distribution, the cross-sectional flip-chip solder joints was prepared to face the cut surface of the IR detector. In Figure 4-33 (a), the temperature distribution in the solder joints was clearly measured. Figure 4-33 (b) is the temperature distribution which was plotted along the line profile

from A point to B point as labeled in Figure 4-33 (a). Surprisingly, non-linear thermal gradient distributed across the flip-chip solder joints under current stressing.

The simulation model with two segments of Al trace connected three solder joints was employed to discuss the non-linear distribution of thermal gradient in the solder bumps. As shown in Figure 4-34 (a), the three-dimensional current density distribution of the circuit was illustrated. The current comes from Cu line of Bump 1 and then pass through Al trace of Bump 2. The current crowing effect occurred in the Bump 1 as discussed before owing to the line-to-bump geometry. Nevertheless, there are almost no currents entering Bump 2 since the blue-color region is filled with Bump 2. For the temperature distribution in Figure 4-34 (b), the well-known Joule heating effect, the high current density region occupied Al trace to be the heat source of the whole system. Therefore, high temperature region, the red-color region, spread in Al trace.

As shown by the cross-sectional temperature distribution of Bump 1 displayed in Figure 4-35 (a), the hot spot clearly exists in the current crowding entrance. Now, three paths of thermal gradient from chip side to board side have been defined as V1, V2 and V3. They are shown in Figure 4-35 (b). The thermal gradient of V1 is non-linear distribution which is very similar to the experiment. The thermal gradient of V2 is linear distribution since the current bypass on top of it. For the thermal

gradient of V3, even the temperature near the chip side is a little bit lower than that in the solder bump. However, in Figures 4-36 (a) and (b), whole Bump 2 distributed as a linear profile.

The heating and current crowding effect played crucial roles for the non-linear distribution in the flip-chip solder joints under current stressing. For the typical type of Bump 1, the heating source comes from the entrance of Al trace. Also the current crowding effect caused the local Joule heating near there. These two combined reasons induced the hot spot in the solder joints. However, the heat need to be dissipated in the solder bumps. Therefore, the temperature distribution in the solder joints with current crowding effect led to the non-linear thermal gradient. Yet, for Bump 2, the heating source is almost the whole Al pad. The heat conduced uniformly into the solder joints. Thus, the temperature become linear distribution in the solder bumps.

Consequently, the non-linear thermal gradient prevailed in the solder joints when the current crowding effect is in it. The definition of the thermal gradient seems needs to be modified. Otherwise, the flux of thermomigration might have some underestimation. From these results, the extreme high thermal gradient would happen at the upper part of the solder bumps.

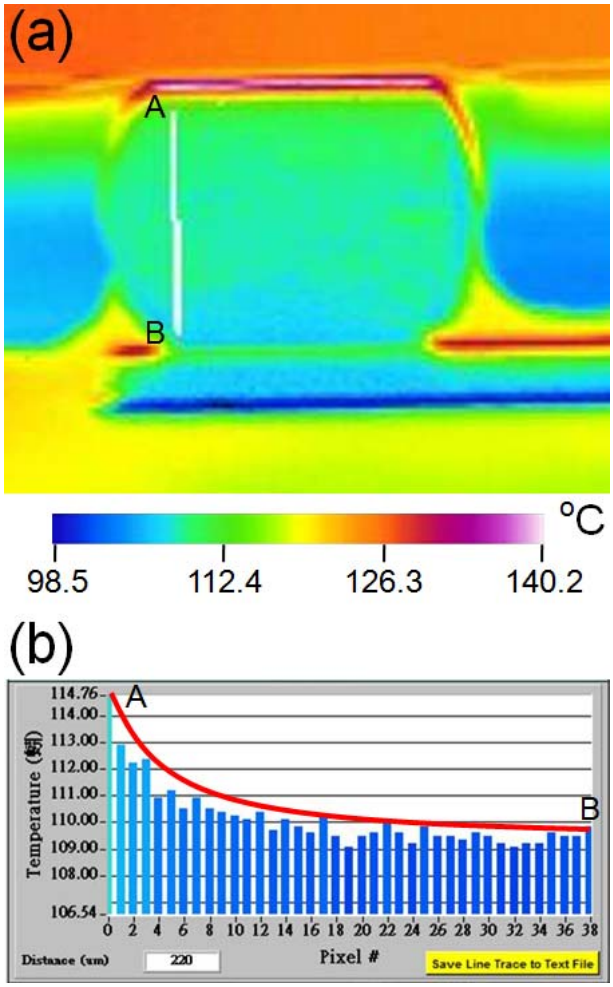


Figure 4-33: (a) IR images shows the temperature distribution. (b) The temperature profiles along the dashed lines in the solder bumps. The red line shows the non-linear distribution of the thermal gradient.

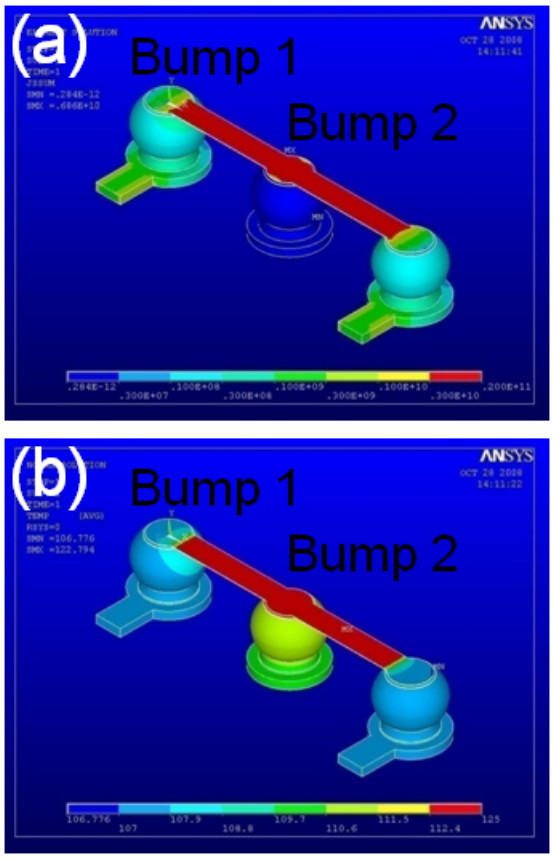


Figure 4-34: (a) Tilted view of three-dimensional current-density distribution in the whole circuit. (b) Tilted view of three-dimensional temperature distribution in the whole circuit.

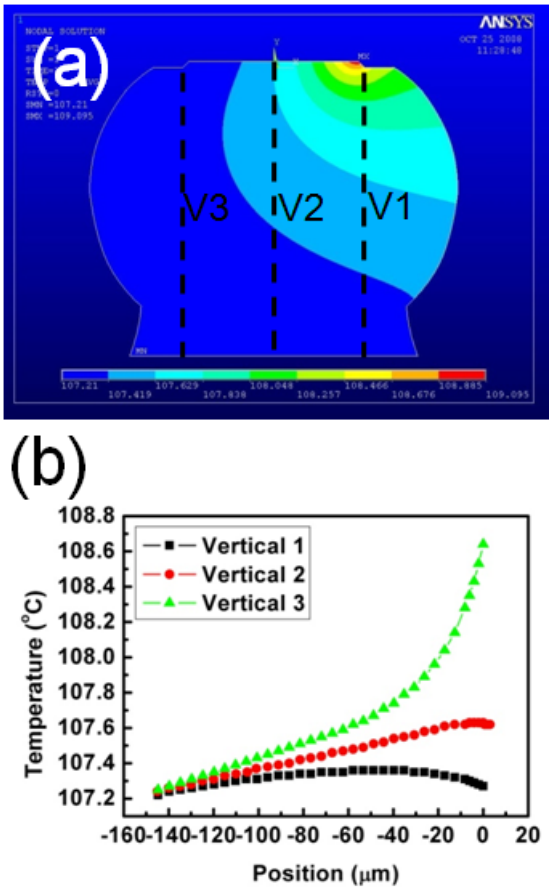


Figure 4-35: (a) The cross-sectional temperature distribution in Bump 1. (b) Three corresponding temperature profiles as defined in (a).

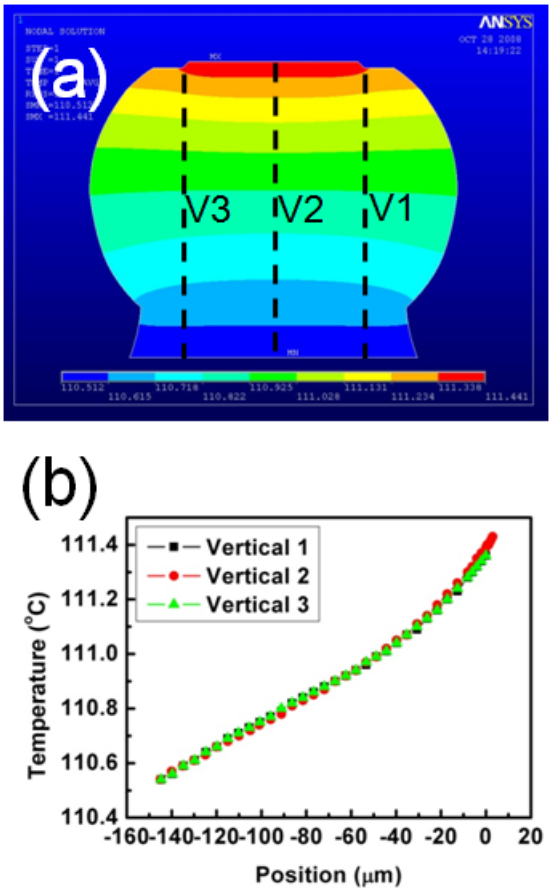


Figure 4-36: (a) The cross-sectional temperature distribution in Bump 2. (b) Three corresponding temperature profiles as defined in (a).

4.7.2 Summary

In summary, the non-linear temperature distribution was found both in experiment and simulation. The reason for the non-linear thermal gradient is due to current crowding effect, creating a point heat source. For the non-linear distribution, the thermal gradient in the solder joints might needs to be modified. The thermal gradient is higher in the upper part of the solder bump than the lower solder bump.

Chapter 5 Methods for enhancing EM resistance

5.1 Optimal structures for enhancing EM resistance

Form the Section 3.1, the CAE by ANSYS simulation software can also be used to provide the prediction of the optimal manufacture design in flip-chip solder joints on reliving current crowding and Joule heating effects. Since the current density and temperature in the solder joints cannot be measure directly, they can be obtained by finite-elements method on thermo-electrical simulation. In the following section, better designs will be proposed to relieve the current crowding and Joule heating effects to enhance the EM resistance. Later, the estimated Black's equation will be used to calculate the enhance ratio on MTTF.

5.1.1 UBM resistivity

The first method of suppressing the current crowding effect in this section was to use a resistive UBM layer. In this simulation, we simulated four solder joints with 295 μΩ·cm, 1477 μΩ·cm, 2954 μΩ·cm and 14770 μΩ·cm, which corresponded to 10, 50, 100 and 500 times the UBM resistivity of the Al/Ni(V)/Cu thin film UBM. Figures 5-1 (a) through (d) show the 3-D distribution of current density in the solder joints for the four models, respectively. It was found that the current density redistributed in the contact opening. With the increase in UBM resistivity, a greater amount of current traveled further along Al pad before flowing down into the contact opening. In addition,

the current density distribution in the top layer of the solder became more uniform as UBM resistivity increased. Figure 5-2 shows the current density distribution inside the top layer of the solder along Z-axis. The current became uniformly distributed inside the solder layer, and maximum current densities ranged from 7.01 to 1.55×10^4 A/cm^2. The corresponding crowding ratios are 14.0, 7.4, 5.4, and 3.1 for the solder joints with UBM resistivities of 295 μΩ·cm, 1477 μΩ·cm, 2954 μΩ·cm and 14770 μΩ·cm, respectively, as listed in Table 5-1. Furthermore, the current distribution in the UBM, IMC layers, and in the solder bump also became more uniform when using highly resistive UBM layers.

Since the insertion of the resistive layers may increase the bump resistance and thus cause higher Joule heating in the solder joints, thermal simulation was performed to examine temperature distribution in the above models. Figures 5-3 (a) through (e) show the temperature distributions in the solder joints with 29.5 μΩ·cm (standard model), 295 μΩ·cm, 1477 μΩ·cm, 2954 μΩ·cm and 14770 μΩ·cm UBM, respectively. The solder joints were applied by 0.567 A and the bottom of BT substrate was maintained at 70 °C. For the standard model in Figure 5-3 (a), the average temperature in the solder bumps was 94.5 °C, which was obtained by averaging the temperatures in the white dotted line in the figure. The solder near the entrance area of Al trace has higher temperature of 98.8 °C. As the resistivity of the UBM increased, Joule heating

effect became significant, as shown in Figures 5-3 (b) through (e). The temperature increase due to Joule heating was as large as 30.7 °C for the solder joints with 14770 μΩ·cm UBM. However, the current flowing in the solder joints is generally less than 0.2 A during device operation. Figure 5-3 (f) shows the temperatures in the solder joints as a function of applied current up to 0.567 A. It is found that Joule heating effect was not serious under 0.2 A. For the standard model, the temperature increase was 2.2 °C, whereas it was 2.8 °C for the solder joints with 14770 μΩ·cm UBM. It indicates that the temperature increase due to the resistive UBM was only 0.6 °C at 0.2 A.

Figure 5-4 depicts the crowding ratios at cross sections Y1 to Y6 for the above four methods in which cross-section Y1 is located inside the UBM layer, cross-section Y2 represents the IMC layer, cross-section Y3 is located in the top layer of the solder joints connecting to the IMC, and cross-section Y4 is situated near the middle of the solder joints, which has the largest cross-section of 184 μm in diameter. Cross-section Y5 is situated between the middle and the bottom of the solder, which has a necking due to the necessity of there being a solder mask, and cross-section Y6 represents the bottom of the solder joints close to the Ni_3Sn_4 IMC on the substrate side. It is clear that the crowding ratios in the solder joints can be lowered from 22.2 to 3.1 through using more resistant UBM. This UBM layer can suppress current crowding at the

UBM/solder interface.

As shown in Figures 5-1, one can clearly see that the current density drops very rapidly when it moved away from the chip side. Therefore, if the thickness of UBM increased, the current crowding region will locate within the UBM. And the UBM/solder interface will be further away from it.

To suppress the current crowding effect, the best scenario would be to have the current flowing though the whole solder uniformly. To achieve this goal, increasing the resistivity of UBM would be the best method. Our simulation shows that the current crowding ratio can be reduced to 3.1 when the UBM resistivity increased to 4770 μΩ·cm. However, the tradeoff is the increase in the resistance of the solder joints. The vertical resistance of the standard model was estimated to be 1.2 mΩ. The total resistances of the solder joints became 1.4, 2.1, 3.0 and 10.3 mΩ for the solder joints with a UBM resistivity of 295 μΩ·cm, 1477 μΩ·cm, 2954 μΩ·cm and 14770 μΩ·cm, respectively. This resistive layer could be a TiN, TaN or Ta material, and could be deposited with UBM, or it could be an additional layer between Al pad and UBM. Furthermore, our thermal simulation shows that the Joule heating effect due to the resistive layers was less than 0.6 °C when the applied current was less than 0.2 A. Therefore, the insertion of the resistive layers could relieve current crowding effect significantly, and caused very small Joule heating effect at low applied current.

Nevertheless, it is still unknown if it is compatible with the current flip-chip manufacturing process. Thus, it requires further experimental study.

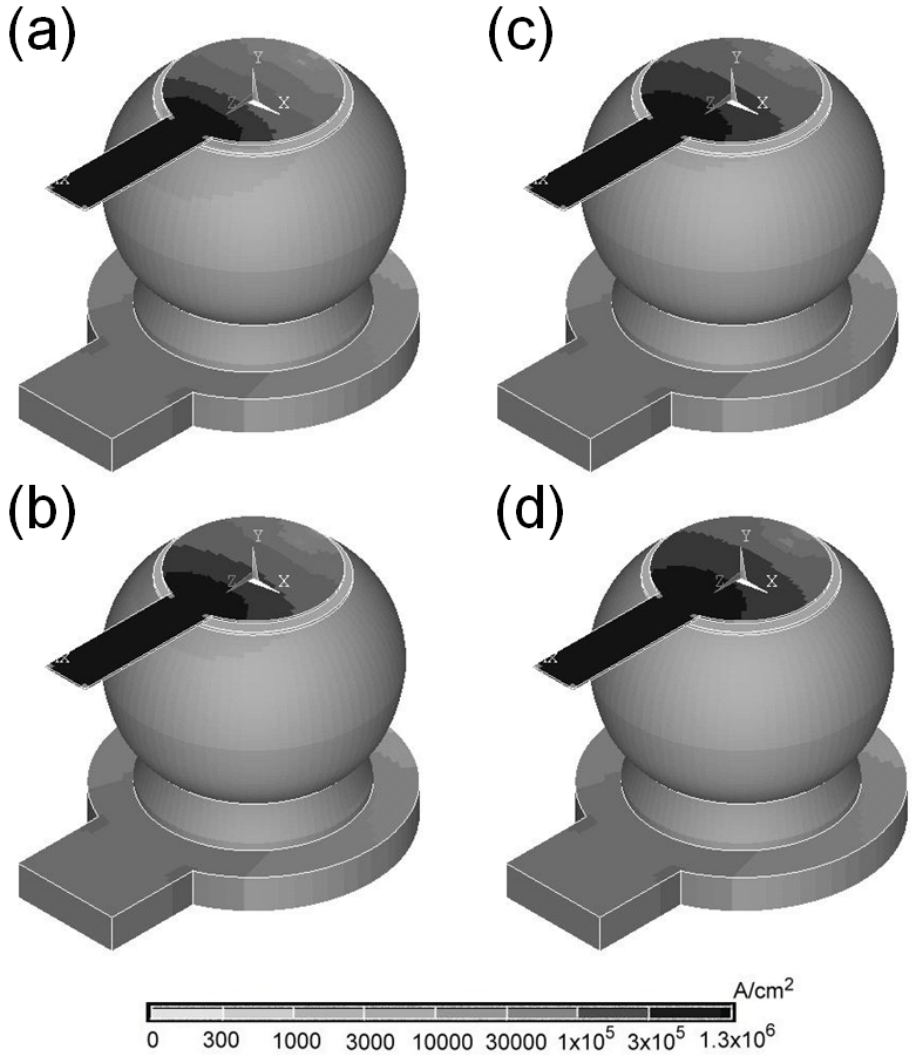


Figure 5-1: The 3-D current density distribution in the solder joints with different UBM resistivity values (a) 295.4 μΩ·cm. (b)1477 μΩ·cm. (c) 2954 μΩ·cm. (d)14770 μΩ·cm.

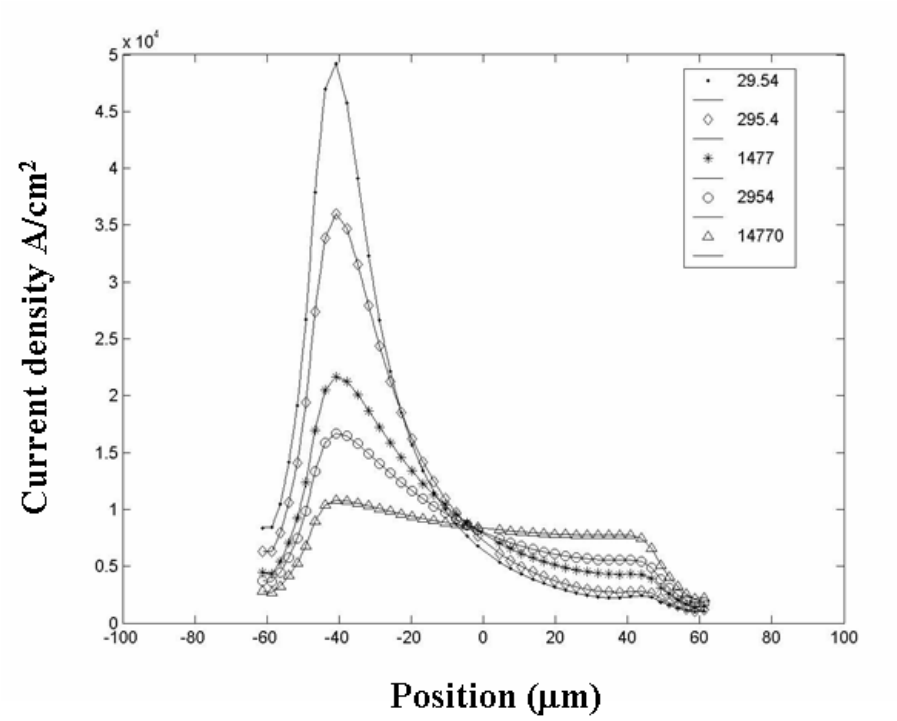


Figure 5-2: The current density distribution inside the solder along Z-axis for the five UBM resistivity values at the top layer of the solder (cross-section Y3).

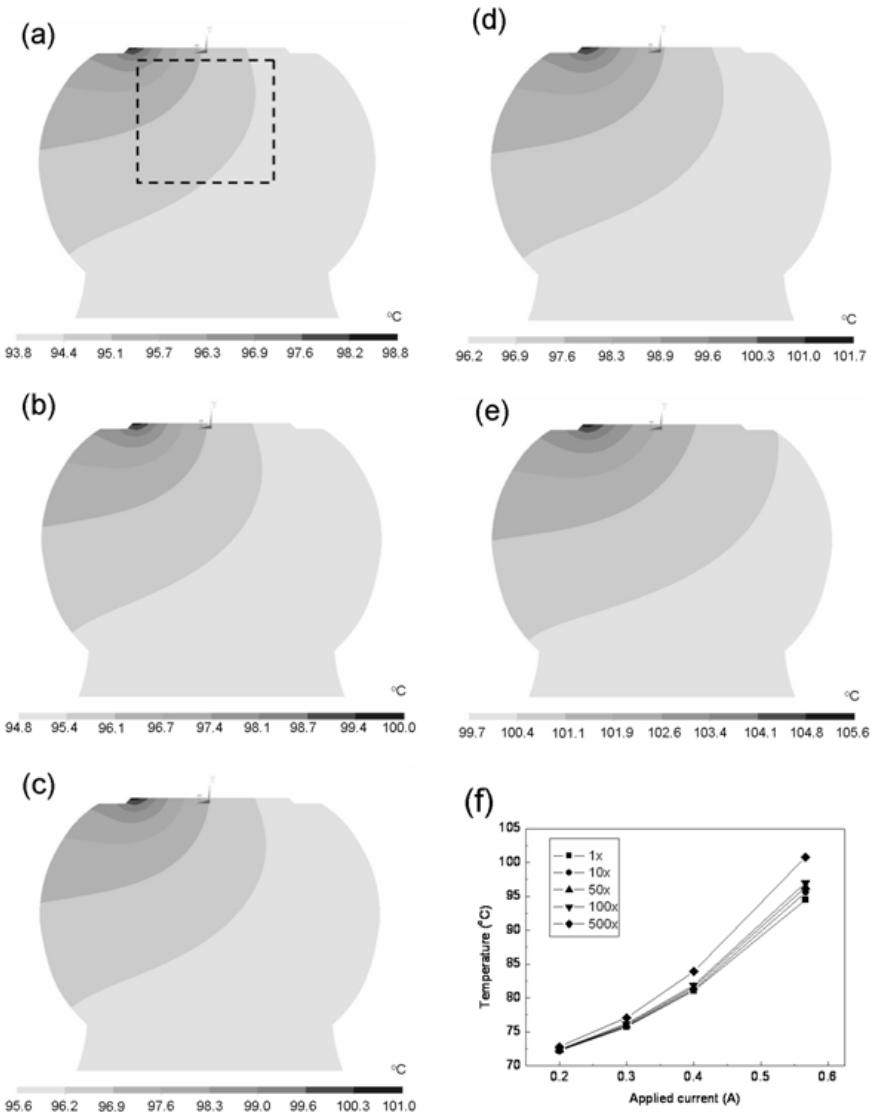


Figure 5-3: Temperature distribution in the solder bumps when stressed by 0.567 A. (a) Standard model. (b) Solder joints with resistive UBM of 295.4 μΩ·cm. (c) Solder joints with resistive UBM of 1477 μΩ·cm. (d) Solder joints with resistive UBM of 2954 μΩ·cm. (e) Solder joints with resistive UBM of 14770 μΩ·cm (f) Simulated temperature in the solder joints as a function of applied current up to 0.567 A

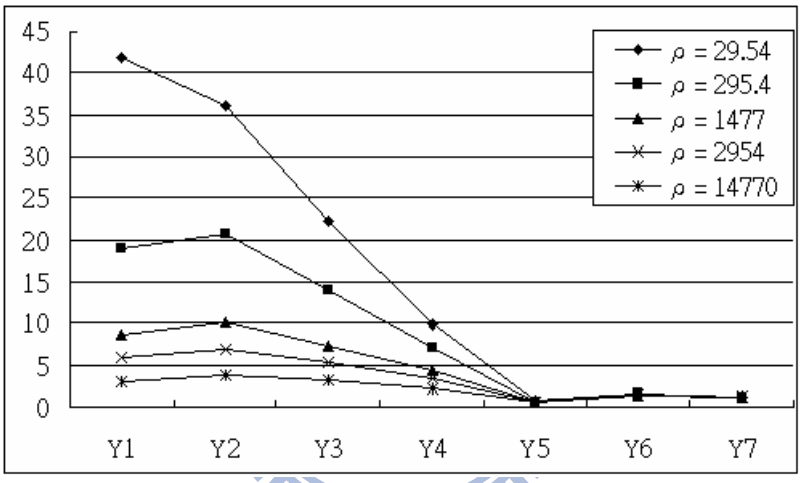


Figure 5-4: The crowding ratios for Y1 to Y6 cross-sections for the effect of UBM resistivity.

Table 5-1: Maximum current density and crowding ratios at different cross sections for the solder joints with various UBM with high resistivities.

method \ cross-section			Y1: UBM layer	Y2: IMC layer	Y3: top layer of solder	Y3: UBM layer of solder	Y4: middle layer of solder	Y5: necking layer of solder	Y6: bottom layer of solder
UBM resistivity (μΩ·cm)	29.54	Max.	2.1×10^{5}	1.8×10^{5}	1.1×10^{5}	4.9×10^{4}	3.5×10^{3}	7.6×10^{3}	5.9×10^{3}
		ratio	41.9	36.2	22.2	9.8	0.7	1.5	1.2
	295.4	Max.	9.5×10^{4}	1.0×10^{5}	7.0×10^{4}	3.6×10^{4}	3.4×10^{3}	7.3×10^{3}	5.8×10^{3}
		ratio	19.0	20.8	14.9	7.2	0.7	1.5	1.2
	1477	Max.	4.3×10^{4}	5.0×10^{4}	3.7×10^{4}	2.2×10^{4}	3.2×10^{3}	7.3×10^{3}	5.8×10^{3}
		ratio	8.7	10.0	7.4	4.3	0.6	1.5	1.2
	2954	Max.	3.0×10^{4}	3.5×10^{4}	2.7×10^{4}	1.7×10^{4}	3.2×10^{3}	7.2×10^{3}	5.8×10^{3}
		ratio	5.9	7.0	5.4	3.3	0.6	1.4	1.2
	14770	Max.	1.5×10^{4}	1.9×10^{4}	1.6×10^{4}	1.1×10^{4}	3.1×10^{3}	7.0×10^{3}	5.7×10^{3}
		ratio	3.0	3.7	3.1	2.2	0.6	1.4	1.1
	29540	Max.	1.3×10^{4}	1.6×10^{4}	1.4×10^{4}	9.8×10^{3}	3.1×10^{3}	7.0×10^{3}	5.7×10^{3}
		ratio	2.5	3.2	2.7	2.0	0.6	1.4	1.1

5.1.2 Solder composition

To elucidate how the current density and temperature distribute during current stressing by solder alloys, 3D thermo-electrical coupled modeling was performed on the solder joints with identical configuration but with different solders materials. They include eutectic SnPb, high-Pb SnPb95 and eutectic SnAg.

Among these three solders, Pb-free SnAg possesses the lowest electrical resistivity and thermal conductivity of 12.3 μΩ·cm and 33 W/m·K respectively. Figures 5-5 (a) through (c) display the current-density distribution in the solder joints under the stress current of 0.6A. The distribution profiles remain essentially the same. The maximum current density were 1.03×10^5, 9.42×10^4, 1.11×10^5 A/cm^2 for the eutectic SnPb, high-Pb, and the eutectic SnAg solders, respectively. The Pb-free solder exhibits the highest current crowding effect because of its lowest electrical resistivity. Figures 5-6 (a) through (c) illustrate the temperature distribution in the solder bumps. The solders near the entrance point of Al trace all show higher temperature than the rest solders. Figures 5-7 (a) through (c) show the cross-sectional views for the temperature distribution. The results indicate the existence of hot-spots in these solder bumps. The hot-spot temperature was 100.0, 103.6 and 105.4 °C respectively, whereas the average temperature was 95.9, 99.2 and 98.9 °C for the eutectic SnPb, high-Pb and the eutectic SnAg solder. The Pb-free solder experienced the highest Joule heating

effect, which may due to limited intrinsic capability for heat dissipation and highest current crowding effect. Since the major heating source was Al trace [19], lower resistivity of Pb-free solders did not necessarily render a smaller Joule heating effect. The simulation results are summarized in Table 5-2.

So far, our data demonstrate that the current crowding and Joule heating effects in Pb-free SnAg solder bump are marginally worse than those in eutectic SnPb solder bump, as shown in Figures 5-5 and 5-6. Nevertheless, Pb-free solder exhibits far better EM resistance than that of the eutectic SnPb. This surprising improvement may be attributed to the reduced diffusivity for Pb-free solder as its melting point is approximately 50 °C higher than that of the eutectic SnPb solder. As a result, the rate of void formation is much lower than that in the eutectic solder. In addition, the highest MTTF for the high-Pb solder may be mainly due to its higher liquidus temperature of about 320 °C. For example, at stressing temperature of 150 °C, it is 93%, 86% and 71% of the melting points for the eutectic SnPb, eutectic SnAg and high-Pb solders, respectively. Typically, at melting point metal atoms exhibit a diffusivity of 10^5 to 10^7 cm^2/s in nature. Therefore, it is prudent to assume that the diffusivity of Pb-free solder would fall somewhere in between these two Pb-containing solders. This is in accordance to the findings that the EM resistance of Pb-free solder is higher than that of the eutectic SnPb solder, but lower than that of the high-Pb solder.

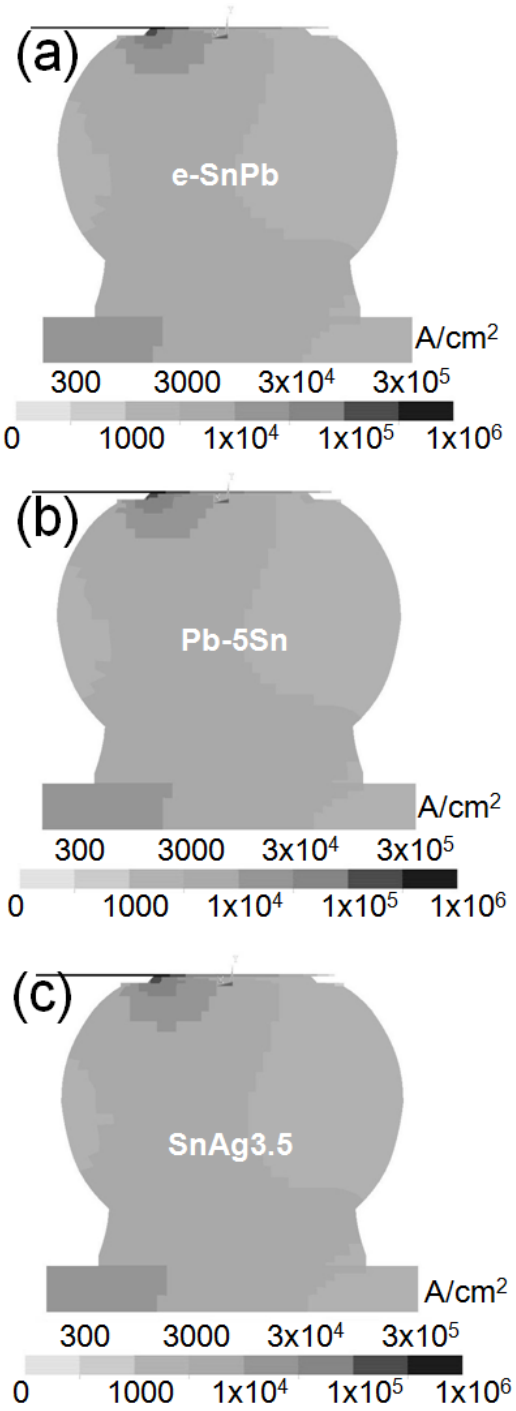


Figure 5-5: The simulation results shows the current density distribution under 0.6 A in (a) Eutectic solder bump. (b) High-Pb solder bump. (c) Eutectic solder bump.

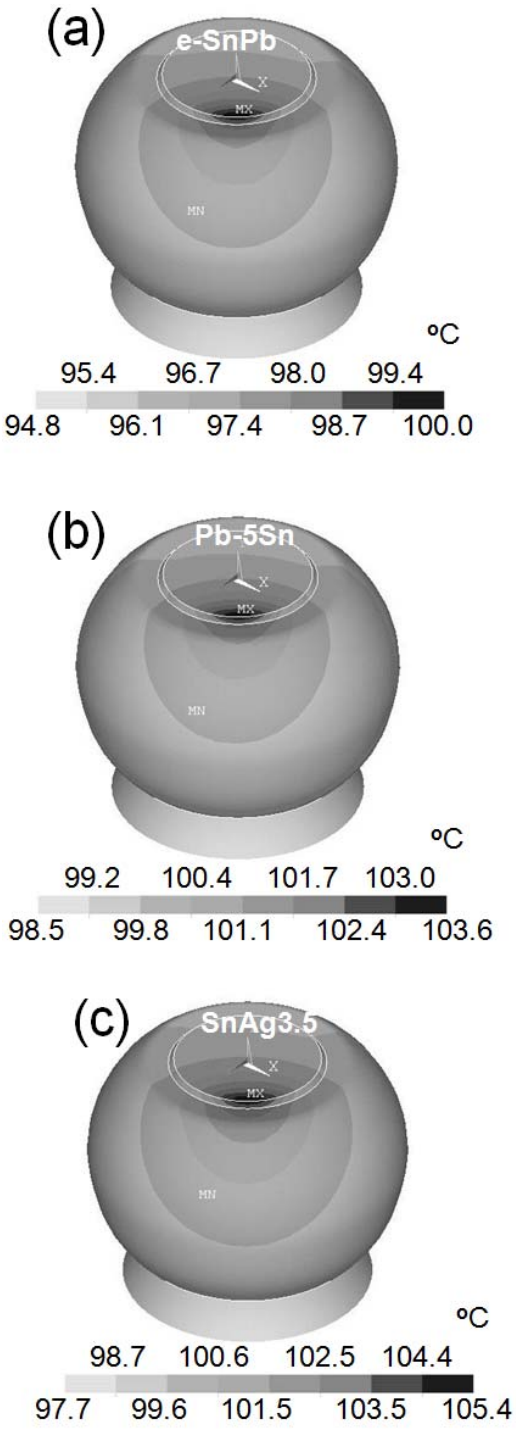


Figure 5-6: The simulation results shows the temperature distribution under 0.6 A in (a) Eutectic solder bump. (b) High-Pb solder bump. (c) Eutectic solder bump.

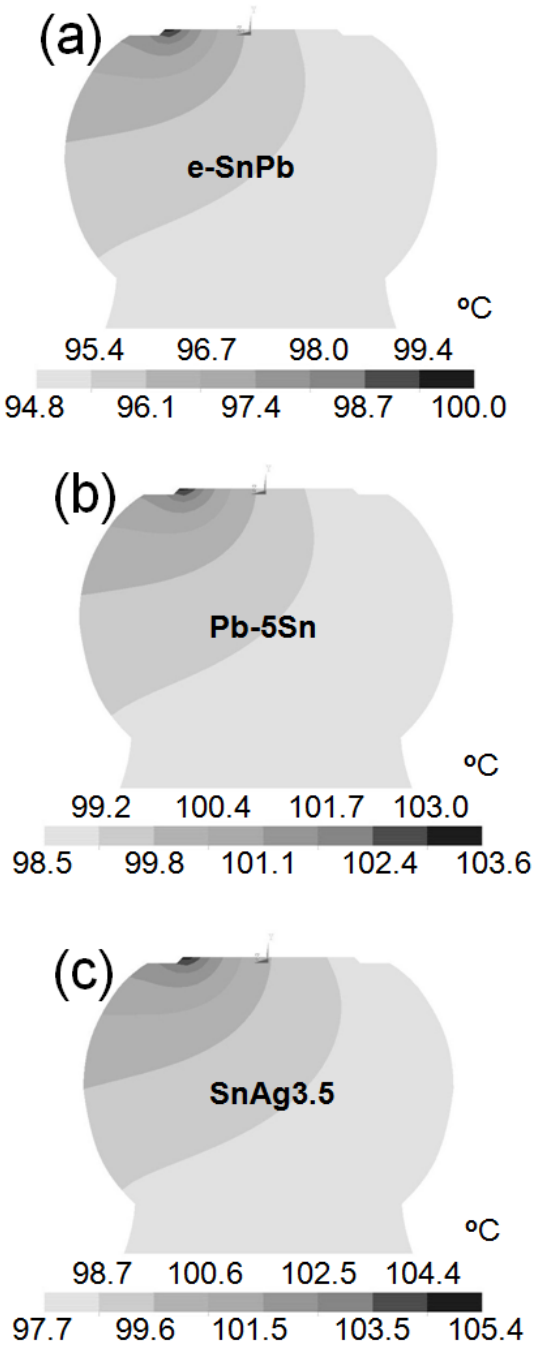


Figure 5-7: The cross-sectional view of the results in Figure 5. (a) Eutectic solder bump. (b) High-Pb solder bump. (c) Eutectic solder bump.

Table 5-2: The simulation results on maximum current density, hot-spot and average temperatures and thermal gradient for the high-Pb, eutectic SnPb and SnAg solders.

Solder alloys	Maximum current density (A/cm^2)	Hot spot (°C)	Average temperature (°C)	Thermal gradient (°C/cm)
Pb95Sn5	9.4×10^4	103.6	99.2	246.9
e-SnPb	1.0×10^5	100.0	95.5	259.2
SnAg3.5	1.1×10^5	105.4	98.9	398.7

5.1.3 Al-trace design

To investigate the effect of Al-trace dimension on Joule heating and current crowding, four models with identical structure of solder bumps and Cu lines but with different dimensions of Al-trace were constructed. The first one is the standard model, which includes two SnPb solder bumps connected by an about 1840-μm-long Al trace of 34 μm wide and 1.5 μm thick, as shown in the Figure 5-8 (a). For the second model, as shown in Figure 5-8 (b), the width of Al trace was increased to 100 μm with the rest of the structure remained the same. Figure 5-8 (c) shows the third model, in which the thickness of Al trace was increased to 4.4 μm while the rest of the features remained the same as the standard model. The second and the third models had the same cross-section area of Al trace. For the fourth model, as depicted in Figure 5-8 (d), shorter the Al trace with 670 μm less than the standard model was adopted with the rest of the features remained the same as those in the first model.

The current crowding effect can be relieved to some extent by increasing the width or the thickness of Al trace. In this letter, we denote the crowding ratio to be the maximum current density inside the solder bump divided by the average current density in UBM opening, which was obtained by assuming the current spreads uniformly on UBM opening. The crowding ratio means the non-balanced degree of the current distribution in the solder bumps, and the current crowding would accelerate the

EM damage due to larger wind force in the current-crowding region. Figures 5-9 (a) through (d) show the cross-sectional views for the current density distribution of the four models when they were stressed by 0.6 A. The local current density inside the solder bumps near the entrance of Al trace was reduced in the second and the third models. The crowding ratio for the first model 1 was as high as 19.8. When the cross-section of Al trace was increased by 2.9 times, the crowding ratios were reduced down to 12.0 and 11.7 for the second and the third model, respectively. Since the geometry of the Al trace near the solder bumps did not change for the fourth model, the distribution of current remained the same as the first model. Therefore, enlarging the cross-section of Al trace may reduce the crowding ratio.

Furthermore, the dimension of Al trace had significant effect on Joule heating of the solder bumps. Figures 5-10 (a) to (d) illustrate the temperature distributions in the center cross-sections for the four models when they were applied by 0.6 A at 70°C. A hot spot inside solder bumps occurred near the entrance point of Al trace into solder bumps below the passivation opening. The average temperature was obtained by averaging the node temperatures in 70 μm × 70 μm area, as shown in Figure 5-10 (a). The temperature in the hot spot was 102.8 °C, 81.7 °C, 83.6 °C and 90.3 °C for the four models, respectively, whereas the average temperature was 97.9 °C, 80.6 °C, 82.0 °C, and 86.1 °C for the four models, respectively. It is obvious that the Joule heating

effect was greatly reduced when the cross-section of Al trace was increased. Figures 5-11 (a) and (b) show the hot-spot and average temperatures as a function of applied current up to 0.6 A. The trend for lower stressing current behaves the same as that stressed by 0.6 A. Due to the hot spot, a thermal gradient was built up across the solder bumps. The thermal gradient in this section was calculated from the temperature difference between the hot-spot and the average temperature of the solder close to the BT side, divided by the bump height. It can be observed that the second model had the lowest thermal gradient among the four models. In Figure 5-11 (c), the gradient in the fourth model was almost the same as than in the first model, which implies that the hot spot was mainly induced by current crowding effect.

In general, Al trace is the major Joule heat source during accelerated EM test, since its cross-section area is typically one to two orders in magnitude less than that of the solder bumps and Cu line. Under the same applied current, Joule heating power is proportional to the total resistance of the stressing circuit. The resistance of Al trace for the first model was 1331 mΩ, whereas it decreased to 530 mΩ, 551 mΩ and 532 mΩ for the rest of the three models, respectively. Therefore, the Joule heating effect was less significant for the stressing circuit with smaller resistance.

Furthermore, the effect of Al trace dimension on MTTF could be estimated by using Equation 1.6. For the same solder joint with different dimension of Al traces

under the same stressing condition, the activation energy Q and the constant A are the same for the four models. For the solder joint in the standard model, the maximum current density reached to 1.05×10^5 A/cm^2 and the hot-spot temperature was 102.8 °C. For the solder joint with 100-μm-wide Al trace, the maximum current density was 6.39×10^4 A/cm^2 and the hot-spot temperature was reduced down to 81.7 °C. The MTTF would be 6.1 times longer than that of the standard model under 0.6 A at 70 °C, in which the relief of current crowding contributed about 2.5 times, and the decrease in Joule heating contributed approximately 2.5 times on the increasing of the lifetime increase. For the joint with 4.4-μm-thick Al trace, the maximum current density decreased to 6.20×10^4 A/cm^2 and the hot-spot temperature was reduced to 83.6 °C. The estimated MTTF would be 5.9 times longer than that of the standard. For the fourth model, the MTTF is about 1.7 times longer than that of the standard model. It is noteworthy that the Joule heating effect could be further reduced if the length of Al trace is further decreased. But the current crowding effect remains the same when only the length is changed. The above estimation demonstrates that the solder joints with wider or thicker Al traces could significantly increase the EM resistance.

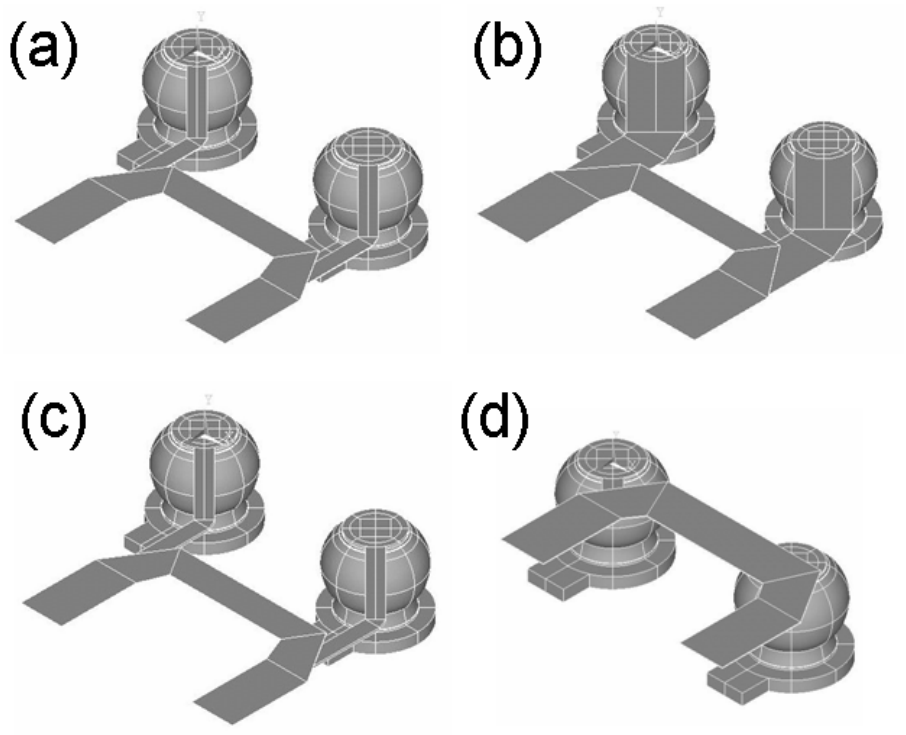


Figure 5-8: The four models constructed in this study. (a) The first model with a 34-μm-wide, 1.5-μm-thick and about 1000-μm-long Al trace. (b) The second model with a wider Al trace of 100 μm. (c) The third model with a thick Al trace of 4.4 μm. (d) The fourth model with a shorter Al trace of about 400 μm.

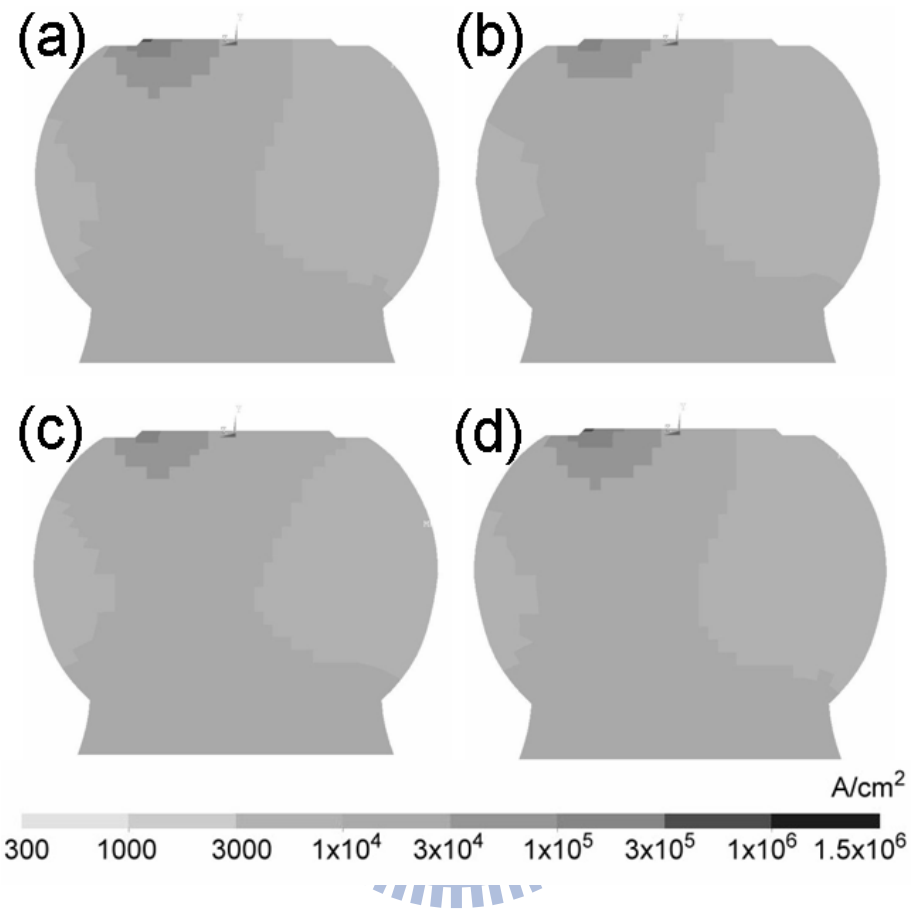


Figure 5-9: The cross-sectional views for the current-density distribution in the solder bumps when they were stressed by 0.6 A. (a) The first model. (b) The second model. (c) The third model. (d) The fourth model.

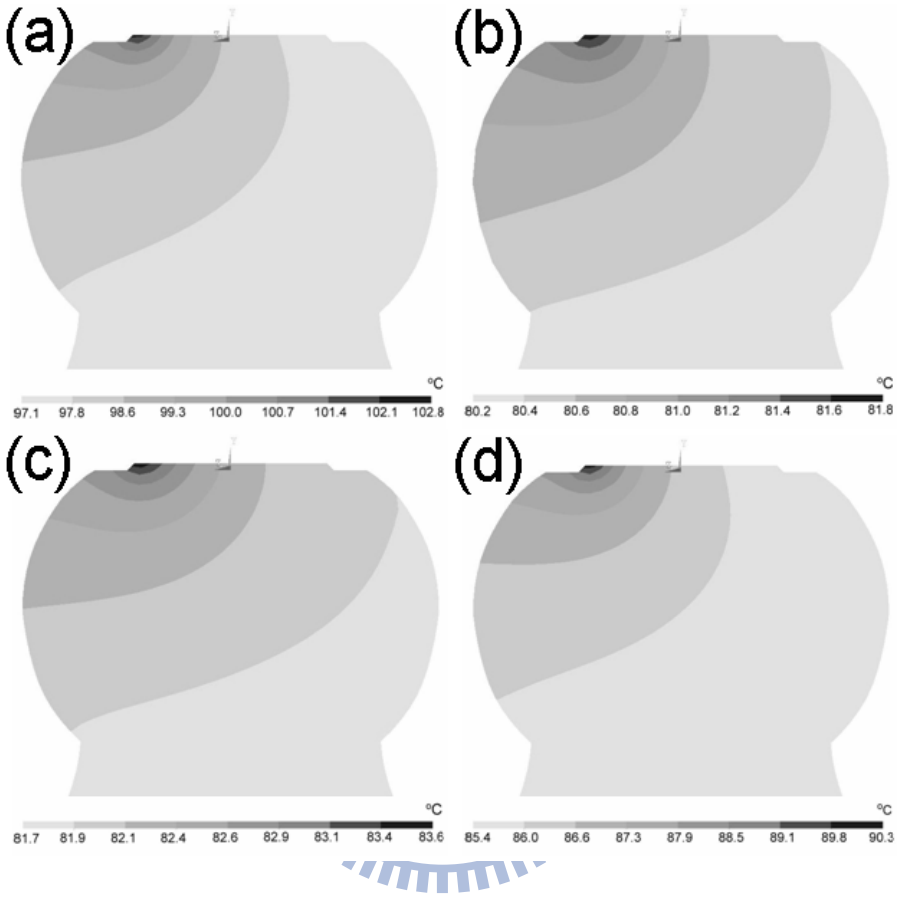


Figure 5-10: The cross-sectional views for the temperature distribution in the solder bumps when they were applied by 0.6 A at 70°C. (a) The first model. (b) The second model. (c) The third model. (d) The fourth model.

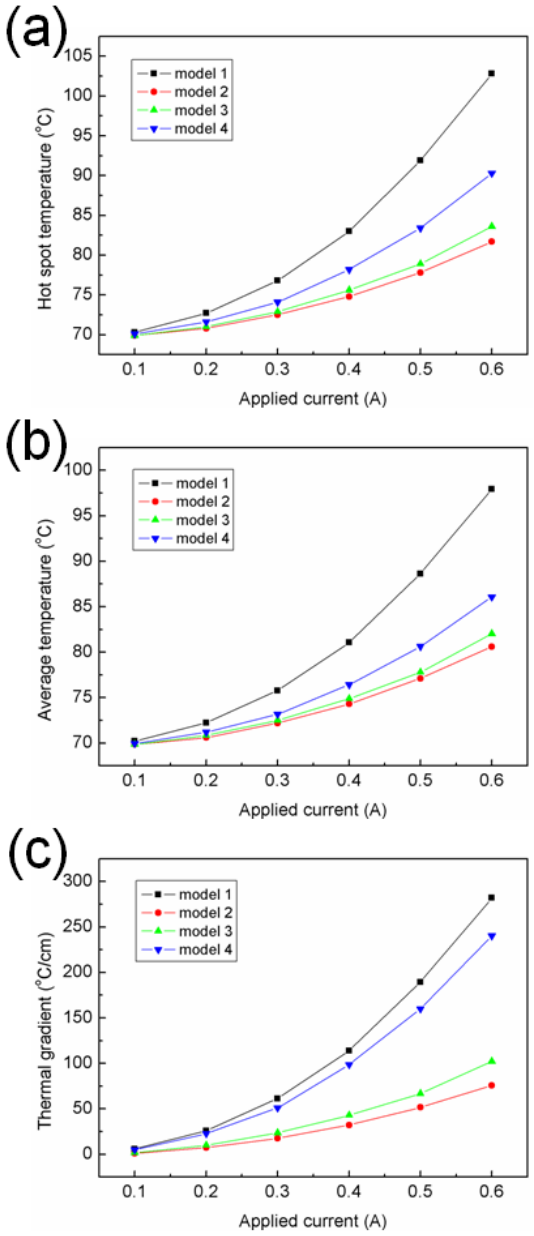


Figure 5-11: (a) The hot-spot temperature. (b) The average temperature. (c) The thermal gradient in the solder bumps as a function of applied current up to 0.6 A at 70 °C for the four models.

5.1.4 UBM thickness

For this study, a 3D finite-elements method was employed to simulate the current-density and temperature distributions in the solder joints with 0.5-μm, 5-μm, 25-μm, 50-μm and 100-μm Cu UBMs.

With a thicker Cu UBM, more uniform distribution of current density was obtained in the solder bumps. Figures 5-12 (a) through (e) show the current-density distribution in the solder joints with 0.5-μm, 5-μm, 25-μm, 50-μm and 100-μm Cu UBMs, respectively, when applied by 0.6 A. It can be seen that the current crowding effect still occurs in the thick Cu UBM near the entrance of Al trace into the solder joints. However, as the thickness of Cu UBM increases, the solder is kept away from the crowding region. When Cu UBM is thicker than 50 μm, the current crowding occurs mostly in Cu UBM, and the maximum current density in solder decreases dramatically. The crowding ratio in this paper is denoted as the maximum current density in the solder divided by the average value in UBM opening, which is 5.01×10^3 A/cm^2. It is 19.0, 9.6, 2.9, 1.7, and 1.6 for the solder joints with 0.5-μm, 5-μm, 25-μm, 50-μm, and 100-μm Cu UBMs, respectively. We conclude that thick Cu UBM results in uniform current-density distribution and reduced maximum current density. In short, the current flow spreads out more uniform before reaching the solder bumps with a thicker Cu UBM.

In addition, thick Cu UBM can relieve the hot-spot issue in solder bumps. Figures 5-13 (a) and (b) show the Joule heating effect in Al trace for the solder joints with 0.5-μm and 100-μm Cu UBMs, respectively. It was found that the overall Joule heating effect in the stressing circuit did not reduce when 0.5-μm Cu UBM was replaced by 100-μm UBM. The total resistance for the circuit was about was 1330 mΩ, while the resistance decreased due to thicker Cu column was only in milli-ohm range. Thus, both models are almost the same overall Joule heating effect in Al trace. Nevertheless, Joule heating effect in solder bumps was quite different. Figure 5-14 (a) through (e) show the tile-views for the temperature distribution in the solder joints with 0.5-μm, 5-μm, 25-μm, 50-μm and 100-μm Cu UBMs, respectively, when applied by 0.6 A. For clear view of the hot spot, Cu UBMs are not shown in these figures. The top surfaces of these bumps represent the solder connecting to Cu UBMs. Hot spots exist in the solder joints with thin Cu UBMs. However, it was found that with a Cu UBM greater than 50 μm, the hot spot could be almost eliminated completely. Figure 5-15 (a) through (e) show the corresponding cross-sectional views for the temperature distribution. It is clear that the hot-spot was almost eliminated for the solder joints with 50 μm and 100 μm Cu column. The temperature difference between the hot spot and the average values is 4.5 °C, 2.5 °C, 0.7 °C, 0.3 °C, 0.1 °C for the solder joints with 0.5-μm, 5-μm, 25-μm, 50-μm and 100-μm Cu UBMs, respectively, when applied by 0.6 A. The

difference between the hot spot and the average temperature increased as the applied current increased. Figure 5-16 (a) through (c) shows the hot spot and average temperatures as a function of applied current up to 0.6 A for the solder joints with the 25-μm, 50-μm and 100-μm Cu columns. No obvious hot spot was found after Cu column was thicker than 50 μm.

Although thick Cu UBM can relieve the hot spot, the overall Joule heating remains unchanged even for the solder joints with 100-μm Cu UBM. Figure 5-17 (a) depicts the hot-spot temperature as a function of applied current for the five models. Compared with the solder joints with 0.5-μm-thick Cu UBM, 100-μm-thick Cu reduce the hot-spot temperature by 5.0 °C. However, the overall Joule heating effect did not change much, as illustrated in Figure 5-17 (b). It can be observed that the average temperature in solder does not decrease significantly even when Cu UBM was as thick as 100 μm. The insensitivity to Cu UBM thickness is because the primary heating source is Al trace. In these simulation models, the total resistance for the stressing circuit is about 1330 mΩ. The bump resistances are 6.1, 4.4, 3.3, 3.1 and 2.7 mΩ for the five models, respectively. Therefore, the reductions in bump resistance due to thicker Cu UBMs are negligible compared to the total resistance. Although the solder was kept away from the heating source for 100 μm Cu column, Cu is a superb heat conductor, which is expected to facilitate heat conduction. Thus, the average

temperatures in solder for the five models were quite close. Furthermore, with thicker Cu UBM, thermal gradient is reduced considerably. The thermal gradient in this letter is determined from temperature difference between the top and bottom solder divided by the height of the solder bumps. As shown in Figure 8, the gradient reduced from 400 °C/cm to 60 °C/cm when Cu UBM is increased from 0.5 μm to 100 μm. Thus, the thermomigration in solder would be inhibited with thicker Cu UBM [37].

The elimination of the hot spot for solder joints with thick Cu UBM may be attributed to the absence of the serious current crowding since there is no serious local Joule heating for these joints. The local Joule heating power is proportional to the square of the local current density. For the above five models, the overall Joule heating were quite close. Yet, the crowding ratios for the five models are 19.0, 9.6, 2.9, 1.7 and 1.6. It is expected that the local Joule heating power in the hot spot for the bump with 100-μm Cu column is 140 times less than that of the bump with 100-μm. Therefore, the hot-spot issue could be relieved significantly in solder bumps with thick Cu columns due to reduced current crowding effect.

Furthermore, the effect of the thickness of Cu UBM on MTTF could be estimated using the equation for solder joints. Table 5-3 summarizes the maximum current density, hot-spot temperature and the ratio of estimated MTTF for the five models in this letter. Compared with the solder joint with 0.5-μm Cu UBM, MTTF for the solder

joints with 5-μm, 25-μm, 50-μm and 100-μm Cu UBM exhibit a longer EM lifetime of 1.8, 4.6, 6.7, 7.3 times, respectively. Therefore, the solder joints with thicker Cu UBMs are likely to demonstrate better EM resistance due to lesser current crowding effect and lower hot-spot temperature. In addition, when Cu thickness is increased from 50 to 100 μm, there is no obvious increase in MTTF since there are negligible current crowding Joule heating effects when Cu UBM was thicker than 50 μm. Consequently, further thickening in Cu UBM is not expected to render longer EM lifetime.

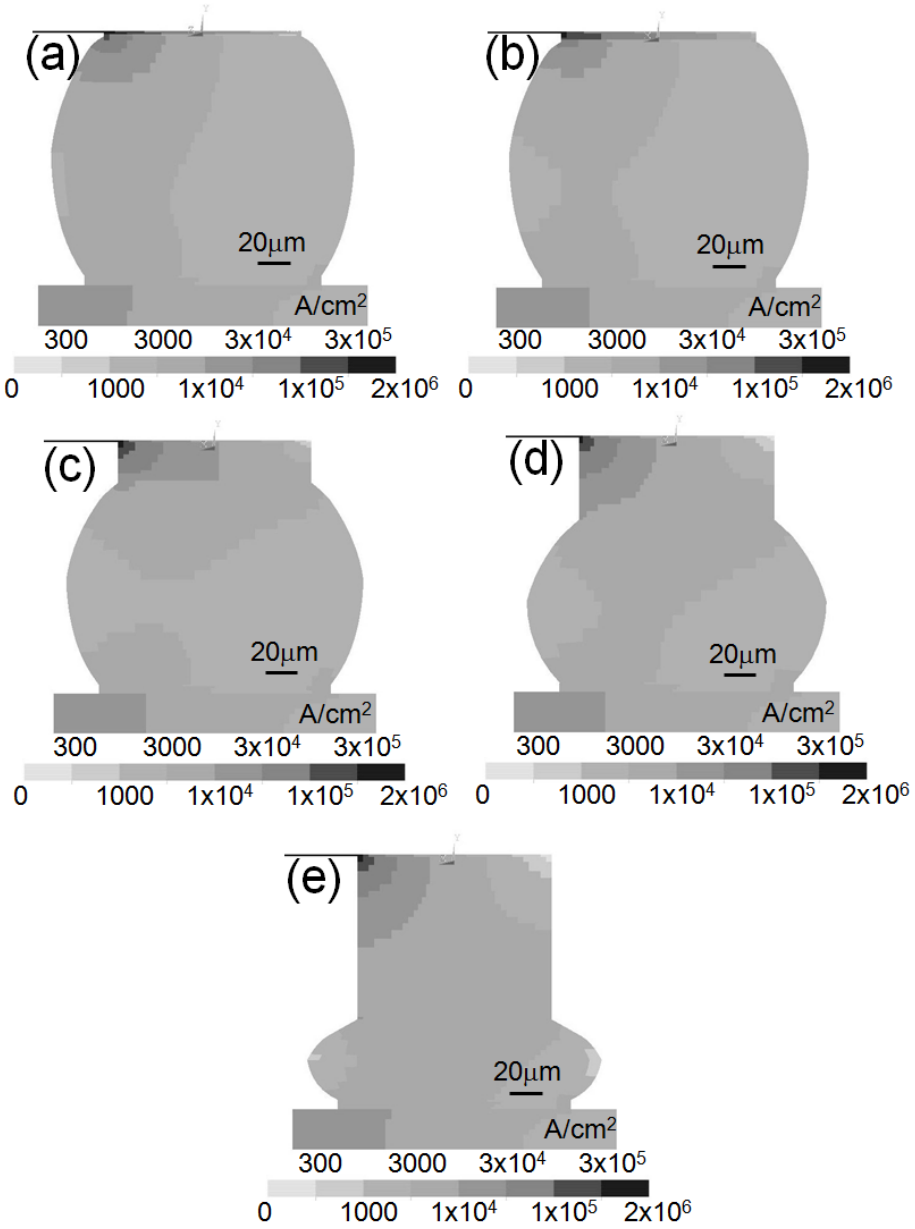


Figure 5-12: Current-density distribution in the solder joints with (a) 0.5-μm. (b) 5-μm. (c) 25-μm. (d) 50-μm. (e) 100-μm Cu UBM when applied by 0.6A.

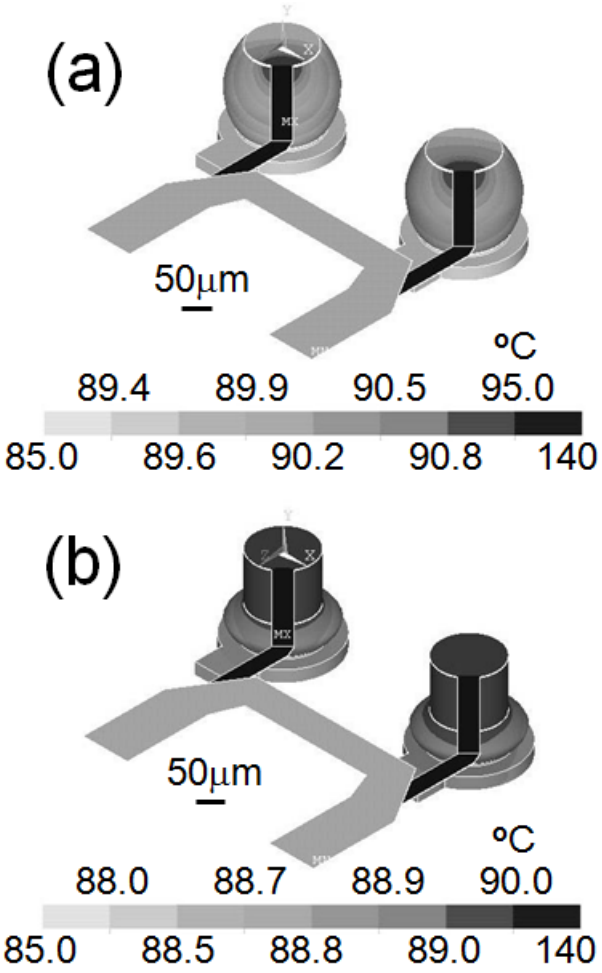


Figure 5-13: Joule heating effect in Al trace for the solder joints with (a) 0.5-μm UBM. (b) 100-μm Cu column.

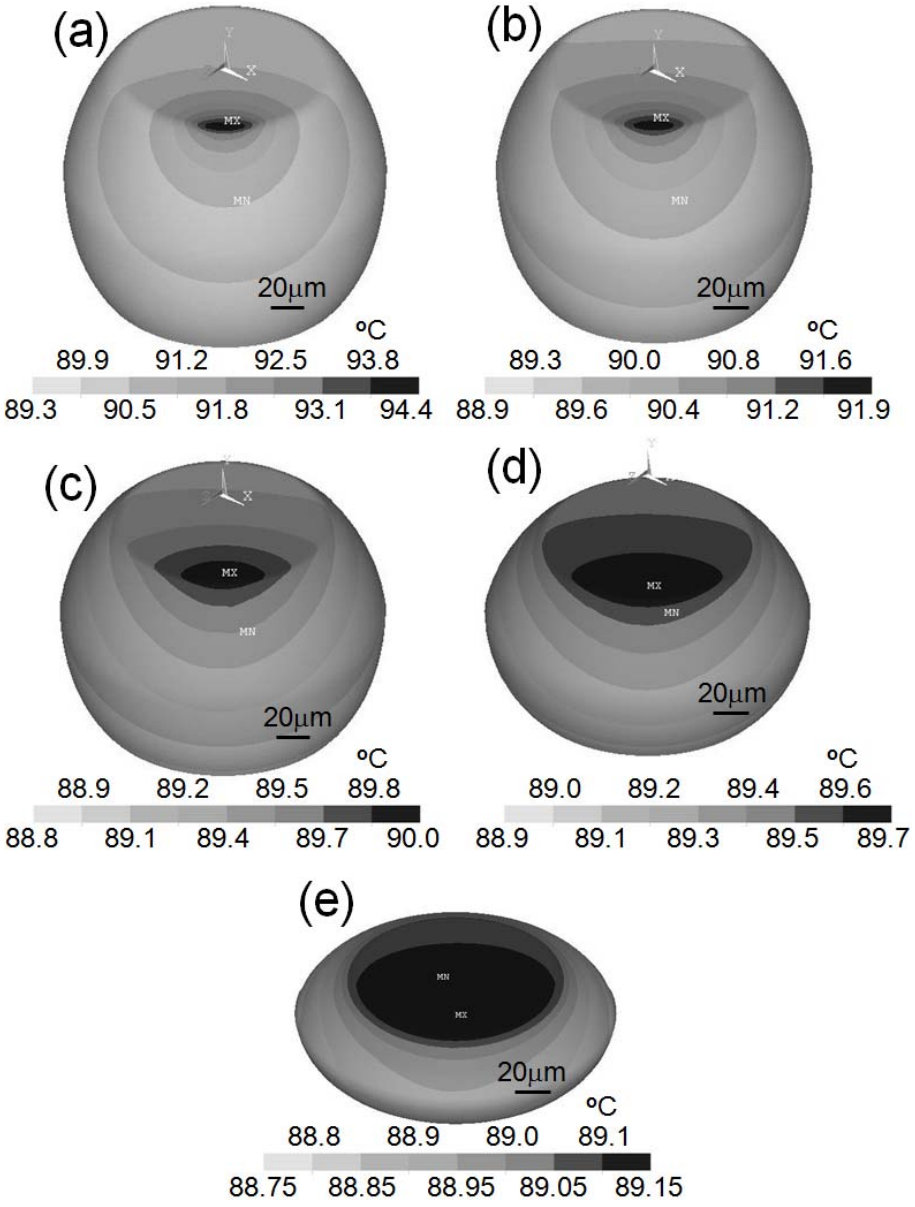


Figure 5-14: The temperature distribution in the solder bumps with (a) 0.5-μm. (b) 5-μm. (c) 25-μm. (d) 50-μm. (e) 100-μm Cu UBM when applied by 0.6 A at 100 °C. Only solder bump was shown.

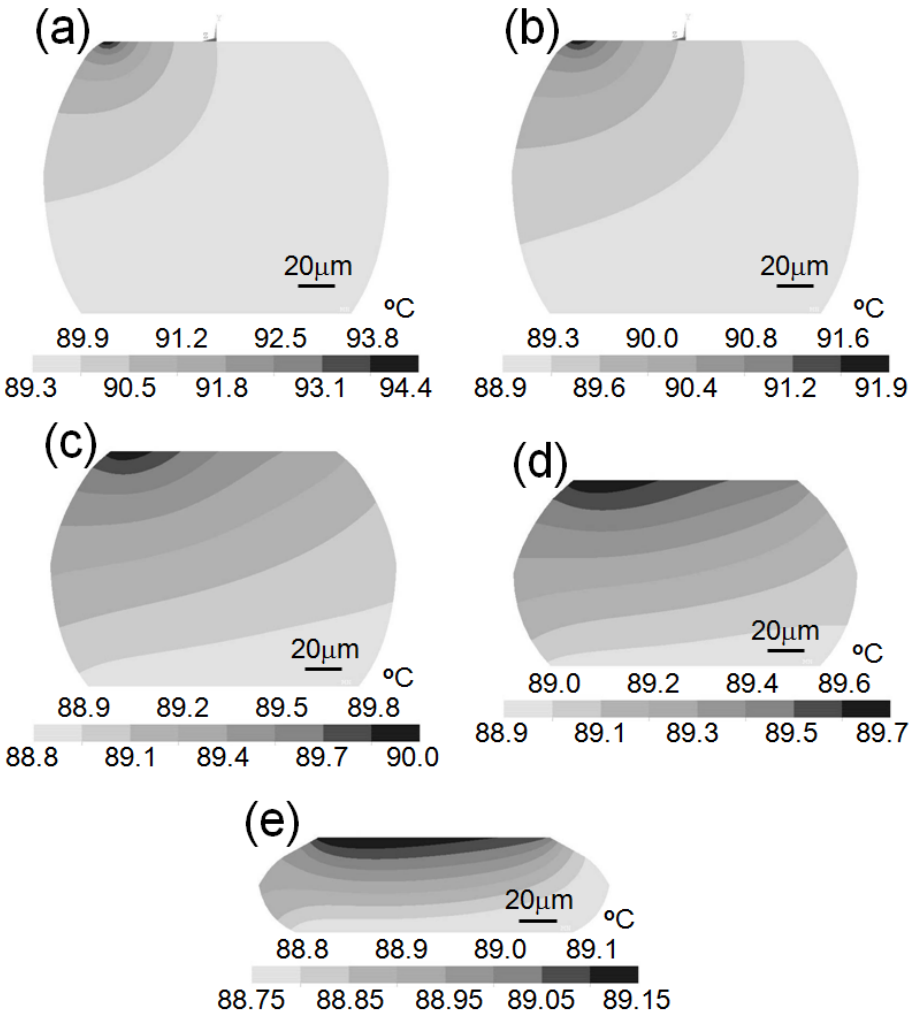


Figure 5-15: The cross-sectional view for the temperature distribution in the solder bumps with (a) 0.5-μm. (b) 5-μm. (c) 25-μm. (d) 50-μm. (e) 100-μm Cu UBM when applied by 0.6 A at 100 °C. Only solder bumps were shown.

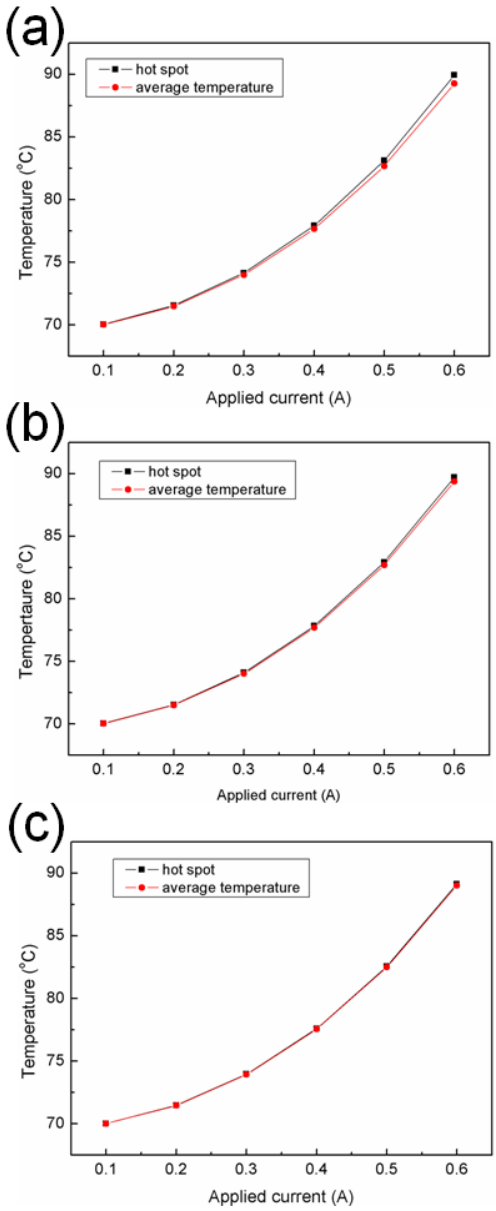


Figure 5-16: Hot spot and average temperatures as a function of applied current up to 0.6A for the solder joints with (a) 25-µm. (b) 50-µm. (c) 100-µm Cu columns. The hot-spot was almost eliminated completely when the Cu column was thicker than 50 µm.

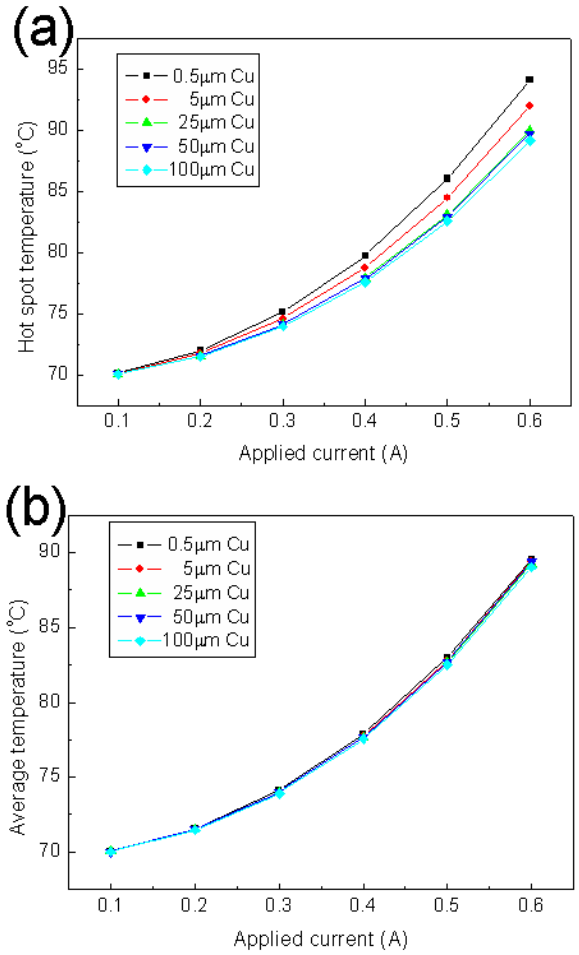


Figure 5-17: (a) Hot-spot temperature as a function of applied current for the five models. The hot-spot temperature decreased as the thickness of Cu UBM increased. (b) Average temperature in solder as a function of applied current for the five models. No obvious increase in average temperature when the thickness of Cu UBM was increased.

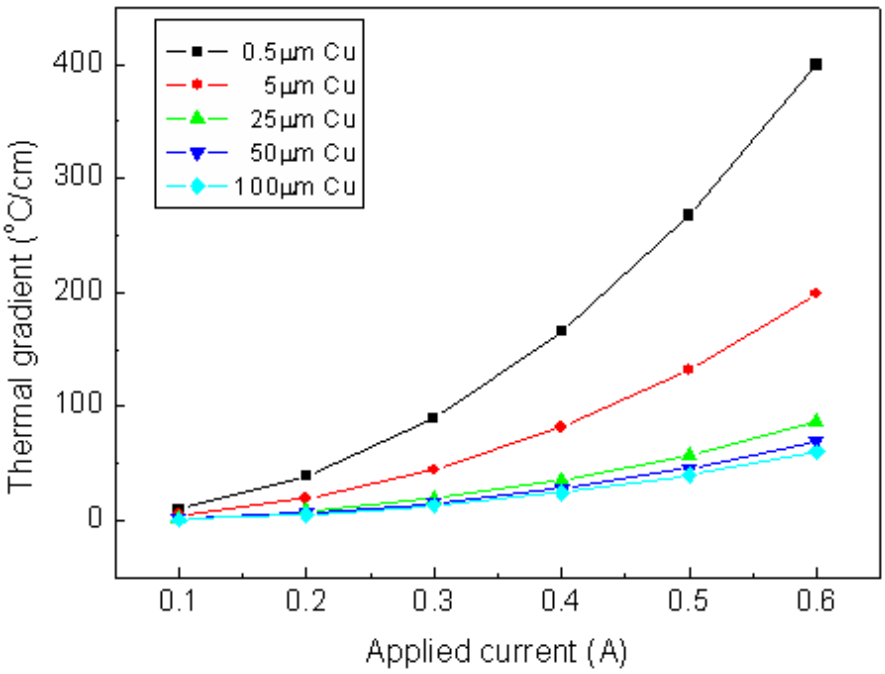
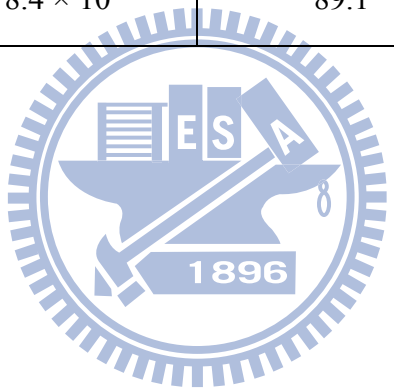


Figure 5-18: Thermal gradient as a function of applied current. Thick Cu UBM can effectively reduce the thermal gradient.

Table 5-3: The maximum current density, hot-spot temperature, and estimated MTTF for the five models in this section.

Cu UBM thickness (μm)	Maximum current density (A/cm^2)	Hot-spot temperature (°C)	MTTF ratio
0.5	1.0×10^5	94.1	1
5	5.1×10^4	91.9	1.8
25	1.5×10^4	90.0	4.6
50	9.1×10^3	89.7	6.7
100	8.4×10^3	89.1	7.3



5.1.5 Size of contact opening

In this research, we used finite-elements analysis to simulate the current density distribution of the solder joints with 1-μm, 5-μm, 10-μm and 25-μm thick of Cu UBM with various contact openings of flip-chip solder joints to investigate the size effect of the contact opening. We found that there exists an optima diameter of the contact opening with the lowest maximum current density in the solder joints for each thickness of Cu UBM.

Figure 5-19 shows the current density distributions in the solder bumps with 10-μm-thick Cu UBM and the diameter of contact opening in 30 μm, 60 μm, 85 μm and 110 μm, respectively. In Figure 5-19 (a), the current is coming from the left upper corner. The high current density region almost occupied the contact window and then spread in the solder bumps directly in the solder with 30-um diameter of contact opening. The current was confine in Al trace until it reached the contact opening to pass the current. The maximum current density in the solder bump is 1.13×10^4 A/cm^2 for the 30-μm contact opening in diameter. When the diameter of contact opening increased to 60 μm, the entering current spread out in the top solder region due to UBM has become a conducting path. As the green color shows in the Figure 5-19 (b), the high current density almost occupied half of UBM opening and then dispersed into the solder bumps. The maximum current density reduced to 9.5×10^3 A/cm^2 for the

60-μm contact opening in diameter. Keep increasing the contact opening, the current crowding region reduced. The current is coming from Al trace and directly get into the solder without spreading in UBM as show in Figures 5-19 (c) and (d). For the 85-μm and 110-μm contact opening in diameter, the maximum current density increased to 1.22×10^4 A/cm^2 and 1.92×10^4 A/cm^2, respectively.

Since the conductivity of Cu is better than that of solder alloy, the current would like to spread out in Cu UBM. But, the contact opening would influence the spread position of Cu UBM and also affect the current density distribution in the solder bumps. The enlarge current density distribution of the solder joints with four different diameter of contact opening was illustrated in Figures 5-20 (a) through (d). It was found that the higher current density region uniformly and symmetrically distributed in Cu UBM for the solder bumps that adopted 30-μm contact opening in diameter as show in Figure 5-20 (a). When 60-μm contact opening in diameter was employed in the solder bumps illustrates in Figure 5-20 (b), the current density coming from Al trace spread out in the contact opening and some part of it draft toward the left hand side of UBM opening. Further increasing in the diameter of the contact opening, the current density still can spread out in Cu UBM. In addition, the higher current density region preferred to enter into the solder bumps near the entrance of Al trace. Since this behavior was observed, the more uniform and symmetrical current density distribution

will relieve the current crowding effect in the solder joints. However, the optima diameter is not the smallest contact opening. This is because that the best relieving current crowding effect is the resistance balance among the resistance of Cu UBM from the current entrance point to the right hand side, the resistance of Cu UBM from the current entrance point to the left hand side, and the resistance of the solder bumps. If the contact opening is small, the resistance of the Cu UBM from the current entrance point to the right hand side is small enough to let the current enter into the solder bumps directly. On the other hand, when the contact opening is large, the resistance of Cu UBM from the current entrance point to the left hand side is small to keep the current crowding in the left upper corner of the solder bumps. Then the optimal diameter of the contact opening will exist for the solder joints. For the solder bumps with 10-μm-thick Cu UBM, the optimal diameter of the contact opening is 60 μm.

Since different thickness of UBM was adopted in the flip-chip solder joints [93, 94], the effect of UBM thickness on the optima diameter of the contact opening will also be discussed in this study. In Figure 5-21 (a), the optima diameter of the contact opening is 100 μm for the solder joints with 1-μm-thick Cu UBM. That means when 100-μm contact opening in diameter was used in the solder joints, it will have 35% lower current density than 30-μm contact opening in diameter was used. For the thicker UBM, it would relieve the current crowding effect by keep the solder away the

current crowding region [Section 5.1.4]. Since the optimal diameter of the contact opening has been investigated, it will enhance to relieve the current crowding region in the solder bumps. In Figures 5-21 (b) through (d), the optimal diameter of the contact opening is 70 μm, 60 μm and 30 μm for the solder joints with 5-μm-thick, 10-μm-thick and 25-μm-thick Cu UBMs, respectively. It can be found that to have 25-μm-thick Cu UBM may not be necessary, since the 60-μm contact opening in diameter for the solder joints with 10-μm-thick Cu UBM has similar current density to that of the solder joints with 25-μm-thick Cu UBM.

Figure 5-22 summarized the optima contact opening for the solder joints against UBM thickness. Thicker UBM has smaller optima contact opening. Due to the resistance balance among the resistance of Cu UBM from the current entrance point to the right hand side, the resistance of Cu UBM from the current entrance point to the left hand side, and the resistance of the solder bump, the different thickness of UBM should have the different optima contact opening. Except the solder joints with 1-μm-thick Cu UBM, the curve should be a linear profile. The reason is that the UBM is too thin to spread the current in it. Since UBM narrow down to 1 μm which is thinner than Al trace, that would cause higher resistance in UBM than that in Al trace. Then, the current would like to spread out in Al trace. Therefore, the resistance balance will become more completely. The resistance of Al pad needs to be included. The

optima diameter of contact opening for the solder joints with thin film UBM should exceed in the expectation for that with thick film UBM.

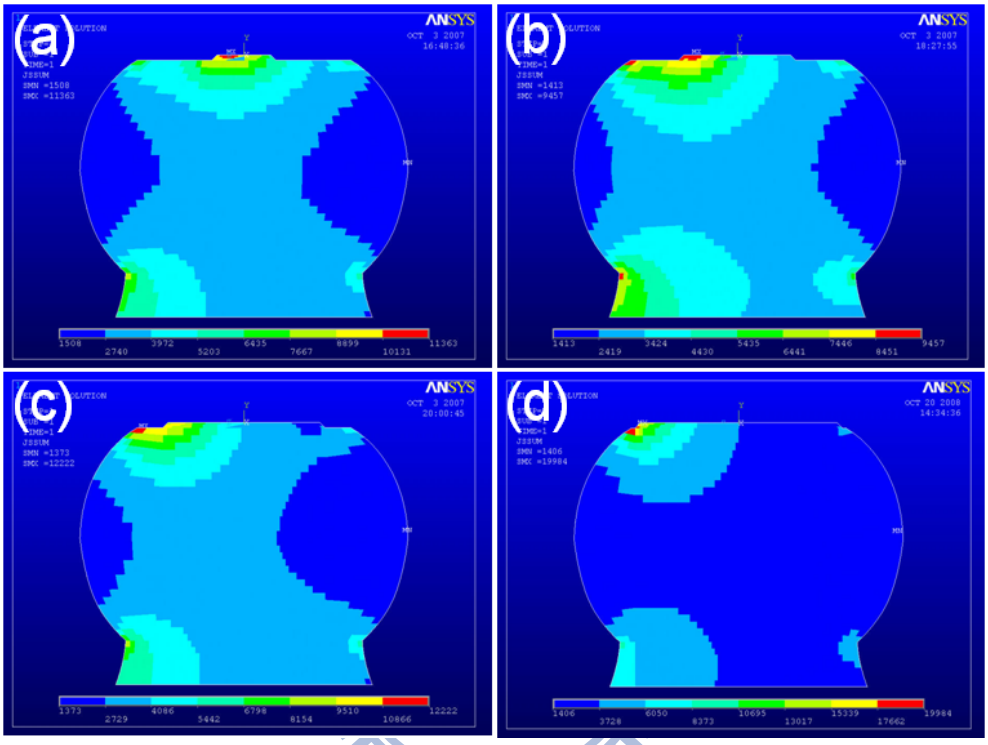


Figure 5-19: The cross-sectional current density distribution of the solder bumps only with 10-μm-thick Cu UBM for different contact opening. (a) 30 μm in diameter. (b) 60 μm in diameter. (c) 85 μm in diameter. (d) 110 μm in diameter.

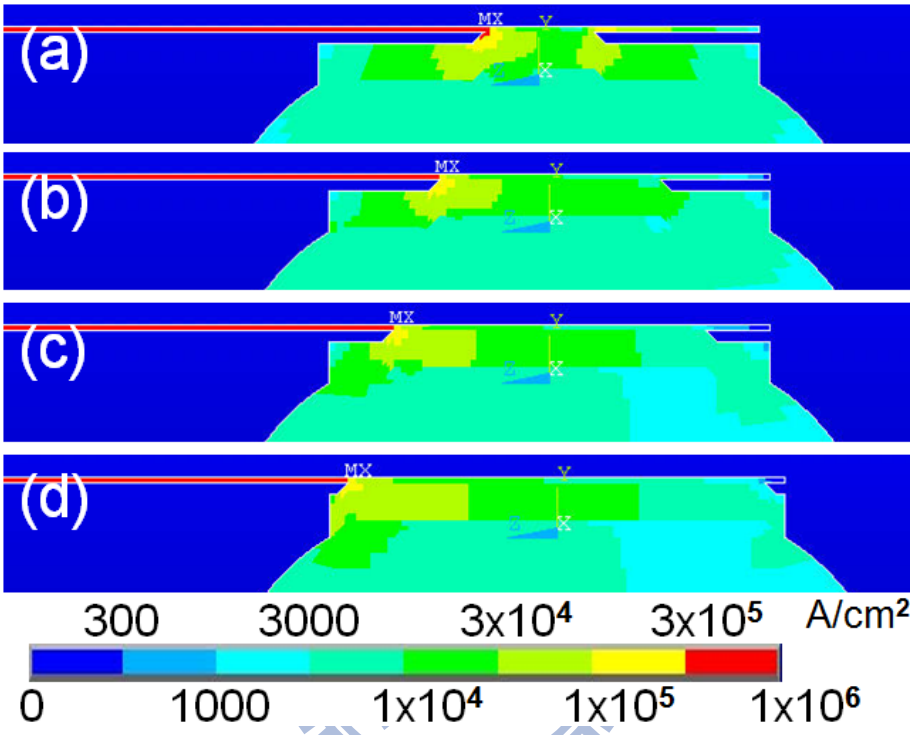


Figure 5-20: The enlarged cross-sectional current density distribution of the solder joint with 10-μm-thick Cu UBM for different contact opening. (a) 30 μm in diameter. (b) 60 μm in diameter. (c) 85 μm in diameter. (d) 110 μm in diameter.

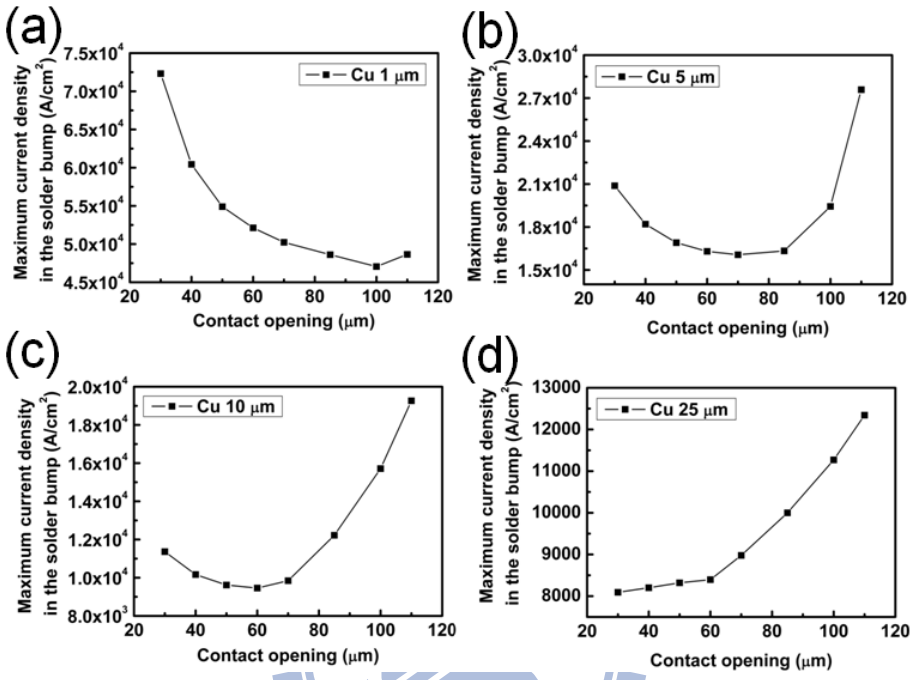


Figure 5-21: Maximum current density in the solder joints as a function of contact opening. (a) The solder joints with 1-μm-thick Cu UBM. (b) The solder joints with 5-μm-thick Cu UBM. (c) The solder joints with 10-μm-thick Cu UBM. (d) The solder joints with 25-μm-thick Cu UBM.

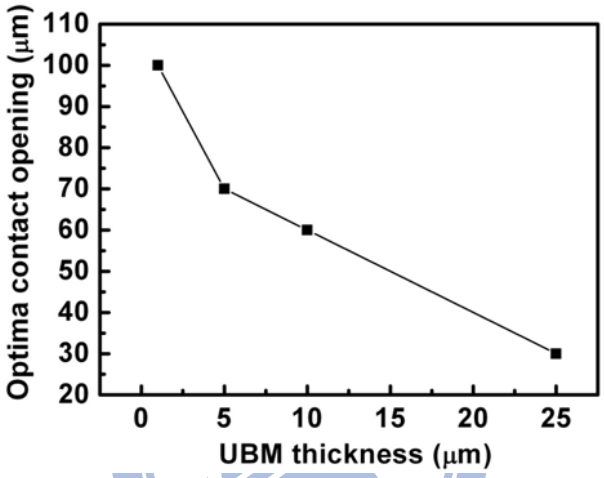


Figure 5-22: The optima contact opening for the solder joints as a function of UBM thickness.

5.1.6 Proposed optimal structures

The methods for relieving the current crowding effect inside the solder bumps fall into two categories: (1) moving the UBM/solder interface away from the current crowding region, and (2) suppressing current crowding at UBM/solder interface. If the UBM/solder interface can be moved away from the current crowding region, it can avoid the threat coming from the high current density. On the other hand, the methods for decreasing the temperature in the solder joints are quite similar to the methods for relieving the current crowding effect.

Here, the optimal structures to enhance the EM lifetime will be summarized. First, the higher resistance materials may be able to select as UBM materials. Second, the design of Al trace should be as thicker and wider as possible. Third, Cu column is the best choice since it is well used. Finally, try to find the optimal size of contact opening can be also useful if the Cu column cannot be adopted.

5.2 Future structures

Since the packaging technology of flip-chip solder joints continues to scale down, the tread of this technology should be discussed. First, the shrinkage of the solder joints needs to be investigated. Second, in 3D IC packaging, Si die would become thinner. The thickness effect of Si die on temperature in flip-chip solder joints is also studied.

5.2.1 Effect of bump size on current and temperature during current stressing

To investigate the bump size effect, the component dimensions of the model were scaled down to examine the change in current density and temperature. The diameter of Al pad, the width of Al trace and Cu line, the radii of passivation opening, UBM opening and the metallization opening, the bump height, the diameter of Cu pad, and pitch of two solder joints were decreased proportionally to 80%, 60%, 40% and 20%, respectively, of the standard model. Therefore, the width of Al trace decreased from 100 μm to 20 μm. The passivation, UBM, and metallization openings become 17, 24, and 28.8 μm in diameter, respectively. The diameters of Al pad and Cu pad reduced to 22 μm and 40 μm, respectively. The width of Cu line has changed to 16 μm, the bump height has diminished to be 28.9 μm, and the pitch decreased down to 80 μm. However, the thicknesses of Al trace, UBM layers, IMCs, and Cu line remained the same as "Model 100%". More detailed information for the dimensions of all the models were

listed in Table 5-4.

Figure 5-23 (a) illustrates the cross-sectional current density distribution for Model 100% along Z axis in the solder joints under 0.5 A. The current crowded in a small region of the solder joint near the entrance of Al trace. The maximum current density was 1.0×10^4 A/cm^2 in the top solder since the current density in Al trace is as high as 4.5×10^5 A/cm^2. The current entered into the solder joint from Al trace, and then drifted down vertically toward the substrate (along Y-axis), and also spread out laterally at the same time (along X-axis and Z-axis). Thus, the solder close to the entrance carried a high density of current. Figures 5-23 (b) through (e) show the current density distributions for Model 80%, Model 60%, Model 40% and Model 20%, respectively. As the solder shrank, the majority of the current still crowded into UBM and solder joints. Especially, when the size of the solder bump decreased to 20%, high current density appeared over half of UBM and larger regions in the solder bump. The maximum current density of Model 80%, Model 60%, Model 40% and Model 20% are 1.5×10^4 A/cm^2, 2.4×10^4 A/cm^2, 4.7×10^4 A/cm^2 and 1.5×10^5 A/cm^2, respectively, when they are supplied by 0.5 A current. Figure 5-24 summarizes the maximum current density as a function of UBM opening. Under the same applied current, the maximum current density was found to increase upon decreasing UBM opening. 20% model carried the highest maximum current and is about 15 times larger than that of

100% Model.

Figure 5-25 shows the trend of crowding ratio for all the five models. The crowding ratio indicates the degree of unbalance in the current distribution in the solder bump. It is realized that the current crowding effect would accelerate the EM damage because of the enhanced wind force in the current crowding region. The average current densities on the UBM opening are 4.4×10^3 A/cm^2 in Model 100%, 6.9×10^3 A/cm^2 in Model 80%, 1.2×10^4 A/cm^2 in Model 60%, 2.8×10^4 A/cm^2 in Model 40%, 1.1×10^5 A/cm^2 in Model 20%. The crowding ratio inside the solder in Model 100% is about 2.3, which means that the local current density is 2.3 times larger than the average one on UBM opening. Similarly, the crowding ratio is 2.1, 1.9, 1.7 and 1.4 for the Model 80%, 60%, 40% and 20%, respectively. It is interesting that the crowding ratio in Model 20% is the smallest among the five models. This may be attributed to the fact that the Model 20% has small UBM opening for electric conduction. Most of the opening area is in the current crowded region. In addition, the average current density for the Model 20% is also higher than the rest models. Thus, the current crowding effect can be relieved by decreasing the bump size. However, it is noteworthy that both the average and the maximum current densities are higher in smaller bumps. Thus the smaller bumps will fail earlier.

The dimension of Al trace has significant effect on the Joule heating of solder

bumps due to its large resistance. Figures 5-26 (a) through (e) show the temperature distribution in Al trace and in the solder bumps for the five models stressed by 0.5 A at 100 °C. It was found that the maximum temperature in Al trace in Model 100% was 108.4 °C, whereas it increased to 202.1 °C in Model 20%. This is because both the width and length of Al trace decreased upon reducing the joint size. Thus, the resistance of Al trace was 71.3, 90.8, 92.3, 96.1 and 115.0 mΩ for the five models. Since the heating power was equal to I^2R, the large Al-trace resistance induced higher joule heating since the heat dissipation was almost the same. Figures 5-27 (a) through (e) illustrates the cross-sectional temperature distributions in the solder bumps for the five models when they experienced an applied current of 0.5 A at 100 °C. A hot spot inside the solder bumps was observed near the entrance point of the Al trace by two reasons: First, the Al trace was the main heating source. The generated heat dissipated into the solder directly. Second, the current crowding effect induced local joule heating effect in the solder bump near the entrance of the Al trace. The average temperature was obtained by averaging the node temperatures in the center of the solder. The temperatures in the hot spot are 103.2 °C, 105.3 °C, 109.1 °C, 119.0 °C and 181.3 °C, respectively, when the five models are stressed by 0.5 A, whereas the average temperatures were 102.9 °C, 104.8 °C, 108.4 °C, 117.6 °C and 178.8 °C. A higher temperature increase was observed in smaller solder joints because of higher Joule

heating of the reduced Al trace. Figures 5-28 (a) and (b) show the hot-spot and average temperatures as a function of the applied current from 0.1 A to 0.5 A for the five models. At a lower stressing current of 0.1 A, the hot-spot and the average temperatures are almost the same. However, the temperature differs significantly at higher stressing currents. Model 20% has the highest increase in both hot-spot and average temperatures. For Model 100%, Model 80%, Model 60%, Model 40% and Model 20%, the differences in temperature between hot spot and average temperature are 0.3 °C, 0.5 °C, 0.7 °C, 1.4°C and 2.5 °C, respectively. For smaller solder joints, there is an increase temperature differences between the hot-spot and the average temperature.

Thermal gradient was built up across the solder bump due to the non-uniform temperature distribution. The thermal gradient was derived from the temperature difference between the hot-spot and the bottom of the solder on the substrate divided by the bump height. The thermal gradients for Model 100%, Model 80%, Model 60%, Model 40%, and Model 20% are 29 °C/cm, 82 °C/cm, 118 °C/cm, 340 °C/cm and 1530 °C/cm as shown in Figure 5-29. It can be observed that Model 20% exhibits the highest thermal gradient, which implies that as the solder becomes smaller, the thermomigration issue may become more critical.

Table 5-5 summaries MTTF ratios for all the simulated stressing conditions in this

study. As one can see, MTTF for the Model 20% at 0.1 A is still much shorter than that for Model 100% at 0.5A, since both the hot-spot temperature and the maximum current density are larger in Model 20%. Therefore, the current carrying capability for smaller bumps decreases significantly. Furthermore, the analysis indicates that the higher maximum current density is the main contributor for shorter MTTF in a smaller bump stressed. For example, the MTTF for 100% model is 5063 times longer than the 20% model at 0.5A, in which the current density effect contributes 130.2 times while the Joule heating effect contributes 38.9 times. Yet, for 40% and 20% models, the effect of Joule heating on MTTF becomes more significant than the current density effect. For 20% model stressed at 0.1 A, MTTF is 545 times longer than the 20% model stressed at 0.5 A. In this case, the Joule heating effect contributes 30 times, whereas the current density effect only contributes 18 times. Therefore, Joule heating effect plays a critical role on MTTF in very smaller bumps.

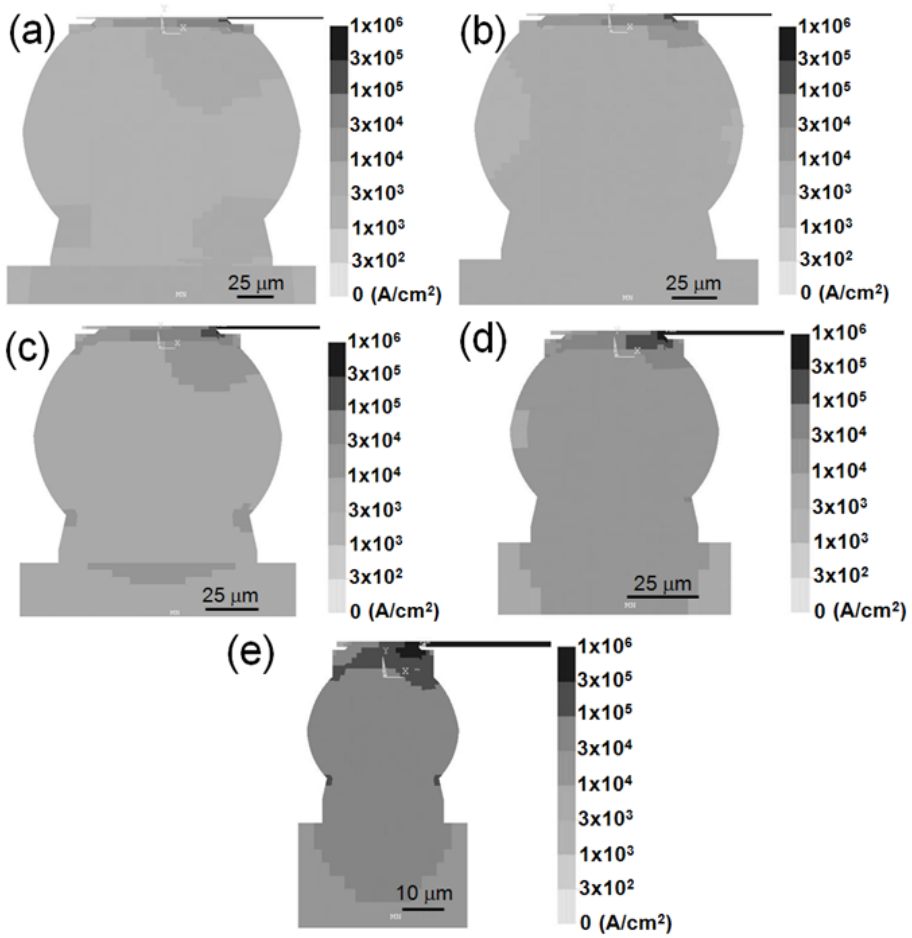


Figure 5-23: Cross-sectional view of current density distribution in the solder joints for (a) Model 100%, (b) Model 80%, (c) Model 60%, (d) Model 40%, (e) Model 20%. When a current of 0.5 A was applied.

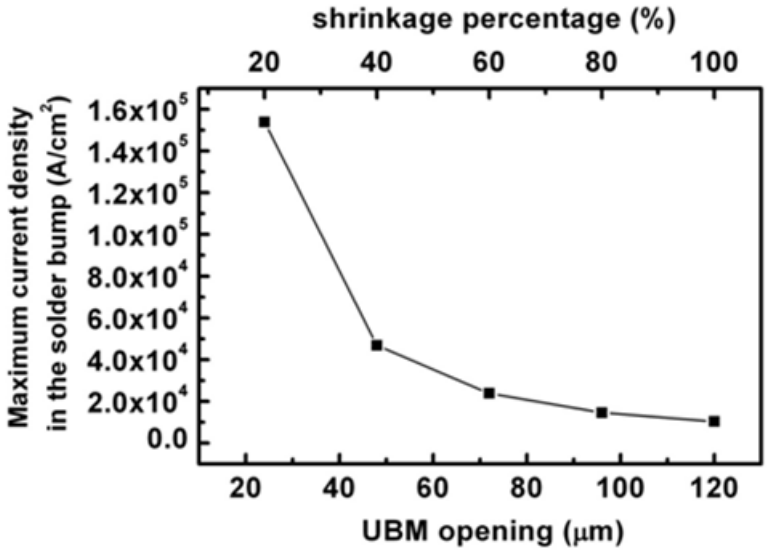


Figure 5-24: Plot of maximum current density in the solder bumps against the diameter of UBM opening.

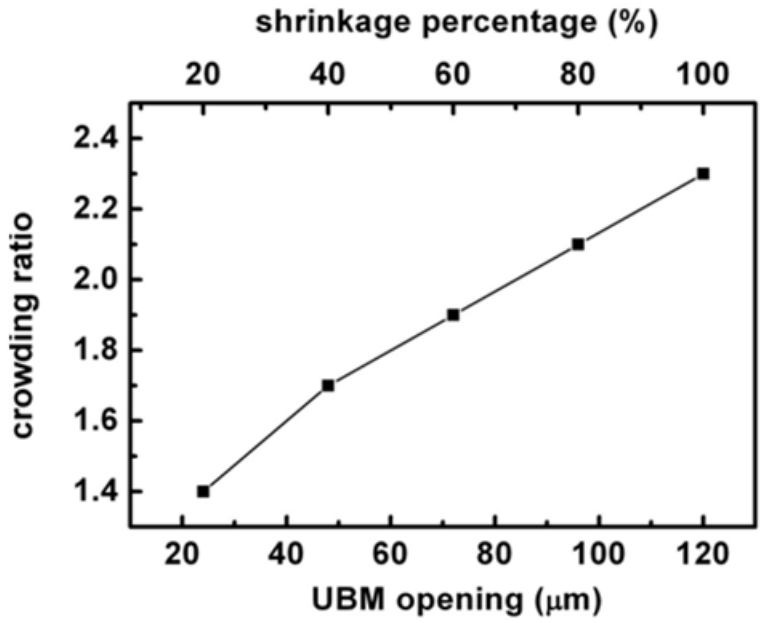


Figure 5-25: Plot of crowding ratio against the diameter of UBM opening.

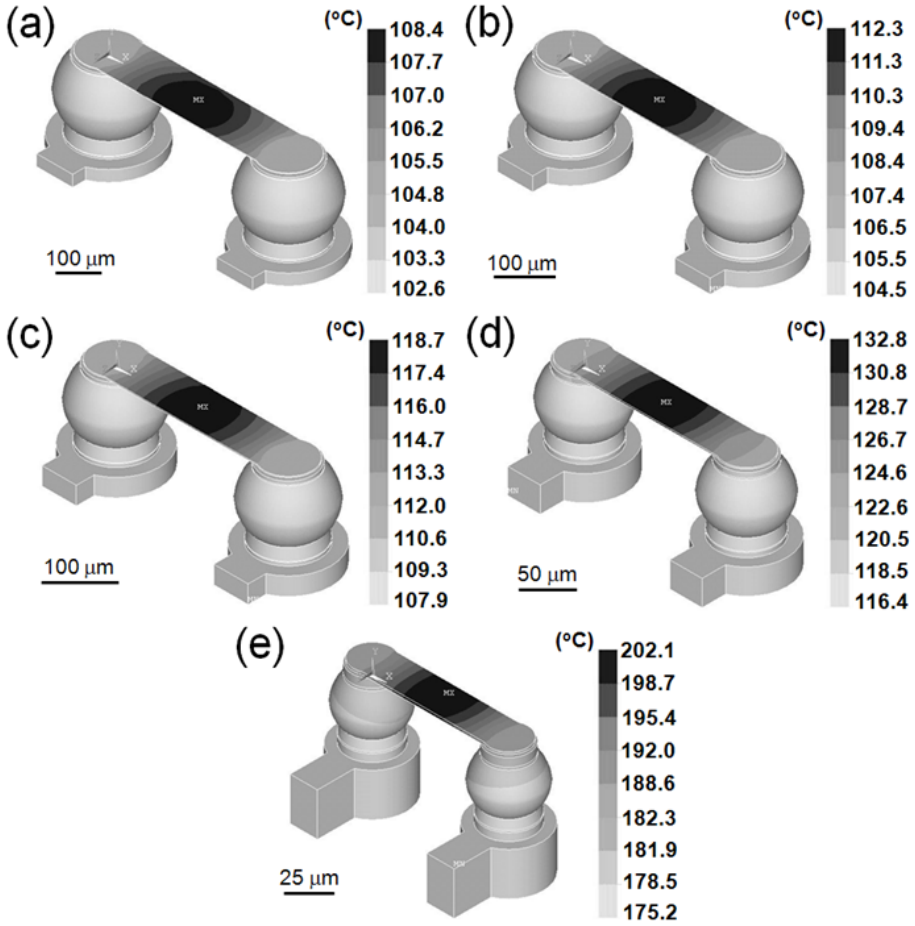


Figure 5-26: The Joule heating effect in the solder joints for: (a) Model 100%, (b) Model 80%, (c) Model 60%, (d) Model 40%, (e) Model 20%.When a current of 0.5 A was applied on 100 °C substrate.

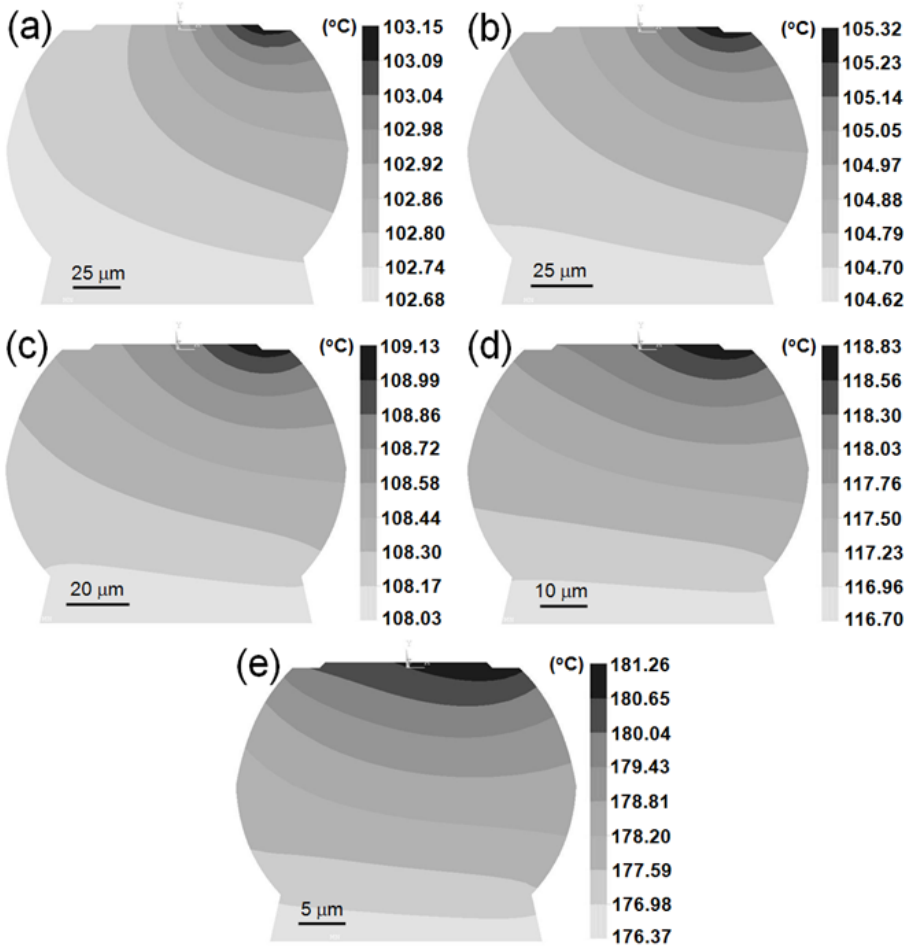


Figure 5-27: Cross-sectional view of the temperature distribution in the solder bumps for: (a) Model 100%, (b) Model 80%, (c) Model 60%, (d) Model 40%, (e) Model 20%. When a current of 0.5 A was applied and the substrate kept at 100 °C. Only the solder bumps are shown.

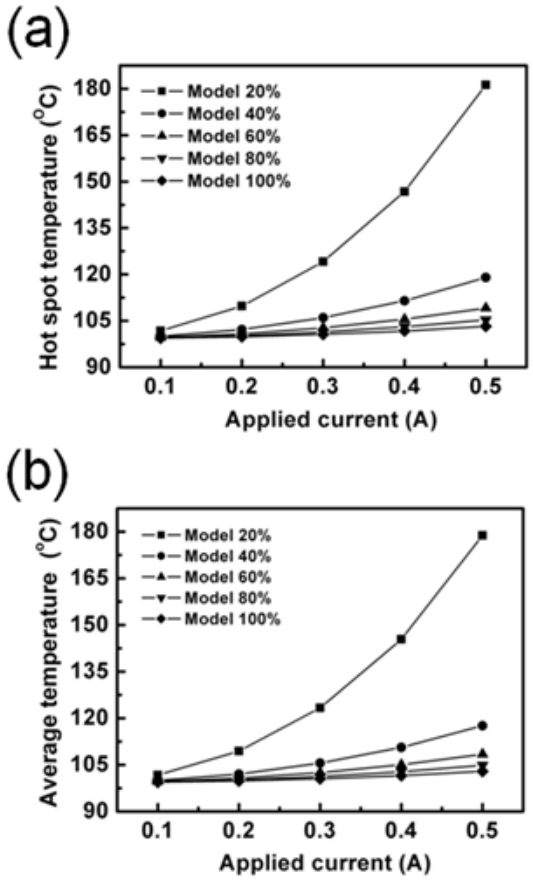


Figure 5-28: (a) Hot-spot temperature as a function of the applied current for the five models. The hot-spot temperature increases as the bump size decreased. (b) Average temperature in the solder as a function of the applied current for the five models. The average temperature increases as the bump size was decreased.

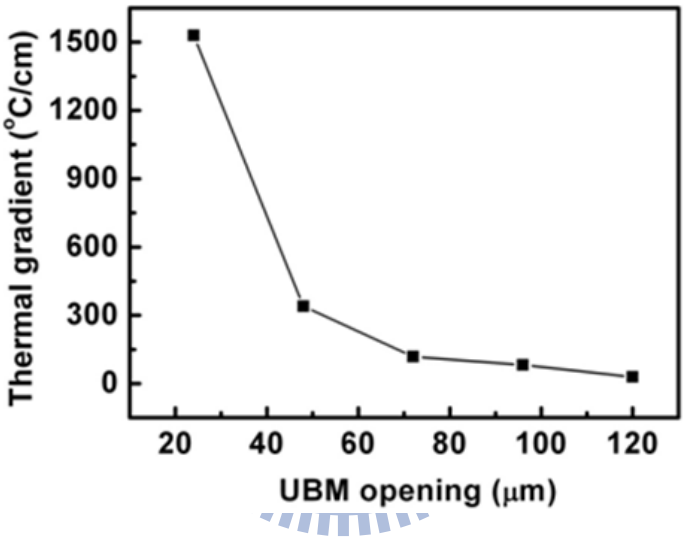


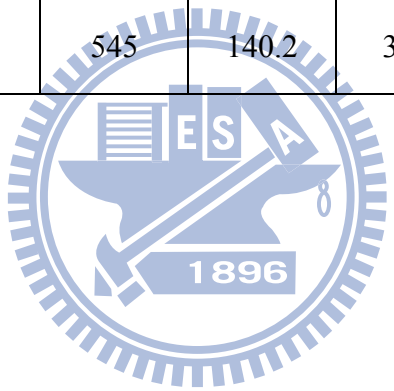
Figure 5-29: Thermal gradient as a function of the UBM opening. Significant thermal gradients were established when the solder size decreased.

Table 5-4: Dimensions for the five simulation models in this section.

unit: μm	Model 100%	Model 80%	Model 60%	Model 40%	Model 20%
diameter of Al pad	110	88	66	44	22
width of Al trace	100	80	60	40	20
pitch	400	320	240	160	80
contact opening	85	68	51	34	17
UBM opening	120	96	72	48	24
bump height	144.7	115.8	86.8	57.9	28.9
metallization opening	144	115.2	86.4	57.6	28.8
diameter of Cu pad	200	160	120	80	40
width of Cu line	80	64	48	32	16

Table 5-5: MTTF Ratio for the five models stressed at 0.1 A to 0.5 A. MTTF for Model 20% at 0.5 A is set as 1.0.

Applied current (A) / Model (%)	0.1	0.2	0.3	0.4	0.5
100	114008	31809	14643	8239	5063
80	61245	16893	7601	4042	2431
60	24813	6689	2893	1472	807
40	7221	1282	711	313	141
20	545	140.2	31.8	6.4	1



5.2.2 Effect on die thickness on current and temperature distribution during current stressing

To study the effect of Si thickness, the various die thicknesses from 50 μm to 750 μm were adopted for the simulation model of the package of the flip-chip solder joints. Since the structure of the circuit of the flip-chip solder was constant, the current density distribution would not change too much under this change. Therefore, the current density distribution will not be metioned in this section. The temperature distributions of Si dies and the solder bumps with 50 μm, 75 μm, 150 μm, 300 μm, 500 μm and 750 μm thick will be used to investigate the die thickness effect on flip-chip solder joints.

In Figures 5-30 (a) through (f), the temperature distributions of Si die with various thicknesses has been contoured. When Si die become thinner, the heat will not conduct through whole Si die. The heat from main heating source, i.e. Al trace, needs to dissipate by Si die or the substrate. Since Si is too thin to have good benefit on heat sink, the heat will pass through the underfill and BT substrate to spread out. On the other hand, when Si die is thick, it can help the heat to pass through by itself. Thus, the thick Si can sink the heat to reduce the temperature of the whole system.

However, in the solder bump, the temperature distribution is quite similar with each other for different die thickness as shown in Figure 5-31. It is worth to mention

that when Si thickness is less than 100 μm, as illustrated in Figures 5-31 (a) and (b), the high temperature area in the solder is bigger. That means the heat turns to pass in the solder since the Si die is too small to sink the heat.

As a function of die thickness, the hot spot temperature is plotted in Figure 5-32 (a). It was found that the hot spot temperature will not change a lot when the die thickness is larger than 300 μm. That may means the heat might sink by Si since the volume is enough to spread in the chip. However, if the die is less than 300 μm, the heat would like to use solder bump as the path of heat dissipation to increase the temperature in the solder joints. As a result, the heat cannot spread out by Si die efficiently, heat flux across the solder will increase. But the thermal conductivity of the solder joints is a constant, the thermal gradient in the solder joints will increase due to the decrease in die thickness. As the prediction, the thermal gradient in the solder joints increased as the die thickness decreased as shown in Fighre 5-32 (b).

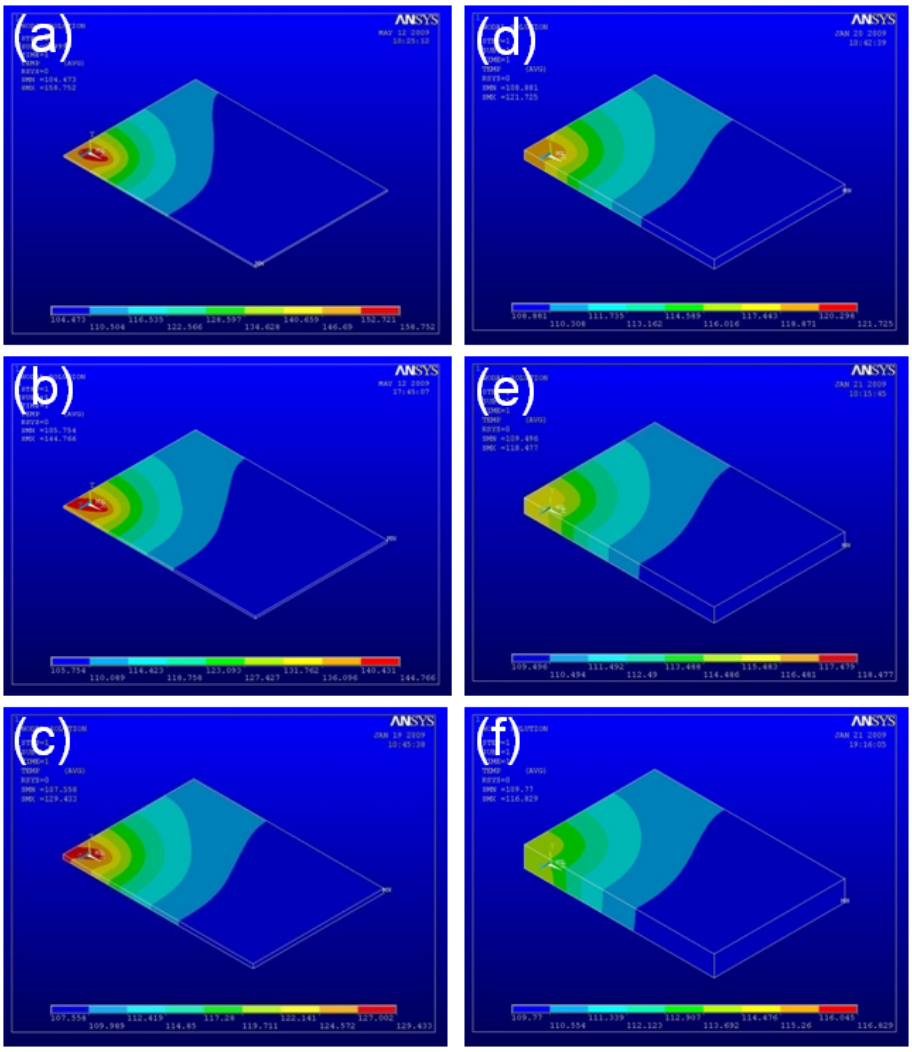


Figure 5-30: The temperature distribution of Si die only for: (a) 50-µm-thick Si, (b) 75-µm-thick Si, (c) 150-µm-thick Si, (d) 300-µm-thick Si, (e) 500-µm-thick Si, (f) 750-µm-thick Si. When a current of 0.6 A was applied on 100 °C substrate.

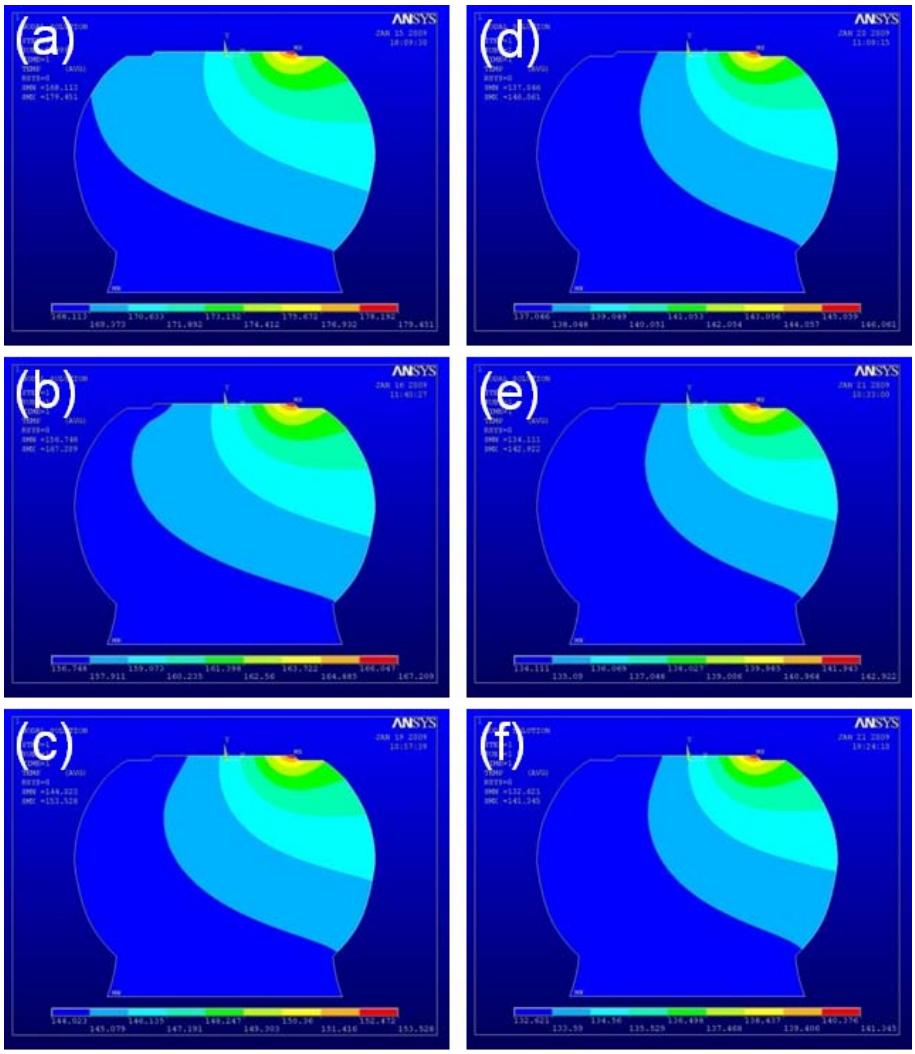


Figure 5-31: The cross-sectional temperature distribution of the solder bumps only for: (a) 50-µm-thick Si, (b) 75-µm-thick Si, (c) 150-µm-thick Si, (d) 300-µm-thick Si, (e) 500-µm-thick Si, (f) 750-µm-thick Si. When a current of 0.6 A was applied on 100 °C substrate.

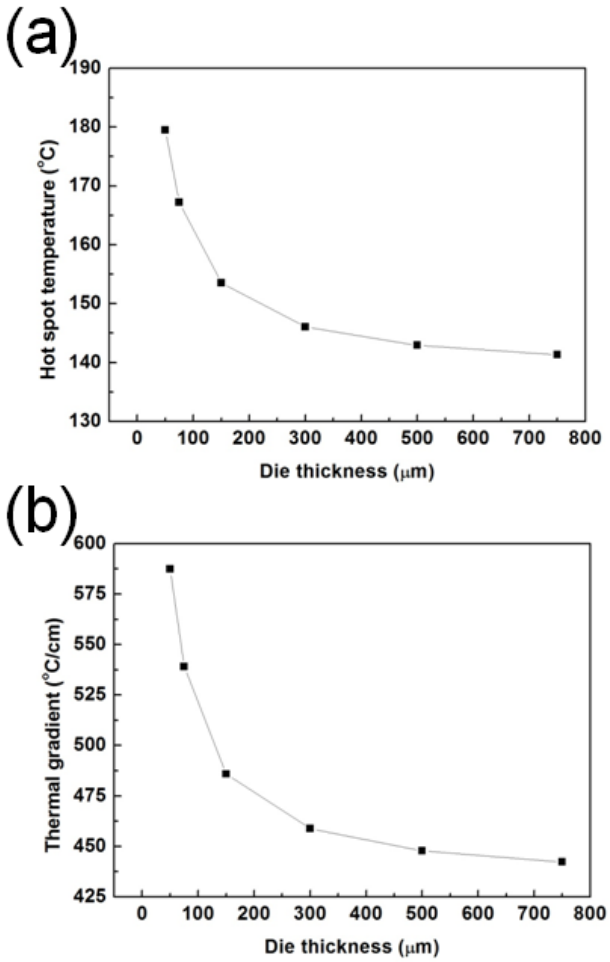


Figure 5-32: (a) Hot spot temperature in the solder joints as a function of die thickness.

(b) Thermal gradient across the solder joints as a function of die thickness.

Chapter 6 Conclusions

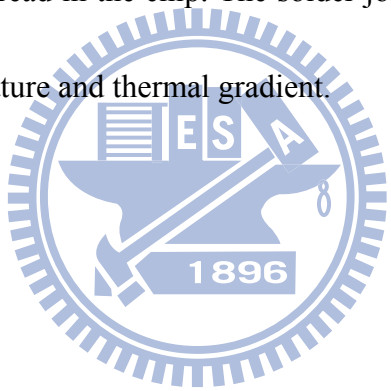
In conclusion, the finite-elements method was used to explain the experimental results well. It was known that the EM flux is proportional to the current density. Here, the higher EM velocity happened near the current crowding region has been investigated by FIB marker movement and current density distribution in the solder joints under current stressing. In addition, due to the line-to-bump geometry of flip-chip solder joints, the bump resistance would be different depended on the position of measurement. Moreover, it is able to have higher sensitivity to monitor the void formation and propagation based on the suitable position. The three-dimensional current density and temperature re-distributions due to void formation and propagation have been investigated in this thesis. It shows that void will grow owing to the current crowding and hot spot region step by step since it will block the conducting path and force to pass through the void. Then, the simulation and the temperature measurement by TCR effect have employed to analyze MTTF of the flip-chip solder joints. It was found the temperature is the key reason to affect MTTF since this factor is at the experiential term of Black's equation. Furthermore, the melting solder will come up in the final stage of current stressing. This is because Al trace was damaged under such stressing condition to increase the resistance. Therefore, the Joule heating effect increased the increase in temperature to over the

melting point of solder. Finally, the non-linear thermal gradient was reported due to the current crowding effect. Non-linear thermal gradient leads to modify the thermomigration flux since it is proportional to thermal gradient. Thus, the useful tool, simulation, can help to analysis the experiment data.

Not only for analyzing the experiment results, the simulation provides to predict the methods for relieving the current crowding effect and the Joule heating effect in the flip-chip solder joints under EM test. Therefore, the optimal structure for enhancing the EM lifetime will be discussed. It was determined that UBM materials, Al-trace design, UBM thickness, and size of contact opening will affect the current density distribution. As a result, the optimal structures to enhance the EM lifetime are going to be summarized. First, the higher resistance materials may be able to select as UBM materials. Second, the better design of Al trace is as thicker and wider as possible. Third, Cu column is the best choice since it is well used. Finally, try to find the optimal size of contact opening can be also useful if Cu column cannot be carried out.

To project the tendency of the flip-chip solder joints, the temperature and current distributions in the smaller solder bumps and reduced Si-die thickness were performed. The results revealed that as the solder joints became smaller, the solder bumps possessed a higher maximum current density and a higher hot-spot

temperature. On the other hand, as the solder size is reduced, the crowding ratio is also decreased. Therefore, the EM become a critical reliability issue as the solder joints continues to scale down. Also, the thermal gradient becomes larger due to the higher carrier current density and higher Joule heating effect. Then, the thermomigration issue will be another important issue in the future. Otherwise, when the thickness of Si die becomes thinner, the temperature and thermal gradient in the solder joints will get higher. The reason is that the heat would not sink by Si since the volume is not enough to spread in the chip. The solder joints need to carrier on more heat to increase the temperature and thermal gradient.



References

[1] J. H. Lau, *"Flip Chip Technology"* (McGraw-Hill, New York, 1995), p.123.

[2] E. M. Davis, W. E. Harding, R. S. Schwartz, and J. J. Corning, IBM J. Res. Develop. 44, 56 (2000).

[3] L. R. Miller, IBM J. Res. Develop., 239 (1969).

[4] P. A. Totta and R. P. Sopher, SLT device metallurgy and its monolithic extensions, IBM J. Res. Develop 13 (1969).

[5] K. Puttlitz and P. A. Totta, *"Area Array Interconnection Handbook"* (Kluwer Academic, Boston, MA, 2001).

[6] H. B. Huntigton, A.R. Grone, J. Phys. Chem. Solids 20, 76 (1961).

[7] K. N. Tu, J. Appl. Phys. 94, 5451 (2003).

[8] P. G. Shewmon, *"Diffusion in Solids"* (TMS, Warrendale, PA 1989), Chapter 7.

[9] I. A. Blech and C. Herring, Appl. Phys. Lett. 29, 131 (1976).

[10] I. A. Blech, J. Appl. Phys. 47, 1203 (1976).

[11] J. J. Clement and C. V. Thompson, J. Appl. Phys. 78, 900 (1995).

[12] S. Brandenburg and S. Yeh, in Proceedings of Surface MountInternational Conference and Exhibition, San Jose, CA, 1998, p. 337.

[13] K. Zeng and K. N. Tu, Mater. Sci. Eng. Rep. R38, 55 (2002).

[14] E. C. C. Yeh, W. J. Choi, K. N. Tu, P. Elenius, and H. Balkan, Appl. Phy. Lett. 80, 580 (2002).

[15] W. J. Choi, E. C. C. Yeh, and K. N. Tu, J. Appl. Phys. 94, 5665 (2003).

[16] T. L. Shao, S. W. Liang, T. C. Lin, and Chih Chen, J. Appl. Phys. 98, 044509 (2005).

[17] T. L. Shao, Thesis, National Chiao Tung University, 2005

[18] H. Ye, C. Basaran, and D. Hopkins, Appl. Phys. Lett. 82, 7 (2003).

[19] T. L. Shao, S. H. Chiu, Chih Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. 33, 1350 (2004).

[20] S. H. Chiu, T. L. Shao, Chih Chen, D. J. Yao, and C. Y. Hsu, Appl. Phys. Lett. 88, 022110 (2006).

[21] S. H. Chiu , Thesis, National Chiao Tung University, 2007

[22] K. N. Tu, C. C. Yeh, C. Y. Liu, and C. Chen, Appl. Phys. Lett. 76, 988 (2000).

[23] T. Y. Lee, K. N. Tu, and D. R. Frear, J. Appl. Phys. 90, 4502 (2001).

[24] L. Y. Zhang, S. Q. Ou, J. Huang, K. N. Tu, S. Gee, and L. Nguyen, Appl. Phy. Lett. 88, 012106 (2006).

[25] A. T. Huang, K. N. Tu, and Y. S. Lai, J. Appl. Phys. 100, 033512 (2006).

[26] J. W. Nah, J. O. Suh, K. N. Tu, S. W. Yoon, V. S. Rao, V. Kripesh, and F. Hua, J. Appl. Phys. 100, 123513 (2006).

[27] Y. H. Lin, Y. C. Hu, C. M. Tsai, C. R. Kao, and K. N. Tu, Acta Mater. 53, 2029 (2005).

[28] Y. S. Lai , K. M. Chen, C. L. Kao, C. W. Lee, and Y. T. Chiu, Microelectron. Reliab. 47, 1273 (2007)

[29] M. H. R. Jen, L. C. Liu, and Y. S. Lai, IEEE Trans. Compon. Packag. Technol. 32, 79 (2009).

[30] 何煇耀, 可靠度保證-工程與管理技術之應用: 中華民國品質學會發行

[31] J. R. Black, IEEE Trans. Electron Devices ED-16, 338 (1969).

[32] D. V. Ragone, *"Thermodynamics of Materials"* (Wiley, New York, 1995), Volume II, Chapter 8.

[33] D. R. Campbell, K. N. Tu, and R. E. Robinson, Acta Mater. 24, 609 (1976).

[34] W. Roush and J. Jaspal, in IEEE Proc. Thermomiration in Pb-In solder, 1982, p. 342.

[35] J. R. Lloyd, K. N. Tu, and J. Jaspal, *"Handbook of Lead-Free Solder Technology for Microelectronic Assemblies"* (CRC, New York, 2004), Chapter 20.

[36] K. N. Tu, *"Solder joint thechnology : Materials, Properties, and Reliability"* (Springer, New York, 2007), Chpater 12.

[37] A. T. Huang, A. M. Gusak, K. N. Tu, and Y. S. Lai, Appl. Phy. Lett. 88, 141911 (2006).

[38] A. T. Huang, Thesis, University of California Los Angeles, 2006

[39] http://www.apack.com.tw

[40] http://www.megic.com.tw

[41] http://www.aseglobal.com

[41] http://www.keithley.com

[43] http://www.home.agilent.com

[44] http://www.ni.com

[45] Y. W. Chang, Thesis, National Chiao Tung University, 2007

[46] W. R. Runyan, Technology Semiconductor Silicon, McGrow-Hill, (New York, 1965), p. 201

[47] http://www.ansys.com/

[48] N.F. Mott and H. Jones, *"The Theory of the Properties of Metals and Alloys"* Dover, (New York, NY, 1958), p. 242.

[49] http://www.mathworks.com/

[50] Clayton Paul, *"Fundamentals of Electric Circuit Analysis"* John Wiley & Sons, (2001).

[51] Yugnus A Cengel, "Heat transfer-A Practical Approach" McGrow-Hill, (New York, 2003), p. 26.

[52] Louis C. Burmeister, *"Convective Heat Transfer"* Wiley-Interscience, (1993) p. 107

[53] J. W. Nah, K. W. Paik, J. O. Suh, and K. N. Tu ,J. Appl. Phys. 94, 7560 (2003).

[54] Y. W. Chang, S.W. Liang, and Chih Chen, Appl. Phys. Lett. 89, 032103 (2006).

[55] Fan-Yi Ou Yang, Thesis, University of California Los Angeles, 2007

[56] H. Y. Hsiao and Chih Chen, Appl. Phys. Lett. 90, 152105 (2007)

[57] H. Y. Hsiao and Chih Chen, Appl. Phys. Lett. 94, 092107 (2009)

[58] H. C. Yu, S. H. Liu, and Chih Chen, J. Appl. Phys. 98, 013540 (2005).

[59] H. B. Huntington and A. R. Grone, J. Phys. Chem. Solids 20, 76 (1961).

[60] I. A. Blech, Acta Mater. 46, 3717(1998)

[61] Luhua Xu, John H. L. Pang, and K. N. Tu, Appl. Phys. Lett. 89, 221909 (2006).

[62] K. N. Tu, in Solder Joint Technology: Materials, Properties, and Reliability (Springer 2007), Chapter 6, p.175.

[63] C. M. Tsai, Y. S. Lai, Y. L. LIN, C. W. Chang, and C. R. Kao, J. Electron. Mater. 35, 1781 (2006)

[64] Minhua Lu, Da-Yuan Shih, Paul Lauro, Charles Goldsmith, and Donald W. Henderson, Appl. Phys. Lett. 92, 211909 (2008).

[65] B. F. Dyson, T. R. Anthony, and D. Turnbull, J. Appl. Phys. 38, 3408 (1967).

[66] D. C. Yeh and H. B. Huntington, Phys. Rev. Letter., 53, 1469 (1984).

[67] J. S. Kang, R.A. Gagliano, G. Ghosh, and M.E. Fine, J. Electron. Mater., 31, 1238-1243 (2002).

[68] S. J. Proctor and L.W. Linholm, IEEE Electron Device Lett., Vol. EDL-3, No. 10, p. 294 (1982)

[69] W. M. Loh, K. Saraswat, and R.W. Dutton, IEEE Electron Device Lett., Vol. EDL-6, No. 3, p. 105 (1985)

[70] M. Natan, S. Purushothan, and R. Dobrowski, J. Appl. Phys., 53, p5776 (1982).

[71] D. S. Liu, C. Y. Ni, Microelectronic Engineering, 63 363 (2002).

[72] International Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA (2003)

[73] S. N. Gee, N. Kelkar, J. Huang, and K. N. Tu, Proceedings of IPACK 2005 ASME InterPACK, San Francisco, California, USA.

[74] P. Su, M. Ding, T. Uehling, D. Wontor, P. S. Ho, Proceeding of Electronic Components and Technology Conference, IEEE Components, Packaging, and Manufacturing Technology Society, Lake Buena Vista, FL, 1431 (2005)

[75] B. Ebersberger, R. Bauer, and L. Alexa, Proceeding of Electronic Components and Technology Conference, IEEE Components, Packaging, and Manufacturing Technology Society, Lake Buena Vista, FL, 1407 (2005)

[76] H. J. Goldsmid, Thermoelectric Refrigeration (Plenum, New York, 1964)

[77] C. N. Liao, Chih Chen and K. N. Tu, J. Appl. Phys., 86, 3204 (1999)

[78] J. Zhang and D. Baldwin, Proceeding of IEEE 8th International Symposium on Advanced Packaging Materials, 97 (2002).

[79] M. Amagai, Y. Toyoda, T. Ohnishi, S. Akita, Proceeding of Electronic Components and Technology Conference, IEEE Components, Packaging, and Manufacturing Technology Society, Las Vegas, NV, 1304 (2004)

[80] T. L. Shao, Y. H. Chen, S. H. Chiu, and Chih Chen, J. Appl. Phys. 96, 4518 (2004).

[81] S. H. Chiu, Chih Chen, and D. J. Yao, J. Electron. Mater. 35, 1740 (2006).

[82] H. Gan and K. N. Tu, J. Appl. Phys. 97, 063514 (2005).

[83] J.R. Huang, C.M. Tsai, Y.W. Lin, and C.R. Kao, J. Mater. Res. 23, 250 (2008).

[84] H. Y. Hsiao, S. W. Liang, M. F. Ku, Chih Chen, and D. J. Yao, J. Appl. Phys. 104, 033708 (2008).

[85] Y. C. Hsu, T. L. Shao, C. J. Yang, and Chih Chen, J. Electron. Mater. 32, 1222 (2003).

[86] M. O. Alam, B. Y. Wu, Y. C. Chan, and K. N. Tu, Acta Mater. 54, 613 (2006).

[87] C. M. Tsai, Y. L. Lin, J. Y. Tsai, Y. S. Lai, and C. R. Kao, J. Electron. Mater. 35, 1005 (2006).

[88] C-K. Hu, M. B. Small, K. P. Rodbell, C. Stanis, P. Blauner, and P. S. Ho, Appl. Phys. Lett. 62, 1023 (1993).

[89] K-D Lee, E. T. Ogawa, H. Matsuhashi, P. R. Justison, K.-S. Ko, Paul S. Ho, and V. A. Blaschke, Appl. Phys. Lett., 79, 3236 (2001)

[90] C.-K. Hu, L. Gignac, E. Liniger, B. Herbst, D. L. Rath, S. T. Chen, S. Kaldor, A. Simon, and W.-T. Tseng, Appl. Phys. Lett., 83, 869 (2003)

[91] Yi-Shao Lai and Chin-Li Kao, Microelectron. Reliab. 45, 1357 (2006.)

[92] B. Y. Wu, Y. C. Chan, H. W. Zhong, M. O. Alam, J. K. L. Lai, Appl. Phys. Lett. 90, 232112 (2007).

[93] H. Y. Chen, Chih Chen, and K. N. Tu, Appl. Phys. Lett. 93, 122103 (2008).

[94] J. W. Nah, Kai Chen, K.N. Tu, B. R. Su, and Chih Chen, J. Mater. Res. 22, 763 (2007).

Vita

SHIH-WEI LIANG

EDUCATION

PhD (02/2005~-07/2009)

National Chiao Tung University, Taiwan

Department of Materials Science and Engineering

Advisor: Professor Chih Chen

BSc (09/2000~01/2005)

National Chiao Tung University, Taiwan

Major in Applied Mathematics

Minor in Materials Science and Engineering

SPECIALIZED KNOWLEDGE/ABILITY

- FIB operation for cross-section samples
- EM failure mode analysis by SEM and EDX
- EM failure statistic by Weibull distribution and MTTF calculation
- Thermo-electrical simulation on temperature and current density distribution in flip-chip solder joints
- Simulation on thermo-electrical coupling field

WORKING EXPERIENCE

PhD student in National Chiao Tung University, Taiwan (02/2005~-04/2008)

Key projects:

- The electromigration behavior for the flip-chip solder joints with thick Cu UBM
  (cooperate with **Megic**, Taiwan and **NSC**, Taiwan)
- Electromigration study of Flip-chip solder joints and 3D packaging
  (cooperate with **TSMC**, Taiwan)
- Electromigration reliability of flip-chip solder joints with SnAg and SnCu alloys
  (cooperate with **ASE**, Taiwan)

Exchange program in University of California, Los Angeles (04/2008~present)

Key projects:

- Electromigration and thermal migration of Pb-free flip chip solder joint (cooperate with **NSC**)
- Dynamic Equilibrium of IMC growth in Pb-free solder joint using V-groove sample (cooperate with **Hitachi**)
- Electromigration test and drop test in TSV structure and microbumps (cooperate with **ITRI**, Taiwan)

AWARDS & HONORS

1. 10/2007 **Best Paper Award** at **MRS-T, Taiwan**
2. 12/2007 **Graduate Students Study Abroad Program** form **NSC, Taiwan**
3. 08/2008 **Best Paper Award** at **PCB Society, Taiwan**

PUBLICATIONS

International Journals :

1. T.L. Shao, S.W. Liang, T.C. Lin, and Chih Chen*, Three Dimensional Simulation on Current Density Distribution in Flip-chip Solder Joints Under Electrical Current Stressing, ***J. Appl. Phys.***, 98(4), 044509, 2005. (第二作者) IF=2.498
2. S.W. Liang, T.L. Shao, Chih Chen*, Everett C.C. Yeh, and K.N Tu, Relieving the current crowding effect in flip-chip solder joints during current stressing, ***J. Mater. Res.***, 21(1), 137-146, 2006. (第一作者) IF=2.104
3. C.K. Chou, C.A. Chen, S.W. Liang, and Chih Chen*, Redistribution of Pb-rich phase during electromigration in eutectic SnPb solder stripes, ***J. Appl. Phys.***, 99(5), 054502, 2006. (第三作者) IF=2.498
4. S.W. Liang, Y.W. Chang, and Chih Chen*, Effect of Al-trace dimension on Joule heating and current crowding in flip-chip solder joints under accelerated electromigration, ***Appl. Phys. Lett.***, 88(17), 172108, 2006. (第一作者) IF=4.127
5. C.Y. Hsu, D.J. Yao*, S.W. Liang, Chih Chen, and Everett C.C. Yeh, Temperature and current-density distributions in flip-chip solder joints with Cu traces, ***J. Electronic Materials***, 35(5), 947-953, 2006. (第三作者) IF=1.358
6. S.W. Liang, Y.W. Chang, T.L. Shao, Chih Chen*, and K.N. Tu, Effect of 3-dimensional Current and Temperature Distribution on Void Formation and Propagation in Flip-chip Solder Joints during Electromigration, ***Appl. Phys. Lett.***, 89(2), 022117, 2006. (第一作者) IF=4.127
7. Y.W. Chang, S.W. Liang, and Chih Chen*, Study of void formation due to electromigration in flip-chip solder joints using Kelvin bump probes, ***Appl. Phys. Lett.***, 89(3), 032103, 2006. (第二作者) IF=4.127

8. S.W. Liang, Y.W. Chang, and Chih Chen*, Geometrical Effect of Bump Resistance for Flip-Chip Solder Joints: Finite-Element Modeling and Experimental Results, ***J. Electronic Materials***, 35(8), 1647-1654, 2006. (第一作者) IF=1.358
9. Chih Chen*, and S.W. Liang, invited review on "Electromigration Issues in Lead-Free Solder Joints", ***J. Mater. Sci. : Materials in Electronics***, 18(1-3), 259-268, 2007. (指導教授除外第一作者) IF=0.781
10. Ching-Jung Yang, Shun-Min Wang, Shih-Wei Liang, Yung-Huang Chang, Chih Chen*, and Jia-Min Shieh, Low-temperature growth of ZnO nanorods in anodic aluminum oxide on Si substrate by atomic layer deposition, ***Appl. Phys. Lett.***, 90(3), 033104, 2007. (第三作者) IF=4.127
11. S.W. Liang, S. H. Chiu, and Chih Chen*, Effect of Al-trace degradation on Joule heating during electromigration in flip-chip solder joints, ***Appl. Phys. Lett.***, 90(8), 082103, 2007. (第一作者) IF=4.127
12. S.W. Liang, Y.W. Chang, and Chih Chen*, 3-D Thermo-electrical Simulation in Flip-chip Solder Joints with Thick under Bump Metallizations during accelerated electromigration testing, ***J. Electronic Materials***, 36(2), 159-167, 2007. (第一作者) IF=1.358
13. Ching-Jung Yang, Chih Chen*, Pu-Wei Wu, Jia-Min Shieh, Shun-Min Wang, Shih-Wei Liang, Fabrication of Ordered Ta_2O_5 Nanodots Using Anodic Aluminum Oxide Template on Si Substrate, ***J. Mater. Res.***, 22(4), 1064-1071, 2007. (第六作者) IF=2.104
14. S.W. Liang, Y.W. Chang, and Chih Chen*, Relieving hot-spot temperature and current crowding effect of electromigration in solder bumps by Cu columns, ***J. Electronic Materials***, 36(10), 1348-1354, 2007. (第一作者) IF=1.358
15. Ching-Jung Yang, Shih-Wei Liang, Pu-Wei Wu*, Chih Chen, and Jia-Min Shieh, Fabrication of Anodic Aluminum Oxide Film on Large-Area Glass Substrate, ***Electrochemical and Solid-State Letters***, 10(12), C69-C71, 2007. (第二作者) IF=2.009
16. S.W. Liang, Y.W. Chang, Chih Chen*, Jackie Preciado, and K.N. Tu, Effect of Migration and Condensation of Pre-existing Voids on Bump Resistance Increase in Flip-Chip on Flexible Substrate during Electromigration, ***J. Electronic Materials***, 37(7), 962-967, 2008. (第一作者) IF=1.358
17. H.Y. Hsiao, S.W. Liang, M.F. Ku, Chih Chen*, and D.J. Yao, Direct measurement of hot-spot temperature in flip-chip solder joints under current stressing using infrared microscopy, ***J. Appl. Phys.***, 104(3), 033708, 2008. (第二作者) IF=2.498
18. Wei-Chih Kuan, S.W. Liang, Chih Chen*, Effect of bump size on current density

and temperature distributions in flip-chip solder joints, ***Microelectronics Reliability***, 49(5), 544-550, 2009. (第二作者) IF=1.011

19. S.W. Liang, H.Y. Hsiao, Chih Chen*, Luhua Xu, K.N. Tu, and Y.S. Lai, Non-uniform and negative marker displacements induced by current crowding during electromigration in flip chip Sn-0.7Cu solder joints, ***J. Electronic Materials***, in press, 2009. (第一作者) IF=1.358

International Conferences :

1. T.L. Shao, Shih-Wei Liang, and Chih Chen*, 3-D Current Density Simulation in Flip Chip Solder Joint under Electrical Current Stressing, Proceedings of the Minerals, Metals & Materials Society, San Francisco, CA, USA, February 13-17, 2005. (第二作者)
2. Sheng-Hsiang Chiu, Shih-Wei Liang, Chih Chen*, S.S. Lin, C.M. Chou, Y.C. Liu, K.H.Chen, Electromigration in eutectic SnPb solder bumps with Ni/Cu UBM, Advanced Packaging Materials: Processes, Los Angeles, CA, USA, March 16-18, 2005. (第二作者)
3. S.W. Liang, T. L. Shao, and Chih Chen*, 3-D Simulation on Current Density Distribution in Flip-Chip Solder Joints with Thick Cu UBM under Current Stressing, Proceedings of the Electronic Components and Technology Conference, Packaging, and Manufacturing Technology Society, Orlando, FL, USA, May 31-June 3, 2005. (第一作者)
4. S.W. Liang, Y.W. Chang, T.L. Shao, and Chih Chen*, Mechanism of Void Formation in Flip-Chip Solder Joints, Proceedings of the Minerals, Metals & Materials Society, San Antonio, TX, USA, March 12-16, 2006. (第一作者)
5. Y.W. Chang, S.W. Liang, and Chih Chen*, Electromigration study Using Kelvin Bump Structure, Proceedings of the Minerals, Metals & Materials Society, San Antonio, TX, USA, March 12-16, 2006. (第二作者)
6. S.H. Chiu, S.W. Liang, Chih Chen*, D. J. Yao, Y. C. Liu, K. H. Chen, and S. H. Lin, Joule Heating Effect under Accelerated Electromigration in Flip-chip Solder Joints, Proceedings of the Electronic Components and Technology Conference, Packaging, and Manufacturing Technology Society, San Diego, CA, USA, May 30- June 2, 2006. (第二作者)
7. S.W. Liang, Y.W. Chang, and Chih Chen*, Geometrical Effect of Bump Resistance for Flip-Chip Solder Joints during Electromigration Test measured by Kelvin Probes, MRS Fall 2006 Symposium V: Advanced Electronic Packaging, Boston, MA, USA, November 27-December 1, 2006. (第一作者)
8. S.W. Liang, Y.W. Chang, and Chih Chen*, Effect of Thickness of Cu Under-Bump-Metallization on the Electromigration Lifetime of Flip-Chip Solder

Joints, Proceedings of the Minerals, Metals & Materials Society, Orlando, FL, USA, February 25-March 1, 2007. (第一作者)

9. C.K. Lin, S.W. Liang, and Chih Chen*, Electromigration in Gold Bumps on Flexible Substrates under High Current and High-electrical Field, Proceedings of the Minerals, Metals & Materials Society, Orlando, FL, USA, February 25-March 1, 2007. (第二作者)
10. S.W. Liang, S.H. Chiu, and Chih Chen*, Effects of Current Crowding and Joule Heating on Reliability of Solder Joints, 9th International Workshop on Stress-Induced Phenomena in Metallization, Kyoto, Japan, April 4-6, 2007. (第一作者)
11. S.W. Liang and Chih Chen*, Effect of Thickness of Under-Bump-Metallization on the Electromigration Lifetime of Flip-Chip Solder Joints, IEEE 2008 Pan Pacific Microelectronics Symposium, Kauai, Hawaii, USA, January 22-24, 2008. (第一作者)
12. S.W. Liang and Chih Chen*, Effect of Al Trace Width on Electromigration Failure Time of Flip-Chip Solder Joints, Proceedings of the Minerals, Metals & Materials Society, New Orleans, LA, USA, March 9-13, 2008. (第一作者)
13. S.W. Liang and Chih Chen*, Direct Measure the Current Crowding Effect in Flip-Chip Solder Joints, Proceedings of the Minerals, Metals & Materials Society, San Francisco, CA, USA, February 15-19, 2009. (第一作者)
14. S.W. Liang, Chih Chen*, J.K. Han, Luhua Xu, and K.N. Tu, IMC Formation to Block Whisker and Hillock Growth in Lead-Free Flip-Chip Solder Joints under Electromigration, Proceedings of the Minerals, Metals & Materials Society, San Francisco, CA, USA, February 15-19, 2009. (第一作者)
15. S.W. Liang and Chih Chen*, Optima Design of Contact Opening for Relieving Current Crowding Effect in Flip-Chip Solder Joints, IEEE EuroSimE 2009, Delft, The Netherlands, April 27-29, 2009. (第一作者)
16. Luhua Xu, S.W. Liang, Di Xu, Jung-Kyu Han, Jarrett Liang, and K. N. Tu, Electromigration Failure with Thermal Gradient Effect in SnAgCu Solder Joints with Various UBM, Proceedings of the Electronic Components and Technology Conference, Packaging, and Manufacturing Technology Society, San Diego, CA, USA, May 26-29, 2009. (第二作者)

Domestic Journals :

1. 楊慶榮, 陳智*, 王舜民, 梁世緯, 謝嘉民, 利用鋁陽極處理模板輔助製作高規則排列氧化鈤奈米柱陣列於矽基材之研究, 奈米通訊期刊,新竹,中華民國. (第四作者)

Domestic Conferences :

1. 梁世緯, 林大鈞, 邵棣樑, 陳智*, 覆晶銲錫中電流密度分佈的三度空間模擬, 材料年會, 新竹, 中華民國, Nov. 17-18, 2004. (第一作者)
2. S. W. Liang, Y. W. Chang, Chih Chen*, Y. C. Liu, K. H. Chen, and S. H. Lin, Geometrical Effect of Bump Resistance for Flip-Chip Solder Joints, IMAPS-Taiwan 2006 Technical Symposium, Taipei, Taiwan, ROC, June 28-July 1, 2006. (第一作者)
3. S.W. Liang (梁世緯), Y.W. Chang (張元蔚), and Chih Chen* (陳智), Cu Column Effect in Flip-Chip Solder Joints during Electromigration Test, 材料年會, 台南, 中華民國, Nov. 24-25, 2006. (第一作者)
4. 梁世緯, 陳智*, 鋁導線的寬度效應影響覆晶封裝無鉛銲錫的電遷移壽命之研究, 材料年會, 新竹, 中華民國, Nov. 16-17, 2007. (第一作者)
5. 梁世緯, 陳智*, 杜經寧, 賴逸少, 直接量測在覆晶封裝銲錫接點之電流集中效應, 材料年會, 台北, 中華民國, Nov. 21-22, 2008. (第一作者)