# 以凱文結構與三維模擬研究電遷移造成覆晶銲錫接點中孔洞的形成

學生：張元蔚　　　　　　　　　指導教授：陳智

國立交通大學材料科學與工程學系（研究所）碩士班

## 摘　要

近年來由於電子元件不可避免地走向輕、薄、短、小等趨勢，為增加接點密度、提升反應時間，銲錫接點內的電遷移現象逐漸成為熱門的研究範圍。在電遷移測試中，因為電流集中效應的原因，孔洞通常生成於與導線相接處，亦即電子流進入處，可是孔洞的生成與成長機制目前還未有清楚的研究。在鋁、銅等金屬接點中，孔洞的成核與成長皆可利用電阻的變化來坐標定與觀測，可是對銲錫接點而言，銲錫接點的電阻遠較一般的金屬導線與接點小，所以以往研究電遷移效應時所用的雛菊花環結構無法感測到銲錫電阻隨微結構產生的微小變化。在本研究中，我們設計製作了凱文銲錫球接點結構，並利用此結構在電遷移測試中來對銲錫接點作量測，此外在本研究中也利用三維立體的有限元素分析模型，對銲錫電阻因孔洞產生的變化做進一步的分析。本研究提供一個研究覆晶銲錫接點電遷移測試破壞機制的系統性方法。

Study of void formation due to electromigration in flip-chip solder joints using Kelvin bump probes and 3-D Simulation

Student：Yuan-Wei Chang Advisor：Dr. Chih Chen

Department of Materials Science and Engineering

National Chiao Tung University

## Abstract

Electromigration of flip-chip solder joints has been studied extensively in recent years. Voids formed at the solder in the vicinity of the entrance point of the Al trance for solder joints with thin film UBM. However, the nucleation and propagation of the voids is still not clear. For Al and Cu inter-connects, void nucleation and propagation during electromigration is monitored by resistance change. But the bump resistance is quite small compared with the resistance of the metallization traces. Therefore, daisy-chain structure cannot detect the slight changes in microstructure in the solder joint. In this study, we designed and fabricated Kelvin bump probe, and used it to monitor the bump resistance change during electromigration successfully. Three-dimensional (3D) finite element modeling was also performed to simulate the bump resistance increase due to void formation. This approach facilitates the systemic study of failure mechanism due to electromigration in flip-chip solder joints.