國　立　交　通　大　學

電子物理學系

碩士論文

新穎堆疊矽/鍺 T 型閘極複晶矽薄膜電晶體

A Novel Poly-Silicon Thin-Film Transistors with Stacked Si/Ge T-Gate

研 究 生：謝佩珊

指導教授：趙天生 博士

中華民國 九十五年 六月

新穎堆疊矽/鍺 T 型閘極複晶矽薄膜電晶體

A Novel Poly-Silicon Thin-Film Transistors with Stacked Si/Ge T-Gate

研 究 生：謝佩珊 Student：Pei-Shan Hsieh

指導教授：趙天生 博士 Advisor：Tien-Sheng Chao

國 立 交 通 大 學

電子物理學系

碩士論文

A Thesis
Submitted to Department of Electrophysics
National Chiao Tung University
In partial Fulfillment of the Requirements
For the Degree of Master of Science
In
Electrophysics

June 2006
HsinChu, Taiwan, Republic of China

中華民國 九十五年 六月

新穎堆疊矽/鍺 T 型閘極複晶矽薄膜電晶體

研究生：謝佩珊　　　　　　　　　　　指導教授：趙天生 博士

國立交通大學

電子物理學系

摘要

多晶矽薄膜電晶體擁有高載子遷移率目前被廣泛地運用在主動矩陣式液晶顯示器開關元件，然而，在汲極端產生的強電場會造成嚴重漏電流和元件不穩地性，將會阻礙多晶矽薄膜電晶體在高效能積體電路的應用。造成漏電的主要因素是由於在汲極端附近的強電場經由顆粒邊界的受限載子引起場發射而使漏電上升。

在本論文中，我們針對多晶矽薄膜電晶體提出新的製程方法，此製程簡單無需額外的光罩，或是離子佈植步驟，即可形成堆疊矽/鍺T型閘極元件，期可達到抑制電場效果。利用模擬軟體來分析證明，藉由T型閘極可有效降低汲極端附近的電場。

我們對於堆疊矽/鍺T型閘極複晶矽薄膜電晶體，探討其元件特性，包括傳輸性能、開/關電流比、漏電強度、輸出性能，以及熱載子可靠度分析。由結果顯示，堆疊矽/鍺T型閘極複晶矽薄膜電晶體，可使漏電流降低，並提升開/關電流比，此外Kink效應及熱載子可靠度也明顯優於傳統元件。

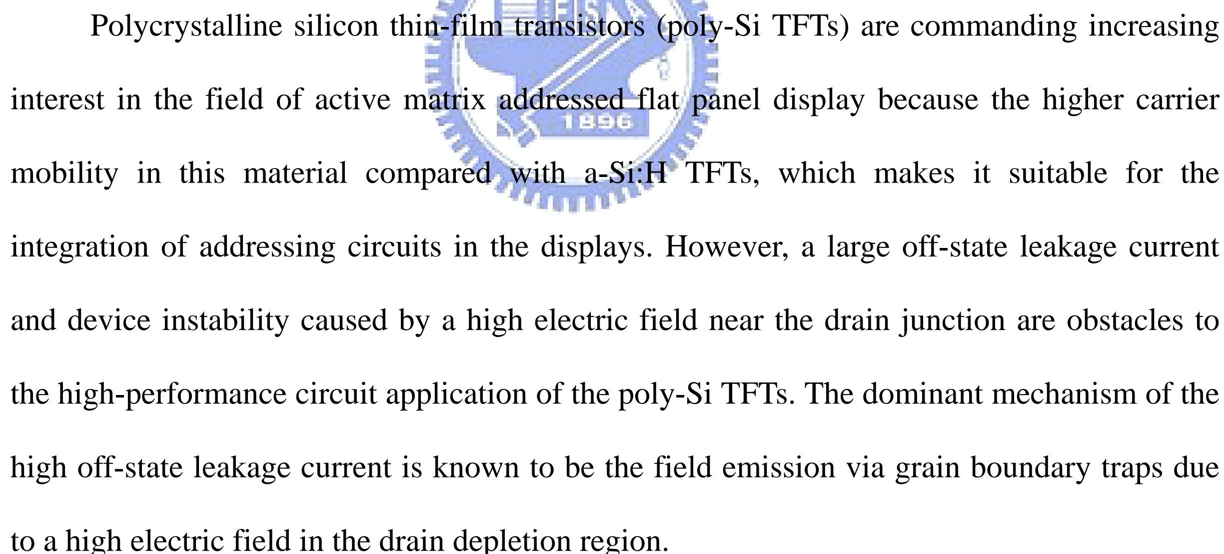
A Novel Poly-Silicon Thin-Film Transistors with Stacked Si/Ge T-gate

Student：Pei-Shan Hsieh　　　Advisors：Dr. Tien-Sheng Chao

Department of Electrophysics

National Chiao Tung University

Abstract



Polycrystalline silicon thin-film transistors (poly-Si TFTs) are commanding increasing interest in the field of active matrix addressed flat panel display because the higher carrier mobility in this material compared with a-Si:H TFTs, which makes it suitable for the integration of addressing circuits in the displays. However, a large off-state leakage current and device instability caused by a high electric field near the drain junction are obstacles to the high-performance circuit application of the poly-Si TFTs. The dominant mechanism of the high off-state leakage current is known to be the field emission via grain boundary traps due to a high electric field in the drain depletion region.

In this thesis, we have proposed a new fabrication method of poly-Si TFT without a troublesome ion implantation or any additional mask. This device employs the stacked Si/Ge T-Gate to suppress the electric field. It was verified by the devices simulator that the electric field is reduced near the drain junction by the T-Gate structure.

We have investigated the electrical characterizations of the Si/Ge T-gate TFTs

including the transfer characteristics, On/Off current ratio, off -state leakage, output characteristics and hot carrier stress. The results show that the Si/Ge T-Gate TFT give low off-state leakage, the suppress of floating body effect, good On/Off current ratio and better hot carrier reliability.

誌謝

兩年短暫的碩班生活，匆匆走過卻不虛此行，而此論文也為求學生涯畫下短暫的句點。一路走來，受到許多人的關心幫助，在此表達感謝之意。首先要感謝指導教授趙天生老師在學業及實驗上給予最大的支持與協助，此外在為學處世及待人接物上也都讓我有相當多啟發。此外，我要特別感謝東海大學的蕭錫鍊老師，大學兩年的專題指導，讓我更早認知研究生態，及學習實驗研究精神。

再者要特別感謝郭柏儀學長，在實驗、研究上熱心無私的指導，使我獲得許多寶貴的實驗經驗，而學長的認真執著的研究精神，也是我永遠的學習榜樣。此外，也感謝當初和我們同時進入實驗室的吳偉成學長，絕佳領導風範及特別的人生哲學，讓我有更開闊的視野及想法。另外，還要感謝浪費寶貴時間聽我們報告的羅文政學長，告訴我們許多人生道理的李耀仁學長，熱心認真的吳家豪學長，以及協助我找到好工作的張宗憲學長，有大家這一路的提攜照顧，實在感激不盡。

同時，也要謝謝竣祥、彥學、武欽、棟煥，有幸能夠當同學，一起上課、做實驗、寫論文，度過充實的兩年，真的非常有緣。另外也要感謝可愛搞笑的學弟妹，美君、國興、宗諭、德馨、宜憲、妍心、明宏、家塵，枯燥單板的碩班生活，有了妳們的加入，讓實驗室常常充滿歡笑，也讓我的回憶更加美好精采，然而也要特別謝謝宗諭，在實驗模擬上的幫忙，使我的論文更加完整。

感謝國家奈米元件實驗室和交通大學奈米中心在儀器設備上的支援，以及每位工程師在製程上的幫忙。對於諸位口試委員的建議與指證也表感激之意。

最後，我要對我的父母表達我最深的敬意及感謝，二十多年來，辛苦工作省吃儉用，讓我擁有優良的讀書環境，無怨無悔地付出，令我非常感激，還有非常感謝我摯愛的弟弟、妹妹，在人生路上的陪伴支持與鼓勵。

Contents

Abstract (Chinese)……………………………………………………………I

Abstract (English)……………………………………………………………II

Acknowledge…………………………………………………………………..IV

Contents………………………………………………………………………V

Table captions………………………………………………………………VII

Figure captions……………………………………………………………VIII

Chapter 1 Introduction……………………………………………………1

1.1 Overview of Thin-Film Transistor Technology………………………………....1

1.2 Motivation…………………………………………………………………….... 2

1.3 Thesis Outline………………………………………………………………….. 3

Chapter 2 Experimental Process and Electrical Parameters Extraction….

…………………………………………………………………………… 5

2.1 Fabrication of the thin-film transistors (TFTs)…………………………….... 5

2.1.1 Fabrication of the Si/Ge T-Gate TFTs……………………………...5

2.1.2 Fabrication of the Conventional TFTs……………………………... 6

2.2 Method of device parameter extraction……………………………………...... 8

2.2.1 Threshold Voltage (V_{TH})……………………………………………..... 8

2.2.2 Subthreshold Swing (S.S.)…………………………………………….. 8

2.2.3 On/Off Current Ratio………………………………………………...... 9

2.3 Material analysis……………………………………………………….…...... 10

Chapter 3 Electrical Characterization of the Si/Ge T-Gate TFTs............. 17

3.1 Device Simulation…………………………………………………………… 17

3.2 Basic Electrical Characteristics of Si/Ge T-Gate TFTs……………………....... 18

3.2.1 Transfer Characteristics……………………………………………………... 18

3.2.2 On /Off Current Ratio…………………………………………………...... 20

3.2.3 Off -State Leakage………………………………………………………... 21

3.2.4 Output Characteristics……………………………………………….…... 21

3.2.5 Hot Carrier Stress……………………………………………………...... 23

Chapter 4 Conclusions and Future Works………………………………… 64

4.1 Conclusions……………………………………………………………………64

4.2 Future Works………………………………………………………………...65

References ……………………………………………………………………......67

Table Captions

Chapter 2

Table2.1 Split condition for all samples with different thickness of stacked Si/Ge and undercut length.

Table2.2 Split conditions for control devices.

Figure Captions

Chapter 2

Fig.2.1 The schematic cross section of the Si/Ge T-gate TFTs with TEOS passivation

Fig.2.2 The schematic cross section of the Si/Ge T-gate TFTs with Si_3N_4 passivation

Fig.2.3 The schematic cross section of conventional TFTs

Fig.2.4 Process flows of Si/Ge T-gate TFTs.

Chapter 3

Fig.3.1 Stacked Si/Ge gate with the germanium undercut structure observed by cross section TEM microphotographs.

Fig.3.2 Thickness of channel film, gate oxide, gate, and undercut length are shown in this picture.

Fig.3.3 SEM image of the Stacked Si/Ge gate with undercut structure.

Fig.3.4 The simulated lateral electric field along the channel (10 μm) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) Undercut length is 400nm. (b) Undercut length is 800nm.

Fig.3.5 The simulated vertical electric field along the channel (10 μm) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) undercut length is 400nm. (b) undercut length is 800nm.

Fig.3.6 The simulated lateral electric field along the channel (10 μm) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) undercut length is 400nm. (b) undercut length is 800nm.

Fig.3.7 The simulated vertical electric field along the channel (10 μm) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) undercut length is 400nm. (b) undercut length is 800nm.

Fig.3.8 The simulated lateral electric field along the channel (10 μm) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

Fig.3.9 The simulated vertical electric field along the channel (10 μm) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

Fig.3.10 The simulated lateral electric field along the channel (10 μm) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

Fig.3.11 The simulated vertical electric field along the channel (10 μm) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

Fig.3.12 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 5 μm.

Fig.3.13 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 8 μm.

Fig.3.14 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 5 μm.

Fig.3.15 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 3 μm.

Fig.3.16 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate

length is 10 μ m.

Fig.3.17 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 8 μ m.

Fig.3.18 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 5 μ m.

Fig.3.19 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 3 μ m.

Fig.3.20 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 10 μ m.

Fig.3.21 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 8 μ m.

Fig.3.22 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 5 μ m.

Fig.3.23 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 3 μ m.

Fig.3.24 Gate length dependence of On/ Off current ratio in Si/Ge T-gate TFTs with TEOS passivation and conventional TFT. (a) The channel thickness is 50nm (b) The channel thickness is 100nm.

Fig.3.25 Gate length dependence of On/ Off current ratio in Si/Ge T-gate TFTs with Si_3N_4

passivation and conventional TFT.

Fig.3.26 Off-state leakage Characteristics in Si/Ge T-gate TFTs with TEOS passivation which compared with conventional TFT. (a) The channel thickness is 50nm (b) The channel thickness is 100nm.

Fig.3.27 Off-state leakage Characteristics in Si/Ge T-gate TFTs with Si_3N_4 passivation which compared with conventional TFT.

Fig.3.28 The output characteristics of the Si/Ge T-Gate TFTs with TEOS passivation. The channel thickness is 50nm. (a) Germanium layer thickness is 50nm (b) Germanium layer thickness is 100nm.

Fig.3.29 The output characteristics of the Si/Ge T-Gate TFTs with TEOS passivation .The channel thickness is100nm. (a) Germanium layer thickness is 50nm (b) Germanium layer thickness is 100nm.

Fig.3.30 The output characteristics of the Si/Ge T-Gate TFTs with Si_3N_4 passivation. The channel thickness is 50nm. (a) Germanium layer thickness is 50nm (b) Germanium layer thickness is 100nm.

Fig.3.31 Stress time dependence of I_{on} variation in Si/Ge T-Gate TFTs and conventional TFT. (a) Channel length is 10μm. (b) Channel length is 5μm.

Fig.3.32 Variations of the threshold voltage under hot carrier stress in conventional TFT and Si/Ge T-Gate TFTs. (a) Channel length is 10μm. (b) Channel length is 5μm.

Chapter 4

Fig.4.1 The schematic cross section of stacked Si/Ge T-Gate TFT with O/N/O tripping layer.

Chapter 1

Introduction

1.1. Overview of Thin-Film Transistor Technology

A thin film transistor (TFT) is defined as a field-effect transistor built using a semiconductor thin film which is originally deposited on an insulating material [1].We usually use the amorphous-Si and poly-Si as the thin film materials.

Most of TFT-LCD products were fabricated using a-Si:H TFTs as the pixel devices because of their advantages, such as low processing temperature (<350°C), good compatibility with large area glass substrate, simple process, and low leakage current, which is suitable for pixel switching. However, a-Si:H TFT's have some inherent undesirable properties. First of all, its carrier mobility is extremely low (typically below 1 $cm^2/V\text{-}s$), which will prohibit the integration of driver circuitry on the active matrix plate. Furthermore, the quality of gate dielectric and oxide-poly interface is not good enough because of the low temperature process. Therefore, the mobile carriers from the source may somewhat leak to gate terminal or suffer lots of scatterings at the interface during the transport process. As the display area and pixel density of TFT-LCD are increasing, the TFT-LCD pixel driver needs to use high mobility in order to shorten the charging time of pixel electrodes. It is very difficult for a-Si:H TFT because of its low carrier mobility.

Recently, polycrystalline silicon thin-film transistors (poly-Si TFTs) are commanding increasing interest in the field of active matrix addressed flat panel display because the higher carrier mobility in this material, compared with a-Si:H TFTs, makes it suitable for the integration of addressing circuits in the displays.[2] In comparing poly-Si devices with their single-crystal counterparts, the main difference in their characteristics arises because of the

presence of grain boundaries in the poly-Si, which will affects the device performances including the on-state current, threshold voltage, and field-effect mobility. In addition, these defects also generate junction leakage current at the source and drain which increases the off-state leakage current.[3][4] The off-state leakage current has been found to increase exponentially with increasing different between gate and drain voltage, and has been attributed to the field emission of carriers via the traps by high electric-field near the drain junction.[5][6][7]

Recently, dozens of researches have been made to develop various technologies for improving the performance and reliability of LTPS TFTs. Poly-Si films crystallized from a-Si usually results in a larger grain size has been considered the most important process for fabrication high-performance LTPS TFTs. Many techniques about crystallization of amorphous silicon, such as solid phase crystallization (SPC)[10][11], excimer-laser annealing (ELA)[12][13], rapid thermal annealing (RTA)[14][15], metal induced lateral crystallization (MILC)[16][17], have been proposed. However, other low-temperature process technologies in the procedure of fabricating LTPS TFTs, such as gate dielectric formation, thin film deposition, ion doping/dopant activation, defect passivation, lithography, and etching are also indispensable for producing high-performance LTPS TFTs. [18]

1.2. Motivation

In poly-Si film, carrier mobility large than 10 cm^2/Vs can be easily achieved, that is enough to used as peripheral driving circuit including n- and p-channel devices.[17][18] For the drive circuits, the carrier field effect mobility is a key issue, but for the pixel TFT the leakage current is the major concern. Before poly-Si can be used for the switching transistor, a leakage current must be reduced below 1pA. [19]

The electrical characteristics of conventional self-aligned polysilicon TFTs are

known to present several undesired effects, including large off-current [20], kink effect [21] and electrical instabilities induced by hot-carrier effects (HCEs) [22][23]. The dominant mechanism of the high off-state leakage current is known to be the field emission via grain boundary traps due to a high electric field in the drain depletion region [24][25].

In order to reduce the abovementioned effects, a poly-Si TFT with an offset gate, a lightly doped drain (LDD), and a field-induced drain structure have been widely used to reduce the drain electric field. [26][27][28][29] Since the offset region between gate and source/drain suppresses the drain electric field, the offset gated poly-Si TFT has a low off-state leakage current. However, these structures inevitably decrease the on-state current due to the extra series resistance of the offset region is a serious problem. To alleviate this problem, an additional step of spacer formation followed by implantation is employed. Although a poly-Si TFT with LDD has better turn-on characteristics than an offset-gated TFT, device degradation due to implant damage and difficulty in doping control at the grain boundaries are important issues.[30] A poly-Si TFT with field-induced drain (FID) have high ON/OFF current ratio, because this structure can effectively reduce the drain electric field and is free from implant damage.[31] Compared with LDD structure, the FID structure is attractive obviously because it can overcome the shortcomings existed in LDD approach.

In the thesis, the novel poly-Si thin film transistor with stacked Si/Ge T-gate is proposed and experimentally demonstrated. The process dose not require any additional mask step or ion implantation process. It is found that this device structure provides low off-state leakage current compared with the conventional TFTs by reduced the electric field near the drain junction.

1.3. Thesis Outline

In this thesis, experimental process and electrical parameters extraction are shown in chapter 2. In chapter 3, the electrical characterization of the Si/Ge T-gate TFTs are compared

with the conventional TFT. In chapter 4, the conclusions of this thesis and the future work are given.

Chapter 2

Experimental Process and Electrical Parameters Extraction

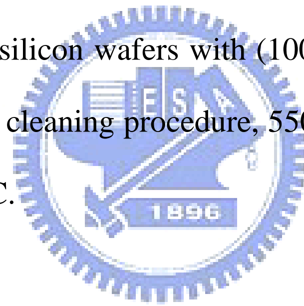
2.1 Fabrication of the thin-film transistors (TFTs)

The schematic cross sections of the Si/Ge T-Gate TFT is shown in Fig.2.1 and Fig.2.2. And the schematic cross section of conventional device is shown in Fig.2.3. The fabrication procedures of these devices are described as following (Fig.2.4):

2.1.1 Fabrication of the Si/Ge T-Gate TFTs

I. Substrate:

The 6-in single crystalline silicon wafers with (100) orientation were used as the starting materials. After an RCA initial cleaning procedure, 550 nm thick thermal oxide was grown in steam oxygen ambient at 980°C.



II. Poly-Si thin film active region formation:

Undoped amorphous silicon layers of thickness about 50/100nm were deposited by low pressure chemical vapor deposition (LPCVD) on buried oxide by hydrolysis of silane (SiH_4) at 550°C. Then, the amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24 hrs in an N_2 ambient. These recrystallized poly silicon films were then patterned into active region islands by transformer couple plasma (TCP) etching using the mixture of Cl_2 and HBr.

III. Gate dielectric and gate electrode formation:

After defining the active region, the 50nm thick gate TEOS oxide was deposited by low pressure chemical vapor deposition (LPCVD). Then, the germanium layer and the a-Si layer

were deposited as a gate, as shown Table 2.1. Table 2.2 shows the conditions for control devices.

Then, the wafers were ion implanted by phosphorous. The energy and the dose of implantation were 60keV and 5E15cm^{-2}. After the ion implantation, the germanium film and the a-Si layer were patterned and etched by transformer couple plasma (TCP-9400) to be the gate electrode.

IV. Si/Ge T-gate structure formation:

The T-gate was etched by selective wet etch method to form a T-shape structure. Then, Source and drain region were implanted by phosphorus (P) at 15keV /25keV to a dose of 5E15 cm^{-2}.

V. Passivation layer and contact metal:

Following, 300nm thick TEOS oxide by LPCVD was deposited and the contact hole was defined. TEOS oxide was etched by buffer oxide etchant (BOE) dip. Then, 500nm Aluminum sputtering and defines the metal pad. After etching Aluminum, the device was finished.

The nitride was also used to be a passivation material compare with the TEOS passivation device. In the chapter3, the electrical characteristics of the Si/Ge T-gate TFTs with Si_3N_4 passivation would compare with the TEOS passivation device.

2.1.2 Fabrication of the conventional TFTs

I. Substrate:

The 6-in single crystalline silicon wafers with (100) orientation were used as the starting materials. After an RCA initial cleaning procedure, 550 nm thick thermal oxide was grown in steam oxygen ambient at 980°C.

II. Poly-Si thin film active region formation:

Undoped amorphous silicon layers of thickness about 50/100nm were deposited by low pressure chemical vapor deposition (LPCVD) on buried oxide by hydrolysis of silane (SiH_4) at 550°C. Then, the amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24hrs in an N_2 ambient. These recrystallized poly silicon films were then patterned into active region islands by transformer couple plasma (TCP) etching using the mixture of Cl_2 and HBr.

III. Gate dielectric and gate electrode formation:

After defining the active region, the 50nm thick gate TEOS oxide was deposited by low pressure chemical vapor deposition (LPCVD). Then, the 200nm a-Si film was deposited immediately on the gate dielectric by LPCVD at 550°C. (Table2)

Then, the wafers were ion implanted by phosphorous. The energy and the dose of implantation were 60 keV and 5E15 cm^{-2}. After the ion implantation, the a-Si layer were patterned and etched by transformer couple plasma (TCP-9400) to be the gate electrode.

IV. Source/Drain region formation:

Source and drain region were implanted by phosphorus (P) at 15 keV /25 keV to a dose of 5E15 cm^{-2}.

V. Passivation layer and contact metal:

Following, 300nm thick TEOS oxide by LPCVD was deposited and the contact hole was defined. TEOS oxide was etched by buffer oxide etchant (BOE) dip. Then, a 500 nm Aluminum was sputtered and patterned as for the metal pad. After etching Aluminum, the device was finished.

2.2 Method of device parameter extraction

In this thesis, all the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer. Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs. In this section, extractions of various electrical parameters are introduced. These parameters induced the threshold voltage (V_{TH}) and subthreshold swing (*S.S.*), maximum On-current (I_{on}), minimum Off-current (I_{off}), and the *On*/*Off* current ratio.

2.2.1 Threshold voltage (V_{TH})

In this thesis, the threshold voltage (V_{TH}) is defined at a fixed drain current $I_D = I_{DN} \times (W/L)$ where I_{DN} is a normalized drain current. Here, I_{DN} is 100 nA and the same for all devices. This definition corresponds to approximately the same surface band bending for all devices and avoids the ambiguity associated with an extrapolated threshold which arises in devices where the effective channel mobility depends strongly on the gate bias.

2.2.2 Subthreshold swing (S.S.)

The drain current in the saturation region ($V_D > V_{GS}-V_{TH}$) is expressed as the following equation:

$$I_{DS} = \frac{1}{2}\mu_{FE} C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \qquad \text{(Eq.1)}$$

Where *W* is gate width and *L* is gate length. C_{ox} is the gate oxide capacitance. μ_{EF} is the field effect mobility.

It appears that the current abruptly vanishes while V_G is reduced to zero from the equation. In reality, there is still some drain conduction below threshold, and this is known as subthreshold conduction. This current is due to the weak inversion in the channel between flat-band and threshold, which leads to a diffusion current from source to drain.

The subthreshold swing (*S.S.*) is defined as the reciprocal of slope of the I_D-V_G curve in weak inversion region. It means that a change in the input V_G, *S.S.* (V) will change the output current I_D by an order of magnitude. It is a typical parameter to describe the control ability of gate toward channel.

2.2.3 On/Off current ratio

A poly-Si TFT with good characteristics should not only provides high *On* state driving current but also low *Off* state leakage current. For pixel transistors, the *Off* state is frequently encountered in normal operation. Therefore, *On*/*Off* current ratio is obviously a more appropriate evaluation parameter compared with On state current alone. In addition, the mechanism of leakage current in poly-Si TFT's quite differs from that in MOSFET's. In MOSFET's, it is the single crystalline that consists of the channel film and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFT's, the channel film is composed of polycrystalline. Lots of traps located in grain boundaries play a dominant role in this situation.

Consider large negative gate bias V_G is applied, a hole channel forms under the gate. In principle, little current flows because the junction between the hole channel and the drain is revered-biased. However, due to the large electric field and the existing numerous trap states in the polysilicon film, electron and hole emission from trap states becomes a strongly increasing function of electric field. Here, a trap could be modeled by a potential well. For large electric fields, it is possible for electrons to escape the potential well by quantum mechanical tunneling. The tunneling rate increases strongly with electric field because the barrier thickness decreases. The effect is a rapid increase in leakage current. The tunneling rate depends upon the total electric field, and consequently the leakage current is increased when both drain and gate voltages are high.

In this thesis, the *On* current is defined as the current when gate voltage equals to 20V

and drain voltage is 10V. The *Off* current is specified as the minimum current when drain voltage equals to 10V.

2.3 Material analysis

In order to demonstrate that the T- gate structure has been fabricated, and the length of the T-gate undercut region, we use the transmission electron microscope (TEM) and scanning electron microscopy (SEM) to confirm.

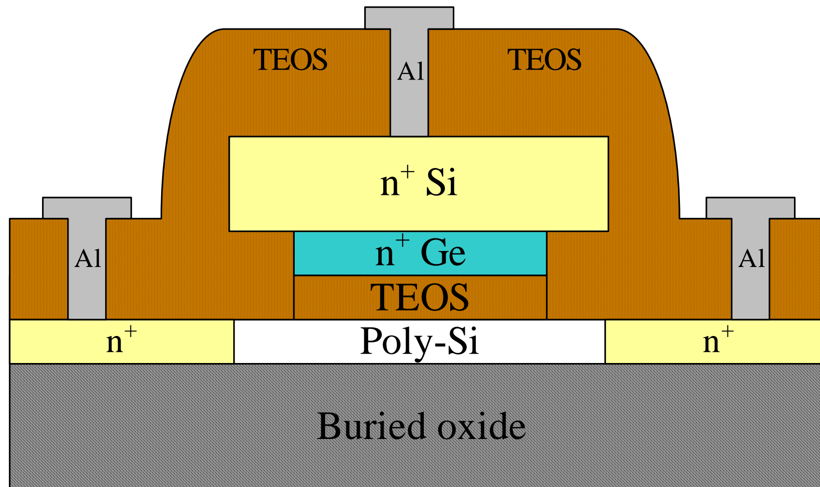


Fig.2.1 The schematic cross section of the Si/Ge T-Gate TFTs with TEOS passivation

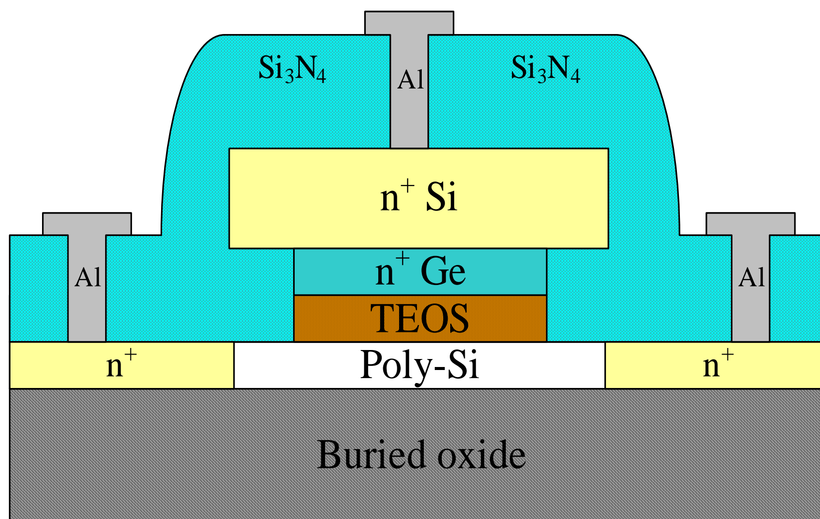


Fig.2.2 The schematic cross section of the Si/Ge T-Gate TFTs with Si_3N_4 passivation

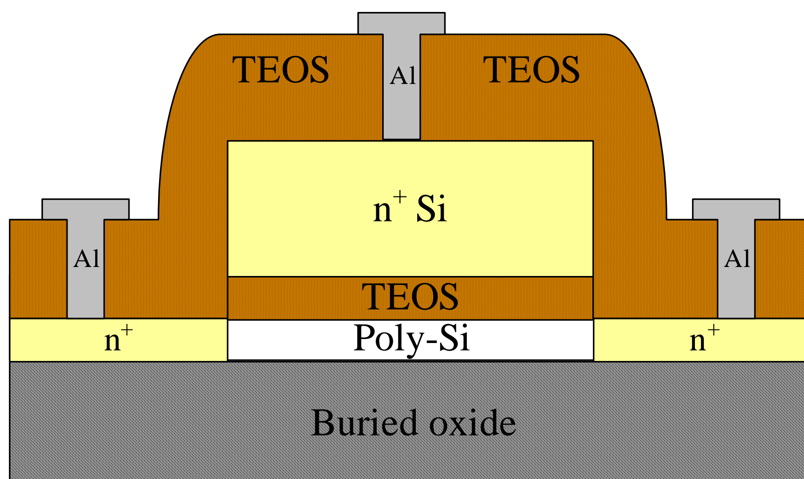
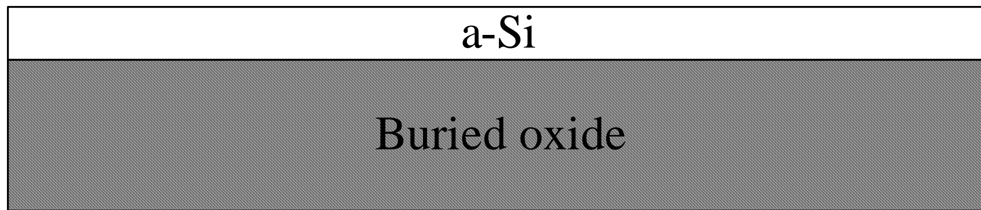
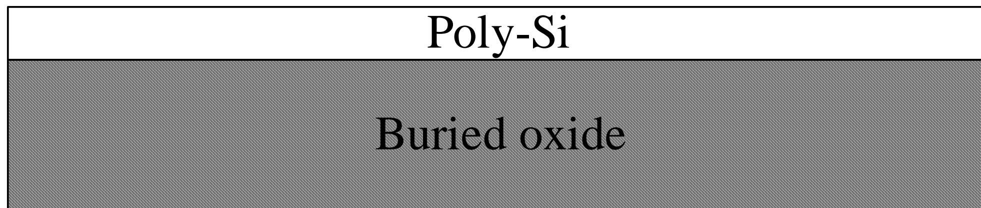


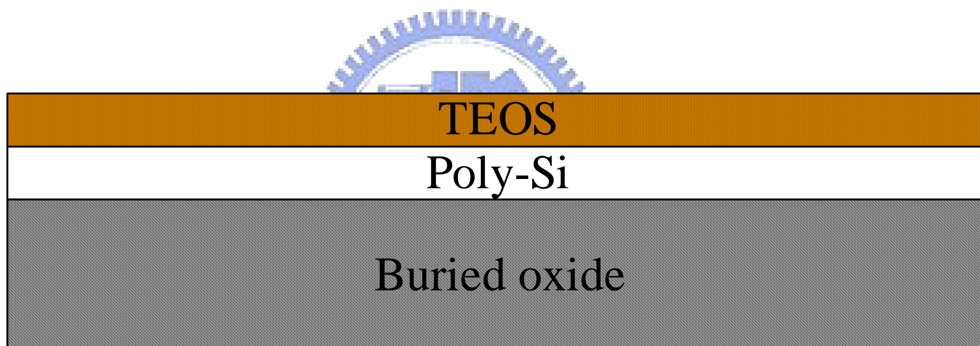
Fig.2.3 The schematic cross section of conventional TFTs



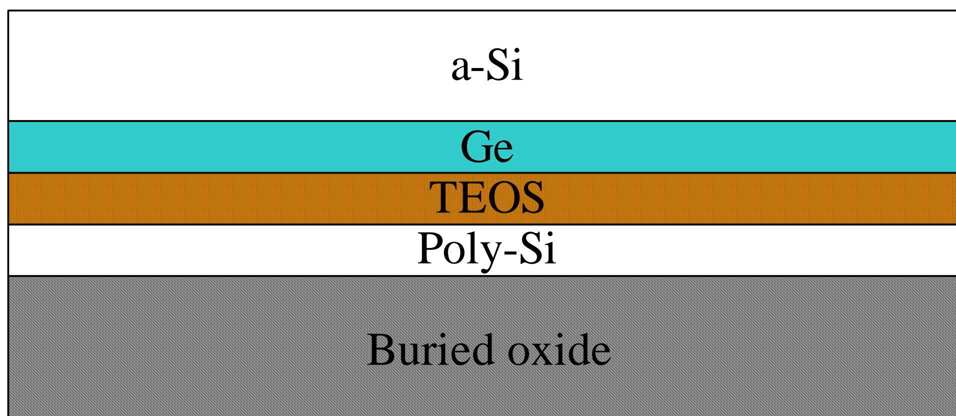
(1) 550 nm thick buried oxide and 50/100nm thick a-Si were deposited.



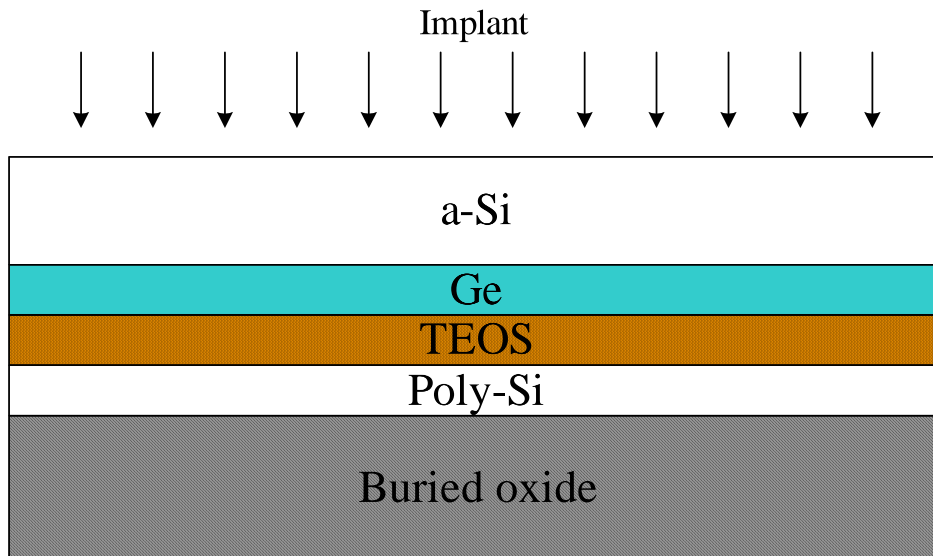
(2) 600°C annealing for 24-hr and active region definition.



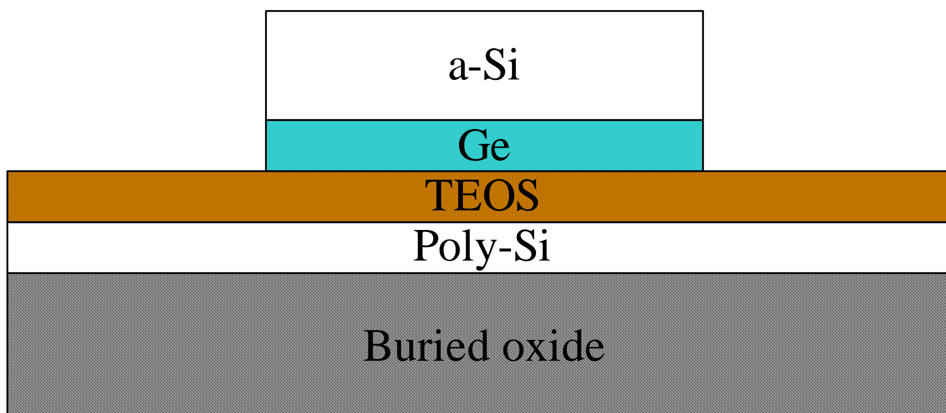
(3) 50 nm thick TEOS oxide was deposited.



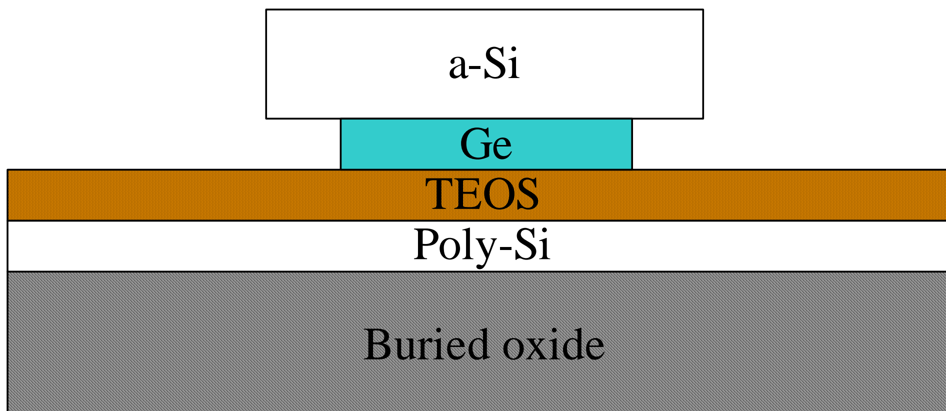
(4) 50/100nm thick germanium layer and 150/100nm thick a-Si were deposited.



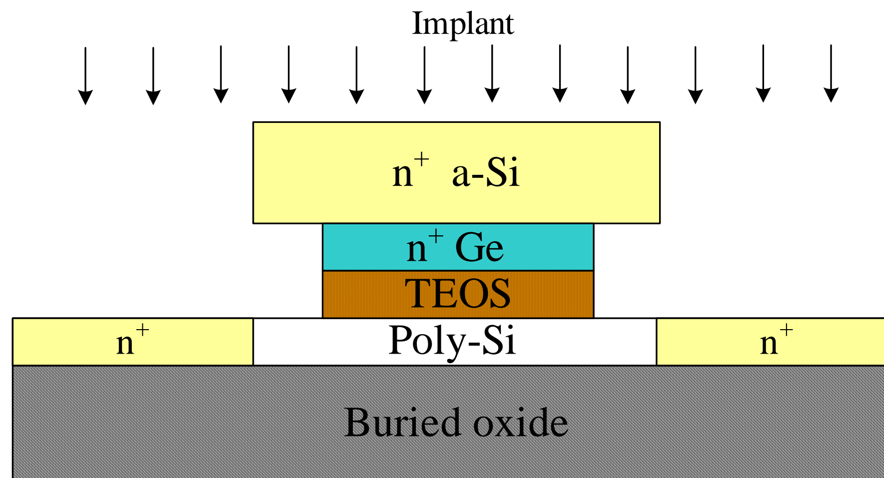
(5) Phosphorous implantation.



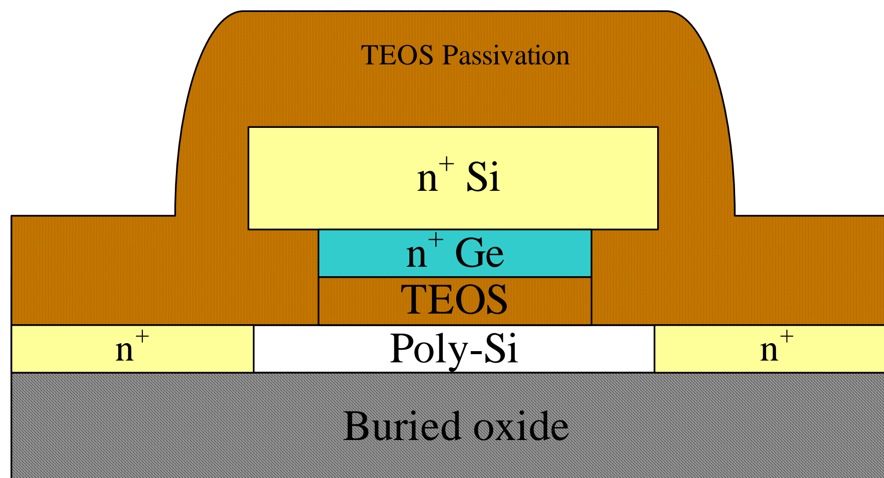
(6) Gate definition.



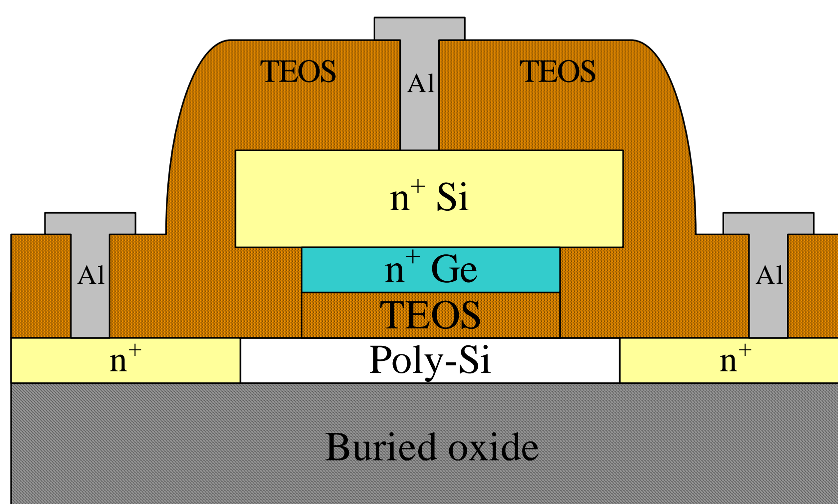
(7) Si/Ge T-Gate structure formation.



(8) Source/Drain region formation.



(9) TEOS passivation layer.



(10) Contact hole and metal pad.

Fig. 2.1 Process flows of Si/Ge T-Gate TFTs.

Table 3.1 Split condition for all samples with different thickness of stacked Si/Ge and undercut length.

Device	Channel thickness	Gate oxide	Gate (Si/ Ge)	Undercut
Si/Ge_{50nm} T-gate TFT(400nm)	50nm	All 50nm	150nm / 50nm	400nm
Si/Ge_{50nm} T-gate TFT(800nm)				800nm
Si/Ge_{50nm} T-gate TFT(400nm)			100nm / 100nm	400nm
Si/Ge_{50nm} T-gate TFT(800nm)				800nm
Si/Ge_{100nm} T-gate TFT(400nm)	100nm		150nm / 50nm	400nm
Si/Ge_{100nm} T-gate TFT(800nm)				800nm
Si/Ge_{100nm} T-gate TFT(400nm)			100nm / 100nm	400nm
Si/Ge_{100nm} T-gate TFT(800nm)				800nm

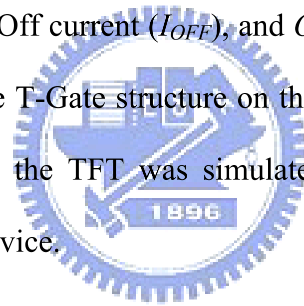
Table 3.2 Split conditions for control devices.

Device	Channel thickness	Gate oxide	Gate (a-Si film)	Undercut
Conventional TFT	50nm	50nm	200nm	
Conventional TFT	100nm		200nm	

Chapter 3

Electrical Characterization of the Si/Ge T-gate TFTs

At first, the cross-section TEM of T-gate TFTs is shown in Fig.3.1. Thickness of channel film, gate oxide, gate, and undercut length are shown in Fig.3.2. Fig. 3.3 shows the SEM image of the Stacked Si/Ge gate with undercut structure. The T-Gate structure was successfully fabricated, which had shown in the TEM and SEM pictures clearly. In this chapter, the electrical characteristics of the Si/Ge T-gate TFTs and conventional TFTs are discussed carefully. The device parameters including threshold voltage (V_{TH}), subthreshold swing (*S.S.*), On current (I_{ON}), Off current (I_{OFF}), and *On/Off* current ratio are all extracted. In order to verify the effect of the T-Gate structure on the vertical and lateral electric field near the drain, the electric field in the TFT was simulated by employing the commercial 2-D simulator for semiconductor device.


1896

3.1 Device Simulation

As we know that the undesirable effect, anomalous leakage current, kink effect, and hot-carrier effect, are related to the lateral electric field in the channel. In order to study the electric field effects of the various LTPS TFT structures, the two-dimensional (2D) numerical device simulator TCAD- ISE (Integrated Systems Engineering) was utilized.

The 2D cross-section of TFTs structure obtained from DIOS-ISE process simulation. The device simulation grids for the structures are generated using MDRAW-ISE. For electrical analysis is then carrier out in DESSIS-ISE on the structures. We consider the drift-diffusion model in our calculation.

Fig.3.4 and Fig.3.5 show the electric field distribution along the channel/gate insulator

interface for V_G= -10V and V_D= 10V. At the active layer surface under the T-Gate structure, the vertical electric field and lateral electric field are reduced considerably compared with conventional TFT. Especially, the Si/Ge T-Gate TFTs with high thickness of the germanium layer have shown a lower electric field than that of the Si/Ge T-Gate TFTs with 400nm germanium layer thickness.

Fig.3.6 and Fig.3.7 show the electric field distribution along the channel/gate insulator interface for V_G= 0V and V_D= 15V. It is also found that the Si/Ge T-Gate TFTs with TEOS passivation reduce both horizontal and vertical electric fields.

Fig. 3.8 and Fig.3.9 show the simulated electric field distribution for Si/Ge T-Gate TFTs with Si_3N_4 passivation. Results show that higher electric field at the drain edge of the high-k passivation TFT compared to the TEOS passivation TFT. The vertical and lateral electric field distribution along the channel/gate insulator interface for V_G= 0V and V_D= 15V are shown in Fig.3.10 and Fig.3.11.

It is well known that the leakage current increases significantly with the increase of gate voltage and drain voltage due to the field enhanced generation [32][33]. The lateral peak electric field in the depletion region between the p^+ accumulation layer and the n^+ drain causes the field emission via trap states, which makes the leakage current increase with drain voltage. Increase of gate voltage increases the vertical electric field around the interface between the gate oxide and the active poly-Si near the drain, which causes the serious increase of leakage current due to the enhanced thermal generation [34].

3.2 Basic Electrical Characteristics of Si/Ge T-Gate TFTs

3.2.1 Transfer Characteristics

The I_D-V_G characteristics of an n-channel Si/Ge T-Gate TFTs with different gate length (10 μm、8 μm、5 μm、3 μm) are shown in Fig.3.12~Fig.3.15. The leakage current of the Si/Ge T-Gate TFTs is lower by two orders of magnitude than that of conventional devices at

V_G= -10V. It is because that T-Gate TFTs could effectively reduce the electric field near the drain junction. For an LPCVD polysilicon TFT, according to the trap-assisted field-emission model, the leakage current can be expressed as [32]

$$I_L \approx qZx_eN_T\left(\frac{1}{\tau_{TC}+\tau_{TV}}\right)\left(\frac{|V_D|}{E_y}\right) \qquad \text{(Eq.2)}$$

where x_e is the effective depth of the junction region, Z is the channel width, and N_T is the trap density. The time constants τ_{TC} and τ_{TV} represent the probability per unit time that a trapped carrier will tunnel through a triangular barrier at the channel/drain junction, which is exponentially dependent on the inverse of the strength of the lateral electric field E_y. Therefore, the leakage current can be reduced by decreasing the electric field at the channel/drain junction region.

The off-state current of the Si/Ge T-Gate TFTs are much lower than that of the conventional TFT. When the germanium layer thickness is increased, the off-state leakage current is reduced at V_D = 10V, compared to the conventional TFT, which is due to the vertical electric field and lateral electric field near the drain edge are both reduced. As channel length is reduced, the leakage current is lower with increase of the T-Gate height is obviously.

Fig.3.16~Fig.3.19 show the transfer characteristics of the Si/Ge T-Gate TFTs with high channel thickness (100nm), the leakage current are also reduced significantly with increase of germanium layer thickness and undercut length.

The off-state leakage current was effectively suppressed in the Si/Ge T-Gate TFTs with channel thickness 50nm, especially when the increase of germanium layer thickness and undercut length. However, the on-current for these conditions is decreased due to the increased series resistance caused by the undercut regions. Hence, the Si_3N_4 with higher dielectric constant was used to improve the on-state characteristic.

The I_D-V_G characteristics of the Si/Ge T-Gate TFTs with a Si_3N_4 passivation for different gate length (10 μm、8 μm、5 μm、3 μm) are shown in Fig. 3.20~Fig. 3.23. These

TFTs have better subthreshold swing and high I_{on} than those TFTs with a TEOS passivation. High dielectric constant materials have been used to increase capacitance C_{ox} which could improve the on-state current. The combination of T-Gate structure and Si_3N_4 material can suppress the electric field and improve the on-state characteristics.

3.2.2 On/Off Current Ratio

Fig.3.24 show the gate length dependence of On/Off current ratio in Si/Ge T-gate TFTs with TEOS passivation and conventional TFT. The devices with 50/ 100nm thickness of channel film are shown in the figure (a) and (b). The higher series resistance of the undercut regions slightly degrades the on-current of the Si/Ge T-Gate TFTs with thick germanium film. For this reason, the On/Off current ratio is lower than the thin germanium film devices, as shown in figure (a).

For the channel thickness is increased, shown in Fig.3.24 (b), the influence of series resistance is slightly released when increasing the thickness of germanium layer. In addition, the off-state leakage current of the Si/Ge T-Gate TFTs with thick germanium film is lower than other devices. The Si/Ge T-Gate TFTs with 100nm thickness of germanium layer have increased the On/Off current ratio relative to the Si/Ge T-Gate TFTs with 50nm thickness of germanium film.

The Si/Ge T-Gate TFTs with a Si_3N_4 passivation was shown in Figure 3.25. The On/Off current ratio trend is similar in the T-Gate devices because of the on-state current is considerably increased and off-state leakage current is almost the same.

All conventional TFTs show a smaller On/ Off current ratio among these devices, which is due to the leakage current can not be effectively suppressed with large electric field near the drain edge.

3.2.3 Off-State Leakage

The temperature dependence of the mobile holes in equilibrium with the trapped charge is given by [35]

$$I_{off} = I_0 e^{-\frac{E_a}{kT}} \qquad \text{(Eq.3)}$$

I_0 = constant independent of temperature, and E_a = drain current activation energy which measures the difference between the valence band edge and the energy of the grain boundary states within kT of the Fermi level. In TFTs, the increase in the electric field strength causes the decrease of the leakage current activation energy [36]. As the drain bias increases, the drain depletion field increases and E_a decreases. This suggest that the high electric field in the drain depletion region has reduced the barrier that carrier must overcome. This leakage current mechanism is thermionic field emission [35].

The Off-state leakage current characteristics are shown in Fig.3.26 and Fig.3.27. The Si/Ge T-Gate TFTs show the leakage current as low as 1pA/μm. It is because the T-Gate structure can effectively suppress the electric field near the drain edge. In the conventional TFT, I_{off} abruptly increases with increasing V_d because of the thermionic field emission current at drain junction [37].

3.2.4 Output Characteristics

The current increase in the output characteristics at large V_{DS}, usually referred to as “kink effect,” is explained by impact ionization occurring in the high-field region at the drain end of the channel. Its effect is enhanced by the action of a parasitic bipolar transistor in the back-channel region, whose base current arises from the impact generated holes [38].

Figure 3.28~ Figure 3.30 show the output characteristics of conventional TFTs and Si/Ge T-gate TFTs with W/L=10μm/10μm. The I_D-V_D performances of the Si/Ge T-gate TFTs were much better than the conventional TFT. For the conventional TFTs, the severe kink

effect at high drain biases is a result of the exaggerated avalanche multiplication near drain junction caused by the high drain field and large amount of traps [39].

Impact ionization has been modeled by the Chynoweth expressions of the ionization rates for electrons (α_n) and holes (α_p) [40]

$$\alpha_n = a_n \exp\left(\frac{-b_n}{F_\parallel}\right) \qquad \alpha_p = a_p \exp\left(\frac{-b_p}{F_\parallel}\right) \qquad \text{(Eq.4)}$$

where $F_\parallel$ is the component of the electric field along the current-flow direction. The ionization rate is reduced by suppressing lateral electric field. Therefore, at very high source-drain voltages, drain avalanche is unobvious for T-Gate structure.

Figure 3.28 shows the result for (a) germanium layer thickness is 50nm, and (b) germanium layer thickness is 100nm. The device with thickness of germanium layer 100nm exhibits a smaller on-current than that of 50nm germanium layer case. This is because the series resistance is increased under the undercut region. However, floating body effect is reduced in Si/Ge T-gate TFTs with thick thickness of germanium film which caused by suppressed lateral electric field.

The kink effect in SOI MOSFETs is a combination of the channel avalanche multiplication occurred in the high-field region near the drain and the floating body effect at the channel of the device [41]. However, in poly-Si TFTs, there is an additional mechanism that causes the poor saturation characteristics. It is the high grain-boundary trap density in the poly-Si material that exaggerates the effect of the avalanche multiplication [42] [43].

When channel film is increased, the grain-boundary trap density in the channel will cause the sever kink effect at high drain biases, as shown in Figure 3.29. But it is found that the Si/Ge T-gate TFTs exhibits with good current saturation characteristics compared with conventional TFT. In the conventional TFT, the higher lateral electric field will generate more hot carriers which cause seriously floating body effect to occur.

The output characteristics of Si/Ge T-Gate TFTs with a Si_3N_4 passivation were shown

in the Fig.3.30. The anomalous current was suppressed at $V_D < 15V$ and the on-current characteristic are better than those TFT with a TEOS passivation. But the drain avalanche occurs as the drain voltage is increased, which is due to the lateral electric field is larger than the Si/Ge T-Gate TFTs with a TEOS passivation. In order to obtain excellent saturation characteristics in the low temperature poly-Si (LTPS) TFT's, both the high electric field and high grain-boundary trap density at the channel near the drain must to be reduced effectively.

3.2.5 Hot Carrier Stress

Hot carrier stress was used to test the long-term reliability of LTPS TFT in this work. Hot carrier instabilities in poly-Si thin film transistors are caused by high electric fields at the drain. These high fields are determined mainly by the abruptness of the lateral n^+ doping profile in the drain and the two-dimensional (2D) coupling of the x and y components of the electric field between the gate and drain [44]. Fig.3.31 illustrating the time evolution $(0 < t < 10^3)$ of the relative on-current degradation that bias-stressing at V_{GS} = 10V, V_{DS} = 20V cause minor ΔI_{on} for the Si/Ge T-gate TFTs which compared with conventional TFTs. The trend of Si/Ge T-gate TFTs with different conditions were shown in these figures. The device with the 100nm-thick of germanium layer shows larger on-current degradation than that of 50nm case. This is because the increased series resistance under the undercut region causing a reduced $I \times R$ drop and on-state current. However, the Si/Ge T-gate TFTs still have lower I_{on} variation than the conventional TFTs, since the lateral electric field is reduced.

Figure 3.32 (a)~(b) show the ΔV_{TH} versus stress time for conventional TFTs and Si/Ge T-gate TFTs with different channel length (W/L=10 μm/10 μm, 5 μm). These figures illustrate the threshold voltage variations and the degradation in a poly-Si TFTs under static hot-carrier stress and the DC stress conditions are V_{DS} = 10V and V_{GS} = 20V for 1000s. The large drain junction electric field under hot carrier stress resulted in serious degradation on conventional TFTs, was due to the high electric field at the drain junction. The high electric

field promotes impact ionization, resulting in numerous grain-boundary traps being created in the drain junction. On the other hand, the Si/Ge T-gate TFTs exhibited better hot carrier endurance than conventional one resulted from the relief of drain junction electric field.

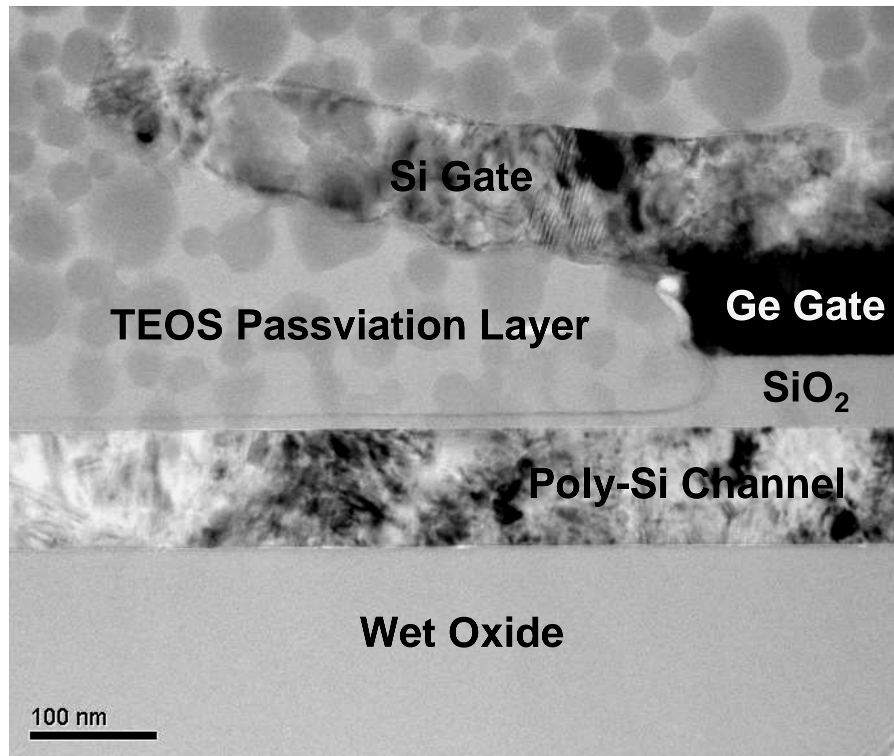


Fig. 3.1 Stacked Si/Ge gate with the germanium undercut structure observed by cross section TEM microphotographs.

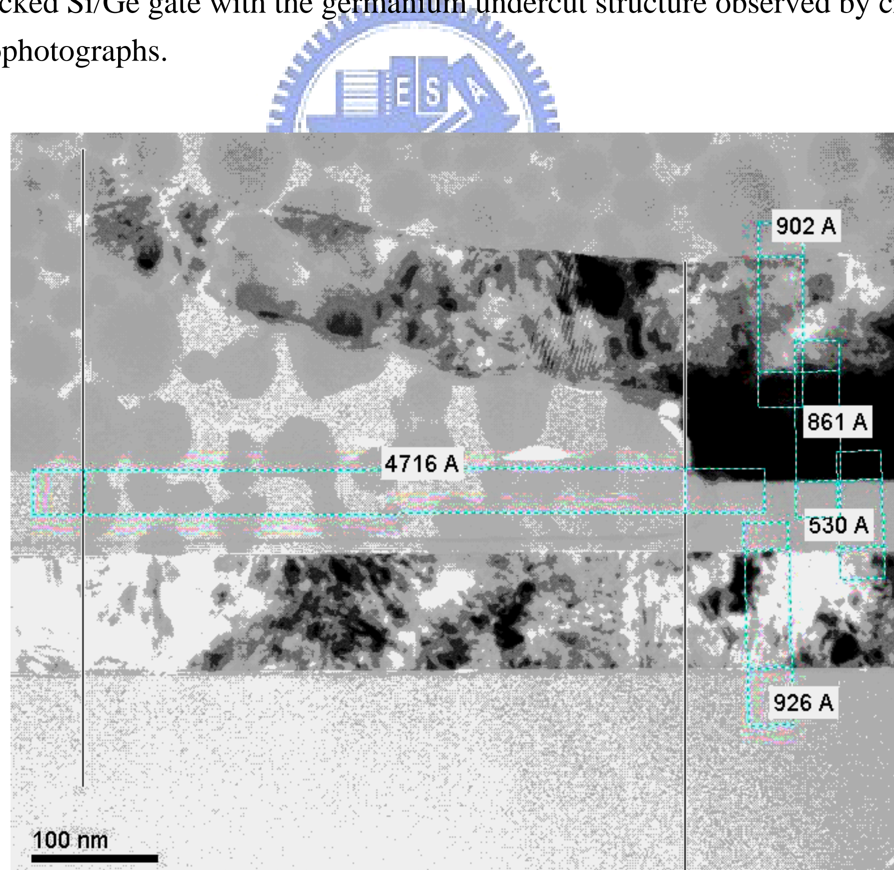


Fig. 3.2 Thickness of channel film, gate oxide, gate, and undercut length are shown in this picture.

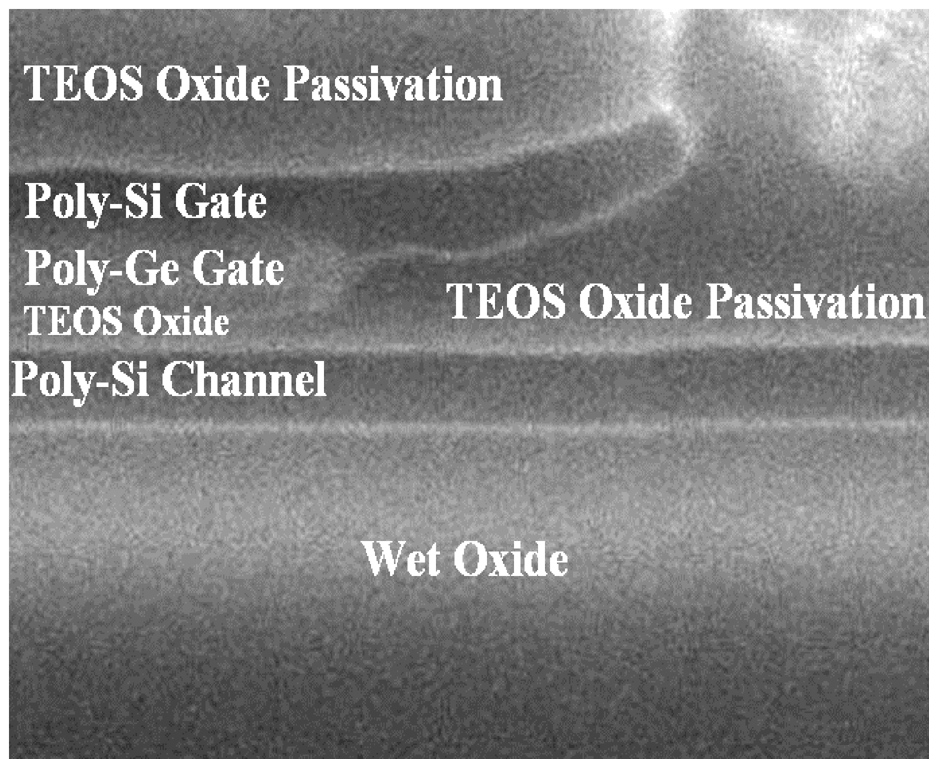
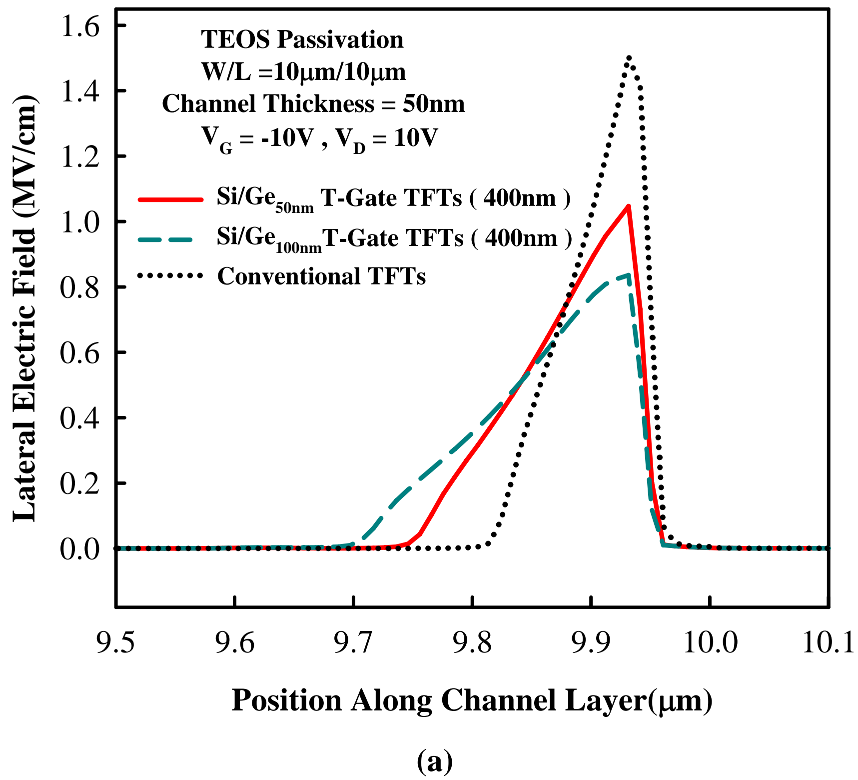
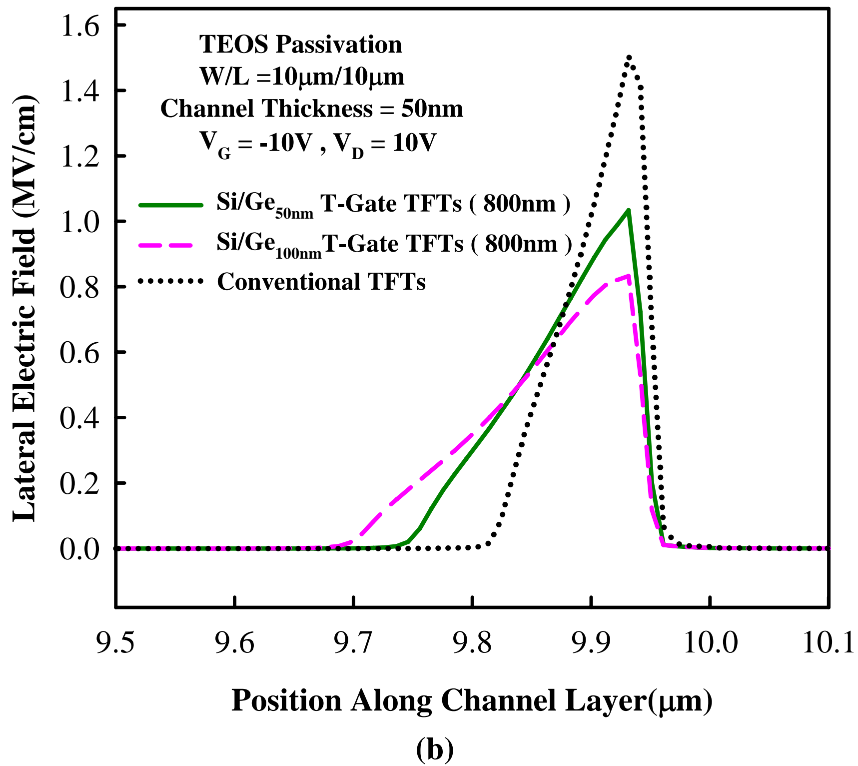


Fig. 3.3 SEM image of the Stacked Si/Ge gate with undercut structure.

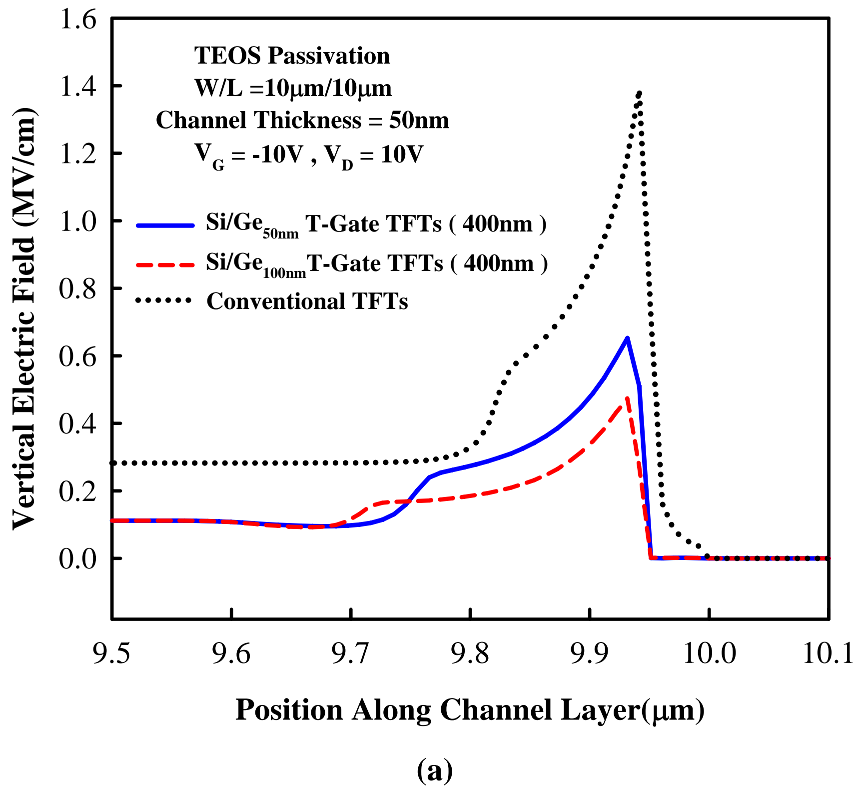


(a)

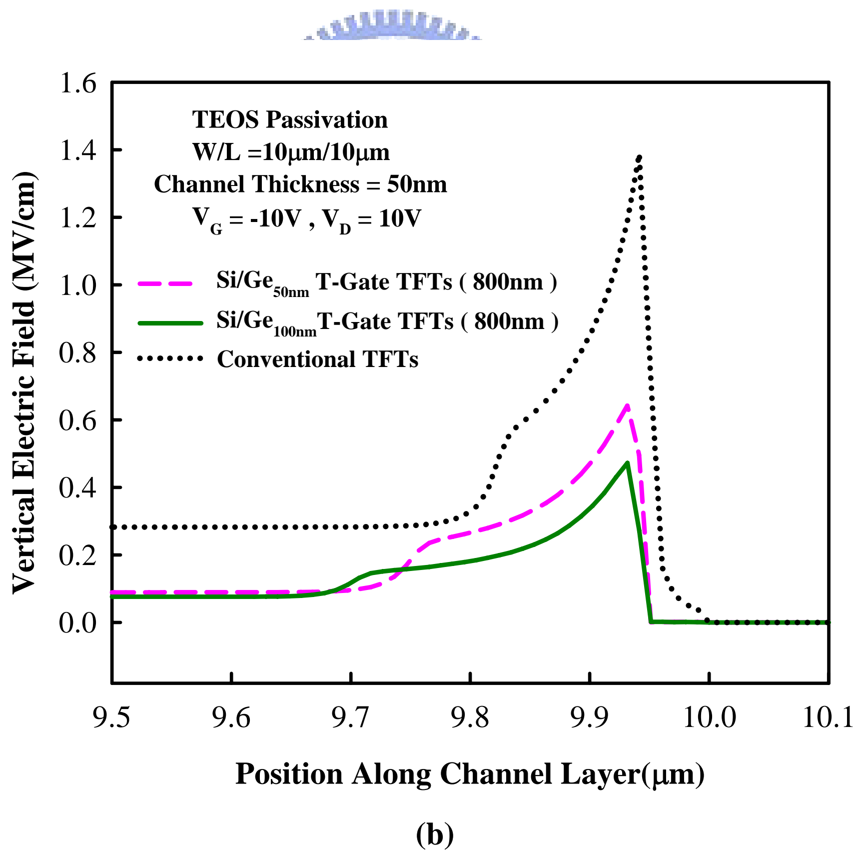


(b)

Fig. 3.4 The simulated lateral electric field along the channel (10 μ m) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) Undercut length is 400nm. (b) Undercut length is 800nm.

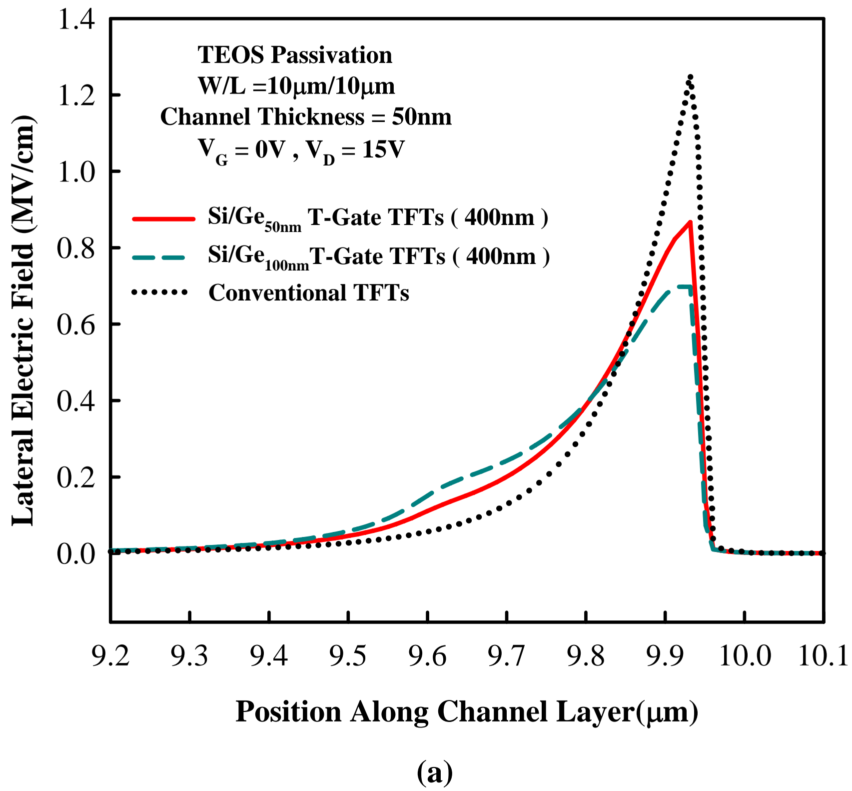


(a)

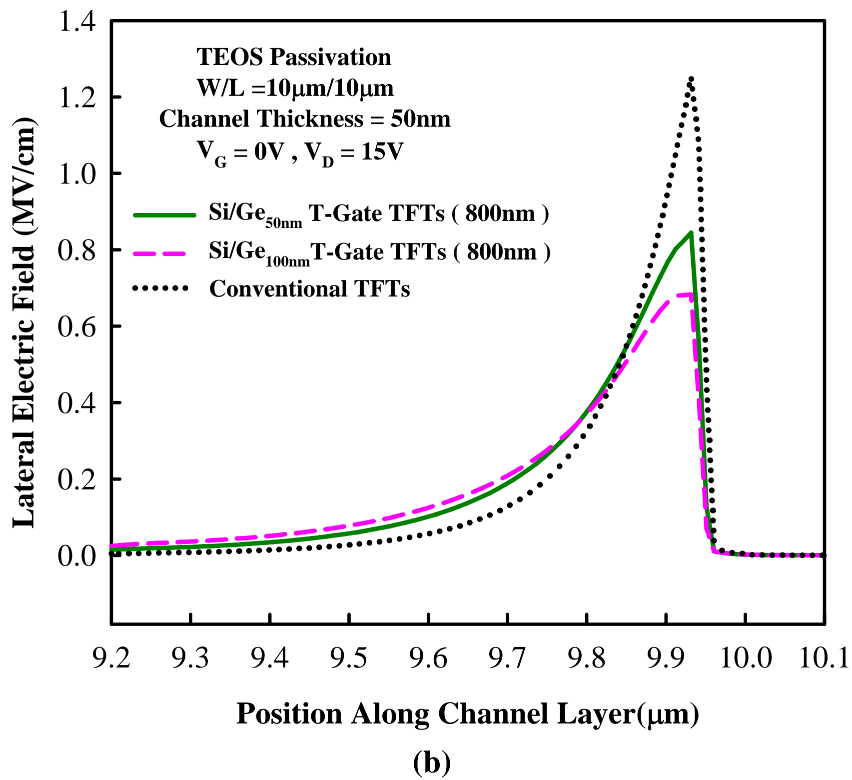


(b)

Fig. 3.5 The simulated vertical electric field along the channel (10 μ m) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) undercut length is 400nm. (b) undercut length is 800nm.

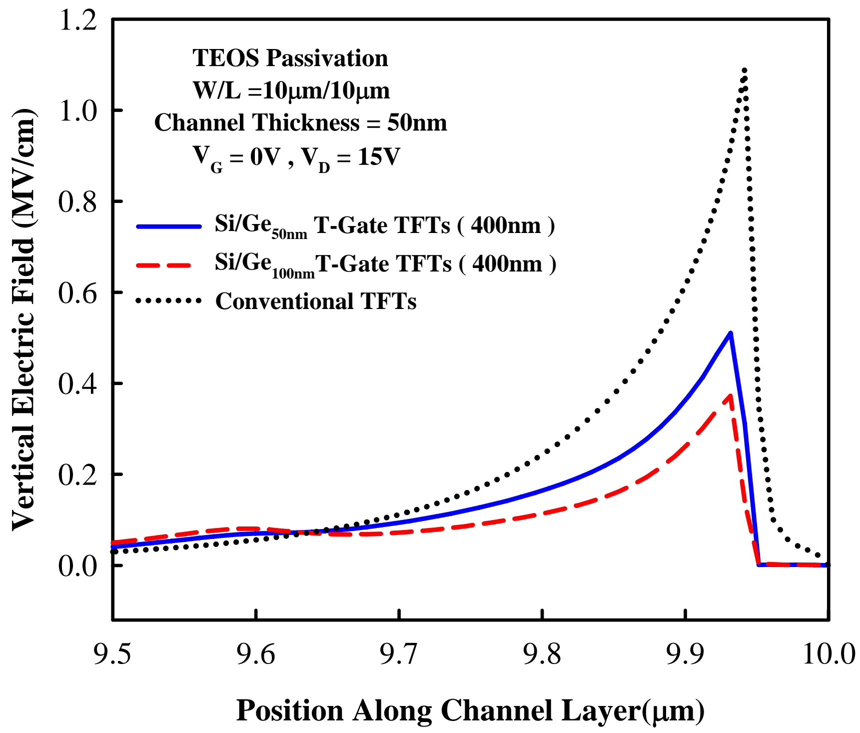


(a)

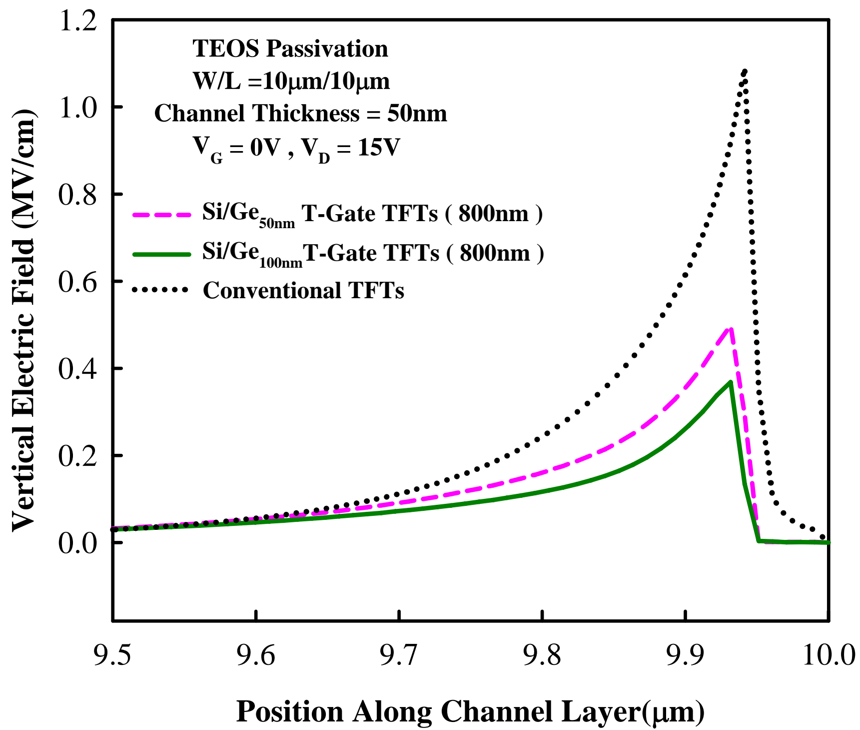


(b)

Fig. 3.6 The simulated lateral electric field along the channel (10 μ m) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) undercut length is 400nm. (b) undercut length is 800nm.



(a)



(b)

Fig. 3.7 The simulated vertical electric field along the channel (10 μ m) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with TEOS passivation of (a) undercut length is 400nm. (b) undercut length is 800nm.

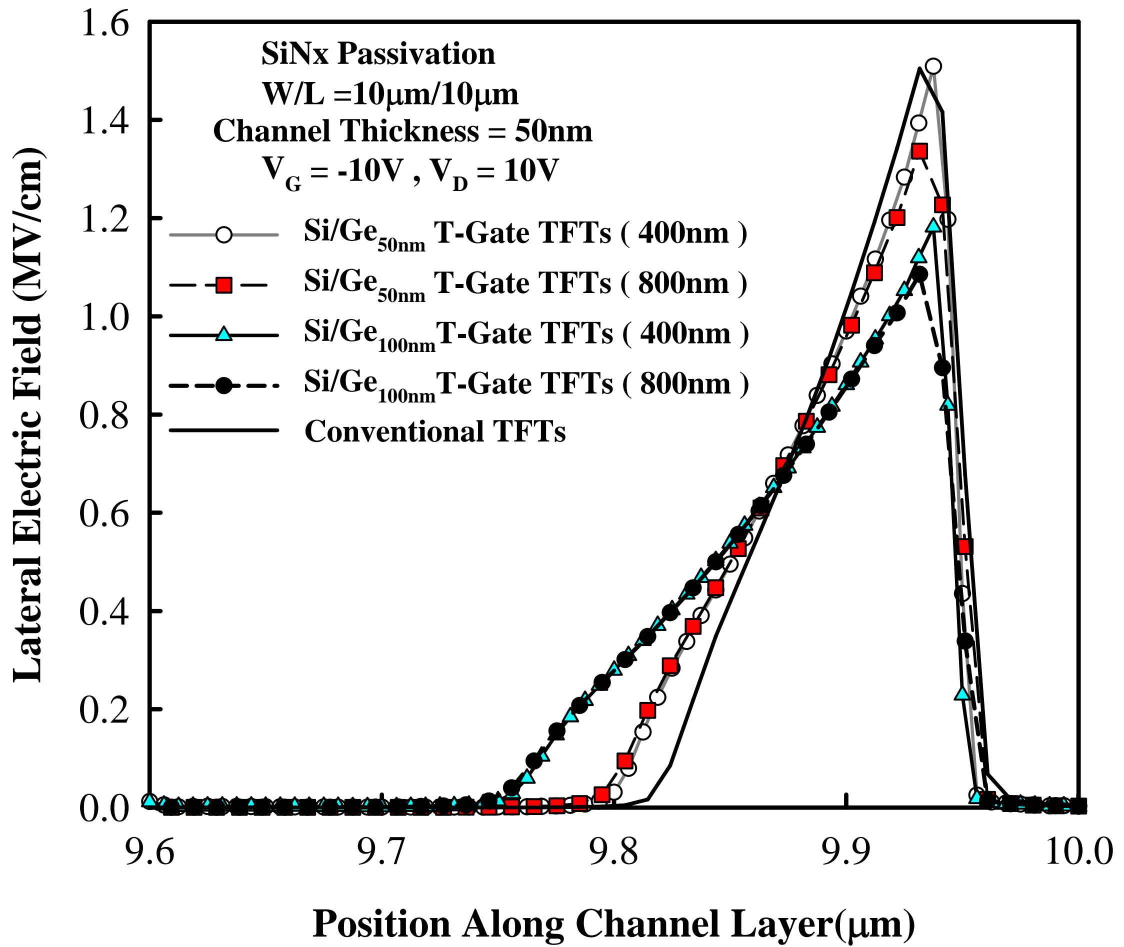


Fig. 3.8 The simulated lateral electric field along the channel (10 μ m) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

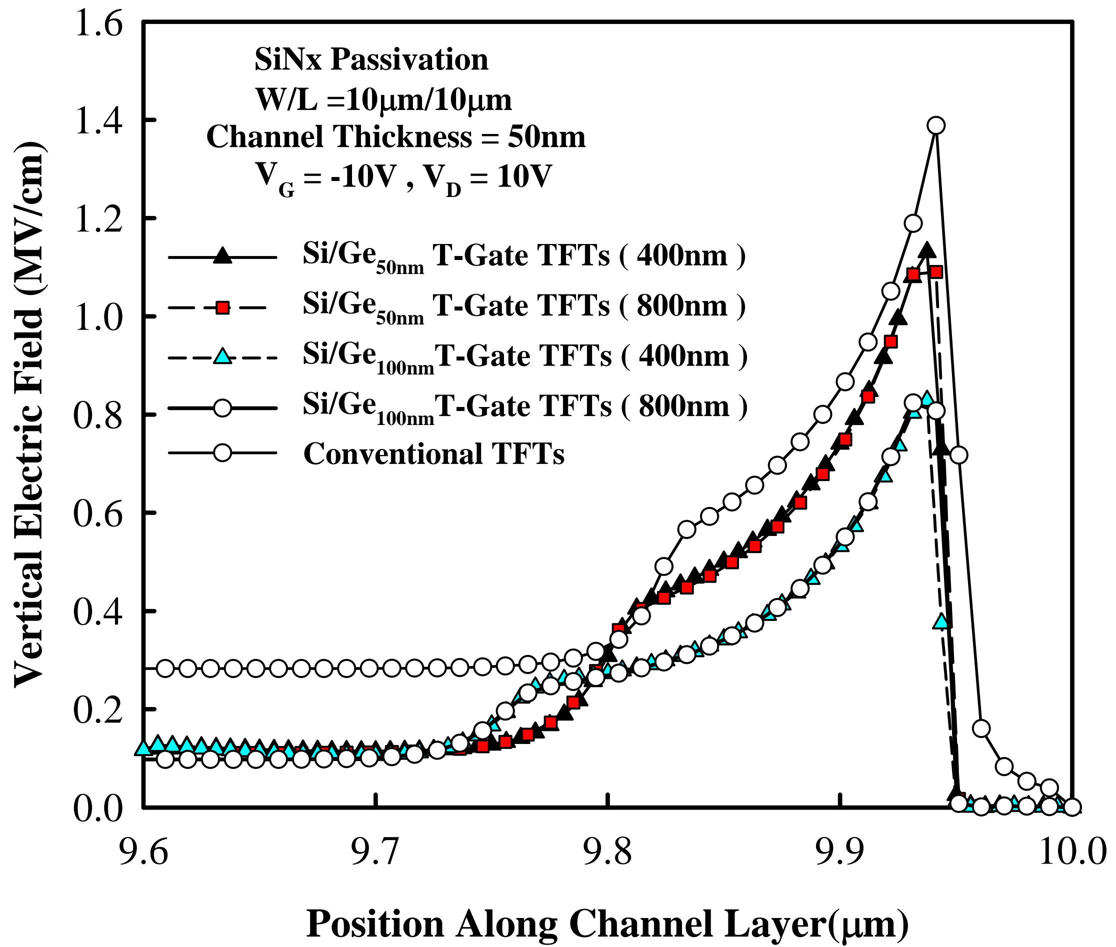


Fig. 3.9 The simulated vertical electric field along the channel (10 μ m) direction near the drain the V_G= -10V, V_D= 10V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

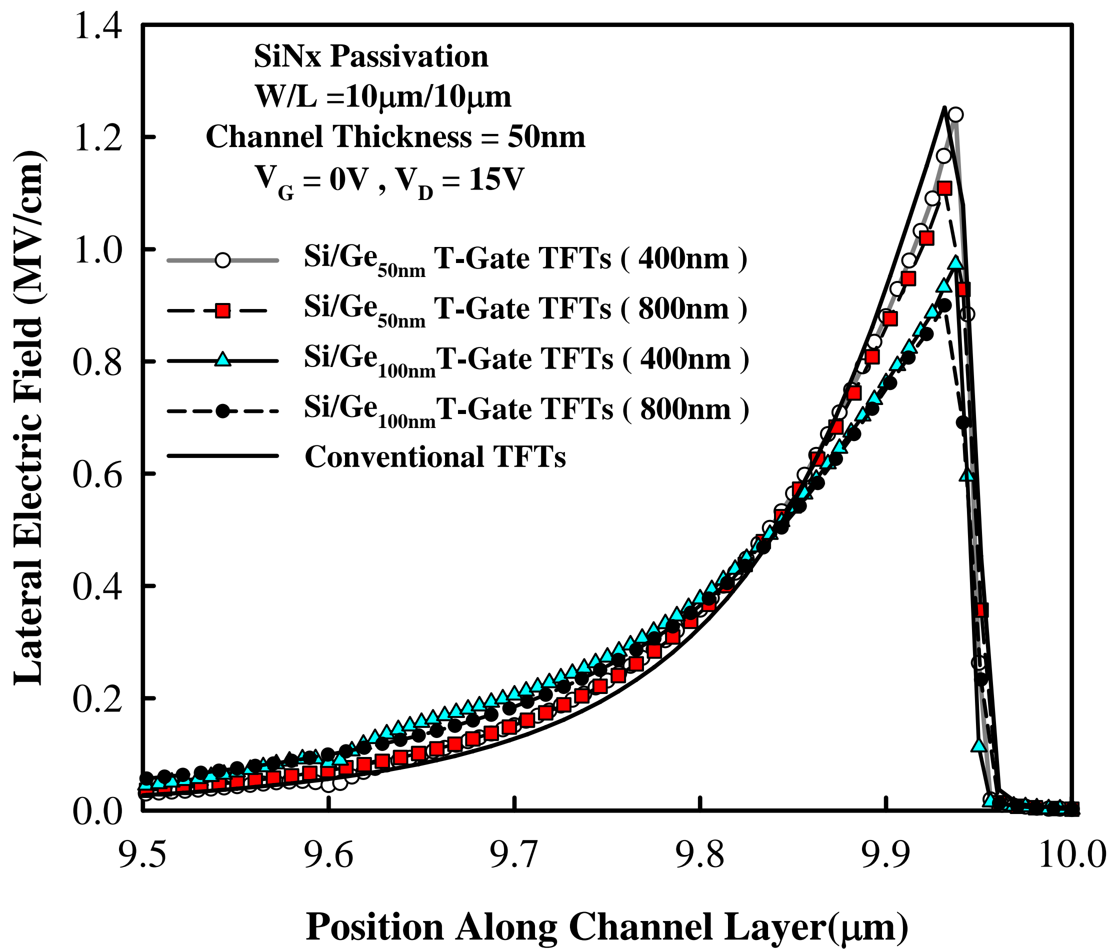


Fig. 3.10 The simulated lateral electric field along the channel (10 μm) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

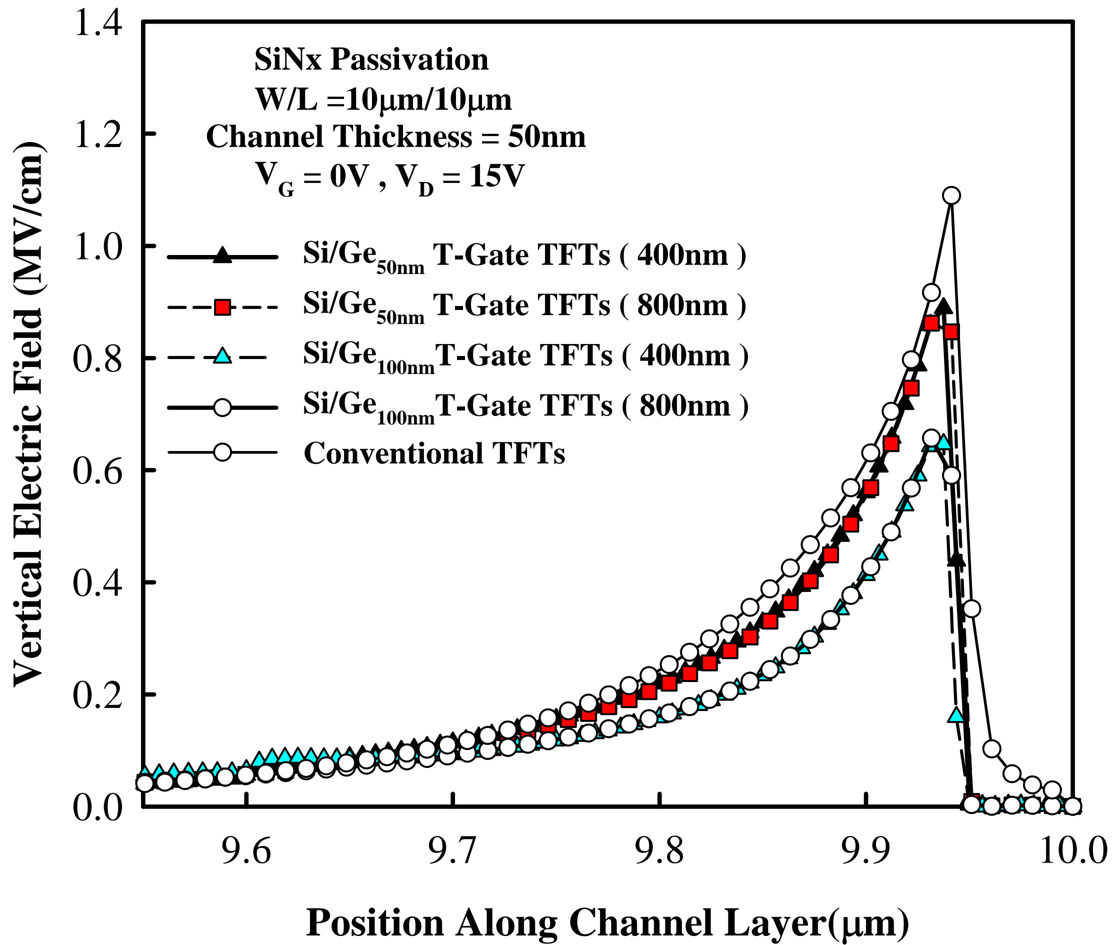
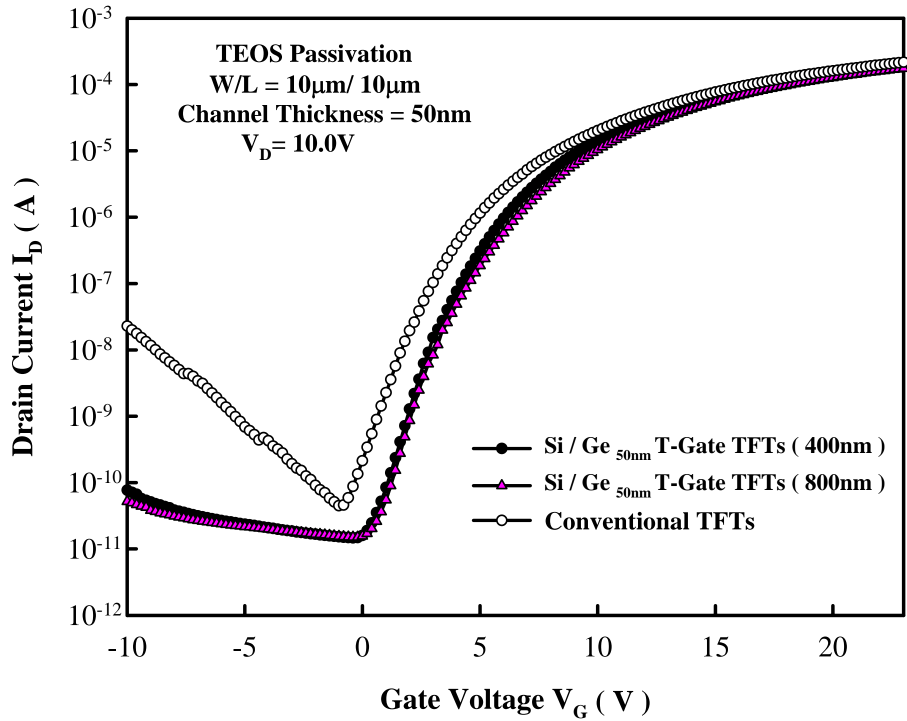
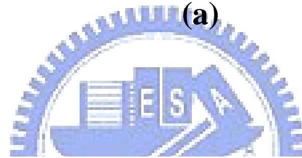
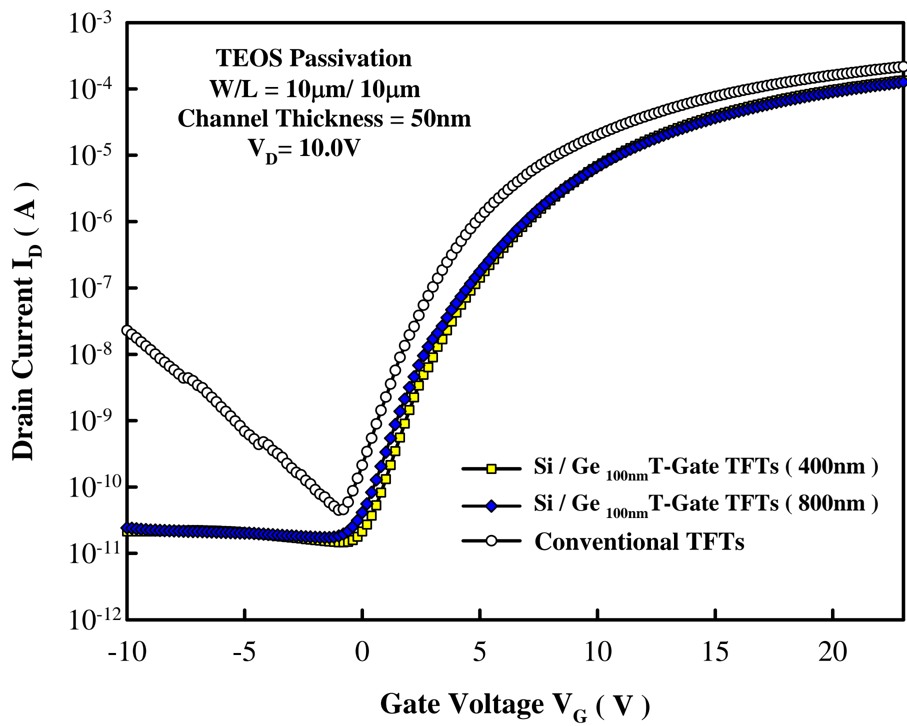


Fig. 3.11 The simulated vertical electric field along the channel (10 μm) direction near the drain the V_G= 0V, V_D= 15V. The different stacked Si/Ge gate thichness with SiNx passivation are shown.

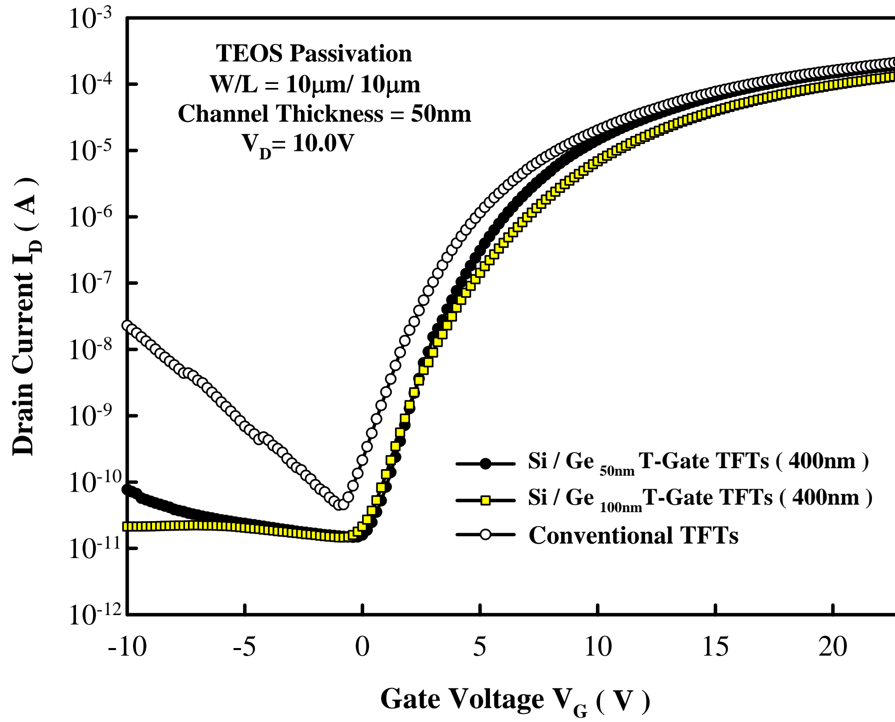


(a)

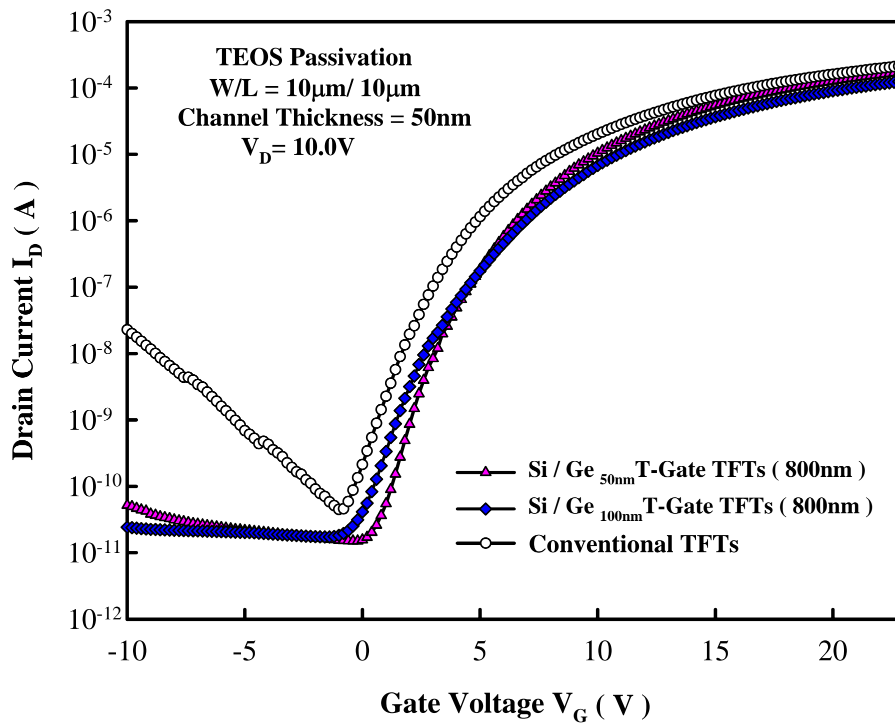




(b)

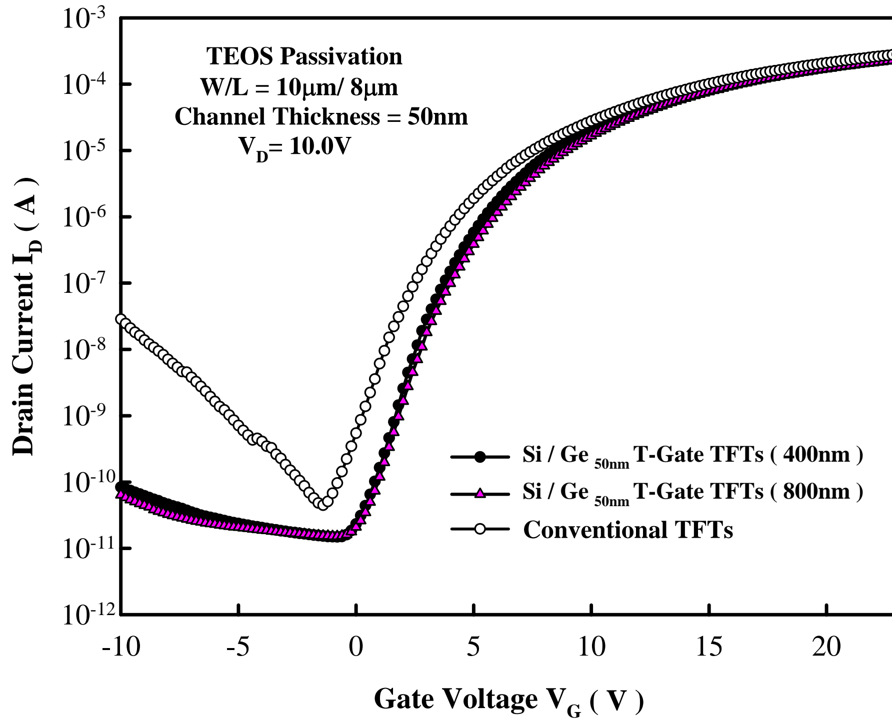


(c)

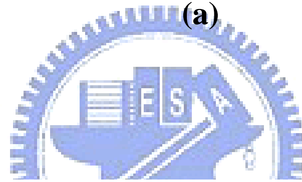


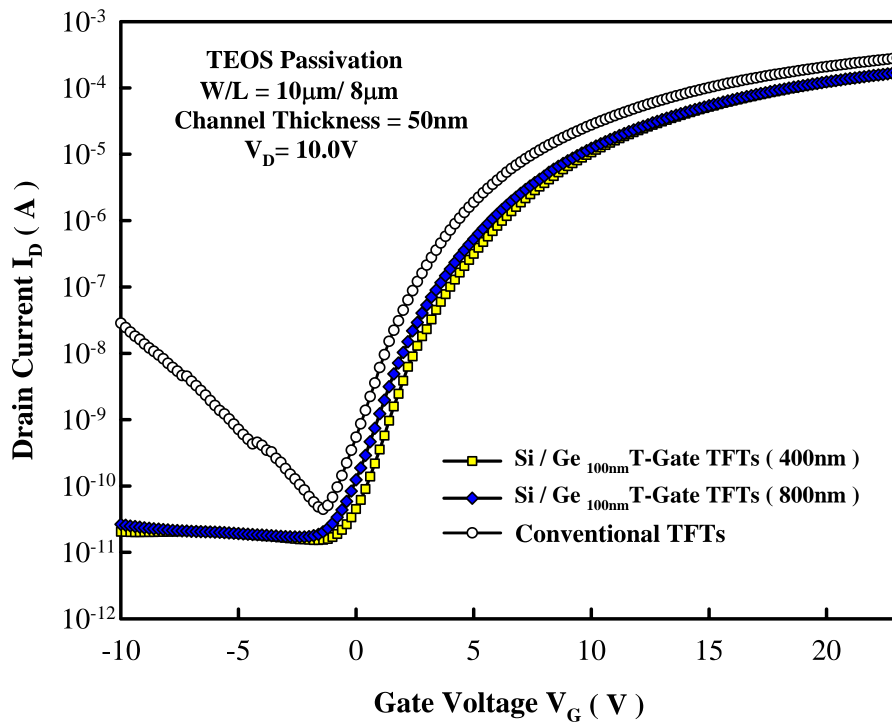
(d)

Fig.3.12(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 5 μm.

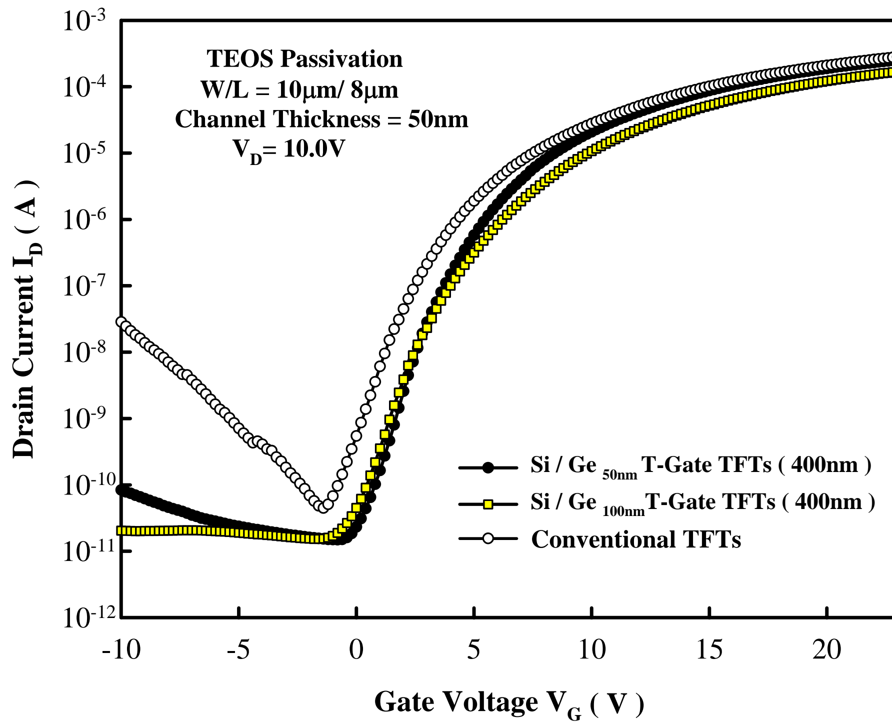


(a)

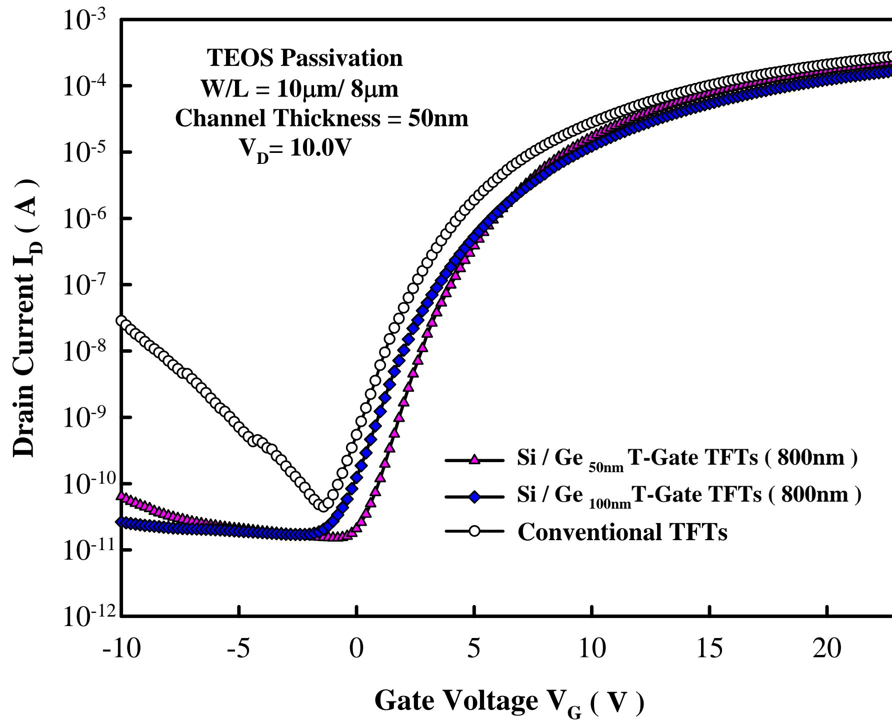




(b)

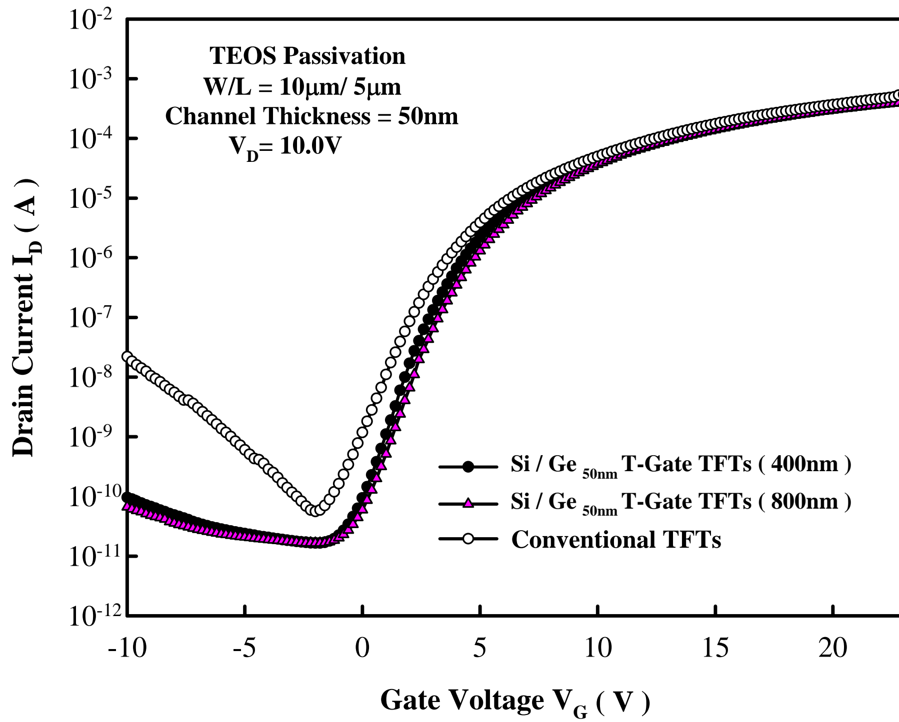


(c)

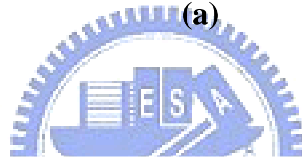


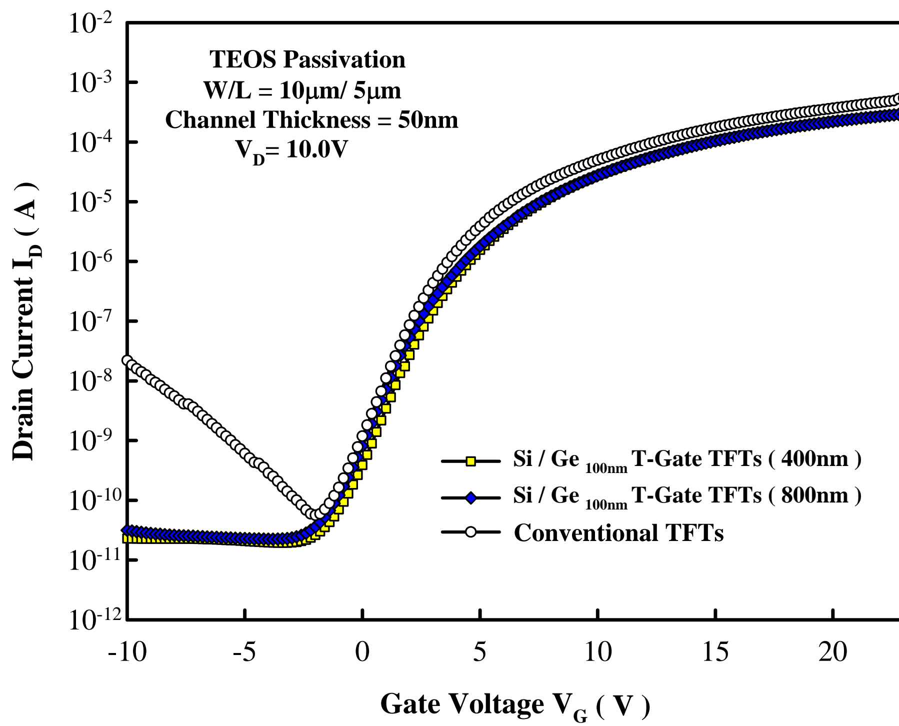
(d)

Fig.3.13(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 8 μ m.

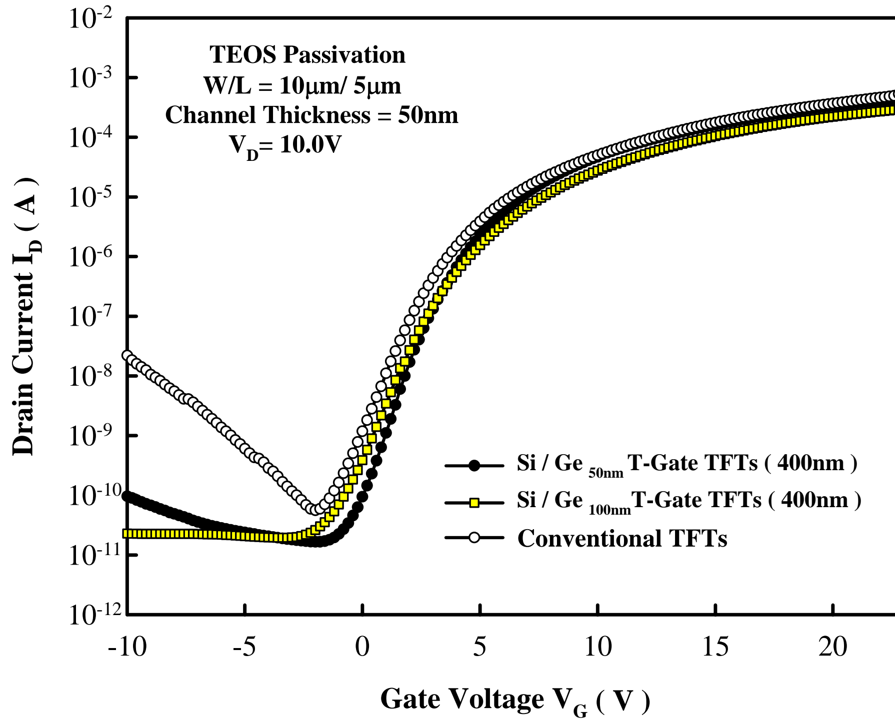


(a)

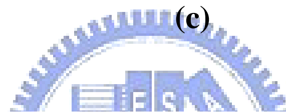


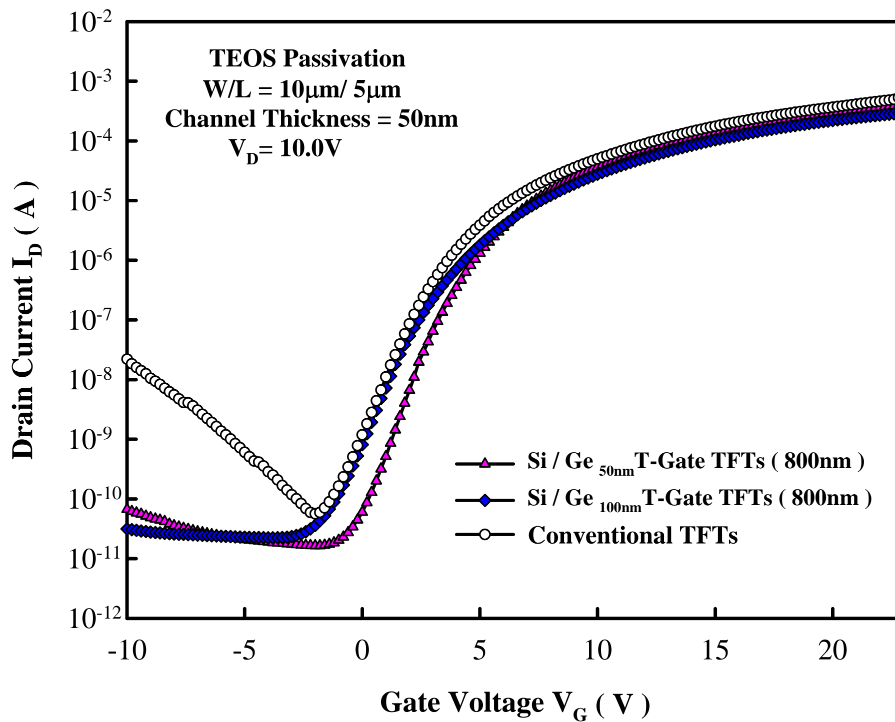


(b)



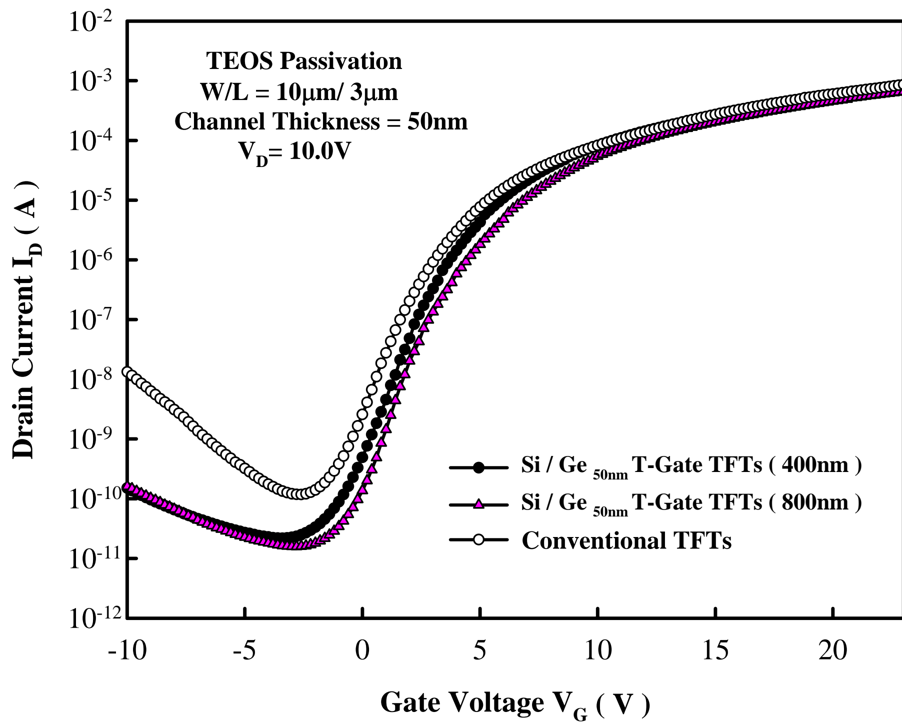
(c)



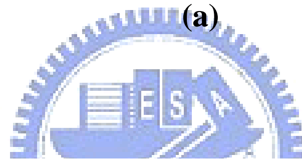


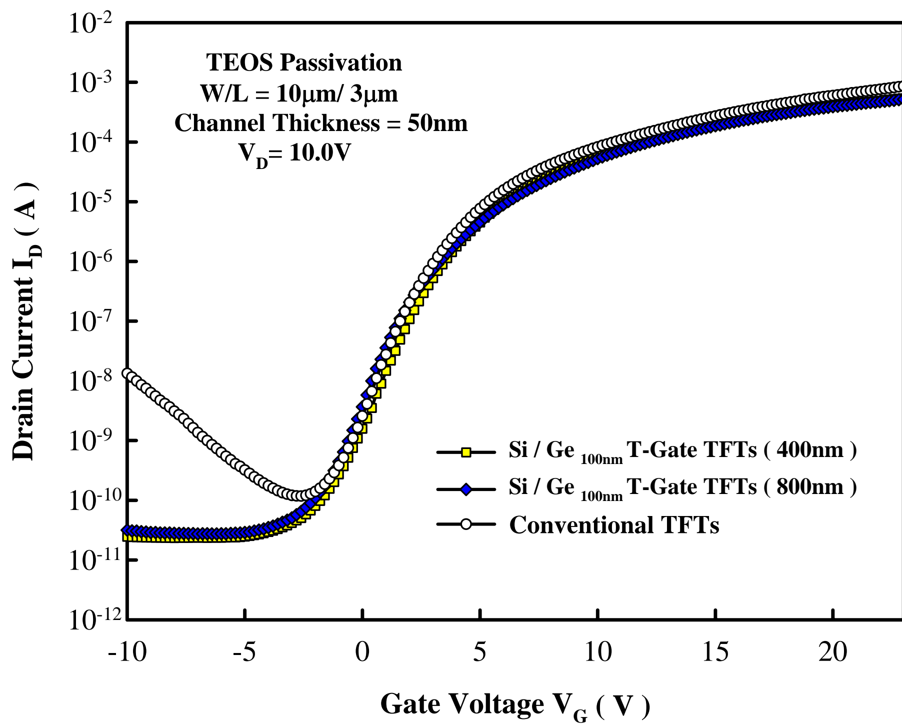
(d)

Fig.3.14(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 5 μm.

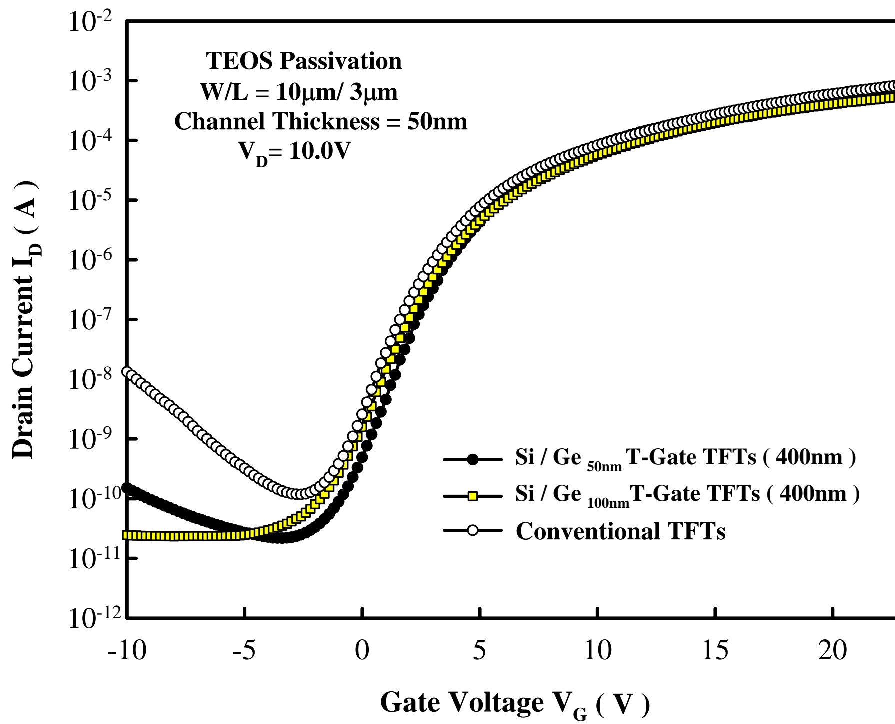


(a)

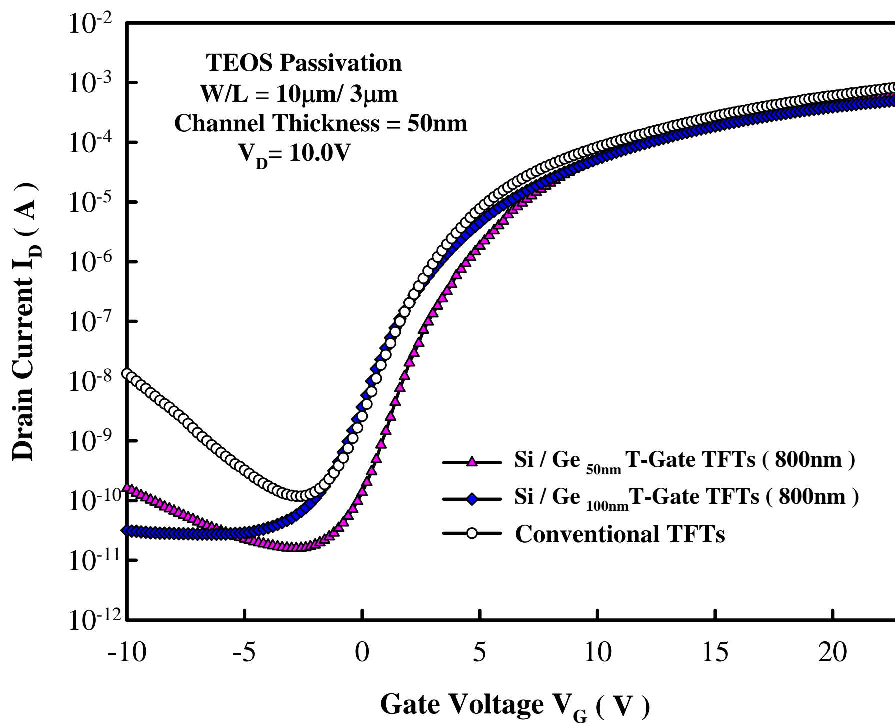




(b)



(c)



(d)

Fig.3.15(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm and gate length is 3 μ m.

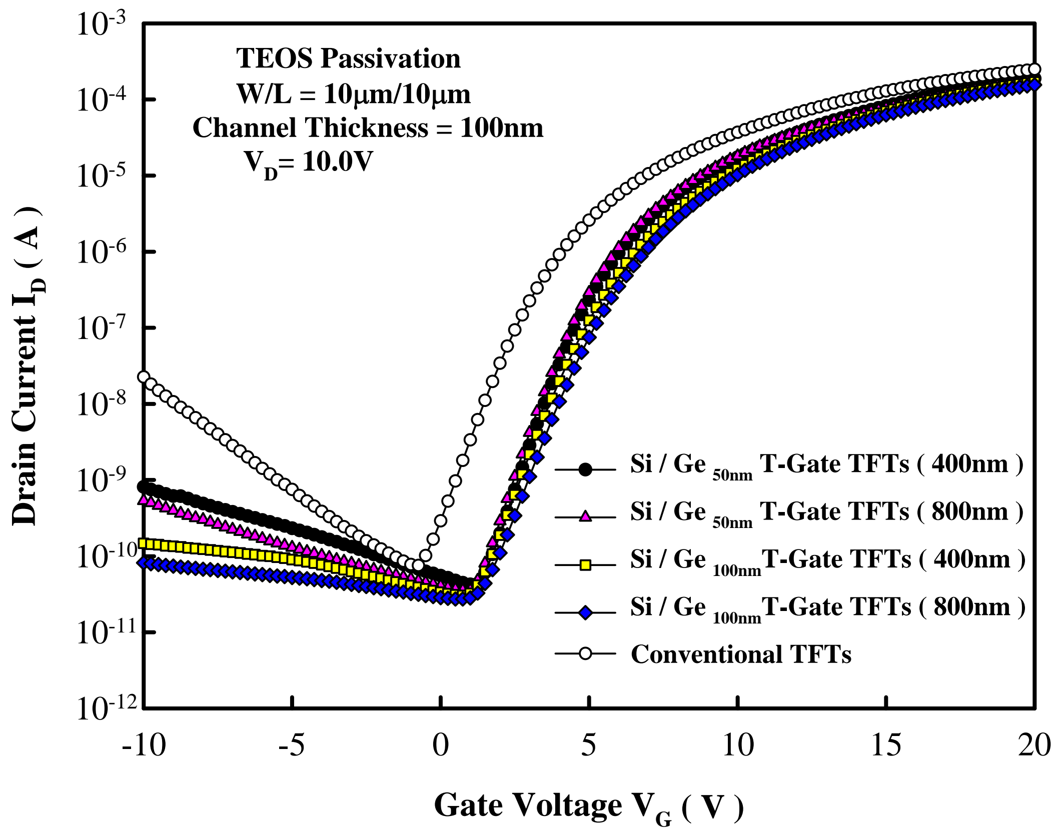


Fig.3.16 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 10 μ m.

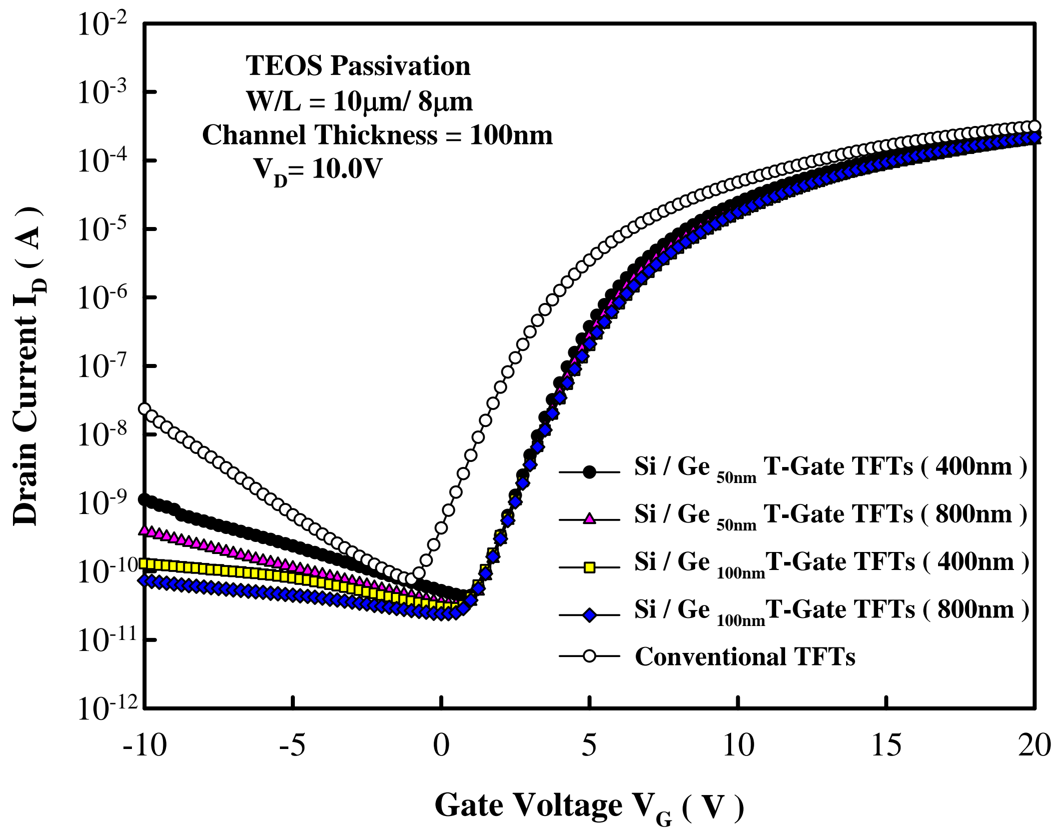


Fig.3.17 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 8 μ m.

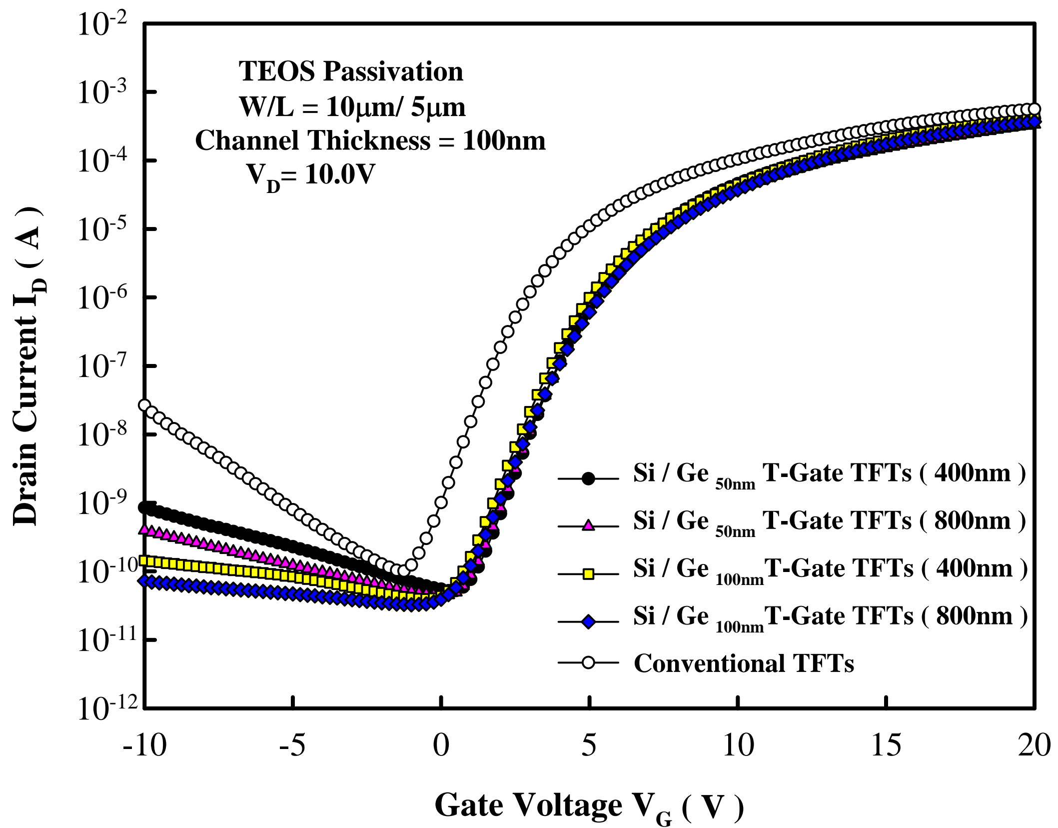


Fig.3.18 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 5 μ m.

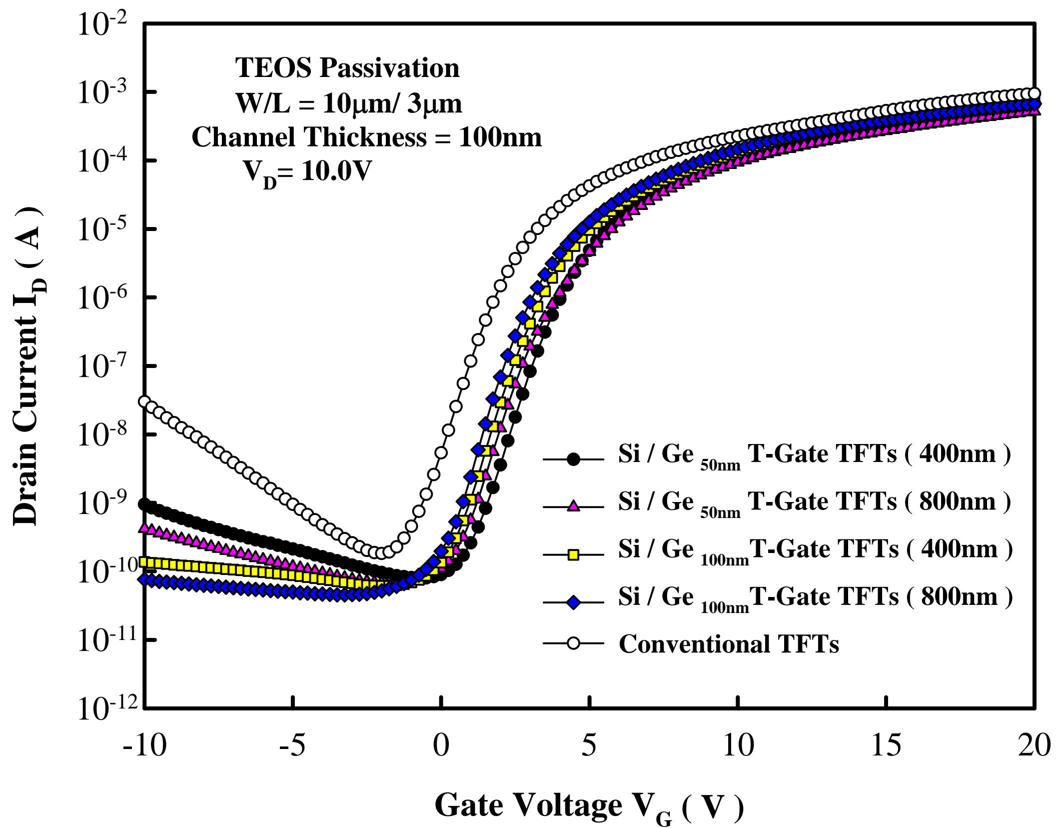
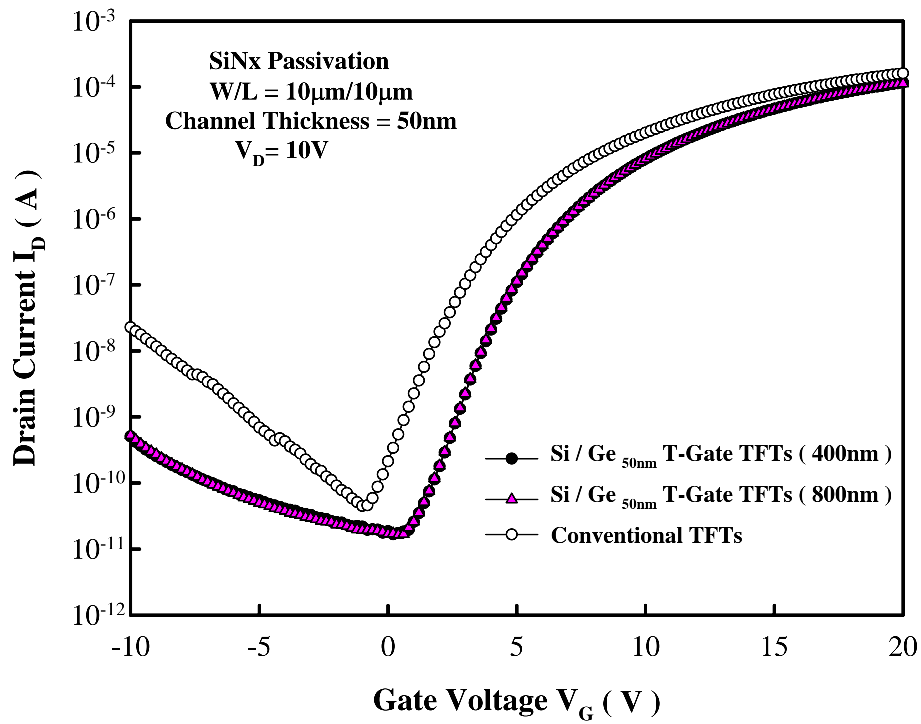
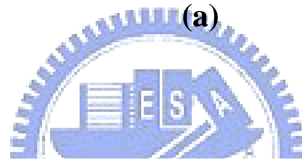
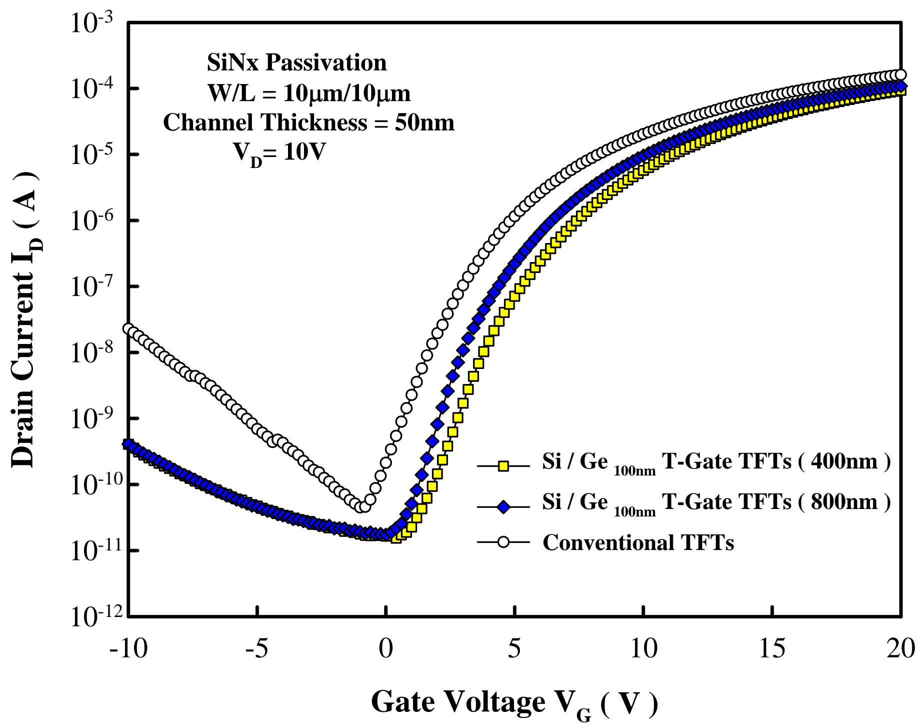


Fig.3.19 The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 100nm and gate length is 3 μ m.

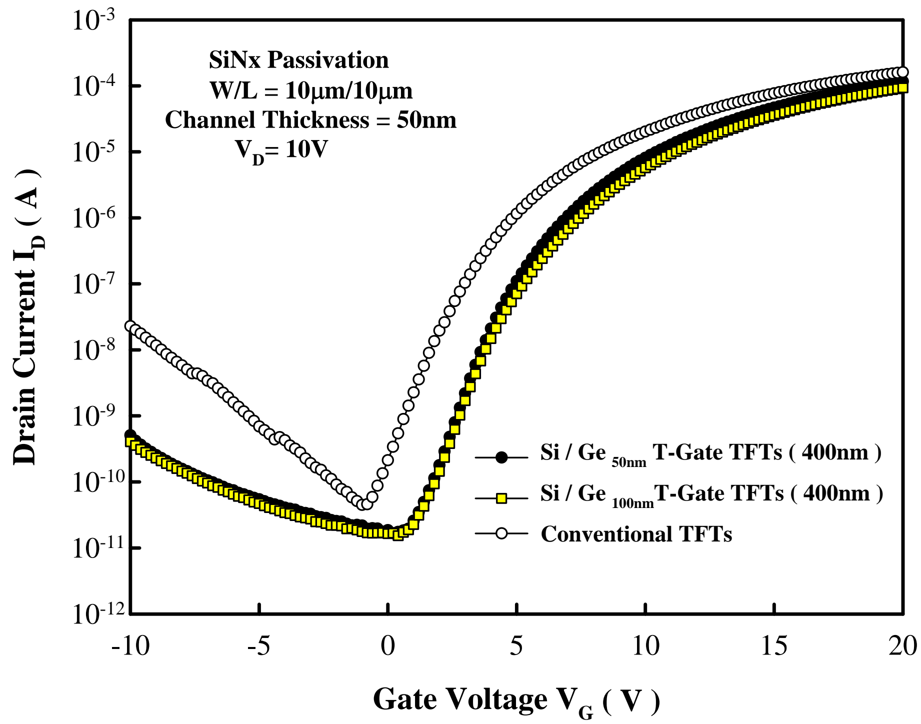


(a)

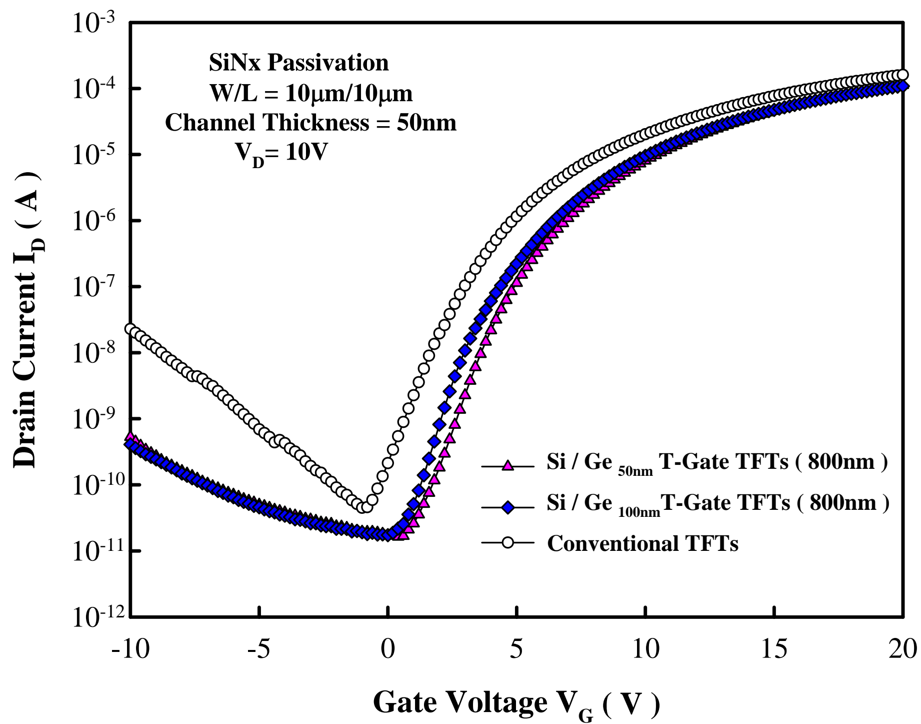




(b)

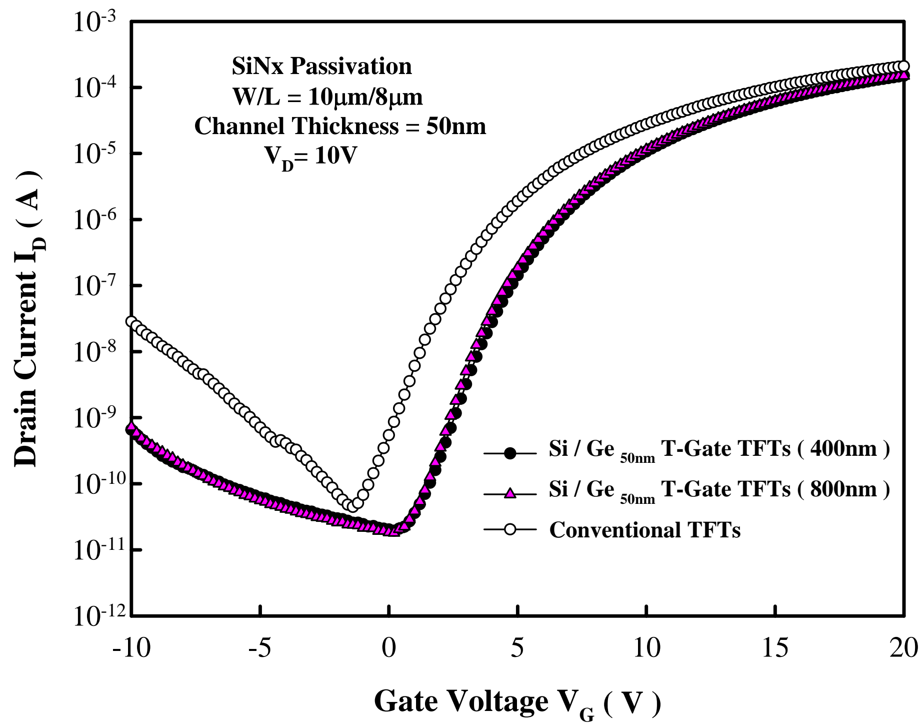


(c)

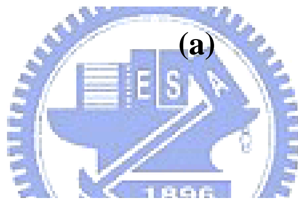


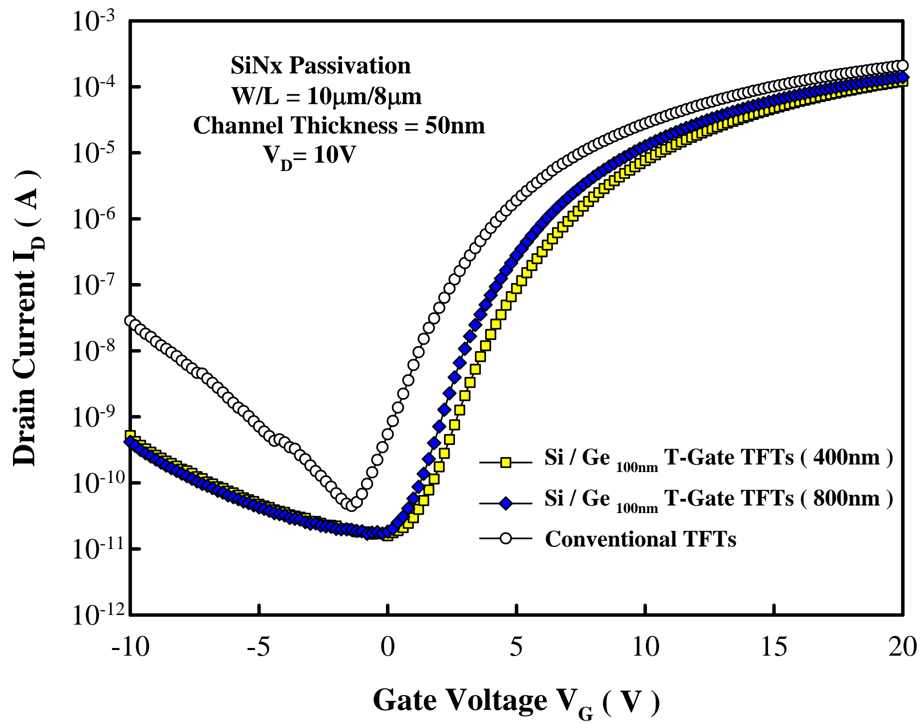
(d)

Fig.3.20(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 10 μ m.

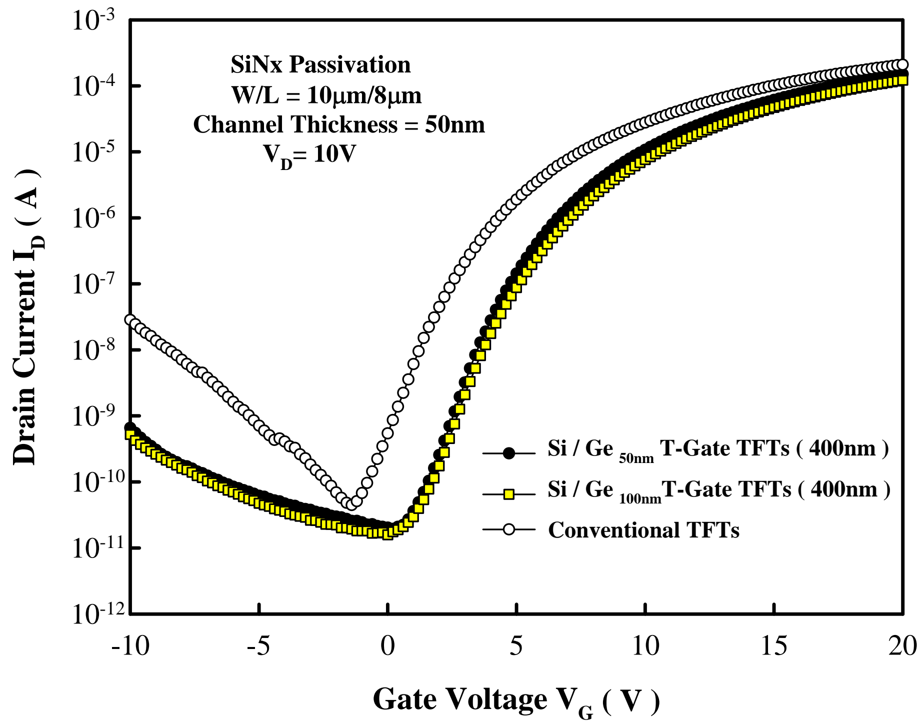


(a)

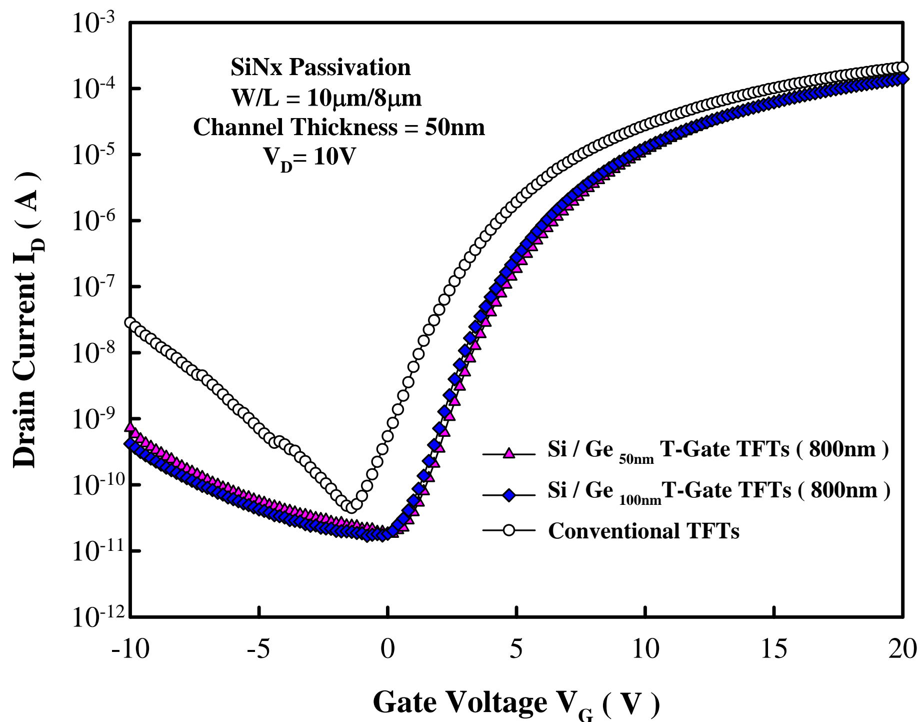




(b)

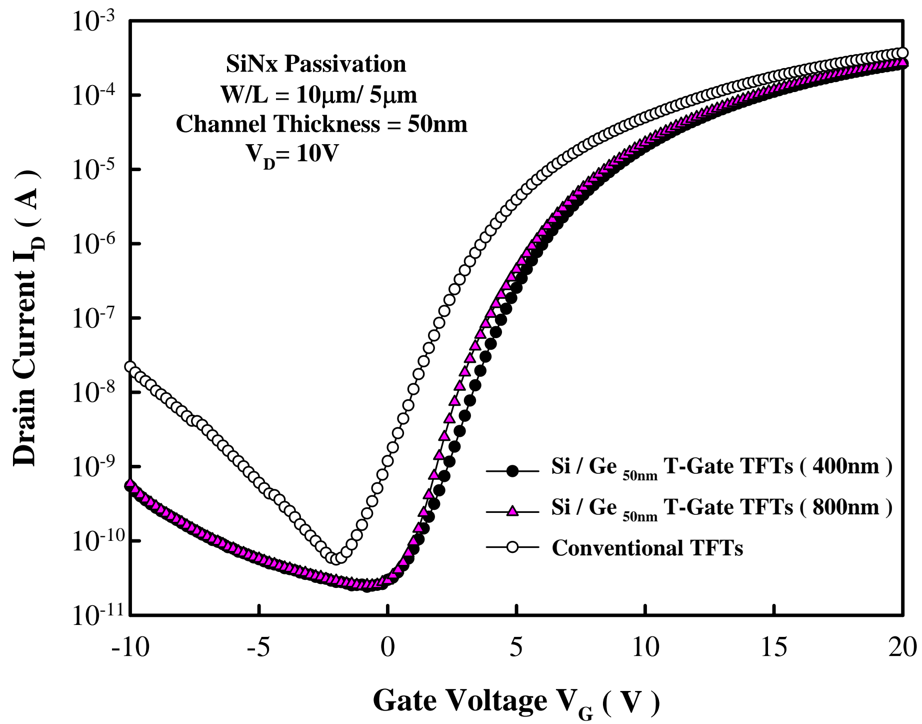


(c)

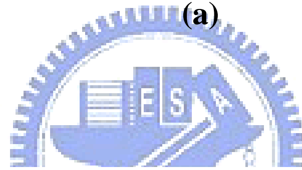


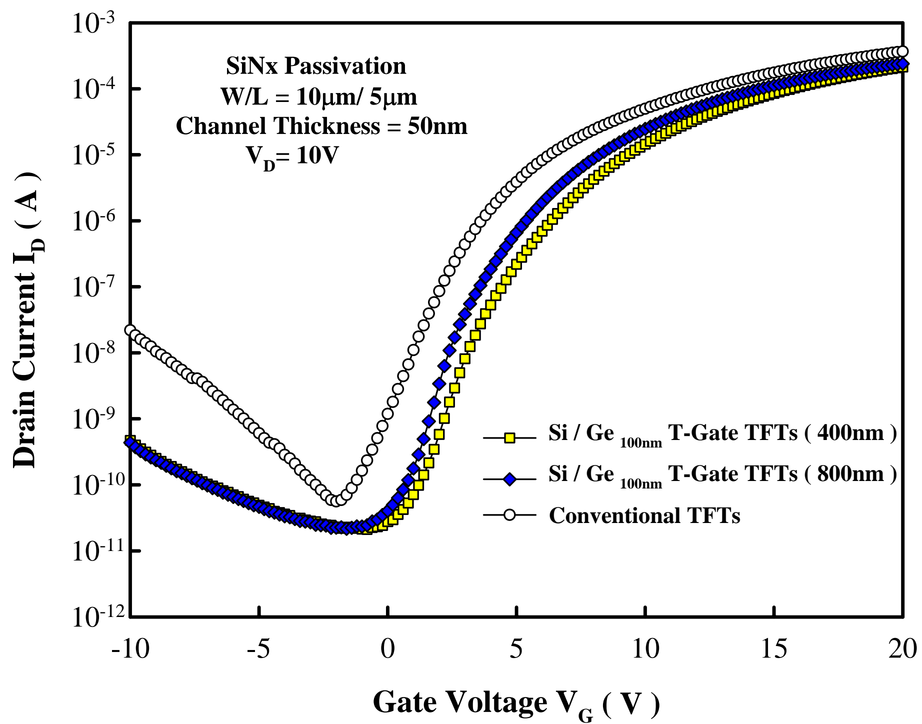
(d)

Fig.3.21(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 8 μ m.

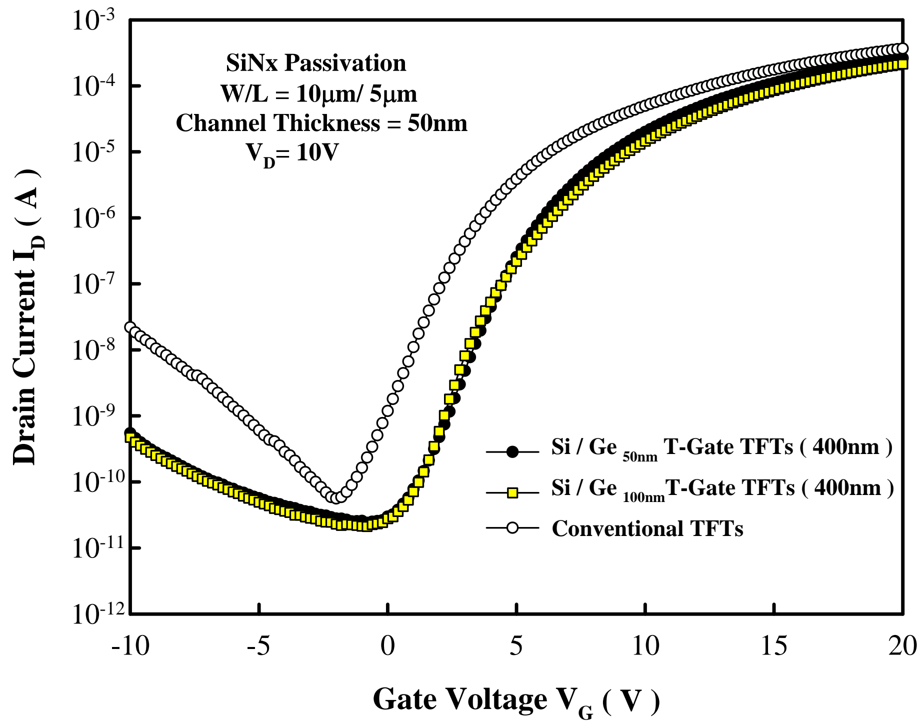


(a)

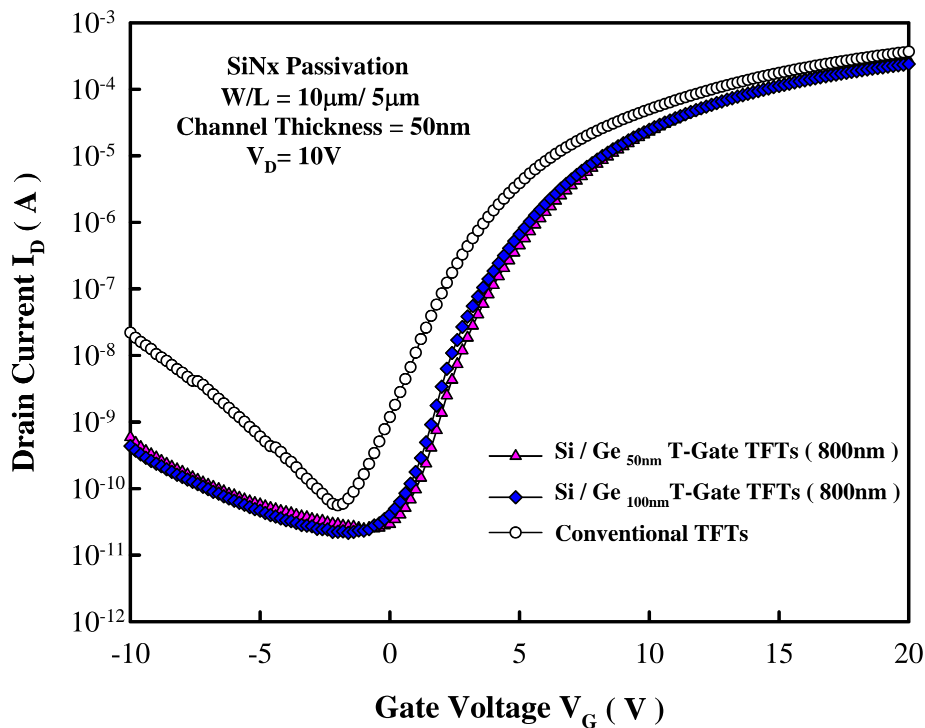




(b)

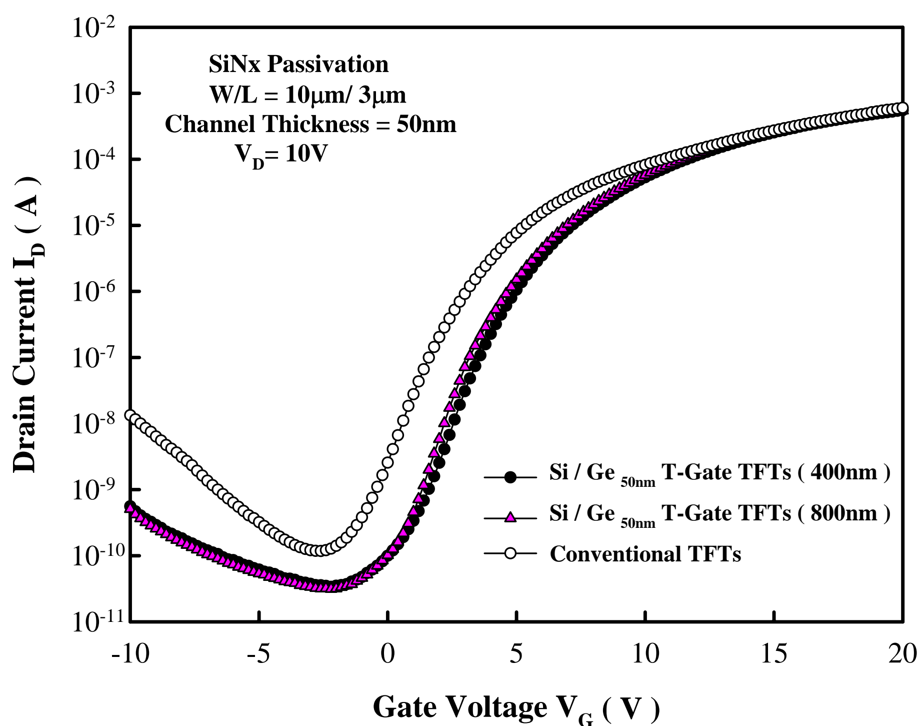


(c)

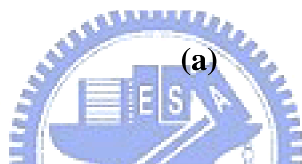


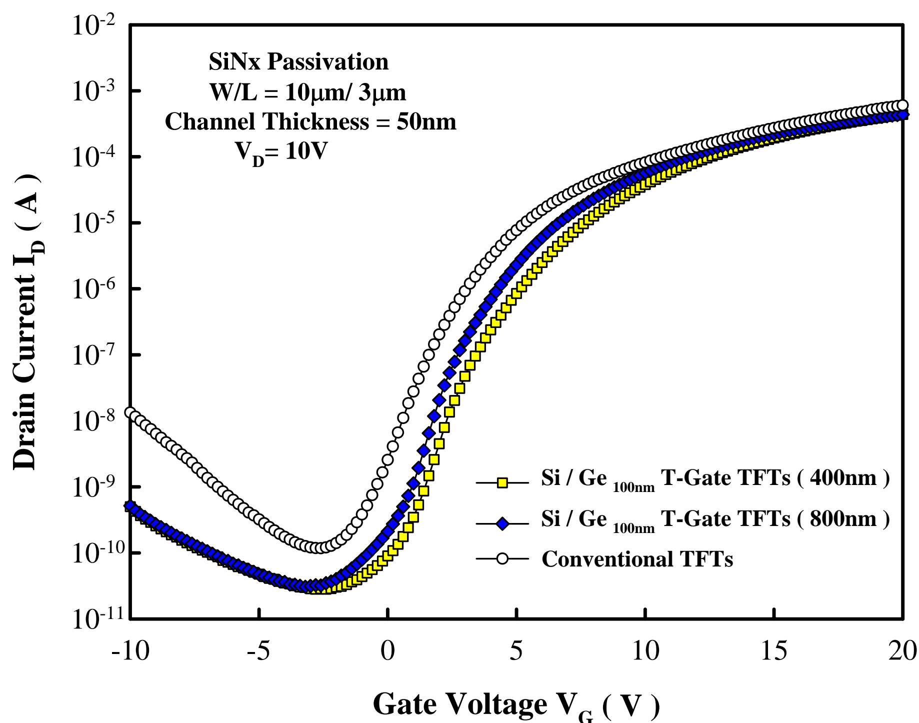
(d)

Fig.3.22(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 5 μ m.

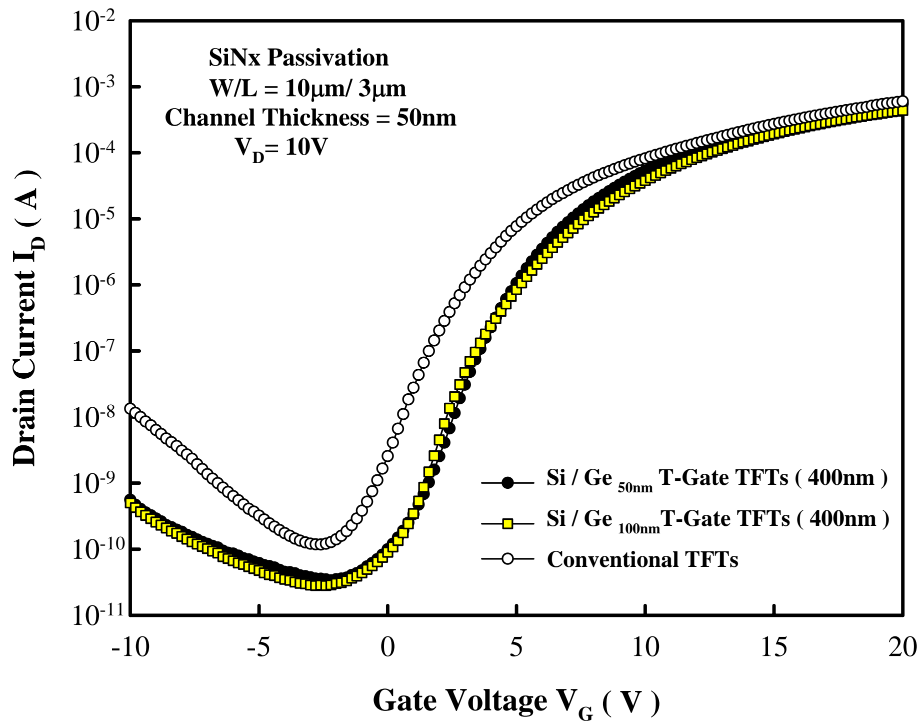


(a)

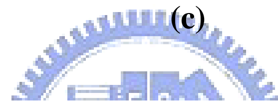


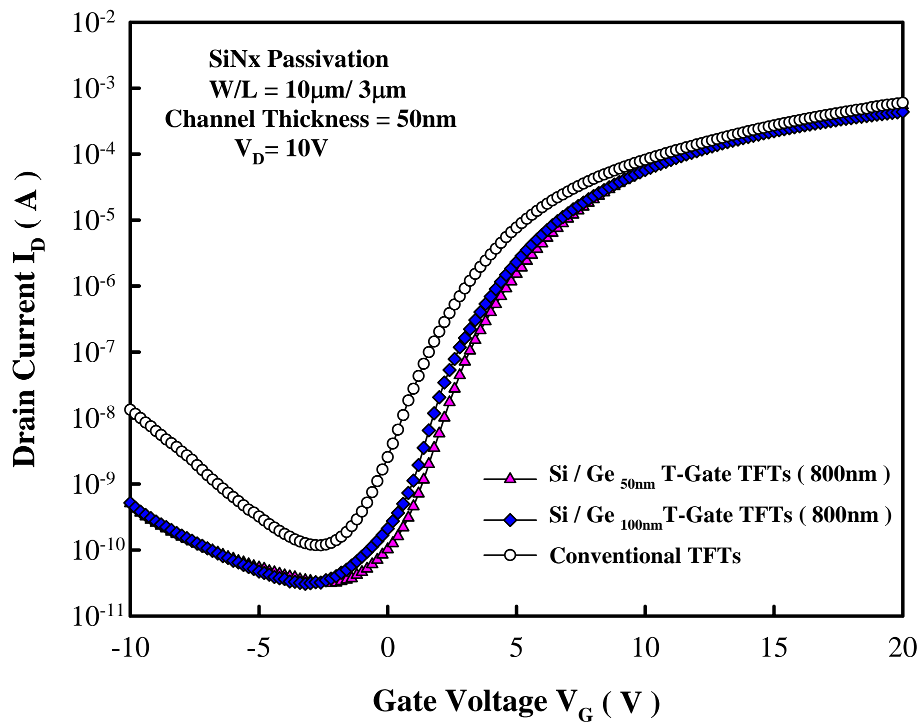


(b)



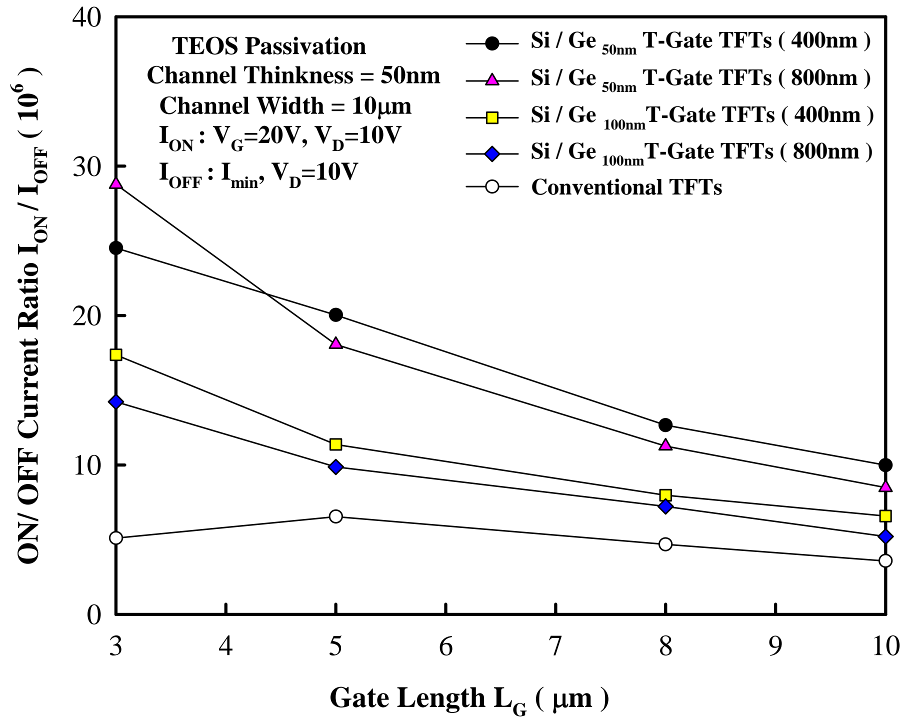
(c)



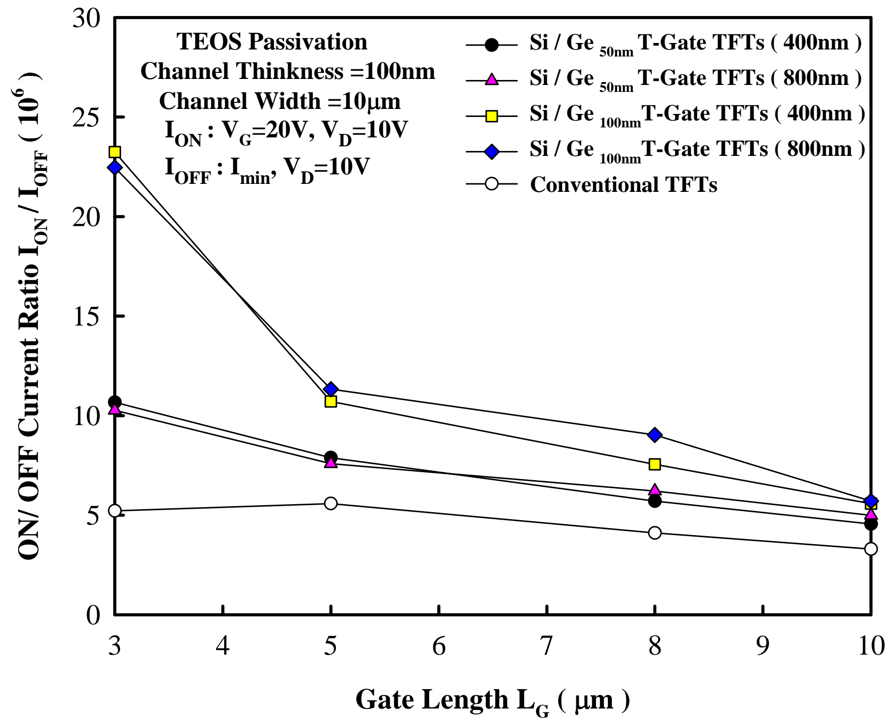


(d)

Fig.3.23(a) ~ (d)The transfer characteristics of the Si/Ge T-Gate TFTs with different thickness of stacked Si/Ge and undercut length. The channel thickness is 50nm, gate length is 3 μ m.



(a)



(b)

Fig.3.24 Gate length dependence of On/ Off current ratio in Si/Ge T-gate TFTs with TEOS passivation and conventional TFT. (a) The channel thickness is 50nm (b) The channel thickness is 100nm.

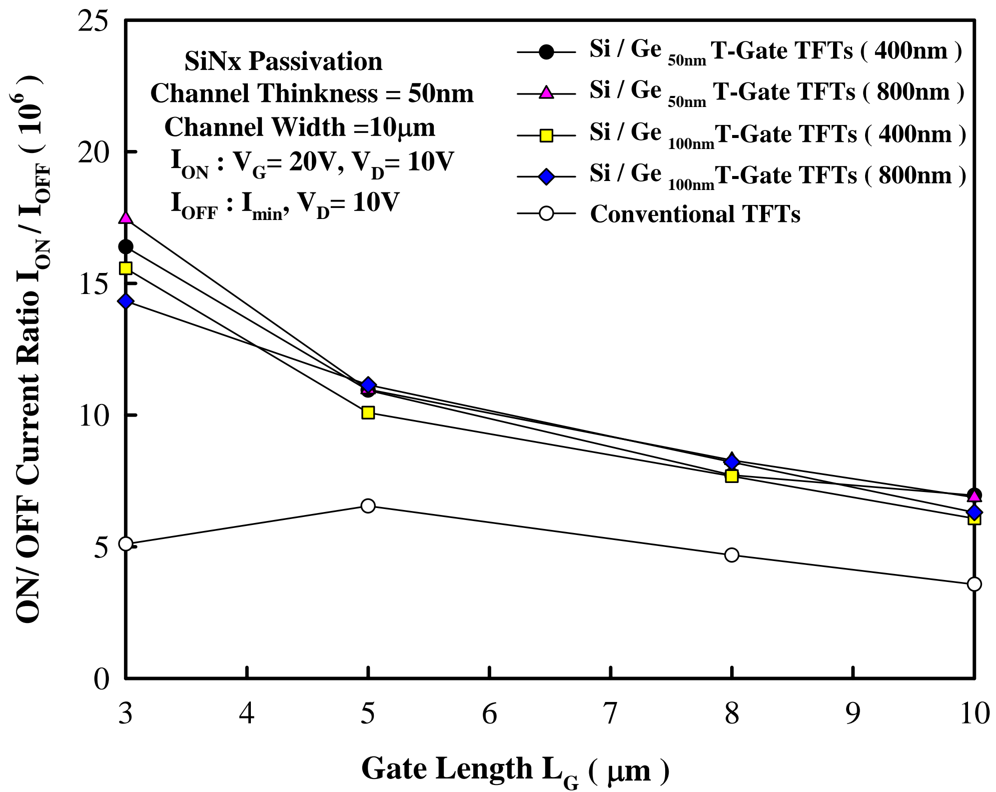
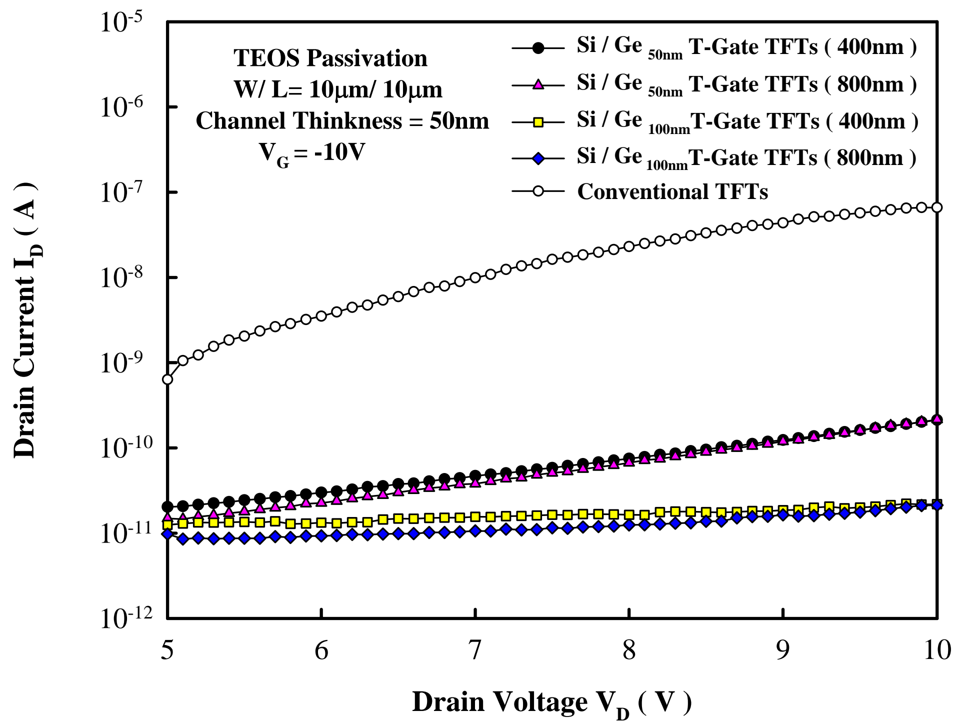
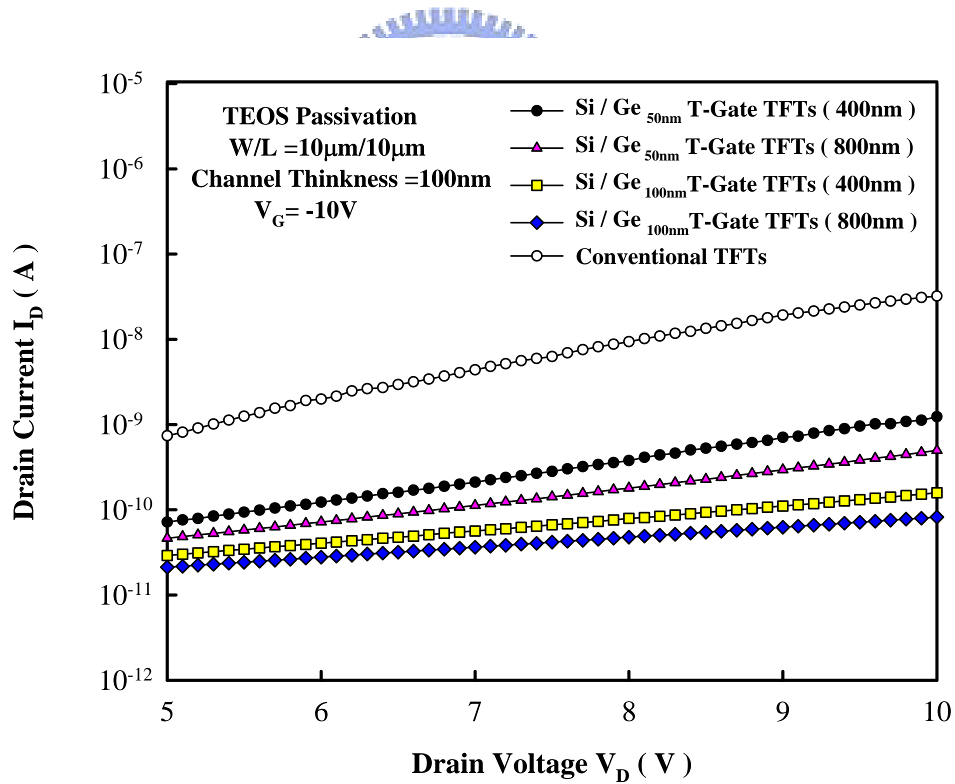


Fig.3.25 Gate length dependence of On/ Off current ratio in Si/Ge T-gate TFTs with Si_3N_4 passivation and conventional TFT.



(a)



(b)

Fig.3.26 Off-state leakage Characteristics in Si/Ge T-gate TFTs with TEOS passivation which compared with conventional TFT. (a) The channel thickness is 50nm (b) The channel thickness is 100nm.

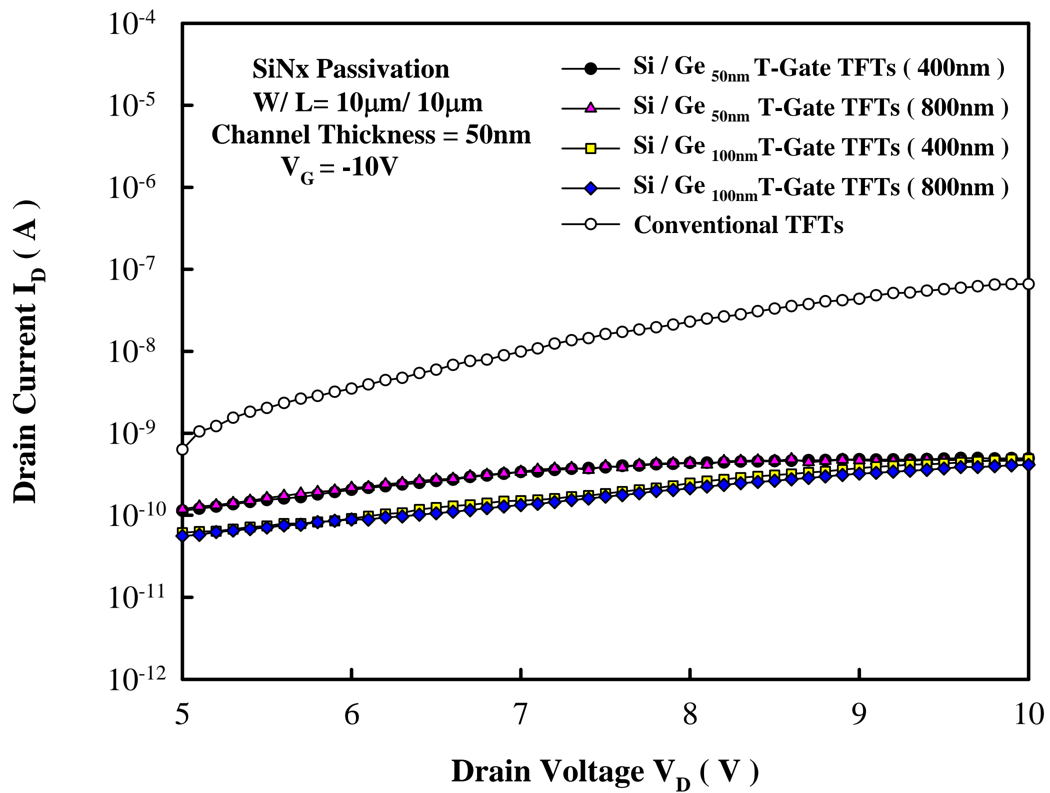
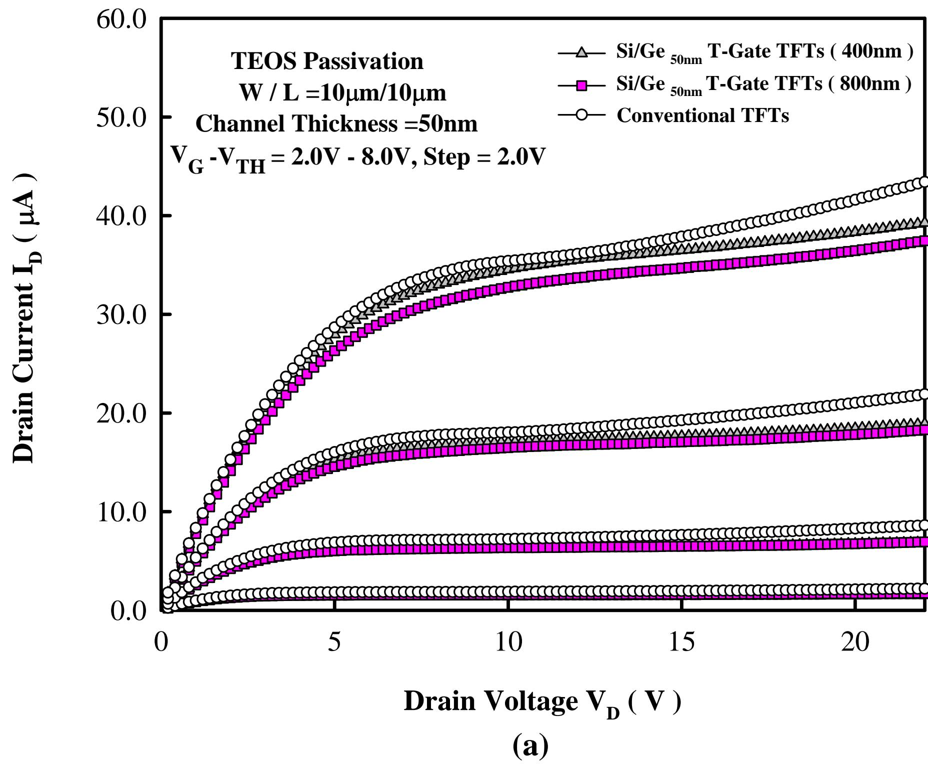
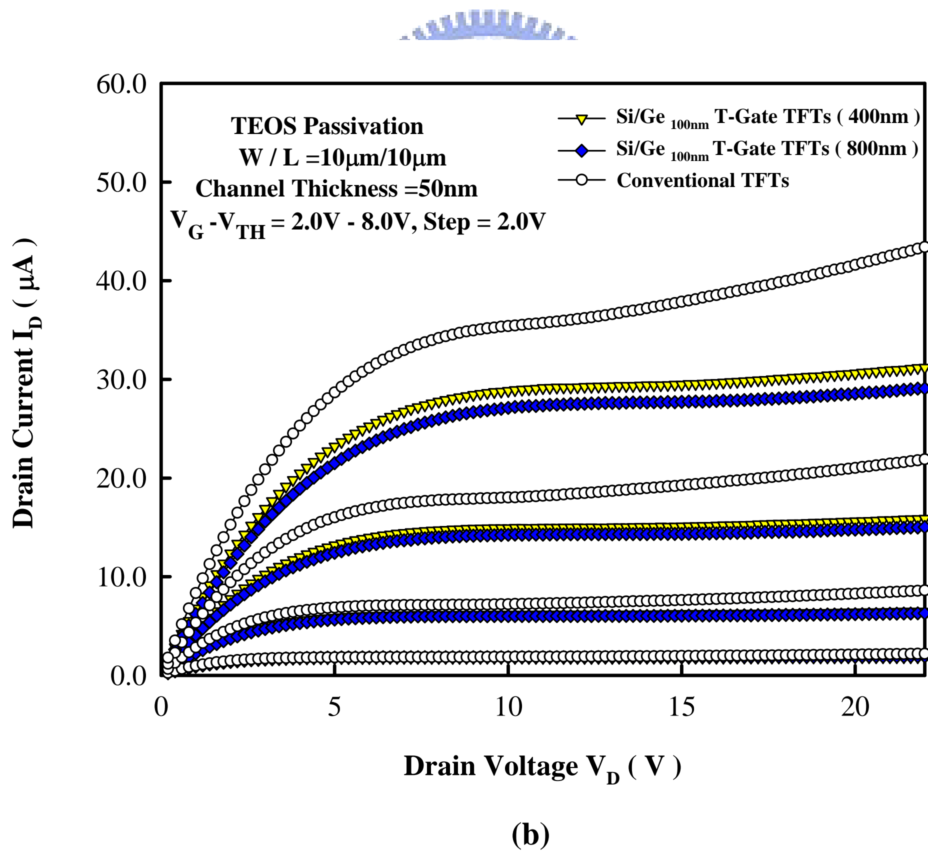


Fig.3.27 Off-state leakage Characteristics in Si/Ge T-gate TFTs with Si_3N_4 passivation which compared with conventional TFT.

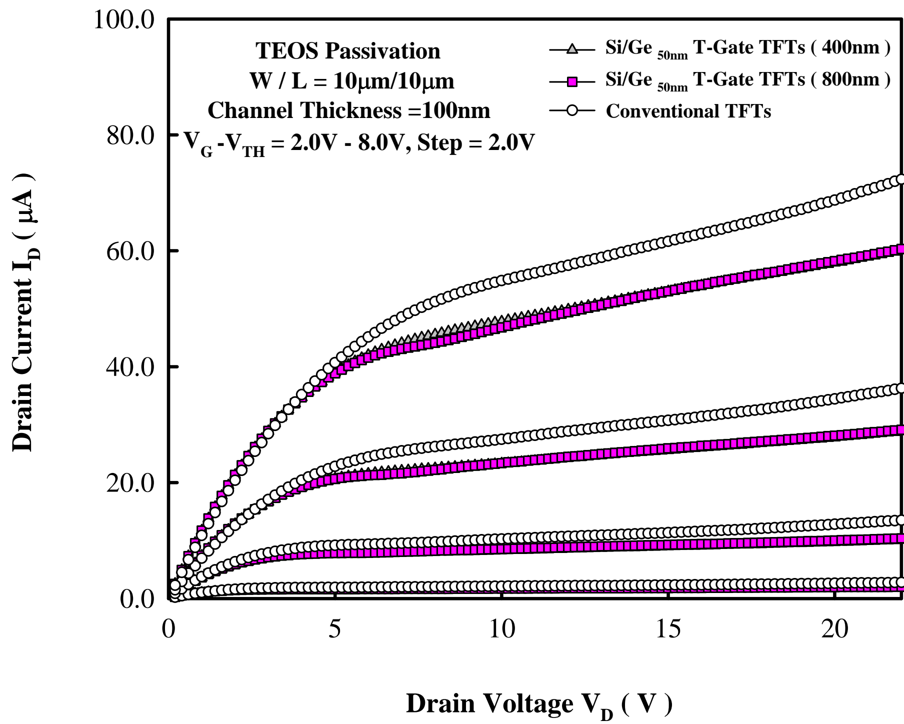


(a)

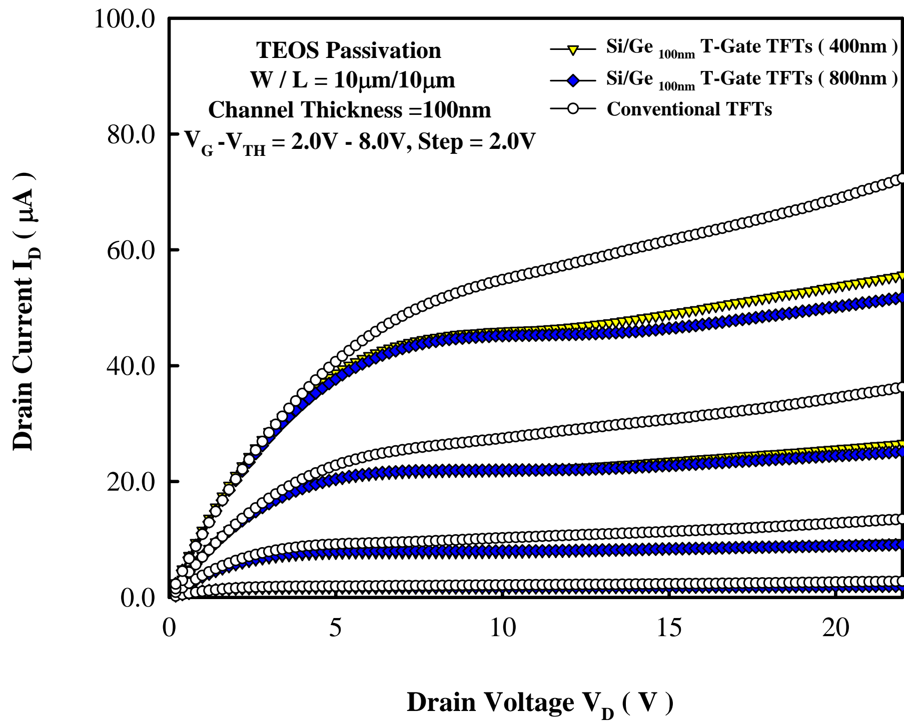


(b)

Fig.3.28 The output characteristics of the Si/Ge T-Gate TFTs with TEOS passivation. The channel thickness is 50nm. (a) Germanium layer thickness is 50nm (b) Germanium layer thickness is 100nm.

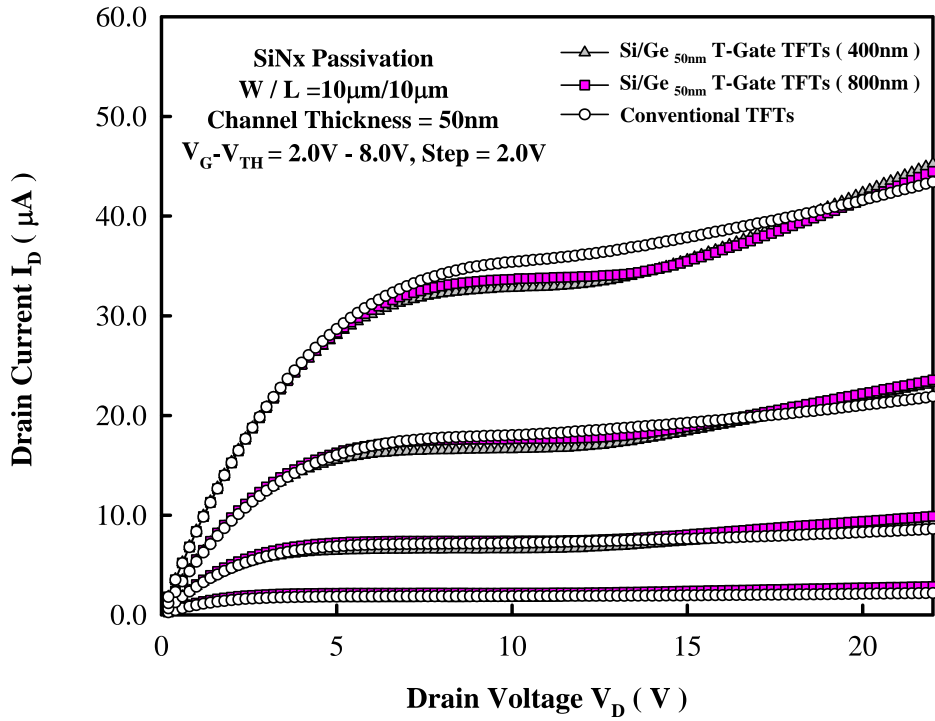


(a)

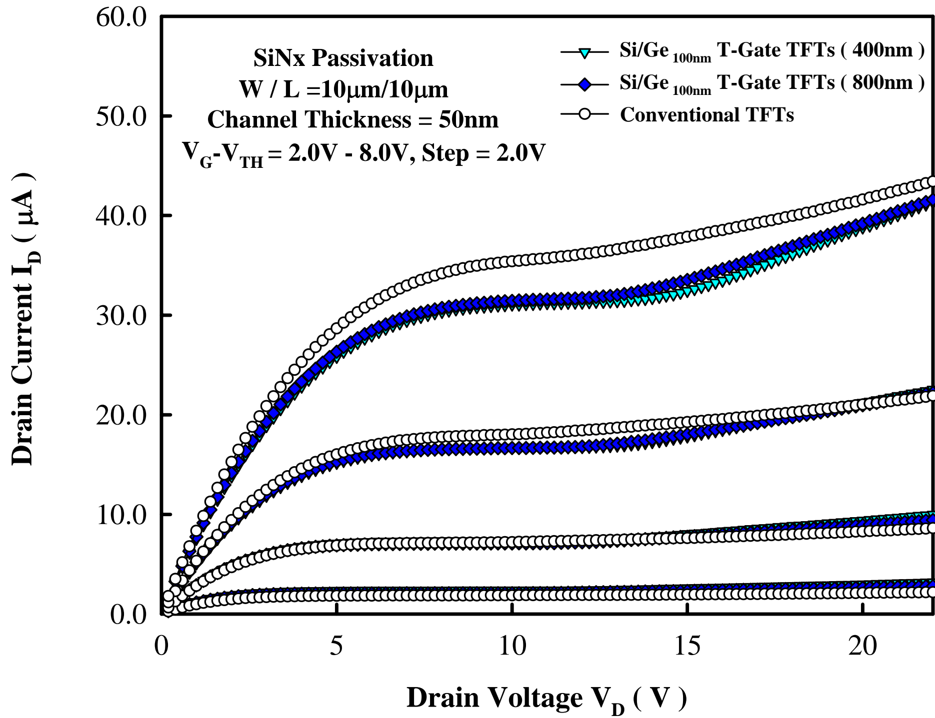


(b)

Fig.3.29 The output characteristics of the Si/Ge T-Gate TFTs with TEOS passivation .The channel thickness is100nm. (a) Germanium layer thickness is 50nm (b) Germanium layer thickness is 100nm.

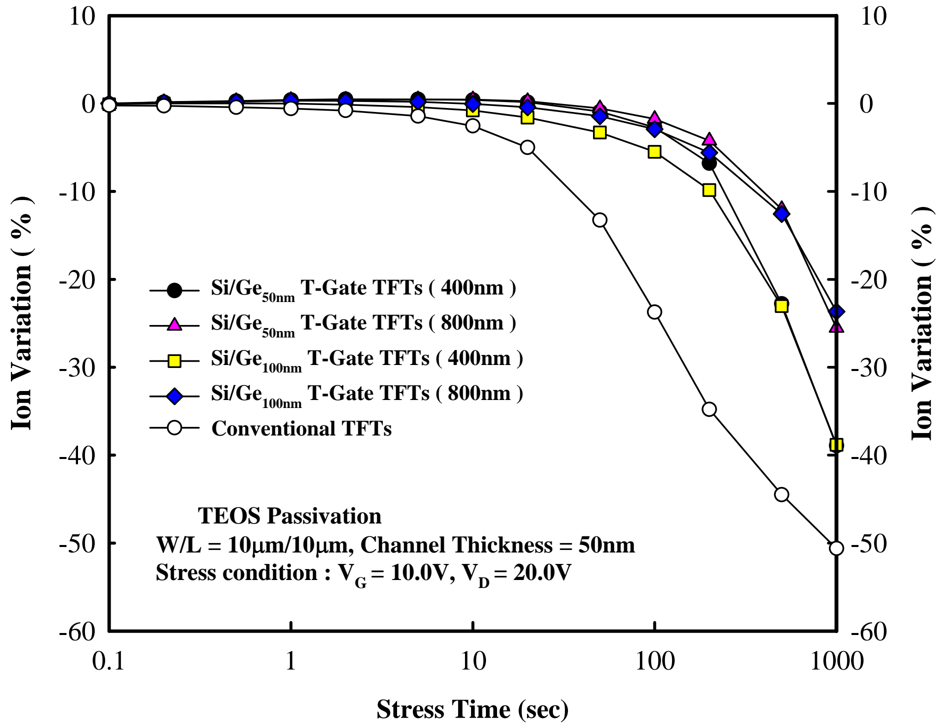


(a)

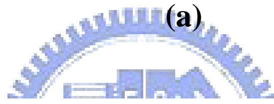


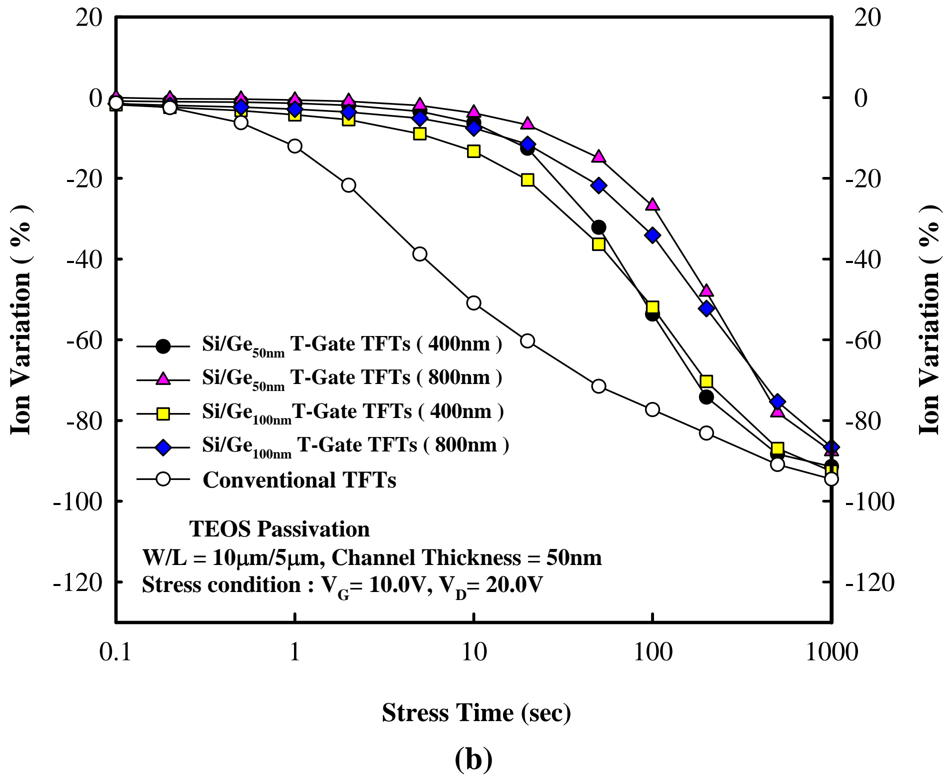
(b)

Fig.3.30 The output characteristics of the Si/Ge T-Gate TFTs with Si_3N_4 passivation. The channel thickness is 50nm. (a) Germanium layer thickness is 50nm (b) Germanium layer thickness is 100nm.



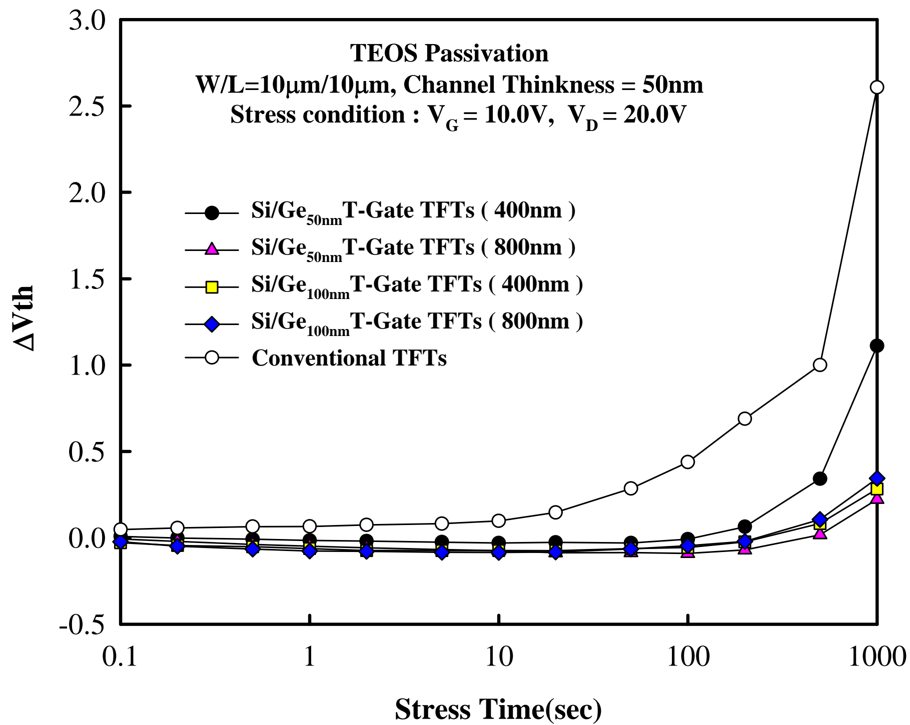
(a)



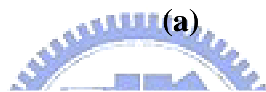


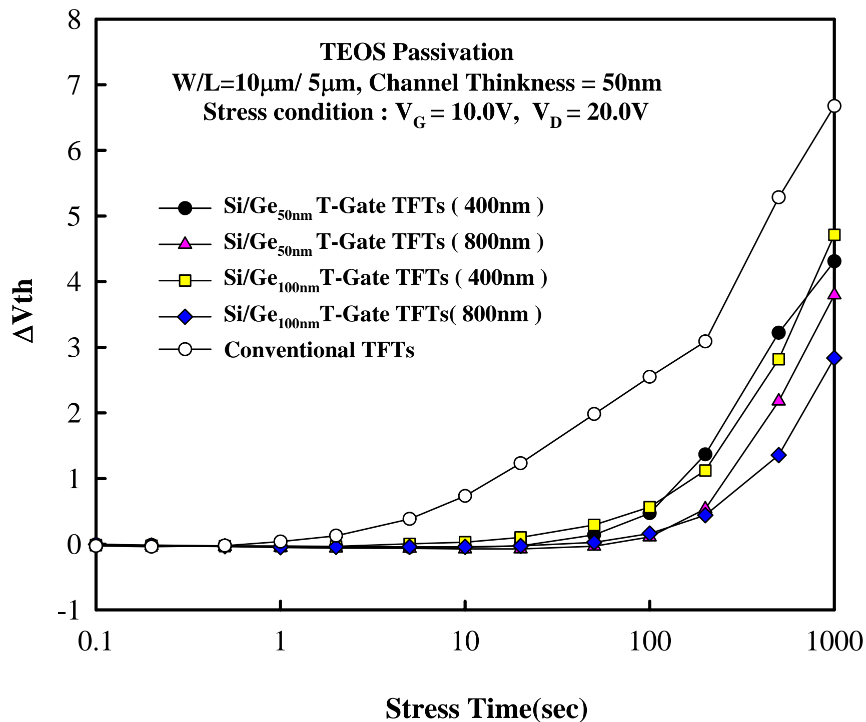
(b)

Fig.3.31 Stress time dependence of I_{on} variation in Si/Ge T-Gate TFTs and conventional TFT. (a) Channel length is 10 μ m. (b) Channel length is 5 μ m.



(a)





(b)

Fig.3.32 Variations of the threshold voltage under hot carrier stress in conventional TFT and Si/Ge T-Gate TFTs. (a) Channel length is 10 μ m. (b) Channel length is 5 μ m.

Chapter 4

Conclusions and Future Works

4.1 Conclusions

In this thesis, a novel poly-silicon thin-film transistor with stacked Si/Ge T-Gate has been proposed and successfully demonstrated. Device simulation was also performed to help understanding the operation of the fabricated devices. From the simulation results, it is observed that the maximum electric fields of Si/Ge T-Gate TFTs are much smaller than those of the conventional TFTs. The increase in drain electric field will result in a high anomalous leakage current at high drain biases. We found that the leakage current of T-Gate devices are reduced lower more than that of the conventional structure. The On-Off current ratio of the new TFT is significantly increased. On the other hand, it is shown that the Si/Ge T-Gate TFTs have better hot carrier stability which is comparable to the conventional TFT.

Si/Ge T-Gate TFTs with different channel thickness have been investigated in this thesis. The devices with thin channel thickness have low grain-boundary trap density in the poly-Si material that will suppress the sever kink at high drain biases. However, the Si/Ge T-Gate TFTs with good current saturation characteristics compared with conventional TFT because of the reduced of lateral electric field. The Si/Ge T-Gate TFTs with thick germanium layer and long undercut length have low off-state leakage current which caused by effectively suppressed the vertical and lateral electric field.

The high-k material has been used as a passivation layer for fabrication of T-Gate devices in this thesis. The Si/Ge T-Gate TFTs with Si_3N_4 passivation can provide high on-state current while still maintaining a leakage current, which compared with conventional TFT. Although the off-state current is increased than that with the TEOS passivation T-Gate

TFT, the subthreshold swing and on-state characteristic are improved effectively.

4.2 Future Works

The Si/Ge T-Gate structure can be form by elective wet etch method, but the etch time and temperature of liquors are difficult to control. Furthermore, the TEOS oxide deposited by LPCVD has poor quality which would cause additional problems. Thus, we must find the optimum conditions to accurately control the length of undercut and use PECVD for deposit the TEOS oxide.

The T-Gate structure can be applied as a memory device. This idea is shown in Figure 4.1. The oxide/SiNx/oxide stacked layers be formed under the undercut region of T-Gate TFTs. The expression of good data retention and endurance will be expected.

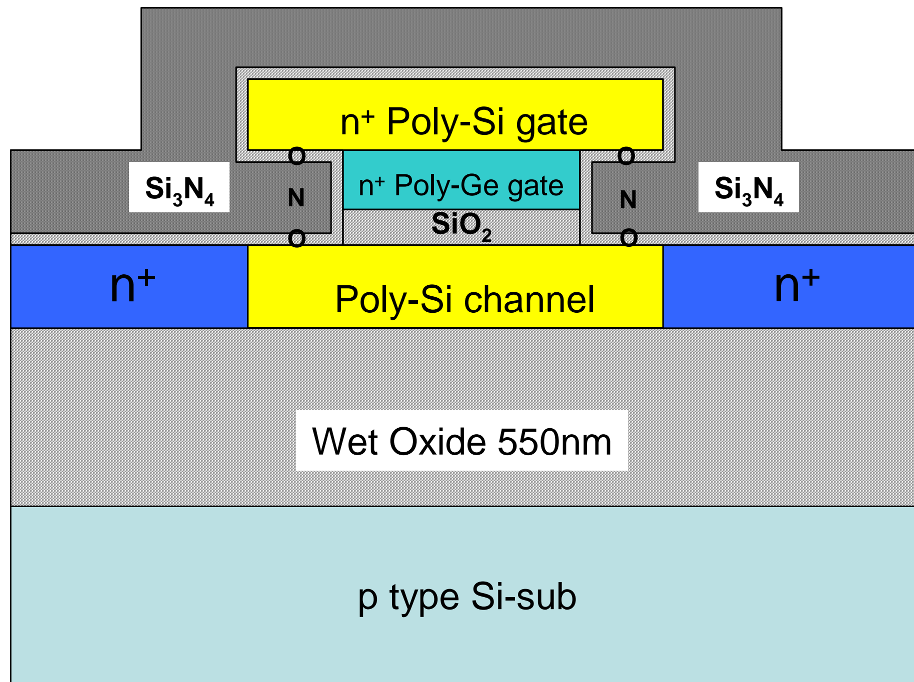


Fig.4.1 The schematic cross section of stacked Si/Ge T-Gate TFT with O/N/O tripping layer.

References

[1] N. Yamauchi, and R. Reif, "Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments, and thin-film transistor application," *J.Appl. Phys.*, vol. 75, pp.3235-3257, 1994.

[2] W. G. Hawkin, "Polycrystalline-silicon device technology for large-area electronics," *IEEE Trans. Electron Device*, vol.33, p.481, 1986.

[3] I. W. Wu, W. B. Jackson, T. Y. Huang, A. G. Lewis and Ciang, " Passivation Kinetics of Two Types of Defects in Polysilicon TFT by plasma hydrogenation", *IEEE Electron Device Lett.*, vol.12, p.181, 1991.

[4] Y. Morimoto, Y. Jinno, K. Hirai, H. Ogata, T. Yamada and K. Yoneda, "Influence of the Grain Boundaries and Intragrain Defects on the Performance of Poly-Si Thin Film Transistors", *J. Electrochem. Soc.*, vol.144, 1997.

[5] J. G. Fossum, A. Ortiz-Conde, H. Shicjijo, and S. K. Banerjee, "Anomalous Leakage Current in LPCVD Polysilicon MOSFET's, "*IEEE Trans. Electron Device*, vol.32, pp.1878-1884,1985.

[6] I-Wei Wu, Alan G. Lewis, TIAO-yuan Huang, Warren B. Jackson, and Anne Chiang, "Mechanism and Device-to-Device Variation of Leakage Current in Polysilicon Thin-Film Transistor," *IEDM Tech.Dig.*,pp.867-870,1990.

[7] K. R. Olasupo, M. K. Hatalis, "Leakage Current Mechanism in Sub-Micron Polysilicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol.43, pp.1218-1223, 1996.

[8] F. Emoto, K. Senda, E. Fujii, A. Nakamura, A. Yamamoto, "Solid Phase Growth Technique for High Cut-Off Frequency Polysilicon TFT Integrated Circuits on a Quartz Substrate," *IEEE Trans. Electron Device*,vol.37, p.1462,1990.

[9] A. Chiang, T. Y. Huang, I- W. Wu and M. H. Zarzycki, "Effects of Silicon Implantation

and Processing Temperature on Performance of Poly-Crystalline Silicon Thin-Film Transistors Fabricated from Low Temperature CVD Amorphous Silicon," in *Mat. Res. Soc. Symp. Proc*., vol.106, p.305, 1998.

[10] C. L. Fan an M. C. Chen, "Performance Improvement of Excimer Laser Annealed Poly-Si TFTs Using Fluorine Ion Implantation," *Elctrochem, And Solid State Lett*., vol.5, G75, 2002.

[11] T. F. Chen, C. F. Yeh, and T. C. Lou, "Inverstigation of Grain Boundary Control in The Drain Junction on Laser-Crystalized Poly-Si Thin Film Transistors," *IEEE Electron Device Lett*., vol.24, p.457, 2003.

[12] S. Batra, K. Park, S. Banerjee, D. Kwong, A. Tasch, M. Rodder, "Rapid Thermal Hydrogen Passivation of Polysilicon MOSFETs," *IEEE Electron Device Lett*., vol.11, no.5, p.194,1990.

[13] M. Bonnel, N. Duhamel, T.Henrion, B. Loisel, and L. Haji, "Furance and Rapid Thermal Annealing for Polysilicon Thin Film Transistor- Influence of Channel Film Thickness," J. Electrochem. Soc., vol.10, 99.3584-3587, 1993.

[14] R. C. Cammarata, C. V. Thompson, C. Hayzelden, and K. N. Tu, *J. Mater. Res*., 5,2133,1990.

[15] C. Hayzelden and J. L. Batstone, " Silicide Formation and Silicide- Mediate Crystallization of Nickel- Implanted Amorphous Silicon Thin Film," *J. Appl. Phys*. Vol.73, p.8297, 1993.

[16] T. Sameshima," Status of Si Thin Film Transistors," *J.Non-Cryst. Solids*, Vol. 227-230, pp.1196-1201, 1998.

[17] H. Oshima and S. Morozumi, "Future trends for TFT integrated circuits on glass substrates," in *IEDM Tech. Dig.*, 1989, pp. 157–160.

[18] S. D. Brotherton, "Polycrystalline silicon thin-film transistors," *Semicond. Sci. Technol.*, vol. 10, pp. 721–738, 1995.

[19] G. Fossum, A. Ortiz-Conde, H. Shichijo, and S. K. Banerjee, “Anomalous leakage current in LPCVD polysilicon MOSFET’s,” *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1878–1885, 1985.

[20] S. D. Brotherton, J. R. Ayres, and M. J. Trainor, “Control and analysis of leakage currents in poly-Si thin-film transistors,” *J. Appl. Phys.*, vol.79, pp. 895–904, 1996.

[21] M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, “Floating body effects in polysilicon thin-film transistors,”*IEEE Trans. Electron Devices*, vol. 44, pp. 2234–2241, Dec. 1997.

[22] J. R. Ayres, S. D. Brotherton, D. J. McCulloch, and M. J. Trainor, “Analysis of drain field and hot carrier stability in polysilicon thin film transistors,” *Jpn. J. Appl. Phys.*, vol. 37, pp. 1801–1808, 1998.

[23] A. Valletta, L. Mariucci, G. Fortunato, S. D. Brotherton, and J. R. Ayres,“Hot carrier-induced degradation of gate overlapped lightly doped drain (GOLDD) polysilicon TFTs,” *IEEE Trans. Electron Devices*, vol. 49,pp. 636–642, Apr. 2002.

[24] H. G. Fossum, A. Oritz-Conde, H. Shichijo, and S. K. Banerjee, “Anormalous leakage current in LPCVD polysilicon MOSFET’s,” *IEEE Trans. Electron Devices*, vol. ED-32, no. , pp. 1878–1884, 1985.

[25] K. R. Olasupo and M. K. Hatalis, “Leakage current mechanism in submicron polysilicon thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1218–1223, Aug. 1996.

[26] C. A. Dimitriadis and M. Miyasaka, “Performance enhancement of offset gated polysilicon thin-film transistors,” *IEEE Electron Device Lett.*, vol. 21, pp. 584–586, May 2000.

[27] Z. Xiong, H. Liu, C. Zhu, and J. K. O. Sin, “A novel self-aligned offset-gated polysilicon TFT using high-k dielectric spacers,” *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 194–195, Apr. 2004.

[28] H.-C. Lin, C.-M. Yu, C.-Y. Lin, K.-L. Yeh, T.-Y. Huang, and T.-F. Lei, “A novel thin-film transistor with self-aligned field induced drain,” *IEEE Electron Device Lett.*, vol. 22, no. 1, pp. 26–28, Jan. 2001.

[29] C. W. Lin, C. H. Tseng, T. K. Chang, C. W. Lin, W. T. Wang, and H.C. Cheng, “A novel laser-processed self-aligned gate-overlapped LDD poly-Si TFT,” *IEEE Electron Device Lett.*, vol. 23, pp. 133–135, May 2002.

[30] K. R. Olasupo, W. Yarbrough, and M. K. Hatalis, “The effect of drain offset on current-voltage characteristics in sub micron polysilicon thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp.1306–1308, Aug. 1996.

[31] Joon-ha Park and O. Kim, “A Novel Self-Aligned Poly-Si TFT With Field-Induced Drain Formed by the Damascene Process,” *IEEE Trans. Electron Devices*, vol. 26, no.4, pp.249–251, Aug. 2005.

[32] J. G. Fossum, A. Ortiz-Conde, H. Shichijo, “Anomalous leakage current in LPCVD polysilicon MOSFET’s,” *IEEE Trans. Electron Devices,* vol. ED-32, pp. 1878–1884, Sept. 1985.

[33] S. K. Madan and D. A. Antoniadis, “Leakage current mechanisms in hydrogen-passivated fine-grain polysilicon silicon-on-insulator MOSFET’s,” *IEEE Trans. Electron Devices,* vol. ED-33, pp. 1518–1528, Oct. 1986.

[34] K. Y. Choi , J. W.Lee, M. K. Han, “Gate-overlapped lightly doped drain poly-Si thin-film transistors for large area-AMLCD,” *IEEE Trans. Electron Devices,* vol. 45, No.6, June. 1988.

[35] K. R. Olasupo, M. K. Hatalis, “Leakage current mechanism in sub-micron polysilicon thin-film transistors,” *IEEE Trans. Electron Devices,* vol. 43, No.8, August. 1996.

[36] M. Yazaki, S. Takenaka, “Conduction mechanism of leakage current observed metal-oxide-semiconductor transistors and poly-Si thin-film transistors,” *Jpn .J. Appl. Phy,* vol. 31, pp. 206–209, Part 1, No. 2A, Feb. 1992.

[37] C. F. Yeh, S. S. Lin, "Performance and off-state current mechanisms of low-temperature processed polysilicon thin-film transistors with liquid phase deposited SiO_2 gate insulator," *IEEE Trans. Electron Devices,* vol. 44, pp. 173–178, Feb. 1994.

[38] M.Valdinoci, G. Baccarani and L. Colalondo, "Floating body effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices,* vol. 44, No.12, Dec. 1997.

[39] M. Hack, and A. G. Lewis, "Avalanche-induced effects in polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 203-205, 1991.

[40] A. G. Chynoweth, "Ionization rates for electrons and holes in silicon," *Phy. Rev.,* vol. 109, pp.1537–1540, 1958.

[41] J. P. Colinge, "Reduction of floating-substrate effects in thin-film SOI MOSFET's," *Electron Lett.*, vol. 22, pp. 187-188, 1986.

[42] S. Zhang, C. Zhu and Johnny K. O. Sin, "Ultra- thin elevated channel poly-Si TFT technology for fully-integrated AMLCD sysrem on glass," *IEEE Trans. Electron Devices,* vol. 47, No. 3, Mar. 2000.

[43] P. S. Shih, H. W. Zan , "Dimensional effects on the drain current of N- and P-channel polycrystalline Silicon thin-film transistors," *Jpn .J. Appl. Phy,* vol. 39, pp. 3879-3882, Part 1, No. 7A, July. 2000.

[44] J. R. Ayres, S. D. Brotherton, "Analysis of drain field and hot carrier stability of poly-Si thin-film transistors," *Jpn .J. Appl. Phy,* vol. 37, pp.1801–1808, Part 1, No. 4A, Apr. 1998.

簡歷

姓名：謝佩珊

性別：女

生日：03/28/1982

籍貫：台灣省 台中縣

學歷：國立交通大學電子物理研究所碩士班

論文題目：

新穎堆疊矽/鍺 **T** 型閘極複晶矽薄膜電晶體

A Novel Poly-Silicon Thin-Film Transistors with Stacked Si/Ge T-Gate

指導教授：趙天生博士