國 立 交 通 大 學

電子物理學系

碩士論文

n 型通道與 p 型通道完全鎳自我對準矽化源/汲與閘極複晶矽薄膜電晶體之研究

n-Channel and p-Channel Poly-Silicon Thin-Film Transistors With Fully Ni-Salicided S/D and Gate Structure

研 究 生：黃彥學

指導教授：趙天生 博士

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研 究 生：黃彥學　　Student：Yan-Syue Huang

指導教授：趙天生 博士　　Advisor：Tien-Sheng Chao

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學生： 黃彥學　　　　　指導教授： 趙天生 博士

國 立 交 通 大 學

電子物理學系 電子物理研究所碩士班

摘 要

在先進互補式金氧半導體元件裡，當接觸尺寸縮小至奈米等級，源極及汲極的接觸電阻也會隨之增加。因此，金屬矽化物的技術應用在源極及汲極已經被開發用來同時降低接觸電阻及接面寄生電阻。所以，具有與矽基材完好介面特性的金屬矽化物是元件製程的重要考量。相同的問題也會發生在多晶矽薄膜電晶體上，超薄的多晶矽薄膜電晶體限制了元件的驅動電流。然而，為了減少多晶矽薄膜電晶體的寄生電阻，在很多研究裡採用了完全鎳自我對準矽化反應去解決這個問題。

近幾年來，完全矽化鎳閘極被廣泛地研究來取代金屬閘極，金屬矽化鎳閘極具有低電阻率、消除多晶矽閘極空乏現象、可調變的功函數以及整合容易等優點。同樣地，完全矽化鎳源/汲極也被廣泛地應用來減少接觸電阻以及接面寄生阻值。此外，就電阻而言，矽化鎳(NiSi)的片電阻是跟二矽化鈦($TiSi_2$)和二矽化鈷($CoSi_2$)差不多的。然而，鎳金屬矽化物沒有窄線寬效應(narrow line effect)，且鎳金屬矽化物可以在低溫(400~600℃)時形成而不會有結塊效應(agglomeration effect)。還有在矽化鎳的形成過程當中，它消耗較少的矽，所以它可以形成較淺的接面。這些都是鎳金屬材料所具有的優點。

在本論文研究中，N型和P型的完全鎳自我對準矽化源/汲與閘極多晶矽薄膜電晶體(FSA-TFTs)已經被成功地製造出來。另外，為了和完全鎳自我對準矽化源/汲與閘極多晶矽薄膜電晶體比較，我們也特地製造了局部鎳自我對準矽化源/汲與閘極多晶矽薄膜電晶體(partially salicided TFTs)。特別地，在此研究裡我們也去比較了金屬快速熱製程溫度與時間對元件特性的影響。由完全鎳自我對準矽化多晶矽薄膜電晶體和局部鎳自我對準矽化多晶矽薄膜電晶體以及傳統的多晶矽薄膜電晶體比較，完全鎳自我對準矽化多晶矽薄膜電晶體有較好的特性。其原因為有較小的源/汲極與閘極片電阻以及減少的寄生阻值，且能夠有效的鈍化矽基材裡的缺陷。而且, 它可以有效地抑制浮接基體效應(floating-body effect)和寄生雙極性接面電晶體效應(parasitic bipolar junction transistor action)。因此，我們從實驗結果發現，完全鎳自我對準矽化多晶矽薄膜電晶體能夠得到較高的驅動電流、較低的漏電流、較好的次臨界特性、較少的臨界電壓變化量和較大的場效遷移率等。所以，完全鎳自我對準矽化多晶矽薄膜電晶體的特性適合用在需要穩定的臨界電壓和大的崩潰電壓。

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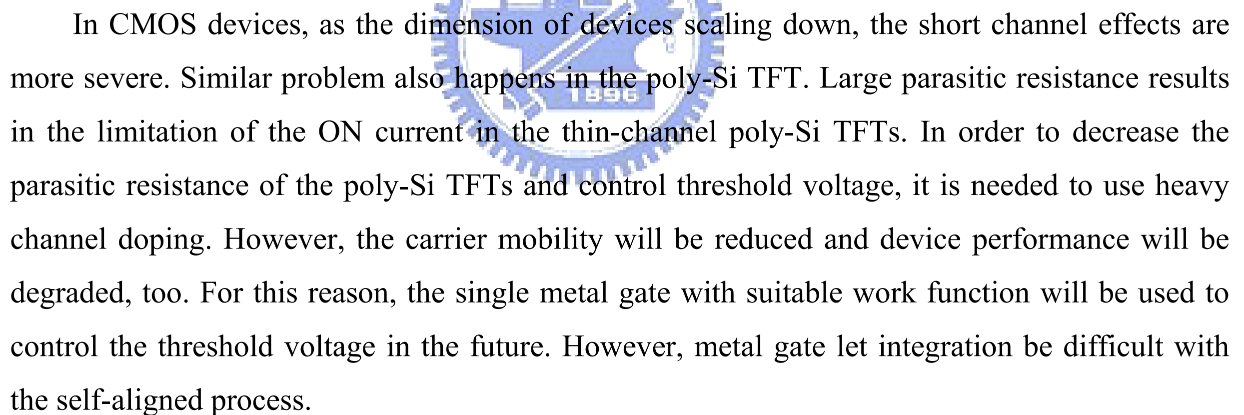
Student: Yan-Syue Huang **Advisor: Dr. Tien-Sheng Chao**

Department of Electrophysics
National Chiao Tung University

ABSTRACT



In CMOS devices, as the dimension of devices scaling down, the short channel effects are more severe. Similar problem also happens in the poly-Si TFT. Large parasitic resistance results in the limitation of the ON current in the thin-channel poly-Si TFTs. In order to decrease the parasitic resistance of the poly-Si TFTs and control threshold voltage, it is needed to use heavy channel doping. However, the carrier mobility will be reduced and device performance will be degraded, too. For this reason, the single metal gate with suitable work function will be used to control the threshold voltage in the future. However, metal gate let integration be difficult with the self-aligned process.

Recently, the **fu**ll **si**licide (FUSI) NiSi is investigated as an alternative metal-gate. The fully Ni-salicided gate structure has several advantages, such as low resistivity, elimination of poly depletion effect, tunable work function, and better process compatibility. Moreover, Ni-salicided S/D structure can drastically decrease the parasitic resistance and passivate the defects of S/D junction. In addition, the sheet resistivity of NiSi is comparable with that of $TiSi_2$ and $CoSi_2$, and NiSi does not have narrow line effect, and NiSi can be accomplished at low temperature (400~600℃) without agglomeration effect. During the formation of NiSi, it is the less silicon consumption. So it can form shallower junction.

In this thesis, n-channel and p-channel poly-Si thin-film transistors (FSA-TFTs) with fully Ni self-aligned silicided (fully Ni-salicided) source/drain and gate structure have been successfully fabricated. In addition, we also fabricate partially Ni-salicided S/D and gate in order to compare with FSA-TFTs. Specially, we also investigated the influence of RTA temperature and time in this study. The FSA-TFTs exhibit the best electrical characteristics because of FSA-TFTs have small S/D and gate sheet resistance and low parasitic resistance. Moreover, FSA-TFTs can effectively suppress the floating-body effect and parasitic bipolar junction transistor action compared with conventional TFTs. Experimental results show that the FSA-TFTs give higher on-state current, lower off-state leakage current, improved subthreshold characteristics, less threshold voltage variation, and larger field-effect mobility compared with control TFTs. The characteristics of the FSA-TFTs are suitable for high performance driving TFTs with a stable threshold voltage and large breakdown voltage.

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光陰似箭，歲月如梭。這兩年來的碩士生活終將隨著此論文的完成而畫上句點，同時也將為我長久的求學生涯畫上一個短暫的休止符。回想在研究生的求學過程當中，受到了許多人的幫忙才得以完成此論文，本人在此僅以簡短的言語來表達我心中無限的感激。首先，我要感謝指導教授趙天生老師，老師不論是在課業上或著待人處事上都給予了我相當多的鼓勵與指導，而老師的諄諄教誨，學生也將永記心中，更會珍惜這段難得的師生緣分。

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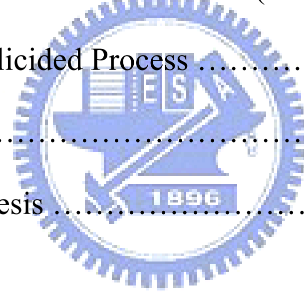

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Fig.3-47 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/10μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

Fig.3-48 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/10μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

Fig.3-49 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/0.8μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

Fig.3-50 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/0.8μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

Fig.3-51 Transfer characteristics of p-channel FSA-TFTs with undoped gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

Fig.3-52 Transfer characteristics of p-channel FSA-TFTs with undoped gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

Fig.3-53 Field-effect mobility of p-channel FSA-TFTs with undoped gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

Fig.3-54 Field-effect mobility of p-channel FSA-TFTs with undoped gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by

RTA 500°C for 60 seconds.

Fig.3-55 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for p-channel FSA-TFTs with undoped gate. Ni-salicide was formed by RTA 500°C for 60 seconds.

Fig.3-56 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for p-channel conventional TFTs.

Fig.3-57 Comparison of threshold voltage roll-off between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W=10μm, and V_D=0.5V.

Fig.3-58 Comparison of subthreshold swing roll-off between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W=10μm, and V_D=0.5V.

Fig.3-59 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/10μm, and V_G-V_{TH}=-5.0V, -6.0V, -7.0V, -8.0V, -9.0V.

Fig.3-60 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/10μm, and V_G-V_{TH}=-2.0V, -3.0V, -4.0V, -5.0V, -6.0V.

Fig.3-61 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_G-V_{TH}=-5.0V, -5.5V, -6.0V, -6.5V, -7.0V.

Fig.3-62 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_G-V_{TH}=-3.5V, -4.0V, -4.5V, -5.0V, -5.5V.

Fig.3-63 Parasitic resistance R_P is extracted by plotting the on-state resistance (R_{on}) versus gate length. FSA-TFTs with undoped gate and Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage is 0.5V.

Fig.3-64 Parasitic resistance R_P of conventional TFTs is extracted by plotting the on-state resistance (R_{on}) versus gate length. The channel width is 10μm, and the drain voltage is 0.5V.

Fig.3-65 Comparison of the On/Off current ratio between p-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. The I_{ON} is measured at V_G=15V and V_D=3.0V. I_{OFF} is equal to minimum current at V_D=3.0V. Ni-salicide was formed

by RTA 500°C for 60 seconds. The channel width is 10μm.

Fig.3-66 The floating-body effect in Poly-Si TFTs.

Chapter 4

Fig.4-1 (a) Si/Ge stack gate without Ni-salicied process and (b) Si/Ge stack gate with Ni-salicied process.

Fig.4-2 (a) Si/Ge T-gate without Ni-salicied process and (b) Si/Ge T-gate with Ni-salicied process.

Chapter 1

Introduction

1.1 Overview of Poly-Si Thin-Film Transistors

In 1966, C. H. Fa *et al.* fabricated the first polycrystalline silicon thin film transistors (Poly-Si TFTs) [1]. So far, thin-film transistors have been widely used in static random access memories (SRAM) [2], electrical erasable programming read only memories (EEPROMs) [3], linear image sensors [4], thermal printer heads [5], photodetector amplifier [6], scanner [7], and active matrix liquid crystal displays (AMLCDs) [8]-[10], etc. Within these applications, the application of AMLCDs is the major driving force to promote the developments of poly-Si TFTs technology.

It is known that the pixel switching device of AMLCDs rely on α-Si:H TFTs. However, due to their low electron mobility (≤ 1 cm^2/Vs), it is hard to realize the integration of the switching pixels with the peripheral driver circuits in one signal substrate to further reduce the production cost of AMLCDs. Recently, poly-Si TFTs have attracted much attention, because the field effect mobility in poly-Si is significantly higher than that in α-Si, thus higher driving current can be achieved in poly-Si [11]. The high driving current of poly-Si TFTs makes the integration of switching pixels and driver circuits possible. Moreover, the aperture ratio and the panel brightness can be also greatly promoted due to small device size needed using poly-Si TFTs. So, the performance of display can be significantly improved. As a result, poly-Si TFTs have a great potential to realize high performance large area AMLCDs applications, and further to accomplish System-on-Panel (SOP).

But it is important to note that poly-Si TFTs have larger leakage current compared with α-Si:H TFTs, therefore how to obtain a good quality polycrystalline Si film with higher carrier mobility, lower leakage current with excellent reliability has become a major concern

for the poly-Si thin film transistors fabrication. The conduction mechanism and the performance of poly-Si TFTs are strongly related to grain boundaries and intra-grain defects. In order to obtain desirable electrical characteristics of poly-Si TFTs, several methods have been proposed to improve the device performance by enlarging the grain size of poly-Si films [12] and reducing the trap states in grain boundaries. It has been reported that the α-Si films can be crystallized by several techniques, such as solid phase crystallization (SPC) [13], laser annealing crystallization [14], metal induced crystallization (MIC) [15], and metal-induced lateral crystallization (MILC) [16] to obtain a large grain size of poly-Si to raise the field effect mobility. Additionally, there are other methods such as H_2 [17], NH_3 [18], N_2O [19] and O_2 plasmas [20] plasma treatments to passivate the defects in the channel or narrowing the channel width to reduce the trap state density have been intensely investigated to accomplish this goal.

Finally, novel structure design is another approach to fabricate high-performance poly-Si TFTs. This technique focuses on the reduction of the electric field near the drain junction, and thus suppresses the device’s off-state leakage current. Many structures including multiple channel structures [21], offset drain/source [22]-[23], lightly doped drain (LDD) [24], gate-overlapped LDD [25], field induced drain [26] and vertical channel [27] have been proposed and investigated intensively. [28]

1.2 Brief Introduction of Silicided Process

In the ultra-thin film silicon on insulator metal oxide field effect transistors (SOI MOSFETs), large parasitic resistance degrades device performances. Similar problem also happens in the poly-Si TFTs. However, in order to decrease the parasitic resistance of the poly-Si TFTs, the self-aligned silicided (salicided) source/drain (S/D) is a technology to solve this problem. Moreover, the fully silicided gate has some advantages. For example, the fully silicided gate does not have poly depletion effect (PDE) compared with the poly-Si gate, and the work function of the silicided gate can be tuned by doping the poly-Si with different

dopants and dosages. In addition, sputtering damage may occur when metal is deposited on the gate dielectrics, therefore the silicided gate technology can avoid this problem.

Recently, the material of the fully salicide includes $TiSi_2$ [29], $CoSi_2$ [30], NiSi [31], HfSi [32], PdSi [33] and so on. Among the metal silicides, $TiSi_2$, $CoSi_2$, and NiSi were widely used in the silicided process. Because $TiSi_2$ has a low sheet resistance (13~15Ω/□) and better thermal stability, it is widely used in the IC industry. But $TiSi_2$ has the narrow lines effect, and Ti may react with implanted dopants to form compounds such as Ti-B and Ti-As [34], and the processing temperature window of $TiSi_2$ is relatively narrow due to the high temperature requirement for the high resistivity C49 to low resistivity C54 phase transition and the silicide agglomeration temperature limit [35]. In addition, the creep-up phenomenon during the formation of $TiSi_2$ silicide may form a bridge between the gate and source/drain regions to cause device failure. Subsequently, $CoSi_2$ is an attractive replacement of $TiSi_2$ due to its relatively linewidth independent sheet resistance [36]. The formation of $CoSi_2$ does not need phase transformation, so it can be extensively used in the narrow line. Moreover, Co does not react with implanted dopants. However, the formation of the $CoSi_2$ will consume more Si than the formation of the $TiSi_2$. It will result in a deeply junction and also a large junction leakage current.

Unlike $TiSi_2$ and $CoSi_2$, Nickel monosilicide (NiSi) has been recognized as a promising candidate for a contact metal in the future ULSI salicide application [37]. Regarding the sheet resistance, NiSi has a low resistive phase with an electrical resistivity of 14-20 $\mu\Omega$-cm which is comparable to those of $TiSi_2$ and $CoSi_2$, and no creep-up phenomenon. Moreover, NiSi process also offers a number of benefits. First, silicidation can be formed at low temperature (400~600°C) without agglomeration. Second, nickel is not reacted with implanted dopants. Finally, during the silicided process, NiSi has the less silicon consumption compared with $TiSi_2$ and $CoSi_2$. Hence, NiSi can form the shallower junction. [38]-[39]

1.3 Motivation

In the n-channel ultra-thin film Poly-Si TFTs, the output characteristics exhibit an anomalous increase of current in the saturation regime, often called the “kink” effect because of an analogy with silicon-on insulator (SOI) devices. This phenomenon can be attributed to the floating-body effect and the avalanche multiplication enhanced by grain boundary traps. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return [40]. In addition, both the n-channel and p-channel ultra-thin film Poly-Si TFTs have large parasitic resistance degrades device performance. So, in order to suppress the floating-body effect and decrease the parasitic resistance of the Poly-Si TFTs, the self-aligned silicided (salicided) process is a technology to solve this problem.

In this thesis, we carried out the n-channel fully Ni-salicided source/drain (S/D) and gate Poly-Si TFTs with different gate implant dosages, including un-doped gate and in-situ gate. Furthermore, the n-channel partially Ni-salicided S/D and gate Poly-Si TFTs with in-situ doped gate as well as the p-channel fully Ni-salicided S/D and gate Poly-Si TFTs with un-doped gate have also been fabricated. Mainly, in addition to show suppressed floating body effect, we want to discuss the influence of the different metal RTA temperature and time, and difference between fully and partially Ni-salicided S/D and gate for n-channel Poly-Si TFTs as well. Moreover, we hope to increase the driving current of device, decrease the gate and S/D parasitic and have high gate capacitance capability compared with conventional devices, therefore fully Ni-salicided S/D and gate Poly-Si TFTs (FSA-TFTs) will show higher mobility, stable V_{TH}, alleviated V_{TH} roll-off, improved subthreshold swing, increased breakdown voltage, and increased ON/OFF current ratio for n-channel and p-channel Poly-Si TFTs.

Thus, the performances of FSA-TFTs are expected to have a better performances than conventional Poly-Si TFTs.

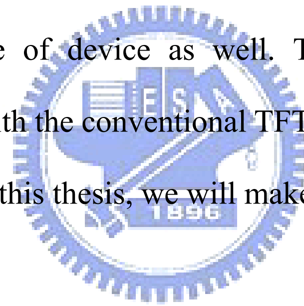
1.4 Organization of The Thesis

In this section, we will show our research efforts. This thesis is organized as follow:

In chapter 1, the overview of Poly-Si TFTs, the brief introduction of silicided process, and motivation in this thesis are described.

In chapter 2, experimental process flows, and electrical parameter extraction are shown.

In chapter 3, for n-channel Poly-Si TFTs, we will show Ni salicided process can decrease parasitic resistance, passivate defects, and suppress floating body effect to obtain the better performances of device. Moreover, the performances of FSA-TFTs with in-situ doped gate and FSA-TFTs with un-doped gate are compared with the conventional TFTs. In addition, we discuss the influence of the different RTA temperature and time, and difference between fully and partially Ni-salicided S/D and gate at the same time. For p-channel Poly-Si TFTs, we will show Ni salicide process can decrease parasitic resistance evidently and passivate defects to obtain the better performance of device as well. The performances of FSA-TFTs with un-doped gate are compared with the conventional TFTs.



In chapter 4, at the end of this thesis, we will make conclusions and future works.

Chapter 2

Experimental Process and Electrical Parameters Extraction

2.1 Fabrication of Poly-Si Thin-Film Transistors (Poly-Si TFTs)

In this section, the process flows of poly-Si thin-film transistors are described, including the process flows of the fully Ni self-aligned silicided TFTs (FSA-TFTs) and the conventional TFTs.

2.1.1 Fabrication of the FSA-TFTs

The process flows of devices are showed in Fig.2-1. First, a 550-nm thick oxide was deposited on the 6-in wafers. Then, a 50-nm thick amorphous-Si (a-Si) layer was deposited as the active layer in a LPCVD system using SiH_4 as source at 550°C. Next, the a-Si was crystallized to poly-Si by solid phase crystallization (SPC) process at 600°C for 24 hours. After the wafers were subjected to photolithography for active region definition, a 50-nm thick tetraethoxysilane (TEOS) gate dielectric layer, a 50-nm a-Si layer were deposited, and nitride was deposited by LPCVD as hard mask. The a-Si gate layers were divided into in-situ n+ phosphorus doped gate or un-doped gate. After patterning of the gate electrode, the nitride layer and the a-Si layer were etched by the oxide dry etcher (TEL-5000) and poly-Si dry etcher (TCP-9400), respectively. Then the gate oxide was removed by HF-dip. Subsequently, a self-aligned ion implantation was used to form n+ S/D with phosphorous (p^+) at 20 keV to a does of 5×10^{15} cm^{-2}, and p+ S/D with BF_2^+ at 25 KeV to a dose 5×10^{15} cm^{-2}. Dopants were activated in a furnace at 600^oC for 12 hours. Next, the TEOS oxide was deposited and etched to form the sidewall spacer. Then, the Si_3N_4 hard-mask layer was selectively etched by a hot phosphoric acid (H_3PO_4). After a HF-dip for 10-sec, a 40-nm thick Ni and a 10-nm thick TiN were deposited on the wafer by Metal-PVD, and then the fully Ni-salicided S/D and gate was carried out at 500°C for 30 seconds or 500°C for 60 seconds by one-step rapid thermal

annealing (RTA) in the N_2 ambient. Finally, the unreacted TiN and Ni were selectively removed by sulfuric acid (H_2SO_4). Before measurement, an NH_3 plasma treatment was performed to passivate the crystalline defects.

2.1.2 Fabrication of Conventional TFTs

In addition to the fabrication of FSA-TFTs, conventional TFTs were fabricated as the control ones. The structure of conventional TFT is showed in Fig.2-2. First, a 550-nm thick oxide was deposited on the 6-in wafers. Then, a 50-nm thick a-Si layer was deposited as active layer in a LPCVD system. Next, the a-Si was crystallized to poly-Si by SPC process at 600°C for 24 hours. Then, the wafers were subjected to photolithography for active region definition. After a 50-nm thick TEOS oxide layer, one of the two wafers was deposited a 200-nm in-situ doped a-Si layer in a vertical furnace as n+ gate, the other was deposited a 200-nm a-Si layer in LPCVD system and then it was ion implanted by Boron (B^+) at 25 keV to a dose 5×10^{15} cm^{-2} as p+ gate. Next, after gate patterning, gate dielectric layer on S/D region was removed by HF-dip. Subsequently, a self-aligned ion implantation was used to form n+ S/D with phosphorous (p^+) at 20 keV to a does of 5×10^{15} cm^{-2}, and p+ S/D with BF_2^+ at 25 keV to a dose 5×10^{15} cm^{-2}. Dopants were activated in a furnace at $600^{\circ}C$ for 12 hours. Then, 300-nm passivation oxide was deposited by PECVD and patterned for contact holes opening. Finally, a 500-nm thick Al was immediately thermal evaporated, followed by lithography for Al pad pattern definition. Before measurement, an NH_3 plasma treatment was performed to passivate the crystalline defects.

2.2 Electrical Parameters Extraction

In this section, all the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer. Moreover, the methods of parameter extraction used in this study are described. These parameters include threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), subthreshold swing (S.S.), parasitic resistance (R_P),

ON current (I_{ON}), OFF current (I_{OFF}), ON/OFF current ratio (I_{ON}/I_{OFF}).

2.2.1 Threshold Voltage (V_{TH})

The threshold voltage V_{TH} is an important parameter required for the channel length-width and series resistance measurements. However, V_{TH} is not unique defined. Various definitions exist and the reason for this can be found in the I_D-V_G curves. One of the most common threshold voltage measurement technique is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of 50~100 mV typically to ensure operation in the linear MOSFET region [41].

However, in this thesis, the threshold voltage is defined at a low drain voltage of 0.5V, and a fixed drain current I_D=I_{DN}×(W/L) where I_{DN} is a normalized drain current. Here, I_{DN} is 100 nA for n-channel and 10nA for p-channel.

2.2.2 Field Effect Mobility (μ_{FE})

Usually, field effect mobility (μ_{FE}) is determined from the maximum value of transconductance (g_m) at low drain bias. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{TH}$) can be approximated as the following equation:

$$I_{DS} = \mu_{FE} C_{OX} (\frac{W}{L})[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2] \quad \text{.................. (Eq.2.1)}$$

where W is the channel width, L is the channel length, V_{TH} is the threshold voltage, C_{ox} is the gate oxide capacitance per unit area. Thus, g_m is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_{OX} (\frac{W}{L}) V_{DS} \quad \text{.................. (Eq.2.2)}$$

Therefore, the field-effect mobility is

$$\mu_{FE} = \frac{L}{C_{OX} W V_{DS}} g_{m(\max)} \quad \text{.................. (Eq.2.3)}$$

2.2.3 Subthreshold Swing (S.S.)

The drain current in the saturation region ($V_{DS} > V_{GS} - V_{TH}$) is expressed as the following

equation:

$$I_{DS} = \frac{1}{2}\mu_{FE}C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad \text{.................. (Eq.2.4)}$$

It appears that the current abruptly vanishes while V_G is reduced to zero from the equation. In reality, there is still some drain conduction current below threshold, and this is known as the subthreshold conduction. This current is due to the weak inversion in the channel between flat-band and threshold, which leads to a diffusion current from source to drain. The subthreshold swing (S.S.) is defined as the reciprocal of slope of the I_D-V_G curve in weak inversion region. It is the amount of gate voltage required to increase/ decrease drain current by one order of magnitude. It is a typical parameter to describe the control ability of gate toward channel. [38]

In this thesis, the subthreshold swing is defined as one-third of the gate voltage required decreasing the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.2.4 Parasitic Resistance (R_P)

The device parasitic resistances are extracted from their output characteristics. It is known that when devices are operated under low drain voltage and high gate voltage their measured resistance (R_m) can be expressed as

$$R_m = R_{ch} + R_P = \frac{L - \Delta L}{W_{eff}\mu_{eff}C_{ox}(V_{GS} - V_T)} + R_P \quad \text{.................. (Eq.2.5)}$$

where R_{ch} and R_p represent channel resistance and parasitic resistance. C_{OX} is the gate dielectric capacitance per unit area, and W, L, V_{TH} are device channel width, length and threshold voltage, respectively. The parasitic resistance R_p can be extracted by plotting R_m versus L for varying gate voltages. [42]

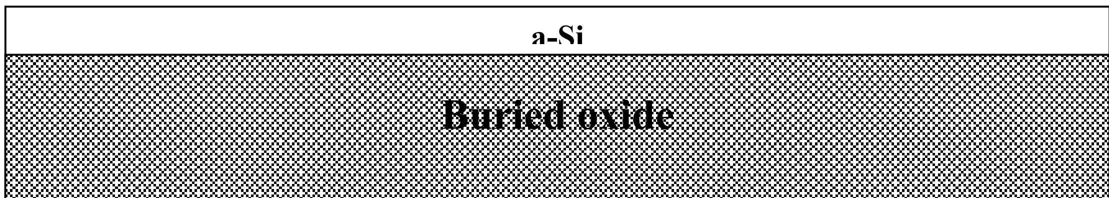
2.2.5 ON/OFF Current Ratio

A poly-Si TFT with good characteristics should have not only high ON state driving current but also low OFF state leakage current. For pixel transistors, the OFF state is

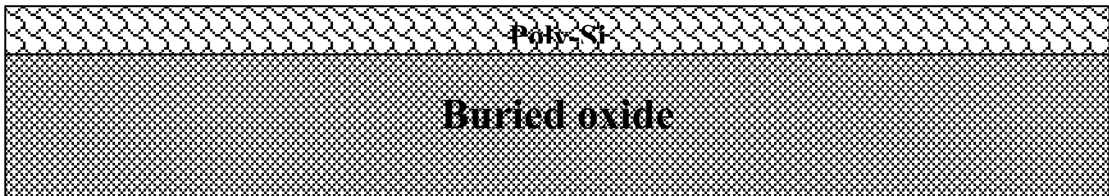
frequently encountered in normal operation. Therefore, ON/OFF current ratio is obviously a better evaluation parameter compared with ON state current alone. The leakage current mechanism in poly-Si TFTs is not like that in MOSFETs. In MOSFETs, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly crystalline Si. A large amount of trap densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current due to the tunneling effect is much larger in poly-Si TFTs than that in MOSFETs. Considering large negative gate bias V_G is applied, a hole-channel forms under the gate. In principle, little current flows because the junction between the hole-channel and the drain is reverse-biased. However, due to the existing numerous trap states in the polysilicon film and the large electric field, electron and hole emission from trap states becomes a strongly increasing function of electric field. Here, a trap could be modeled by a potential well. For large electric fields, it is possible for electrons to escape the potential well by quantum mechanical tunneling. The tunneling rate increases strongly with electric field because the barrier thickness decreases. The effect is a rapid increase in leakage current. The tunneling rate depends upon the total electric field, and consequently the leakage current is highest when both drain and gate voltages are large. [38]

In this thesis, the ON current is defined as the drain voltage is 3V, and the drain current when gate voltage equals to 10 V for n-channel and gate voltage equals to 15 V for p-channel. The OFF current is specified as the minimum current when drain voltage equals to 3 V.

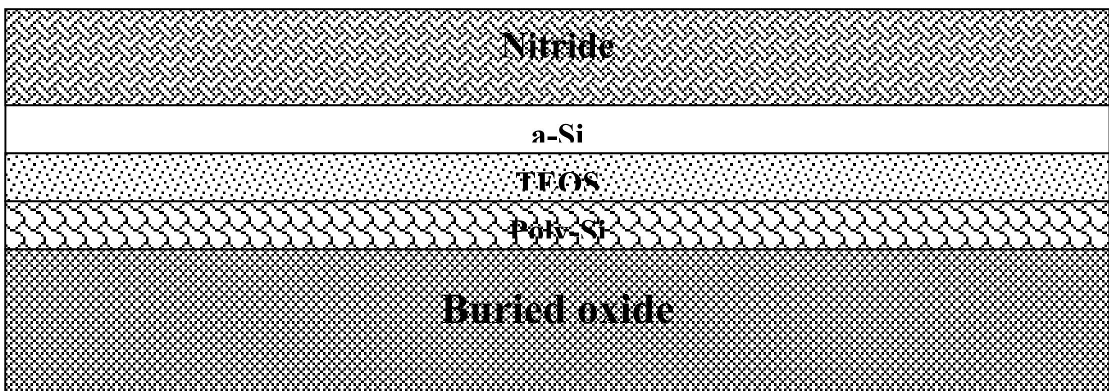
$$\frac{I_{ON}}{I_{OFF}} = \frac{\text{Current of } I_{DS} \text{ - } V_{GS} \text{ Plot at } V_{DS} = 3V,\ V_{GS} = 10V \text{ or } 15V}{\text{Minimum Current of Plot at } V_{DS} = 3V} \quad \text{..................} \quad \text{(Eq.2.6)}$$



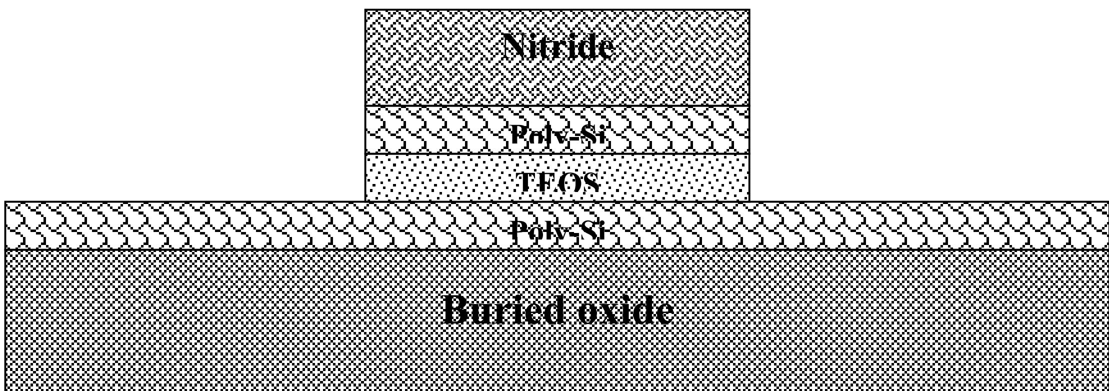
(1) 550-nm thick buried oxide and 50-nm thick a-Si were deposited.



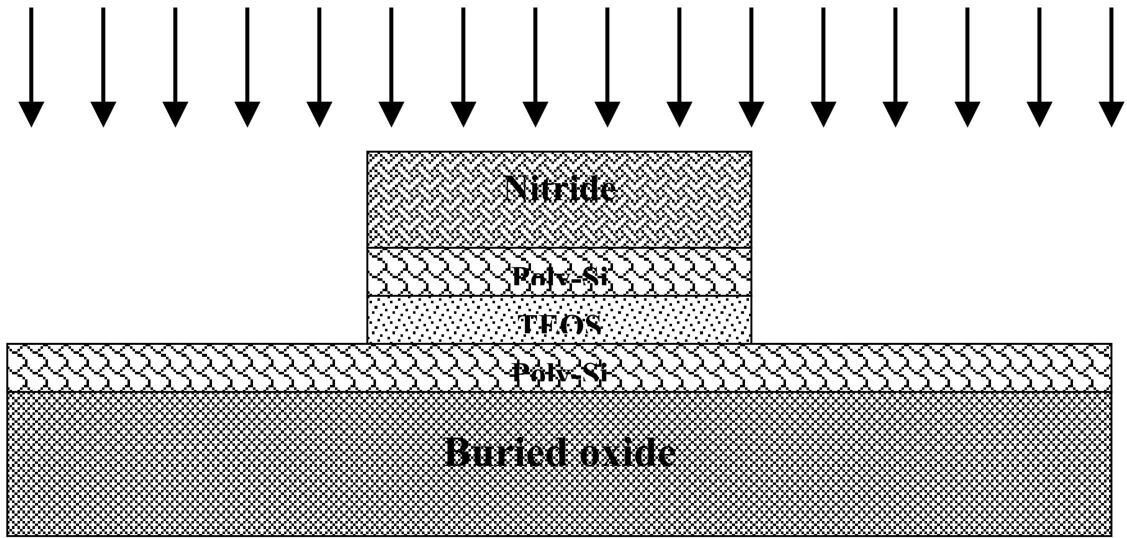
(2) 600°C annealing for 24-hr and active region definition.



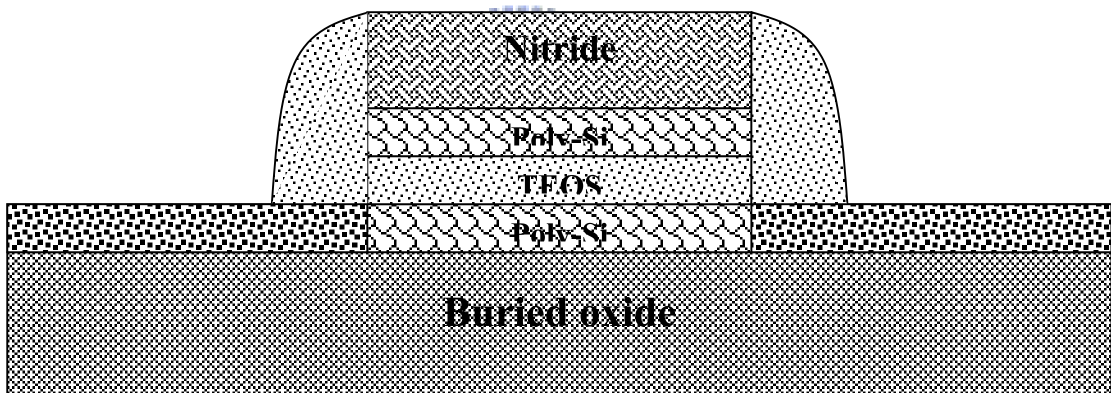
(3) 50-nm thick TEOS oxide, 50-nm thick a-Si and 100-nm thick nitride layer.



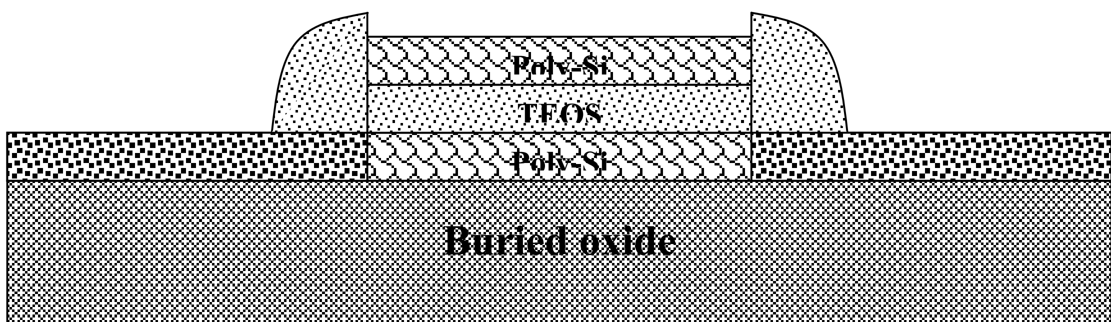
(4) Gate definition.



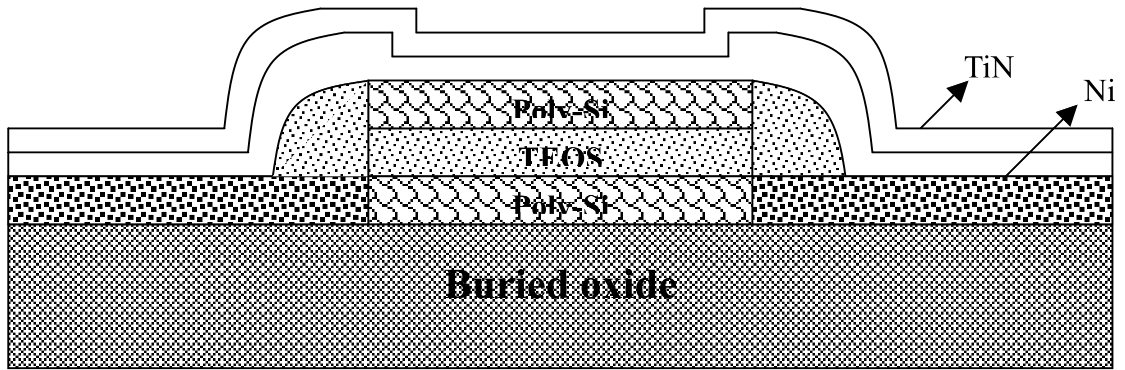
(5) phosphorous implantation for n-channel and BF_2^+ implantation for p-channel.



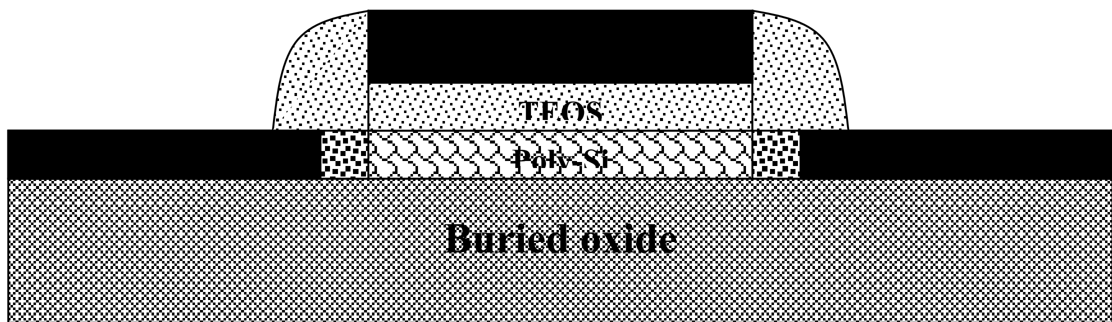
(6) TEOS spacer formation.



(7) Nitride layer was etched by H_3PO_4.



(8) Ni and TiN deposition.



(9) Ni-salicide formation by RTA 500°C.

Fig.2-1 Process flows of fully Ni-salicided TFTs.

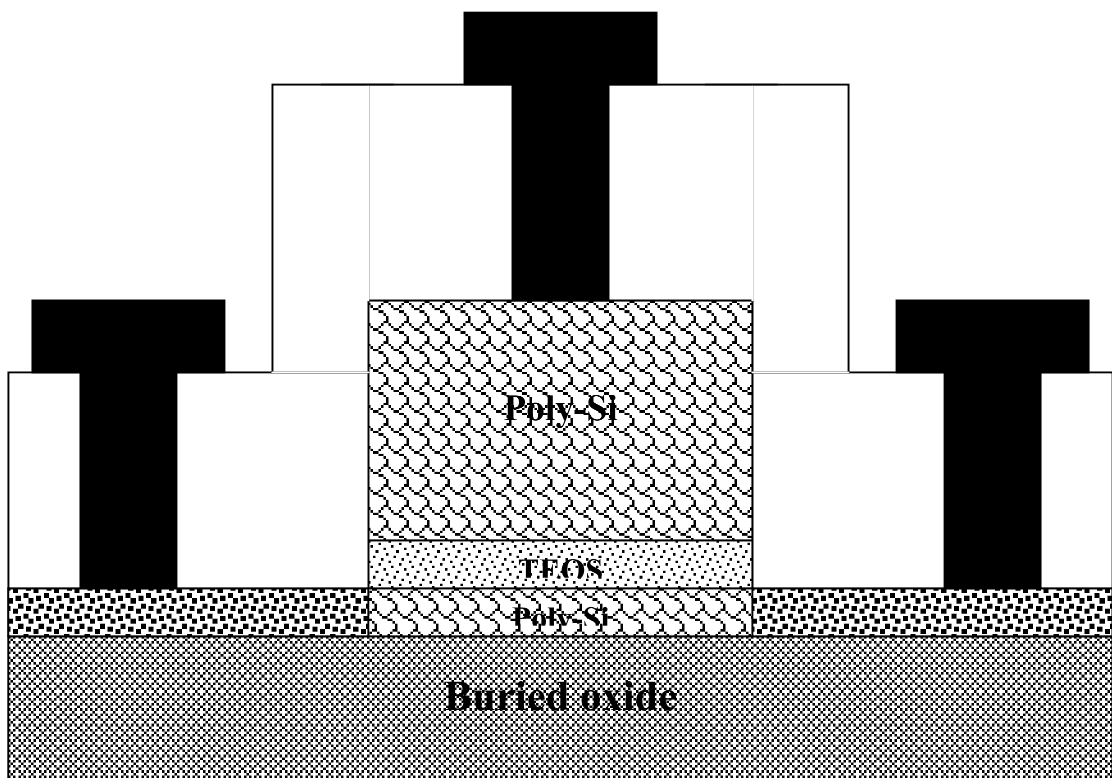


Fig.2-2 The Structure of Conventional TFT.

Chapter 3

Electrical Characteristics and Discussion of the n-Channel and the p-Channel FSA-TFTs

In this chapter, we will show electrical characteristics as well as discuss physical meaning for n-channel and p-channel. At first, the TEM photograph for cross-section of FSA-TFTs is shown in Fig.3-1 and the TEM photograph for cross-section of Source/Drain (S/D) junction is shown in Fig.3-2. Subsequently, basic characteristics of n-channel and p-channel are shown in session 3.1 and 3.3, respectively. Moreover, differences between fully-salicided and partially salicided n-channel TFTs with in-situ poly-Si gate are shown in session 3.2. Device parameters including threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), subthreshold swing (S.S.), parasitic resistance (R_P), and ON/OFF current ratio are all extracted. These methods of extraction have been explained in session 2.2. Finally, we found that poly-Si TFTs with fully Ni-salicided S/D and gate structure for n-channel and p-channel have better electrical characteristics such as higher ON current, lower leakage current, stable V_{TH}, higher field-effect mobility, alleviated V_{TH} roll-off, improved subthreshold swing, increased breakdown voltage, and increased ON/OFF current ratio, etc.

3.1 Basic Characteristics of n-Channel FAS-TFTs with Undoped and In-situ Poly- Si Gate

In this section, we will explain the basic characteristics of n-channel FSA-TFTs. At first, the transfer characteristics of FSA-TFTs with undoped gate, in-situ gate, and conventional TFTs are compared in session 3.1.1. In addition, the output characteristics of FSA-TFTs with undoped gate, in-situ gate, and conventional TFTs are compared in 3.1.2. The floating-body effect of FSA-TFTs with undoped gate, in-situ gate, and conventional TFTs are compared in

3.1.3. The influence of metal RTA temperature and time for FSA-TFTs with undoped and in-situ poly-Si gate are compared in 3.1.4. The parasitic resistance of FSA-TFTs with undoped gate, in-situ gate, and conventional TFTs are compared in 3.1.5. Finally, the ON/OFF current ratio of FSA-TFTs with undoped gate, in-situ gate, and conventional TFTs are compared in 3.1.6.

3.1.1 Transfer Characteristics

Fig.3-3 and Fig.3-4 show the I_D-V_G transfer characteristics of conventional TFTs with W/L=10μm/10μm and W/L=10μm/0.8μm, respectively. Moreover, these figures show two different treatment steps for n-channel. Obviously, conventional TFTs with NH_3 plasma treatment have better subthreshold swing, and higher ON/OFF current ratio. In addition, they have more stable V_{TH} than conventional TFTs without NH_3 plasma treatment.

Fig.3-5 and Fig.3-6 show the I_D-V_G transfer characteristics of FSA-TFTs with undoped gate, and W/L=10μm/10μm with different metal RTA at 500°C for 30 seconds and 60 seconds, respectively. Fig.3-7 and Fig.3-8 show the I_D-V_G transfer characteristics of FSA-TFTs with undoped gate, and W/L=10μm/0.8μm with different metal RTA at 500°C for 30 seconds and 60 seconds, respectively. In addition, Fig.3-9 and Fig.3-10 show the I_D-V_G transfer characteristics of FSA-TFTs with in-situ gate, and W/L=10μm/10μm with different metal RTA at RTA 500°C for 30 seconds and 60 seconds, respectively. Fig.3-11 and Fig.3-12 show the I_D-V_G transfer characteristics of FSA-TFTs with in-situ gate, and W/L=10μm/0.8μm with different metal RTA at RTA 500°C for 30 seconds and 60 seconds, respectively. From Fig.5 to Fig.12, all of FSA-TFTs have the same channel thickness 50nm and T_{OX}=50nm. The drain voltage bias is 0.5V and 3.0V. It is noted that poly-Si TFTs with fully Ni-salicided process and NH_3 plasma treatment have better subthreshold swing, higher ON/OFF current ratio, and more stable V_{TH} than poly-Si TFTs without fully Ni-salicided process and NH_3 plasma treatment, and poly-Si TFTs only with fully Ni-salicided process. The reasons for these

improvements may be due to two aspects, one is that fully Ni-salicided S/D is able to passivate the defects of S/D junction, and the other is that fully Ni-salicided gate is able to obtain the better value of C_{OX}. The NH_3 plasma treatment can also passivate the defects of S/D surface and dielectric interface [43]. It is found that FSA-TFTs with RTA 500°C for 60 seconds have better S.S. and lower leakage current than FSA-TFTs with RTA 500°C for 30 seconds. So, RTA 500°C for 60 seconds is selected as the condition for comparison. The extracted values of V_{TH}, S.S., and ON/OFF current ratio are shown in Table 3-1.

Fig.3-13 and Fig.3-14 show I_D-V_G transfer characteristics of n-channel FSA-TFTs with undoped gate compared with conventional TFTs. Ni-salicide is formed by RTA at 500°C for 60 seconds. Devices with W/L=10μm/10μm and W/L=10μm/0.8μm have been measured. The drain voltage bias is 0.5V and 3.0V. It is found that FSA-TFTs with NH_3 plasma treatment have stable V_{TH}, better S.S., and higher ON/OFF current ratio than without ones; it is also found that devices with fully Ni-salicided S/D exhibit a lower leakage current about 10^{-13} ~10^{-14} order than conventional TFTs only with NH_3 plasma. This may be due to the passivation of the defects of S/D junction during the silicidation process.

Fig.3-15 and Fig.3-16 show field-effect mobility of n-channel FSA-TFTs with undoped gate compared with conventional TFTs. The Ni-salicide is formed by RTA at 500°C for 60 seconds. Devices with W/L=10μm/10μm and W/L=10μm/0.8μm have been measured. The drain voltage bias is 0.5V. The values of field-effect mobility are deduced and shown in Table 3-2. It is found that both long-channel and short-channel FSA-TFTs have higher mobility than conventional TFTs. These improvements are due to that NSA-TFTs have better value of C_{OX} for long-channel and reduced parasitic resistance for short-channel.

Fig.3-17 and Fig.3-18 show comparison of field-effect mobility between devices with W/L=10μm/10μm and W/L=10μm/0.8μm. Devices are n-channel FSA-TFTs with undoped gate and conventional TFTs, respectively. The Ni-salicide was formed at RTA 500°C for 60 seconds. It is found that FSA-TFTs with W/L=10μm/10μm and W/L=10μm/0.8μm exhibit the

same order of magnitude of mobility; however, conventional TFTs show a significant difference. This difference is due to the reduced parasitic resistance in FSA-TFTs, which shows no significant difference between long and short channel.

Fig.3-19 and Fig.3-20 show I_D-V_G transfer characteristics of n-channel FSA-TFTs with in-situ gate compared with conventional TFTs. The Ni-salicide was formed by RTA at 500^oC for 60 seconds. Devices with W/L=10μm/10μm and W/L=10μm/0.8μm have been measured. The drain voltage bias is 0.5V and 3.0V. It is found that FSA-TFTs with in-situ gate have stable V_{TH}, better S.S., larger ON/OFF current ratio than conventional TFTs. The reason of these results is the same as FSA-TFTs with undoped gate.

Fig.3-21 and Fig.3-22 show field-effect mobility of n-channel FSA-TFTs with in-situ gate compared with conventional TFTs. The Ni-salicide was formed by RTA at 500^oC for 60 seconds. Devices with W/L=10μm/10μm and W/L=10μm/0.8μm have been measured. Fig.3-23 and Fig.3-24 show comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel FSA-TFTs with in-situ gate and conventional TFTs, respectively. The drain voltage bias is 0.5V. The values of field-effect mobility are extracted and shown in Table 3-2. It is found that FSA-TFTs with in-situ gate have the same trends as FSA-TFTs with undoped gate.

3.1.2 Output Characteristics

Fig.3-25 shows comparison of I_D-V_D output characteristics between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. The Ni-salicide was formed by RTA at 500^oC for 60 seconds. Device with W/L=10μm/0.8μm has been measured at V_G-V_{TH}=0.5V, 1.0V, 1.5V, 2.0V, 2.5V. It is found that FSA-TFTs have a reduced kink effect and also an increased drain breakdown voltage. These results can strongly support that floating-body and parasitic BJT effects are significantly suppressed by the fully silicided S/D structure [44].

3.1.3 Floating-Body Effects

Fig.3-26 and Fig.3-27 show the comparison of floating-body effect between n-channel FSA-TFTs with undoped gate and in-situ gate and conventional TFTs. The Ni-salicide was formed by RTA at 500°C for 60 seconds. Device with W/L=10μm/0.8μm has been measured at V_D=0.5V, 1.0V, 3.0V, 5.0V, 7.0V. From these figure, it is found that FSA-TFTs have suppressed floating-body effect compared with conventional TFTs.

Fig.3-28 shows comparison of threshold voltage roll-off between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. Devices with W/L=10μm/0.8μm have been measured at V_D=0.5V, 1.0V, 3.0V, 5.0V, 7.0V. The values of V_{TH} are shown in Table 3-3. Fig.3-29 shows comparison of threshold voltage shift between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. The dimension of device is W/L=10μm/0.8μm, and reference values of V_{TH} are defined at V_D=0.5V.

The reduced V_{TH} roll-off and V_{TH} shift strongly support that the BJT effect is significantly suppressed in the fully salicided S/D structure. Similar suppression of the floating-body effect is reported in deep silicidation of partially depleted SOI devices, where the thick silicide layer worked as a sink for holes [45]. The diagram of Floating-body effect is shown in Fig.3-66.

3.1.4 Influence of Metal RTA Temperature and Time

Fig.3-30 shows comparison of threshold voltage roll-off for n-channel FSA-TFTs with undoped gate at RTA 500°C for 30 seconds and 60 seconds. The channel width is 10μm, and the drain voltage bias is 0.5V. The values of V_{TH} roll-off are shown in Table 3-4. We can find that FSA-TFTs with RTA 500°C for 60 seconds have less V_{TH} roll-off than FSA-TFTs with RTA 500°C for 30 seconds. Moreover, FSA-TFTs with RTA 500°C for 30 seconds have more positive values of V_{TH} than FSA-TFTs with RTA 500°C for 60 seconds. This result is due to

that FSA-TFTs with RTA 500°C for 30 seconds have worse subthreshold swing than FSA-TFTs with RTA 500°C for 60 seconds, as shown in Fig.3-31.

Fig.3-31 shows comparison of S.S. roll-off for n-channel FSA-TFTs with undoped gate at RTA 500°C for 30 seconds and 60 seconds. The channel width is 10μm, and the drain voltage bias is 0.5V. The values of S.S. roll-off are shown in Table 3-5. It is found that FSA-TFTs with RTA 500°C for 60 seconds have less values of S.S. than FSA-TFTs with RTA 500°C for 30 seconds. So, these results make FSA-TFTs with RTA 500°C for 30 seconds have more positive value of V_{TH} than RTA 500°C for 60 seconds.

Fig.3-32 shows comparison of threshold voltage roll-off for n-channel FSA-TFTs with in-situ gate at RTA 500°C for 30 seconds and 60 seconds. The channel width is 10μm, and the drain voltage bias is 0.5V. The values of V_{TH} are shown in Table 3-4. It is found that FSA-TFTs with RTA 500°C for 60 seconds have less V_{TH} roll-off than FSA-TFTs with RTA 500°C for 30 seconds. The reason of these results is the same as FSA-TFTs with undoped gate. Fig.3-33 shows comparison of S.S. roll-off for n-channel FSA-TFTs with in-situ gate at RTA 500°C for 30 seconds and 60 seconds. The channel width is 10μm, and the drain voltage bias is 0.5V. The values of S.S. roll-off are shown in Table 3-5.It is found that FSA-TFTs with RTA 500°C for 60 seconds have less value of S.S. than FSA-TFTs with RTA 500°C for 30 seconds. So, these results of V_{TH} and S.S. are the same trends as FSA-TFTs with undoped gate.

Fig.3-34 shows comparison of threshold voltage roll-off for n-channel FSA-TFTs with in-situ doped gate, undoped gate, conventional TFTs, and FSA-TFTs with RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage bias is 0.5V. The values of V_{TH} are shown in Table 3-4. It is found that the roll-off of threshold voltage V_{TH} is improved in FSA-TFTs. With this fully Ni-salicided structure, the floating body and parasitic bipolar effects can be eliminated, resulting in a stable V_{TH} and lower off-state leakage current [46]. Fig.3-35 shows comparison of S.S. roll-off for all devices. The values of S.S. are shown in Table 3-5. It is found that the anomalous roll-off of subthreshold swing is suppressed in

FSA-TFTs.

3.1.5 Extraction of Parasitic Resistance

Fig.3-36 and Fig.3-37 exhibit the parasitic resistance R_P of n-channel FSA-TFTs with undoped gate and in-situ gate, respectively. They are extracted by plotting the on state resistance (R_{on}) versus gate length. The channel width is 10μm, and the drain voltage bias is 0.5V. The R_P of FSA-TFTs with undoped gate is about 0.37 kΩ, and FSA-TFTs with in-situ gate is about 0.44 kΩ.

Fig.3-38 shows the parasitic resistance R_P of conventional TFTs, and the R_P of conventional TFTs is about 5.78 kΩ. It is found that FSA-TFTs have lower value of R_P than conventional TFTs. Obviously, this result is due to Ni-salicided process which can reduce parasitic resistance of S/D.

3.1.6 On/Off Current Ratio

Fig.3-39 shows the On/Off current ratio of n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. The I_{ON} is measured at V_G=10V and V_D=3.0V. I_{OFF} is the value of minimum current at V_D=3.0V. The channel width is 10μm. The values of On/Off current ratio are shown in Table 3-6. The ON/OFF current ratio can be increased with scaling down gate length in FSA-TFTs. The value of ON/OFF current ratio is about 10^7~10^9 order for FSA-TFTs and 10^6 order for conventional TFTs. It is found that leakage current can be reduced in FSA-TFTs with scaling down gate-length, but it not the case for the conventional TFTs. This is because of floating body effect for n-channel TFTs which result in larger leakage current at off-state for conventional TFTs. On the other hand, FSA-TFTs can suppress floating-body effect, resulting in a low leakage current.

3.2 Difference between Fully-Salicided and Partially Salicided n-Channel

TFTs with In-situ Poly- Si Gate

Fig.3-40 and Fig.3-41 exhibit transfer characteristics of n-channel FSA-TFTs with in-situ gate and partially Ni-salicided TFTs with in-situ gate. The partially Ni-salicided TFTs are formed suing thin 15 nm Ni-layer. Devices dimensions are W/L=10μm/10μm and W/L=10μm/0.8μm, respectively. Fig.3-42 and Fig.3-43 exhibit transfer characteristics for n-channel partially Ni-salicided TFTs with in-situ doped gate with W/L=10μm/10μm and W/L=10μm/0.8μm at RTA 500°C for 60 seconds and RTA 550°C for 30 seconds, respectively.

Fig.3-44 exhibits threshold voltage roll-off of n-channel FSA-TFTs with in-situ gate with RTA 500°C for 60s, partially Ni-salicided TFTs with in-situ gate witch RTA 550°C for 30s, and partially Ni-salicided TFTs with in-situ gate witch RTA 500°C for 60s. The values of V_{TH} roll-off are shown in Table 3-7. For long channel devices, uncompleted silicidation will occur as temperature of RTA is not high enough. This partially salicided TFTs have negative shift of V_{TH} than FSA-TFTs. But, for short channel devices, all of V_{TH} closed to each others. Specially, partially salicided TFTs with RTA 550°C for 30 seconds have the smallest V_{TH} roll-off among these devices. The electrical characteristics of the partially salicided TFTs with RTA 550°C for 30 seconds are also better than partially sallicided TFTs with RTA 500°C for 60 seconds. The reason for these improvements can be attributed to that thin Ni-layer make S/D lateral diffusion less than thick Ni-layer at high temperature. Hence, there is no large leakage current found in partially salicided TFTs with RTA 550°C for 30 seconds.

3.3 Basic Characteristics of p-Channel FAS-TFTs With Undoped Poly- Si Gate

In this section, the basic characteristics of p-channel FSA-TFTs will be explained. At first, the transfer characteristics of FSA-TFTs with undoped gate and conventional TFTs are compared in 3.3.1. In addition, the output characteristics of FSA-TFTs with undoped gate and conventional TFTs are compared in 3.3.2. The parasitic resistance of FSA-TFTs with undoped

gate and conventional TFTs are compared in 3.3.3. Finally, the ON/OFF current ratio of FSA-TFTs with undoped gate and conventional TFTs are compared in 3.3.4.

3.3.1 Transfer Characteristics

Fig.3-45 and Fig.3-46 display the I_D-V_G transfer characteristics of conventional TFTs with W/L=10μm/10μm and W/L=10μm/0.8μm, respectively. Moreover, these figures show two different treatment steps for p-channel. Obviously, conventional TFTs with NH_3 plasma treatment have better subthreshold swing, and higher ON/OFF current ratio. In addition, they have more stable V_{TH} than conventional TFTs without NH_3 plasma treatment.

Fig.3-47 and Fig.3-48 display the I_D-V_G transfer characteristics of FSA-TFTs with undoped gate with W/L=10μm/10μm at RTA 500°C for 30 seconds and 60 seconds, respectively. In addition, Fig.3-49 and Fig.3-50 show the I_D-V_G transfer characteristics of FSA-TFTs with undoped gate with W/L=10μm/0.8μm at RTA 500°C for 30 seconds and 60 seconds, respectively. From Fig.45 to Fig.50, all of FSA-TFTs are with channel thickness equal to 50nm and T_{OX}=50nm. The drain voltage bias is 0.5V and 3.0V. Obviously, poly-Si TFTs with fully Ni-salicided process and NH_3 plasma treatment have better subthreshold swing, higher ON/OFF current ratio, and more stable V_{TH} than poly-Si TFTs without fully Ni-salicided process and NH_3 plasma treatment, and poly-Si TFTs only with fully Ni-salicided process. It is found that these improvements can be attributed to that fully Ni-salicided S/D can passivate the defects of S/D junction, and fully Ni-salicided gate has a high value of C_{OX}. In addition, NH_3 plasma treatment can also passivate the defects of S/D surface and dielectric interface. Specially, we found that p-channel FSA-TFTs are more sensitive than n-channel FSA-TFTs on parasitic resistance. It is found that FSA-TFTs with RTA 500°C for 60 seconds have better S.S. and lower leakage current than FSA-TFTs with RTA 500°C for 30 seconds. So, RTA 500°C for 60 seconds is selected for reference.

Fig.3-51 and Fig.3-52 display I_D-V_G transfer characteristics of p-channel FSA-TFTs with

undoped gate compared with conventional TFTs. The Ni-salicide was formed by RTA at 500°C for 60 seconds. Devices with W/L=10μm/10μm and W/L=10μm/0.8μm have been measured. The drain voltage bias is 0.5V and 3.0V. The extracted values of V_{TH}, S.S., and ON/OFF current ratio are shown in Table 3-8 (a) and (b). It is found that FSA-TFTs with NH_3 plasma treatment have stable V_{TH}, better S.S., and higher ON/OFF current ratio. Similar to the n-channel, p-channel with fully Ni-salicided S/D with passivated defects of S/D junction can achieve a lower leakage current about 10^{-13} ~10^{-14} than conventional TFTs only with NH_3 plasma.

Fig.3-53 and Fig.3-54 display field-effect mobility of p-channel FSA-TFTs with undoped gate compared with conventional TFTs. The Ni-salicide was formed by RTA at 500°C for 60 seconds. Devices with W/L=10μm/10μm and W/L=10μm/0.8μm have been measured. The drain voltage bias is 0.5V. The values of field-effect mobility are shown in Table 3-8 (a). We find that both long-channel and short-channel of FSA-TFTs have higher mobility than conventional TFTs. This improved mobility is due to that FSA-TFTs have a high C_{OX} in long-channel and reduced parasitic resistance in short-channel.

Fig.3-55 and Fig.3-56 display field-effect mobility of devise with W/L=10μm/10μm and W/L=10μm/0.8μm, with undoped gate and conventional TFTs, respectively. The Ni-salicide was formed at RTA 500°C for 60 seconds. It is found that FSA-TFTs with W/L=10μm/10μm and W/L=10μm/0.8μm have the same order of magnitude of mobility; however, conventional TFTs have a significant reduction of mobility in short channel devices. This is due to the reduced parasitic resistance of FSA-TFTs in the short channel regime. This trend is the same as n-channel FSA-TFTs.

Fig.3-57 displays threshold voltage roll-off for p-channel FSA-TFTs with undoped gate, and conventional TFTs. The Ni-salicide was formed by RTA at 500°C for 60 seconds. The width is 10μm, and V_D=0.5V. The values of V_{TH} roll off are shown in Table 3-9 (a). Fig.3-58 displays S.S. roll-off of p-channel FSA-TFTs with undoped gate, and conventional TFTs. The

Ni-salicide was formed by RTA at 500°C for 60 seconds. The width is 10μm, and V_D=0.5V. The values of S.S. roll off are shown in Table 3-9 (b). From Fig.3-57 and Fig.3-58, we found that threshold voltage roll-off has the same trend as S.S. roll-off. Moreover, FSA-TFTs have less V_{TH} roll-off and S.S. than conventional TFTs. This implies that the trend of V_{TH} roll-off is affected by the trend of S.S. roll-off.

3.3.2 Output Characteristics

Fig.3-59 and Fig.3-60 display I_D-V_D output characteristics of p-channel FSA-TFTs with undoped gate and conventional TFTs with W/L=10μm/10μm. The Ni-salicide was formed by RTA at 500°C for 60 seconds. V_G-V_{TH} was set at -5.0V, -6.0V, -7.0V, -8.0V, -9.0V and V_G-V_{TH}=-2.0V, -3.0V, -4.0V, -5.0V, -6.0V, respectively.

Fig.3-61 and Fig.3-62 display I_D-V_D output characteristics between p-channel FSA-TFTs with undoped gate conventional TFTs with W/L=10μm/0.8μm. The Ni-salicide was formed by RTA at 500°C for 60 seconds. They are measured at V_G-V_{TH}=-5.0V, -5.5V, -6.0V, -6.5V, -7.0V and V_G-V_{TH}=-3.5V, -4.0V, -4.5V, -5.0V, -5.5V, respectively. It is found that I_D-V_D output characteristics of p-channel FSA-TFTs are smooth at saturation region. This is because that p-channel FSA-TFTs is not easy to produce impact ionization, which makes p-channel FSA-TFTs have lower floating-body effect than conventional TFTs. In addition, FSA-TFTs have lower parasitic resistance than conventional TFTs, so FSA-TFTs have higher drive current than conventional TFTs.

3.3.3 Extraction of Parasitic Resistance

Fig.3-63 and Fig.3-64 show the parasitic resistance R_P of FSA-TFTs with undoped gate and in-situ gate, respectively. They are extracted by plotting the on state resistance (R_{on}) versus gate length. The channel width is 10μm, and the drain voltage is 0.5V. The R_P of FSA-TFTs with undoped gate is about 0.39 kΩ. Fig.3-38 shows the parasitic resistance R_P of

conventional TFTs, and the R_P of conventional-TFTs is about 8.80 kΩ. It is found that FSA-TFTs have lower value of R_P than conventional TFTs. This result is due to the reduced parasitic resistance of S/D by Ni-salicided process.

3.3.4 On/Off Current Ratio

Fig.3-65 displays the On/Off current ratio of p-channel FSA-TFTs with undoped gate and conventional TFTs. The I_{ON} is measured at V_G=15V and V_D=3.0V. I_{OFF} is the minimum current at V_D=3.0V. The channel width is 10μm. The values of ON/OFF current ratio are shown in Table 3-10. The ON/OFF current ratio is increased with scaled down gate length in FSA-TFTs and conventional TFTs. The value of ON/OFF current ratio is about 10^7~10^9 for FSA-TFTs and conventional TFTs. But FSA-TFTs still have higher value of ON/OFF current ratio than conventional TFTs. This is because of FSA-TFTs have higher ON current than conventional TFTs. Moreover, p-channel TFTs have larger parasitic resistance and lower intensity of electric field at drain side than n-channel TFTs, therefore both p-channel FSA-TFTs and conventional TFTs have almost the same order of leakage current. This can explain ON/OFF current ratio of FSA-TFTs has the same trend as conventional TFTs. This result is different from that in n-channel FSA-TFTs.

Table 3-1 Summary of V_{TH}, S.S. and ON/OFF current ratio characteristics of FSA-TFTs and conventional TFTs with W/L=10µm/10µm and W/L=10µm/0.8µm.

	V_{TH} (V) L=10µm	V_{TH} (V) L=0.8µm	S.S. (mV/dec) L=10µm	S.S. (mV/dec) L=0.8µm	I_{ON}/I_{OFF} ratio L=10µm	I_{ON}/I_{OFF} ratio L=0.8µm
Conventional TFTs	1.85	0.35	783.13	591.75	1.25E6	1.54E6
FSA-TFTs with undoped gate (RTA 500°C,30s)	1.69	1.17	370.82	280.51	4.78E7	6.16E8
FSA-TFTs with undoped gate (RTA 500°C,60s)	1.50	1.09	361.99	261.84	4.93E7	6.51E8
FSA-TFTs with in-situ gate (RTA 500°C,30s)	1.70	0.88	473.88	301.66	3.75E7	6.33E8
FSA-TFTs with in-situ gate (RTA 500°C,60s)	1.38	0.71	388.37	282.50	6.20E7	1.58E9

Table 3-2 Summary of V_{TH} and μ_{FE} characteristics of FSA-TFTs and conventional TFTs with W/L=10μm/10μm and W/L=10μm/0.8μm.

	V_{TH} (V) L=10μm	V_{TH} (V) L=0.8μm	μ_{FE} (Max.) (cm^2/V-s) L=10μm	μ_{FE} (Max.) (cm^2/V-s) L=0.8μm
Conventional TFTs	1.85	0.35	29.32	22.44
FSA-TFTs with undoped gate (RTA 500°C,60s)	1.50	1.09	34.81	31.56
FSA-TFTs with in-situ gate (RTA 500°C,60s)	1.38	0.71	32.05	30.98

Table 3-3 Summary of V_{TH} versus drain bias V_{DS} characteristics of FSA-TFTs and conventional TFTs. VD= 0.5V, 1.0V, 3.0V, 5.0V, 7.0V.

	V_{TH} (V) V_D=0.5V	V_{TH} (V) V_D=1.0V	V_{TH} (V) V_D=3.0V	V_{TH} (V) V_D=5.0V	V_{TH} (V) V_D=7.0V
Conventional TFTs	0.52	0.43	0.30	-0.42	-1.96
FSA-TFTs with undoped gate (RTA 500°C,60s)	1.06	0.99	0.89	0.36	-0.49
FSA-TFTs with in-situ gate (RTA 500°C,60s)	0.59	0.51	0.37	-0.11	-1.04

Table 3-4 Summary of V_{TH} roll-off characteristics of FSA-TFTs and conventional TFTs.

	V_{TH} (V) L=10μm	V_{TH} (V) L=8μm	V_{TH} (V) L=5μm	V_{TH} (V) L=3μm	V_{TH} (V) L=2μm	V_{TH} (V) L=1μm	V_{TH} (V) L=0.8μm
Conventional TFTs	1.85	1.68	1.63	1.35	1.12	0.53	0.35
FSA-TFTs with undoped gate (RTA 500°C,30s)	1.69	1.64	1.63	1.62	1.54	1.37	1.17
FSA-TFTs with undoped gate (RTA 500°C,60s)	1.50	1.50	1.47	1.44	1.33	1.18	1.09
FSA-TFTs with in-situ gate (RTA 500°C,30s)	1.70	1.70	1.64	1.60	1.52	1.16	0.88
FSA-TFTs with in-situ gate (RTA 500°C,60s)	1.38	1.35	1.32	1.25	1.10	0.83	0.71

Table 3-5 Summary of subthreshold swing roll-off characteristics of FSA-TFTs and conventional TFTs.

	S.S. (mV/dec) L=10μm	S.S. (mV/dec) L=8μm	S.S. (mV/dec) L=5μm	S.S. (mV/dec) L=3μm	S.S. (mV/dec) L=2μm	S.S. (mV/dec) L=1μm	S.S. (mV/dec) L=0.8μm
Conventional TFTs	**783.13**	**738.64**	**746.52**	**720.19**	**710.35**	**620.04**	**591.75**
FSA-TFTs with undoped gate (RTA 500°C,30s)	**370.82**	**359.22**	**347.25**	**343.30**	**341.76**	**293.65**	**280.51**
FSA-TFTs with undoped gate (RTA 500°C,60s)	**361.99**	**341.30**	**331.42**	**324.94**	**318.24**	**318.24**	**261.84**
FSA-TFTs with in-situ gate (RTA 500°C,30s)	**473.88**	**438.05**	**409.34**	**399.92**	**397.25**	**332.65**	**301.66**
FSA-TFTs with in-situ gate (RTA 500°C,60s)	**388.37**	**371.34**	**356.46**	**342.28**	**342.21**	**300.11**	**282.50**

Table 3-6 Summary of ON/OFF current ratio characteristics of FSA-TFTs and conventional TFTs.

	I_{ON}/I_{OFF} ratio L=10μm	I_{ON}/I_{OFF} ratio L=8μm	I_{ON}/I_{OFF} ratio L=5μm	I_{ON}/I_{OFF} ratio L=3μm	I_{ON}/I_{OFF} ratio L=2μm	I_{ON}/I_{OFF} ratio L=1μm	I_{ON}/I_{OFF} ratio L=0.8μm
Conventional TFTs	1.25E6	1.48E6	1.42E6	3.69E6	1.72E6	1.90E6	1.54E6
FSA-TFTs with undoped gate (RTA 500°C,60s)	4.93E7	5.93E7	1.01E8	1.64E8	2.53E8	4.48E8	6.51E8
FSA-TFTs with in-situ gate (RTA 500°C,60s)	6.20E7	9.42E7	1.60E8	2.99E8	4.99E8	1.38E9	1.58E9

Table 3-7 Summary of V_{TH} roll-off characteristics of FSA-TFTs and partially salicided TFTs.

	V_{TH} (V) L=10μm	V_{TH} (V) L=8μm	V_{TH} (V) L=5μm	V_{TH} (V) L=3μm	V_{TH} (V) L=2μm	V_{TH} (V) L=1μm	V_{TH} (V) L=0.8μm
FSA-TFTs with in-situ gate (RTA 500°C,60s)	1.38	1.35	1.32	1.25	1.10	0.83	0.71
Partially NiSi-TFTs with in-situ gate (RTA 550°C,30s)	0.73	0.61	0.58	0.56	0.52	0.51	0.55
Partially NiSi-TFTs with in-situ gate (RTA 500°C,60s)	-0.24	-0.52	-0.70	-0.48	-0.30	0.13	0.39

Table 3-8 (a) and (b) Summary of V_{TH}, μ_{FE}, S.S. and ON/OFF current ratio characteristics of FSA-TFTs and conventional TFTs with W/L=10μm/10μm and W/L=10μm/0.8μm.

(a) Values of V_{TH}, μ_{FE}

	V_{TH} (V) L=10μm	V_{TH} (V) L=0.8μm	μ_{FE} (Max.) (cm^2/V-s) L=10μm	μ_{FE} (Max.) (cm^2/V-s) L=0.8μm
Conventional TFTs	**-5.86**	**-3.87**	**18.92**	**11.84**
FSA-TFTs with undoped gate (RTA 500°C,60s)	**-4.94**	**-3.55**	**27.57**	**27.66**

(b) Values of S.S. and ON/OFF current ratio

	S.S. (mV/dec) L=10μm	S.S. (mV/dec) L=0.8μm	I_{ON}/I_{OFF} ratio L=10μm	I_{ON}/I_{OFF} ratio L=0.8μm
Conventional TFTs	**805.12**	**307.94**	**1.29E7**	**1.21E8**
FSA-TFTs with undoped gate (RTA 500°C,60s)	**639.47**	**290.74**	**2.89E7**	**9.95E8**

Table 3-9 (a) and (b) Summary of V_{TH} roll-off and subthreshold swing roll-off characteristics of FSA-TFTs and conventional TFTs.

(a) Values of V_{TH}

	V_{TH} (V) L=10μm	V_{TH} (V) L=8μm	V_{TH} (V) L=5μm	V_{TH} (V) L=3μm	V_{TH} (V) L=2μm	V_{TH} (V) L=1μm	V_{TH} (V) L=0.8μm
Conventional TFTs	-5.86	-5.88	-5.90	-5.57	-5.30	-4.38	-3.87
FSA-TFTs with undoped gate (RTA 500°C,60s)	-4.94	-4.98	-4.93	-4.82	-4.64	-4.12	-3.55

(b) Values of S.S.

	S.S. (mV/dec) L=10μm	S.S. (mV/dec) L=8μm	S.S. (mV/dec) L=5μm	S.S. (mV/dec) L=3μm	S.S. (mV/dec) L=2μm	S.S. (mV/dec) L=1μm	S.S. (mV/dec) L=0.8μm
Conventional TFTs	805.12	747.40	696.65	653.59	490.93	410.59	307.94
FSA-TFTs with undoped gate (RTA 500°C,60s)	639.47	632.67	563.06	542.43	428.29	359.49	290.74

Table 3-10 Summary of ON/OFF current ratio characteristics of FSA-TFTs and conventional TFTs.

	I_{ON}/I_{OFF} ratio L=10μm	I_{ON}/I_{OFF} ratio L=8μm	I_{ON}/I_{OFF} ratio L=5μm	I_{ON}/I_{OFF} ratio L=3μm	I_{ON}/I_{OFF} ratio L=2μm	I_{ON}/I_{OFF} ratio L=1μm	I_{ON}/I_{OFF} ratio L=0.8μm
Conventional TFTs	1.29E7	1.94E7	1.97E7	4.62E7	5.78E7	9.80E7	1.20E8
FSA-TFTs with undoped gate (RTA 500°C,60s)	2.89E7	4.95E7	6.33E7	1.84E8	1.89E8	4.01E8	9.96E8

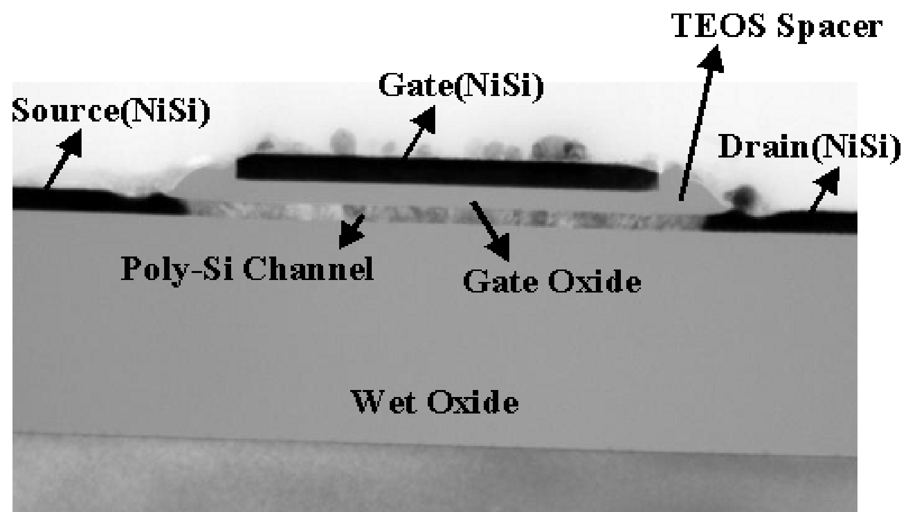


Fig.3-1 TEM photograph for cross-section of FSA-TFTs.

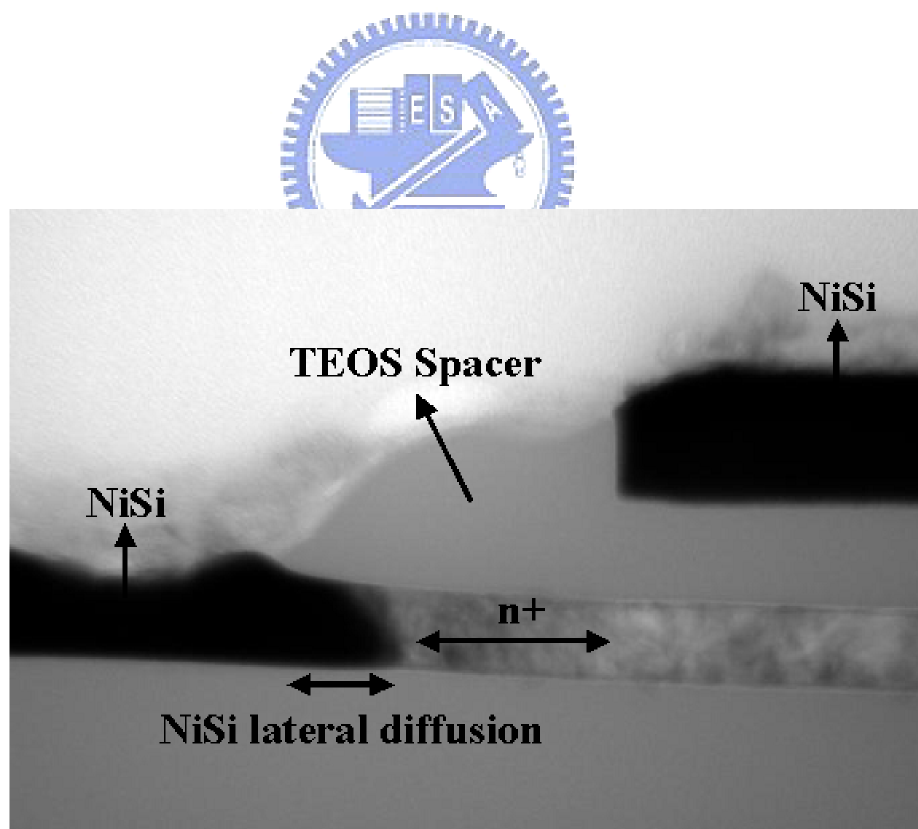


Fig.3-2 TEM photograph for cross-section of S/D junction.

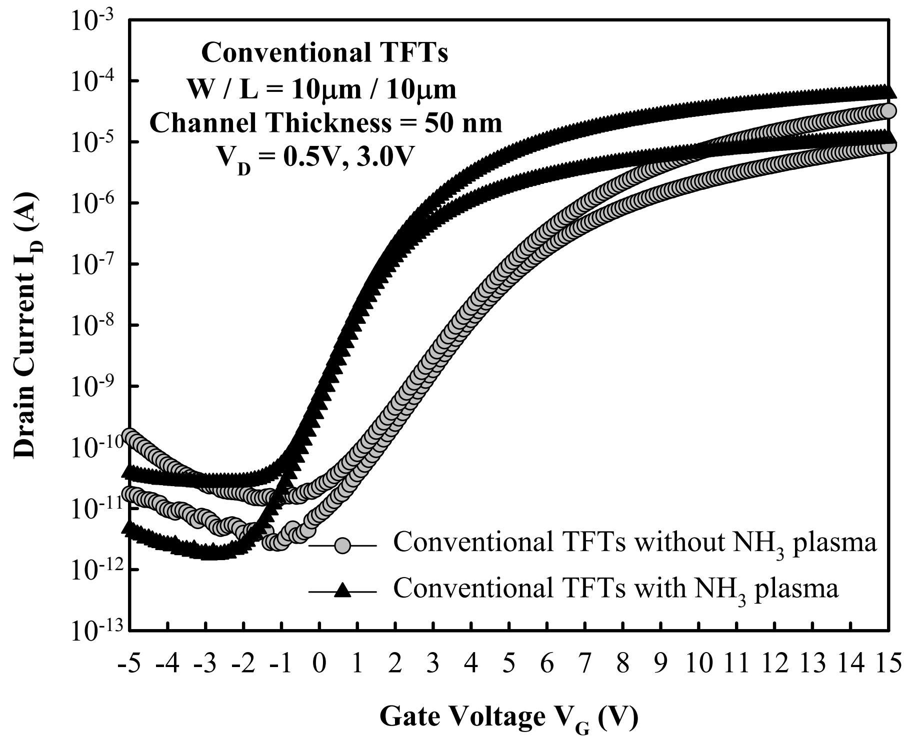


Fig. 3-3 Transfer characteristics of conventional TFTs with W/L=10μm/10μm, and two different treatment steps for n-channel.

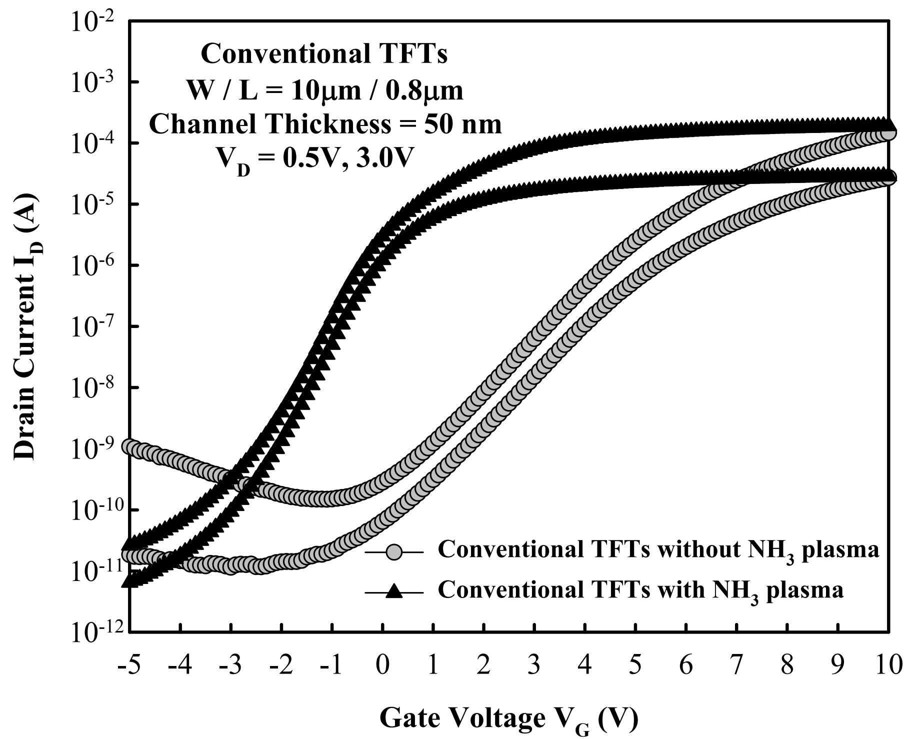


Fig. 3-4 Transfer characteristics of conventional TFTs with W/L=10μm/0.8μm, and two different treatment steps for n-channel.

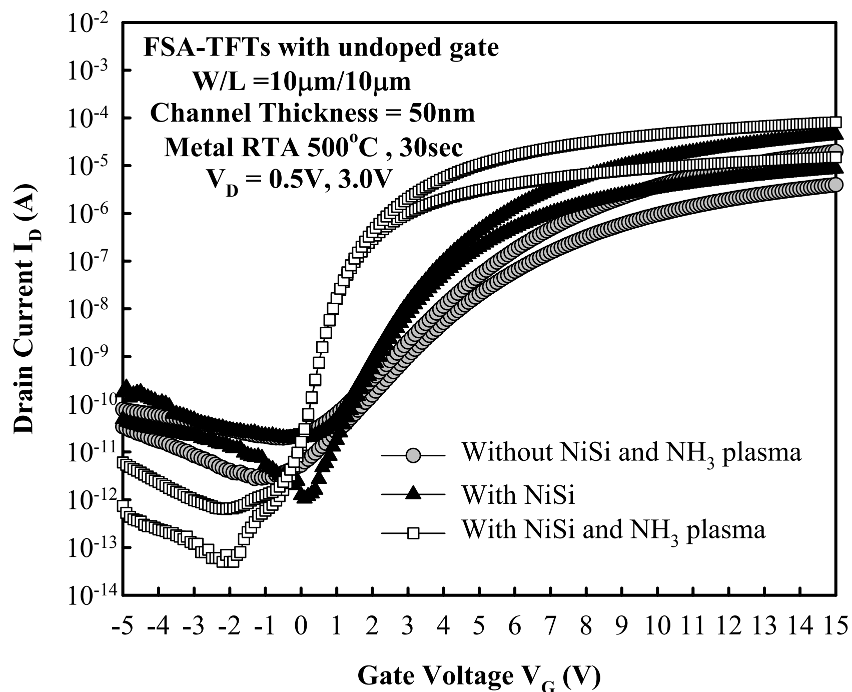


Fig.3-5 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/10μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

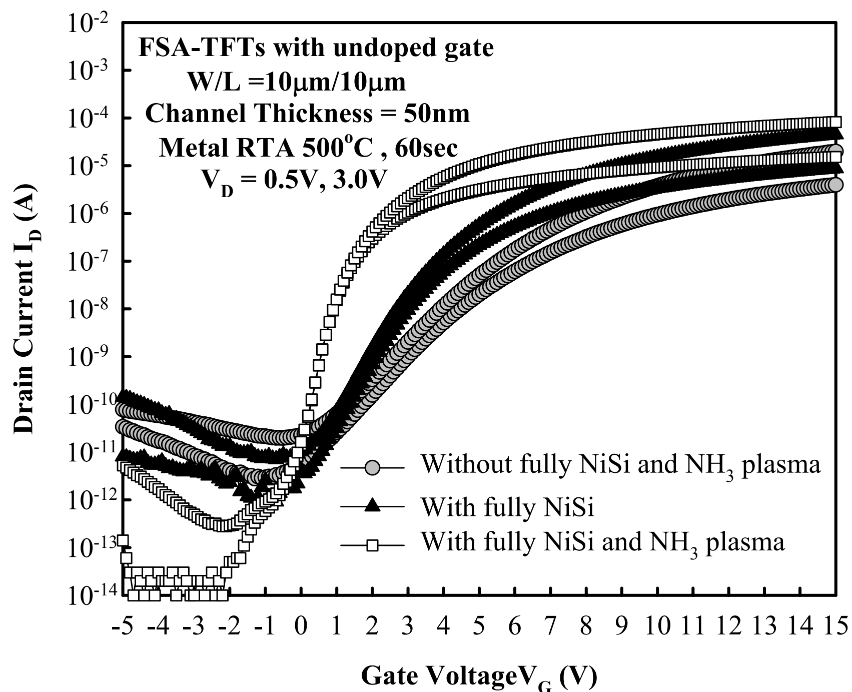


Fig.3-6 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/10μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

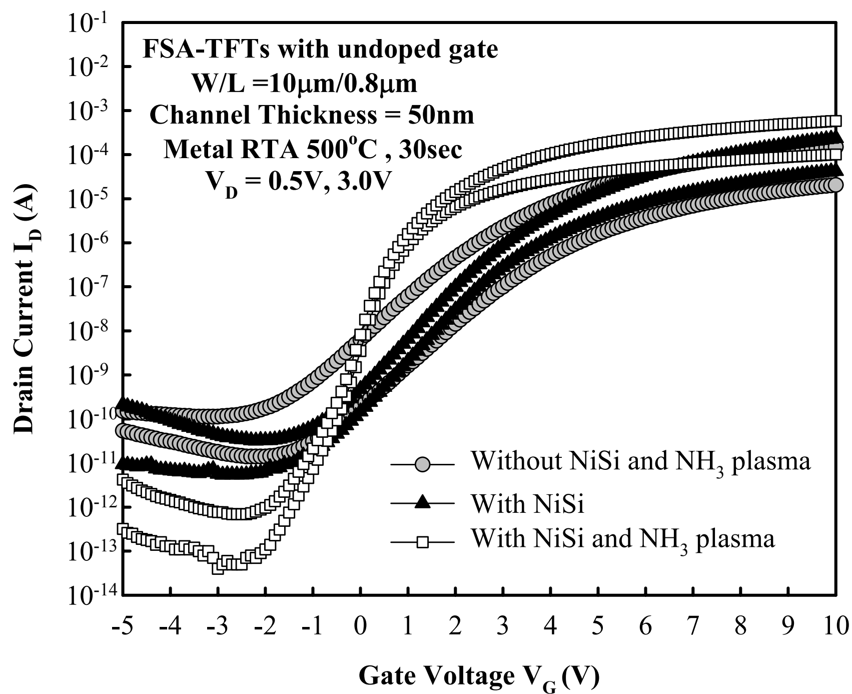


Fig.3-7 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/0.8μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

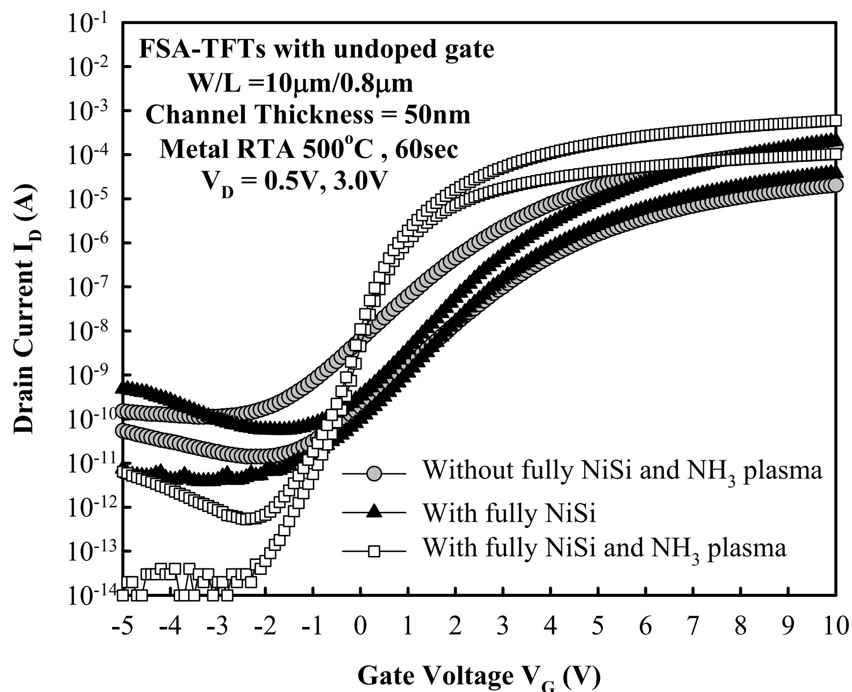


Fig.3-8 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/0.8μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

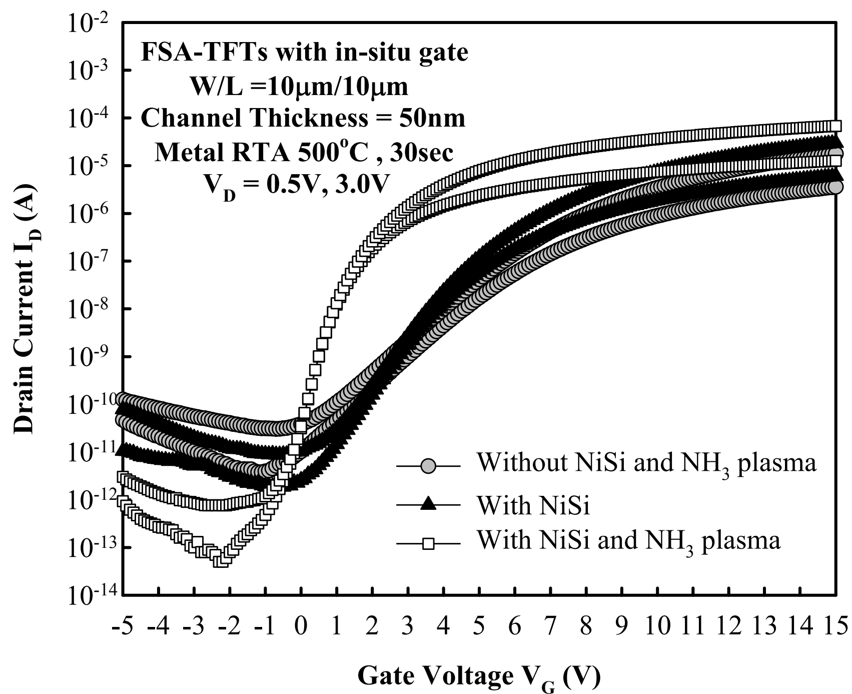


Fig.3-9 Transfer characteristics of FSA-TFTs with in-situ gate, W/L=10μm/10μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

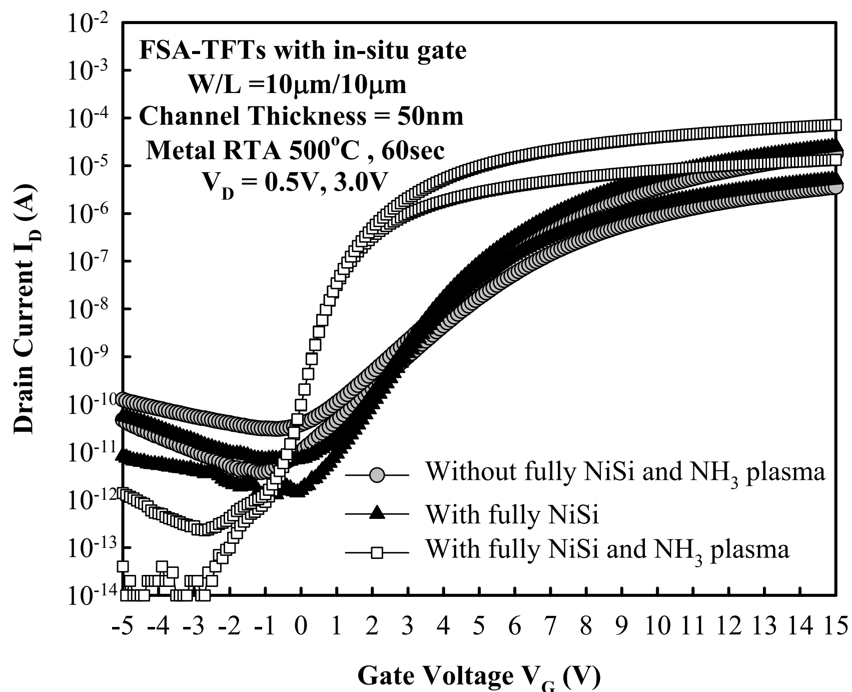


Fig.3-10 Transfer characteristics of FSA-TFTs with in-situ gate, W/L=10μm/10μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

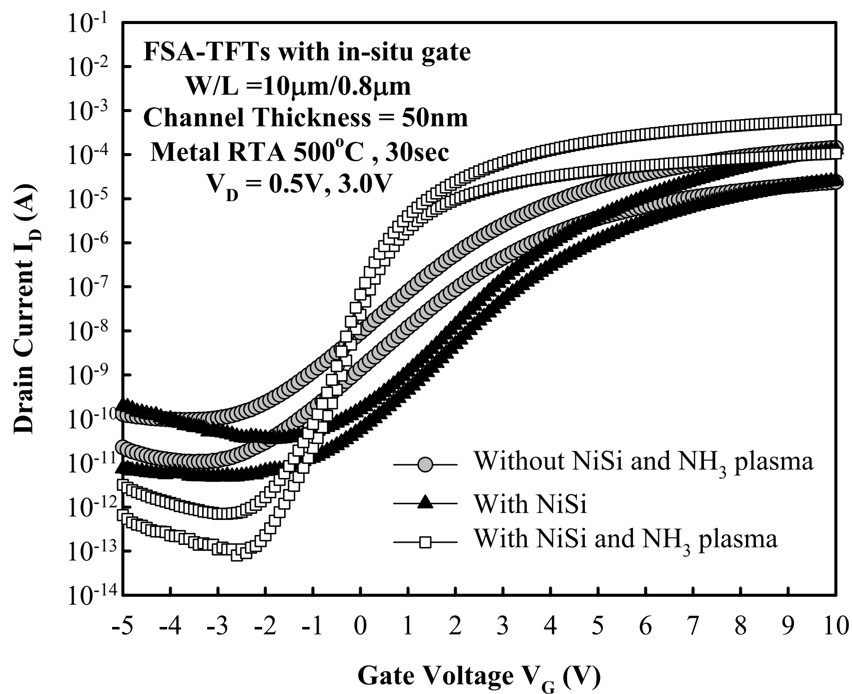


Fig.3-11 Transfer characteristics of FSA-TFTs with in-situ gate, W/L=10μm/0.8μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

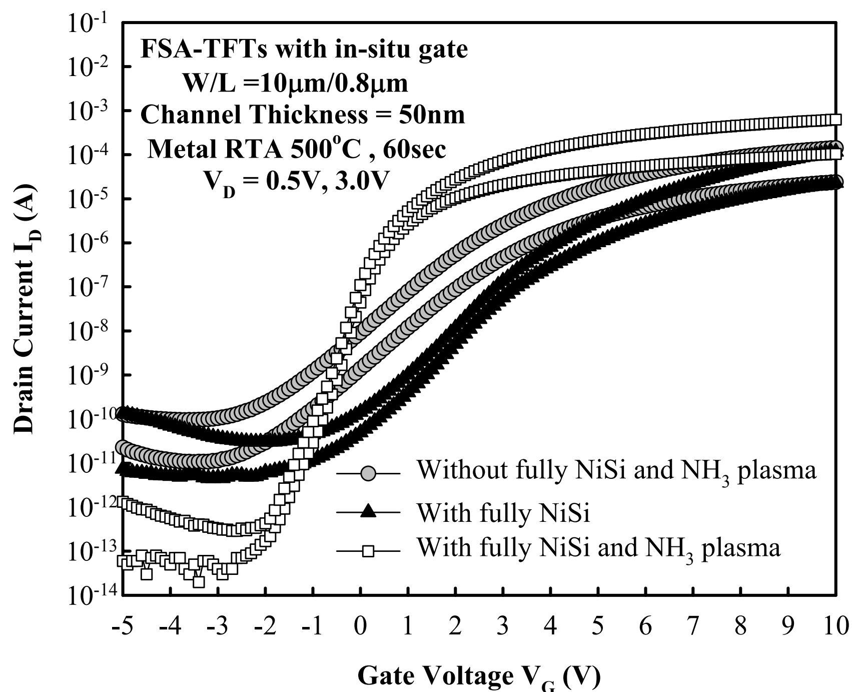


Fig.3-12 Transfer characteristics of FSA-TFTs with in-situ gate, W/L=10μm/0.8μm, and three different treatment steps for n-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

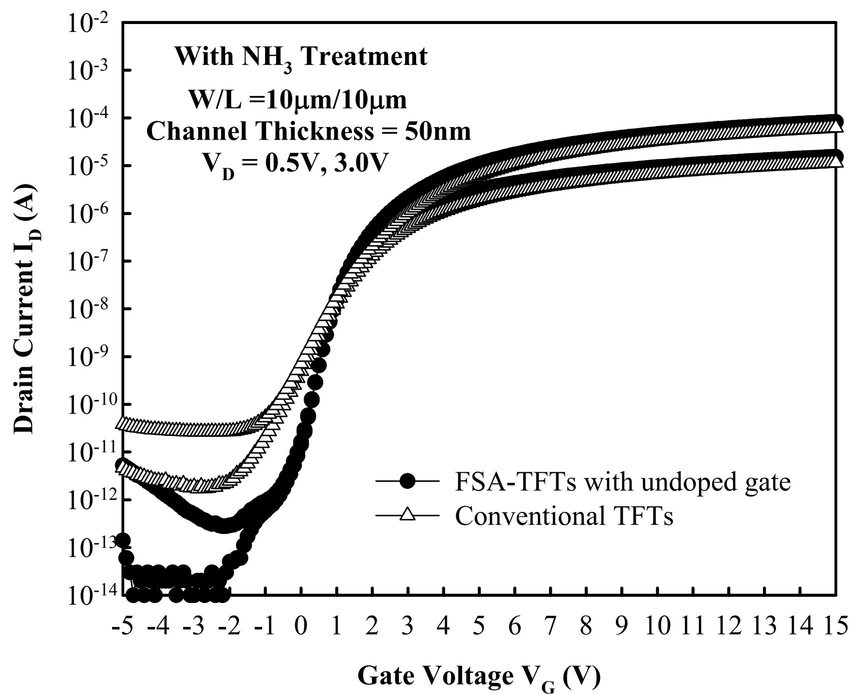


Fig. 3-13 Transfer characteristics of n-channel FSA-TFTs with undoped gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

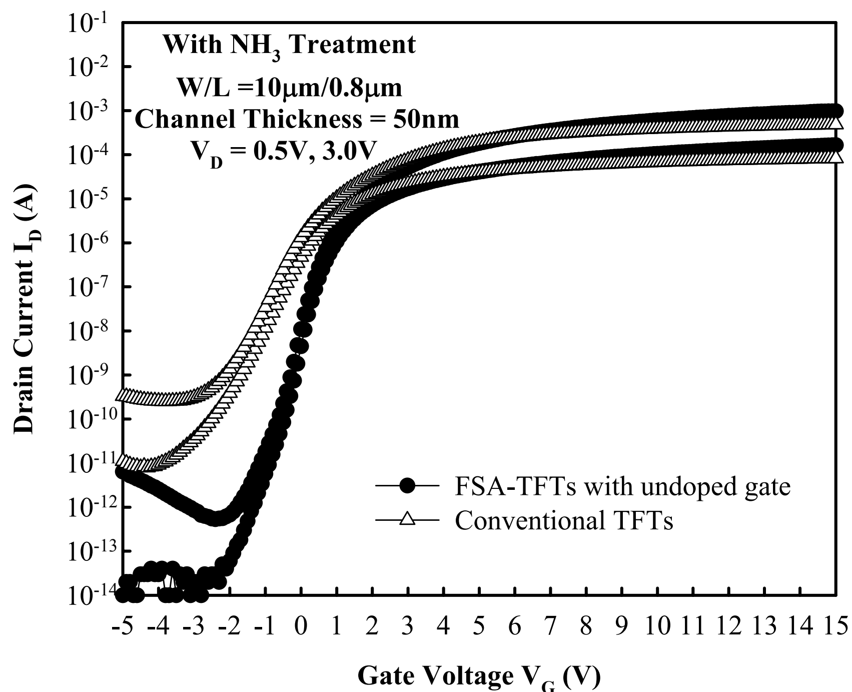


Fig. 3-14 Transfer characteristics of n-channel FSA-TFTs with undoped gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

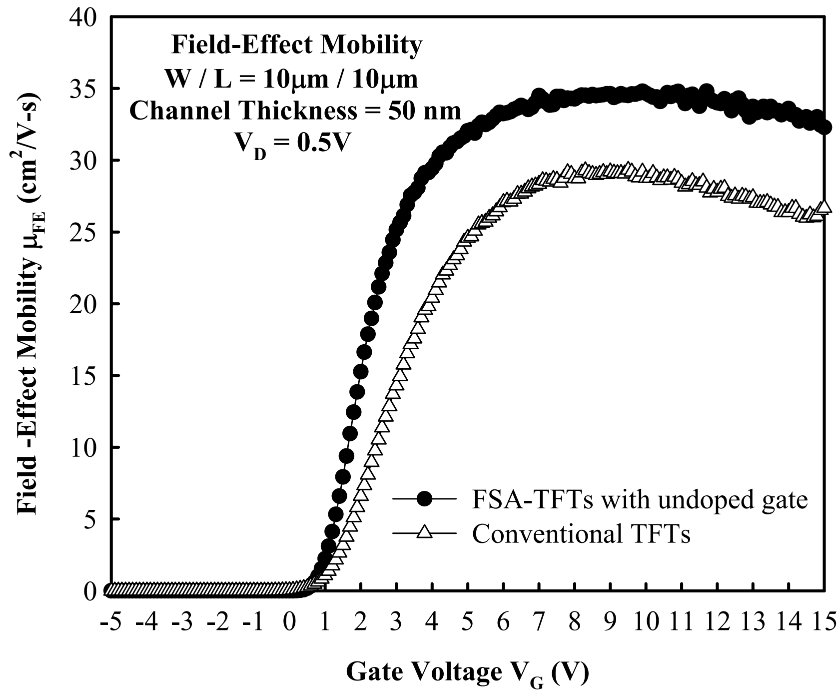


Fig.3-15 Field-effect mobility of n-channel FSA-TFTs with undoped gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

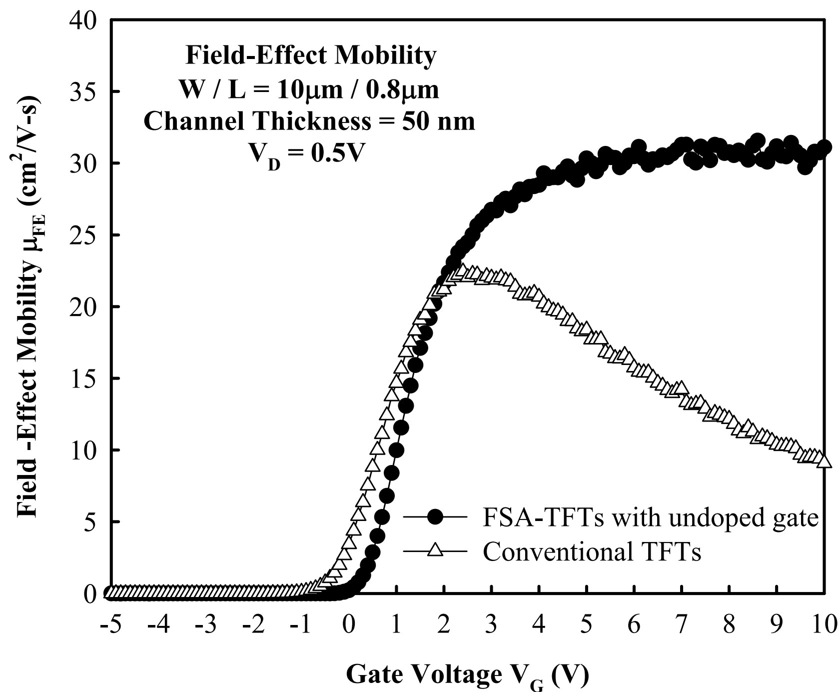


Fig.3-16 Field-effect mobility of n-channel FSA-TFTs with undoped gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

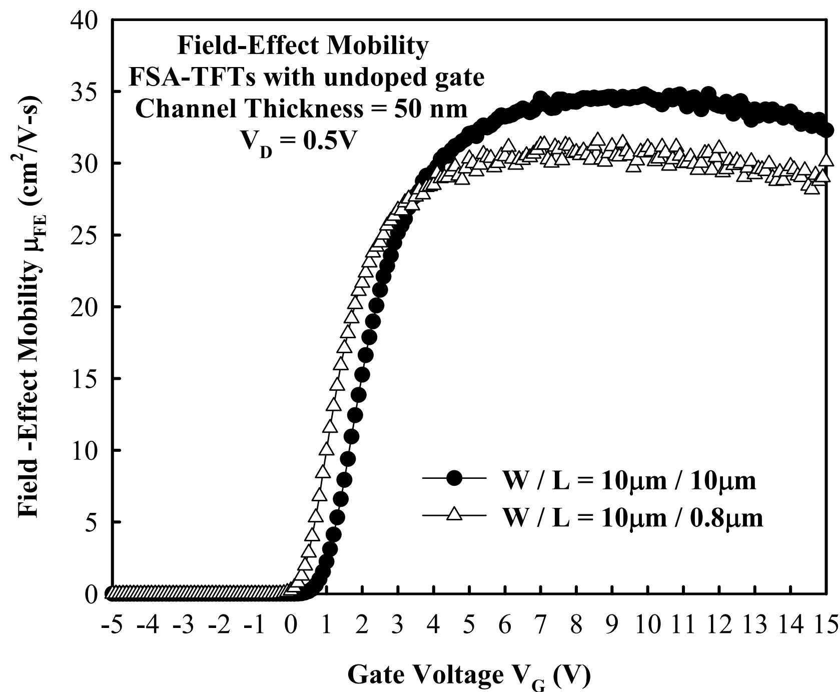


Fig.3-17 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel FSA-TFTs with undoped gate. Ni-salicide was formed by RTA 500°C for 60 seconds.

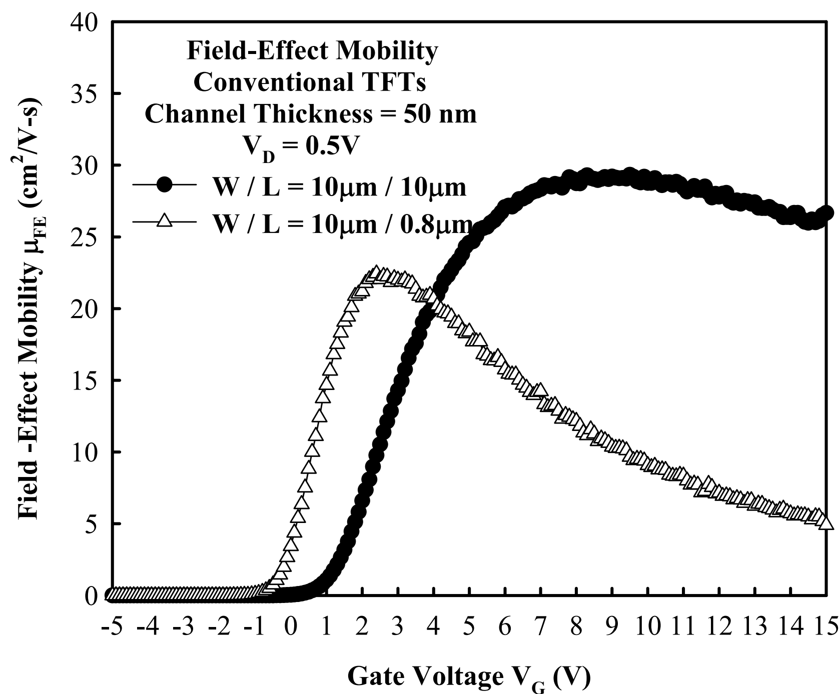


Fig.3-18 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel conventional TFTs.

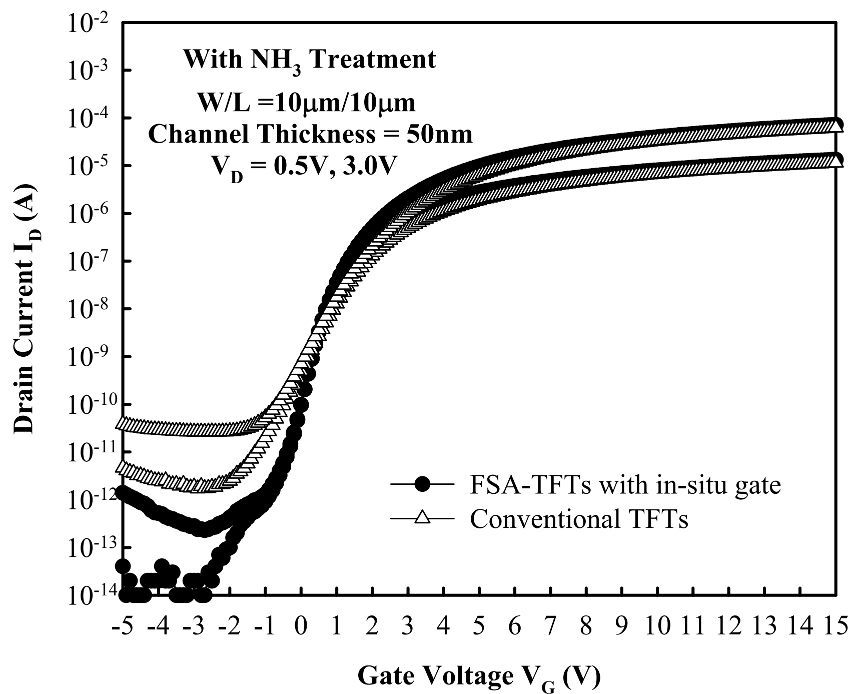


Fig.3-19 Transfer characteristics of n-channel FSA-TFTs with in-situ gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

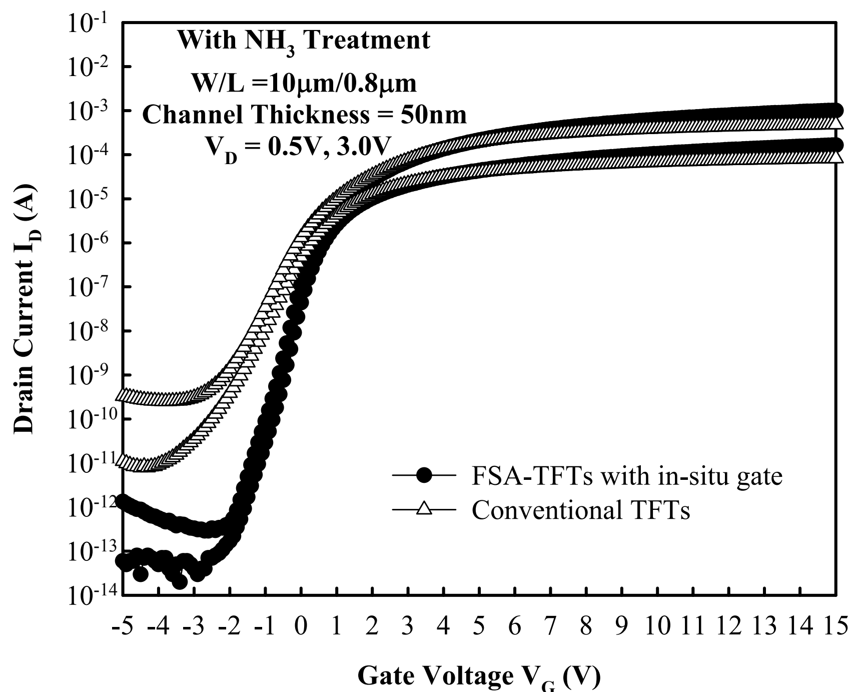


Fig.3-20 Transfer characteristics of n-channel FSA-TFTs with in-situ gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

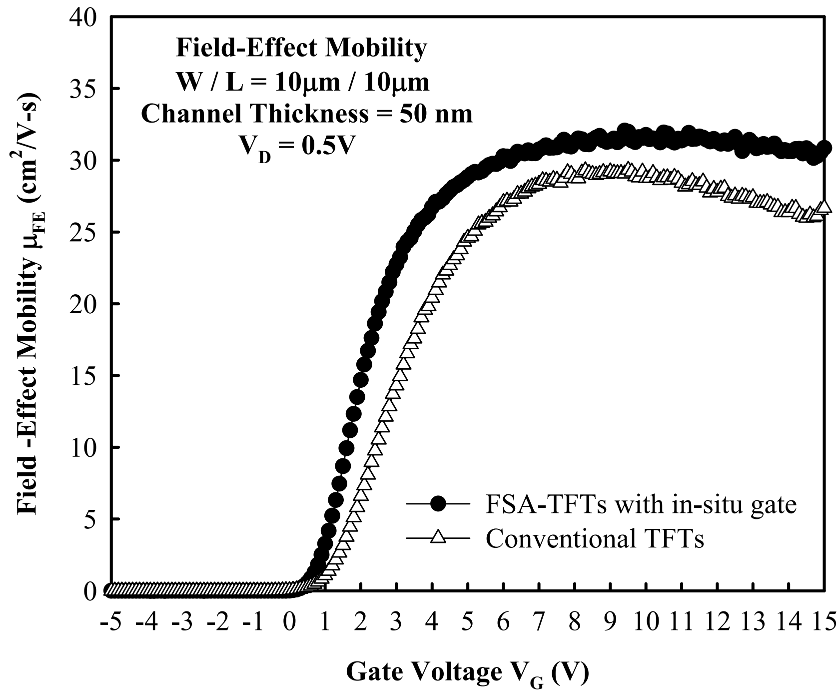


Fig. 3-21 Field-effect mobility of n-channel FSA-TFTs with in-situ gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

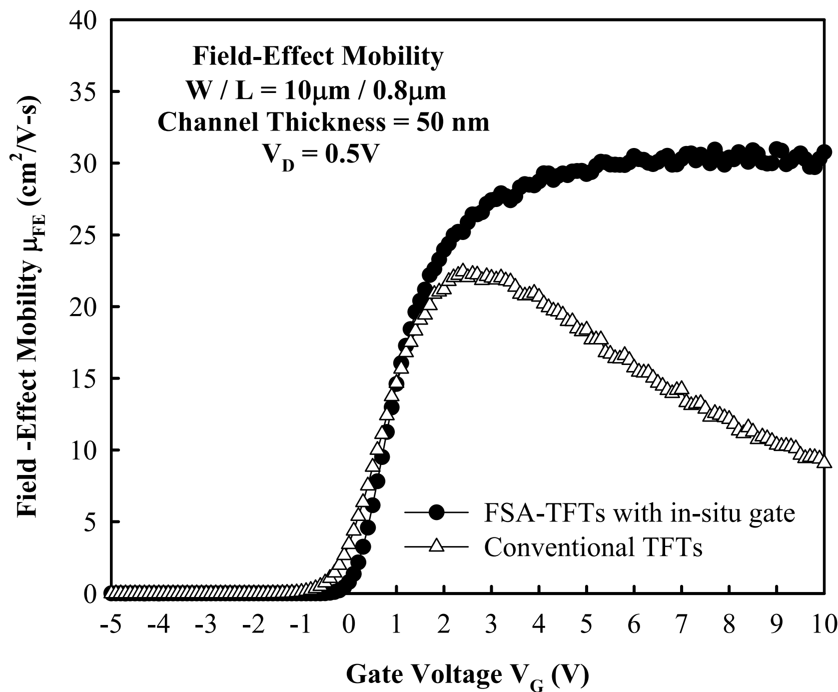


Fig. 3-22 Field-effect mobility of n-channel FSA-TFTs with in-situ gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

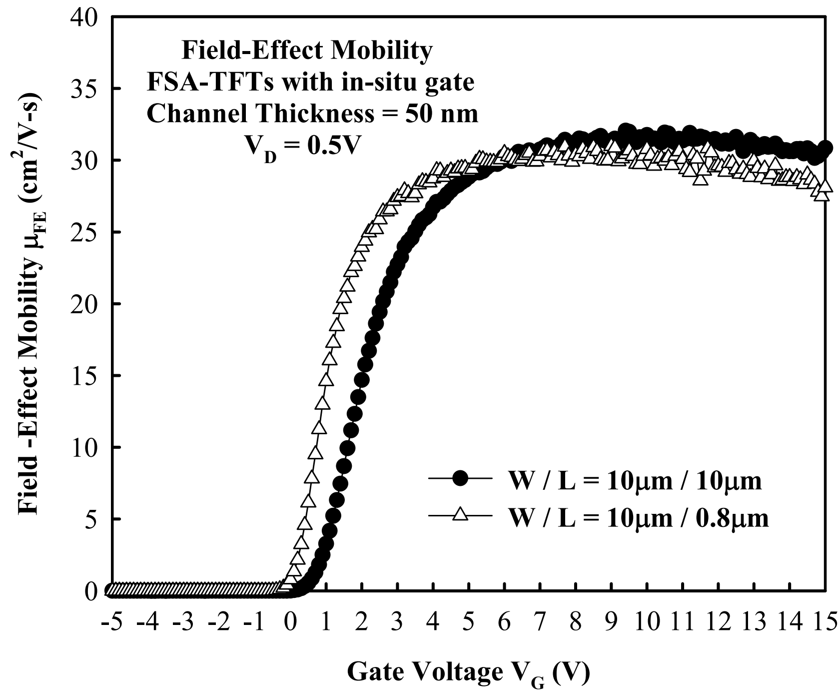


Fig. 3-23 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel FSA-TFTs with in-situ gate. Ni-salicide was formed by RTA 500°C for 60 seconds.

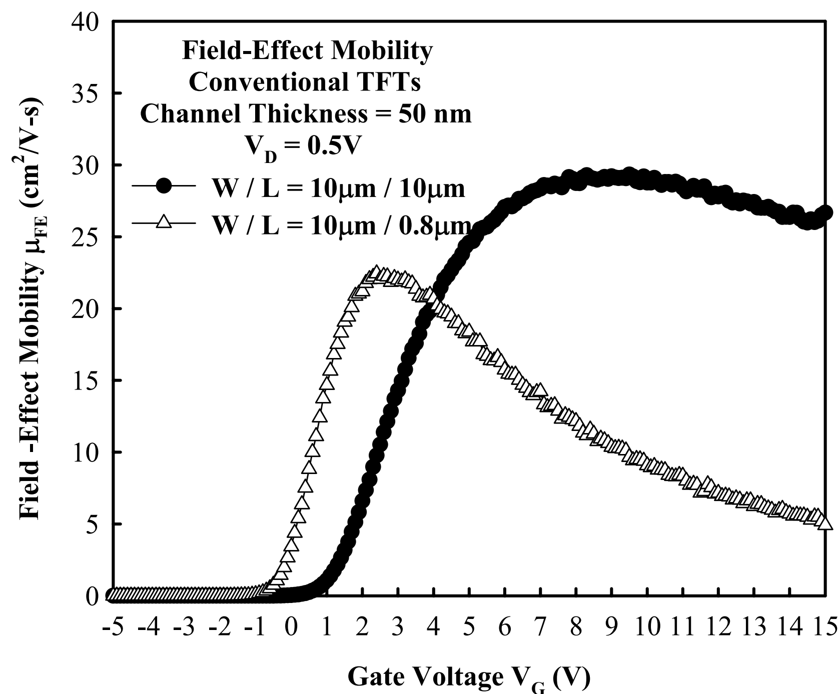


Fig. 3-24 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel conventional TFTs.

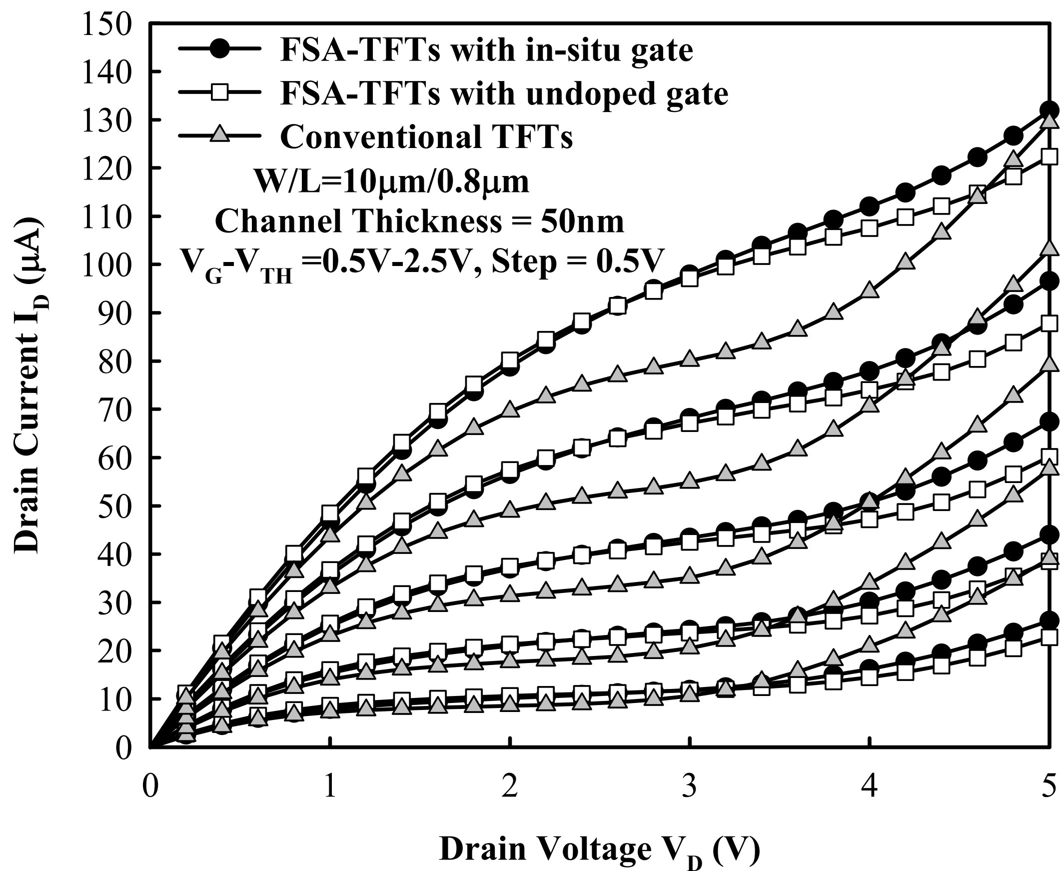


Fig.3-25 Comparison of output characteristics between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_G-V_{TH}=0.5V, 1.0V, 1.5V, 2.0V, 2.5V.

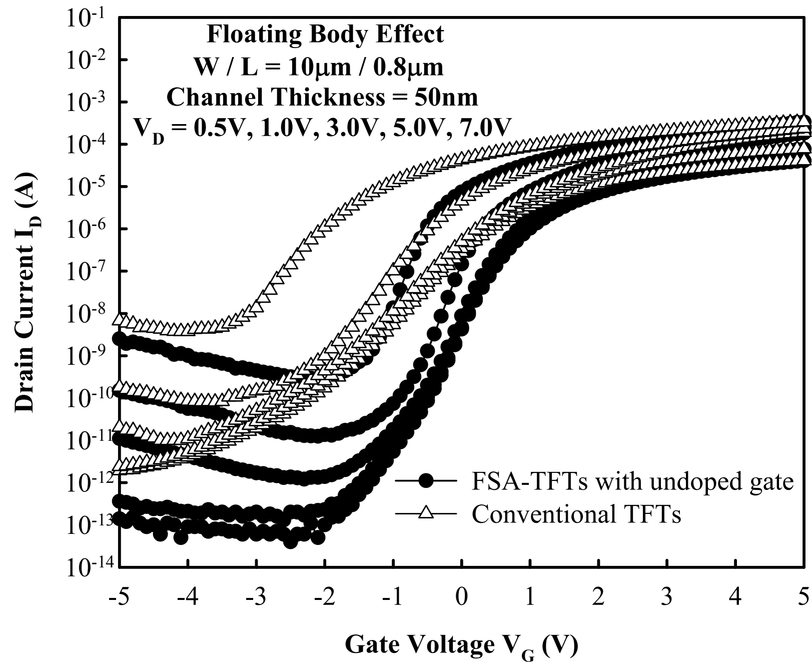


Fig.3-26 Comparison of floating-body effect between n-channel FSA-TFTs with undoped gate and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_D=0.5V, 1.0V, 3.0V, 5.0V, 7.0V.

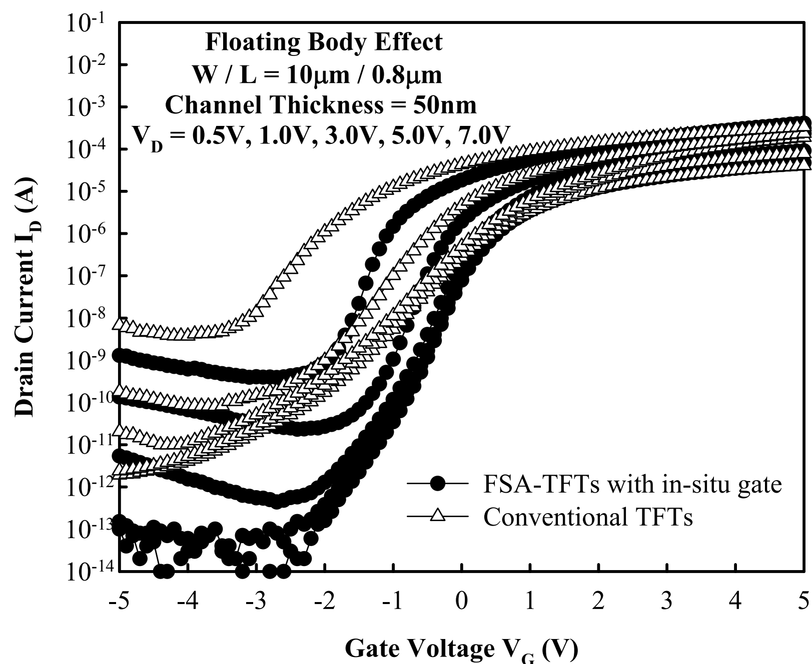


Fig.3-27 Comparison of floating-body effect between n-channel FSA-TFTs with in-situ gate and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_D=0.5V, 1.0V, 3.0V, 5.0V, 7.0V.

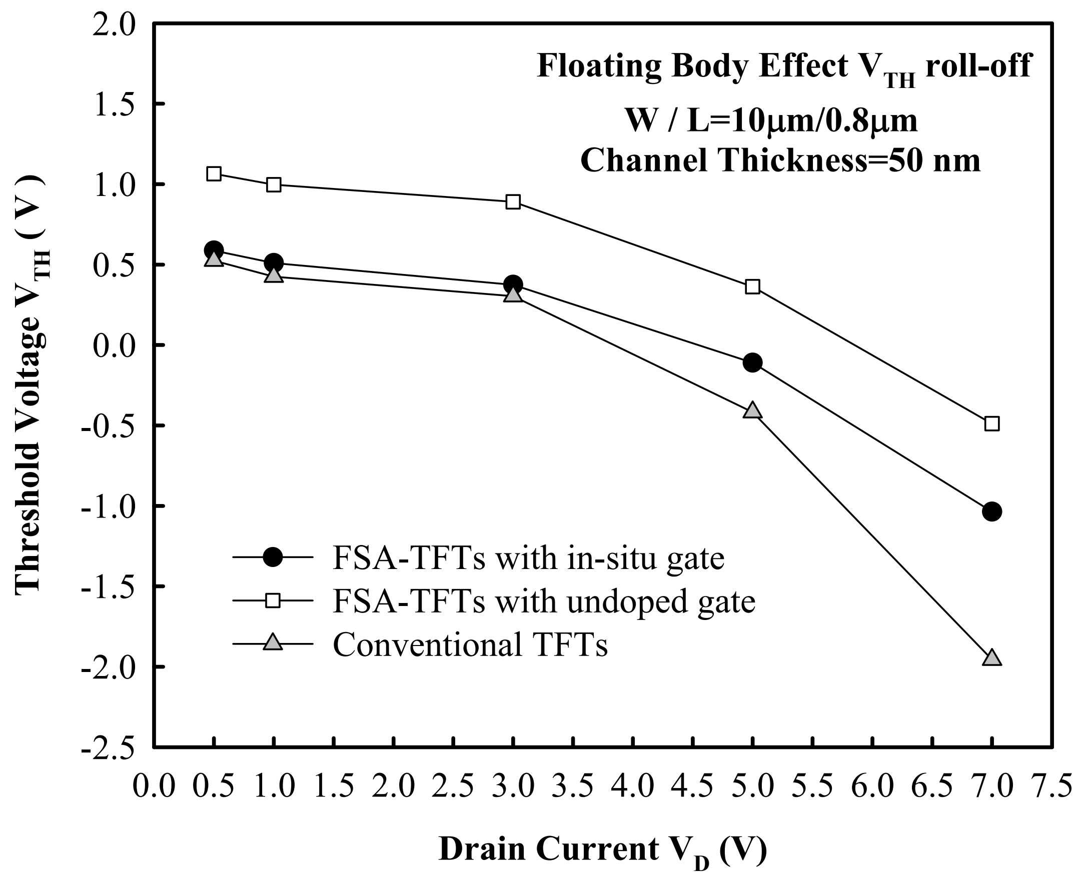


Fig.3-28 Comparison of threshold voltage roll-off between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs for floating-body effect. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_D=0.5V, 1.0V, 3.0V, 5.0V, 7.0V.

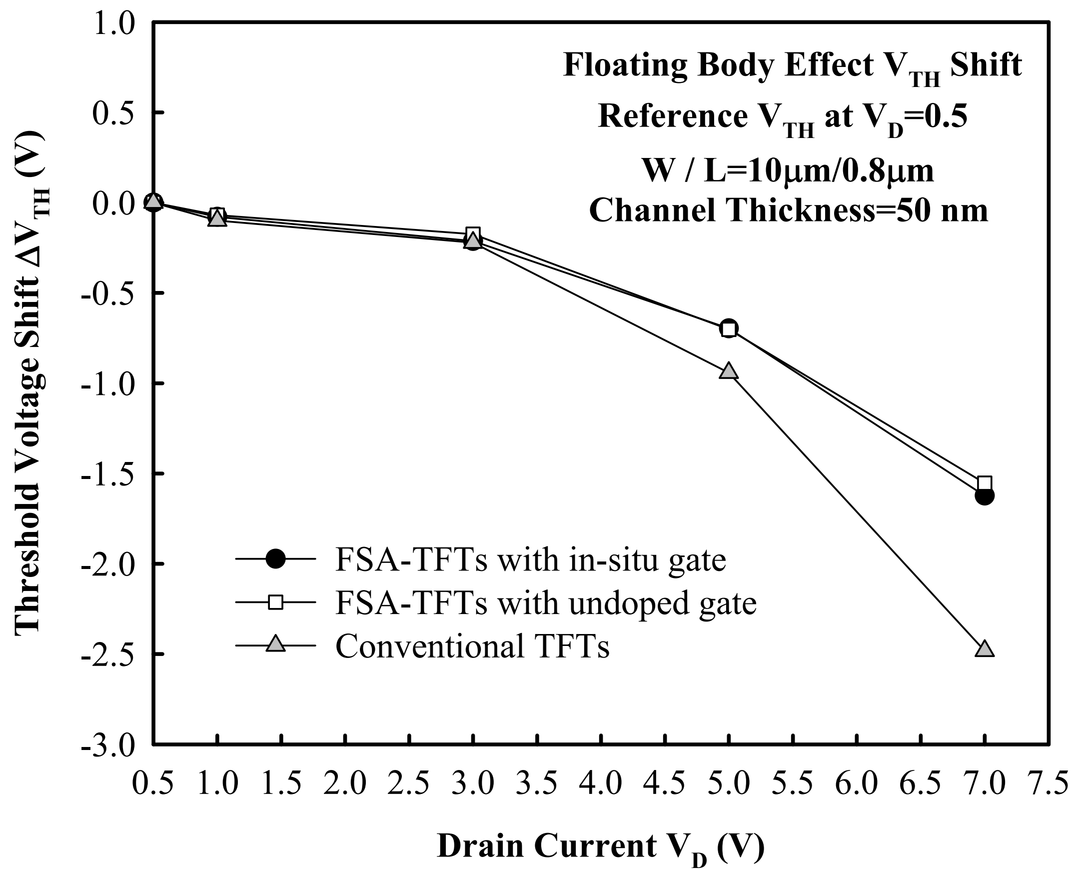


Fig.3-29 Comparison of threshold voltage shift between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs for floating-body effect. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and reference V_{TH} is defined at V_D=0.5V.

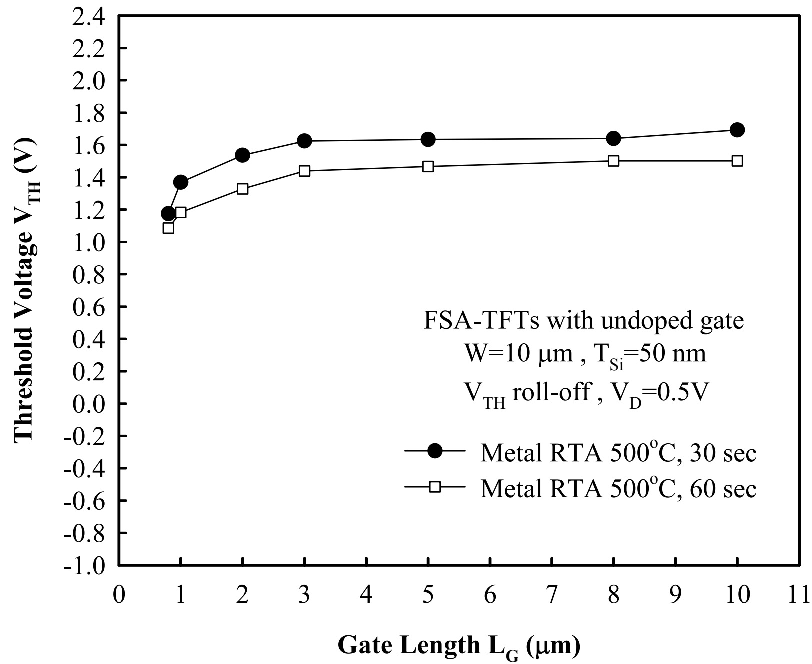


Fig.3-30 Comparison of threshold voltage roll-off between RTA 500°C for 30 seconds and RTA 500°C for 60 seconds for n-channel FSA-TFTs with undoped gate. The channel width is 10μm, and the drain voltage is 0.5V.

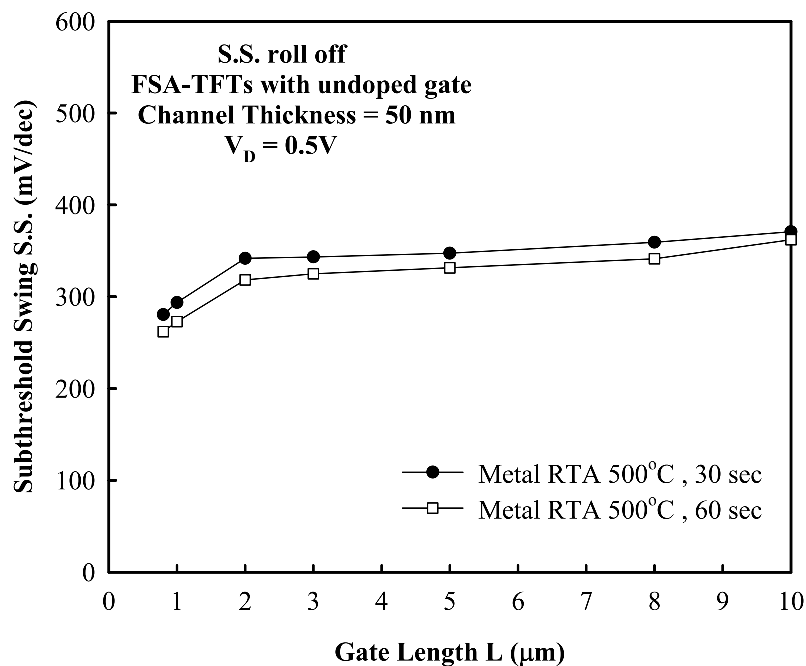


Fig.3-31 Comparison of subthreshold swing roll-off between RTA 500°C for 30 seconds and RTA 500°C for 60 seconds for n-channel FSA-TFTs with undoped gate. The channel width is 10μm, and the drain voltage is 0.5V.

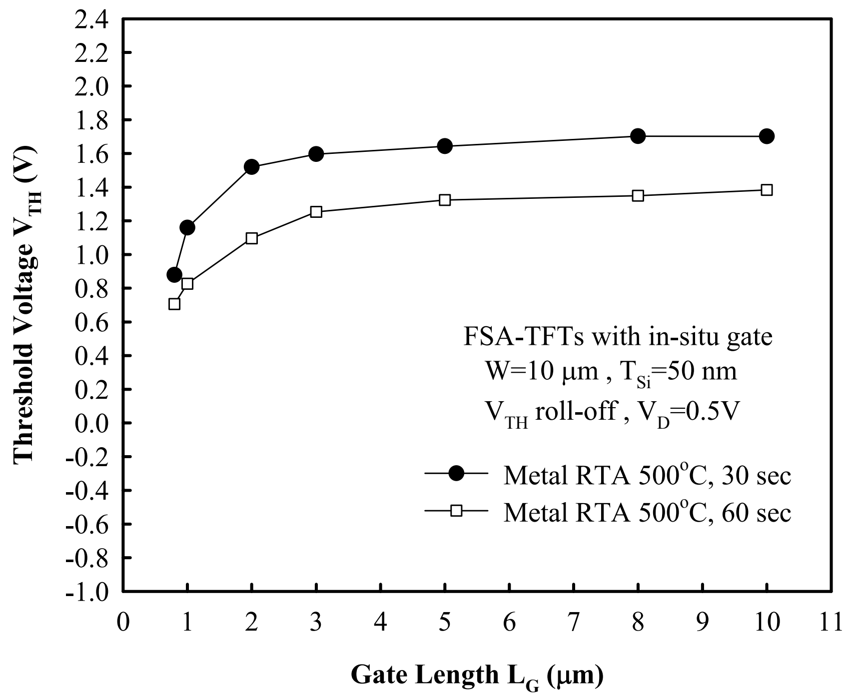


Fig. 3-32 Comparison of threshold voltage roll-off between RTA 500°C for 30 seconds and RTA 500°C for 60 seconds for n-channel FSA-TFTs with in-situ gate. The channel width is 10μm, and the drain voltage is 0.5V.

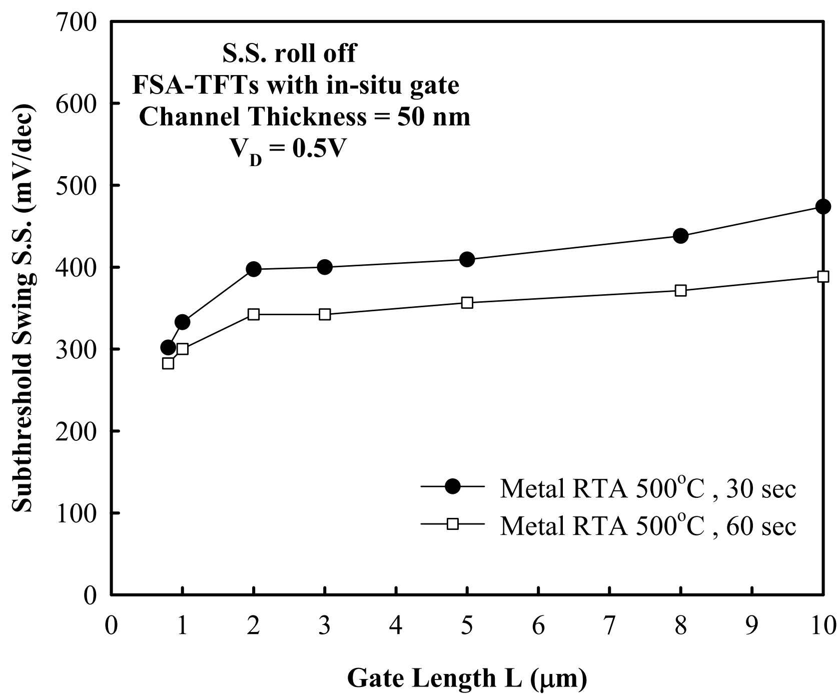


Fig.3-33 Comparison of subthreshold swing roll-off between RTA 500°C for 30 seconds and RTA 500°C for 60 seconds for n-channel FSA-TFTs with in-situ gate. The channel width is 10μm, and the drain voltage is 0.5V.

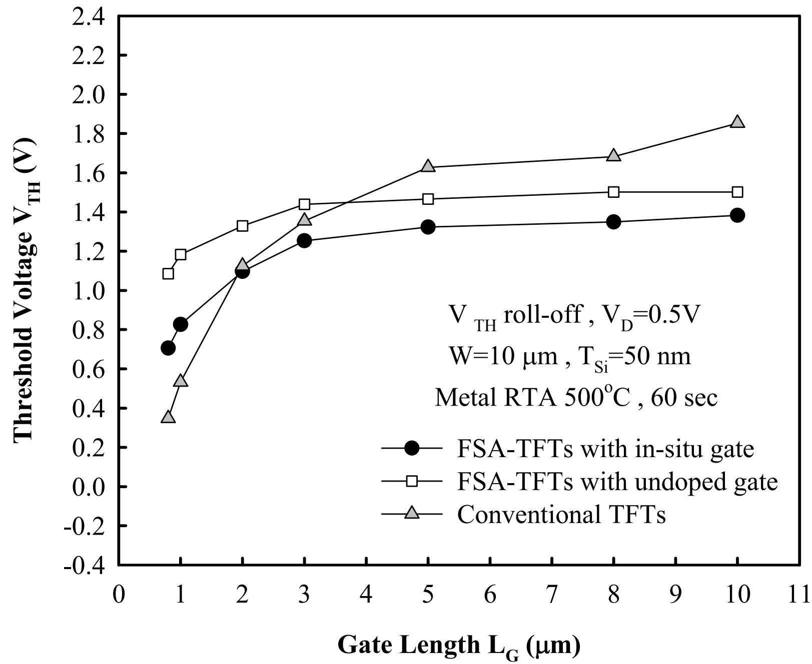


Fig.3-34 Comparison of threshold voltage roll-off between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage is 0.5V.

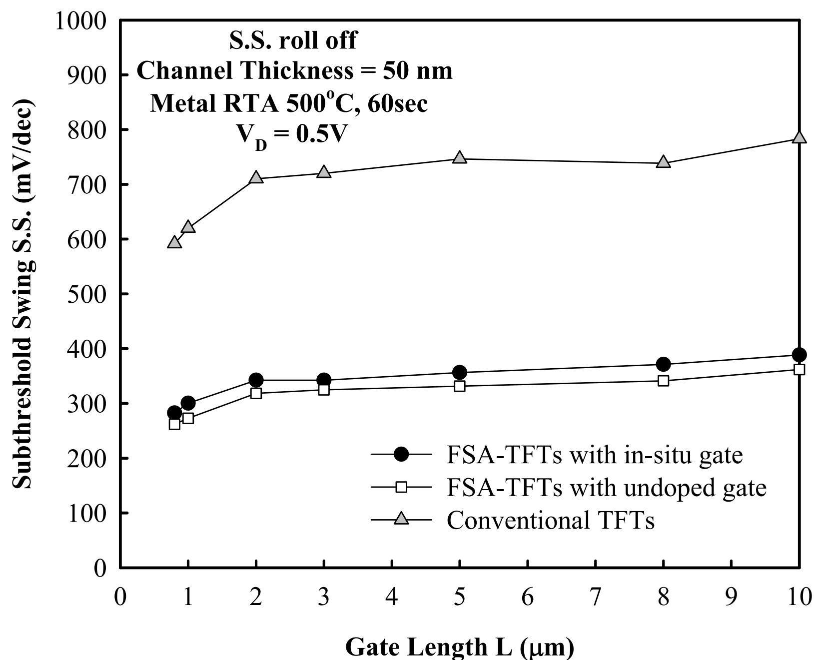


Fig.3-35 Comparison of subthreshold swing roll-off between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage is 0.5V.

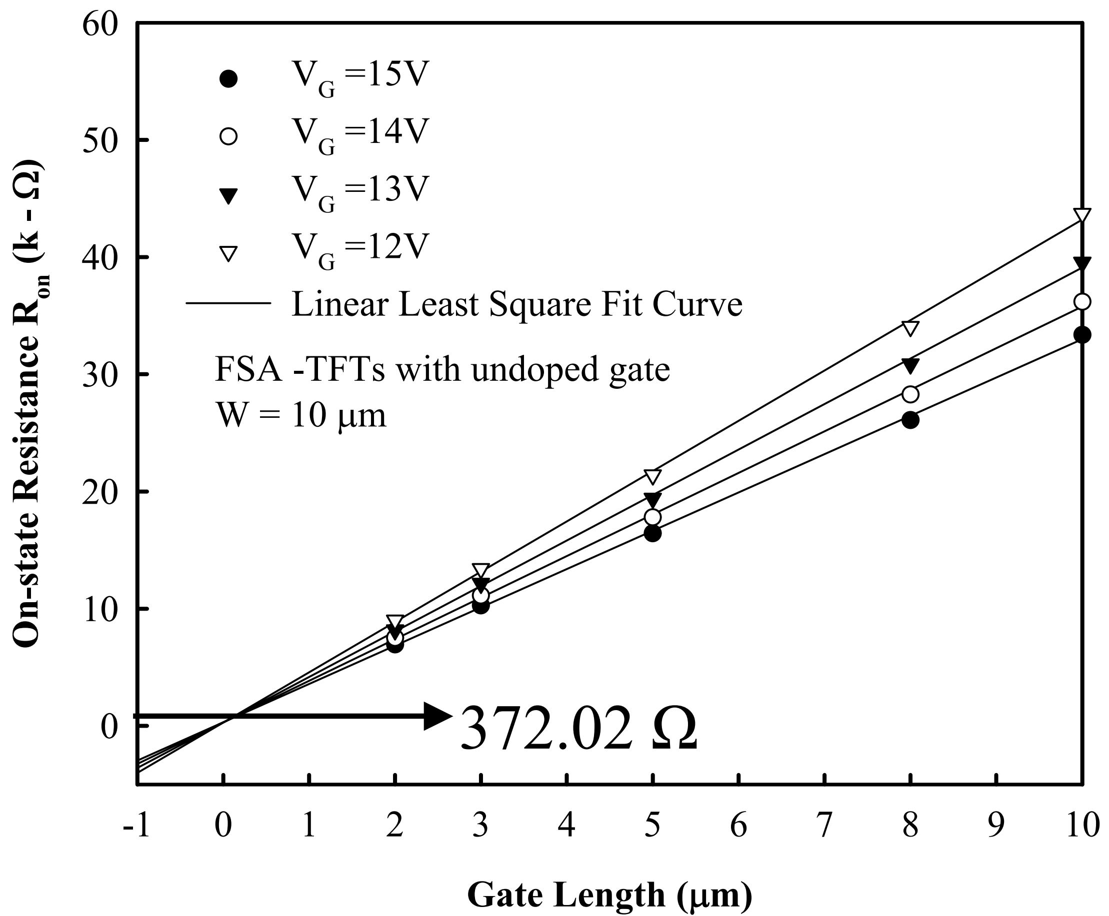


Fig.3-36 Parasitic resistance R_P is extracted by plotting the on-state resistance (R_{on}) versus gate length. FSA-TFTs with undoped gate and Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage is 0.5V.

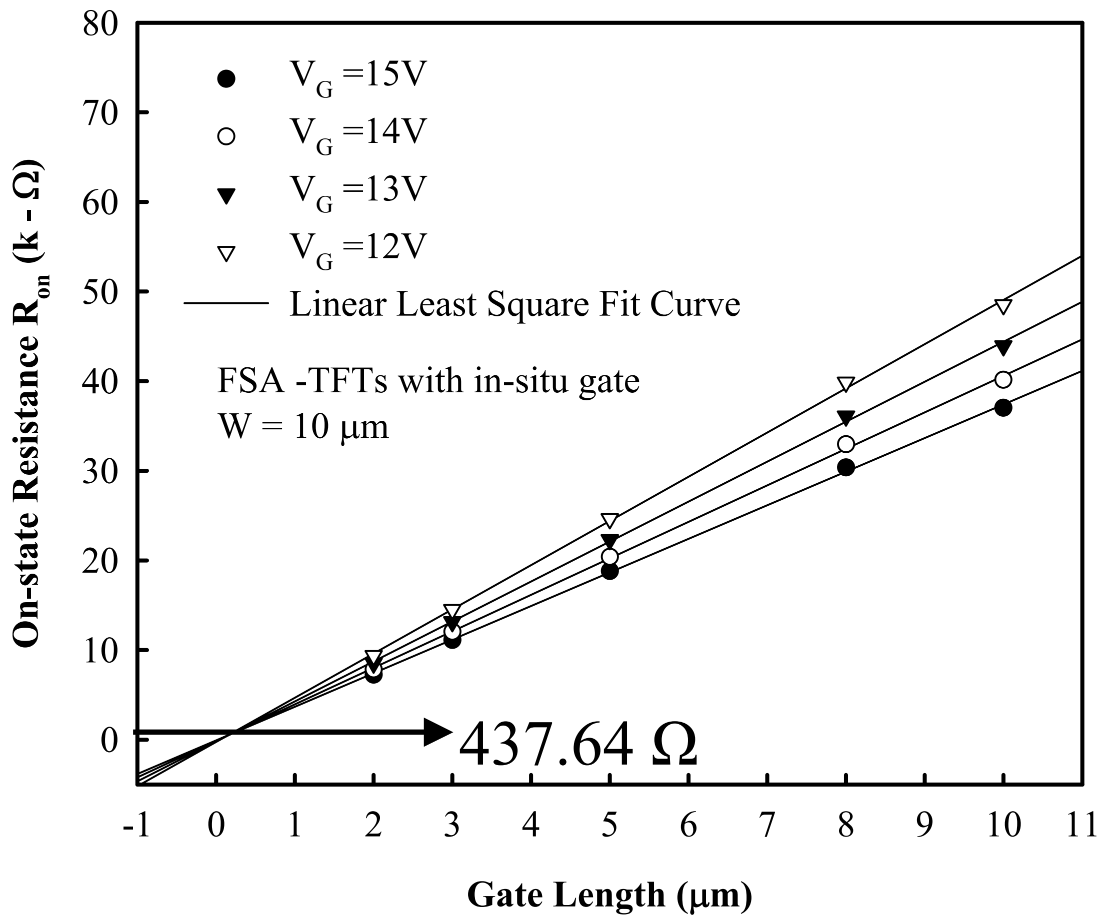


Fig.3-37 Parasitic resistance R_P is extracted by plotting the on-state resistance (R_{on}) versus gate length. FSA-TFTs with in-situ gate and Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage is 0.5V.

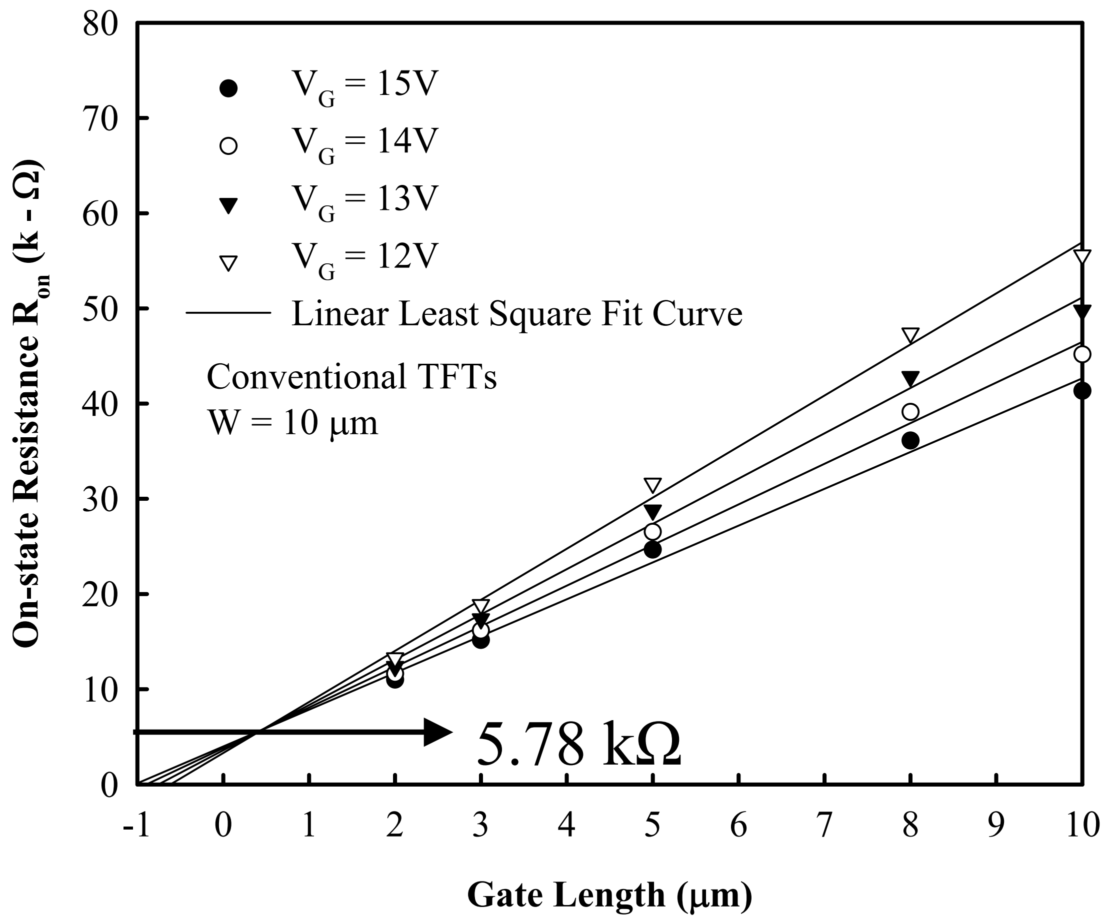


Fig.3-38 Parasitic resistance R_P of conventional TFTs is extracted by plotting the on-state resistance (R_{on}) versus gate length. The channel width is 10μm, and the drain voltage is 0.5V.

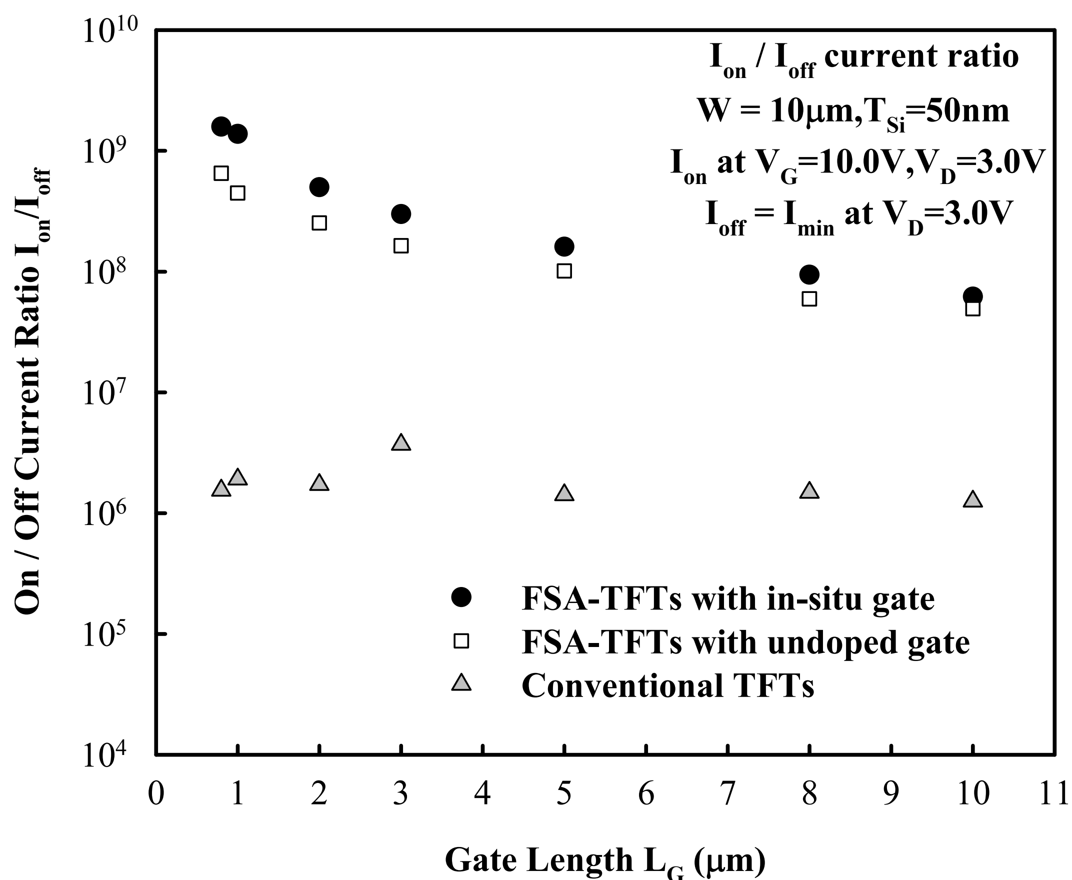


Fig.3-39 Comparison of the On/Off current ratio between n-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. The I_{ON} is measured at V_G=10V and V_D=3.0V. I_{OFF} is equal to minimum current at V_D=3.0V. Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm.

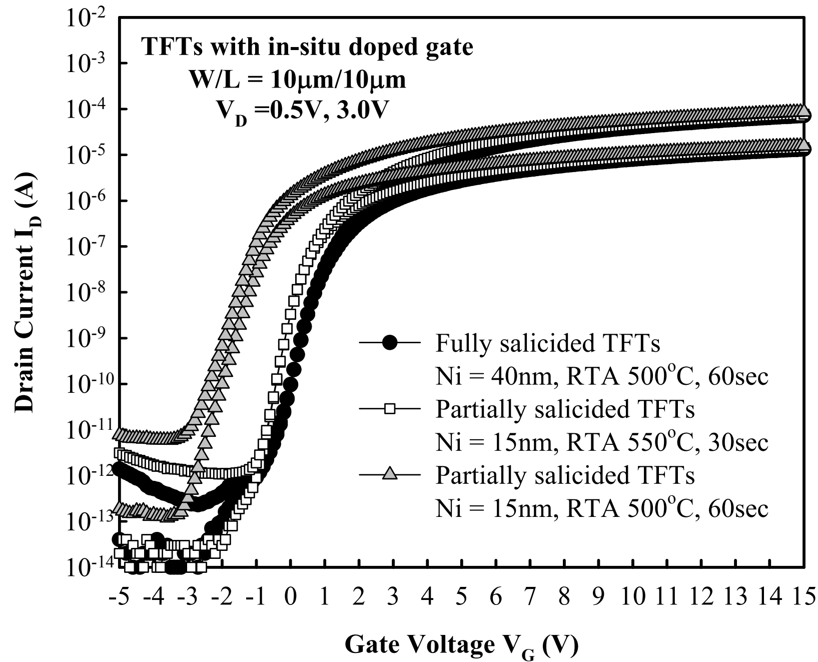


Fig.3-40 Comparison of transfer characteristics between n-channel FSA-TFTs with in-situ gate and partially Ni-salicided TFTs with in-situ gate. Partially Ni-salicided TFTs are defined when Ni thickness is 15nm. W/L=10μm/10μm.

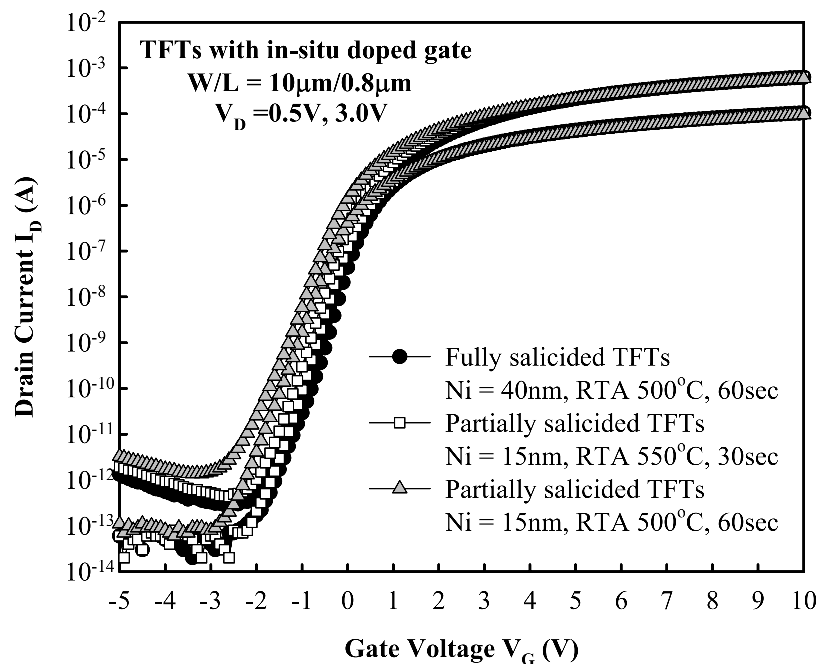


Fig.3-41 Comparison of transfer characteristics between n-channel FSA-TFT with in-situ gate and partially Ni-salicided TFTs with in-situ gate. Partially Ni-salicided TFTs are defined when Ni thickness is 15nm. W/L=10μm/0.8μm.

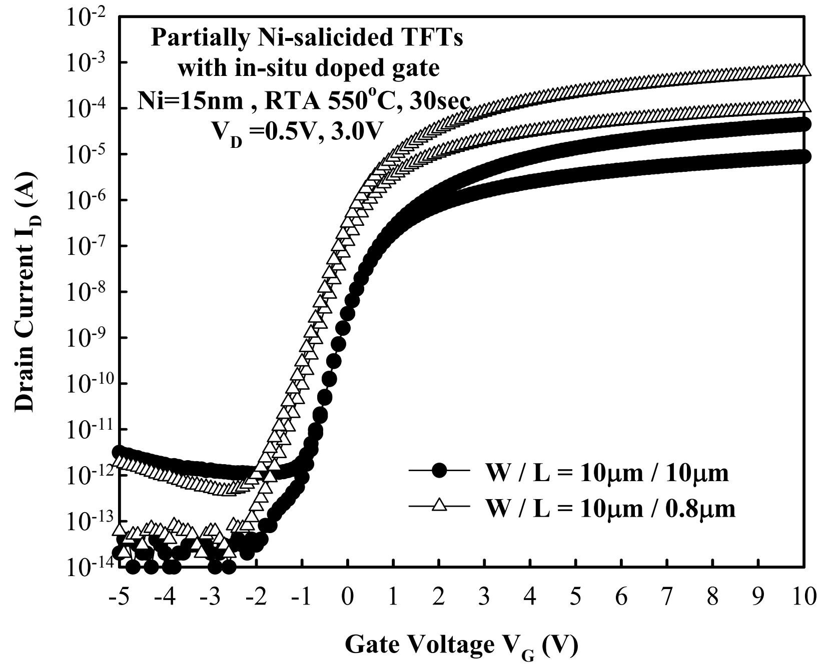


Fig.3-42 Comparison of transfer characteristics between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel partially Ni-salicided TFTs with in-situ doped gate and Ni-salicide was formed by RTA 550°C for 30 seconds.

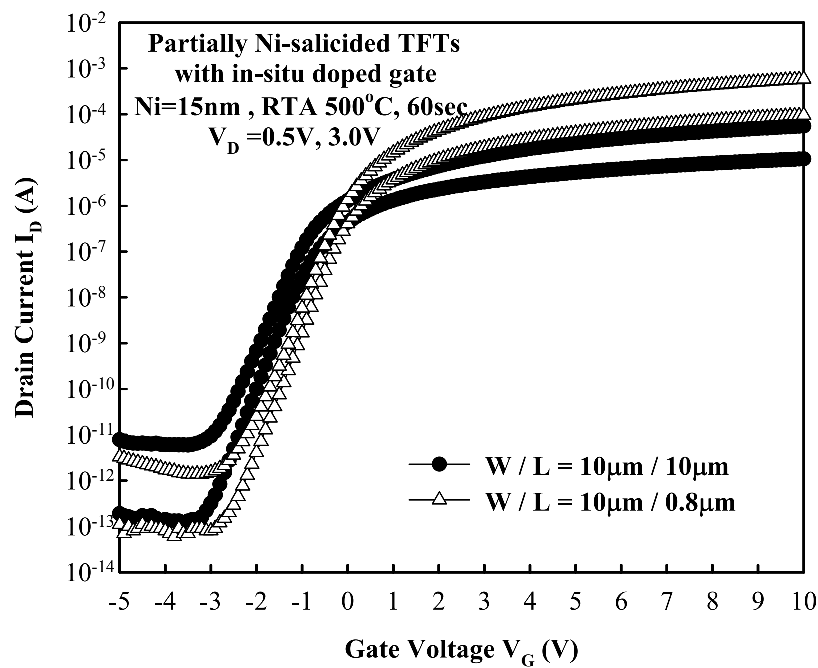


Fig.3-43 Comparison of transfer characteristics between W/L=10μm/10μm and W/L=10μm/0.8μm for n-channel partially Ni-salicided TFTs with in-situ doped gate and Ni-salicide was formed by RTA 500°C for 60 seconds.

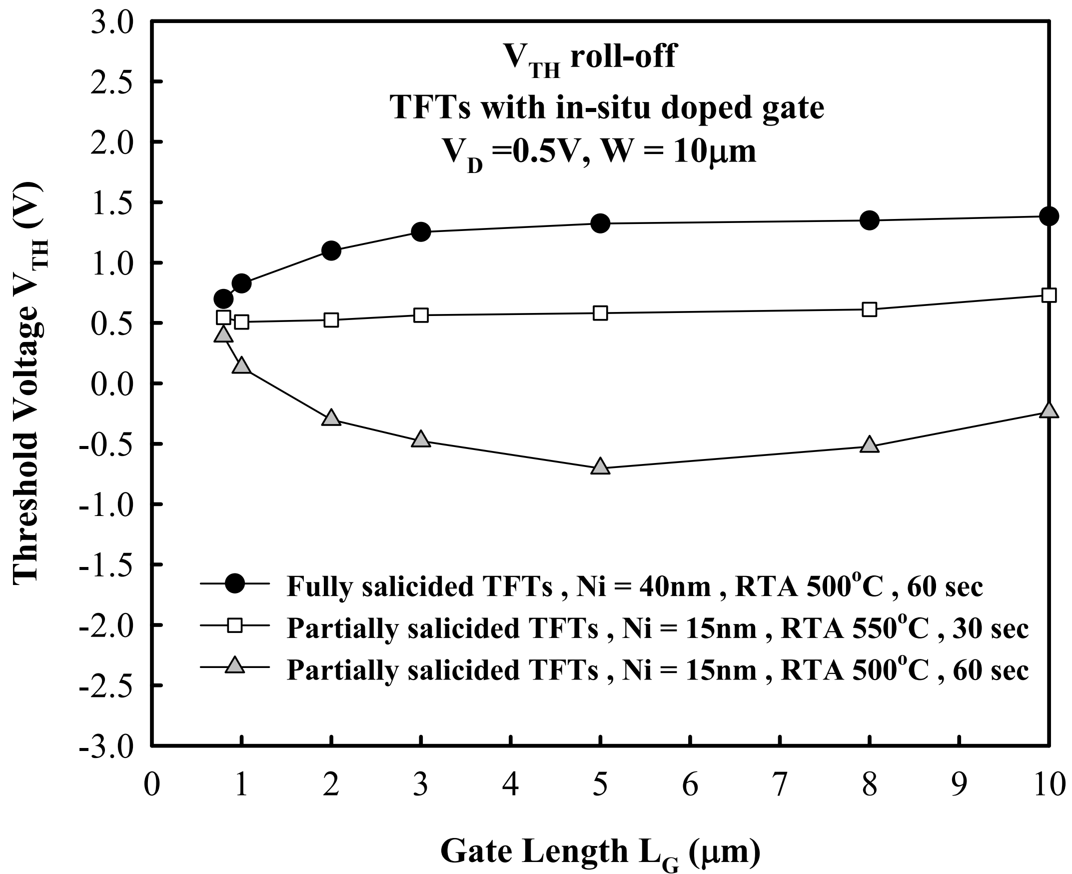


Fig.3-44 Comparison of threshold voltage roll-off between n-channel FSA-TFTs with RTA 500°C for 60 seconds, partially Ni-salicided TFTs with RTA 550°C for 30 seconds, and partially Ni-salicided TFTs with RTA 500°C for 60 seconds. All of them are in-situ doped gate. Partially Ni-salicided TFTs are defined when Ni thickness is 15nm. W=10μm, and V_D=0.5V.

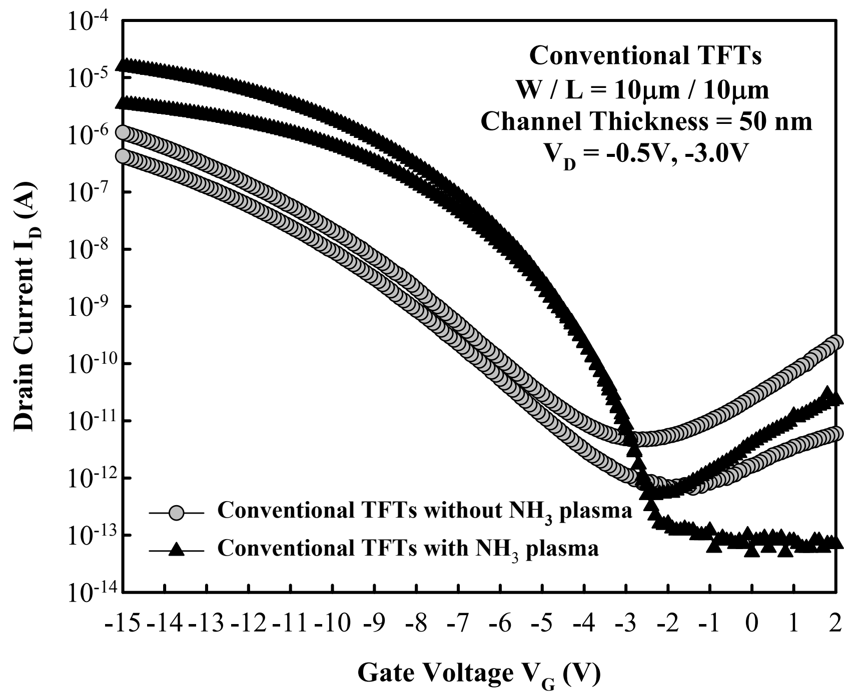


Fig. 3-45 Transfer characteristics of conventional TFTs with W/L=10μm/10μm, and two different treatment steps for p-channel.

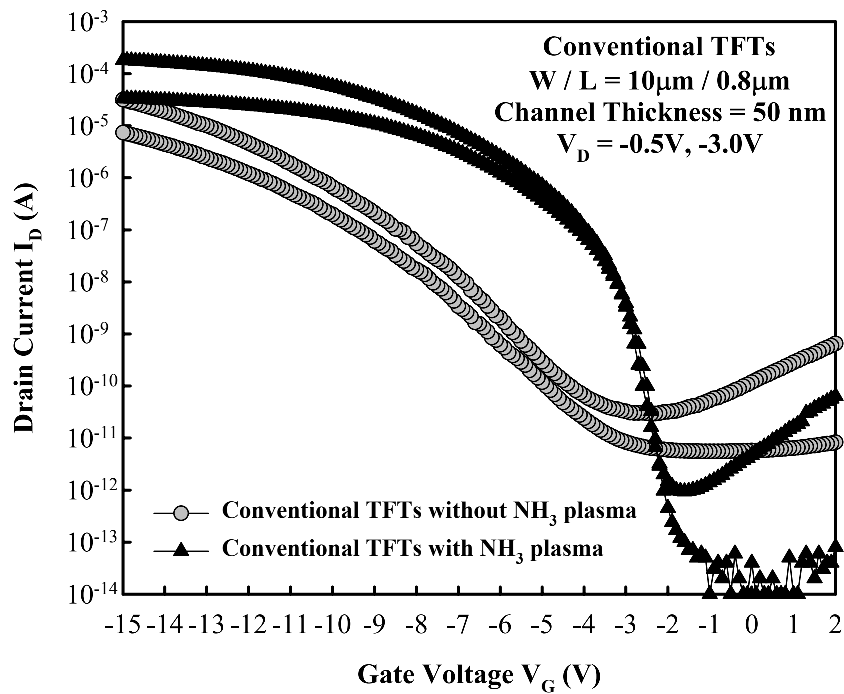


Fig. 3-46 Transfer characteristics of conventional TFTs with W/L=10μm/0.8μm, and two different treatment steps for p-channel.

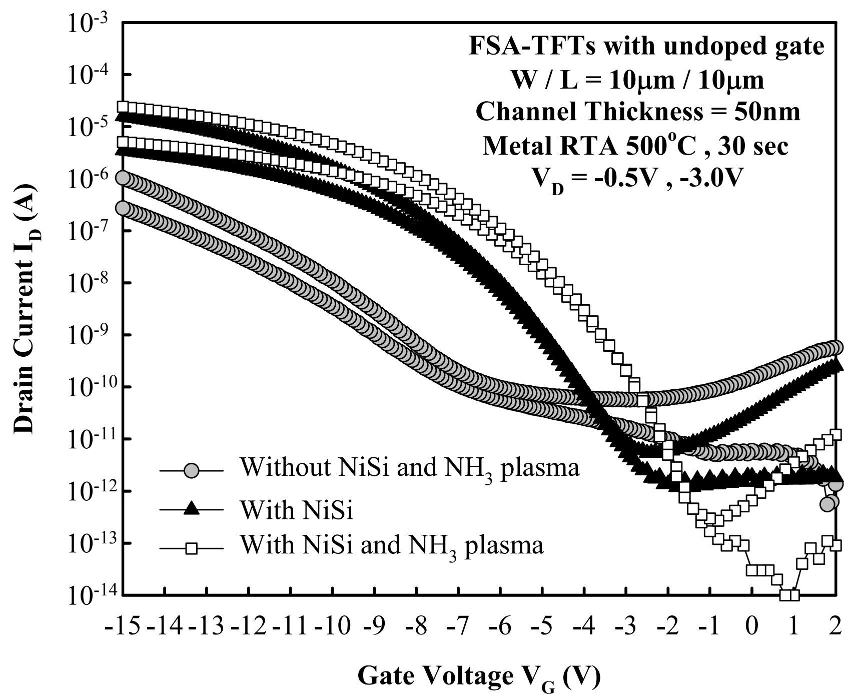


Fig.3-47 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/10μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

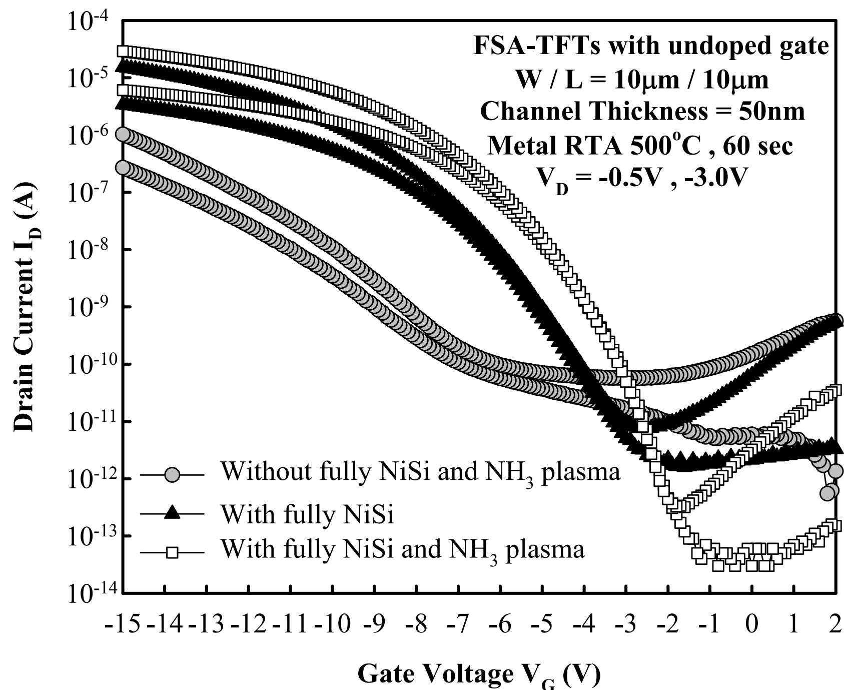


Fig.3-48 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/10μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

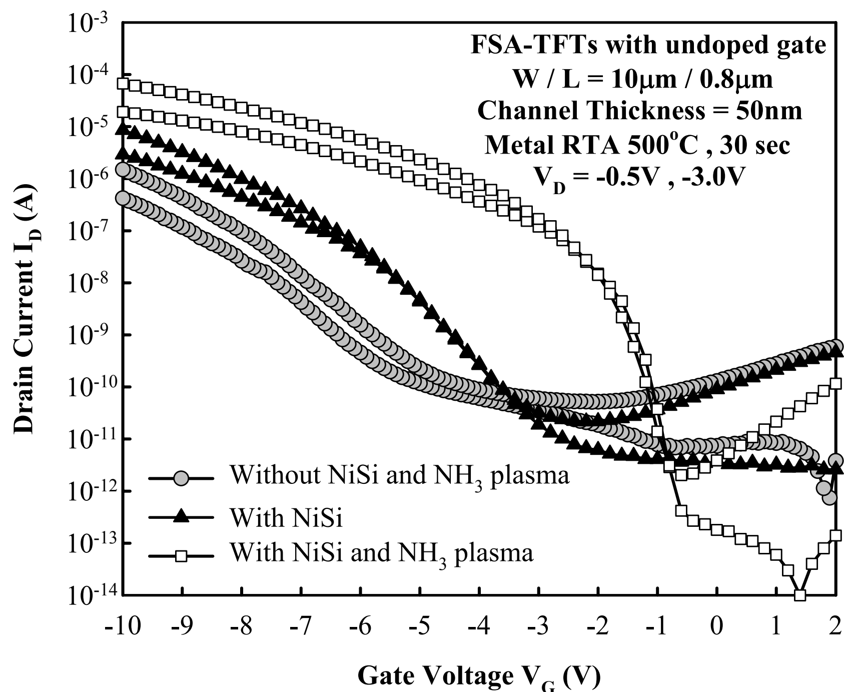


Fig.3-49 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/0.8μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 30 seconds.

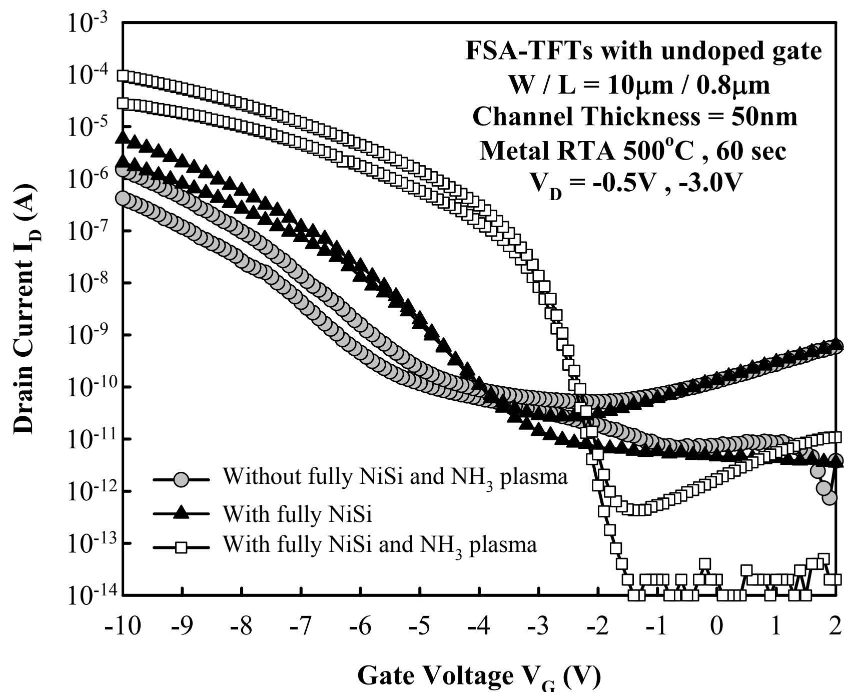


Fig.3-50 Transfer characteristics of FSA-TFTs with undoped gate, W/L=10μm/0.8μm, and three different treatment steps for p-channel. Ni-salicide was formed by RTA 500°C for 60 seconds.

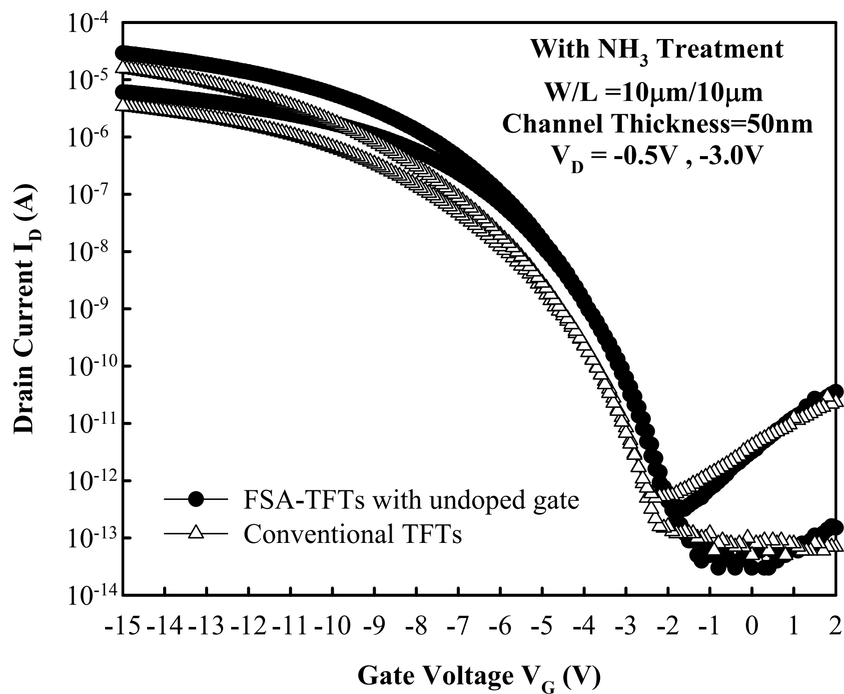


Fig. 3-51 Transfer characteristics of p-channel FSA-TFTs with undoped gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

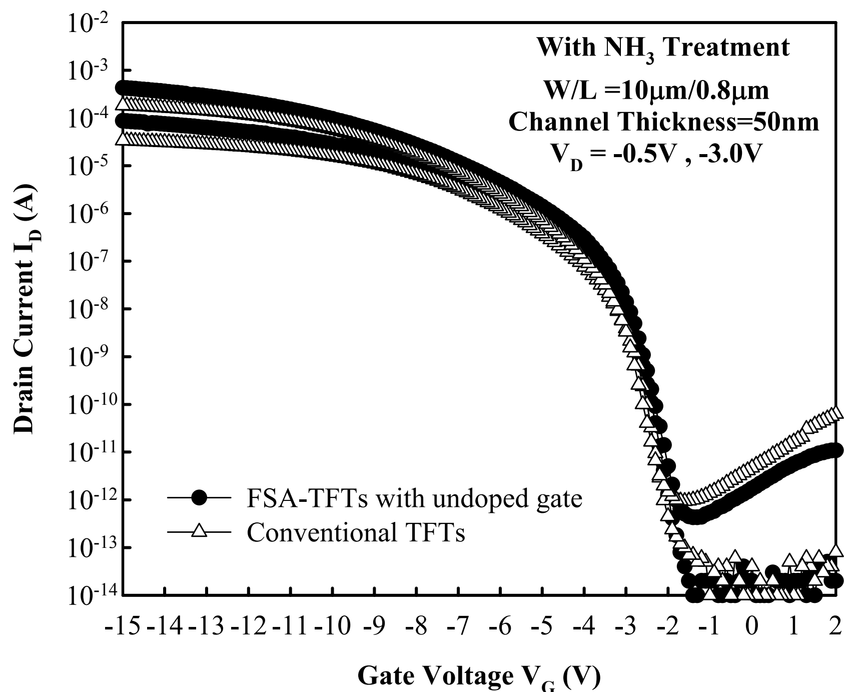


Fig. 3-52 Transfer characteristics of p-channel FSA-TFTs with undoped gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

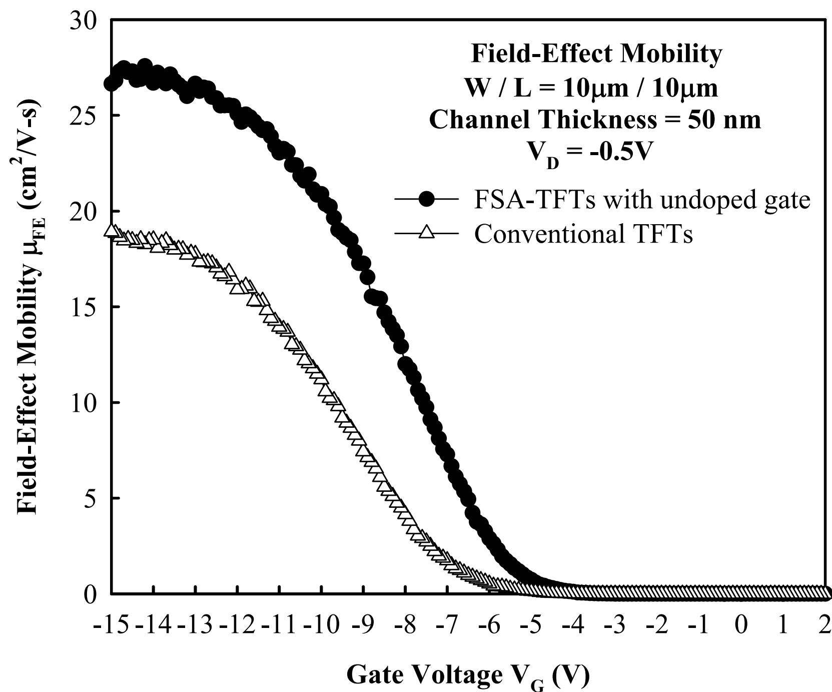


Fig.3-53 Field-effect mobility of p-channel FSA-TFTs with undoped gate, and W/L=10μm/10μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

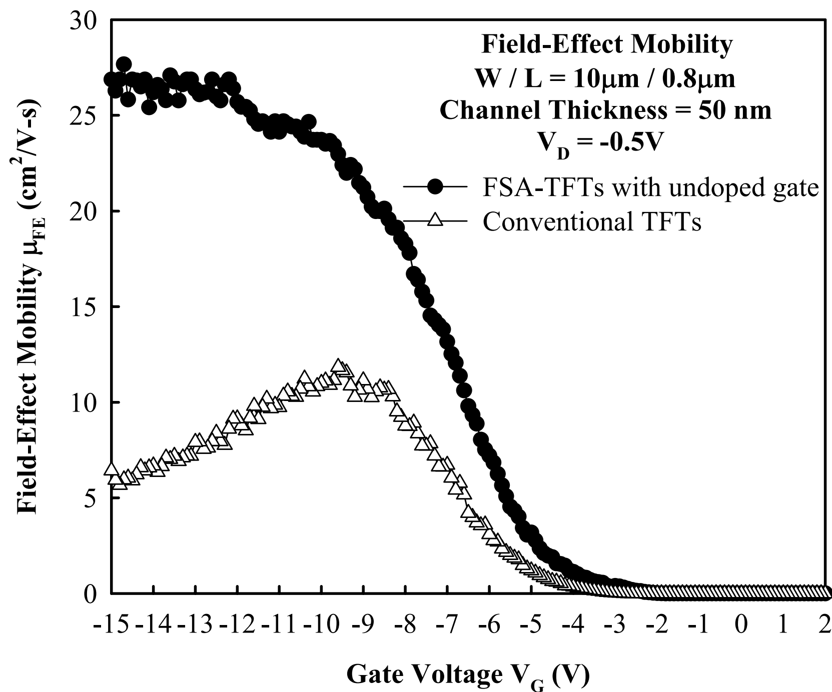


Fig.3-54 Field-effect mobility of p-channel FSA-TFTs with undoped gate, and W/L=10μm/0.8μm compare with conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds.

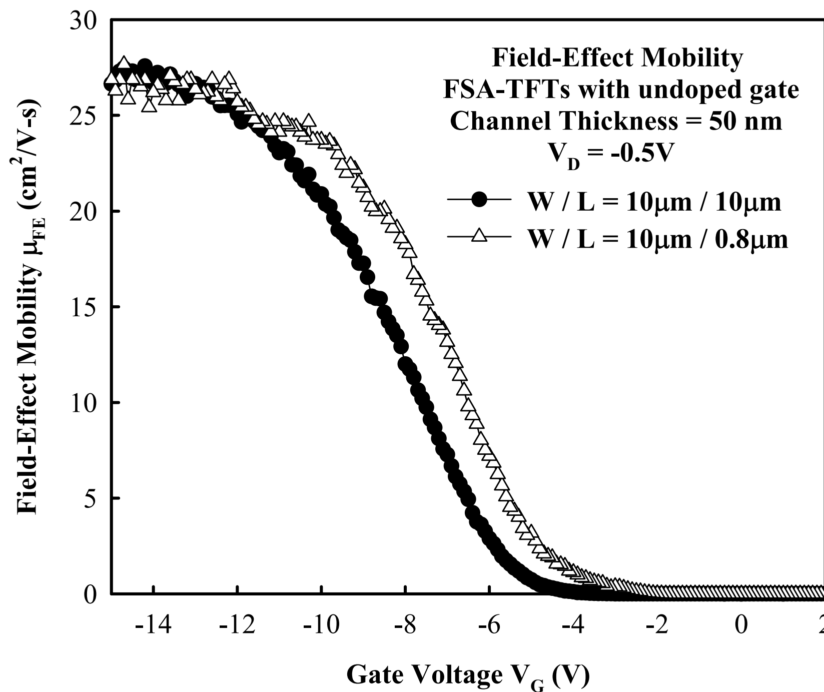


Fig. 3-55 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for p-channel FSA-TFTs with undoped gate. Ni-salicide was formed by RTA 500°C for 60 seconds.

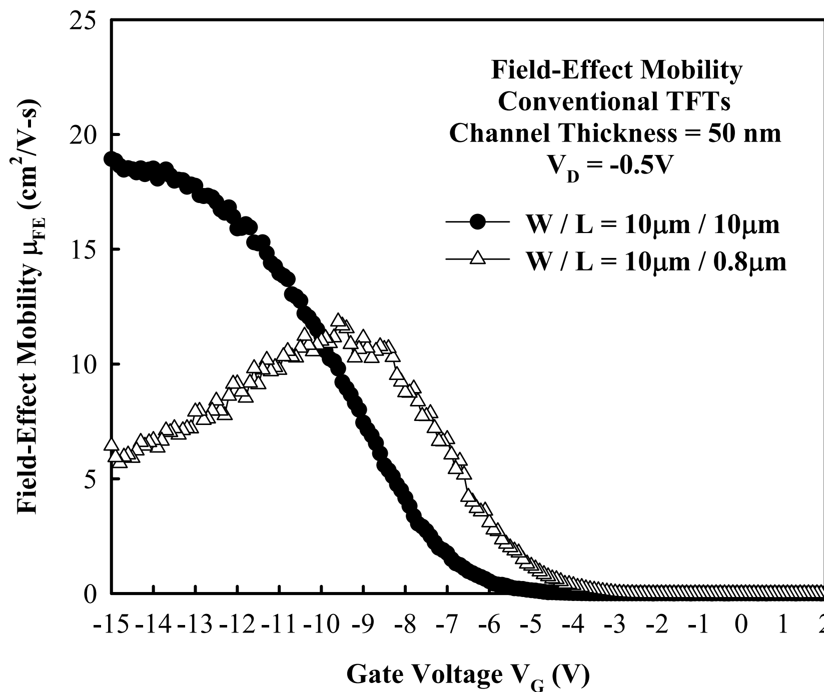


Fig. 3-56 Comparison of field-effect mobility between W/L=10μm/10μm and W/L=10μm/0.8μm for p-channel conventional TFTs.

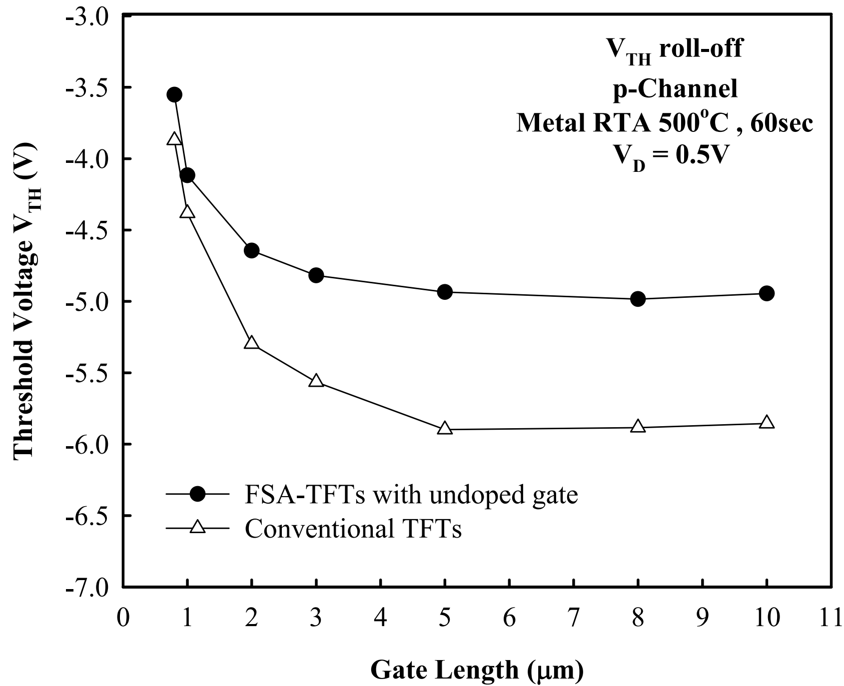


Fig.3-57 Comparison of threshold voltage roll-off between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W=10μm, and V_D=0.5V.

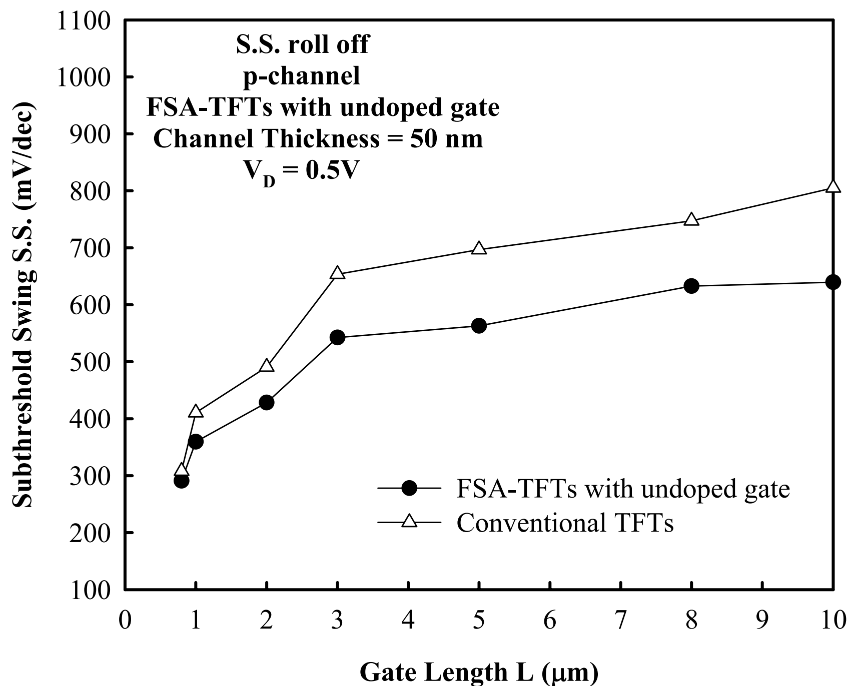


Fig.3-58 Comparison of subthreshold swing roll-off between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W=10μm, and V_D=0.5V.

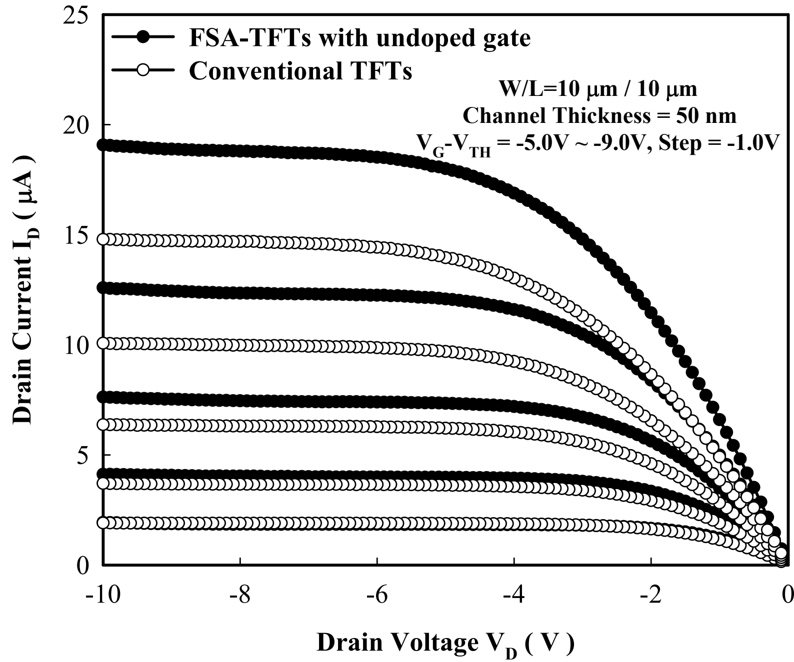


Fig. 3-59 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/10μm, and V_G-V_{TH}=-5.0V, -6.0V, -7.0V, -8.0V, -9.0V.

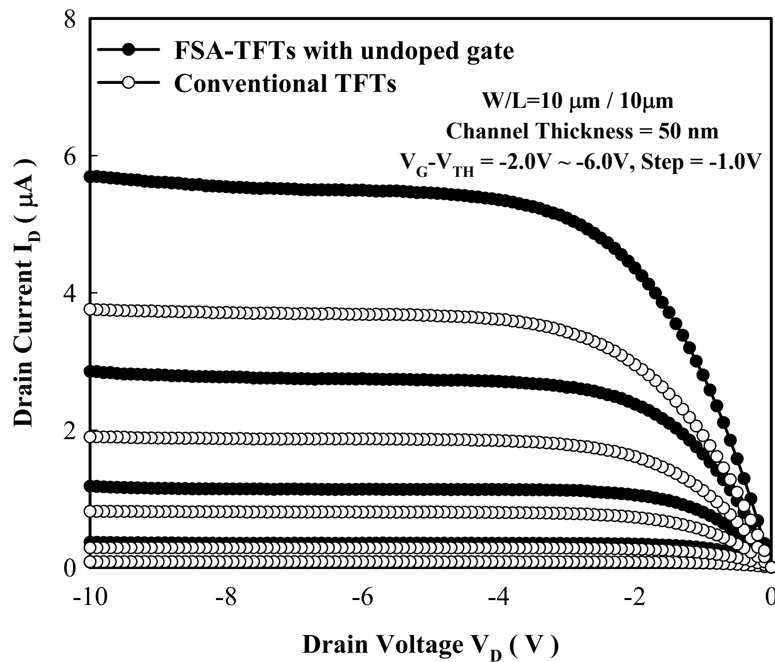


Fig. 3-60 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/10μm, and V_G-V_{TH}=-2.0V, -3.0V, -4.0V, -5.0V, -6.0V.

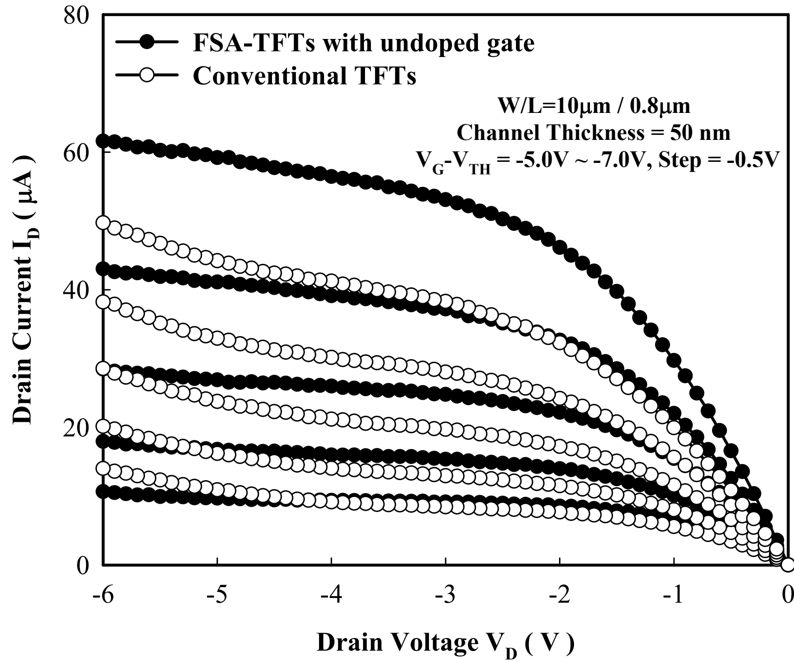


Fig. 3-61 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_G-V_{TH}=-5.0V, -5.5V, -6.0V, -6.5V, -7.0V.

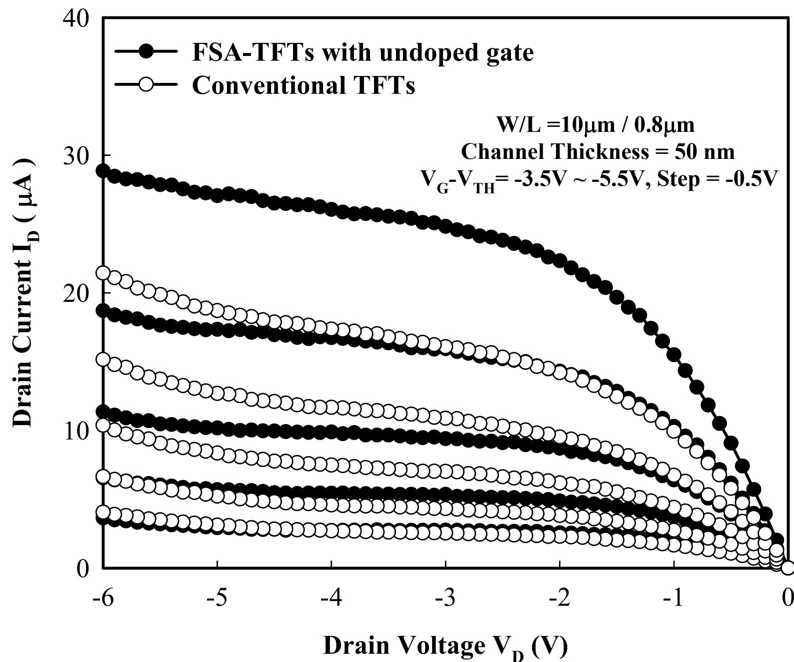


Fig. 3-62 Comparison of output characteristics between p-channel FSA-TFTs with undoped gate, and conventional TFTs. Ni-salicide was formed by RTA 500°C for 60 seconds. W/L=10μm/0.8μm, and V_G-V_{TH}=-3.5V, -4.0V, -4.5V, -5.0V, -5.5V.

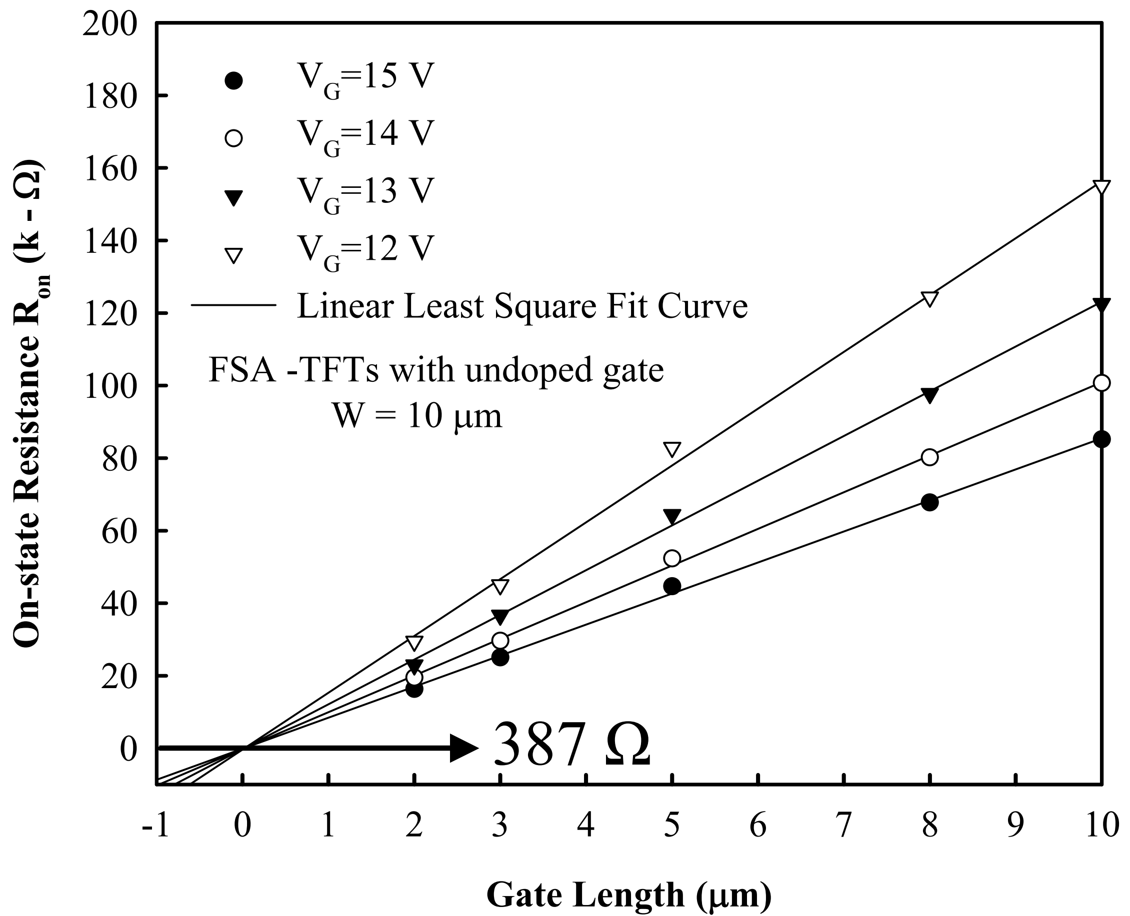


Fig.3-63 Parasitic resistance R_P is extracted by plotting the on-state resistance (R_{on}) versus gate length. FSA-TFTs with undoped gate and Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm, and the drain voltage is 0.5V.

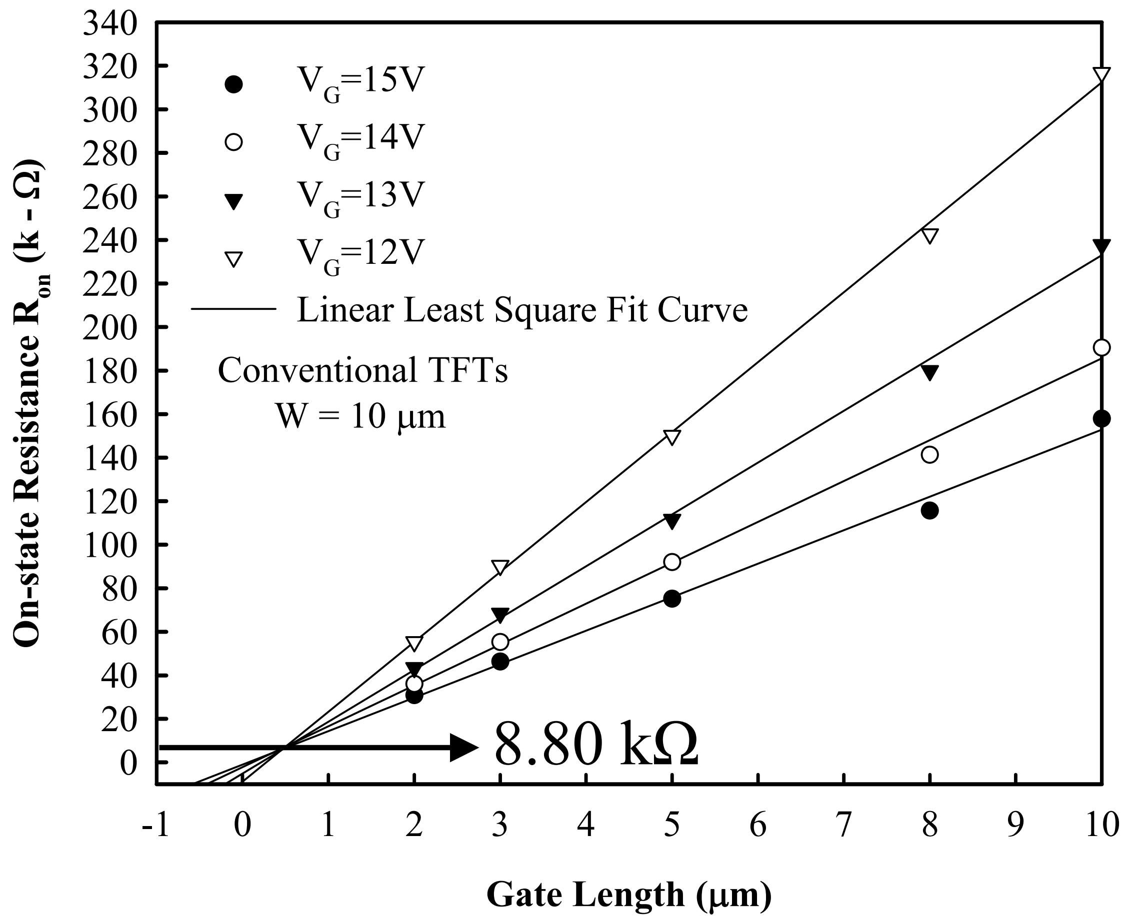


Fig.3-64 Parasitic resistance R_P of conventional TFTs is extracted by plotting the on-state resistance (R_{on}) versus gate length. The channel width is 10μm, and the drain voltage is 0.5V.

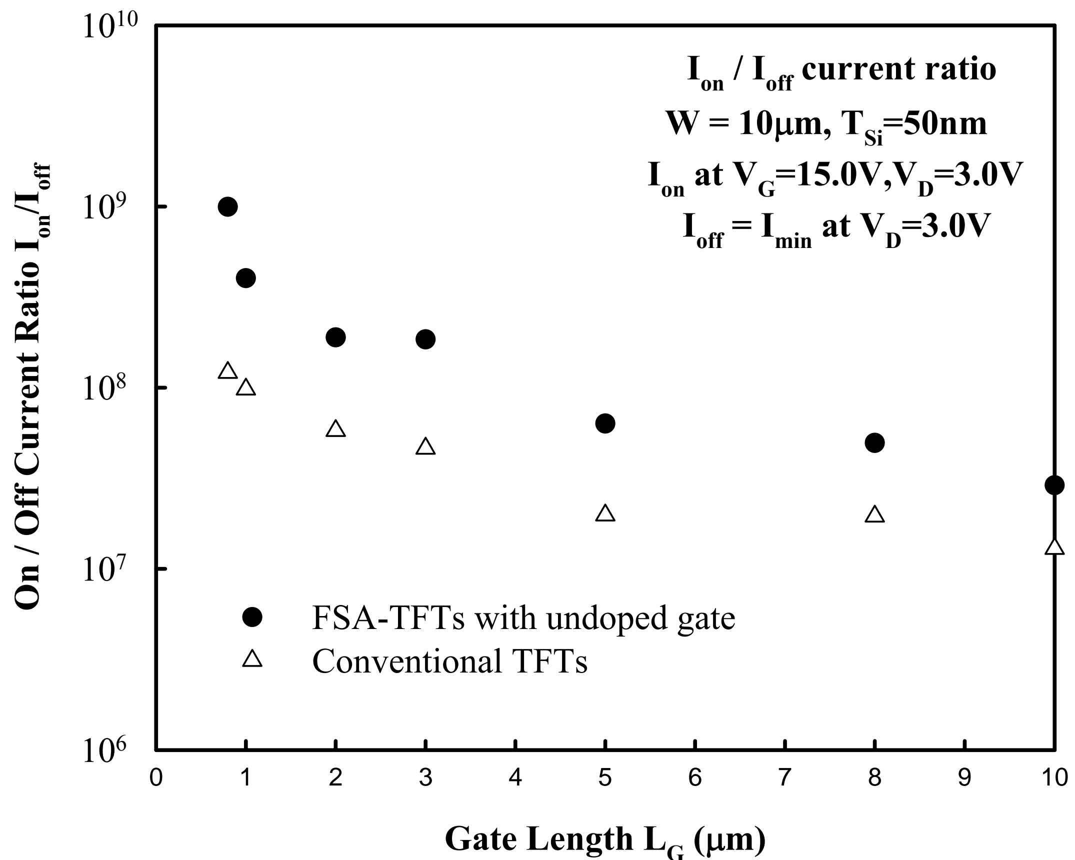


Fig.3-65 Comparison of the On/Off current ratio between p-channel FSA-TFTs with in-situ doped gate, undoped gate, and conventional TFTs. The I_{ON} is measured at V_G=15V and V_D=3.0V. I_{OFF} is equal to minimum current at V_D=3.0V. Ni-salicide was formed by RTA 500°C for 60 seconds. The channel width is 10μm.

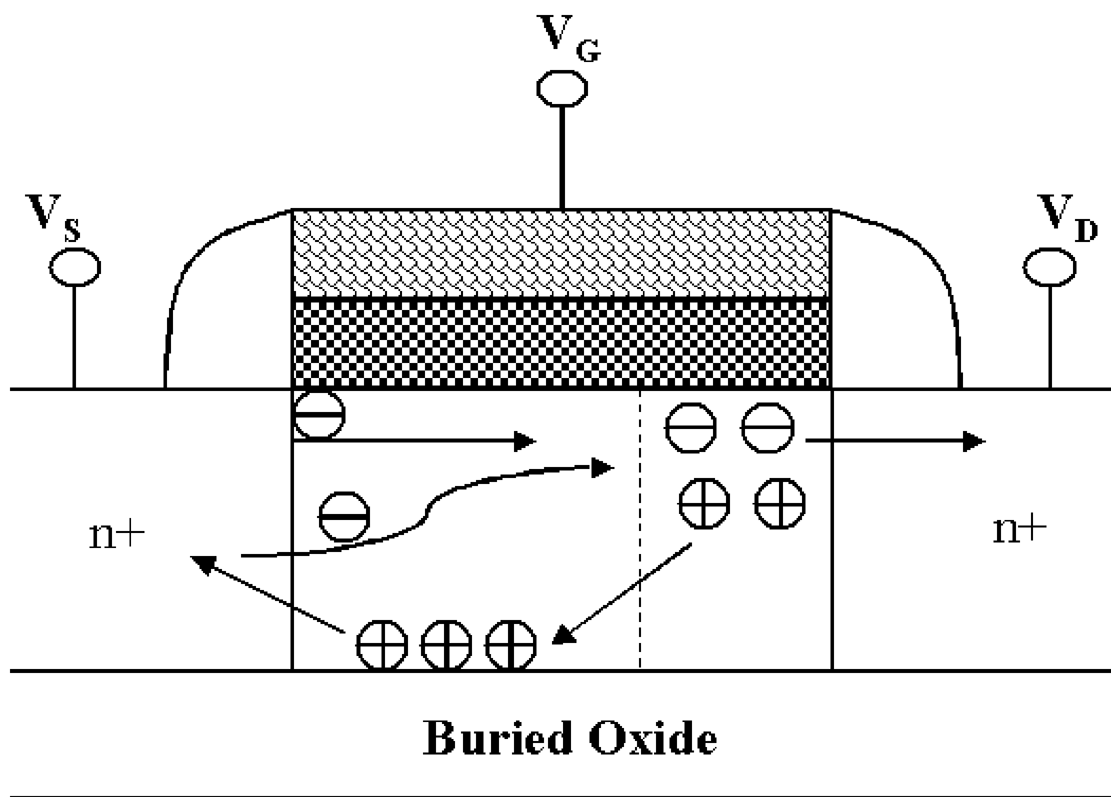


Fig.3-66 The floating-body effect in Poly-Si TFTs.

Chapter 4

Conclusions and Future Works

4.1 Conclusions

In this thesis, we have successfully fabricated FSA-TFTs. Moreover, we have investigated the basic electrical characteristics of n-channel and p-channel poly-Si TFTs with fully Ni-salicided S/D and gate structure. We select material of Nickel to from Ni-salicide. Besides its low resistance, NiSi also has some advantages. For example, NiSi does not have narrow line effect, NiSi has the less silicon consumption compare with $TiSi_2$ and $CoSi_2$, and silicidation can be formed at low temperature (400°C~600°C) without agglomeration.

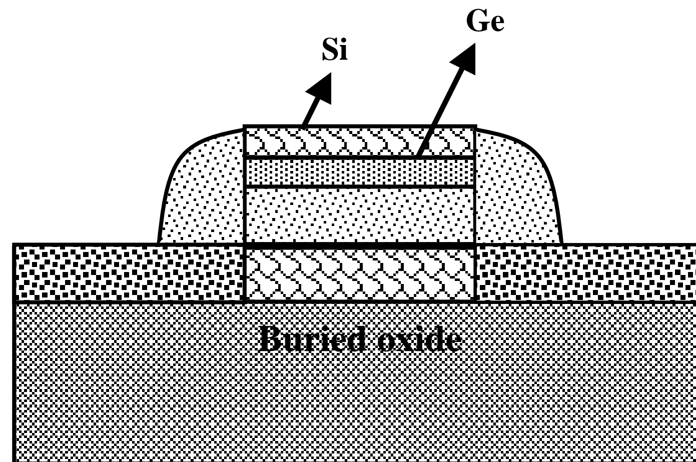
The fully Ni-salicided S/D and gate can be formed by one step RTA 500°C for 30 seconds or RTA 500°C for 60 seconds. In addition, we also fabricated partially Ni-salicided S/D and gate by one step RTA 550°C for 30 seconds or RTA 500°C for 60 seconds in order to compare with FSA-TFTs. We have found that the FSA-TFTs with RTA 500°C for 60 seconds have excellent performance in this study. This is because of Poly-Si TFTs with fully Ni-salicided S/D structure can drastically decrease the parasitic resistance and passivate the defects of S/D junction. Furthermore, Poly-Si TFTs with fully Ni-salicided gate structure can obtain the better value of C_{OX}. So, FSA-TFTs have perfect electrical characteristics as higher ON current, lower OFF current, higher field-effect mobility, stable V_{TH}, alleviated V_{TH} roll-off, improved subthreshold swing, increased breakdown voltage, and increased ON/OFF current ratio for n-channel and p-channel Poly-Si TFTs. We also have investigated the influence of RTA temperature and time. Specially, from comparison of influence of RTA temperature and time, we have found that the size of spacer is a critical point. In other words, the size of spacer must balance with lateral diffusion of NiSi.

Finally, it is demonstrated that fully Ni-salicidation is a promising technology to solve

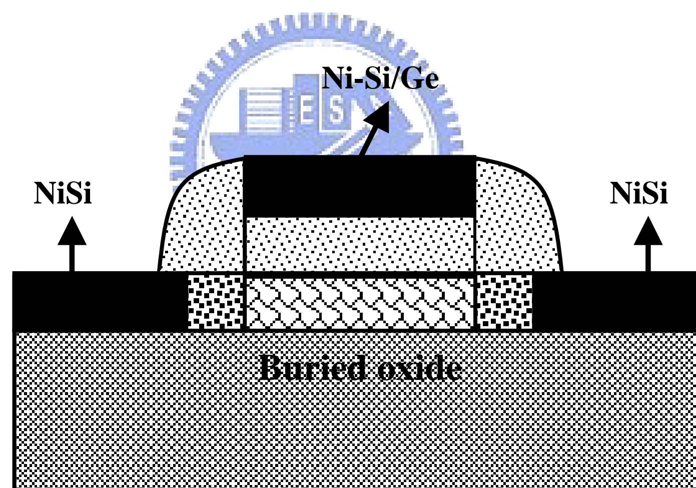
some problems in this study. FSA-TFTs can effectively suppress the floating-body effect and parasitic bipolar junction transistor action compared with conventional TFTs. Experimental results show that the FSA-TFTs give lower off-state leakage current, and better I_D-V_D output characteristics compared with conventional TFTs. The characteristics of the FSA-TFTs are suitable for high performance TFTs with a stable threshold voltage and large breakdown voltage.

4.2 Future Works

There are some interesting and important topics that are valuable for the future works. For example, we can investigate different materials of gate such as FSA-TFTs with stacked Si/Ge gate and Si/Ge T-gate structure, etc. Their structures are shown in Fig.4-1 and Fig.4-2. These different materials of gate have different value of work function and V_{TH}, and have larger field-effect mobility as well as lower subthreshold swing. In addition, Si/Ge T-gate structure can effectively decrease intensity of electric field at drain side, which makes gate induce drain leakage current (GIDL) be suppressed.

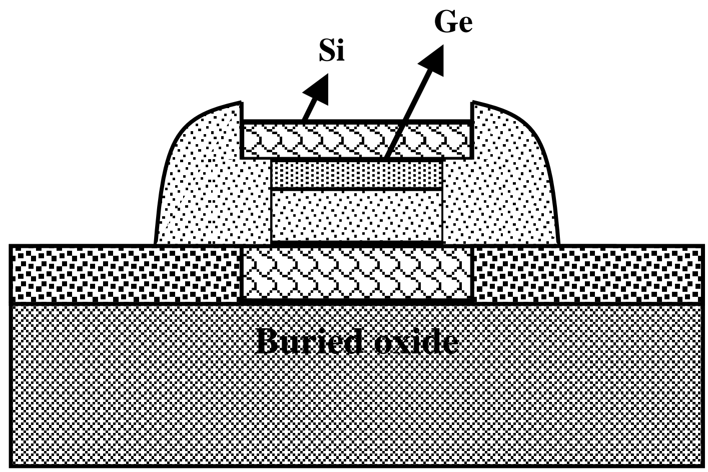


(a) Si/Ge stack gate

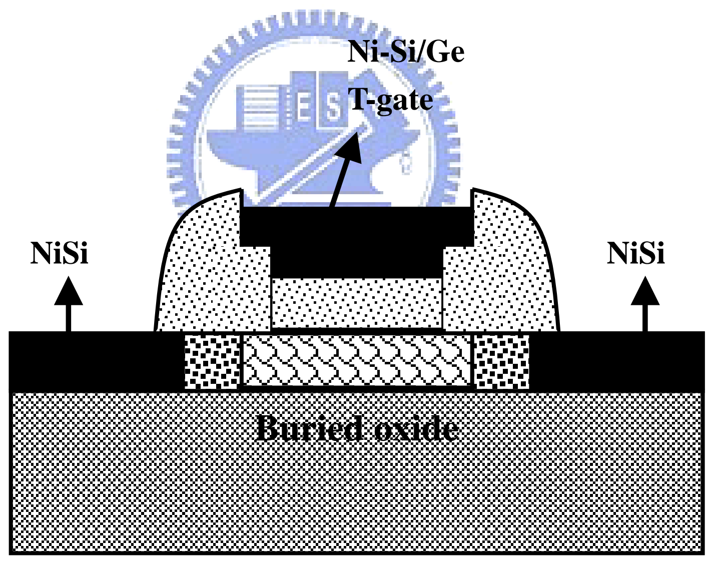


(b) Ni-salicided with Si/Ge stack gate

Fig.4-1 (a) Si/Ge stack gate without Ni-salicied process and (b) Si/Ge stack gate with Ni-salicied process.



(a) Si/Ge T-gate



(b) Ni-salicided with Si/Ge T-gate

Fig.4-2 (a) Si/Ge T-gate without Ni-salicied process and (b) Si/Ge T-gate with Ni-salicied process.

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簡　　歷

姓名：黃 彥 學

性別：男

生日：12 / 31 / 1981

出生地：台北市

學歷：國立交通大學電子物理研究所碩士班

　　　國立中央大學物理學系

論文題目：

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指導教授：趙 天 生 博士