國立交通大學

電子物理學系

博士論文

氧化鉿閘極介電層之氟鈍化製程與應力工程的研究

Study on Fluorine Passivation Techniques and Strain Engineering for HfO_2 Gate Dielectrics

研究生：吳偉成

指導教授：趙天生　　教授

賴朝松　　教授

中華民國九十七年三月

氧化鉿閘極介電層之氟鈍化製程與應力工程的研究

Study on Fluorine Passivation Techniques and Strain Engineering for HfO_2 Gate Dielectrics

研 究 生： 吳偉成　　Student：Woei-Cherng Wu

指導教授： 趙天生　　Advisor：Tien-Sheng Chao

賴朝松　　Chao-Sung Lai

國 立 交 通 大 學

電子物理學系

博 士 論 文

A Dissertation
Submitted to Department of Electrophysics
College of Science
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electrophysics

March 2008
Hsinchu, Taiwan, Republic of China

中華民國 九十七 年 三 月

氧化鉿閘極介電層之氟鈍化製程與應力工程的研究

學生：吳偉成　　指導教授：趙 天 生 博士

賴 朝 松 博士

國 立 交 通 大 學　電 子 物 理 學 系 博 士 班

摘要

首先，我們提出多種氟鈍化(passivatation)技術以製作高效能且高可靠度的二氧化鉿閘極絕緣層(HfO_2 gate dielectrics)。接著研究經過氟化之氧化鉿其電流穿遂機制(current transportation mechanism)與載子捕捉(charge trapping)特性。最後，我們發現氮化矽所引發的應力(strain)矽通道之氧化鉿電晶體，其可靠度以及元件特性都獲得大幅度的改善

一開始我們提出了以矽表面氟離子植入法(silicon surface fluorine implantation)，將氟離子導入二氧化鉿薄膜以及此二氧化鉿薄膜與矽基板之介面處。從實驗結果可以充分證明此氟化二氧化鉿薄膜會擁有較好的熱穩定性，此氟化二氧化鉿薄膜的漏電流會比一般傳統的二氧化鉿還低了三個數量級，此外，應力下所導致的漏電流(stress-induced leakage current)以及電荷捕捉(charge trapping)的問題都可以藉由此氟離子佈值法來使得此二氧化鉿閘極介電層有更好的特性。此氟原子與二氧化鉿薄膜混合不僅僅可以減少介面狀態的懸空鍵結(interface dangling bond)還可以有效減少此薄膜層的電荷捕捉情形，而進一步的有效改善二氧化鉿薄膜的特性。另一方面，我們進一步研究氟化氧化鉿閘極介電層其電流傳導機制。我們利用變溫量測的漏電流變化以及低溫(77 K)量測的漏電流來分析電流傳導特性以及此電容元件的能帶圖(energy band diagrams)，從實驗結果中可以發現氟化介面層與矽基板的傳導帶落差(conduction band offset)有3.2 eV而傳統介面層的落差則只有2.7 eV；氟化二氧化鉿與金屬閘極的傳導帶落差有2.6 eV而傳統二氧化鉿的落差則只有1.9 eV；不論是閘極注入(gate injection)模式或基板注入(substrate injection)模式操作，氟化二氧化鉿的有效載子捕捉深度大約是低於介電

層傳導帶1.25 eV，而傳統的二氧化鉿在閘極注入模式下的有效載子捕捉深度大約是低於介電層傳導帶1.04 eV，而在基板注入模式下的有效載子捕捉深度大約是低於介電層傳導帶1.11 eV。

此外，我們提出與現有製程具高度匹配性的四氟化碳電漿處理(CF_4 plasma treatment)技術，用以製作高效能的二氧化鉿閘極絕緣層之電容。此技術可分類成兩種：首先藉由前處理的技術，我們可以有效的抑制高介電閘極絕緣層電容中的介面層(interfacial layer)生長，藉此得到更薄的等效氧化層厚度(effective oxide thickness)，除此之外，還可以有效的抑制矽化鉿的形成並產生鉿-氟鍵結(Hf-F bonding)。接著利用四氟化碳電漿後處理的技術，氟原子可以有效地被導入二氧化鉿薄膜以及此二氧化鉿薄膜與矽基板之介面以消除薄膜中的載子補獲態(trap states)，並進而有效地改善此閘極絕緣層的介面特性。經由四氟化碳電漿處理的二氧化鉿閘極絕緣層之電容具有較低的漏電流、高的崩潰電壓及較薄的等效氧化層厚度(effective oxide thickness)；其磁滯現象(hysteresis)更大幅改善了超過 90 %。此外，我們更進一步提出物理模型來解釋此磁滯效應的改善機制。

接著我們提出新穎之氟化氧化鉿電晶體，利用四氟化碳電漿處理，可同時改善n型及p型氧化鉿電晶體，相當適用於新型互補式金氧半場效電晶體的製作。此電晶體有相當高水準的表現及可靠度：高達6.69×10^7的導通電流與關閉電流之比例、 接近76 mV/dec的次臨界擺幅、小於20 mV的源極引發能障衰退以及相當高的載子遷移率(~165 $cm^2/V\cdot s$)。此氟化氧化鉿電晶體有較佳的介面特性及品質較好的絕緣層：較小的閘極引發汲極漏電流(gate induced drain leakage)以及較低的正偏壓溫度所引起的元件不穩定性。而造成此特性及可靠度改善的原因是來自於氟原子導入二氧化鉿薄膜以及此二氧化鉿薄膜與矽基板之介面，進一步減少介電層的缺陷且抑制電子電洞對的產生，並導致絕緣層有較深的載子捕捉位置及減少載子捕捉情形的發生。

最後，我們首度對於氮化矽所引發的應變矽通道之氧化鉿電晶體提出新的發現，可靠度以及元件特性都獲得大幅度的改善，此外，我們利用脈衝型量測系統去分析此氧化鉿電晶體接近真實的特性，發現有百分之九十的驅動電流增加以及百分之五十的轉移電導的提升。而此應變矽通道的氧化鉿電晶體會擁有較佳的介面特性以及較低的正偏壓溫度所引起的元件不穩定性，其元件的充電電流泵(charge pumping current)有大約百分之九十的減少且正偏壓溫度所引起的元件不穩定性效應也降低了百分之五十五。之後我們利用動態臨限電壓(dynamic threshold)操作法來提升應變矽通道的氧化鉿電晶體的元件特性，發現轉移電導有高達百分之一百三十五的增加，且次臨界擺幅有接近理想的表現(~62 $cm^2/V\cdot s$)，在元件特性獲得大幅提升的同時，其可靠度亦維持可容忍的劣化表現。

Study on Fluorine Passivation Techniques and Strain Engineering for HfO_2 Gate Dielectrics

Student: Woei Cherng Wu Advisor: Dr. Tien-Sheng Chao

Dr. Chao-Sung Lai

Department of Electrophysics, National Chiao Tung University

Abstract

First, we demonstrated several fluorine passivation technologies to fabricate high performance and highly reliable HfO_2 gate dielectrics. Then, we investigated the current transportation and charge trapping mechanism of fluorinated HfO_2 gate dielectrics. Finally, new observation on improved characteristics and PBTI reliability of contact etching stop layer induced local tensile strained nMOSFETs with HfO_2 gate dielectrics were reported

At beginning, we describe the characteristics of silicon surface fluorine implantation (SSFI) for HfO_2 films with high-temperature postdeposition annealing. The thermal stability of HfO_2 gate dielectrics is much improved owing to the incorporation of fluorine into HfO_2 thin films. The gate leakage current of the SSFI HfO_2 films is about three orders less than that of samples without any fluorine implantation. In addition, improvements in stress-induced leakage current (SILC) and charge trapping characteristics are realized in the HfO_2 films with the SSFI. The incorporation of fluorine atoms into the HfO_2 films reduces not only interface dangling bonds but also bulk traps, which is responsible for the improvements in properties. On the other hand, the current transportation mechanism of HfO_2 gate dielectrics with TaN metal gate and silicon surface fluorine implantation (SSFI) is also investigated. Based on the experimental results of the temperature dependence of gate leakage current and Fowler–Nordheim tunneling characteristics at 77 K, we have extracted the current transport mechanisms and energy band diagrams for $TaN/HfO_2/IL/Si$ structures with fluorine incorporation, respectively. In particular, we have obtained the following physical quantities: i) fluorinated and as-deposited IL/Si

barrier heights (or conduction band offset): 3.2 eV & 2.7 eV; ii) TaN/ fluorinated and as-deposited HfO_2 barrier height: 2.6 eV & 1.9 eV; and iii) effective trapping levels at 1.25 eV (under both gate and substrate injections) below the HfOF conduction band, 1.04 eV (under gate injection) and 1.11 eV (under substrate injection) below the HfO_2 conduction band, which contributes to Frenkel–Poole conduction.

In addition, a process-compatible CF_4 plasma treatment for fabricating high-performance HfO_2 gate dielectrics MOS capacitor is demonstrated. This CF_4 plasma treatment was divided into two parts, which are pre-CF_4 plasma treatment and post-CF_4 plasma treatment, respectively. The effective oxide thickness of high-k gate dielectrics was much reduced by using the pre-CF_4 plasma treatment due to the elimination of the interfacial layer between HfO_2 and Si-substrate. In addition, the Hf-silicide was suppressed and Hf-F bonding was observed for the CF_4 plasma pre-treated sample. On the other hand, the fluorine atoms were effectively incorporated into HfO_2 thin film and HfO_2/Si interface by post-CF_4 plasma treatment. The charge trapping would be eliminated and the interface of the HfO_2 gate dielectrics was also improved. The device post-treated by CF_4 plasma treatment would have low leakage current, higher breakdown voltage, and thinner effective oxide thickness. Besides, the C-V hysteresis was much reduced about 90 %. A physical model was presented to explain the improvement of hysteresis phenomenon and the elimination of charge trapping of the fluorinated HfO_2 gate dielectrics.

Then, a novel high-performance and excellent-reliability HfOF MOSFET was demonstrated. Both n and p-type HfOF MOSFET can be improved by CF_4 plasma treatment, indicating this technique is compatible with CMOS fabrication. Large I_{ON}/I_{min} current ratio (~6.69×10^7), good Subthreshold Swing (~76 mV/dec), small DIBL (<20 mV), and high mobility (~165 $cm^2/V \cdot s$) can be observed for the HfOF nMOSFETs. The HfOF nMOSFET has better HfO_2/Si interface and dielectric quality, including small GIDL current and less PBTI effect. Reduced GIDL current was observed for the HfOF nMOSFET due to HfO_2/Si interface passivation by fluorine, resulting in less hole-electron pair generation. The fluorine incorporation into HfO_2 gate dielectrics effectively passivated the dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps.

Finally, new observation on SiN-cap strain-induced improved characteristics and PBTI reliability of nMOSFETs with HfO_2 gate dielectrics were reported for the first time. The “close-to-intrinsic” characteristics including driving current and g_m of

SiN-capped HfO_2 nMOSFETs were much enhanced about 90% and 50%, respectively by pulse-IV measurement. The CESL-device has better HfO_2/Si interface and dielectric quality, including less charge pumping current (90% reduction) and less PBTI effect (55% reduction). Finally, the performance of CESL-HfO_2 nMOSFETs will have larger g_m (135% increase) and "close-to-ideal" subthresold swing (~62) using dynamic threshold (DT) operation mode with tolerant hot carrier-stress characterization. These results provide a valuable guideline for the future 45 nm and beyond CMOS device design with high-k and strain engineering.

誌謝

畢業了！從沒想過會念博士班的我也畢業了，首先要感謝我的指導教授趙天生博士在這個領域上給我的指導與幫助，從老師身上也讓我看到了身為一個學者該有的風範，老師的一句話：「家庭就是我們最大的事業」，學生將永遠謹記在心並奉為圭臬。另外，我還要感謝共同指導教授賴朝松博士。賴老師對我來說，是亦師亦友。把我從大學時期愛玩的心調教成對研究的熱情，老師耐心一字一句的教導我寫第一篇國際會議論文讓我相當感動且獲益匪淺，在此衷心感謝兩位老師對學生不辭辛勞的指導。

感謝從我碩士班求學期間就帶我、指導我的王哲麒學長。因為有王哲麒學長對我的許多指導與幫助，讓我成長了很多，學長在學術實驗上嚴謹的態度及深厚的理論基礎是我最推崇的，無私的指導學弟更讓我學得如何當一位學長。也感謝我帶過的幾位學弟：武欽、德馨、子銘、冠迪、時璟，這本論文是我們一起努力的成果。感謝陪我渡過漫長求學路的實驗室成員們：建豪學長、柏儀學長、家豪學長、小馬、宗宜、阿邦、慶譚、俊祥、彥學、小棟、佩珊、高興、宗諭、美君、小宗育、智盟、意宏，你們讓我在學校的生活更加多采多姿。相信不久之後在職場中，我們會再相遇的。

要感謝的，還有一群交心的麻吉幫兄弟：百騏（百娘）、弘彬（娘彬）、奕臺（娘臺）、文政（軟政）、克竣（克軟）、智維(志雄)、厚耕(蠢蛋)、佑聰(side)、緒寬(血壓)，和你們的兄弟聚會，是我最輕鬆、最快樂的時光。在我學業跟感情低潮那時，能夠遇到你們這群交心的好兄弟，是我最開心也最珍惜的一件事！更感謝在我漫長求學期間一直陪在我身邊的小晏，妳是我念博士班最大的動力，有了妳我才能夠順利將論文完成。妳除了豐富我的感情生活外，也讓我能夠用更成熟、更自省的心態去完善我以後的感情與人生。

最後，謹以這本博士論文，獻給我的爸媽，沒有你們無怨無悔的犧牲奉獻，不會有今日的我。還有我的妹妹。我的成就，因為有你們，一切才具有了意義。你們永遠都是我最愛的家人！

2008 于 風城 • 交大

CONTENTS

Table Captions

Chapter 3

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1 Introduction

1.1 General Background

Recently, CMOS devices have been aggressively scaled into sub-65 nm regime in order to enhance the device's performance and increase the integrated circuit functionally. The accelerated downsizing rule of the transistor feature size is to scale the vertical horizontal dimensions simultaneously. With this scaling down, the gate oxide thickness of MOSFETs must be reduced. However, the continuous shrinking of gate dielectrics will face several limitations. According to the ITRS roadmap [1.1], the SiO_2 gate dielectric film thickness should be scaled down to 1.0 nm for 45 nm node technology. Such an ultra-thin SiO_2 thin film consists of only a few atomic layers will cause an unendurable large direct tunneling leakage current. This large direct tunneling current which depends on physical film thickness will cause an intolerable level of off-current, resulting in huge power dissipation and heat.

Figure 1.1 demonstrated the measured and simulated I_g-V_g characteristics under inversion region for nMOSFET [1.2]. We can see that the gate leakage current will exceed the limit of 1 A/cm^2 set by the allowable stand-by power dissipation while the gate oxide thickness scaled down to 2 nm. Further scaling of oxide thickness to below 2 nm, which will cause intolerable power consumption resulted form the increase of large direct tunneling current [1.2]. In addition, the reliability issues will also become an important role for such a thin SiO_2 gate dielectric. As a result, a variety of popular high-k materials such as HfO_2, ZrO_2, Al_2O_3, Gd_2O_3, La_2O_3, and HfSiON (Hf-silicate) have been studied as alternative gate dielectrics for 45 nm node and beyond technology to replace the conventional SiO_2 or oxynitrides [1.3-1.5]. The electrical equivalent oxide thickness (EOT) of MOSFET will maintain the same gate

capacitance with a thicker physical thickness by using the high-k gate dielectrics. Figure 1.2 illustrates basic properties of current high-k candidates.

The alternative high-k material should be thermodynamically stable on Si upon high temperature annealing (needed for dopant activation for poly-silicon gates). Unstable dielectrics materials will form interfacial layers, which are between the high-k thin film and silicon substrate. The high-k film and its interfacial layer would affect various device parameters such as EOT, flat band voltage (V_{fb}), barrier height, gate leakage current, and channel mobility, and thus significantly affect the transistor behavior. Some of the metal oxides like Ta_2O_5, TiO_2, and BST are known to degrade when annealed at temperature as low as 600 ^oC and have poor electrical properties for MOS devices [1.6-1.9]. The newer high-k materials including HfO_2, ZrO_2, Al_2O_3, Y_2O_3, and lanthanide oxides as well as their silicate and alumunate alloys have generated a lot of interest primarily due to their potential thermal stability in the presence of Si based on thermodynamic considerations.

To improve the dielectric performance of high-k gate dielectrics, some methods such as deuterium (D_2) and forming gas (FG) annealing [1.10-1.11], surface nitridation pre-treatment [1.12], and formation of the aluminate, silicate and oxynitride [1.13-1.15] alloys, have been investigated recently. It is reported that high-temperature (500 ^oC~600 ^oC) post-metal-annealing (PMA) in forming gas prior to metallization improved the channel carrier mobility as well as subthreshold slope of HfO_2 MOSFET [1.11]. Unlike the forming gas annealing, the deuterium annealing provided the hafnium oxide gate dielectrics MOSFET with better reliability characteristics such as threshold voltage (V_T) stability under high voltage stress [1.10]. Besides, surface nitridation technique was found effective in preventing boron penetration with a possible drawback of mobility reduction and negative bias temperature instability (NBTI) degradation [1.12]. To further raise the dielectrics

properties, cosputtering of silicon aluminum with hafnium to deposit hafnium silicate and aluminate dielectrics [1.13], and the use of nitric gas for chemical vapor deposition (CVD) [1.14] or oxidizing sputtered metal nitride like HfN to form hafnium oxynitride (HfON) films [1.16], are commonly used.

1.2 Motivation

As the gate oxide thickness scaled continuously, and replacement of the SiO_2 or oxynitride gate film by high-k materials are strongly demanded in order to suppress the direct tunneling current of the gate insulator. NO stack film [1.17], which suppresses the gate leakage current about 1.5 orders of magnitude, could be a good intermediate solution. However, further high-k materials are requested, as the EOT values reduce with downscaling as nearly 0.7 nm [1.18]. Among the candidates shown in Fig. 1.2, HfO_2 and its aluminates, silicates or oxynitrides are now the most popular candidates in recent years.

Nevertheless, there are still various problems to be solved for high-k gate dielectrics before their use in IC technology. First, the poor interface with Si is commonly observed [1.19]. The high-k metal oxides are deposited on the surface of Si and thus do not passivate its surface. This results in a large number of interface traps and charges which is detrimental to metal-oxide-semiconductor (MOS) device performance such as flat band voltage shift and mobility degradation [1.20-1.21]. Second, there is contamination by metal atoms during the deposition of metal oxides (from precursor for CVD) [1.18]. The metal atoms used to form high-k oxides generate deep traps in the silicon band gap. Third, the compatibility of high-k materials with gate electrode needs to be considered [1.22]. Many of the metal oxides mentioned above may not be compatible with traditional gate electrodes used today,

such as poly-Si. The may react with the gate electrode during the subsequent processing and charge its properties, e.g., work function. In addition, one of the main problems is that common high-k dielectrics will crystallize at a fairly low temperature (much less than 900 ^{o}C) [1.23]. Crystal grain boundaries then act as high dopant diffusivity paths and may also be the cause of device failure and high leakage. In order to further apply the high-k materials into the CMOS devices, all the problems mentioned above need to be effectively solved.

For the reasons mentioned above, the main purpose of this research is to develop high quality high-k gate dielectrics. CF_4 plasma treatment is widely used to improve the SiO_2 gate dielectrics [1.24] and thin film transistor (TFT) [1.25-1.27]. The plasma treatment processes are also general used in ultra large scale integration (ULSI) technology especially on annealing steps. To further realize the dielectrics properties of these high-k materials, some reliability issues such as hysteresis, charge trapping and temperature dependence are extensively studied. Although the C-V hysteresis mechanism of high-k gate dielectrics has been widely investigated [1.28-1.30], there is still no research about the hystersis phenomenon for the fluorinated high-k gate dielectrics by using CF_4 plasma treatment. Besides, the thermal stability of HfO_2 gate dielectrics would be improved for the nitrogen incorporation [1.31-1.33], the characteristics of HfO_2 thin film with fluorine incorporation by high temperature annealing are still not studied. Therefore, the C-V hysteresis phenomenon, charge trapping characteristics, thermal stabilities for the fluorinated HfO_2 gate dielectrics by using the CF_4 plasma treatment and fluorine implantation are entirely studied. A physical model is proposed to well explain the mechanism for electron and hole trapping in fluorinated HfO_2 thin film.

1.3 Organization of the Thesis

There are six chapters in this dissertation. Chapter 1 shows the overview of the high-k gate dielectrics. Motivation for the thesis is also described.

In chapter 2, the improved thermal stability including leakage current, breakdown voltage and thermal stability of the HfO_2 gate dielectrics with fluorine implantation was demonstrated while maintaining the effective oxide thickness (EOT) of 2.5 nm. In addition, the decrease of the stress induce leakage current (SILC) and charge trapping characteristics elimination were also indicated. The reduction of bulk and interface defects by fluorine implantation will contribute to the improved characteristics of HfO_2 gate dielectrics.

On the other hand, the current transportation mechanism of HfO_2 gate dielectrics with TaN metal gate and silicon surface fluorine implantation (SSFI) is investigated. Based on the experimental results of the temperature dependence of gate leakage current and Fowler–Nordheim tunneling characteristics at 77 K, we have extracted the current transport mechanisms and energy band diagrams for TaN/HfO_2/IL/Si structures with fluorine incorporation, respectively. In particular, we have obtained the following physical quantities: i) fluorinated and as-deposited IL/Si barrier heights (or conduction band offset): 3.2 eV & 2.7 eV; ii) TaN/ fluorinated and as-deposited HfO_2 barrier height: 2.6 eV & 1.9 eV; and iii) effective trapping levels at 1.25 eV (under both gate and substrate injections) below the HfOF conduction band, 1.04 eV (under gate injection) and 1.11 eV (under substrate injection) below the HfO_2 conduction band, which contributes to Frenkel–Poole conduction.

In chapter 3, we discussed that the fluorine atoms were incorporated into HfO_2 thin film by CF_4 plasma treatment to form the fluorinated HfO_2 gate dielectrics. At first, the effects of pre-CF_4 plasma treatment on Si for sputtered HfO_2 gate dielectrics are investigated. The Hf-silicide would be suppressed and Hf-F bonding was observed for the CF_4 plasma pre-treated sample. Compared with the as-deposited sample, the

effective oxide thickness was much reduced for the pre-CF_4 plasma treated sample due to the elimination of the interfacial layer between HfO_2 and Si-substrate. These improved characteristics of the HfO_2 gate dielectrics can be explained in terms of the fluorine atoms blocking oxygen diffusion through the HfO_2 film into the Si substrate.

Second, we demonstrated high-performance HfO_2 gate dielectrics fluorinated by postdeposition CF_4 plasma treatment. The secondary ion mass spectroscopy results proved that there was a significant incorporation of fluorine atoms at the interface between the HfO_2 thin film and Si-substrate. The improvement of gate leakage current, breakdown voltage, capacitance-voltage (C-V) hysteresis phenomenon and charge trapping characteristics was observed in the fluorinated HfO_2 gate dielectrics without an increase in interfacial layer thickness. A physical model was presented to explain the improvement of hysteresis phenomenon and the elimination of charge trapping of the fluorinated HfO_2 gate dielectrics. Besides,

In chapter 4, a novel high-performance and excellent-reliability HfOF nMOSFET was demonstrated. Large I_{ON}/I_{min} current ratio (~6.69×10^7), good S. S. (~76 mV/dec), small DIBL (<20 mV), and high mobility (~165 $cm^2/V \cdot s$) can be observed for the HfOF nMOSFETs. The HfOF nMOSFET has better HfO_2/Si interface and dielectric quality, including GIDL current and less PBTI effect. Reduced GIDL current was observed for the HfOF nMOSFET due to HfO_2/Si interface passivation by fluorine, resulting in less hole-electron pair generation. The fluorine incorporation into HfO_2 gate dielectrics effectively passivated the dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps.

In chapter 5, high-performance CESL strained nMOSFET with HfO_2 gate dielectrics has been successfully demonstrated. It is found that the transconductance (g_m) and driving current (I_{on}) increase 70% and 90% for device with a 300 nm capping

nitride layer. A superior HfO_2/Si interface for CESL-devices is observed, demonstrated by an obvious interface state density reduction (6.56×10^{11} to 9.85×10^{10} cm^{-2}). The CESL-device has better HfO_2/Si interface and dielectric quality, including less charge pumping current (90% reduction) and less PBTI effect (55% reduction). Further, the effects of the CESL layer to the high-k without trapping behaviors are investigated by the pulse-IV technique for the first time. A roughly 50% and 60% increase of g_m and I_{on}, respectively, can be achieved for the 300 nm CESL HfO_2 nMOSFET under pulsed-IV measurement.

Finally, in chapter 6, the conclusions are made and the recommendation describes the topics which could be further researched.

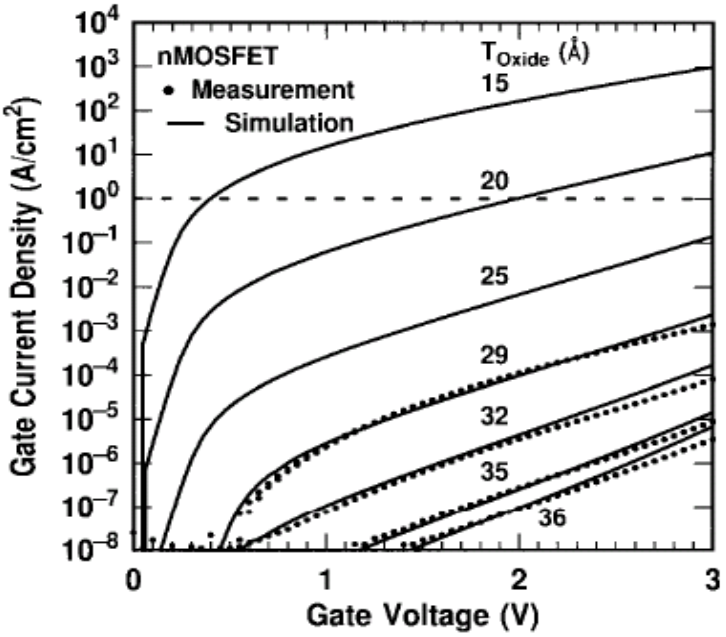


Fig. 1.1 Measured (dots) and simulated (solid lines) tunneling currents in thin-oxide nMOSFETs. The horizontal dashed line indicates a tunneling current level of 1 A/cm^2.

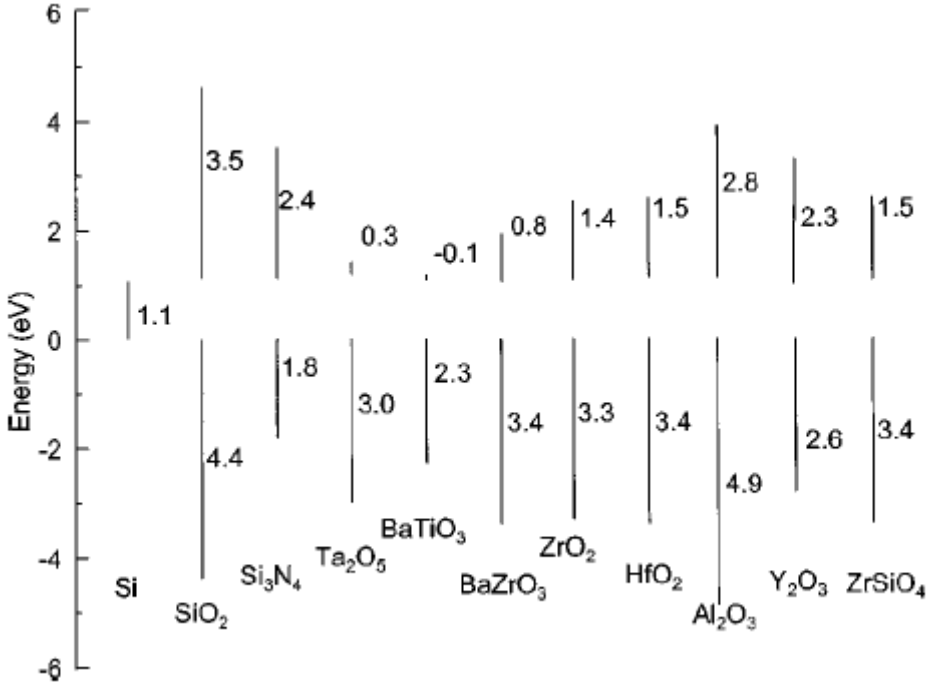


Fig. 1.2 Bandgap and band alignment of high-k dielectrics with respect to siliocn.

Chapter 2

Characteristics of HfO_2 Gate Dielectrics with Fluorine Implantation

2-1 Characteristics of Fluorine Implantation for HfO_2 Gate Dielectrics with High Temperature Annealing

2-1.1 Introduction

According to the International Technology Roadmap for Semiconductors projection, an equivalent oxide thickness of less than 1.0 nm will be needed for sub-65-nm MOSFET devices [2.1]. Due to the high tunneling leakage current, scaling of SiO_2 below 1.0 nm with acceptable leakage current level is very difficult. Recently, high-dielectric-constant (high-*k*) oxide thin films are attracting great interest as replacement for the nitrided-SiO_2 gate oxide film [2.2]-[2.5]. The various extrinsic gate dielectrics Ta_2O_5 , Y_2O_3, ZrO_2, TiO_2 , $SrTiO_3$, $BaSrTiO_3$ (BST), and HfO_2 have been investigated extensively. Among these high-*k* gate materials, HfO_2 gate dielectrics [2.6]–[2.9] are the most promising candidates being studied due to its high dielectric constant (25~30), wide energy bandgap (~5.68 eV), and high stability with the Si surface. However, the thermal stability is still a challenge for the HfO_2 due to the crystallization during the integration thermal processes. It will result in the degradation including dielectric constant lowing, gate leakage current increase and breakdown voltage decrease that limit low power application and cause reliability problems [2.10]-[2.11]. Appropriate fluorine incorporation into gate oxide films has proposed to improve breakdown-distribution tails in Weibull plots, while maintaining both Si/SiO_2 interface characteristics [2.12] and the interfaces of the fluorinated oxide are more resistant to radiation damage [2.13].

In this work, for the first time, fluorine atoms were ion implanted into the HfO_2/Si interface to improve the thermal stability of the HfO_2 gate dielectrics. It improved the characteristics including leakage current, breakdown voltage and thermal stability while maintaining the effective oxide thickness (EOT) of 2.5 nm. The property of the capacitance-voltage for HfO_2 gate dielectrics with high temperature annealing was also improved after fluorine incorporation. In addition, the decrease of the stress induce leakage current (SILC) and charge trapping characteristics elimination were also indicated. The reduction of bulk and interface defects by fluorine implantation will contribute to the improved characteristics of HfO_2 gate dielectrics.

2-1.2 Experiment

The devices used in this work were MOS capacitors fabricated on p-Si (100) wafers. Fluorine ions were implanted through 30 nm screen oxide films at a low energy of 25 keV, in order to prevent implantation damage. The implanted fluorine dosage ranged from $1\times10^{13}/cm^2$ to $1\times10^{15}/cm^2$, respectively. Then, annealing in an N_2 ambient at 850℃ for 30 minutes was performed to remove the implant-induced damage and, at that time, the fluorine atoms diffused into silicon surface. Then, HfO_2 was deposited by reactive RF sputter method. For thermal stability study, all samples were examined by the rapid thermal annealing in the N_2 ambient for 30 seconds at temperatures of 700, 800 and 900℃, respectively. The 300 nm thick Aluminum film was evaporated for top and bottom electrode to form the MOS capacitors by thermal evaporator. The process flow was schematic and summarized in Fig. 2.1.

The electrical properties were analyzed by HP 4285 for capacitance-voltage (C-V) characteristics at 100 kHz, and the effective oxide thickness (EOT) was extracted from the capacitance under the accumulation region without considering the quantum

effect. The current-voltage (I-V) curves were measured by HP 4156C. In addition, the fluorine concentration was measured by secondary ion mass spectroscopy (SIMS). Moreover, the physical thickness was checked by a transmission electron microscopy (TEM) to obtain the dielectric constant. The X-ray Diffraction (XRD) analysis was used to realize the crystallization phenomenon of the HfO_2 thin film.

2-1.3 Results and discussion

A typical fluorine profile, for the samples with F dose of 1 x 10^{13} /cm^2 and 1 x 10^{15} /cm^2, measured by secondary ion mass spectroscopy (SIMS) was shown in Fig. 3.2. The fluorine concentration was increased with increasing the dosage of fluorine implantation. The transmission electron microscopy (TEM) image of the sample with fluorine incorporation (F dose 1 x 10^{15} /cm^2) was illustrated in the inset of Fig. 2.2. The physical thickness of the HfO_2 film is 4.7 nm and an interfacial layer of 2.9 nm formed between the HfO_2 thin film and the Si-substrate was also observed in this figure. Besides, the other interfacial layer was formed between the HfO_2 thin film and the Al-gate. The effective dielectric constant derived based on the physical thickness, including the interfacial layers, is about 15. We can also observe that the fluorine atoms were accumulated mainly at the interfacial layer for the sample with F dose of 1 x 10^{15} /cm^2. Therefore, we suggest that after fluorine implantation, the fluorine atoms would accumulate at the surface of the Si substrate, and then distributed into the bulk of HfO_2 thin film after annealing, as shown in Fig. 2.3. The incorporated fluorine will replace the hydrogen bond and terminate the dangling bond. Figure 2.4 (a) and (b) has shown the X-rays diffraction (XRD) patterns of 50 nm thick HfO_2 and HfO*x*F*y* films, respectively. The HfO_2 films with fluorine implantation would not be crystallized after 700^{o}C post-deposition annealing (PDA). This result suggested that

the fluorine incorporation could restrain the crystallization for HfO_2 films with 700°C PDA treatment. Besides, for the HfO_2 films with 800°C PDA, we observed a weak degree of crystallization; on the other hand, for the as-deposited sample annealed above 800°C, a well crystallized structure with an HfO_2 (111) orientation was observed.

Fig. 2.5 shows the capacitance-voltage (C-V) curves of the HfO_2 films with and without fluorine implantation and 900°C annealing. The large flat band voltage shift of the HfO_2 films without annealing was obtained due to the plasma damage induced by sputtering of the thin films. After 900°C annealing, the flat band voltage would be improved as shown in this figure. This post-deposition RTA process will reduce the flat band voltage and dense the thin film. Furthermore, the C-V distortion of the HfO_2 films with only RTA process was observed at the high negative gate bias owing to the crystallization induced leakage current. The high thermal stability in the EOT change was obtained for the fluorine-implanted samples as shown in Fig. 2.6. After high temperature annealing, the EOT of the sample without fluorine implantation was much thicker than the HfO_2 films with fluorine implantation. We also observed that the thermal stability in EOT was significantly improved with increasing the fluorine implantation dosage. The EOT of the sample without fluorine implantation was increased with increasing PDA temperature for about 2.7 Å, whereas the EOT increase was suppressed to less than 0.3 Å for the F-implanted sample (1×10^{15} cm^{-2}). Fig. 2.7 shows the gate current density versus the gate voltage (J-V) characteristics of all samples with and without 900°C RTA annealing. As we can see, the gate leakage current of the sample without fluorine implantation was much larger than the films with fluorine implantation. Not only the leakage current but also the breakdown voltage was improved for the sample with fluorine incorporation. The characteristics were improved with increasing the fluorine implantation dosage as illustrated in this

figure. In addition, the HfO_2 films with fluorine implantation exhibit superior thermal stability in gate leakage as shown in Fig. 2.8. With the increase of the annealing temperature, the increase of gate leakage current of the fluorine-implanted samples was significantly diminished. This indicated that the fluorine incorporation reduces the defect density at the bulk HfO_2 film and the HfO_2/IL interface. The thermal stability of the relationship between gate leakage current density at $V_G = V_{FB}$ -1 V and capacitance equivalent oxide thickness was shown in Fig. 2.9. The gate leakage current for the sample without fluorine implantation was much higher than the sample with fluorine implantation while the EOT is the same for all these three samples with 700°C PDA. Besides this, the gate leakage current of all samples was increased as the PDA temperature increasing. The leakage current of the control sample with high temperature (900°C) PDA was much larger than that of the samples with fluorine implantation as illustrated in this figure. The gate leakage current density of the sample with 1×10^{15} cm^{-2} F-implantation, was three orders improved as compared to the control sample with PDA at 900°C. This indicated that the thermal stability was much improved after the fluorine incorporation. The same tendency was shown in the performance of the equivalent oxide thickness (EOT). Even after PDA at 900 °C, low EOT (25.4 Å) was obtained while keeping the leakage current less than 0.1 mA/cm^2 for the HfO_2 films with SSFI. The superior thermal stability of the F-incorporated HfO_2 gate dielectrics can be explained by the Si-H bond being replaced by Si-F and strengthened the interface quality of HfO_2/Si interface.

Fig. 2.10 shows the stress induce leakage current (SILC) characteristics of the HfO_2 films without post-deposition RTA process. We can find that the gate leakage current increases with the stress time. This increase of leakage current in the low field region is due to the trap assisted tunneling process, which is analogous to the stress induced leakage current (SILC) in SiO_2 [2.14]. Compared to the sample without

fluorine implantation, the HfO_2 films with fluorine implantation present small SILC current, which is due to the defect density being reduced as shown in Fig. 2.11. The gate leakage current of the HfO_2 films without post-deposition RTA process increase under stress was reduced with increasing the dosage of the fluorine implantation as indicated in Fig, 2.11. Therefore, the fluorine incorporation would improve the charge trapping effect in HfO_2 gate dielectrics [2.15]. Fig. 2.12 demonstrates the charge trapping characteristics of these samples without post-deposition RTA process under constant current stress (CCS) at Jg = -1.3 x 10^{-4} A/cm^2. The hole trapping was observed for all samples as shown in this figure, and was effectively suppressed for the F-incorporated HfO_2 gate dielectrics. In addition, the reduced gate voltage shift is obtained for the increased dosage of the fluorine implantation. This reduction of charge trapping indicates that the characteristics for the HfO_2 thin film were improved after the fluorine implantation at the silicon surface. The physical model of fluorinated HfO_2 gate dielectrics was proposed to explain the charge trapping reduction as shown in Fig. 2.13. Both the electron and hole trappings occurred in the HfO_2 thin film under constant voltage stress but located at different side of the HfO_2 gate dielectrics. The electron trapping takes place in the HfO_2 layer, while the positive charge (hole) is generated close to the HfO_2/Si interface where a lot of defects are presented [2.16]. We believe that the more defect density at the HfO_2/Si interface than the bulk HfO_2 film for the sample without fluorine implantation resulted in the hole trapping and indicated in Fig. 2.13(a). For the SSFI HfO_2 gate dielectrics, the fluorine atoms will distribute in the interface between the HfO_2 film and silicon substrate. Therefore, the hole trapping was effectively reduced, and then resulted in the less hole trapping observed at the fluorinated HfO_2 gate dielectrics as illustrated in Fig. 2.13(b).

2-1.4 Summary

In summary, an approach to improve the thermal stability of the HfO_2 by fluorine ion implantation at the silicon surface was proposed and systematic studied. The HfO_2 thin film with fluorine implantation was not crystallized and performed superior thermal stability even after high temperature annealing. This must be owing to the elimination of interface dangling bonds and the bulk traps for the HfO_2 films with pre-deposition fluorine implantation and post-deposition annealing. Besides, the charge trapping characteristics of SSFI HfO_2 gate dielectrics was studied and effectively improved for the samples with SSFI. This fluorinated technology could be used on HfO_2 thin films for future ULSI application.

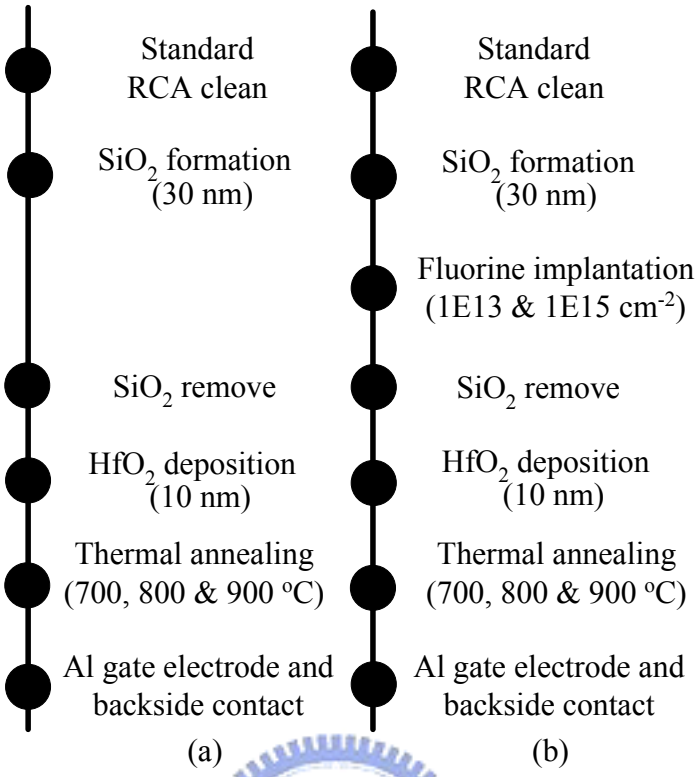


Fig. 2.1 The key processes in this work for (a) sample without fluorine implantation and (b) sample with fluorine implantation, respectively.

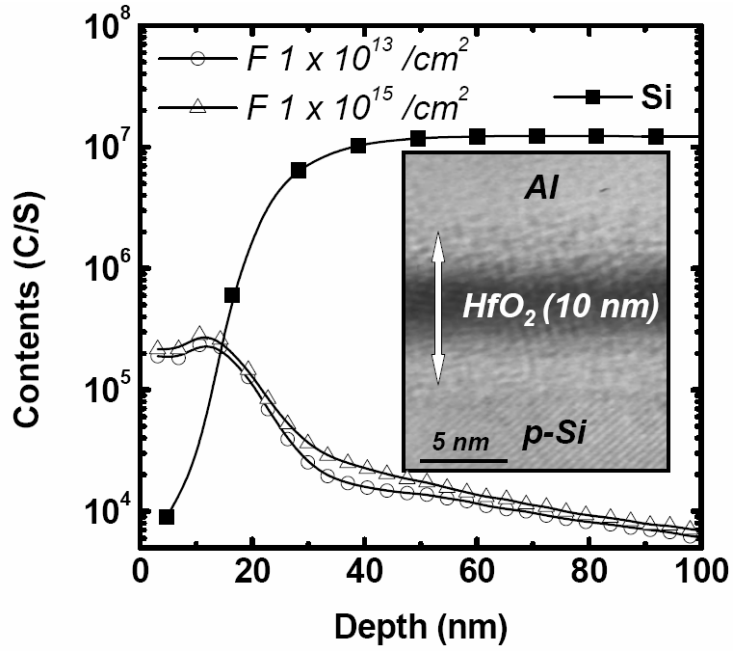


Fig. 2.2 The SIMS depth profile of MOS with fluorine implantation (dose : 1 x 10^{15} /cm^2) structure for fluorine. The peak value for fluorine is located at the interface of HfO_2 and silicon substrate. The inset figure is the TEM of MOS structure with fluorine (dose : 1 x 10^{15} /cm^2) implantation.

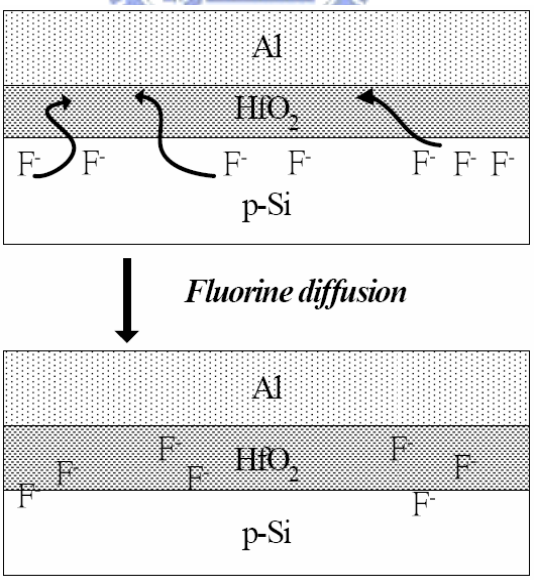
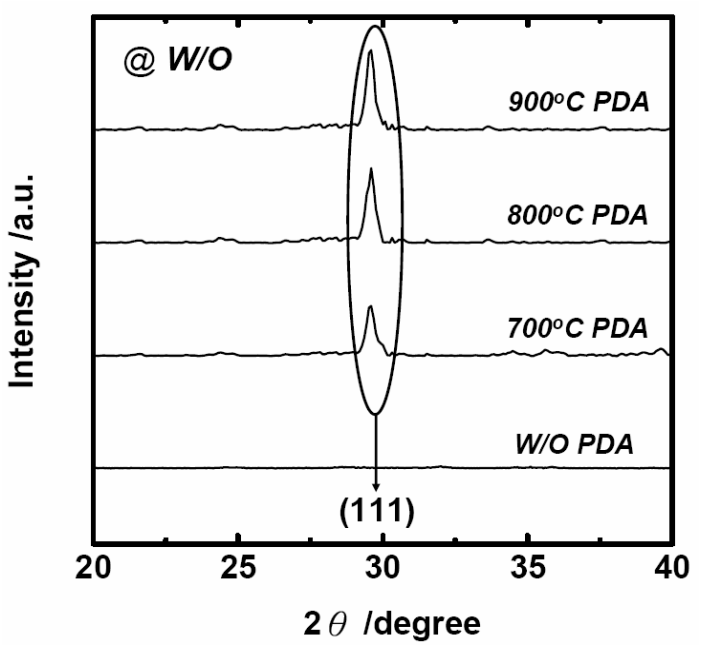
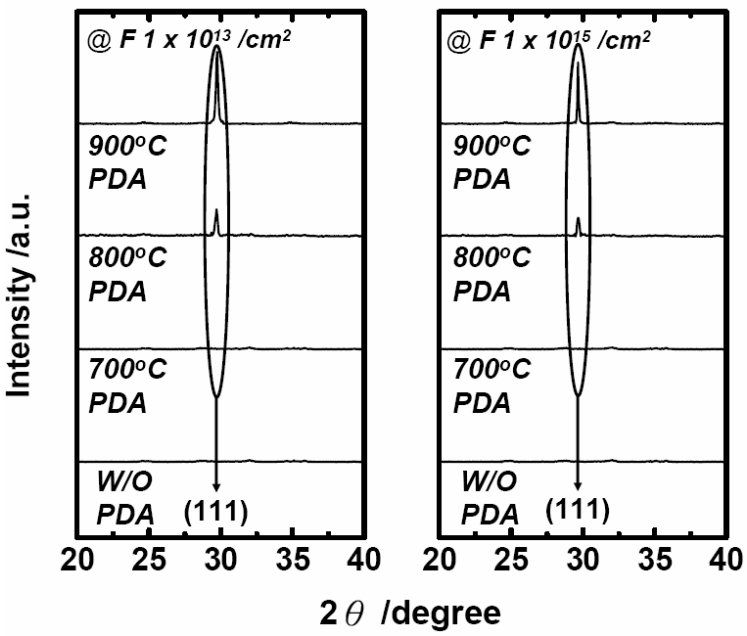


Fig. 2.3 The physical model for the distribution of the fluorine atoms. The fluorine atoms would diffuse into the HfO_2 thin film after thermal annealing.



(a)



(b)

Fig. 2.4 The XRD data for (a) as-deposited sample and (b) the samples with fluorine implantation with different PDA temperature, respectively. The sample without fluorine implantation was crystallized after 700℃ PDA.

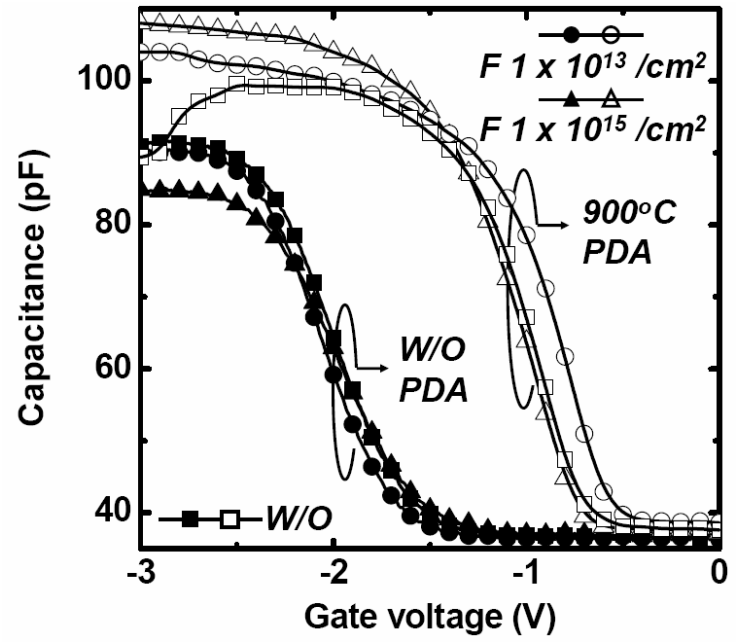


Fig. 2.5 The C-V curves for all samples. The flat band voltage shift positively after 900℃ annealing.

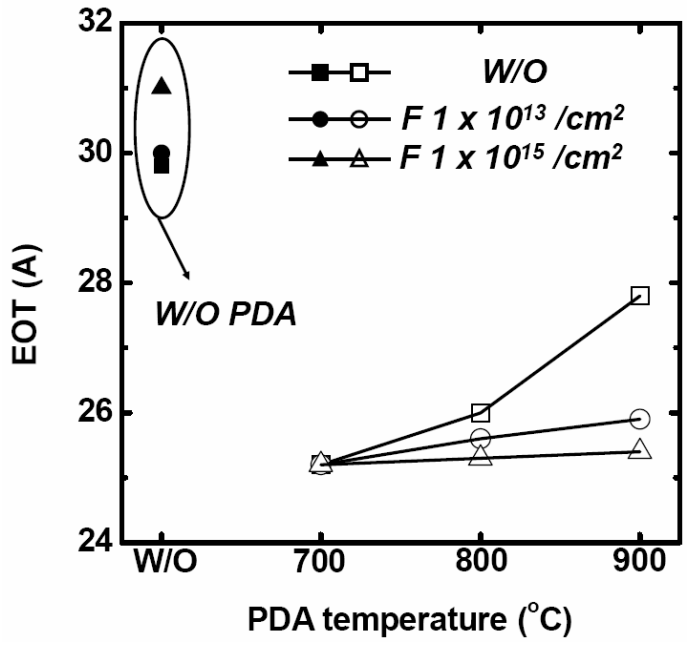


Fig. 2.6 The thermal stability in EOT for all samples. The EOT increase is much smaller for the sample with fluorine implantation.

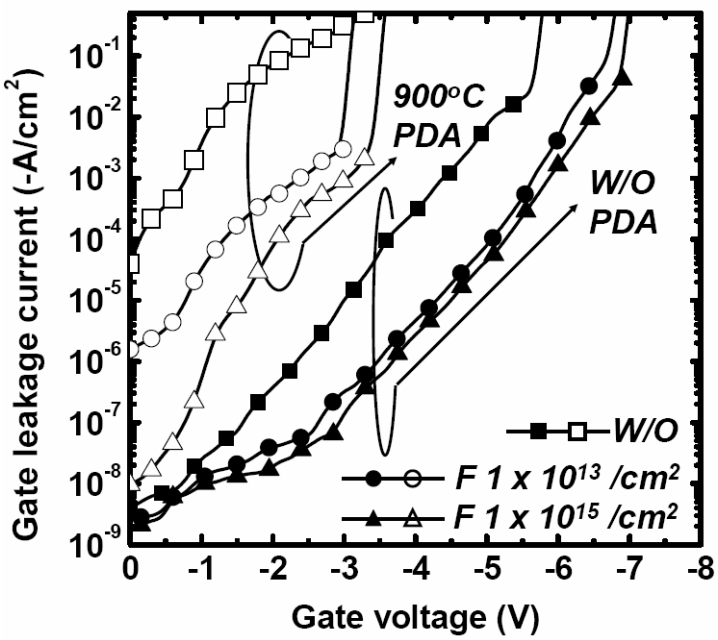


Fig. 2.7 The J-V curves (gate leakage current) for all samples. The leakage current was reduced for sample with fluorine implantation, especially in the condition for 900℃ annealing.

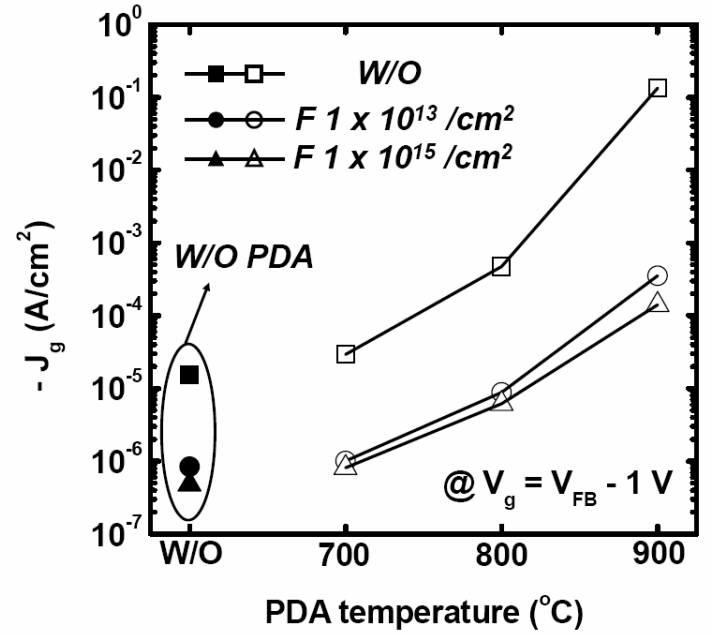


Fig. 2.8 The gate leakage current density at Vg = -2V for all samples with different annealing temperature. The thermal stability was much improved after fluorine implantation.

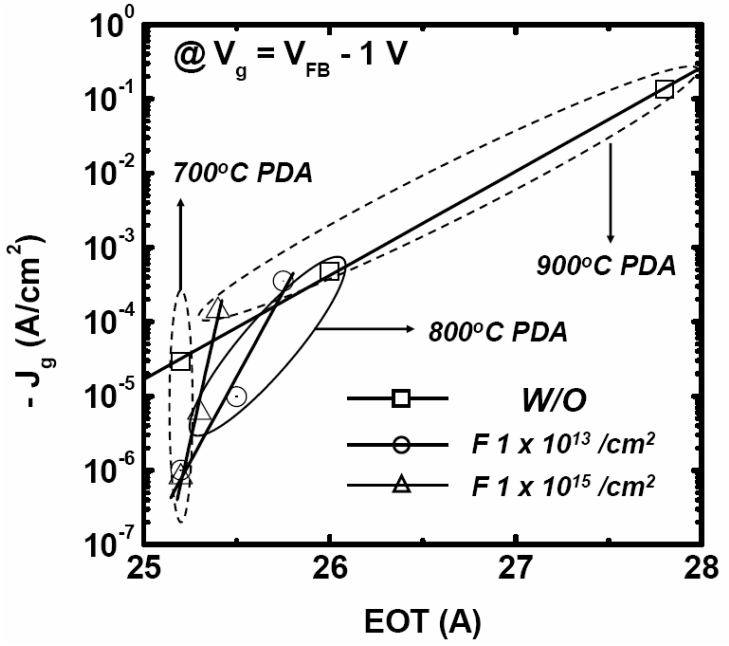


Fig. 2.9 The relationship of the thermal stability between the gate leakage current density (at Vg = -2 V) and the capacitance equivalent oxide thickness for all samples with the different annealing temperature.

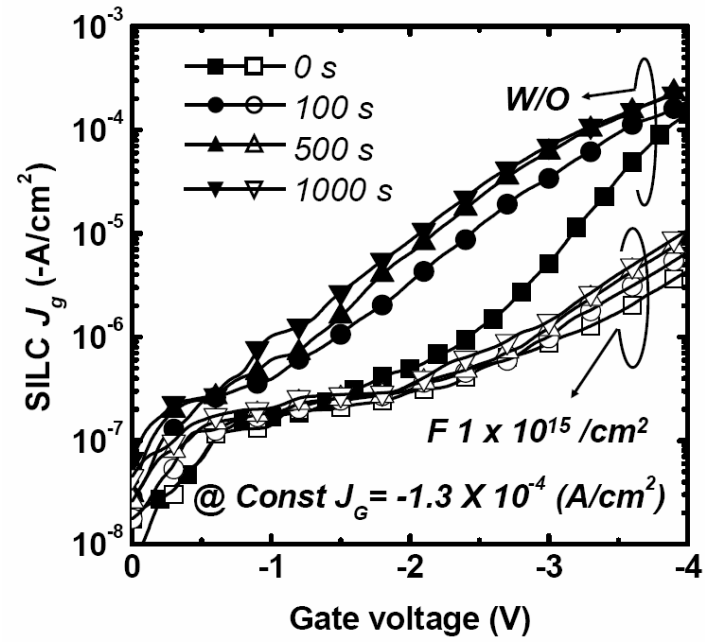


Fig. 2.10 The stress induce leakage current (SILC) characteristics of the as-deposited and the sample with fluorine implantation under negative current stress (– 1.3 x 10^{-4} A/cm^2).

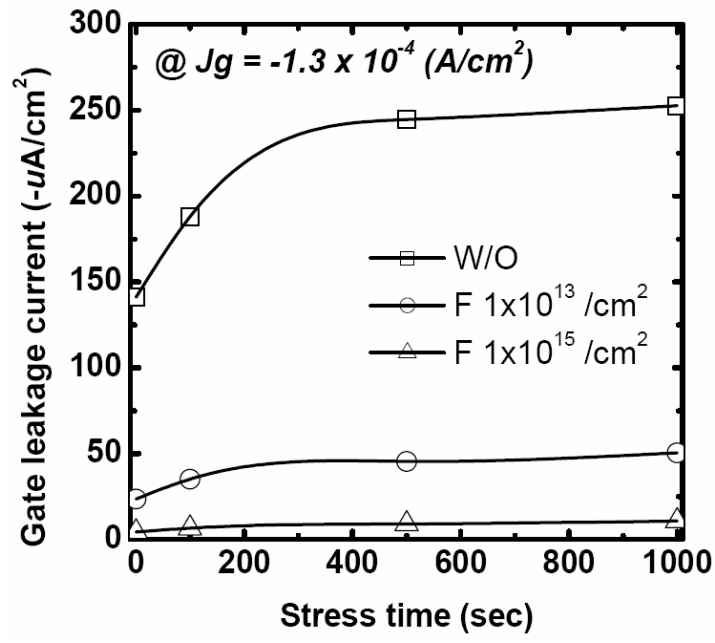


Fig. 2.11 The gate leakage current of stress induce leakage current (SILC) for all samples under constant current stress (– 1.3 x 10^{-4} A/cm^2).

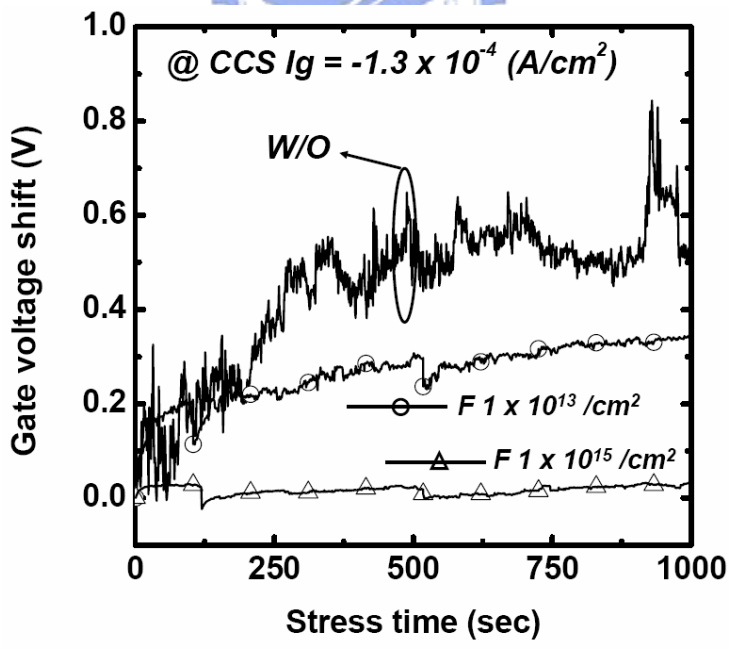


Fig. 2.12 Charge trapping characteristics of the as-deposited and fluorine implanted samples with under constant current stress (– 1.3 x 10^{-4} A/cm^2).

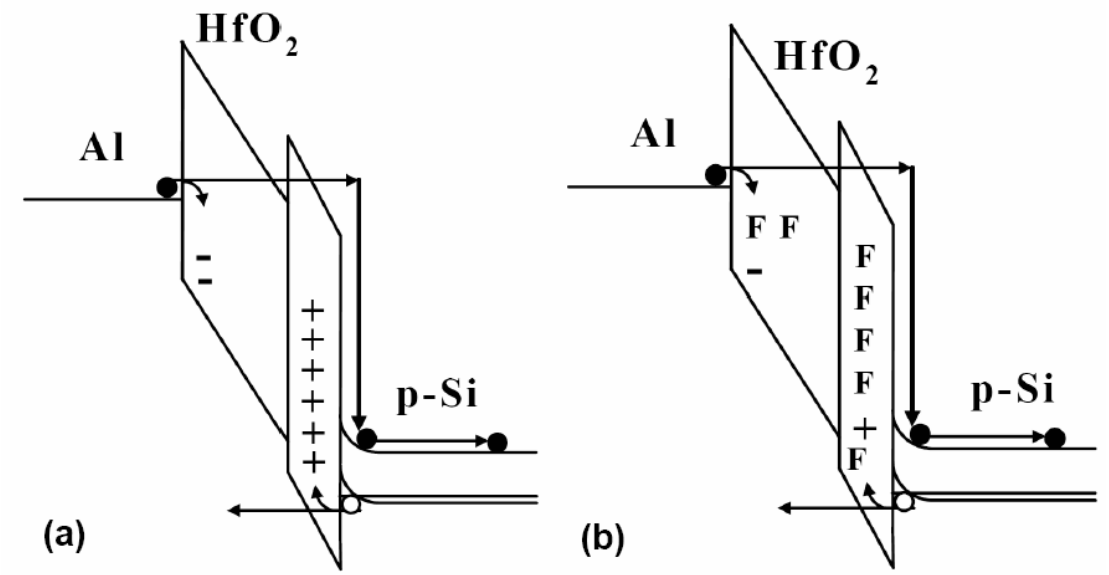


Fig. 2.13 The physical model of charge trapping mechanism under constant current stress for (a) as-deposited sample, (b) fluorine incorporated sample.

2-2 Current Transport Mechanism of TaN/HfO_2/IL/Si Structure with Silicon Surface Fluorine Implantation (SSFI)

2-2.1 Introduction

High-k gate dielectrics, as an alternative to conventional SiO_2 gate oxide, are widely investigated for their capability to reduce gate-leakage current for the same electrical capacitance [2.17]–[2.19]. Among all high-k gate materials, hafnium-based dielectrics are considered the most promising candidates, or at least the most studied, due to their excellent thermal stability, wide bandgap, and high dielectric constant [2.20]-[2.22]. Nevertheless, the metal-gate electrode has also attracted attention as a solution to the polydepletion effect that appears under gate inversion conditions in poly-Si gates, and the incompatibility between some high-*k* materials and poly-Si [2.23]. As a result, metal gate/high-k stacks have been heavily explored in recent years [2.23]-[2.26].

However, HfO_2 gate dielectrics with fluorine incorporation could also exhibit better dielectric performance and reliability [2.27]-[2.31]. F incorporation into HfSiON dielectric has been shown to be highly effective in lowering V_{th} and improving NBTI in pFET, and the drive current could be aggressively increased [2.27]. F is believed to form stronger Hf-F and Si-F bonds than Hf-H and Si-H bonds, which improves the reliability of HfO_2/SiO_2 [2.28]. Recently, we have also documented several studies of ultra-thin fluorinated HfO_2 gate dielectrics. First, the thermal stability of HfO_2 gate dielectrics can be much improved by fluorine ion implantation on the silicon surface [2.32]. Second, the interfacial layer (between HfO_2 film and Si-sub.) formation can be effectively suppressed by pre-CF_4 plasma treatment [2.33]. Third, the charge trapping phenomenon can be largely eliminated for the HfO_2 gate dielectrics fluorinated by postdeposition CF_4 plasma treatment [2.34].

Although several recent studies have investigated fluorinated HfO_2 gate dielectrics [2.27]-[2.34], its carrier transport mechanisms have not been well investigated. Only a few studies have demonstrated the carrier transport and tunneling mechanisms of conventional HfO_2 gate dielectrics [2.35]-[2.37], and none have explored fluorinated HfO_2 gate dielectrics. Electron transport in high-k gate dielectrics will instead be governed by a trap-assisted mechanism, such as Frenkel–Poole conduction or hopping conduction, due to the charge trapping phenomenon. The band diagram of the metal/HfO_2/Si capacitor has been investigated, though without consideration of the interfacial layer [2.35]. However, the interfacial layer is a critical issue for high-k gate dielectrics, and deserves in-depth discussion.

In this section, we investigate the carrier transportation mechanism in devices integrating both HfO_2 gate dielectrics with and without fluorine incorporation and a metal gate (TaN). We present new, accurate characterizations of TaN/as-deposited and fluorinated HfO_2/Si capacitors, including Frenkel-Poole conduction and Fowler-Nordheim tunneling, under both gate and substrate injection modes. The strong temperature dependence of the gate leakage current suggests that the current tunneling mechanism is Frenkel-Poole conduction for both as-deposited and fluorinated HfO_2 gate dielectrics. The effective extracted trapping level of fluorinated HfO_2 gate dielectrics is thus larger than the as-deposited one. We also report the Fowler–Nordheim tunneling characteristics at 77 K, from which we can deduce the energy band diagrams for TaN/HfO_2/IL/Si and TaN/HfOF/(IL+F)/Si structures, as well as their current transport mechanisms.

2-2.2 Experiment

The devices used in this work were MOS capacitors fabricated on p-Si (100)

wafers. First, standard RCA cleaning was performed on all samples. Then, 30 nm screen oxide films were grown in order to prevent implantation damage. Fluorine ions were implanted through the 30 nm screen oxide films at a low energy of 25 keV, with different dosages ranging from $1\times10^{13}/cm^2$ to $1\times10^{15}/cm^2$, designated F 1E13, F 1E14, and F 1E15 (without F implantation, denoted as as-dep.), respectively. Then, annealing in an N_2 ambient at 850°C for 30 minutes was performed, to remove any implant-induced damage. At that time, the fluorine atoms diffused into the silicon surface.

Before HfO_2 thin film deposition, the 30 nm screen oxide was removed by wet HF solution. Then, an HfO_2 thin film was then deposited on a HF-last Si surface by an electron beam evaporation system. For HfO_2 thin film crystallization study, some samples were annealed by rapid thermal annealing in the N_2 ambient for 30 seconds at 600°C. The HfO_2 thin film was crystallized after the 600°C rapid thermal annealing, as approved in XRD analysis (not shown here). Metal gate (TaN) film of 50 nm was deposited by reactive RF sputter for all samples. Thereafter, a 300 nm thick Al film was deposited on the TaN film by thermal evaporator. The gate of the capacitor was defined lithographically and etched. Finally, a 300 nm thick Al film was also deposited on the backside of the wafer to form the ohmic contact.

The electrical properties were analyzed by an HP 4285 for capacitance-voltage (C-V) characteristics at 100 kHz, and the capacitance effective thickness (CET) was extracted from the capacitance under the accumulation region without considering the quantum effects. The current-voltage (I-V) curves were measured by a Keithly 4200. Further, the I-V characteristics were measured at elevated temperature (318-373 K) and low temperature (77 K), in order to study the current transportation and band diagram of the MOS capacitor, respectively. Moreover, the physical thickness was checked by transmission electron microscopy (TEM) to obtain the dielectric constant

of HfO_2 thin film.

2-2.3 Results and discussion

Take-off angles of 60^o and 90° were used to measure the XPS spectra of surface and bulk HfO_2 thin films with fluorine incorporation (Figure 2.14). In Figure 2.14, for all samples except the as-deposited sample, a distinct F 1s peak at 687 eV can be observed. The silicon surface fluorine implantation processes are apparently introducing fluorine atoms into the dielectrics to form the HfOF gate dielectrics. However, the fluorine intensity was larger for the TOA = 90^o than TOA = 60^o, indicating that less fluorine would distribute in bulk HfO_2 gate dielectrics. Figure 2.15 shows the TEM image of the TaN/HfO_2/IL/Si structure with fluorine incorporation ($1\times10^{15}/cm^2$) and 600°C postdeposition annealing (PDA). The great quality of the HfO_2 thin film was demonstrated in this study, as Figure 2.15 shows. As discussed before, PVD deposited HfO_2 thin films tend to have interfacial layers (IL) at the HfO_2/Si interfaces as shown in the TEM images. In addition, the composition of the interfacial layer is believed to be hafnium silicate, because the estimated dielectric constant of the interfacial layer is higher than that of the SiO_2. Furthermore, the thickness of HfO_2 and Hf-silicate were about 3.3 and 2.6 nm, respectively. As a result, the k value of the HfOF (with Hf-silicate) thin film was about 14. In this work, the carrier transportation mechanism of both as-deposited and fluorinated HfO_2 gate dielectrics was investigated, while taking into account the Hf-silicate interfacial layer.

Figure 2.16 shows the gate current density versus the gate voltage (J-V) characteristics of all samples with and without 600°C RTA annealing under (a) gate injection and (b) substrate injection modes, respectively. As we can see, the gate leakage current of the sample without fluorine implantation was much larger than that

of films with fluorine incorporation under both gate and substrate injection modes. Both the leakage current and the breakdown voltage were improved for the sample with fluorine incorporation. Further, these characteristics were improved as the fluorine implantation dosage increased, as illustrated in this figure. In addition, the gate leakage current increased for the samples with 600°C RTA annealing, owing to HfO_2 thin film crystallization. However, the gate leakage current reduction may still be observed for the fluorinated samples, as shown in Fig. 2.16. The gate leakage current for the samples with fluorine incorporation was much smaller than that of the samples without fluorine incorporation, while the CET was also decreased for fluorinated samples with and without 600°C PDA (Fig. 2.17). The decrease of CET for the samples with 600°C PDA is resulted from densification of HfO_2 thin film. However, the HfO_2 films with fluorine incorporation appeared to possess properties superior to those of the as-deposited samples, including thin EOT and low leakage current. Figure 2.17 demonstrates the relationship between gate leakage current density at $V_G = V_{FB}$ -1 V and capacitance equivalent oxide thickness for all samples. The gate leakage current density of the sample with 1×10^{15} cm^{-2} F-implantation displayed a two order of magnitude improvement by comparison with the as-deposited sample with PDA at 600°C under gate injection mode. The same tendency was shown in CET performance. Even after PDA at 600°C, low CET (16.9 Å) was obtained while the leakage current was kept at less than 0.01 mA/cm^2 for the HfO_2 films with fluorine incorporation under substrate injection. The gate leakage current reduction of the F-incorporated HfO_2 gate dielectrics can be explained by F atoms incorporation into HfO_2 layer. The fluorine atoms can be bonded to Hf (or Si) dangling bonds resulting in annihilation of oxygen vacancies. Besides, the fluorine incorporation will effectively eliminate some shallow traps in HfO_2 thin films resulting in lower F-P conduction leakage current for fluorinated HfO_2 gate dielectrics

[2.32][2.34]. This shallow trap elimination will be discussed in the next paragraph. Figure 2.18 shows the Weibull distribution plots of the gate leakage current density at $V_G = V_{FB}$ -1 V for all samples. Both the performance and uniformity distribution of the fluorinated HfO_2 gate dielectrics were superior to those of the as-deposited samples under both gate and substrate injection modes, without an increase in CET.

The temperature dependence of the gate leakage current was studied to understand the current transport mechanisms. The gate leakage currents were measured from 318k to 373 K as shown in Fig. 2.19a-d for (a)-(b) gate electron injection (negative V_G) and (c)-(d) substrate electron injection (positive V_G), respectively. The gate leakage current increases with increasing measuring temperature under both gate injection and substrate injection for all samples, showing obvious temperature dependence. To further investigate the carrier transportation of as-deposited and fluorinated HfO_2 gate dielectrics with and without rapid thermal annealing, the Frenkel-Poole (F-P) conduction fitting is performed, as shown in the inset in Fig. 2.20. The data in the inset of Fig. 2.20 was extracted from good F-P fitting [2.38] ($J = E_{OX} \times \exp\left\{-q\left[\Phi_B - \left(qE_{OX} - \pi\varepsilon_i\right)^{1/2}\right]/kT\right\}$), where Φ_B is the effective F-P barrier, ε_i is dielectric constant of SiO_2. The electric field (E_{OX}=V/T_{OX}) is an "effective" electric field due to T_{OX} is capacitance effective oxide thickness (CET). As a result, Φ_B is named as effective F-P barrier, which is determined by the effective electric field (E_{OX}). Both gate injection and substrate injection were aggressively studied, as shown in this figure. It should be noted that this effective barrier height includes the effect of the interfacial layer between HfO_2 and Si. The extracted trap energy (Φ_B) under substrate injection for the as-deposited sample is 1.11 eV from the conduction band of HfO_2, while that of the fluorinated sample (F 1E15) is about 1.25 eV. Similarly, the extracted trap energy under gate injection for

the as-deposited sample is 1.04 eV from the conduction band of HfO_2, while that of the fluorinated sample (F 1E15) is about 1.25 eV. As the F-implant dosage increases, the increase in the effective trapping level is easily observed, meaning that most of the shallow traps in HfO_2 film can be eliminated using this fluorine implantation technique. Besides, the decreased effective trapping level can be observed for the annealed samples. The gate leakage current will increase for the annealed samples, owing to film crystallization discussed earlier. As a result, the effective trapping level extracted from F-P conduction current will decrease as shown in this figure. Further, the Schottky emission barrier ($J = A^* T^2 \exp\left[\frac{-q(\Phi_B - \sqrt{qE/4\pi\varepsilon_i})}{kT}\right]$) was also calculated. The Schottky emission barrier (Φ_B) is also an effective barrier as we mentioned above. Besides, A* is Richardson constant, and E is an effective electric field. The same as F-P conduction, the gate current of Schottky emission will dependent on temperature variation. This obvious temperature dependence of the gate leakage current was shown in Fig. 2.19. However, because the barrier height extracted from Schottky emission was larger than the trap energy extracted from F-P conduction, the F–P conduction mechanism would dominate the Schottky emission for both as-deposited and fluorinated HfO_2 gate dielectric. The energy band diagrams of carrier injection through traps assisted tunneling (a)-(b) from the silicon substrate into the HfO_2 gate dielectric, and (c)-(d) from the TaN metal gate into the HfO_2 gate dielectric were shown in Fig. 2.21. As mentioned above, the fluorinated HfO_2 gate dielectric had deep trapping, resulting in lower gate leakage current than the as-deposited HfO_2 gate dielectric, due to shallow trap elimination.

In order to obtain the energy band diagram of TaN/ HfO_2/IL/Si structure with and without fluorine incorporation, we studied the tunneling current under gate and substrate injections by biasing the p-type and n-type Si substrate to accumulation at

77 K. The current tunneling under gate and substrate injection can be observed for the MOS capacitors with p-type and n-type Si substrates, respectively. In addition, at such a low temperature, the F–P conduction is suppressed and the Fowler–Nordheim (F–N) tunneling current is dominant. Figure 2.22 shows the leakage current of as-deposited and fluorinated HfO_2 with TaN gate measured at 77 K under (a) gate and (b) substrate injections, respectively. Similar to the J-V characteristics at room temperature, both the leakage current and the breakdown voltage improved for the samples with fluorine incorporation. The characteristics improved with increasing fluorine implantation dosage, as illustrated in this figure. The inset of Fig. 2.23 shows the FN tunneling barrier heights fitted in the high field region ($J = E^2 \exp\left[\frac{-4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right]$), where the electron effective mass in HfO_2 was $0.1m_0$, and m_0 was the free electron mass [2.35], and $\hbar$ is Plank's constant. Φ_B is an effective barrier height that takes into account barrier height lowering and quantization of electrons at the semiconductor surface. The slope of the fitted line in the inset yields the following relationship: $B = -\frac{8\pi(2qm^*)^{1/2}}{3h}\phi_{eff}^{3/2}$. In addition, the FN tunneling is quite different from F-P conduction and Schottky emission. There is no temperature parameter in this equation. What is measured is the gate current as a function of gate voltage. On the other hand, it should be noted that the FN tunneling current originating from gate injection is determined by the metal/HfO_2 barrier and essentially not affected by the presence of the IL between HfO_2 and Si substrate. By the same token, the current originating from the substrate injection is determined by the IL/Si barrier. Thus, we can obtain both the TaN/HfO_2 and IL/Si barrier heights from the FN tunneling current under gate and substrate injections, respectively. Both the TaN/HfO_2 and IL/Si barrier heights were increased with F-implant dosage (Fig. 2.23). As noted above, the IL was Hf-silicate,

not pure oxide. Therefore, the effective IL/Si barrier height was 2.7 eV, which is smaller than the SiO_2/Si barrier height (3.1 eV). However, the Hf-silicate with fluorine incorporation is increased, as shown in Fig. 2.23. It seems likely that F atoms incorporated into the HfO_2 layer are bonded to the Hf (or Si) dangling bond, resulting in annihilation of the oxygen vacancies, resulting in a greater barrier, as noted above. The IL/Si barrier heights were also increased under substrate injection, owing to fluorine accumulating in the IL to passivate defect vacancies in the Si dangling bonds. In addition, the effective TaN/HfO_2 and IL/Si barrier heights will decrease for the samples with PDA treatment as shown in this figure. The effective barrier was extracted from FN equation, which was affected by J_{FN}. The J_{FN} will increase for the annealed samples due to HfO_2 film crystallization as we mentioned above. Therefore, the effective TaN/HfO_2 and IL/Si barrier heights will decrease for the annealed samples with considering HfO_2 film crystallization.

In sum, our results imply that the HfO_2 gate dielectrics with fluorine incorporation in CMOS application would have lower leakage current due not only to the shallow trap elimination but the barrier increases as well. Fig. 2.24 shows the band diagrams of (a) TaN/HfO_2/IL/Si, (b) TaN/HfO_2/IL/Si (with F $1\times10^{13}/cm^2$), (c) TaN/HfO_2/IL/Si (with F $1\times10^{14}/cm^2$), and (d) TaN/HfO_2/IL/Si (with F $1\times10^{15}/cm^2$) capacitors at flat-band, which serve to summarize the key results we have obtained from analysis of their F–N tunneling characteristics.

2-2.4 Summary

The carrier transportation mechanism of fluorinated HfO_2 gate dielectrics was successfully investigated in this work. First, the F-P conduction under gate and substrate injection for as-deposited and fluorinated HfO_2 gate dielectrics was analyzed.

The effective F-P barriers increased with increasing fluorine implantation dosage, indicating that the fluorinated HfO_2 gate dielectrics have a deep trapping level, resulting in lower F-P current. Second, the F-N tunneling mechanism for fluorinated HfO_2 gate dielectrics was also studied by J-V measurement at 77 K. The energy band diagram of the TaN/HfO_2/IL/Si capacitors with fluorine incorporation can be extracted from the good F-N fitting in this work. Further, the energy band diagram of the TaN/HfO_2/IL/Si capacitors was demonstrated taking into account the interfacial layer, which is useful for understanding fluorinated HfO_2 in CMOS applications.

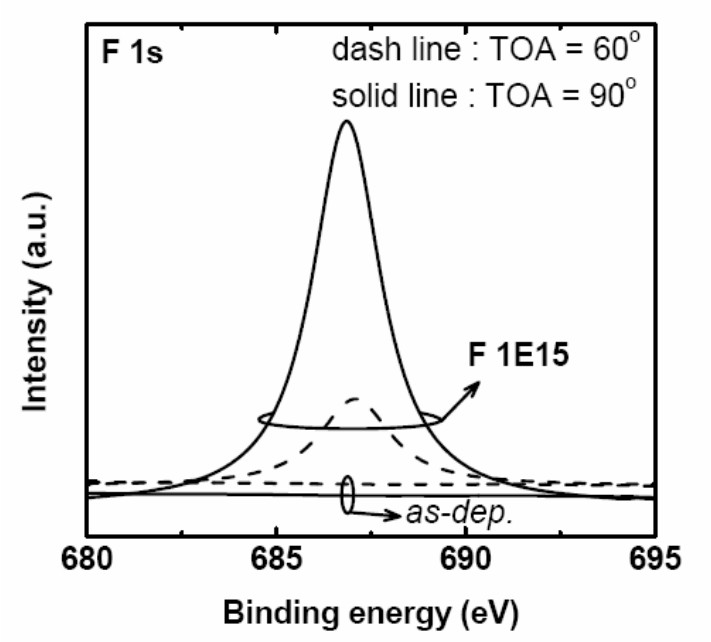


Fig. 2.14 The X-ray Photoelectron Spectroscopy (XPS) analysis of the F 1s electronic spectra of as-deposited and fluorinated samples, TOA angles of 60° and 90°, respectively.

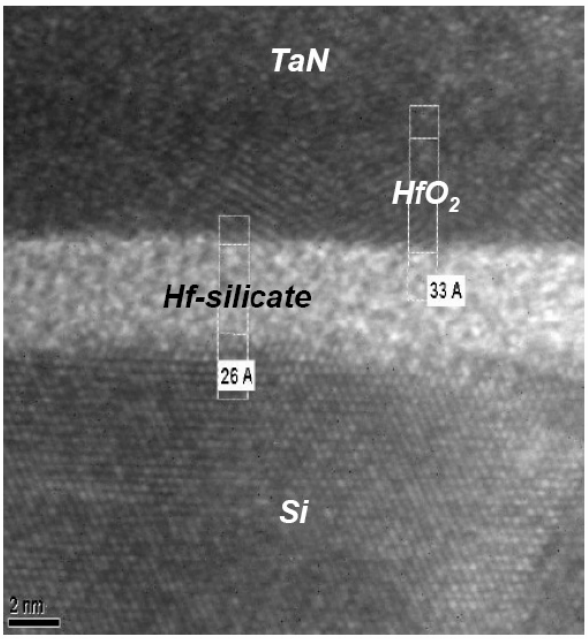


Fig. 2.15 The TEM image of TaN/HfO_2/IL/Si MOS structure with fluorine incorporation (F 1E15) with 600°C PDA.

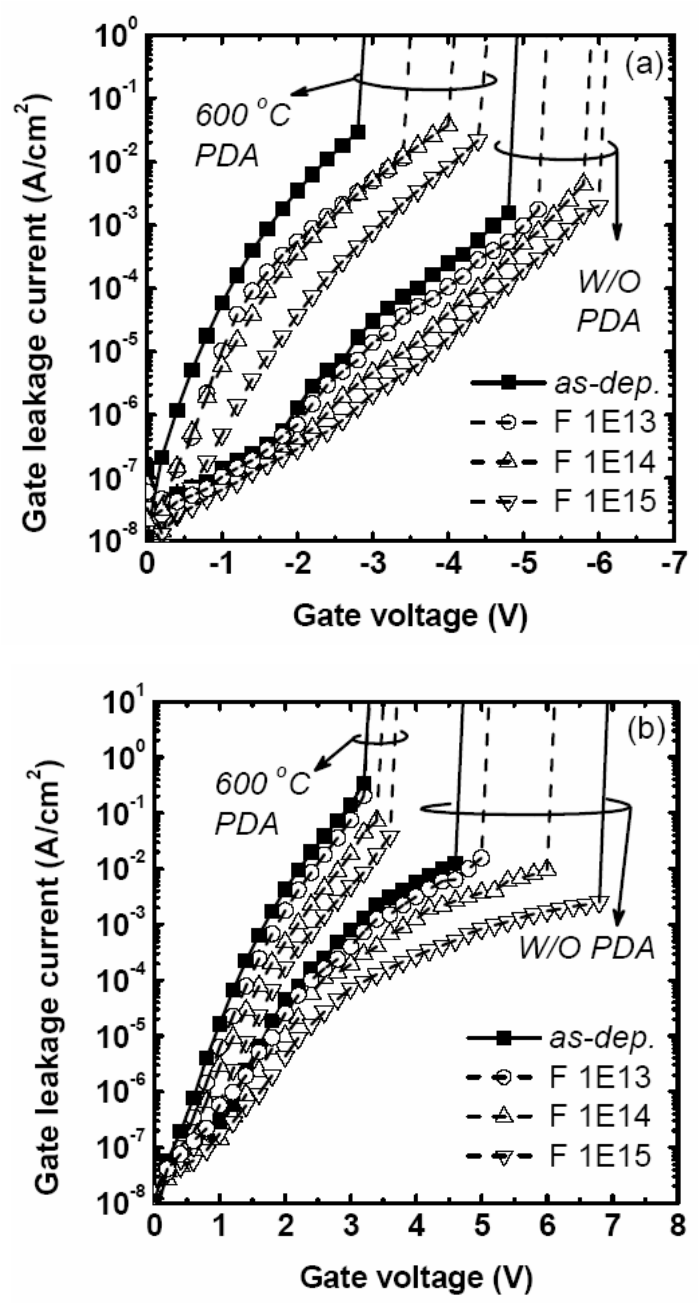


Fig. 2.16 Current-Voltage characteristics for the as-deposited and fluorinated HfO_2 gate dielectrics with and without PDA under (a) gate and (b) substrate injections.

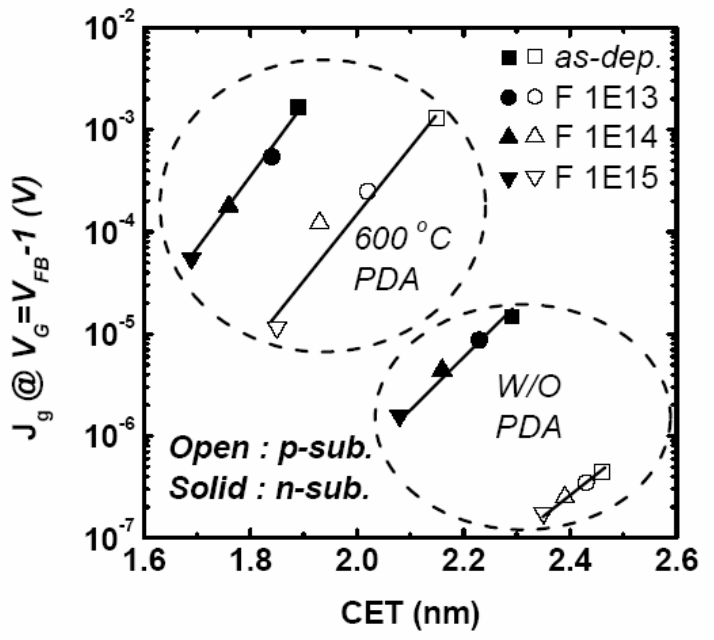


Fig. 2.17 The relationship between gate leakage current and CET for all samples. The fluorinated HfO_2 gate dielectrics have lower leakage current and CET.

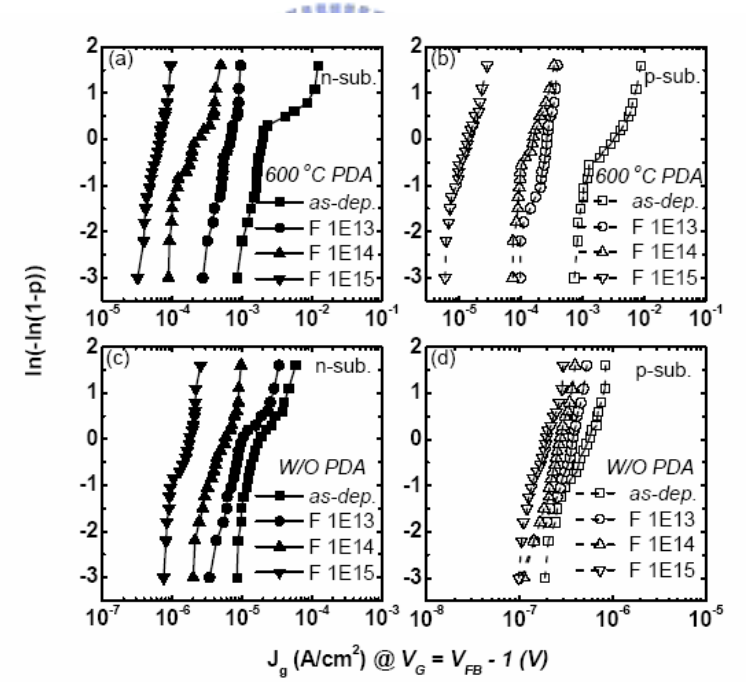


Fig. 2.18 The Weibull distribution of gate leakage current, for the as-deposited and fluorinated HfO_2 gate dielectrics under (a)(c) gate and (b)(d) substrate injections. A good distribution performance of the fluorinated HfO_2 gate dielectrics was observed.

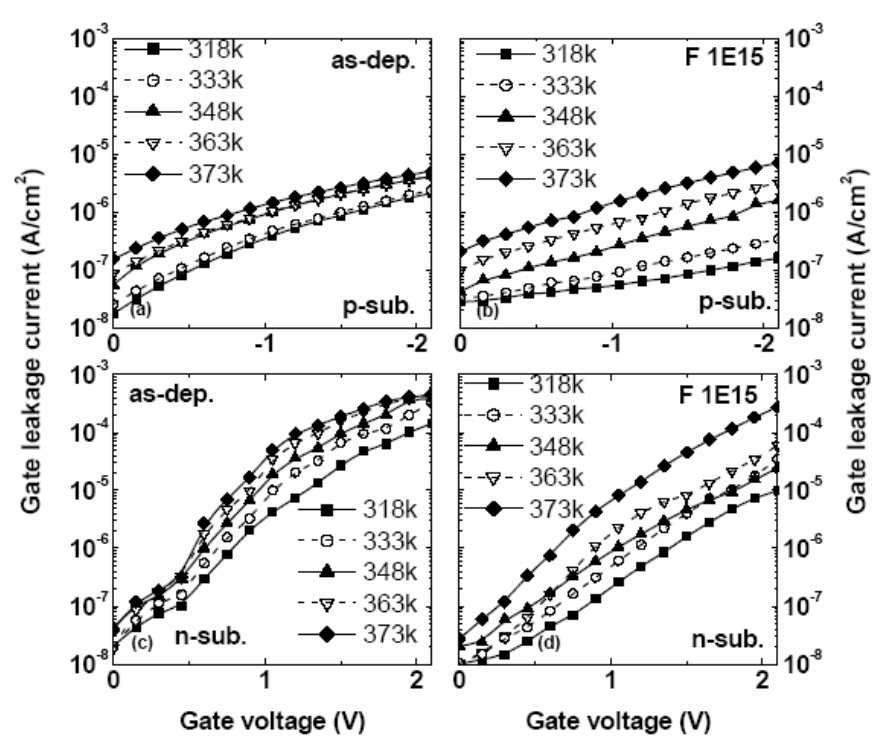


Fig. 2.19 Temperature dependence of gate leakage current increase for the (a)(c) as-deposited and (b)(d) fluorinated HfO_2 (with 1E15 SSFI) gate dielectrics under (a)(b) gate and (c)(d) substrate injections.

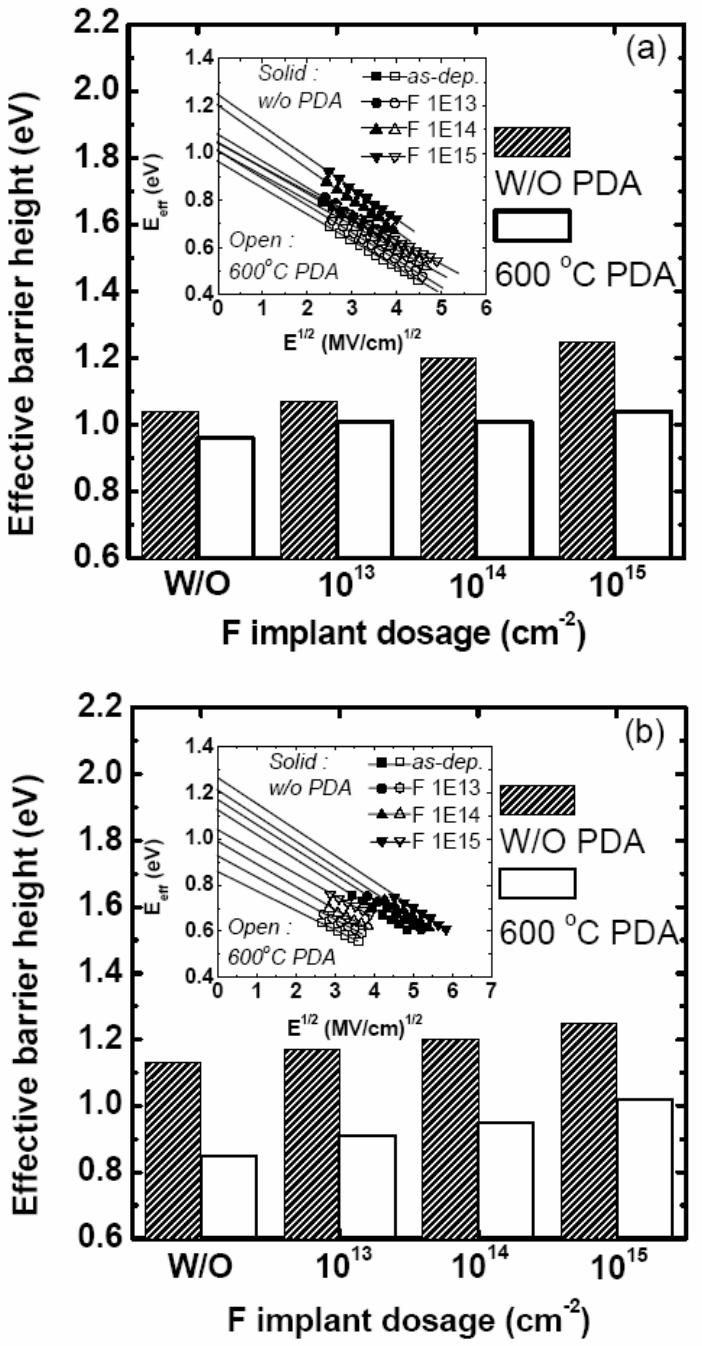


Fig. 2.20 The effective F-P trapping level for the as-deposited and fluorinated HfO_2 gate dielectrics under (a) gate and (b) substrate injections, respectively. The inset figure shows the F-P curve fit for all samples.

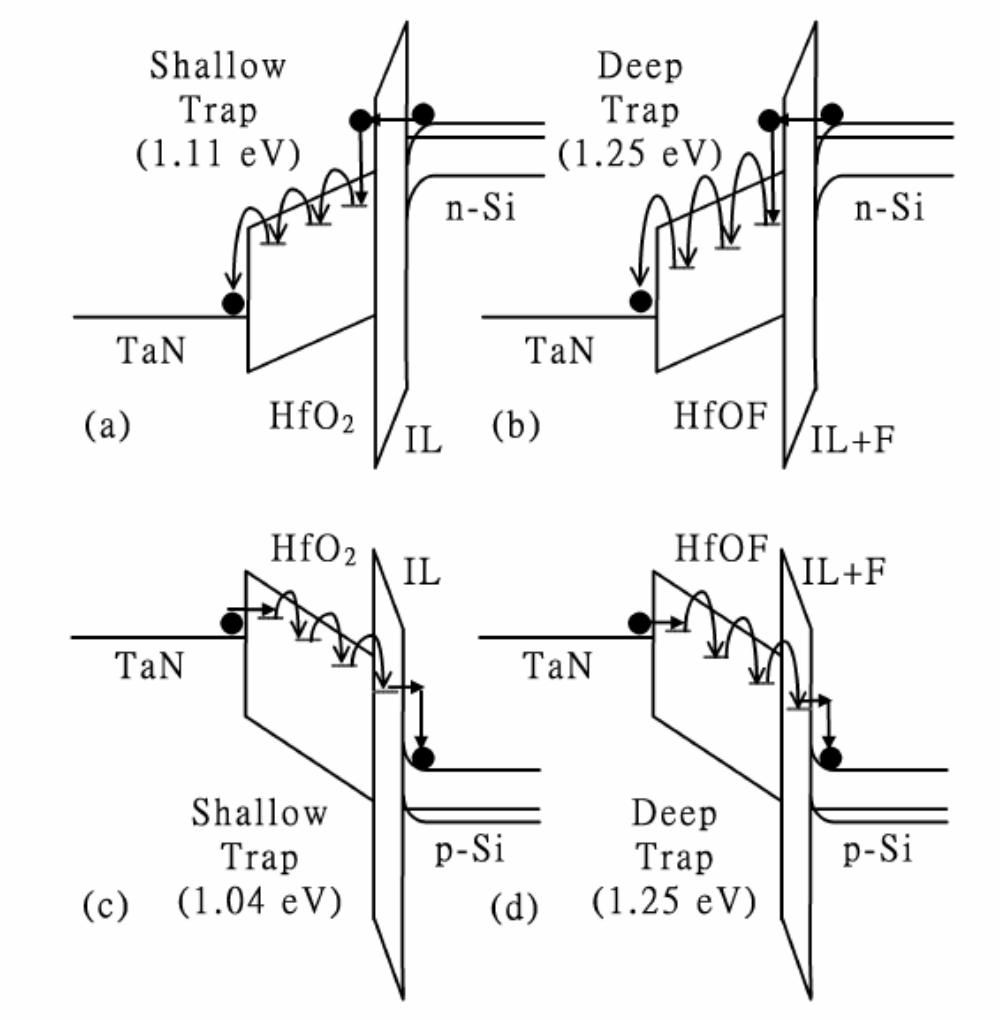


Fig. 2.21 The physical model of (a)(c) as-deposited and (b)(d) fluorinated gate dielectrics for F-P conduction under (a)(b) substrate and (c)(d) gate injections.

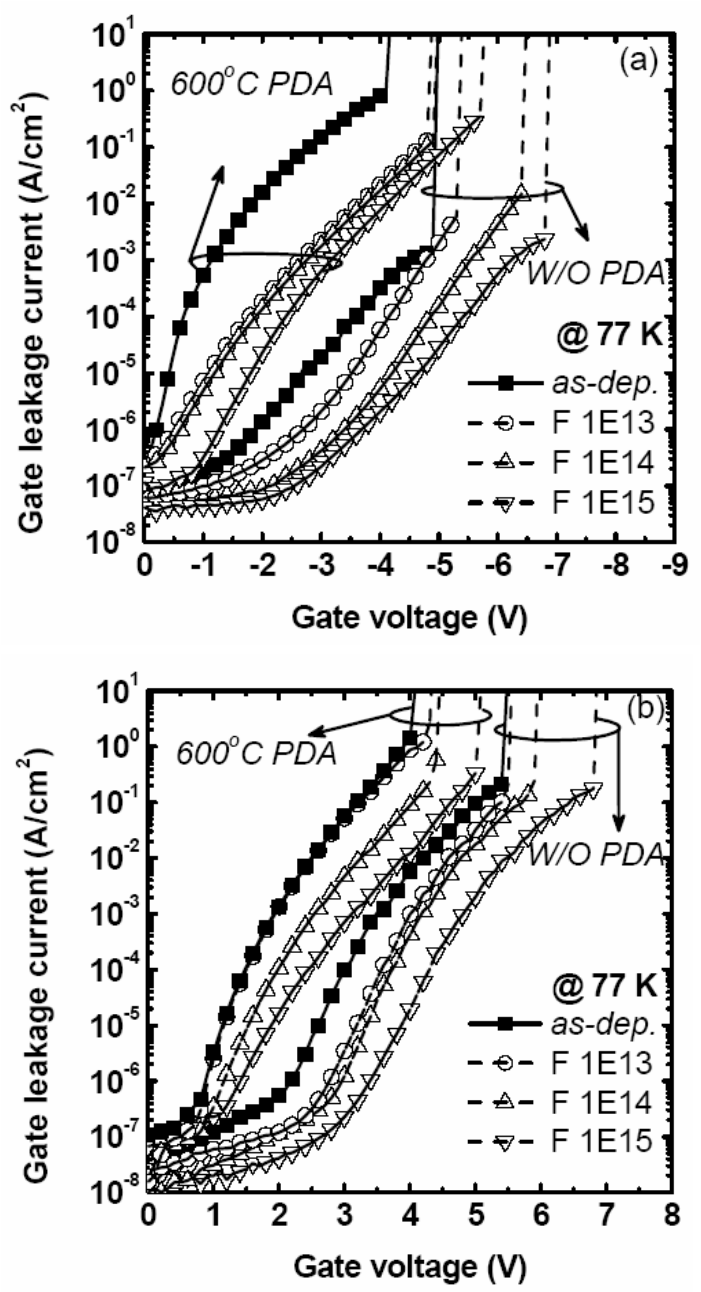


Fig. 2.22 Current-Voltage characteristics at 77 K measuring for the as-deposited and fluorinated HfO_2 gate dielectrics with and without PDA under (a) gate and (b) substrate injections.

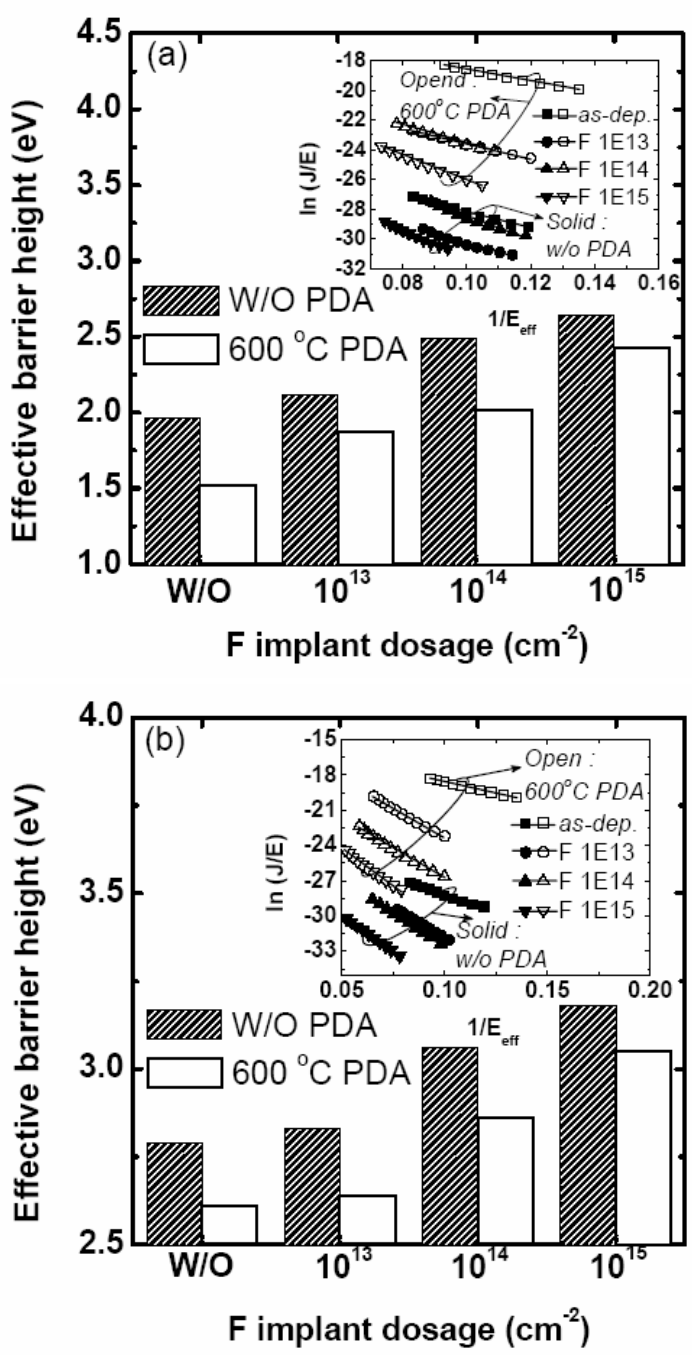


Fig. 2.23 The effective F-N barrier height for the as-deposited and fluorinated HfO_2 gate dielectrics under (a) gate and (b) substrate injections, respectively. The inset figure shows the well FN fitting for all samples.

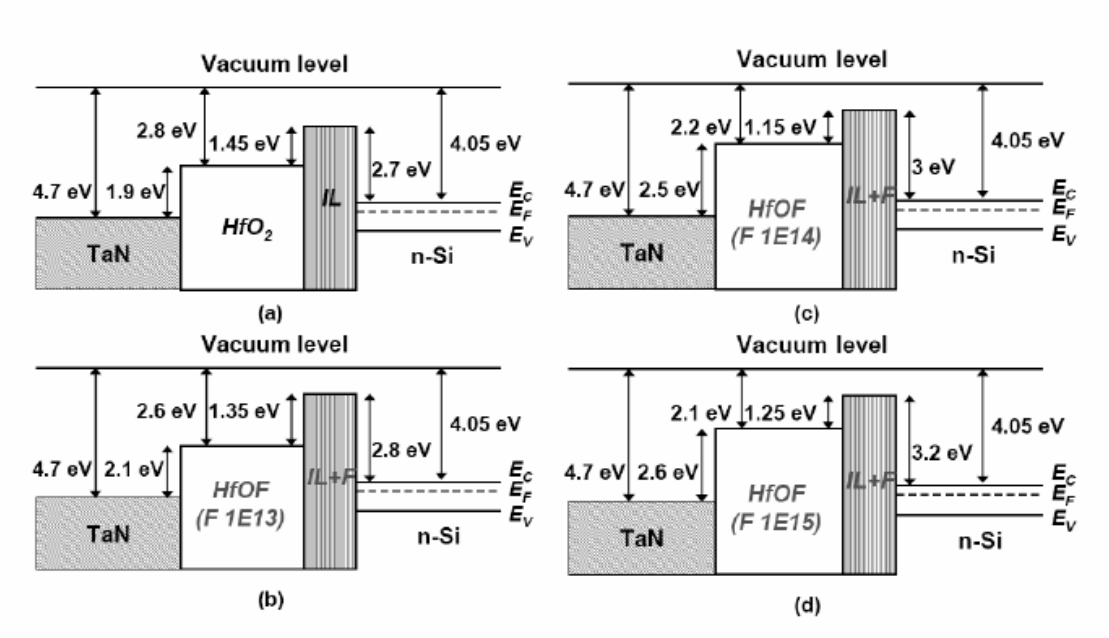


Fig. 2.24 Band diagrams of (a) as-deposited, (b) SSFI (F 1E13) HfO_2, (c) SSFI (F 1E14) HfO_2, and (d) SSFI (F 1E15) HfO_2, with TaN gate extracted from leakage current at 77 K.

Chapter 3

Effects of CF_4 Plasma Treatment on the Ultra-Thin HfO_2 Thin Film

3-1 Suppression of Interfacial Reaction for HfO_2 on Silicon by Pre-CF_4 Plasma Treatment

3-1.1 Introduction

High-*k* gate dielectrics such as HfO_2, ZrO_2, and La_2O_3 have been studied as alternative gate dielectrics for 65 nm node and beyond technology to replace conventional SiO_2 or oxynitrides because of its leakage current and reliability concerns. Among the high-*k* materials, hafnium oxide (HfO_2) gate dielectrics are considered to be the most promising in future ULSI technology [3.1]-[3.2]. However, it is still a big challenge to introduce the high-*k* materials into the complementary metal oxide semiconductor (CMOS) process, especially because of difficulties in controlling the film thickness. During the film growth and post-processing, the formation of an interfacial SiO_2-like layer (IL) is likely and limits the reduction of the effective oxide thickness (EOT) [3.3]-[3.4]. The reasons for this unwanted layer are the presence of excess oxygen during the film growth that initially oxidizes the Si surface [3.5] and Si diffusion into the film producing a silicate layer [3.6]. Therefore, methods such as cosputtering of silicon and aluminum with hafnium to deposit hafnium silicate and aluminate dielectrics [3.7]-[3.8] and the use of nitric gas for chemical vapor deposition (CVD) [3.9] or oxidizing sputtered metal nitride like HfN to form hafnium oxynitride (HfON) films [3.10] are used to improve dielectric quality. However, the nitridation technique induces positive interface charges [3.11] leading to higher hysteresis and lower channel mobility. In this work, a novel CF_4 plasma

pre-treatment approach is proposed which improves the interface between the HfO_2 gate dielectric and the Si-substrate. Fluorine atoms are distributed at the surface of the silicon substrate by CF_4 plasma pre-treatment. Then, the Transmission Electron Microscopy (TEM) and Fourier Transform Infrared Spectroscopy (FTIR) were employed and it was found that the growth of the interfacial layer had been inhibited by fluorine passivation of the silicon surface for oxidation and by the blocking of oxygen diffusion into the silicon. It was also observed that the capacitance equivalent oxide thickness (EOT) was much decreased for the CF_4 plasma pre-treated sample. The Hf-silicide was also depressed for HfO_2 gate dielectrics with CF_4 plasma pre-treatment while maintaining the HfO_2/Si interface characteristics.

3-1.2 Experiments

Metal-Oxide-Semiconductor (MOS) capacitors were fabricated on p-type (100) CZ silicon wafer with a resistance of 4~7 Ω·cm. A standard RCA clean was first performed on all samples. Before the deposition of the HfO_2 thin film, some samples were treated by CF_4 plasma for 1 minute in a plasma enhanced chemical vapor deposition (PECVD) system. Further samples not subjected to the plasma treatment but otherwise identical were the as-deposited samples. The substrate temperature was 300^{o}C and the reactive pressure and the flow rate of CF_4 were 500 mtorr and 500 sccm, respectively. In order to analyse the surface of the samples with and without CF_4 plasma treatment, attenuated total reflection Fourier transform infrared spectroscopy (ATR-FTIR) was used to inspect the variation of the native oxide formation on the silicon substrate. Then HfO_2 films with three different thicknesses of 5, 7 and 9 nm were deposited by reactive RF sputtering. The deposition plasma was created by applying 150 W of RF power to the 7.5 cm diameter target positioned 15

cm away from the substrate. After the gate dielectrics had been formed, a TaN metal gate of 50 nm was deposited by RF sputtering and aluminum films of 300nm were evaporated on both the top and bottom of the silicon wafer to form MOS capacitors. High frequency (100 kHz) capacitance-voltage (C-V) characteristics were measured with a HP4284A analyser, and the effective oxide thickness (EOT) was extracted from the high frequency capacitance under the accumulation region without considering quantum effects. The physical thickness of HfO_2 thin film and the interfacial layer was measured with transmission electron microscopy (TEM). In addition, the fluorine concentration and distribution were obtained with the secondary ion mass spectroscopy (SIMS), and the Hf-O, Hf-Si and Hf-F bonding was characterized by electron spectroscopy for chemical analysis (ESCA).

3-1.3 Results and Discussions

Figure 3.1 shows the SIMS analysis of the HfO_2 films with pre-CF_4 plasma treatment. It is apparent that fluorine atoms have accumulated mainly at the interface between the HfO_2 thin film and the silicon substrate after the CF_4 plasma pre-treatment. This observation indicated that fluorine atoms first are distributed at the surface of the silicon substrate after the CF_4 plasma pre-treatment, and then are incorporated into the HfO_2 thin film during the hafnium dioxide deposition to form fluorinated HfO_2 gate dielectrics. In addition, these fluorine atoms also terminate the dangling bonds of silicon substrate and accumulate at the interfacial layer region [3.12].

Figure 3.2 shows the Hf 4*f* ESCA spectra of as-deposited and CF_4 treated samples (CF_4 plasma treated for 1 minute), respectively. A take-off angle (TOA) of 90° was used to measure the ESCA spectra. For the as-deposited sample, as shown in Figure

3.2(a), two distinct peaks of the Hf-O bonding at 18.7 and 20.3 eV are clearly visible. In addition, Hf-Si bondings at 14.7 and 16.8 eV are also observed, meaning that Hf-silicide was formed during the HfO_2 film deposition. Such Hf-silicides degrade the performance of HfO_2 gate dielectrics[4]. Fortunately, this formation of Hf-Si bonding was effectively suppressed for the CF_4 plasma pre-treated samples as shown in Figure 3.2(b). This observation is a clear indication that the fluorine atoms accumulated at the Si/HfO_2 interface were responsible for the reduction of the amount of Si participating in Hf-silicide formation [3.13]. From the inset of Figure 3.2, we can see that the fluorine atoms were only incorporated into the HfO_2 thin film when CF_4 plasma pre-treatment was employed. Furthermore, the intensity of the Hf 4*f* spectra of HfO_2 dielectrics after CF_4 plasma pre-treatment was much larger although the original peak value at 20.3 eV was less distinct than for the as-deposited sample. This indicates that other chemical bonds were formed [3.14]. Therefore, comparing the Hf-O bonds in Hf 4*f* spectra of the as-deposited HfO_2 gate dielectrics to that of the samples with CF_4 plasma treatment, we see the Hf-F bonding. It induced by the fluorine incorporation into the HfO_2 thin film after CF_4 plasma pre-treatment as shown in the SIMS profiles in Figure 3.1 and the inset in Figure 3.2.

Figure 3.3 presents the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics with and without the CF_4 plasma pre-treatment. The EOT of as-deposited samples were 2.4, 2.9 and 3.8 nm, respectively, for the different deposited film thicknesses. As discussed before, for the sample without CF_4 plasma pre-treatment, the sputtered HfO_2 thin films tended to have interfacial layers (IL) like SiO_2 at the HfO_2/Si interfaces that have relatively small dielectric constants [3.5]-[3.6]. It makes the HfO_2 gate dielectrics exhibit thicker EOT as shown in the inset TEM image (Figure 3.3(b)). However after the CF_4 plasma pre-treatment, the IL was effectively suppressed as shown in Figure 3.3(a). The EOT decreased from 3.8 to 2.9, 2.9 to 2.0

and 2.4 to 1.6 nm, respectively, for the different deposited film thicknesses. Figure 3.4 shows the FTIR absorbance spectra of the Si wafer with and without CF_4 plasma treatment. The FTIR method employed in this work utilizes a high-index Ge hemisphere in intimate contact with the samples. The incident beam was directed to the Ge hemisphere through a reflectometer then to a HgCdTd detector. The Fourier transform spectrometer was equipped with a SiC source and a KBr beamsplitter. As depicted in Fig. 3.4, there is a dominant band at 939 cm^{-1}, which is the GeO reference peak associated with the hemisphere. In addition, the broad features that appear at 1100 cm^{-1} are the characteristic bulk interstitial Si-O-Si vibrations. For the HfO_2 films without CF_4 plasma treatment, one observes a strong and sharp band at 1221 cm^{-1} from the Si-O_x surface layer on Si. The peak is very typical of the native oxide on silicon. After CF_4 plasma treatment, the native oxide band at 1221 cm^{-1} has disappeared and been replaced by a significantly weaker absorption band centered near 1180 cm^{-1} which is similar to that observed for amorphous SiO_2 films on Si [3.15]. It is believed that the reduction of native oxide regrowth on CF_4 plasma treated Si substrates resulted from the fluorine passivation of the silicon surface. From these results, it seem reasonable that for the as-deposited sample the excess oxidizing species such as oxygen radicals, ions, and molecules in the plasma diffuse into the silicon substrate and contribute to the interfacial layer growth. On the other hand, for the CF_4 plasma treated HfO_2 gate dielectrics, the growth of interfacial layer is inhibited by fluorine passivation of the Si substrate and the blocking of oxygen diffusion into the Si. This hypothesis is supported by both the TEM imaging and FTIR spectroscopy.

3-1.4 Summary

In summary, the characteristics of CF_4 plasma pre-treated HfO_2 gate dielectrics were investigated. After the CF_4 plasma pre-treatment, the fluorine atoms were distributed at the interface between the HfO_2 thin film and silicon substrate, effectively inhibiting the formation of an interfacial layer between the HfO_2 thin film and Si-substrate. The fluorine passivation also plays a role in blocking oxygen diffusion into the Si, resulting in an EOT reduction for the HfO_2 gate dielectrics. In addition, the Hf-silicide was also suppressed for the HfO_2 gate dielectrics with CF_4 plasma pre-treatment. The CF_4 plasma pre-treatment technology can be used in device fabrication with high-k gate dielectrics for future ultra-large-scale-integration (ULSI) applications.

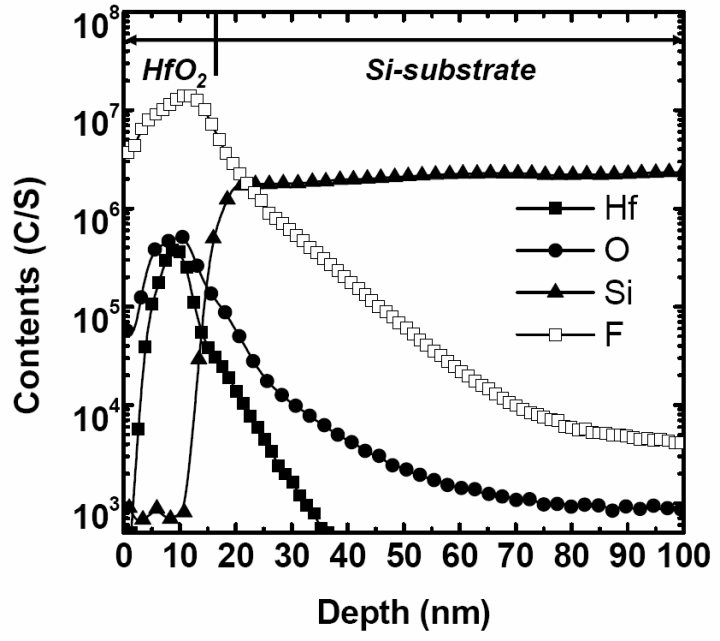


Fig. 3.1 SIMS depth profile of the HfO_2 gate dielectrics. The fluorine atoms accumulated mainly at the HfO_2/silicon substrate interface after CF_4 plasma pre-treatment.

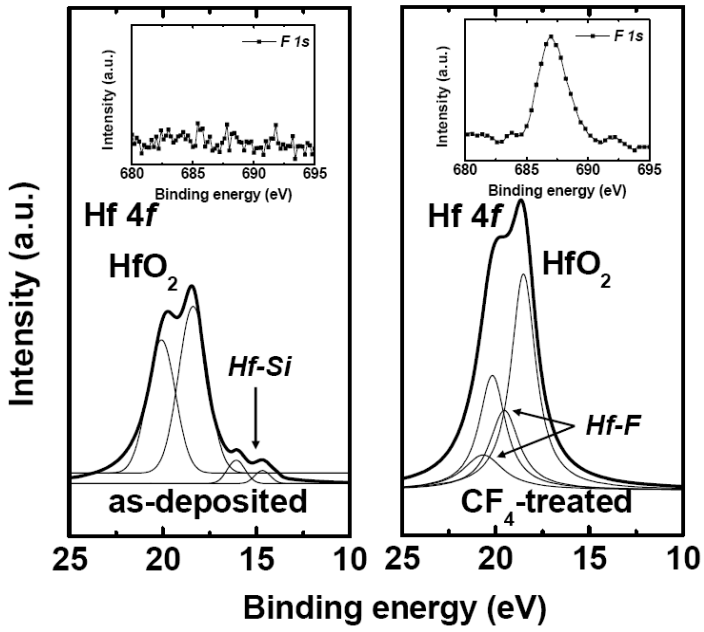


Fig. 3.2 Hf 4*f* ESCA spectra of (a) as-deposited sample, and (b) CF_4 plasma treated sample, respectively. The inset figures are the fluorine 1*s* ESCA spectra. A take-off angle (TOA) of 90° was used to measure the ESCA spectra.

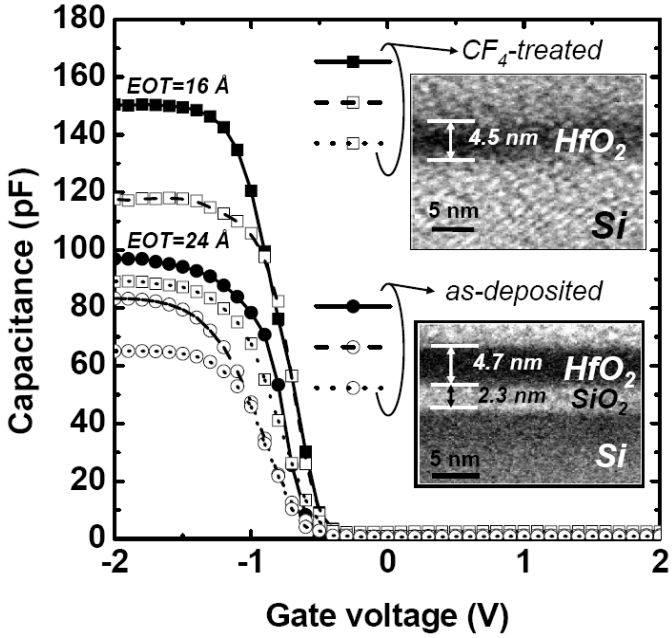


Fig. 3.3 The C-V characteristics for the samples with and without CF_4 plasma pre-treatment for various HfO_2 thin film thicknesses. The inset figures are the TEM images for the as-deposited and CF_4 plasma pre-treated samples.

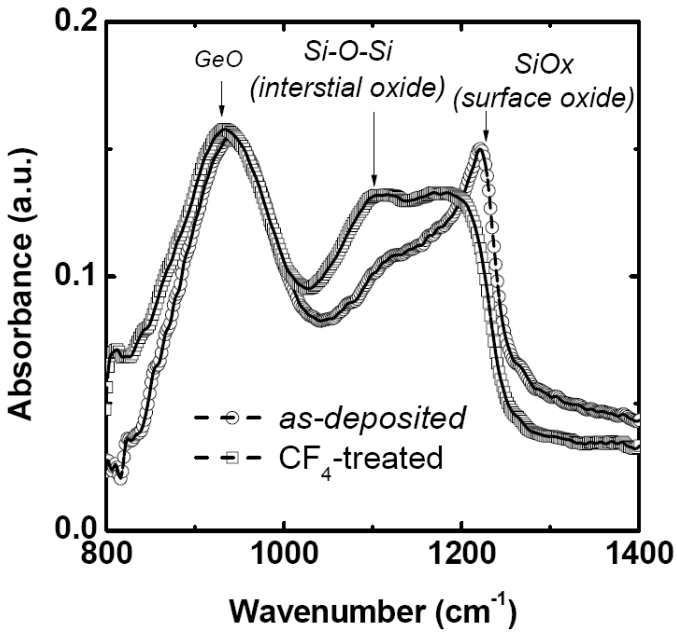


Fig. 3.4 FTIR spectra of the Si wafers with and without the CF_4 plasma treatment. Whereas the as-deposited sample showed a characteristic native oxide band at 1221 cm^{-1}, the CF_4 plasma treated sample did not. The latter sample had a broader weaker oxide feature at 1180 cm^{-1} indicating whatever Si-O_x material was present was more amorphous and with lower surface coverage than in the as-deposited sample.

3-2 High Performance HfO_2 Gate Dielectrics Fluorinated by Post-deposition CF_4 plasma treatment

3-2.1 Introduction

For anticipated applications of very large scale integration (VLSI) technology, more advanced materials for gate dielectrics will be required. Though a physical gate thickness < 1 nm for a complementary metal-oxide-semiconductor transistor with nitride/oxynitride gate stacks has been demonstrated [3.16], continued scaling for future semiconductor technology requires an equivalent oxide thickness of less than 1.0 nm for sub-65-nm MOSFET devices [3.17]. However, development of a dielectric thin film with an effective oxide thickness under 1.0 nm and an acceptable leakage current level will be very difficult, due to the high direct tunneling leakage current of nitride/oxynitride gate dielectrics. As a result, high-dielectric-constant (high-*k*) oxide thin films are currently attracting great interest as possible alternatives to nitrided-SiO_2 gate dielectrics [3.18]-[3.20].

Various extrinsic gate dielectrics, including Ta_2O_5, Y_2O_3, ZrO_2, CeO_2, $SrTiO_3$, $BaSrTiO_3$ (BST), and HfO_2 have been extensively investigated. Among these high-*k* gate materials, HfO_2 gate dielectrics [3.21]-[3.23] are the most popular candidate currently under study, due to their high dielectric constant (25~30), wide energy bandgap (~5.68 eV), and the high stability of their Si surface. At the moment, Capacitance-Voltage (C-V) hysteresis and charge trapping when the hafnium dioxide is applied to the Metal-Oxide-Semiconductor (MOS) field-effect transistor as the gate dielectrics [3.24]-[3.26], are critical problems for future ULSI technology applications of HfO_2. Therefore, various methods have been used to ameliorate these problems, including co-sputtering of silicon and aluminum with hafnium to deposit hafnium

silicate and aluminate dielectrics [3.27]-[3.28], nitridation before HfO_2 deposition [3.29], and oxidizing a sputtered metal nitride such as HfN [3.30] to form hafnium oxynitride (HfON) films.

Recently, fluorinated gate dielectrics have been shown to improve the SiO_2/Si interface [3.31]-[3.34]. Further, fluorine incorporation into the high-k gate dielectrics has been proposed, to improve both the thermal stability [3.35], and the negative bias temperature instability (NBTI) reliability [3.36]-[3.37]. However, characterization of key aspects of fluorinated HfO_2 gate dielectrics formed by CF_4 plasma treatment, including the thermal stability of the gate leakage current and C-V characteristics, breakdown voltage, and effective oxide thickness, has not been well developed. In addition, neither charge trapping during electrical measurement, nor the temperature dependence of the gate leakage current, has been investigated.

In this section, the characteristics of fluorinated HfO_2 gate dielectrics using CF_4 plasma treatment were demonstrated. Fluorinated HfO_2 gate dielectrics show thinner effective oxide thickness (~2.2 nm), smaller C-V hysteresis (45 mV), low gate leakage current density (~$5x10^{-9}$ A/cm^2), high breakdown voltage (~ -9V), better thermal stability, good distribution of electrical performance, and less charge trapping. A physical model is proposed to comprehensively explain the mechanism for electron and hole trapping in fluorinated HfO_2 thin film. Further, the temperature dependence of the leakage current explains why the generated traps are effectively eliminated in fluorinated HfO_2 gate dielectrics.

3-2.2 Experiment

For the purposes of this research, MOS capacitors were fabricated. The silicon wafers used in this study were p-type (100) CZ with a resistance of 4~7 Ω · cm.

Standard RCA cleaning was first performed on all samples. HfO_2 thin film was then deposited by reactive RF sputter method. Deposition plasma was created by applying 150 W rf power to a 7.5 cm diameter target positioned 15 cm away from the substrate. Hafnium dioxide deposition took place for 2.5 minutes, resulting in the formation of a 5 nm HfO_2 thin film. After HfO_2 thin film deposition, CF_4 plasma was used to treat the HfO_2 thin film to form the fluorinated HfO_2 gate dielectrics. Some samples were treated under CF_4 plasma in the plasma enhance chemical vapor deposition (PECVD) system, whose chamber volume is 3.76×10^5 cm^3. The cathode diameter was 40 cm, and the distance between the cathode and the holder was 4 cm. The sample was loaded into the substrate at an elevated temperature (300 ^oC). The reactive pressure and the flow rate of the CF_4 gas were 600 mtorr and 500 sccm, respectively. The RF power was 40W with CF_4 plasma exposure times of 1 min and 5 min (termed P-1 and P-5, respectively). For the normal HfO_2 gate dielectrics samples (denoted as *as-deposited*), there was no CF_4 plasma treatment after the hafnium dioxide deposition. Post-deposition annealing was performed on Rapid Thermal Anneal (RTA) equipment at 700^oC for 30 seconds in N_2 ambient. Samples with PDA treatment were called *as-deposited*/A, or P-1/A and P-5/A. The PDA process was used to determine the thermal stability of the as-deposited HfO_2 and fluorinated HfO_2 gate dielectrics. In a later phase of the investigation, a 50 nm TaN metal gate was also deposited by the RF sputter method. An aluminum film of 300 nm thickness was then deposited on the TaN gate for use as the gate electrode. Finally, the 300 nm aluminum film was evaporated from the bottom of the electrode by a thermal evaporator to form the MOS capacitors.

The effective oxide thickness (EOT) was estimated from the accumulation capacitance of the high frequency (100 khz) C-V measurement with a gate area of 6.75×10^{-5} cm^2. Quantum effects were not considered. To explore CF_4 plasma etching

effects in HfO_2 thin film, atomic force microscopy (AFM) was used to analyze the surface morphology of the HfO_2 thin film after CF_4 plasma treatment. Further, the content and distribution of the fluorine atoms was measured by secondary ion mass spectroscopy (SIMS). X-ray Photoelectron Spectroscopy (XPS) was used to analyze the Hf-O and Hf-F bondings of the fluorinated HfO_2 thin films.

3-2.3 Results and Discussion

Figure 3.5 shows the SIMS depth profiles of HfO_2 film with post-deposition CF_4 plasma treatment. The location of both the top and bottom HfO_2 interfaces was determined from the silicon, oxygen and hafnium profiles. This experimental result shows that the fluorine atoms are located primarily at the two interfaces of the TaN/HfO_2 and HfO_2/Si-substrates. The accumulation of fluorine atoms the interfaces of the gate dielectrics has been proposed in previous studies [3.31],[3.38]. However, some fluorine atoms accumulated in the bulk HfO_2 thin film, as shown by the XPS analysis (Figure 3.6). Thus, it appears that fluorine atoms are distributed in each of the HfO_2 gate dielectrics after CF_4 plasma treatment. Wright *et al.* proposed that fluorine atoms react with Si-O bonds, and then the released oxygen atoms oxidize the SiO_2/Si interface [3.31]. We thus argue that the structural change of the gate-oxide films occurs due to the reaction between the fluorine atoms and the Si-O bonds.

Take-off angles of 60^o and 90° were used to measure the XPS spectra of surface and bulk HfO_2 thin films (Figure 3.6). In Figure 3.6, for all samples except the as-deposited sample, a distinct F 1s peak at 687 eV can be observed. The CF_4 plasma treatment processes are apparently introducing fluorine atoms into the dielectrics, as noted in the prior SIMS analysis. Furthermore, the F 1*s* peak of the sample with the longer CF_4 plasma treatment (5 mins) displays a higher intensity when the TOA is 60^o.

This implies that the longer CF_4 plasma treatment introduces more fluorine at the surface of the HfO_2 thin films. In addition, the fluorine intensity was nearly identical in the bulk of HfO_2 thin films, regardless of CF_4 plasma treatment conditions (Figure 2; TOA is 90^o). Figure 3.7 shows the Hf 4*f* ESCA spectra of HfO_2 and fluorinated HfO_2 thin film. Two distinct peaks of Hf-O bonding, at 18.7 and 20.3 eV, were found in the as-deposited sample. Nevertheless, the as-deposited samples may also have large numbers of other types of bonding defects, which was not observed when the material is prepared. The TOA angles of 60° and 90° were also used to measure the XPS spectra. Compared to the Hf-O bonds in Hf 4*f* spectra of the HfO_2 thin film, the Hf 4*f* spectra of the fluorinated HfO_2 thin film is shifted roughly 0.43 eV (Figure 3.7). This also shows the Hf-F bonding formation after CF_4 plasma treatment, as seen in Figures 3.5 and 3.6. To investigate the plasma etching effect in HfO_2 thin film, we used AFM and ellipsometry to analyze the surface roughness and thickness of the HfO_2 thin film with and without CF_4 plasma treatment. Ellipsometry indicated that the thicknesses of as-deposited and fluorinated HfO_2 thin films (P-5) are 5.035 nm and 4.994 nm, respectively. These results imply that the CF_4 plasma etching effect during the treatment of HfO_2 thin films is negligible. In addition, the root mean square (rms) variations of the surfaces of the as-deposited and fluorinated HfO_2 thin film (P-1), extracted from the AFM images, are 1.05 and 1.74 Å, respectively (Figures 3.8a and 3.8b). Further, the rms of the HfO_2 thin film with 5 minutes of CF_4 plasma treatment was only 2.03 Å. These results appear to show that the CF_4 plasma treatment did not damage the HfO_2 thin film during fluorinated HfO_2 thin film formation.

Figure 3.9 shows the current density versus gate voltage (J-V) characteristics of as-deposited and fluorinated HfO_2 gate dielectrics. The gate leakage current of the samples after 700°C annealing increased due to dielectric film crystallization. In addition, the breakdown voltage of the fluorinated HfO_2 gate dielectrics was also

improved (Figure 3.9). The Figure 3.9 inset depicts the close fit of all samples to the Frenkel-Poole model. The linear behavior is a further indication that the carrier transportation in both as-deposited and fluorinated HfO_2 is F-P emission. The effective barrier heights (Φ_B) were much higher for the fluorinated HfO_2 gate dielectrics, with and without PDA treatment (inset, Figure 3.9). Besides, the Schottky emission barrier (TaN/HfO barrier) was also calculated. Because the barrier height extracted from Schottky emission was larger than the trap energy extracted from F-P conduction, the F–P conduction mechanism would dominate over the Schottky emission.

Figure 3.10 shows the effective oxide thickness versus gate leakage current characteristics of HfO_2 gate dielectrics with and without CF_4 plasma treatment and 700 ^oC post-deposition annealing (PDA). The inset shows the C-V characteristics of all the samples. The thinner EOT extracted from C-V curves was obtained for the HfO_2 gate dielectrics with CF_4 plasma treatment and was further improved after annealing at 700^oC. The CF_4 plasma treated HfO_2 films appeared to possess properties superior to those of the as-deposited samples, including thin EOT and low leakage current. However, the HfO_2 films, after 700 ^oC PDA, still presented higher gate leakage current at the same EOT than the as-deposited samples, owing to the film crystallization discussed earlier.

Figure 3.11 shows the Weibull distribution plots of the gate leakage current density at the gate voltage of -3 V and the breakdown voltage for all samples. Both the performance and uniformity distribution of the fluorinated HfO_2 gate dielectrics were superior to those of the as-deposited samples.

The normalized C-V hysteresis curves of the as-deposited and fluorinated HfO_2 gate dielectrics are shown in Figures 3.12a and 3.12b, respectively. The C-V hysteresis of the as-deposited HfO_2 gate dielectrics was 1 V, but decreased to roughly

50 mV for the fluorinated HfO_2 gate dielectrics (P-5). According to the inner-interface trapping model [3.39], when the capacitor is biased at accumulation (V_G= -3 V), majority carriers (holes for the *p*-type Si substrate) tunnel from *p*-Si substrate through the interfacial layer (IL) and are trapped at the inner-interface, as indicated in the inset band diagram in Fig. 3.12 (a). Furthermore, when the voltage is biased at the inversion region (V_G = 1 V), the trapped holes at the inner-interface will be de-trapped, while at the same time the minority carriers (electrons) tunnel from the *p*-Si substrate and are trapped at the inner-interface. On the other hand, the shifted CV curves are not parallel at intermediate and low voltages. A slight degradation of CV curves in depletion region can be observed as indicated in Fig. 3.12 (a). As a result, the hysteresis phenomenon was contributed by both interface states and bulk trapping. However, for the fluorinated HfO_2 thin film, the number of holes and the number of electrons trapped at the inner-interface and some interface states were reduced, owing to the F atoms incorporated into the HfO_2 thin film (Figure 3.12b, inset). This indicates that hole trapping was observed in our HfO_2 thin film, a finding strongly supported by the negative flat band voltage shift during the CV hysteresis measurement.

Figure 3.13 displays the Weibull distribution of C-V hysteresis for all samples. The C-V hysteresis was improved by increasing the CF_4 plasma treatment duration. Of all the samples, the HfO_2 films with CF_4 plasma treatment for 5min, and rapid thermal annealing at 700^{o}C for 30s (P-5/A) exhibit the smallest C-V hysteresis, about 40mV.

Figure 3.14 shows the Arrhenius plots of the temperature dependence leakage current density for the as-deposited and fluorinated HfO_2 gate dielectrics. The plots were obtained from the current voltage characteristics at V_G = - 3 V, measured at 303-353 K. The data fit to the relationship $J \propto \exp(-E_a / k_B T)$. The calculated values

of the activation energies for the as-deposited sample and fluorinated samples are 0.28, 0.13 (P-1) and 0.06 eV (P-5), respectively. This apparently shows that the CF_4 plasma treatment effectively removed the dielectric vacancies, leading to a lower concentration of generated traps [3.40]. The temperature dependence performance of the gate leakage current for as-deposited HfO_2 gate dielectrics was more obvious, owing to the large concentration of generated traps (hole trapping), as illustrated in C-V hysteresis. The results of the decrease in activation energy (Figure 3.14) indicate that the fluorinated HfO_2 gate dielectrics have a lower concentration of generated hole traps.

Table 3.1 summarizes the characteristics for all samples. The surface roughness of the HfO_2 thin films was not degraded by CF_4 plasma treatment. Further, the fluorinated sample exhibits superior properties in EOT, leakage current, breakdown voltage, hysteresis, and elimination of deep traps.

3-2.4 Summary

An approach to demonstrate the characteristics of fluorinated HfO_2 gate dielectrics formed by CF_4 plasma treatment was proposed and systematically studied. The fluorinated HfO_2 thin film exhibited a superior C-V and I-V performance even after high-temperature annealing. Further, charge trapping occurred in C-V hysteresis, while measurement of the fluorinated HfO_2 gate dielectrics was effectively improved. This technology may be applicable to HfO_2 thin films for future ULSI applications.

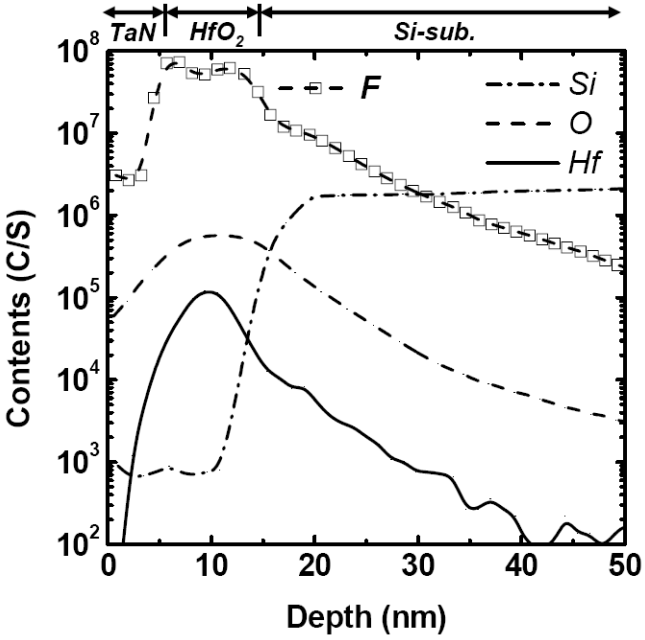


Fig. 3.5 SIMS depth profile of MOS structure for fluorine oxygen, hafnium and silicon atoms distribution. The fluorine atoms were accumulated mainly at the two interfaces of the gate-oxide films.

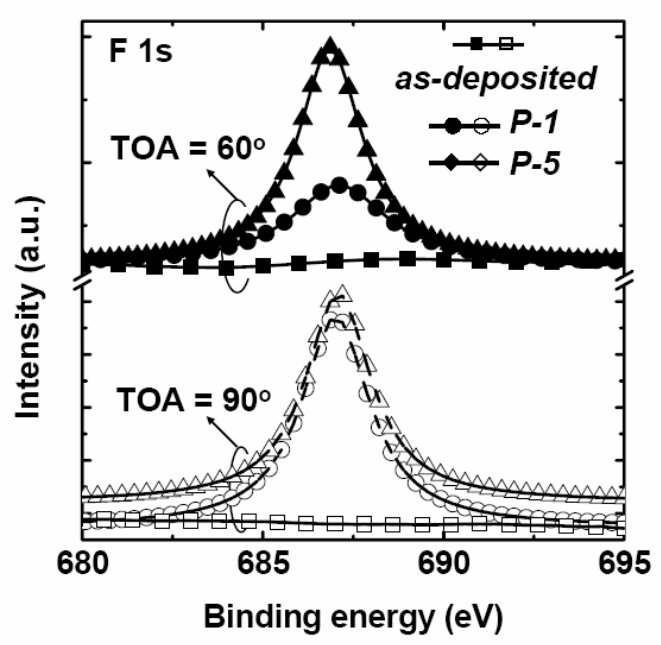


Fig. 3.6 The X-ray Photoelectron Spectroscopy (XPS) analysis of the F 1s electronic spectra of as-deposited and fluorinated samples, TOA angles of 60° and 90°, respectively, where the F 1s peak is at 687 eV.

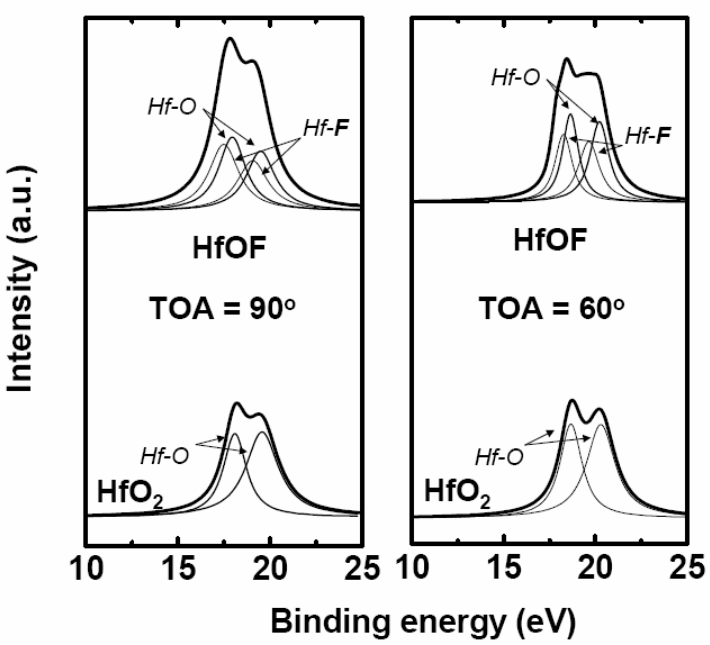
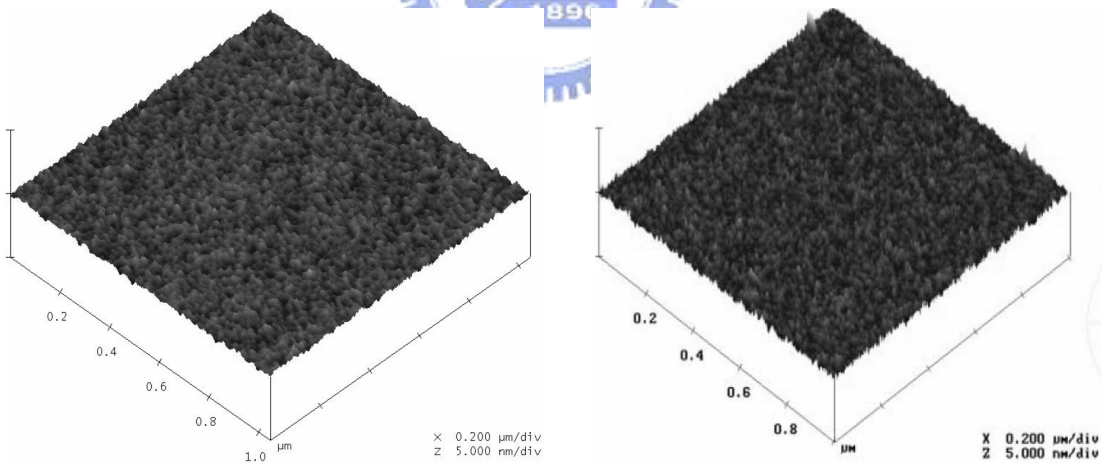


Fig.3. Hf 4*f* XPS spectra of as-deposited and fluorinated HfO_2 thin films, respectively. Take-off angles of 60° and 90° were used to measure the XPS spectra.



(a) (b)

Fig.4. The AFM images of the surface of the HfO_2 thin films (a) without CF_4 plasma treatment, (b) CF_4 plasma treatment 1 minute.

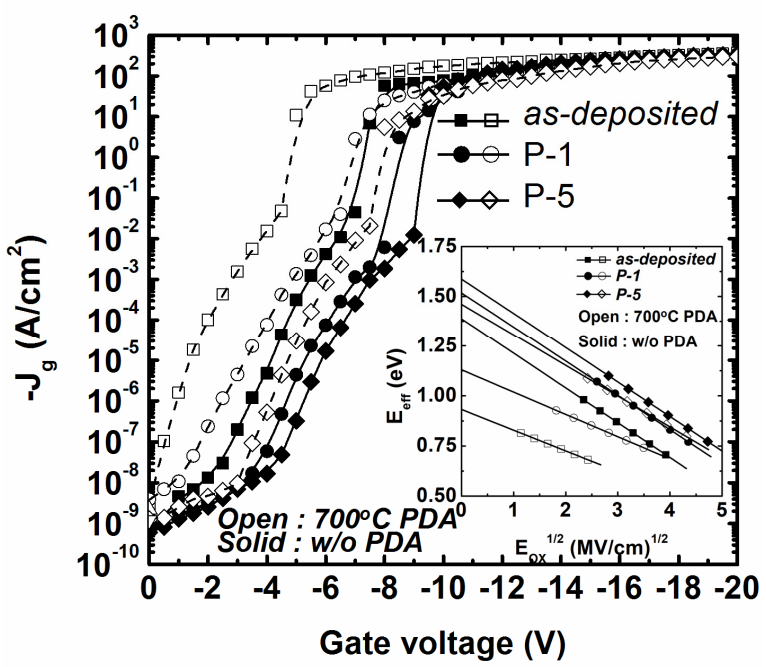


Fig.5. Current-Voltage characteristics for the as-deposited and fluorinated HfO_2 gate dielectrics with and without PDA. The inset figure shows the F-P curve fit for all samples. The fluorinated HfO_2 gate dielectrics have a higher F-P barrier height, which increases as plasma treatment time increases.

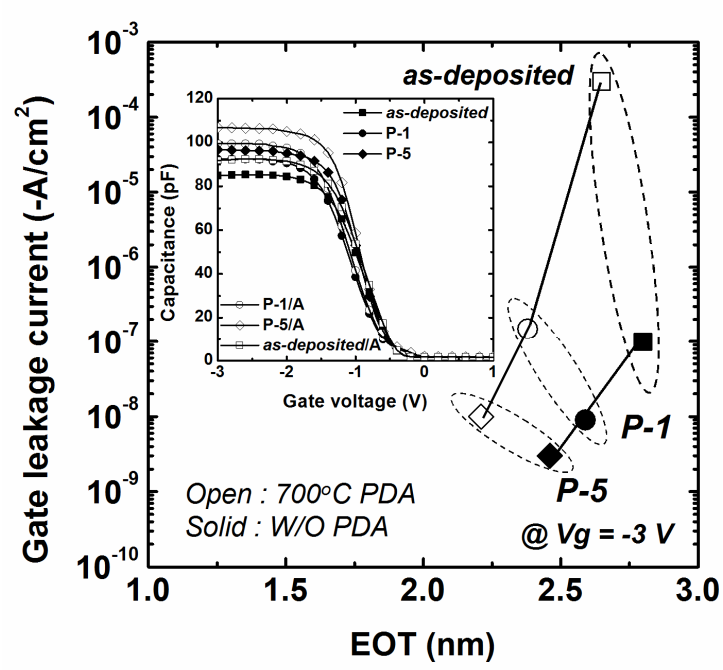


Fig.6. The relationship between gate leakage current and EOT, extracted from the C-V curves (inset figure) for all samples. The fluorinated HfO_2 gate dielectrics have lower leakage current and EOT.

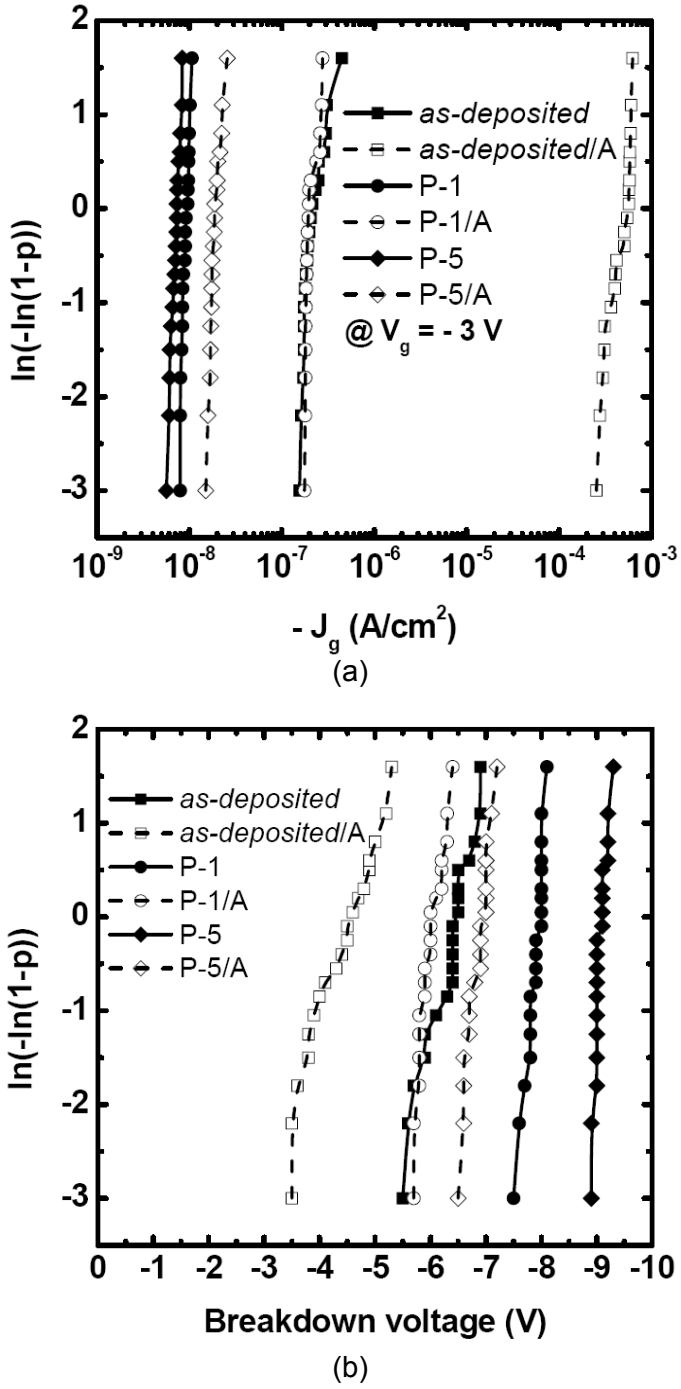


Fig.7. The Weibull distribution of the (a) gate leakage current and (b) breakdown voltage, for the as-deposited and fluorinated HfO_2 gate dielectrics. A good distribution performance of the fluorinated HfO_2 gate dielectrics was observed.

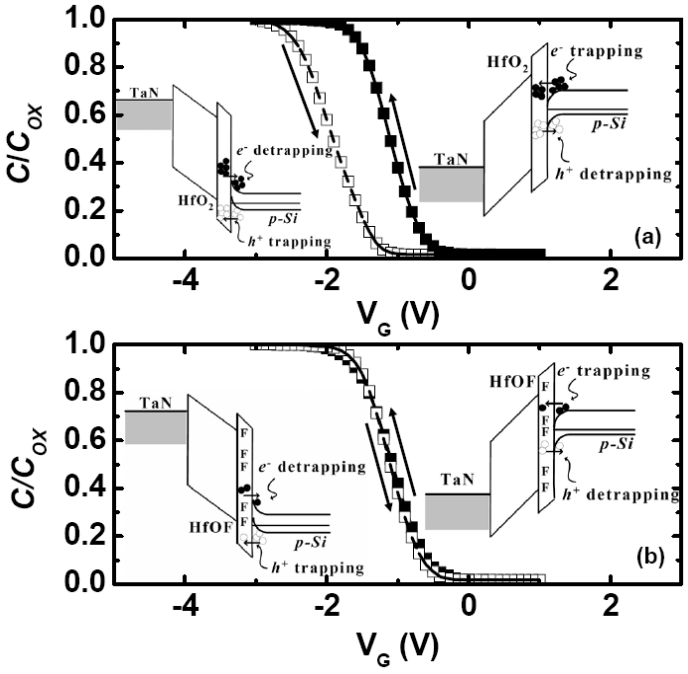


Fig.8. The C-V hysteresis characteristics for the (a) as-deposited and (b) fluorinated HfO_2 gate dielectrics, respectively. The inset band-diagram explains the charge trapping mechanism.

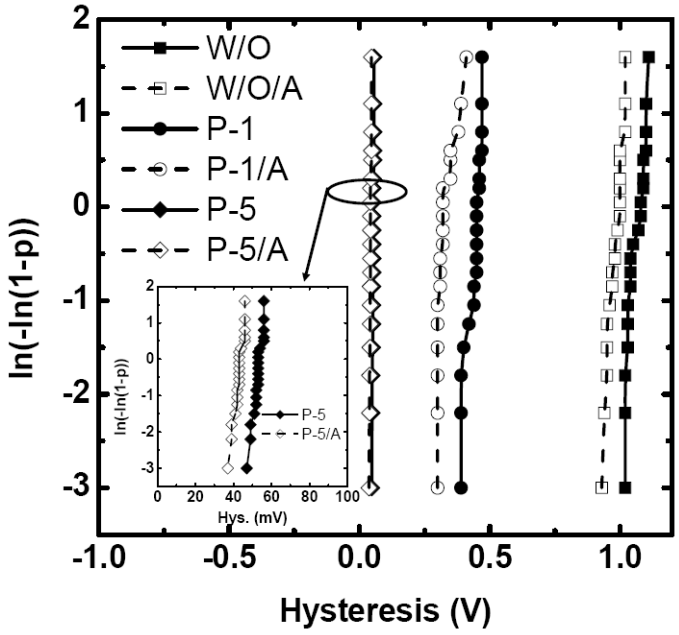


Fig.9. The Weibull distribution of the C-V hysteresis for all samples. Only 50mV C-V hysteresis was observed for the fluorinated HfO_2 gate dielectrics.

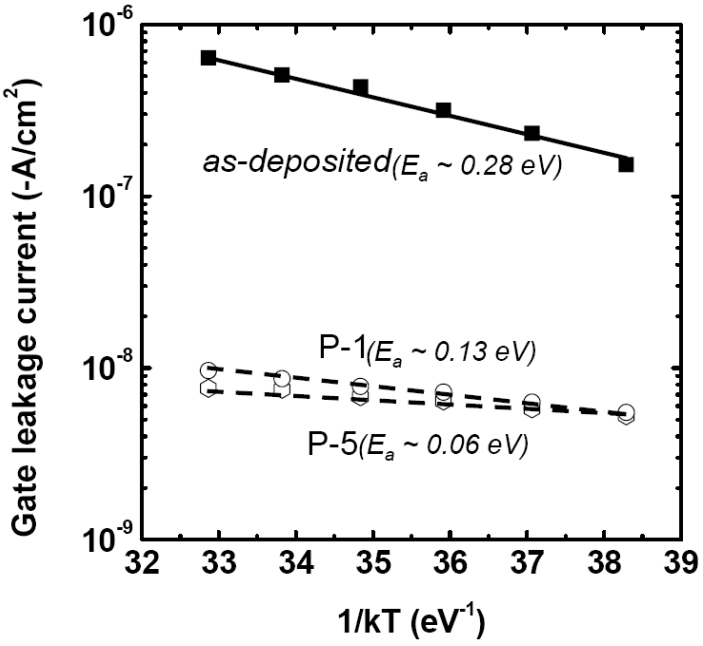


Fig.10. Arrhenius plots of leakage current density for the HfO_2 and fluorinated HfO_2 gate dielectrics. The plots were obtained from the current-voltage characteristics at *V*g = -3 V measured from 303 to 353 K.

Table 3.1 Summaries of the characteristics for all samples. The fluorinated sample exhibits superior properties in EOT, leakage current, breakdown voltage, hysteresis, and charge trapping.

	EOT (nm)	Jg A/cm² @Vg = -3 V	F-P Φ_B (eV)	C-V Hys. (V)	Ea (eV)	$-V_{BD}$ (V)	surface rough. (Å)
as-deposited	2.8	1 x 10^{-7}	1.38	1.1	0.28	6.5	1.05
as-deposited/A	2.68	5 x 10^{-4}	0.93	1	0.27	4.8	
P-1	2.62	9 x 10^{-9}	1.52	0.51	0.13	8	1.74
P-1/A	2.53	1 x 10^{-7}	1.13	0.31	0.13	5.9	
P-5	2.47	7 x 10^{-9}	1.58	0.05	0.06	9	2.03
P-5/A	2.21	1 x 10^{-8}	1.46	0.045	0.06	7	

Chapter 4

Improvement of CMOS Reliability by Post-deposition CF_4 Plasma Treatment

4-1 Improvement of Positive Bias Temperature Instability of HfO_2 nMOSFETs by Post-deposition CF_4 Plasma Treatment

4-1.1 Introduction

As CMOS devices are scaling down aggressively, it has become necessary to identify alternate high-k gate dielectrics that meet the stringent requirements for low leakage current and thin equivalent oxide thickness (EOT) [4.1]-[4.5]. High-k dielectrics are especially advantageous for low-power application and for thickness uniformity control owing to the thicker physical thickness. Among high-k gate dielectric materials, Hf-based gate dielectric including HfO_2 and Hf-silicate are the attractive materials because it has good device characteristics and is compatible with the conventional polysilicon gate process [4.6]-[4.9]. However, before Hf-based gate dielectrics being successfully integrated into future technologies, their reliability characteristics still need to be better identified. Bias temperature instability (BTI) has been recognized as one of the critical concern in the reliability of modern CMOS devices. Many of the past BTI researches on the SiO_2 dielectric have just focused on the negative BTI (NBTI) on PMOS devices [4.10]-[4.11], since it impacts more the devices reliability with respect to positive BTI (PBTI) on NMOS [4.12]. In conventional SiO_2 gate oxides, NMOS under PBTI stress shows little threshold voltage degradation and hence is not a reliability concern while PMOS under NBTI

stress has a continued reliability issue as the gate oxide thickness is scaled thinner. On the contrary, unlike conventional SiO_2 gate dielectrics, NMOS positive bias temperature instability (PBTI) could be a potential scaling limit of CMOS technology with Hf-based gate dielectrics [4.13]. Most of the previous studies showed a significant positive threshold voltage shift for the high-k gate stack under PBTI stressing, which was attributed to the preexisting traps in the high-k layer or the hole induced oxygen vacancy traps [4.14]-[4.18].

Off-state leakage in MOSFET is one of the major issues for device performance degradation, especially for low standby power (LSTP) application. Usually, there is a mixture of contributors to off-state leakage like subthreshold channel leakage, generation of electron hole pairs in the space charge region of the junction, punchthrough, and gate induced drain leakage (GIDL) [4-19]-[4-21]. GIDL current is a leakage between drain and channel which depends on the electrical field in the junction and hence varies with the gate bias. Besides, the reduction of gate oxide thickness causes an increase of the electric field under the gate which makes the transistor more susceptible to GIDL. As a result, the GIDL and its degradation have restricted the scaling of oxide thickness and power supply voltage. Compared to the SiON dielectrics, high-k gate dielectrics can achieve not only I_G reduction but also GIDL suppression because high threshold voltage can be observed with lower channel doping [4-22]. Besides, the GIDL current in HfO_2/SiO_2 stacks will be significantly enhanced due to trap-assisted tunneling by trap existing at the remote HfO_2/SiO_2 interfacial layer [4-23]. However, the mechanism of GIDL degradation for the fluorinated Hf-based dielectrics under PBTI stress has not yet been reported. In this work, the reliability improvement can be presented for the HfO_2 dielectrics with fluorine incorporation. In addition, the mechanism of GIDL degradation for the HfO_2 dielectrics with fluorine incorporation under PBTI and hot carrier stress will be

discussed. Defect passivation in HfO_2/Si by CF_4 plasma treatment will reduce the serious hole-electron pair generation, resulting in less GIDL current.

4-1.2 Experiments

The silicon wafers used in this study were p-type (100) CZ with a resistance of 4~7 Ω · cm. The 500 nm wet oxide was grown at 950 ℃ for device isolation. The device active region was formed by patterning and etching the isolation oxide. Standard RCA cleaning was then performed on all samples. Then, an HfO_2 thin film was then deposited on a HF-last Si surface by an electron beam evaporation system. Hafnium dioxide deposition took place for 2.5 minutes, resulting in the formation of a 5 nm HfO_2 thin film. After HfO_2 thin film deposition, CF_4 plasma was used to treat the HfO_2 thin film to form the fluorinated HfO_2 gate dielectrics. Some samples were treated under CF_4 plasma in the plasma enhance chemical vapor deposition (PECVD) system, whose chamber volume is 3.76×10^5 cm^3. The cathode diameter was 40 cm, and the distance between the cathode and the holder was 4 cm. The sample was loaded into the substrate at an elevated temperature (300 ^oC). The reactive pressure and the flow rate of the CF_4 gas were 600 mtorr and 500 sccm, respectively. The RF power was 40W with CF_4 plasma exposure times of 1 min (termed HfOF). For the normal HfO_2 gate dielectrics samples (denoted as HfO_2), there was no CF_4 plasma treatment after the hafnium dioxide deposition. In a later phase of the investigation, a 50 nm TaN metal gate was also deposited by the RF sputter method. The source and drain regions in the active device region were implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 900 ℃ for 30 s annealing in a N_2 ambient. After the patterning of source/drain contact holes, an aluminum film of 300 nm thickness was then deposited on the TaN gate for use as the gate electrode and source/drain contact

pad. Then, the devices were completed by the contact pad definition. Finally, the 300 nm aluminum film was evaporated from the bottom of the electrode by a thermal evaporator.

The electrical properties were analyzed by an HP 4285 for capacitance-voltage (C-V) characteristics at 100 kHz, and the capacitance effective thickness (CET) was extracted from the capacitance under the accumulation region without considering the quantum effects. The current-voltage (I-V) curves were measured by a Keithly 4200. Further, the I-V characteristics were measured at elevated temperature (300-383 K) in order to study the charge trapping and gate induced leakage current (GIDL) mechanisms of the fluorinated HfO_2 nMOSFETs, respectively. Devices with gate length (L) and width (W) of 10 and 100 μm were measured. The V_{TH} is defined as the gate voltage at which the drain current reaches 100 nA $\times$W/L and V_D = 0.1 V. The transfer characteristics I_D –V_G of HfO_2 nMOSFETs are measured at V_D = 0.1 and 1 V, and V_G = −1.5 to 1 V.

4-1.3 Results and Discussions

Figure 4.1 shows the C-V curves of the HfO_2 nMOSFETs with and without CF_4 plasma treatment. The excellent C-V characteristics can be observed for both as-deposited and CF_4 plasma treated samples. The CET extracted from these C-V curves are 1.93 nm for the as-deposited sample and 1.86 nm for the fluorinated one, respectively. The CET reduction of the CF_4 treated sample can be explained by F atoms incorporation into HfO_2 layer. The fluorine atoms can be bonded to Hf (or Si) dangling bonds resulting in annihilation of oxygen vacancies. Besides, the fluorine incorporation will effectively eliminate some shallow traps in HfO_2 thin films resulting in lower F-P conduction leakage current for fluorinated HfO_2 gate dielectrics.

This shallow trap elimination will be discussed in the next paragraph.

The temperature dependence of the gate leakage current was studied to understand the current transport mechanisms. The gate leakage currents were measured from 303 K to 383 K under gate electron injection as shown in Fig. 4.2. The gate leakage current increases with increasing measuring temperature for all samples, showing obvious temperature dependence. To further investigate the carrier transportation of as-deposited and fluorinated HfO_2 gate dielectrics, the Frenkel-Poole (F-P) conduction fitting is performed, as shown in the inset in Fig. 4.3. The data in the inset of Fig. 4.3 was extracted from good F-P fitting ($J = E_{OX} \times \exp\left\{-q\left[\Phi_B - \left(qE_{OX} - \pi\varepsilon_i\right)^{1/2}\right]/kT\right\}$) [2.38], where Φ_B is the effective F-P barrier, ε_i is dielectric constant of SiO_2. The electric field (E_{OX}=V/T_{OX}) is an "effective" electric field due to T_{OX} is CET. As a result, Φ_B is named as effective F-P barrier, which is determined by the effective electric field (E_{OX}). Figure 4.4 indicated the effective F-P barriers at elevated temperature. The extracted trap energy (Φ_B) at room temperature for the as-deposited sample is 0.93 eV from the conduction band of HfO_2, while that of the fluorinated sample is about 1.02 eV. As the temperature increases, the increase in the effective trapping level is easily observed, meaning that the deep traps in HfO_2 and HfOF films can be observed at high temperature. The Φ_B at 110 ℃ for the as-deposited sample is 1.02 eV from the conduction band of HfO_2, while that of the fluorinated sample is about 1.12 eV. To sum up, the HfOF film has deeper trapping level, indicating that most of the shallow traps in HfO_2 film can be eliminated using this CF_4 plasma treatment technique.

Figure 4.5 shows the I_D-V_G transfer characteristics of the as-deposited and CF_4 plasma treated HfO_2 nMOSFETs, where the device channel length and width were 10 and 100 μm, as mentioned above. High-performance characteristics of HfO_2

nMOSFETs with excellent S. S. ~84 mV/dec, high mobility ~163 $cm^2/V \cdot s$, and high I_{ON}/I_{min} current ratio ~3.23×10^7 are observed without any treatment. For the CF_4 treated one, we can observe that the I_{min} is reduced significantly from 10.07 to 6.05 pA at V_D = 0.1 V, enhanced I_{ON}/I_{min} current ratio (~6.69×10^7), and improved S. S. (~76 mV/dec). In addition, the drain induced barrier lowering (DIBL) was less than 20 mV for all samples as shown in Fig. 4.5. By the same token, the driving current of the fluorinated device was larger than that of conventional devices, as indicated in Fig. 4.6. The driving current of the CF_4 treated device with 10 *u*m gate length showed a 28 % increase over the as-deposited device at V_D = 2 V and V_G-V_{th} = 1.5 V, as shown in Fig. 4.6. The driving current increases with applied gate bias increasing. In addition, the transconductance (g_m) extracted from linear region (V_D = 0.1 V) also increased for the fluorinated device (Fig. 4.7). Only a little 8 % increase can be observed for the fluorinated device with 10 *u*m gate length, by comparison with the as-deposited one. However, the mobility improvement for the fluorinated sample was more pronounced in the higher electric field. A roughly 43 % increase can be observed while the V_G-V_{th} = 1 V. This can be speculated to the improved surface roughness, since fluorine incorporation into HfO_2 film can effectively passivate HfO_2/Si interface. As a result, the surface roughness of HfO_2/Si interface can be effectively improved for the fluorinated sample.

As mentioned above, the I_{min} reduction can be observed for the fluorinated sample. Besides this, the GIDL current also decreased for the fluorinated device, as illustrated in Fig. 4.4, especially for the large drain biasing (V_D = 1 V). In Fig. 4.8, the I_D-V_G curves and I_{SUB} current at various drain and gate bias conditions are shown. The GIDL improvement of fluorinated sample was more obvious when the high drain bias was applied, as shown in Fig. 4.8(b). The substrate current is the same as GIDL current for all samples, indicating that the impact ionization dominates GIDL

phenomenon. Besides, the GIDL current and substrate current increase as measuring temperature increase, as indicated in Fig. 4.9. However, the GIDL increase is much suppressed for the fluorinated device. There is almost no different between room temperature and 70 ℃ for the GIDL current of CF_4 treated HfO_2 nMOSFETs. In the significant V_D and negative V_G bias region, the drain-to-gate bias is sufficiently high to deplete and even invert the n^+ drain region under the gate. This causes enhanced electric field and band bending, resulting in a dramatic increase of high field effects, such as avalanche multiplication and band-to-band tunneling (BTBT). The possibility of tunneling via traps (trap-assisted tunneling) also increases. These high-field effects cause hole-electron pair generation. The electrons tunnel to the drain and contribute to the GIDL current. The holes are swept to the substrate and contribute to the substrate current. The higher electric field due to the higher density of interface traps increases the role of this current component in the high-κ devices [4-23]. The detail GIDL degradation mechanism will be discussed in next paragraph.

To understand the mechanism of PBTI in our high-k dielectrics, Fig. 4.10 shows the I_D-V_G transfer characteristics of the as-deposited and CF_4 plasma treated HfO_2 nMOSFETs under the same PBTI stress (V_G-V_{th} = 2 V) at room temperature. The S. S. is almost the same for all samples, only V_{TH} shift and GIDL increase can be observed during PBTI stress. These results mean that generated oxide trap will dominate the PBTI degradation characteristics. It is worth to note that the HfOF dielectric leads to an obvious reduction in ΔV_{TH} under PBTI stress. This result demonstrates that the HfOF thin film quality is better than HfO_2. As mentioned previous, the HfOF gate dielectrics had the extra Si-F and Hf-F bodings resulting in annihilation of oxygen vacancies and PBTI reduction for HfOF dielectrics. Figure 4.11 demonstrated the ΔV_{TH} under PBTI stress at different temperatures (RT~100 ℃) for (a) HfO_2 dielectrics and (b) HfOF dielectrics, respectively. The ΔV_{TH} in PBTI stress increase

with increasing measuring temperature for both HfO_2 and HfOF gate dielectrics. The difference of threshold voltage degradation under PBTI stress between HfO_2 and HfOF gate dielectrics is not quite apparent. However, the change of ΔV_{TH} in PBTI stress at different temperature is quite different between HfO_2 and HfOF gate dielectrics, as indicated in Fig. 4.12. The slope of ΔV_{TH} at different temperatures (50~70 ℃) for HfOF gate dielectric is larger than that for HfO_2 gate dielectric, indicating that the HfOF gate dielectric has deeper charge trapping, which is consistent with Fig. 4.4. However, the slope at different temperatures (70~100 ℃) of HfO_2 gate dielectric becomes larger than that of HfOF gate dielectric. At the same time, the ΔV_{TH} of HfO_2 gate dielectric is still larger than that of HfOF gate dielectric. Therefore, the increase in ΔV_{TH} of HfO_2 gate dielectric is attributed to the deep charge trapping, which has obvious temperature dependence at the quite high temperature (>70 ℃).

On the other hand, it is worth to note that GIDL improvement during PBTI stress is more obvious for the HfOF gate dielectrics, especially for the high temperature, as shown in Fig. 4.10. Figure 4.13 demonstrated the GIDL current after 1000s PBTI stress at different temperatures for as-deposited and CF_4 treated samples. The GIDL current increases with measuring temperature increasing for all samples. However, the obvious GIDL improvement can be observed for the fluorinated device, especially at high temperature. As mentioned above, enhanced electric field and band bending resulted in a dramatic increase of high field effects, such as band-to-band tunneling and trap-assisted tunneling. Then, it causes large hole-electron pair generation, and the electrons tunnel to the drain and contribute to the GIDL current, as shown in Fig. 4.14. Furthermore, M. Gurfinkel et. al., proposed that the trap-assisted tunneling will dominates the GIDL degradation of high-k device. Besides this, the conventional band-to-band tunneling (electron direct tunneling) can also be observed, as shown in

Fig. 4.15. As a result, the PBTI stress induced GIDL degradation will become more obvious for the high-k device, especially for trap-assisted tunneling induced GIDL current. In this work, this serious GIDL degradation can be observed for the HfO_2 nMOSFET at large V_D (Fig. 4.8-4.9) and PBTI stress. Generally speaking, PBTI stress not only generated oxide trap but degraded HfO_2/Si interface, resulting in increase of trap-assisted tunneling. However, the accumulation of fluorine atoms the interfaces of the gate dielectrics, and some fluorine atoms accumulated in the bulk HfO_2 thin film, resulting in bulk HfO_2 thin film and interface passivation by CF_4 plasma treatment. Then, the trap-assisted tunneling phenomenon can be much suppressed for the HfOF nMOSFET during PBTI stress, resulting in GIDL improvement.

To understand the interface characterization of our high-k dielectrics, Fig. 4.16 shows the I_D-V_G transfer characteristics of the as-deposited and CF_4 plasma treated HfO_2 nMOSFETs under the same hot carrier (HC) stress (V_G-V_{th} = 1.5 V, V_D = 3 V) at room temperature. Obvious V_{TH} shift and GIDL increase can be observed for the HfO_2 nMOSFET during HC-stress. These results mean that large impact ionization will dominate the HC-stress degradation characteristics. The observation of large substrate current after HC-stress also proves that impact ionization will degrade HfO_2/Si interface characterization. It is worth to note that the HfOF nMOSFET leads to an obvious reduction in ΔV_{TH} under HC-stress. This result demonstrates that the better interface characterization of high-k device can be achieved using post-deposition CF_4 plasma treatment. As mentioned previous, the HfOF gate dielectrics had the extra Si-F boding resulting in defect passivation in HfO_2/Si interface, resulting in HC reliability improvement for HfOF dielectrics. Besides, the large impact ionization will induce serious hole-electron pair generation, resulting in larger GIDL current, as shown in HfO_2 nMOSFET (Fig. 4.16(a)). However, the GIDL

degradation can be much improved for the HfOF nMOSFET as shown in Fig. 4.16(b). The same as mentioned above, defect passivation in HfO_2/Si for the HfOF nMOSFET will reduce the serious hole-electron pair generation, resulting in less GIDL current. The serious HC-stress induced V_{TH} shift and GIDL increase can be observed at high temperature, as shown in Fig. 4.17. Figure 4.18 demonstrated the ΔV_{TH} under HC-stress at different temperatures (RT~50 ℃) for (a) HfO_2 dielectrics and (b) HfOF nMOSFETs, respectively. The ΔV_{TH} in HC-stress increase with increasing measuring temperature for both HfO_2 and HfOF nMOSFETs. The difference of threshold voltage degradation under PBTI stress between HfO_2 and HfOF gate dielectrics is not quite apparent. However, the less ΔV_{TH} can be observed for the HfOF nMOSFET at elevated temperature due to better interface characterization. Figure 4.19 demonstrated the GIDL current after 1000s HC-stress at different temperatures for as-deposited and CF_4 treated samples. The GIDL current increases with measuring temperature increasing for all samples. However, the obvious GIDL improvement can be observed for the fluorinated device, especially at high temperature.

4-1.4 Summary

For the first time, a novel high-performance and excellent-reliability HfOF nMOSFET was demonstrated. Large I_{ON}/I_{min} current ratio (~6.69×10^7), good S. S. (~76 mV/dec), small DIBL (<20 mV), and high mobility (~165 $cm^2/V \cdot s$) can be observed for the HfOF nMOSFETs. The HfOF nMOSFET has better HfO_2/Si interface and dielectric quality, including GIDL current and less PBTI effect. Reduced GIDL current was observed for the HfOF nMOSFET due to HfO_2/Si interface passivation by fluorine, resulting in less hole-electron pair generation. The fluorine incorporation into HfO_2 gate dielectrics effectively passivated the dielectric vacancies,

resulting in a deeper trapping cross section and a lower concentration of generated traps. These results provide a valuable guideline for future 32 nm and beyond CMOS device designs with high-k dielectrics with fluorine incorporation.

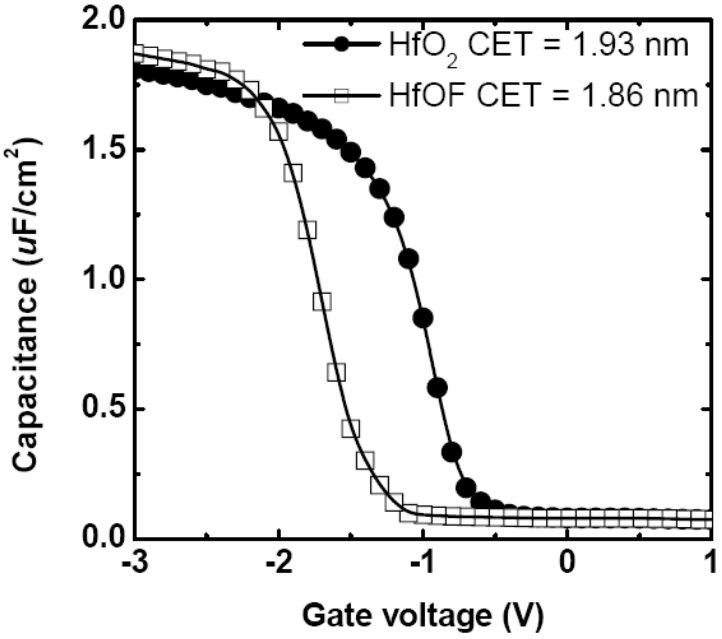
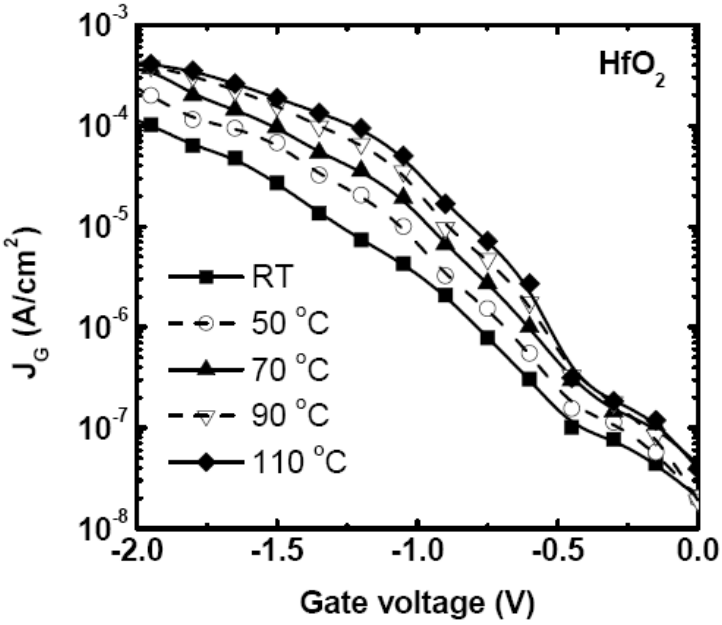
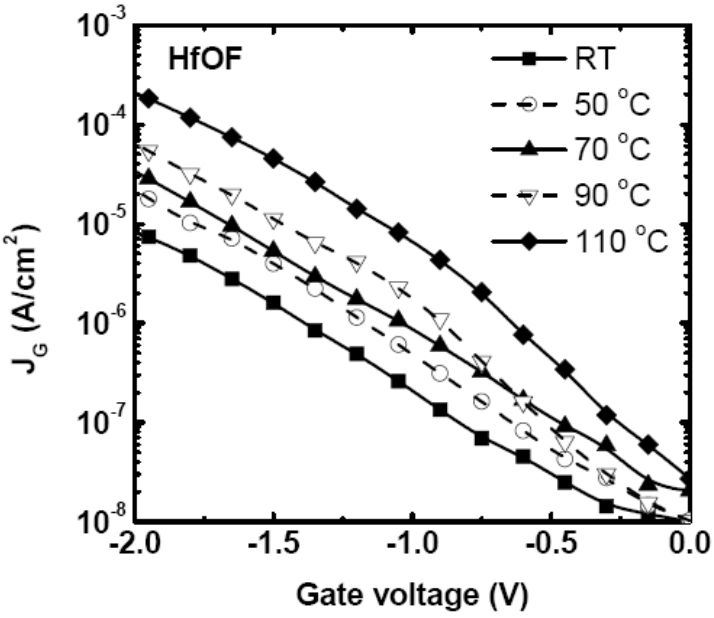


Fig. 4.1 C-V curves of the HfO_2 nMOSFETs with and without CF_4 plasma treatment.

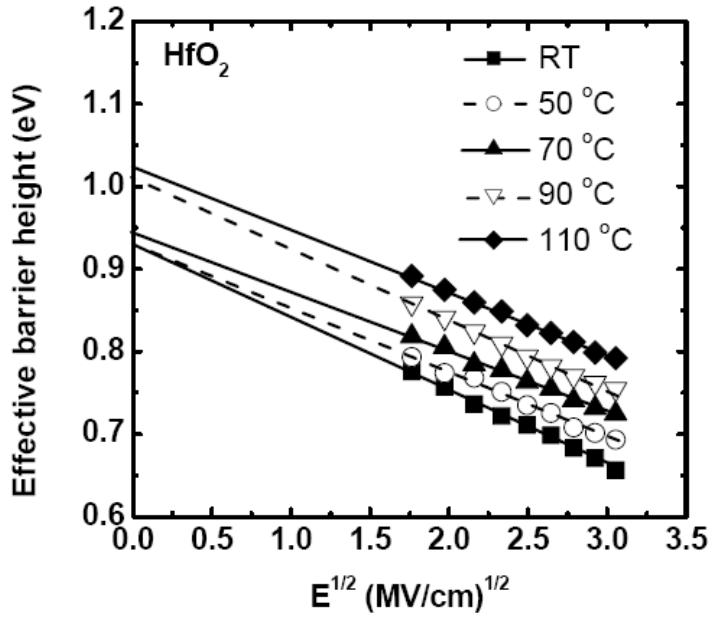


(a)

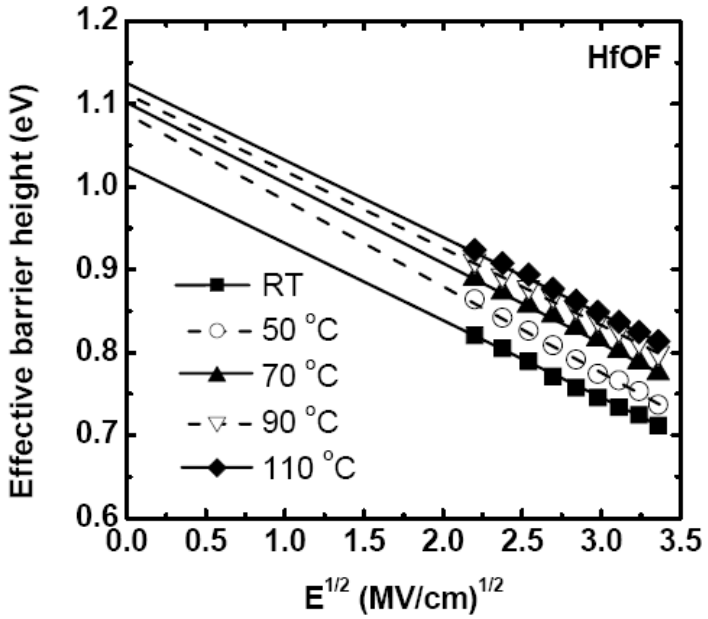


(b)

Fig. 4.2 gate leakage currents measured from 303 K to 383 K under gate electron injection for (a) HfO_2 and (b) HfOF gate dielectrics, respectively.



(a)



(b)

Fig. 4.3 Well Frenkel-Poole (F-P) conduction fitting for (a) HfO_2 and (b) HfOF gate dielectrics, respectively.

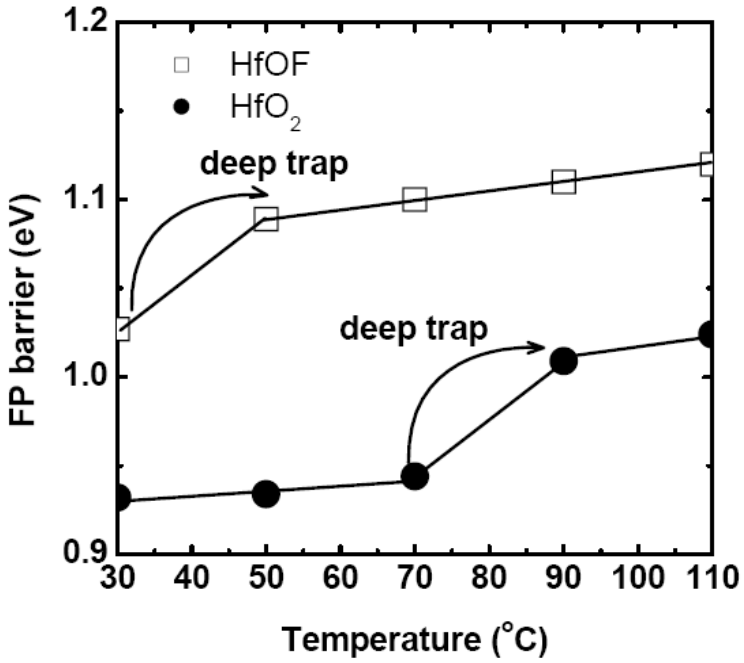
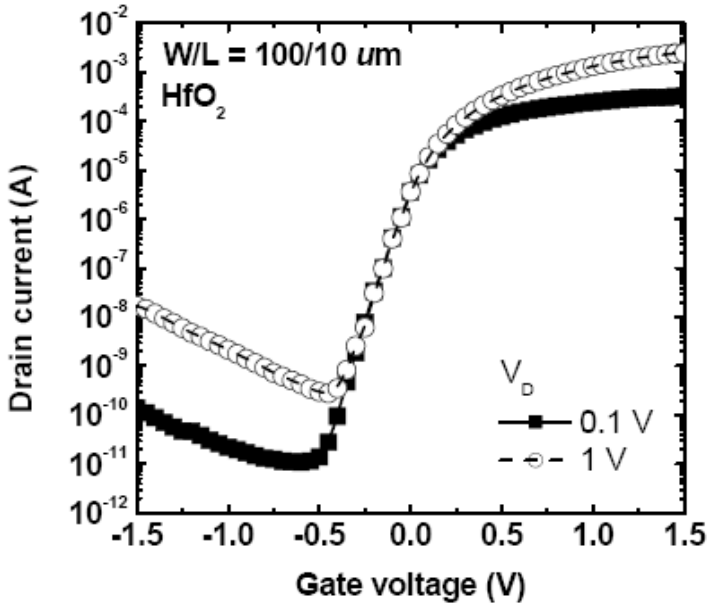
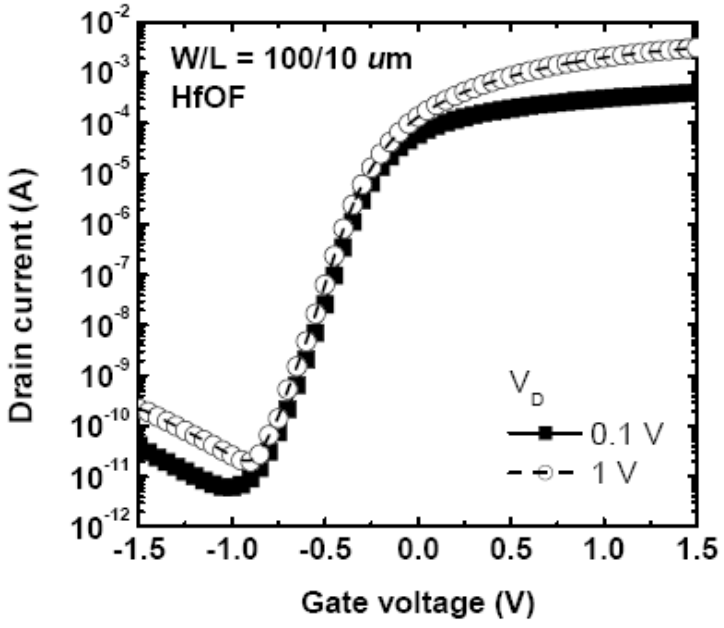


Fig. 4.4 Effective F-P barriers at elevated temperature for (a) HfO_2 and (b) HfOF gate dielectrics, respectively.



(a)



(b)

Fig. 4.5 I_D-V_G transfer characteristics of (a) as-deposited and (b) CF_4 plasma treated HfO_2 nMOSFETs, where the device channel length and width were 10 and 100 μm.

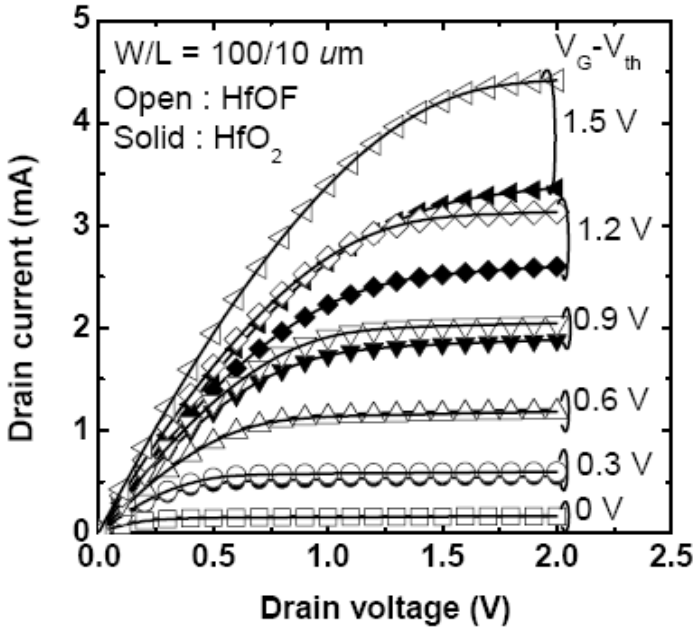


Fig. 4.6 I_D-V_D characteristics of as-deposited and CF_4 plasma treated HfO_2 nMOSFETs, where the device channel length and width were 10 and 100 μm.

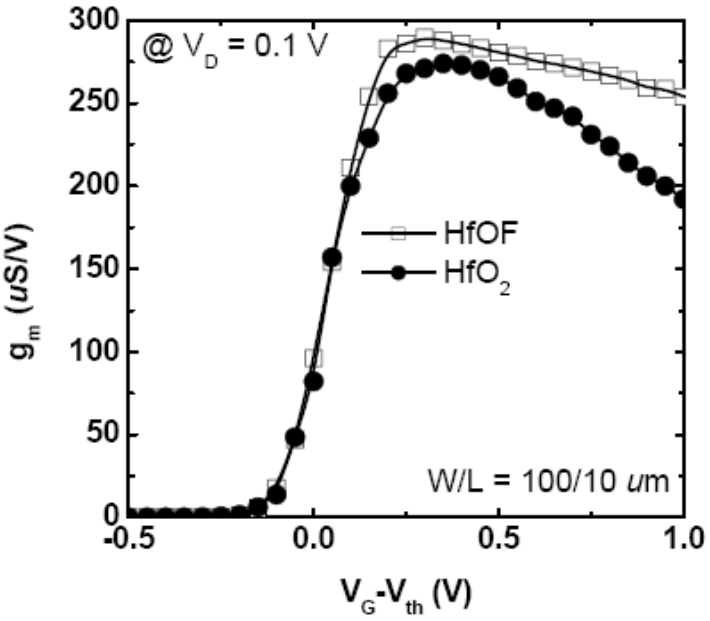
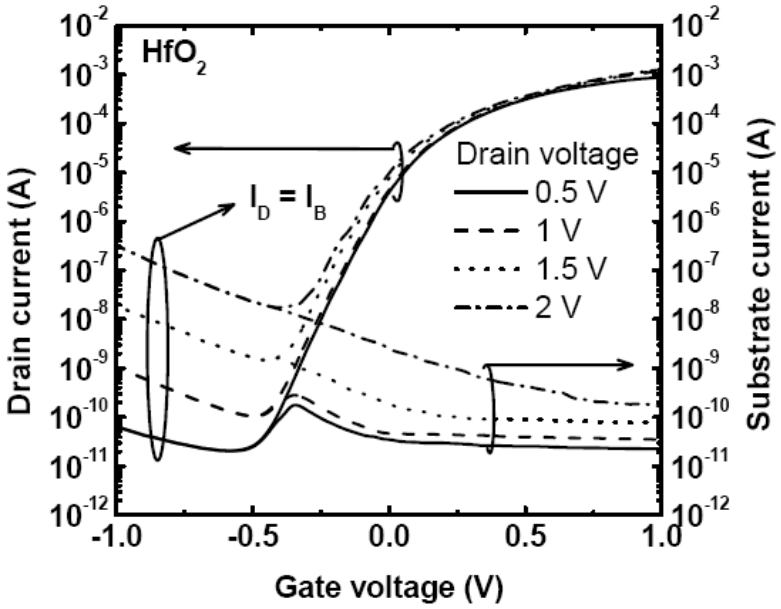
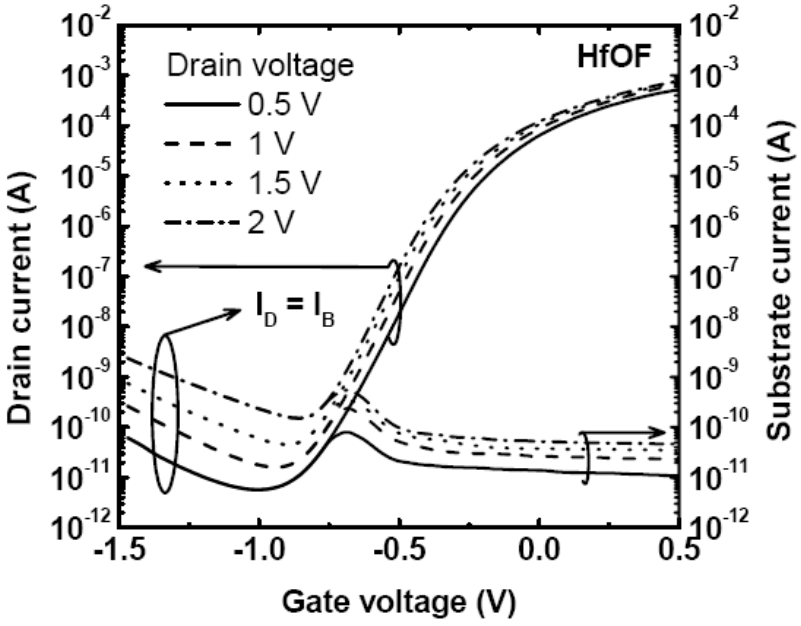


Fig. 4.7 transconductance (g_m) extracted from linear region (V_D = 0.1 V) for the as-deposited and fluorinated HfO_2 nMOSFETs.

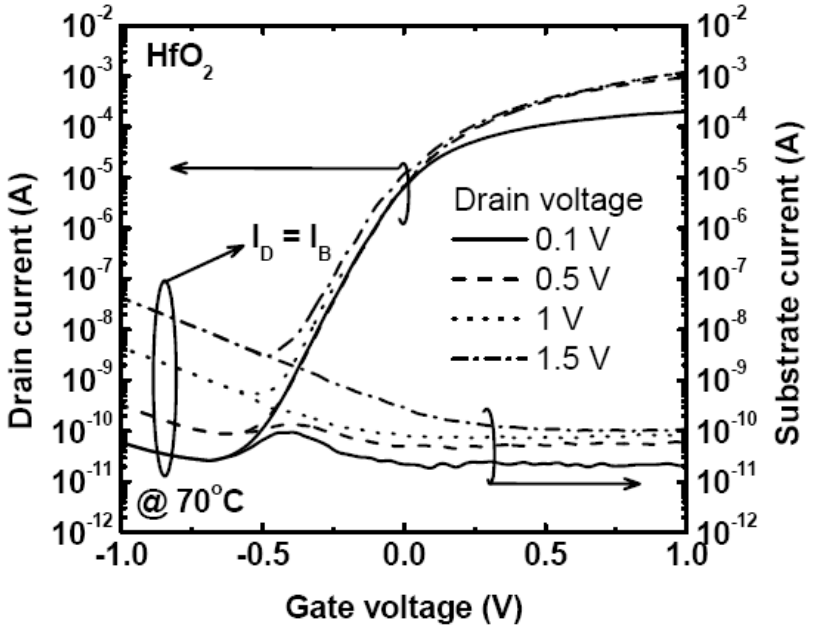


(a)

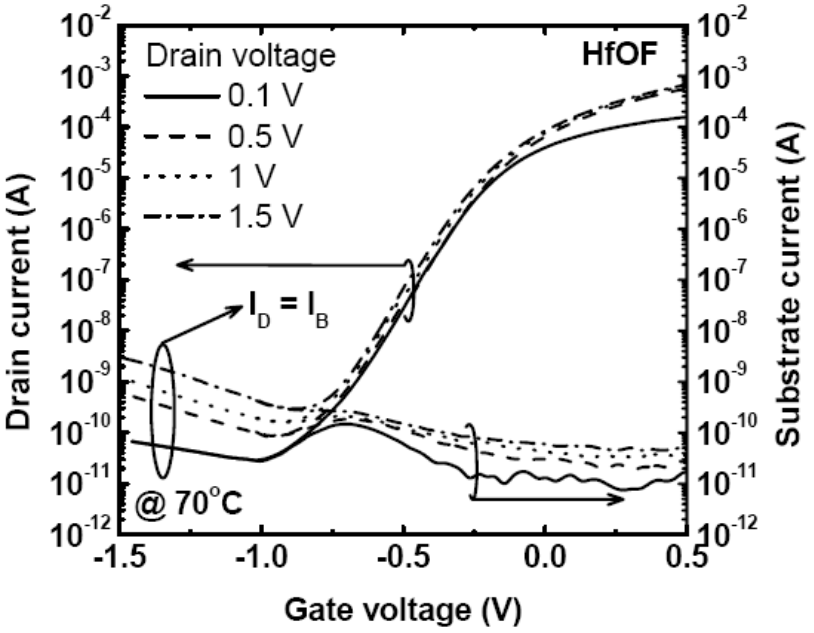


(b)

Fig. 4.8 I_D-V_G curves and I_{SUB} current at various drain and gate bias conditions of (a) as-deposited and (b) CF_4 plasma treated HfO_2 nMOSFETs.

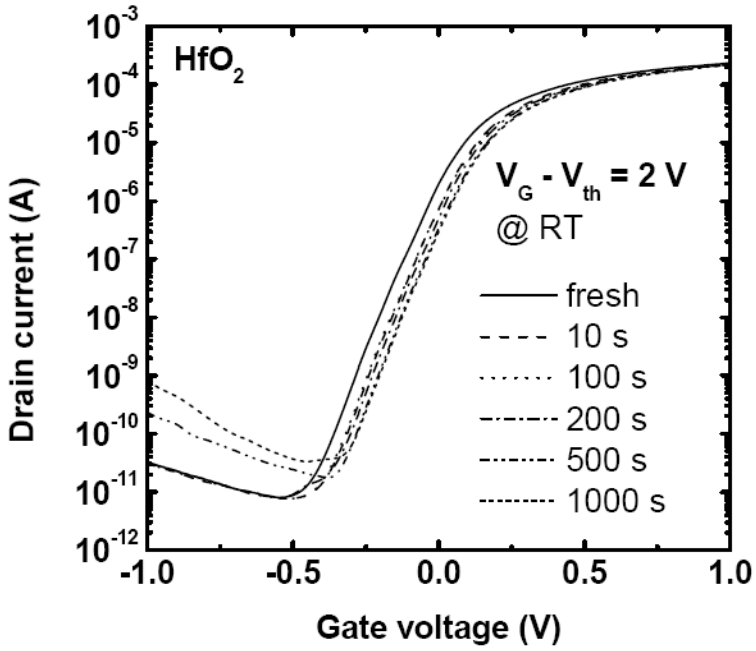


(a)

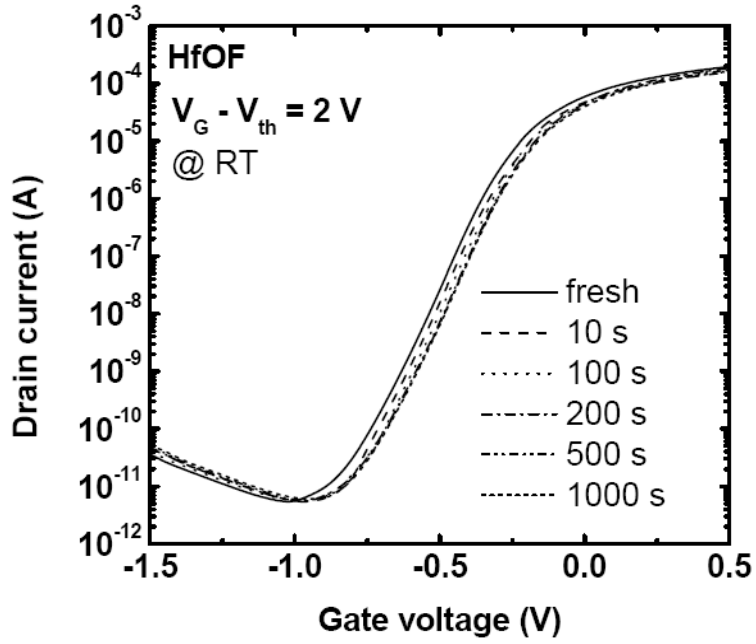


(b)

Fig. 4.9 I_D-V_G curves and I_{SUB} current at various drain and gate bias conditions of (a) as-deposited and (b) CF_4 plasma treated HfO_2 nMOSFETs at 70 ℃.

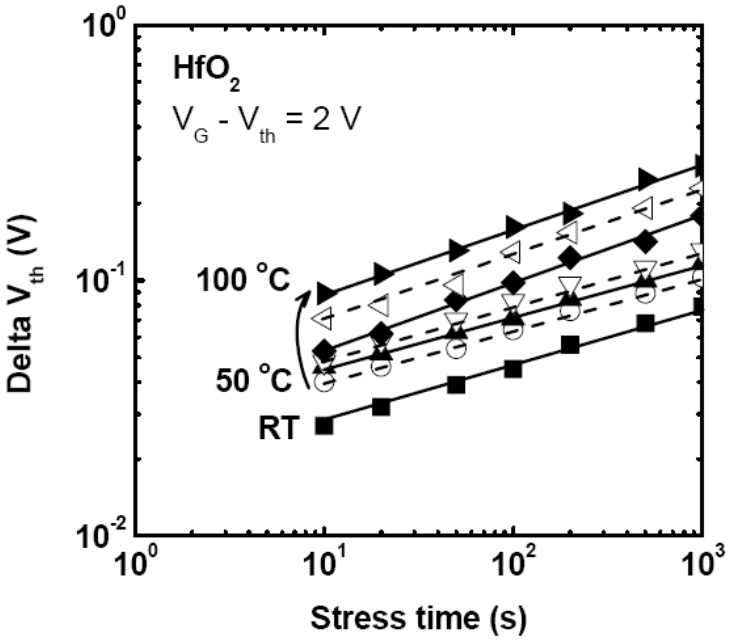


(a)

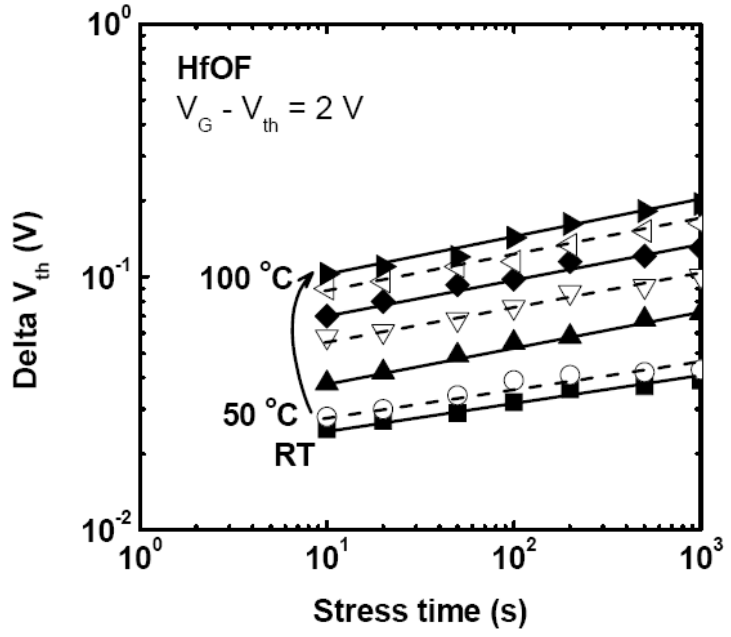


(b)

Fig. 4.10 I_D-V_G transfer characteristics of (a) as-deposited and (b) CF_4 plasma treated HfO_2 nMOSFETs under the same PBTI stress (V_G-V_{th} = 2 V) at room temperature.



(a)



(b)

Fig. 4.11 ΔV_{TH} under PBTI stress at different temperatures (RT~100 ℃) for (a) HfO_2 dielectrics and (b) HfOF dielectrics, respectively.

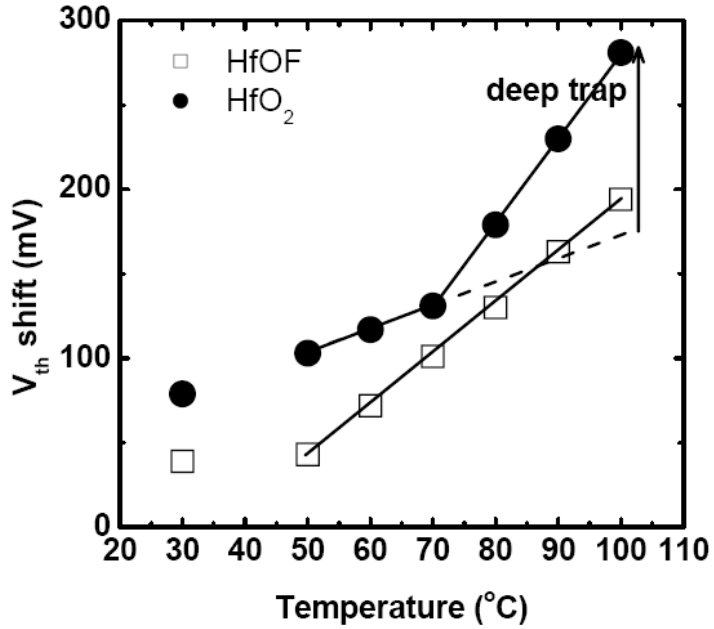


Fig. 4.12 ΔV_{TH} afte 1000s PBTI stress at different temperature is quite different between HfO_2 and HfOF gate dielectrics.

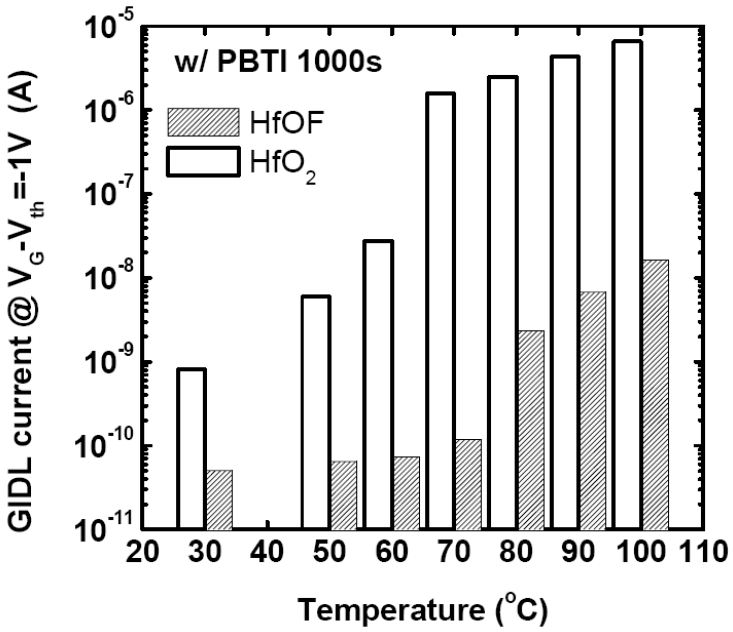


Fig. 4.13 The GIDL current after 1000s PBTI stress at different temperatures for as-deposited and CF_4 treated samples.

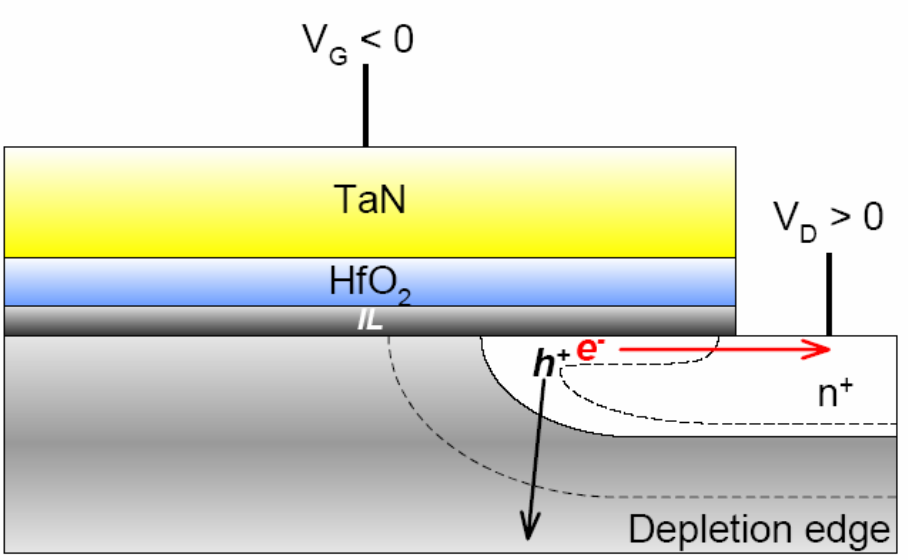


Fig. 4.14 GIDL mechanism: the electrons tunnel to the drain and contribute to the GIDL current. The holes are swept to the substrate and contribute to the substrate current.

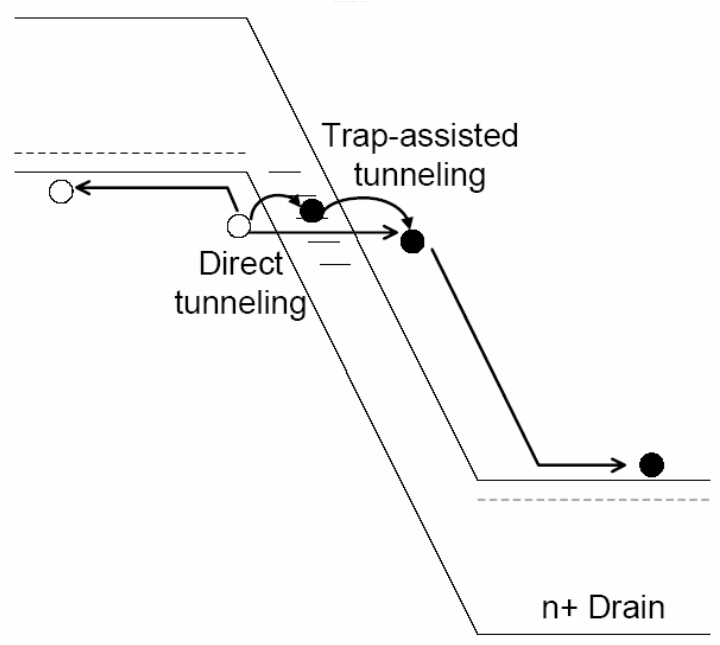
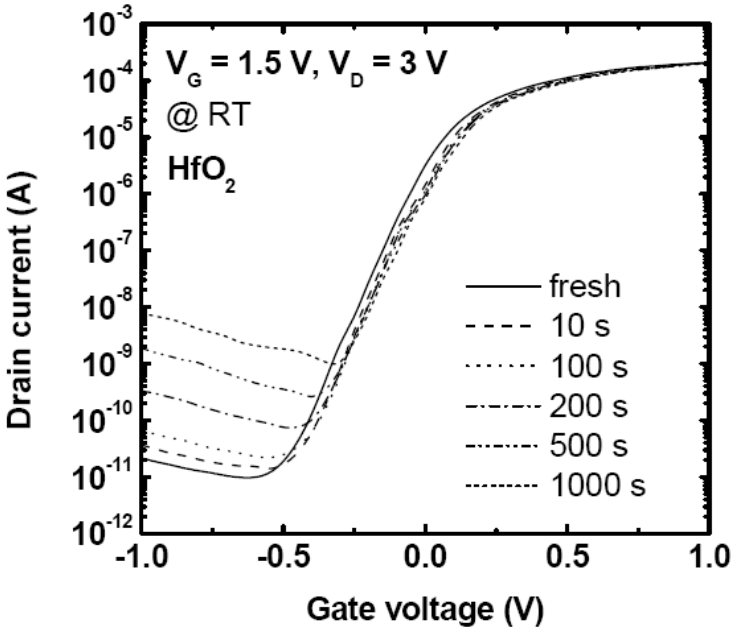
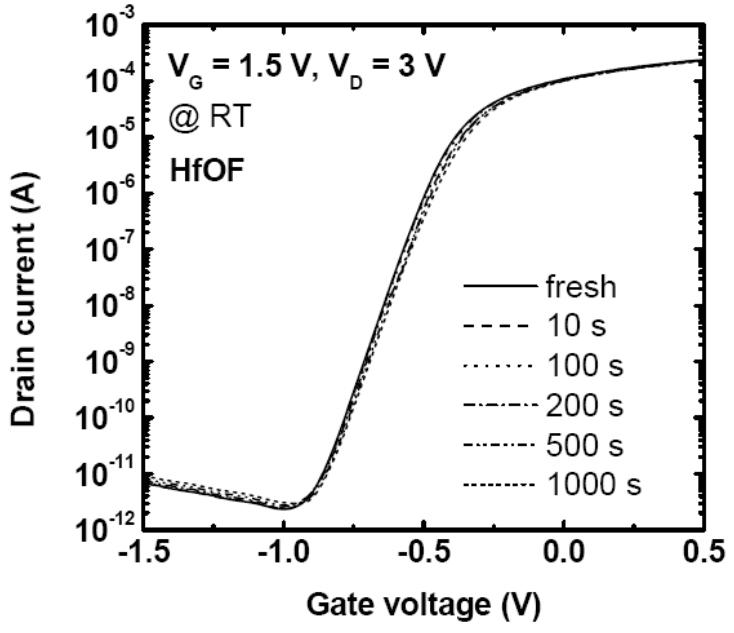


Fig. 4.15 Band diagram of suggested GIDL mechanism: GIDL current includes trap-assisted tunneling and conventional band-to-band tunneling (electron direct tunneling) currents.

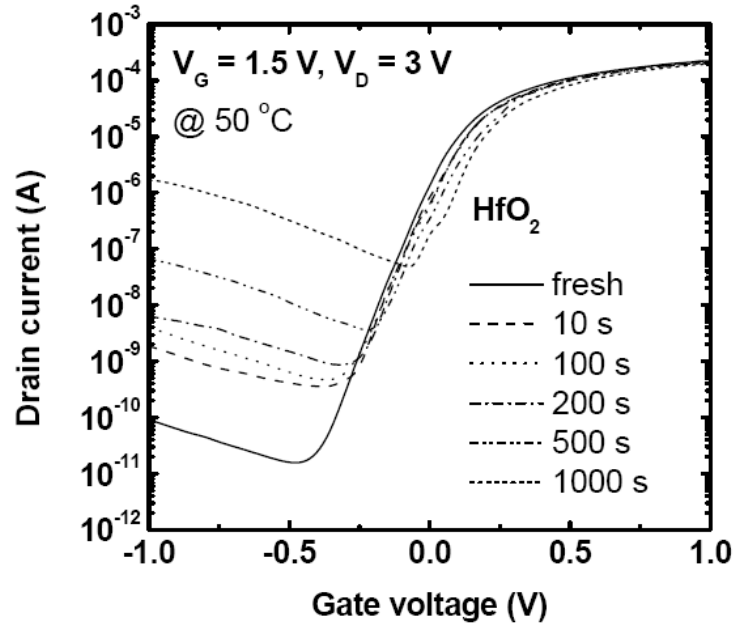


(a)

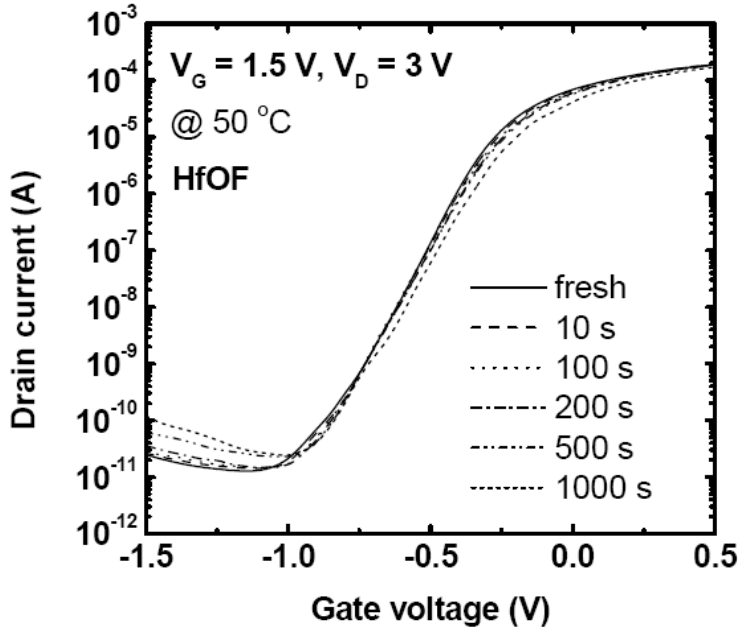


(b)

Fig. 4.16 I_D-V_G transfer characteristics of (a) as-deposited and (b) CF_4 plasma treated HfO_2 nMOSFETs under the same hot carrier (HC) stress (V_G-V_{th} = 1.5 V, V_D = 3 V) at room temperature.



(a)



(b)

Fig. 4.17 I_D-V_G transfer characteristics of (a) as-deposited and (b) CF_4 plasma treated HfO_2 nMOSFETs under the same hot carrier (HC) stress (V_G-V_{th} = 1.5 V, V_D = 3 V) at 50 ℃.

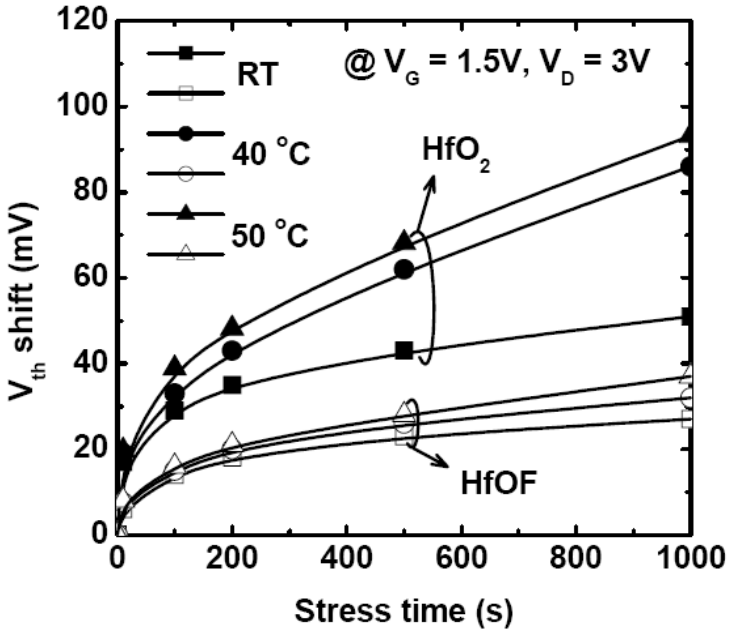


Fig. 4.18 ΔV_{TH} under HC-stress at different temperatures (RT~50 ℃) for HfO_2 dielectrics and HfOF dielectrics, respectively.

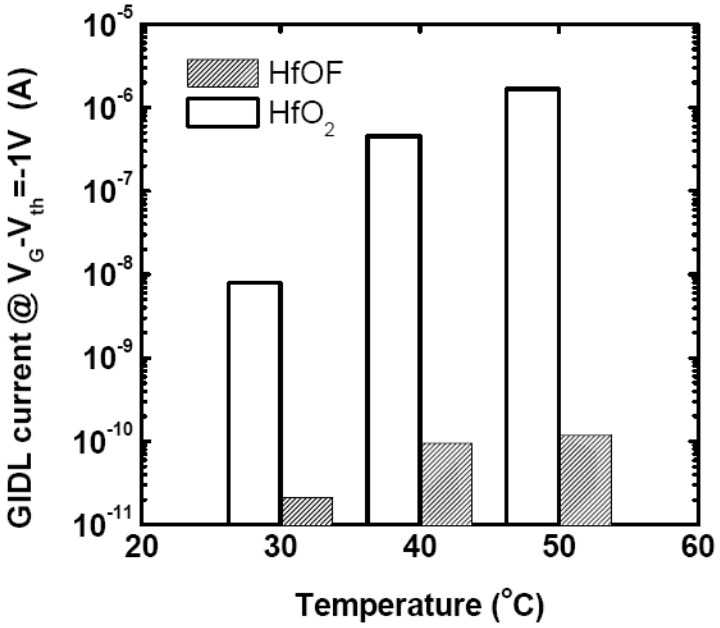


Fig. 4.19 The GIDL current after 1000s HC-stress at different temperatures for HfO_2 dielectrics and HfOF dielectrics, respectively.

4-2 Improved Characteristics of HfO_2 pMOSFETs by Post-deposition CF_4 Plasma Treatment

4-2.1 Introduction

Negative bias temperature instability (NBTI) of p-MOSFET devices is an important reliability concern [4.24]–[4.39]. It results in power-law time dependent degradation of device parameters, like threshold voltage, linear drain–current, etc., with historically measured exponent values of n ~ 0.2–0.3 [4.24]–[4.30]. It is driven by oxide electric field and not by gate voltage [4.25], [4.30], [4.35]. It gets aggravated at higher temperature, and classically shows Arrhenius T activation with energy E_A ~ 0.1–0.2 eV [4.29], [4.35]. It is further aggravated with incorporation of nitrogen in gate oxides (to prevent boron penetration and reduce gate leakage), and severely affect device lifetime for oxynitride devices [4.27], [4.28], [4.38]–[4.39]. Finally, NBTI physical mechanism must be properly understood and modeled for accurate extrapolation from stress (high voltage, short time) to operating (low voltage, long time) condition. For pure SiO_2 gate dielectric films, NBTI is believed due to generation of interface traps (N_{IT}) at the Si-SiO_2 interface. Although various models [4.25], [4.31]–[4.37] have been put forward to explain N_{IT} generation, the reaction-diffusion (R-D) model [4.25], [4.33]–[4.36] has been most widely accepted. According to R-D model, ≡ Si–H bonds at Si-SiO_2 interface is broken by inversion layer holes (reaction) and the released H species subsequently move away from the interface (diffusion) and create N_{IT} (≡ Si−). Except for very short time, the time evolution of N_{IT} is governed by diffusion and the nature of diffusing species determines n. It is shown that n = 1/4 for atomic hydrogen (H^0), n = 1/6 for molecular hydrogen (H_2) and n = 1/2 for protons (H^+) [4.36]. The observed spread in time

exponents can be explained by (a) mix of diffusing species, (b) H^0 or H^+ species undergoing dispersive transport [4.35], [4.37], and (c) H_2 diffusion and impact of measurement delay [4.40].

It is generally conceived that introduction of high-k gate dielectrics is inevitable at the technology nodes of 50 nm and beyond, in order to satisfy the stand-by power requirement without sacrificing metal oxide semiconductor field effect transistor (MOSFET) performance. Conventional SiO_2 cannot satisfy the requirement of these technology nodes due to the quantum-mechanical direct tunneling current [4.41] and reliability concerns [4.42]. HfO_2 is considered one of the most promising high-k dielectrics. As the basic performance of the HfO_2 MOSFETs has been improved, more attention is being focused on reliability characterizations. Although there have been several reports on this issue, most of them dealt with time-dependent dielectric breakdown (TDDB) [4.43]–[4.45]. Degradations in device characteristics due to electrical stressing, such as BTI and hot-carrier injection (HCI), have not been fully investigated yet. It is generally recognized that has a significantly larger amount of charge traps than that in HfO_2. Gusev *et al.* has investigated the traps on deposited by atomic layer deposition (ALD) [4.46], and the same group also observed a significant amount of traps by hot-carrier injection [4.47]. Onishi *et al.* has been evaluating the trapping characteristics on PVD due to BTI. They found that NBTI on pMOSFETs exhibited sufficient lifetime [4.48]. On the other hand, NBTI lifetime was deteriorated by the introduction of an surface nitridation (SN) technique [4.48], which had been effectively used in scaling equivalent oxide thickness (EOT) of and suppressing boron penetration [4.49], [4.50]. Besides, unlike SiO_2, NMOS PBTI could be a potential scaling limit of HfO_2 [4.51]. However, we have found that the PBTI can be much suppressed for the HfO_2 with post-deposition CF_4 plasma treatment, as mentioned in chapter 4.2. In this section, we'll demonstrate the performance and reliability

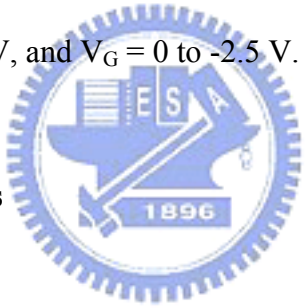
improvement of HfO_2 pMOSFET by post-deposition CF_4 plasma treatment, especially for NBTI. Besides, defect passivation in HfO_2/Si by CF_4 plasma treatment will reduce the serious hole-electron pair generation, resulting in less GIDL current.

4-2.2 Experiments

The silicon wafers used in this study were n-type (100) CZ with a resistance of 4~7 Ω · cm. The 500 nm wet oxide was grown at 950 ℃ for device isolation. The device active region was formed by patterning and etching the isolation oxide. Standard RCA cleaning was then performed on all samples. Then, an HfO_2 thin film was then deposited on a HF-last Si surface by an electron beam evaporation system. Hafnium dioxide deposition took place for 2.5 minutes, resulting in the formation of a 5 nm HfO_2 thin film. After HfO_2 thin film deposition, CF_4 plasma was used to treat the HfO_2 thin film to form the fluorinated HfO_2 gate dielectrics. Some samples were treated under CF_4 plasma in the plasma enhance chemical vapor deposition (PECVD) system, whose chamber volume is 3.76×10^5 cm^3. The cathode diameter was 40 cm, and the distance between the cathode and the holder was 4 cm. The sample was loaded into the substrate at an elevated temperature (300 ^oC). The reactive pressure and the flow rate of the CF_4 gas were 600 mtorr and 500 sccm, respectively. The RF power was 40W with CF_4 plasma exposure times of 1 min (termed HfOF). For the normal HfO_2 gate dielectrics samples (denoted as HfO_2), there was no CF_4 plasma treatment after the hafnium dioxide deposition. In a later phase of the investigation, a 50 nm TaN metal gate was also deposited by the RF sputter method. The source and drain regions in the active device region were implanted with boron (25 keV at 5×10^{15} cm^{-2}) and activated at 900 ℃ for 30 s annealing in a N_2 ambient. After the patterning of source/drain contact holes, an aluminum film of 300 nm thickness was

then deposited on the TaN gate for use as the gate electrode and source/drain contact pad. Then, the devices were completed by the contact pad definition. Finally, the 300 nm aluminum film was evaporated from the bottom of the electrode by a thermal evaporator.

The electrical properties were analyzed by an HP 4285 for capacitance-voltage (C-V) characteristics at 100 kHz, and the capacitance effective thickness (CET) was extracted from the capacitance under the accumulation region without considering the quantum effects. The current-voltage (I-V) curves were measured by a Keithly 4200. Devices with gate length (L) and width (W) of 10 and 100 μm were measured. The V_{TH} is defined as the gate voltage at which the drain current reaches 100 nA $\times$W/L and V_D = -0.1 V. The transfer characteristics I_D –V_G of HfO_2 nMOSFETs are measured at V_D = -0.1 and -1 V, and V_G = 0 to -2.5 V.



4-2.3 Results and Discussions

Figure 4.20 shows the C-V curves of the HfO_2 pMOSFETs with and without CF_4 plasma treatment. The excellent C-V characteristics can be observed for both as-deposited and CF_4 plasma treated samples. The CET extracted from these C-V curves are 2.01 nm for the as-deposited sample and 1.97 nm for the fluorinated one, respectively. The CET reduction of the CF_4 treated sample can be explained by F atoms incorporation into HfO_2 layer. The fluorine atoms can be bonded to Hf (or Si) dangling bonds resulting in annihilation of oxygen vacancies, as mentioned above. Figure 4.21 shows the current density versus gate voltage (J-V) characteristics of as-deposited and fluorinated HfO_2 gate dielectrics. The fluorinated sample shows a reduction of gate leakage current as indicated in this figure, indicating that the fluorine atoms can passivate oxygen vacancies resulted in less Frenkel-Poole

conduction current. In addition, the breakdown voltage of the fluorinated HfO_2 gate dielectrics was also improved.

Figure 4.22 shows the I_D-V_G transfer characteristics of the as-deposited and CF_4 plasma treated HfO_2 pMOSFETs, where the device channel length and width were 10 and 100 μm, as mentioned above. High-performance characteristics of HfO_2 pMOSFETs with excellent S. S. ~82 mV/dec, high mobility ~64 $cm^2/V \cdot s$, and high I_{ON}/I_{min} current ratio ~1.03×10^8 are observed without any treatment. For the CF_4 treated one, we can observe that the I_{min} is reduced significantly from 9.07 to 7.05 pA at V_D = -0.1 V, enhanced I_{ON}/I_{min} current ratio (~1.69×10^8), and improved S. S. (~80 mV/dec). Besides this, the GIDL current also decreased for the fluorinated device, as illustrated in Fig. 4.22, especially for the large drain biasing (V_D = -1 V). As mentioned above, in the significant V_D and positive V_G bias region, the drain-to-gate bias is sufficiently high to deplete and even invert the p^+ drain region under the gate. This causes enhanced electric field and band bending, resulting in a dramatic increase of high field effects, such as avalanche multiplication and band-to-band tunneling (BTBT). The possibility of tunneling via traps (trap-assisted tunneling) also increases. These high-field effects cause hole-electron pair generation. The holes tunnel to the drain and contribute to the GIDL current. The electrons are swept to the substrate and contribute to the substrate current. The higher electric field due to the higher density of interface traps increases the role of this current component in the high-k devices [4.23]. In addition, the drain induced barrier lowering (DIBL) was less than 20 mV for all samples as shown in Fig. 4.22. By the same token, the driving current of the fluorinated device was larger than that of conventional devices, as indicated in Fig. 4.23. The driving current of the CF_4 treated device with 10 *u*m gate length showed a 19 % increase over the as-deposited device at V_D = -2 V and V_G-V_{th} = -2.5 V, as shown in Fig. 4.23. The driving current increases with applied gate bias increasing. In

addition, the transconductance (g_m) extracted from linear region (V_D = -0.1 V) also increased for the fluorinated device (Fig. 4.24). Only a little 5 % increase can be observed for the fluorinated device with 10 *u*m gate length, by comparison with the as-deposited one. However, the mobility improvement for the fluorinated sample was more pronounced in the higher electric field. About 100 % increase can be observed while the V_G-V_{th} = -2 V. As mentioned above, this can be speculated to the improved surface roughness, since fluorine incorporation into HfO_2 film can effectively passivate HfO_2/Si interface. As a result, the surface roughness of HfO_2/Si interface can be effectively improved for the fluorinated sample. However, this result seems better than that of fluorinated HfO_2 nMOSFETs.

To understand the mechanism of NBTI characteristics in our high-k dielectrics, Fig. 4.25 shows the I_D-V_G transfer characteristics of the as-deposited and CF_4 plasma treated HfO_2 pMOSFETs under the same NBTI stress (V_G-V_{th} = -2 V) at room temperature. It is worth to note that the fluorinated device leads to an obvious reduction in ΔV_{TH} under NBTI stress. The ΔV_{TH} is only 22 mV for the CF_4 treated HfO_2 pMOSFET while the as-deposited one exhibits 142 mV ΔV_{TH} after 1000s NBTI stress at room temperature. This result demonstrates that the fluorinated device has better HfO_2/Si interface characterization than as-deposited one. As mentioned above, the fluorine atoms will accumulate in HfO_2/Si interface, resulting in HfO_2/Si interface passivation. Figure 4.26 demonstrated the ΔV_{TH} under NBTI stress at different temperatures (RT~70 ℃) and different biases (-2 and -2.5 V) for (a) HfO_2 dielectrics and (b) HfOF dielectrics, respectively. The NBTI stress induced HfO_2/Si interface degradation is quite obvious for the HfO_2 gate dielectrics while the HfOF gate dielectric exhibits an excellent NBTI reliability. As mentioned above, the fluorine atoms are located primarily at the two interfaces of the TaN/HfO_2 and HfO_2/Si-substrates after CF_4 plasma treatment. The fluorine atoms will react with

Si-O bonds, and then the released oxygen atoms oxidize the SiO_2/Si interface. We thus argue that the structural change of the gate-oxide films occurs due to the reaction between the fluorine atoms and the Si-O bonds, resulting in HfO_2/Si interface passivaiton. The threshold voltage degradation under NBTI stress for the HfOF gate dielectrics becomes obvious at high temperature (70 ℃). However, the change of ΔV_{TH} in NBTI stress at different temperature is quite different between HfO_2 and HfOF gate dielectrics, as indicated in Fig. 4.26. The power-law fitting is suitable for NBTI characteristics of both HfO_2 and HfOF gate dielectrics. The n value of power-law fitting indicates traps generation during NBTI stress. The n is about 0.196 for the as-deposited sample at different temperatures (30~70 ℃) and biases (-2 and -2.5 V). However, for the HfOF gate dielectric, n is smaller than that for HfO_2 gate dielectric, indicating that the HfOF gate dielectric has less traps generation during NBTI stress at different temperatures (30~70 ℃) and biases (-2 and -2.5 V). Besides, the n increase with increasing temperature, indicating that the HfOF gate dielectric has highly temperature dependence in NBTI reliability. Therefore, the increase in n of HfOF gate dielectric is attributed to the deep charge trapping, which has obvious temperature dependence at the quite high temperature (70 ℃). As mentioned previous, the fluorine atoms diffuse to the HfO_2/Si interface and bond with Si. Then, the HfOF gate dielectrics have the defect passivation in HfO_2/Si interface due to extra Si-F boding, resulting in shallow traps elimination for HfOF dielectrics.

On the other hand, it is worth to note that GIDL improvement during NBTI stress is obvious for the HfOF gate dielectrics, as shown in Fig. 4.25. Figure 4.27 demonstrated the GIDL current after 1000s NBTI stress at different temperatures and applied biases for the as-deposited and CF_4 treated samples. The GIDL current increases with measuring temperature increasing for all samples. However, the obvious GIDL improvement can be observed for the fluorinated device, especially at

high temperature. As mentioned above, enhanced electric field and band bending resulted in a dramatic increase of high field effects, such as band-to-band tunneling and trap-assisted tunneling. Then, it causes large hole-electron pair generation, and the electrons tunnel to the drain and contribute to the GIDL current. Furthermore, the trap-assisted tunneling will dominates the GIDL degradation of high-k device. Besides this, the conventional band-to-band tunneling (electron direct tunneling) can also be observed, as shown in Fig. 4.28(a). As a result, the NBTI stress induced GIDL degradation will become more obvious for the high-k device, especially for trap-assisted tunneling induced GIDL current. In this work, this serious GIDL degradation can be observed for the HfO_2 pMOSFET during NBTI stress. Generally speaking, NBTI stress degraded HfO_2/Si interface, resulting in increase of trap-assisted tunneling, as shown in Fig. 4.28(a). However, the accumulation of fluorine atoms the interfaces of the gate dielectrics, and some fluorine atoms accumulated in the bulk HfO_2 thin film, resulting in bulk HfO_2 thin film and interface passivation by CF_4 plasma treatment, as shown in Fig. 4.28(b). Then, the trap-assisted tunneling phenomenon can be much suppressed for the HfOF pMOSFET during NBTI stress, resulting in GIDL improvement.

4-2.4 Summary

For the first time, a novel high-performance and excellent-reliability HfOF pMOSFET was demonstrated. Large I_{ON}/I_{min} current ratio (~1.69×10^8), good S. S. (~80 mV/dec), small DIBL (<20 mV), and high mobility (~67 $cm^2/V \cdot s$) can be observed for the HfOF pMOSFETs. The HfOF pMOSFET has better HfO_2/Si interface, including GIDL current and better NBTI reliability. Reduced GIDL current was observed for the HfOF pMOSFET due to HfO_2/Si interface passivation by

fluorine, resulting in less hole-electron pair generation. The fluorine incorporation into HfO_2 gate dielectrics effectively passivated interface defect vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps. These results provide a valuable guideline for future 32 nm and beyond CMOS device designs with high-k dielectrics with CF_4 plasma treatment.

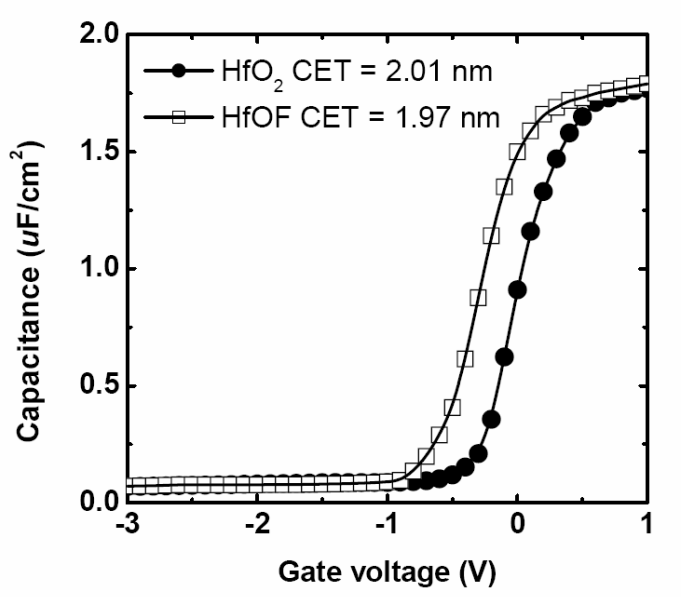


Fig. 4.20 C-V curves of the HfO_2 pMOSFETs with and without CF_4 plasma treatment.

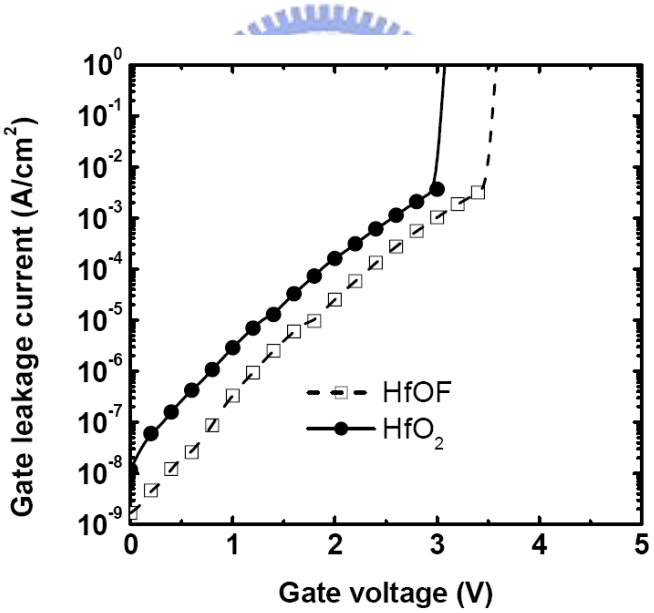
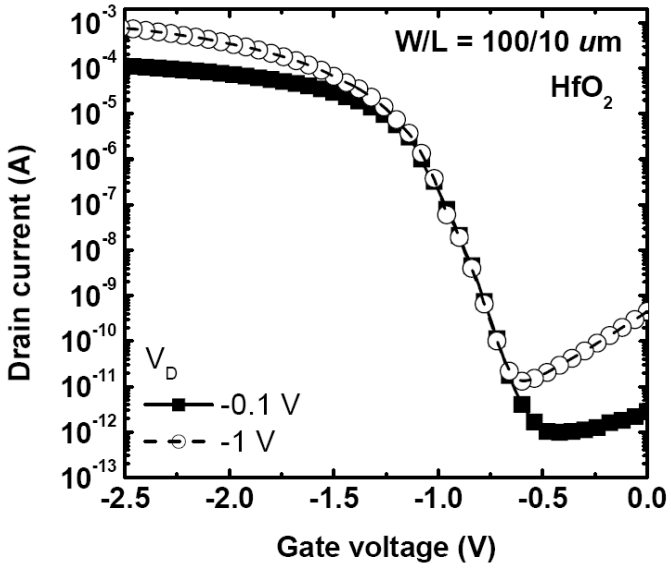
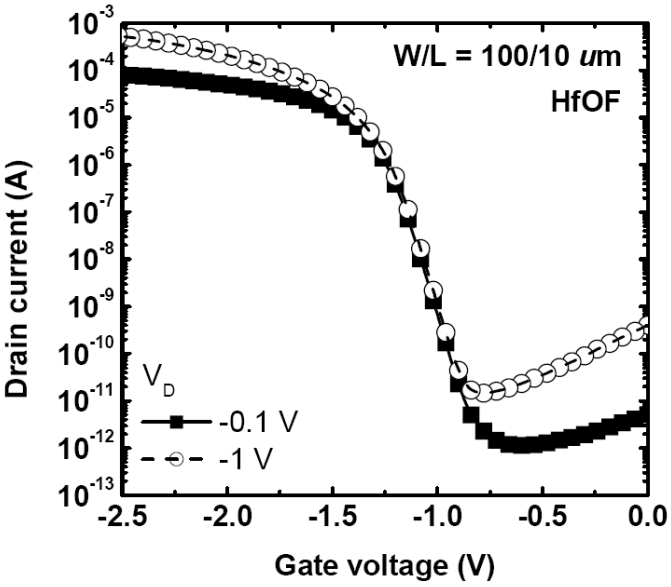


Fig. 4.21 J-V characteristics of the HfO_2 pMOSFETs with and without CF_4 plasma treatment.



(a)



(b)

Fig. 4.22 I_D-V_G transfer characteristics of (a) as-deposited and (b) CF_4 plasma treated HfO_2 pMOSFETs, where the device channel length and width were 10 and 100 μm.

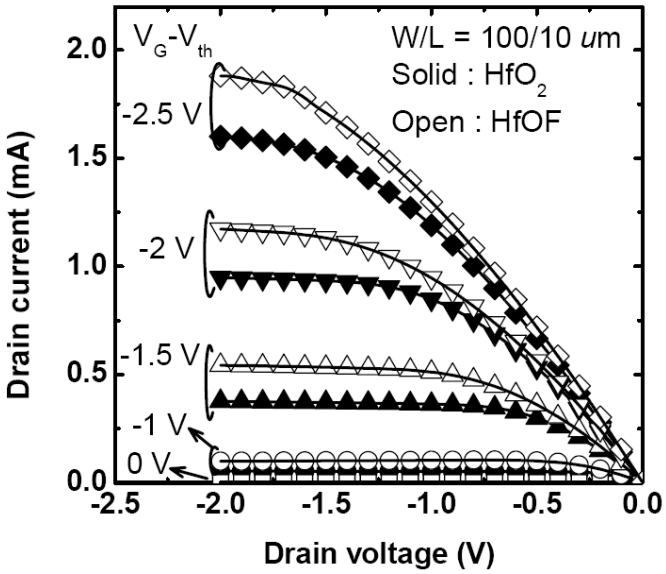


Fig. 4.23 I_D-V_D characteristics of as-deposited and CF_4 plasma treated HfO_2 pMOSFETs, where the device channel length and width were 10 and 100 μm.

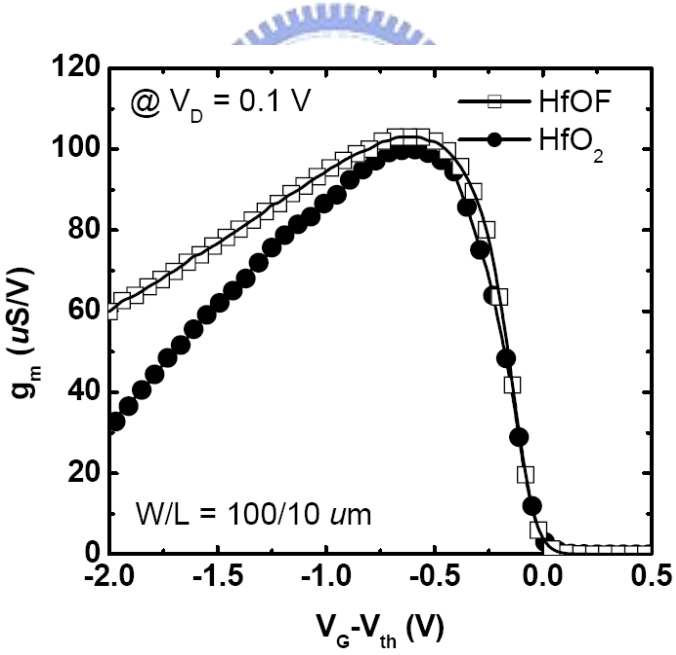
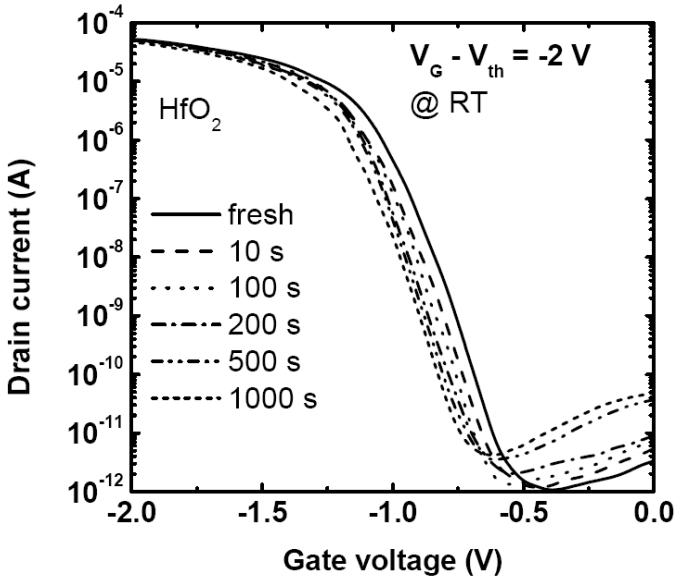
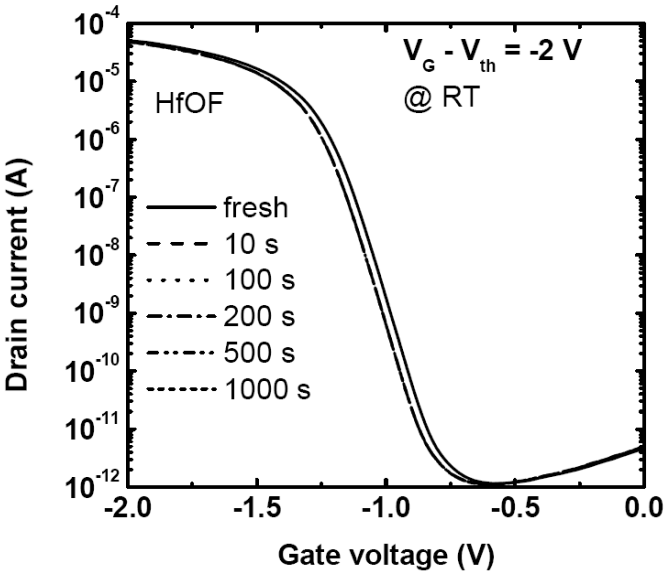


Fig. 4.24 transconductance (g_m) extracted from linear region (V_D = 0.1 V) for the as-deposited and fluorinated HfO_2 pMOSFETs.

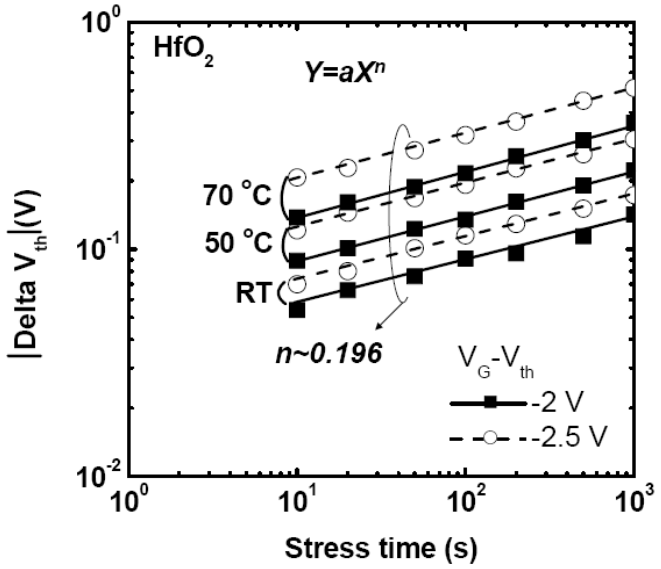


(a)

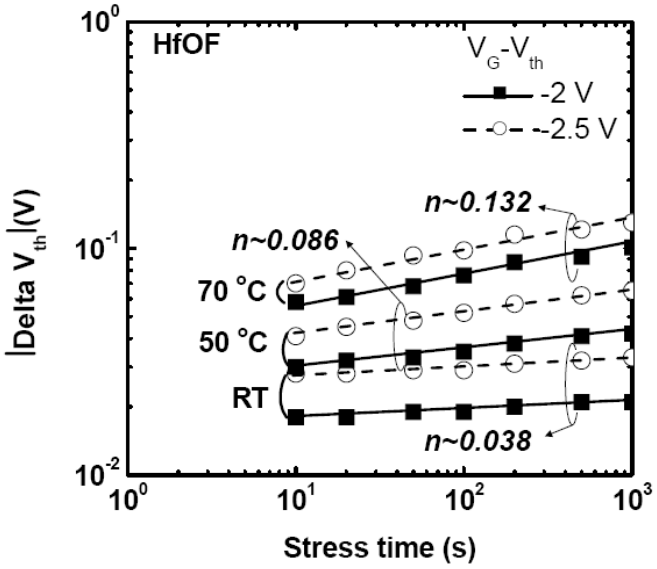


(b)

Fig. 4.25 I_D-V_G transfer characteristics of (a) as-deposited and (b) CF_4 plasma treated HfO_2 pMOSFETs under the same NBTI stress (V_G-V_{th} = -2 V) at room temperature.



(a)



(b)

Fig. 4.26 ΔV_{TH} under PBTI stress at different temperatures (RT~100 ℃) for (a) HfO_2 dielectrics and (b) HfOF dielectrics, respectively.

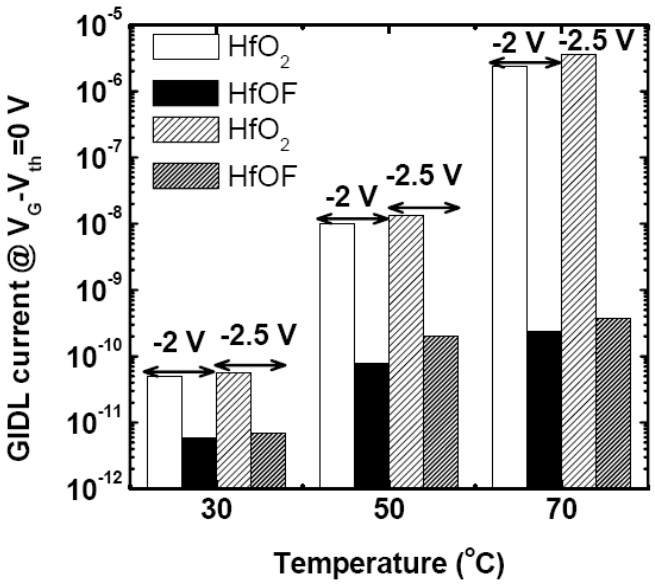


Fig. 4.27 The GIDL current after 1000s PBTI stress at different temperatures for as-deposited and CF_4 treated samples.

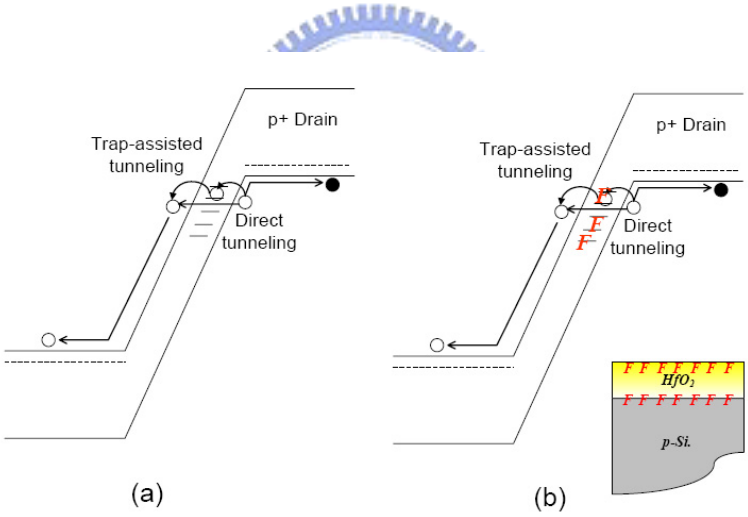


Fig. 4.28 Band diagram of suggested GIDL mechanism: (a) GIDL current includes trap-assisted tunneling and conventional band-to-band tunneling (electron direct tunneling) currents, and (b) fluorine accumulates in HfO_2/Si interface and bulk film, giving interface passivation to reduce trap-assisted tunneling.

Chapter 5

Characteristics of Contact Etch Stop Layer (CESL) Induced Local Strained HfO_2 nMOSFETs

5-1 Performance and Reliability Characteristics for Contact Etch Stop Layer (CESL) Induced Local Strained HfO_2 nMOSFETs Using Pulse-IV Analysis

5-1.1 Introduction

As scaling of CMOS technology reaches its physical limitations, HfO_2 gate dielectric has received considerable attention due to advantages such as sufficiently high dielectric constant (15-25), good thermal stability, wide bandgap (5.6 eV), and large band offsets (~1.5eV) [5.1]-[5.2]. However, threshold voltage instability, low carrier mobility, and dielectric reliability remain critical problems for high-k gate dielectrics. In addition, electron trapping and detrapping in high-k gate dielectrics has been found to be the major source of instability in the devices [5.3]-[5.4]. Therefore, a significantly faster measurement technique than previous studies is needed in order to investigate the intrinsic characteristics of high-k gate dielectrics with minimal charge trapping effect. The pulse method, with very short pulse durations to minimize the effect of fast electron trapping, has been adapted to demonstrate the "close-to-intrinsic" characteristics of high-k devices [5.5]-[5.6].

The improvement of carrier mobility has also been intensely studied by introducing strain in the channel region. One of the most popular technologies is using high tensile-stress contact etch stop layer (CESL), which can obviously improve electron mobility and I_{ON} for nMOSFETs [5.7]-[5.9]. Nevertheless, a CESL strained high-k MOSFET for high mobility application has yet to be proposed. In this work,

for the first time, a high-performance CESL strained nMOSFET with HfO_2 gate dielectrics is successfully demonstrated. The g_m and I_{ON} exhibit 70% and 90% increases for CESL-devices, respectively. In addition, "close-to-intrinsic" improvements for the CESL HfO_2 nMOSFETs were also observed under Pulsed-IV operation.

5-1.2 Experiments

nMOSFETs were fabricated on 6-inch p-type Si wafers with a resistivity of 15–25 Ωcm. A 0.35-μm process was used with local-oxidation-of-silicon (LOCOS) isolation. After a standard HF-last cleaning step, 8-nm HfO_2 gate oxide was deposited. Then, α-Si (deposition at 550℃) with the thickness of 50 nm was deposited in order to create the tensile local strain channel [5.9]. Then, *in situ* n^+-doped poly-Si with 150 nm was deposited in the same ambient. After S/D formation, a low pressure chemical vapor deposition (LPCVD) silicon nitride (CESL) was directly deposited on the transistor at 780°C at different thicknesses (50, 100 and 300 nm), followed by a 200 nm low temperature plasma enhanced (PE) oxide deposition. After contact alignment, the PE-oxide and SiN layer on the S/D regions were etched in the same system. In order to prevent etching damage to the Si surface at S/D, the SiN layer was etched in two steps. The SiN was first dry etched, leaving 10 nm to be finished by wet etching. A hot H_3PO_4 solution was used to etch the residual 10 nm SiN layer. After these processes, a four-level metallization (Ti–TiN–Al–TiN) was carried out in the PVD system for the contact.

In future advanced IC technologies, both strain technique and silicidation processes are necessary for device performance enhancement. To maintain silicide integrity and retain the advantage of the strain at the same time, a low temperature

nitridation process such as plasma-enhanced CVD (PECVD) can be used to match up the thermal budget of silicide. By adjusting the nitride deposition conditions (SiH_4/N_2/He gas flow rate, pressure, HF power, electrode gap), it also can induce tensile strain in channel region [5.10]-[5.11].

These CESL strained HfO_2 nMOSFETs were analyzed using an HP 4285 for C-V characteristics at 100 kHz, and the capacitance effect thickness (CET) was extracted from the capacitance in the accumulation region. The CET of the HfO_2 thin films were about 1.6 nm for all samples. The current-voltage (I-V) curves were measured using a Keithly 4200. Furthermore, the "close-to-intrinsic" characteristics of HfO_2 gate dielectrics can be characterized by using a pulsed-IV (PIV) system, as there was only negligible charge trapping, as mentioned earlier.

5-1.3 Results and Discussions

Figure 5.1 shows the I_D-V_G and I_D-V_D transfer characteristics of the conventional and CESL strained HfO_2 nMOSFETs, where the device channel length and width were 0.35 and 10 μm, respectively. The drain induced barrier lowering (DIBL) was less than 40 mV for all samples as shown in Fig. 5.1(a). However, there was a threshold voltage (V_{th}) shift for the CESL-devices. This was due to the V_{th} roll-off behavior resulted from the bandgap narrowing effect caused by the channel strain [5.12]. Moreover, the CESL-devices experienced additional thermal processing (due to the SiN deposition in the LPCVD system), implying more diffusion of dopants which resulted in the V_{th} decrease [5.9]. Besides, the thermal processing between each CESL device doesn't show an obvious difference. As a result, the V_{th} shift is not obvious for CESL-devices. By the same token, the driving current of the CESL-devices was larger than that of conventional devices, and increased with

increasing capping nitride thickness, as indicated in Fig. 5.1(a). The driving current of the 300 nm SiN-capped device with 0.35 *u*m gate length showed a 90 % increase over the as-deposited device at V_D = 2 V and V_G-V_{th} = 2 V, as shown in Fig. 5.1(b). In addition, the transconductance (g_m) extracted from linear region (V_D = 0.1 V) also increased with increasing capping nitride thickness (Fig. 5.2). A roughly 70 % increase can be observed for the 300 nm SiN-capped device with 0.35 *u*m gate length, by comparison with the as-deposited one. The enhancement of g_m, compared to the as-deposited sample, was increased, with channel length decreasing as shown in the inset in Fig. 5.2. These results imply that the increase of electron mobility for CESL-nMOSFET is the cause of the observed enhancement of the driving current and g_m. In addition, the short channel effect can be ignored in this work. The DIBL is smaller than 40 mV and V_{th} is almost the same for all samples under different gate length. As a result, we can say that the performance improvement almost totally came from CESL induced local strain channel.

The dependence of the interface states density at different thicknesses of the capping nitride layer is measured by the trapezoidal waveform [5.13]-[5.14] (Fig. 5.3). The Q_{CP} was extracted from charge pumping current measurement as indicated in the inset in Fig. 5.3. The as-deposited sample depicts the largest charge pumping current (I_{CP}) among all samples. Further, the I_{CP} was dramatically decreased with the CESL SiN capping layer for HfO_2 nMOSFETs as indicated in the inset in Fig. 5.3. The Nit extracted from I_{CP} is only 9.85×10^{10} cm^{-2} for the 300 nm SiN-capped device, while the as-deposited one is 6.56×10^{11} cm^{-2}. This is ascribed to the use of H-containing precursors (SiH_3Cl and NH_3) during the SiN deposition step. The incorporated hydrogen species tends to passivate the interface states. In addition, the interfacial layer between HfO_2 and Si-substrate formed during the HfO_2 thin film deposition, resulting in a worse HfO_2/Si interface. Then, the hydrogen passivation will become

more obvious for the HfO_2 NMOSFET. However, the extra Si-H bonds would also be responsible for the worse hot carrier degradation as shown in Fig. 5.4. The V_{th} shift increase with increasing capping nitride thickness. However, the G_M (Fig. 5.4), I_{ON} degradations (Fig. 5.5) and I_{CP} (before and after HC stress) (Fig. 5.6) show almost the same trend for all samples, indicating that the HC-stress only do a little damage on interface near the drain side of as-deposited and CESL devices. The other portion of HfO_2/Si interface quality would not be easily degraded during HC-stress. Fig. 5.7 exhibits a physical model for CESL-devices under HC-stress. Some electrons in the channel entering the drain space-charge region experience impact ionization. The above discussion implies that the strained-device can enhance the effective mobility. The more enhancement in channel mobility is, the larger is the device reliability degradation. As a result, the large impact ionization rate can be observed in CESL-devices. Furthermore, the slope of a Q_{CP} versus log (freq.) plot gives the average D_{it}. It shows that the average D_{it} was almost the same for all CESL-devices. However, the slope of the as-deposited sample was quite different from that of SiN-capped one, indicating that the as-deposited sample exhibited larger average D_{it}.

Figure 5.8 shows PBTI characteristics of all devices. Both V_{TH} shift and I_{ON} degradation were much improved for the CESL-devices, as shown in Fig. 5.8 and Fig. 5.9. This can be speculated to the incorporation of N-containing precursors (NH_3) during the SiN deposition step, and the nitrogen species tend to eliminate some defect states of HfO_2 thin film, resulting in less charge trapping during PBTI stress. Besides, there is almost no G_M degradation (Fig. 5.9). It means that PBTI only affects on bulk HfO_2 thin film, instead of HfO_2/Si interface. The PBTI characteristics under different temperatures were shown in Fig. 5.10 and Fig. 5.11. V_{TH} shifts increase a lot at high temperature for CESL-devices, suggesting that the SiN-capped ones would have deep electron trap during PBTI stress as indicated in Fig. 5.12. These results also indicated

that the nitrogen incorporation effectively passivated the dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps.

The "close-to-intrinsic" characteristics of HfO_2 gate dielectrics were analyzed using PIV measurement as shown in Figs. 5.13 and 5.14. The driving current of the 300 nm SiN-capped device measured by the PIV system was larger than that of the conventional measurement (DC) as shown in Fig. 5.13(a). Further, the driving current under PIV operation was also enhanced with increasing capping nitride thickness, as indicated in Fig. 5.13(b). A 60% I_{ON} increase can be observed for the 300 nm SiN-capped device. Figure 5.14 presents the g_m measured by PIV system at different capping SiN-layer thicknesses. Increased g_m with increasing capping SiN-layer thickness is depicted in this figure, and nMOSFETs with CESL 300-nm show a significant g_m increase (50%), by comparison with the as-deposited sample. Therefore, the "close-to-intrinsic" improvement of the characteristics of the CESL-nMOSFETs with HfO_2 gate dielectrics can be obtained under PIV measurement, which can be used for future high-k gate dielectrics device applications.

5-1.4 Summary

For the first time, a novel high-performance CESL strained nMOSFET with HfO_2 gate dielectrics was demonstrated. Both the g_m and driving current were greatly enhanced for the CESL strained HfO_2 nMOSFETs. The CESL-device has better HfO_2/Si interface and dielectric quality, including less charge pumping current (90% reduction) and less PBTI effect (55% reduction). Reduced charge pumping current was also observed for the CESL-devices, indicating that a superior HfO_2/Si interface resulting from hydrogen passivation. The nitrogen incorporation into HfO_2 gate

dielectrics effectively passivated the dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps. On the other hands, “close-to-intrinsic” characteristics and excellent performance were demonstrated for CESL strained HfO_2 nMOSFETs under Pulsed-IV operations. A roughly 50% g_m and 60% I_{ON} increase can be achieved for the CESL HfO_2 nMOSFETs using PIV measurement. These results provide a valuable guideline for future 45 nm and beyond CMOS device designs with high-k and strain engineering.

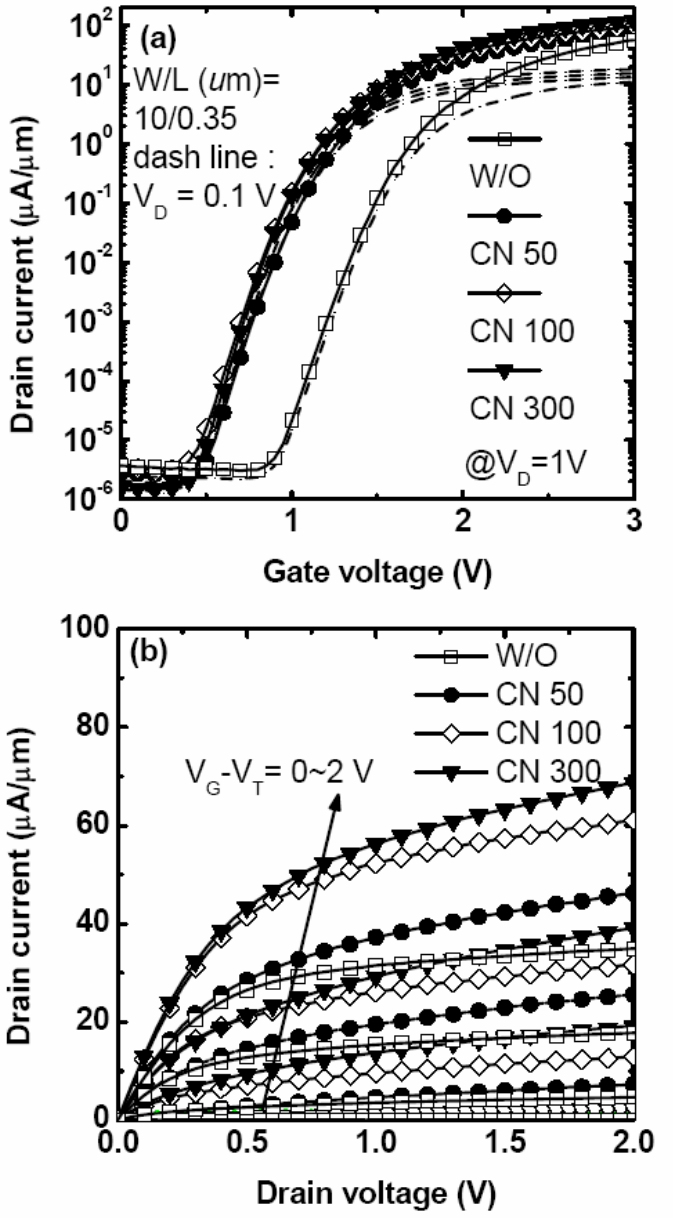


Fig. 5.1. (a) I_D-V_G and (b) I_D-V_D characteristics of HfO_2 nMOSFETs without and with different capping nitride thicknesses.

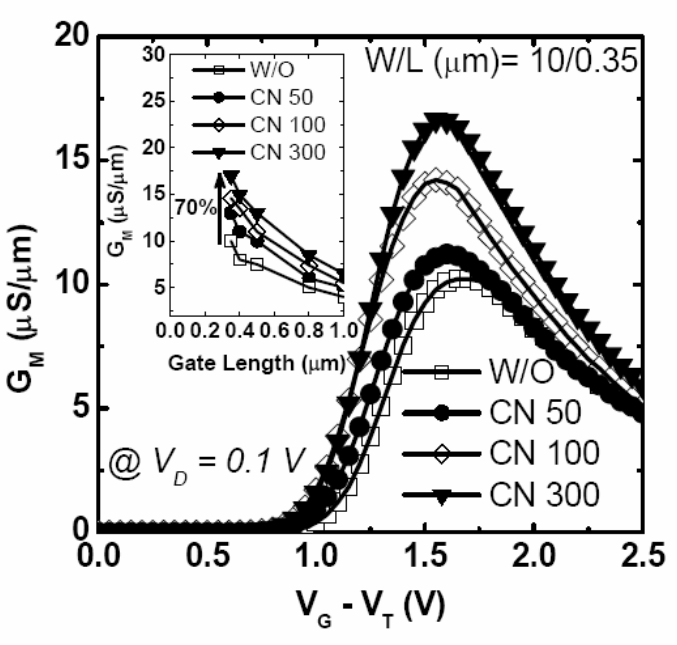


Fig. 5.2. The transconductance (g_m) increases for conventional and CESL strained HfO_2 nMOSFETs. Inset shows G_M increase with gate length decreasing for HfO_2 nMOSFETs.

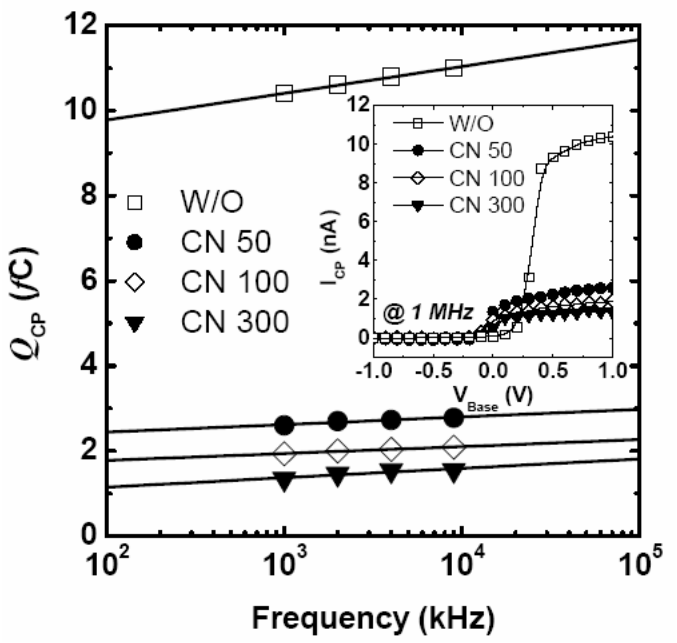


Fig. 5.3. Q_{CP} for all samples under different frequencies measuring extracted from inset figure (Charge pumping characteristics of HfO_2 nMOSFETs without and with different capping nitride thicknesses).

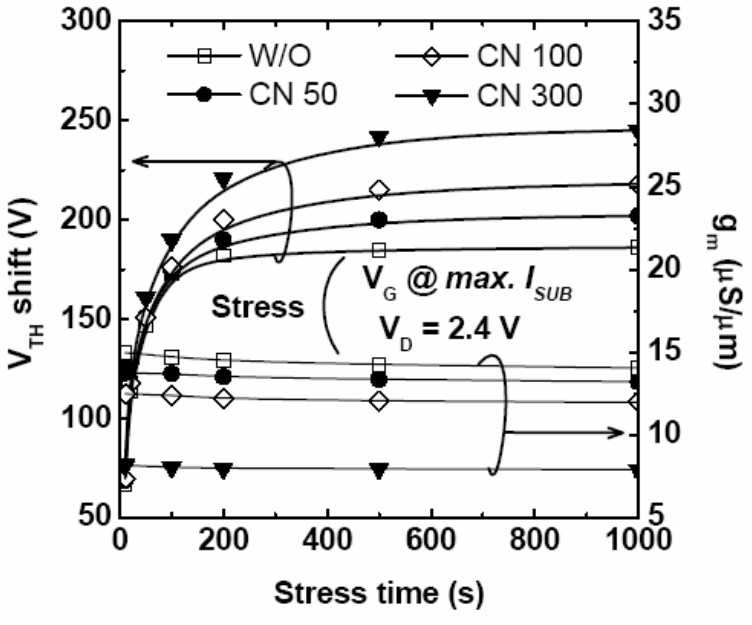


Fig. 5.4. Characteristics of V_{TH} shift and G_M during 1000s hot carrier (HC) stress for all samples.

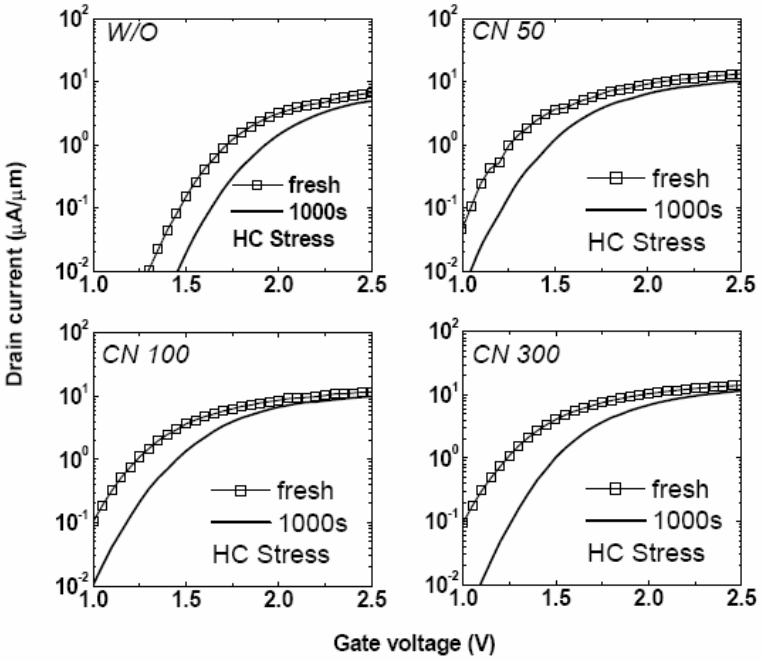


Fig. 5.5. Driving current degradation after 1000s HC stress for all samples. The I_{ON} degradation is almost the same for all samples.

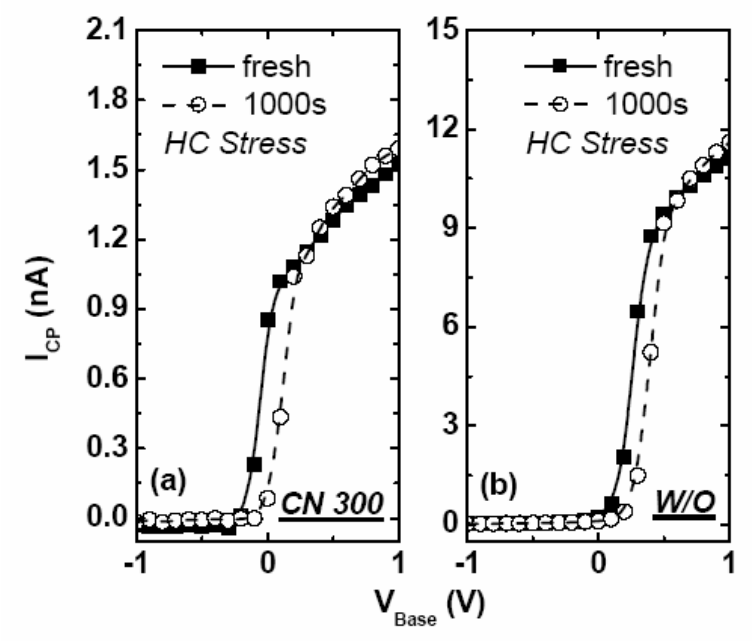


Fig. 5.6. Charge pumping current before and after 1000s HC stress for (a) W/O, and (b) 300 nm CESL devices, respectively. The same I_{CP} increase can be observed for as-deposited and CESL devices.

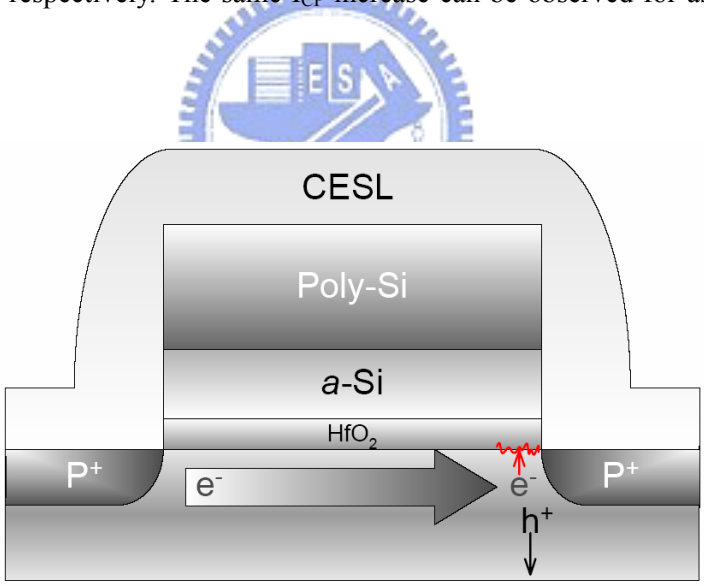


Fig. 5.7. Physical model for CESL-HfO_2 nMOSFET under HC stress. HC-stress only did a little damage on interface near the drain side of CESL-devices.

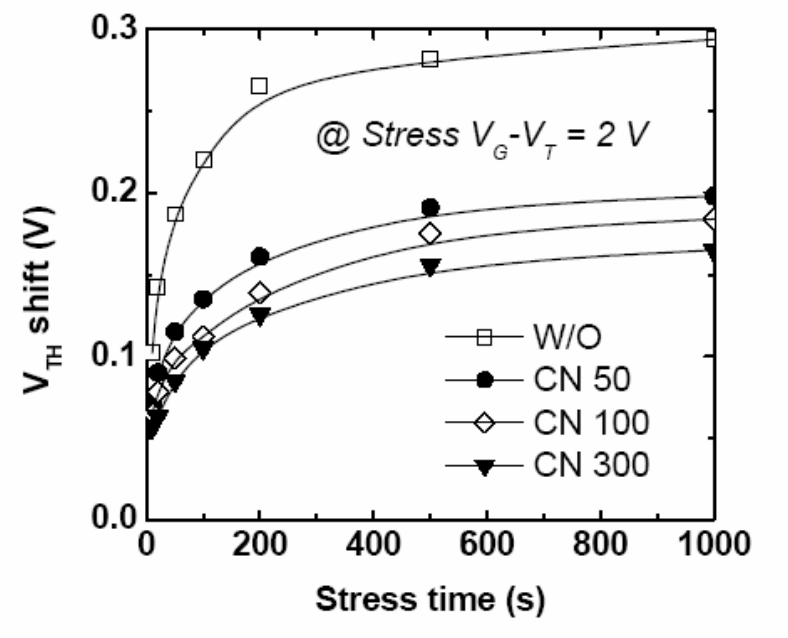


Fig. 5.8. Improved PBTI characteristics can be observed for all CESL-devices. V_{TH} shift decreases with capping nitride increasing.

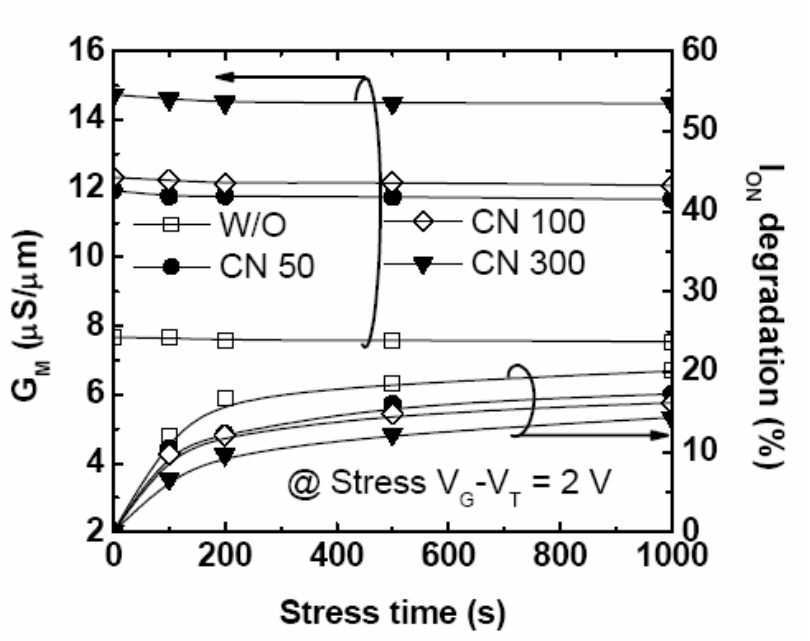


Fig. 5.9. g_m and I_{ON} degradation dring 1000s PBTI stress for all samples. Both g_m and I_{ON} degradation can be improved for CESL devices.

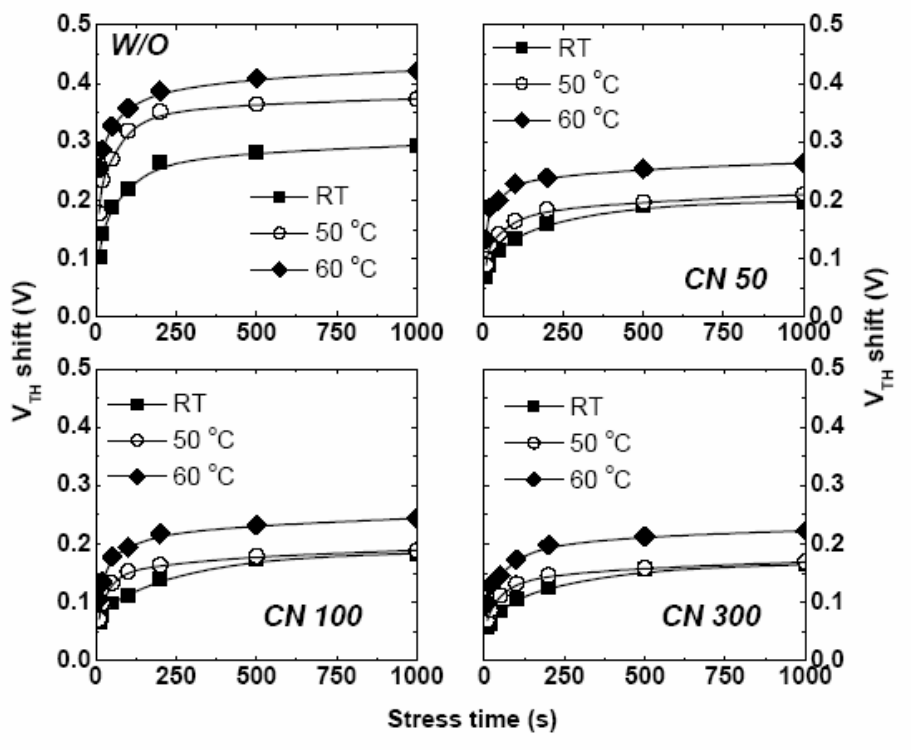


Fig. 5.10. PBTI characteristics (@$V_G - V_{TH} = 2V$) under different temperatures for all samples. The CESL-devices show obvious temperature dependence.

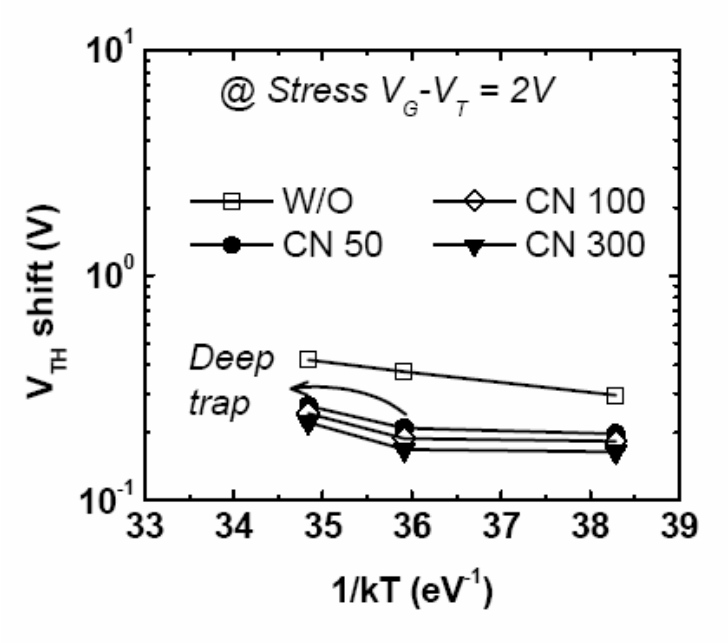


Fig. 5.11. V_{TH} shift increase for CESL-devices after 1000s PBTI stress under high temperature, indicating deeper oxide trap for CESL-devices.

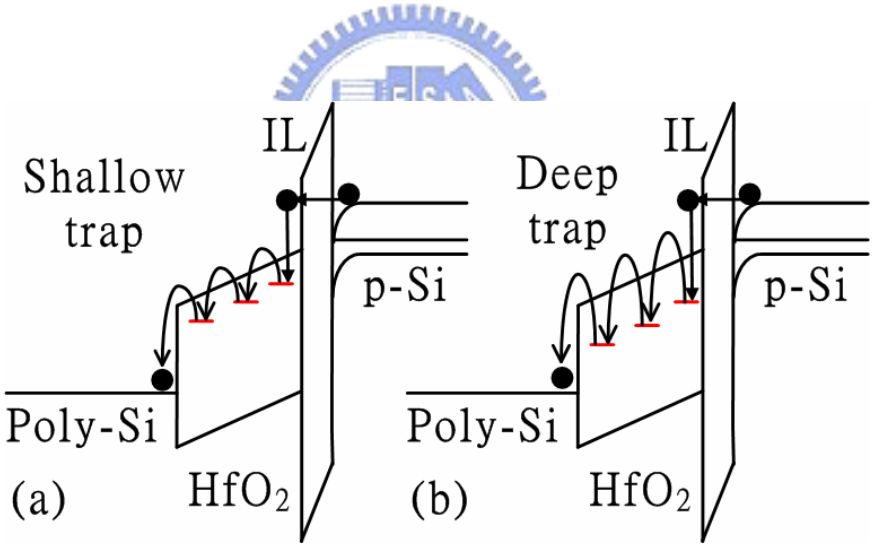


Fig. 5.12. The physical charge trapping model for (a) as-deposited, and (b) CESL-HfO_2 nMOSFET. The CESL devices have deep electron trap.

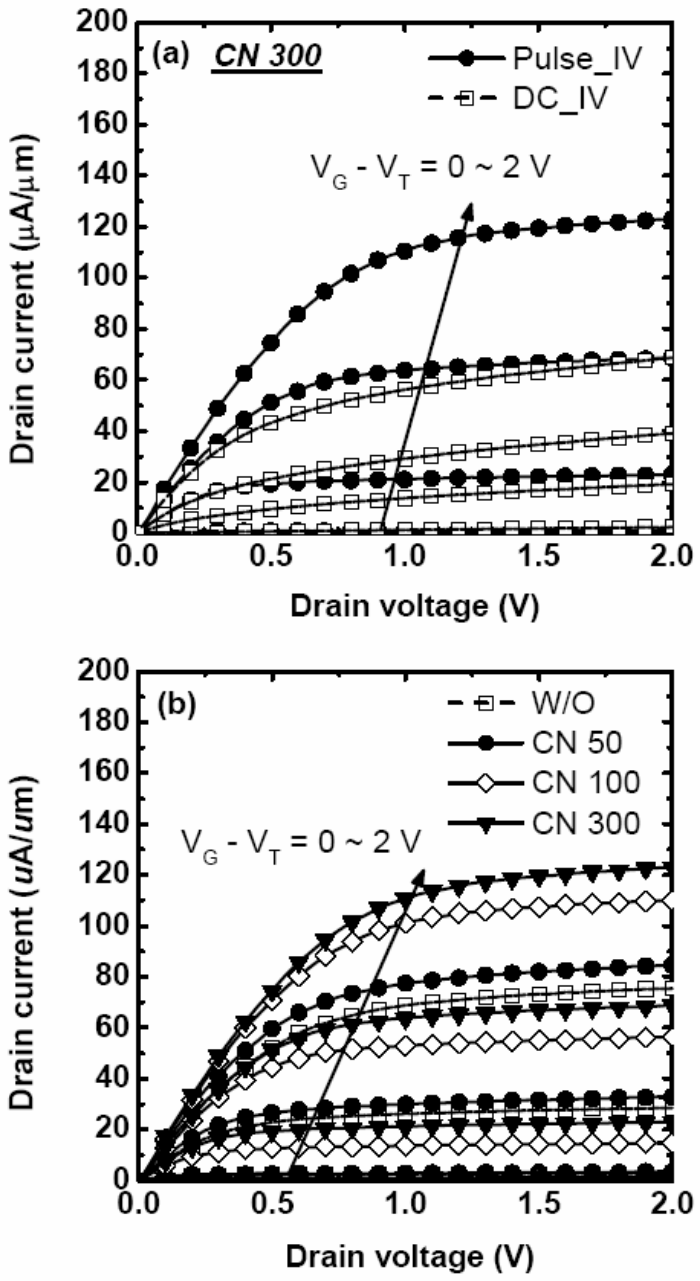


Fig. 5.13. The I_D-V_D characteristics of (a) 300 nm SiN-capped device under conventional and pulsed-IV measurement, and (b) all devices under pulsed-IV operation.

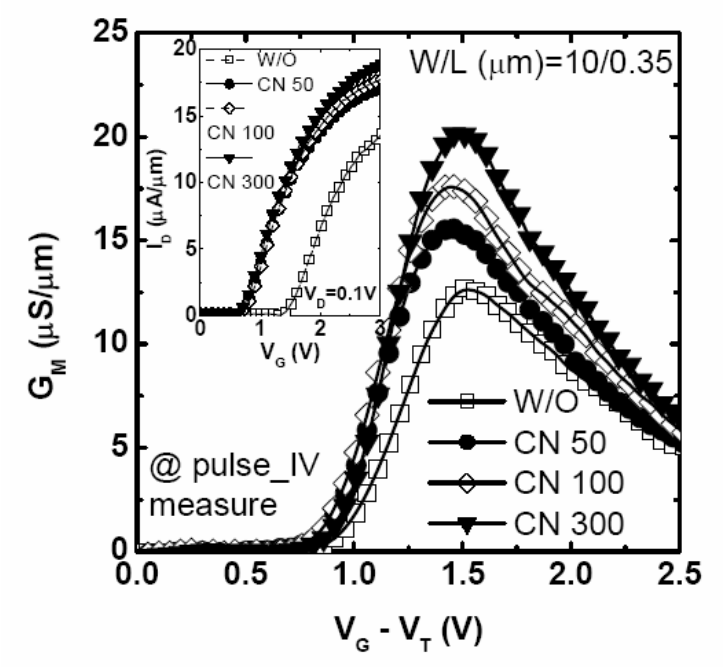


Fig. 5.14. The g_m increases with increasing capping nitride thickness for HfO_2 nMOSFETs under pulsed-IV measurement. Inset shows I_D-V_G characteristics for all samples under pulsed-IV measurement.

5-2 A Novel Dynamic Threshold HfO_2 nMOSFETs (DTMOS) with Local Tensile Strained Channel

5-2.1 Introduction

As scaling of CMOS technology reaches its physical limitations, HfO_2 gate dielectrics are considered to be the most promising high-k dielectrics to meet the future ULSI application [5.15], due to its high dielectric constant and excellent thermal stability [5.16]-[5.18]. Besides, as MOS devices continue to be scaled down, the low supply voltage is desirable to minimize the power consumption. Dynamic threshold voltage metal–oxide–semiconductor field effect transistor (DT-MOSFET) has been extensively studied [5.19]-[5.21], being attractive for lower power supply voltage applications. By shorting the gate to the body, the threshold voltage operating under DT mode is reduced due to the forward biasing of the body. As a result, the driving current can be drastically improved under the on-state for the DT-MOSFET [5.22]. The subthreshold swing could be attained to the ideal value (~60 mV/dec) [5.23]-[5.24]. Since the device exhibits the same normal-mode V_{TH} under the off-state resulted from zero gate and substrate biases, low standby power consumption is maintained. Subthreshold slope and short channel effects are also much improved due to the dynamics substrate bias [5.25].

On the other hand, the improvement of carrier mobility has also been intensely studied by introducing strain in the channel region. One of the most popular technologies is using high tensile-stress contact etch stop layer (CESL), which can obviously improve electron mobility and I_{ON} for nMOSFETs [5.26]-[5.27]. However, the combination of CESL technology, high-k dielectrics and DT operation in CMOS technology has never been investigated. In addition, the CESL HfO_2 nMOSFET

operating under DT-mode for different capping nitride thickness, is, to the best of our knowledge, still lacking in the literature. In this study, we present enhanced performance and improved hot carrier degradations on CESL HfO_2 nMOSFET operating under both conventional and DT modes. The performance of CESL HfO_2 nMOSFETs will have larger G_M (135% increase) and "close-to-ideal" subthresold swing (~62) under DT operation mode with tolerant hot carrier-stress characterization.

5-2.2 Experiment

nMOSFETs were fabricated on 6-inch p-type Si wafers with a resistivity of 15–25 Ωcm. A 0.35-μm process was used with local-oxidation-of-silicon (LOCOS) isolation. After a standard HF-last cleaning step, the HfO_2 thin film with 1.6 nm (CET) was deposited on Si wafer. Then, α-Si with the thickness of 50 nm was deposited in order to create the tensile local strain channel [5.9]. Then, *in situ* n^+-doped poly-Si with 150 nm was deposited in the same ambient. After S/D formation, contact etching stop layer (CESL) silicon nitride was directly deposited on the transistor at different thicknesses (50, 100 and 300 nm), followed by a 200 nm plasma enhanced (PE) oxide deposition. Finally, a four-level metallization (Ti–TiN–Al–TiN) was carried out in the PVD system for the contact.

These CESL strained HfO_2 nMOSFETs were analyzed using an HP 4285 for C-V characteristics at 100 kHz, and the CET was extracted from the capacitance in the accumulation region without considering quantum effect. The current-voltage (I-V) curves under DT and normal modes were measured using a Keithly 4200. For DT mode, the gate is tied to the body while the body is ground for the normal mode.

5-2.3 Results and Discussion

Figure 5.15 shows the I_D-V_G transfer characteristics of the conventional and CESL strained HfO_2 nMOSFETs, where the device channel length and width were 0.35 and 10 μm, respectively. For DT operation mode, the gate is tied to the body and varied from 0 V to 0.7 V by 0.05 V steps. The drain current of the DT mode was larger than that of normal mode for all CESL-devices, and increased with increasing capping nitride thickness, as indicated in Fig. 5.15. The drain current of DT mode showed 4 times increase over the normal mode for the 300nm nitride capped device at V_D = 0.7 V and V_G = 0.7 V, as shown in Fig. 5.15. This large increase can be attributed to the body bias effect. For the DT mode, the device is in on-state. On the contrary, the device with normal operation is operated in depletion region. In addition, the drain induced barrier lowering (DIBL) was less than 20 mV for all samples. By the same token, current driving capability of CESL-DTMOS and standard CESL-MOS are compared. The drive current (measured under V_D=V_G=0.7 V) for all CESL-device is 1 time larger when operating under DTMOS mode than under normal operation (measured under V_D=V_G=1 V)), again because of the larger body effect factor. So because of a smaller threshold voltage (under normal operation mode) and a larger dynamic threshold efficiency, the drain current as high as 30 uA/um at V_D=V_G =0.7 V is achieved for the CESL-DTMOS as shown in Fig. 5.16.

Figure 5.17 demonstrated the transconductance (g_m) of CESL-devices with different channel length, operated under DT and normal modes. The g_m increased with increasing capping nitride thickness for all CESL-devices due to the local tensile strain channel, as mentioned above. In addition, the g_m of all samples for DT mode is larger than that for the normal mode. The enhancement of g_m, compared to the normal operation mode, was increased, with channel length decreasing as shown in Fig. 5.17. A roughly 135 % increase can be observed for the 0.35μm CESL-device with 300nm

capping nitride under DT mode, by comparison with the normal mode. The increase of g_m was about 100 % for the 1μm CESL-device with a 300nm capping nitride layer. These results imply that the increase of electron mobility can be observed for the CESL-DTMOS with HfO_2 gate dielectrics. Furthermore, the subthreshold swing (*S.S.*) can be strongly improved for the DT operation mode as shown in Fig. 5.18. The *S.S.* would be increase about 40% for all samples. In order to realize the mechanism for this *S.S.* improvement, we can see the equations of drain current and *S.S.* [5.28]:

$$I_D = \mu_n \frac{W}{L}(\frac{kT}{q})^2 C_D \phi_S e^{q(V_G - V_{TH})/nkT}(\frac{n}{m})[1 - e^{-(qmV_{DS})/nkT}] \quad (1)$$

$$S.S. = \left[\frac{\partial \log I_D}{\partial V_G}\right]^{-1} = kT \times \ln 10 \times n \quad (2)$$

$$C_D(\phi_S) = (\gamma \frac{C_{OX}}{2}) / \sqrt{\phi_S - \frac{kT}{q}} \quad (3)$$

$$n = 1 + \frac{C_D + C_{it}}{C_{OX}} \quad \text{and} \quad m = 1 + \frac{C_D}{C_{OX}} \quad (4)$$

Where C_D is the depletion layer capacitance, $C_{it} = qD_{it}$, where D_{it} is the interface-trap density, and Φ_S is the surface potential in the subthreshold region. From eq. (1), we can see that the drain current in the subthreshold region is exponentially dependent on V_G, while V_{TH} is constant under normal mode. Therefore, the drain current would increase more significantly with gate voltage as compared to that under normal mode. This is because the threshold voltage in eq. (1) decreases with increasing V_G. As a result, the *S.S.* would be decreased a lot under DT mode.

Figure 5.19 shows V_{TH} degradations for CESL HfO_2 nMOSFET under DT mode. Devices were stressed at V_D=V_G=V_B=0.7 V. The threshold voltage is deduced from the maximum transconductance (g_m max) method at V_D= 0.1 V. It can be seen that the CESL-device with 300nm capping nitride depicts the largest V_{TH} shift at room temperature among all samples. Electron trapping appears to be the dominant

degradation mechanism during the hot carrier stressing for all samples. This is because the vertical electrical field favors the injection of electrons created by impact ionization near the drain region, where some of the injected electrons are captured by the traps in the dielectric layer. However, the threshold voltage shift under DT mode is quite small (within 100 mV after 10^4 s for 300nm nitride capped sample) due to the DT-mode operation. The applied voltage is $V_D=V_G=V_B=0.7$ V for DT operation, therefore, the reliability of DTMOS cannot be easily degraded by such small applied bias. The same excellent reliability can also be observed for the on current degradation, in Fig. 5.20. The 300nm nitride capped sample shows the worst I_{ON} degradation. However, for the worst case, the I_{ON} degradation is only 30% after 10^4 s HC-stress. On the other hand, the interface characterization of CESL-devices is almost not degraded by HC-stress under DT mode, indicating that the electron trapping is the dominant degradation mechanism, as mentioned above. The I_D-V_G curves only show I_{ON} degradation without S.S. variation before and after HC-stress, as illustrated in Fig. 5.20(b). The g_m is almost the same for all samples after 10^4 s HC-stress as indicated in Fig. 5.21, indicating that only electron trapping can be observed during HC-stress. To sum up, the CESL-DTMOS exhibits enhanced performance with tolerant reliability degradation.

5-2.4 Summary

The performance can be much enhanced for the CESL-DTMOS with high-k gate dielectric. 135 % g_m increase can be observed for the 0.35μm CESL-device with 300nm capping nitride under DT mode, by comparison with the normal mode. Besides, the subthreshold swing can be improved about 40% for the CESL-DTMOS. The “close-to-ideal” subthreshold swing can be achieved for the CESL-devices under

DT mode. Nevertheless, the tolerant reliability degradation can be observed for the CESL-DTMOS after hot carrier stress. This result suggests that the CESL-DTMOS with high-k gate dielectric is a very suitable application for future high performance and low power consumption technology.

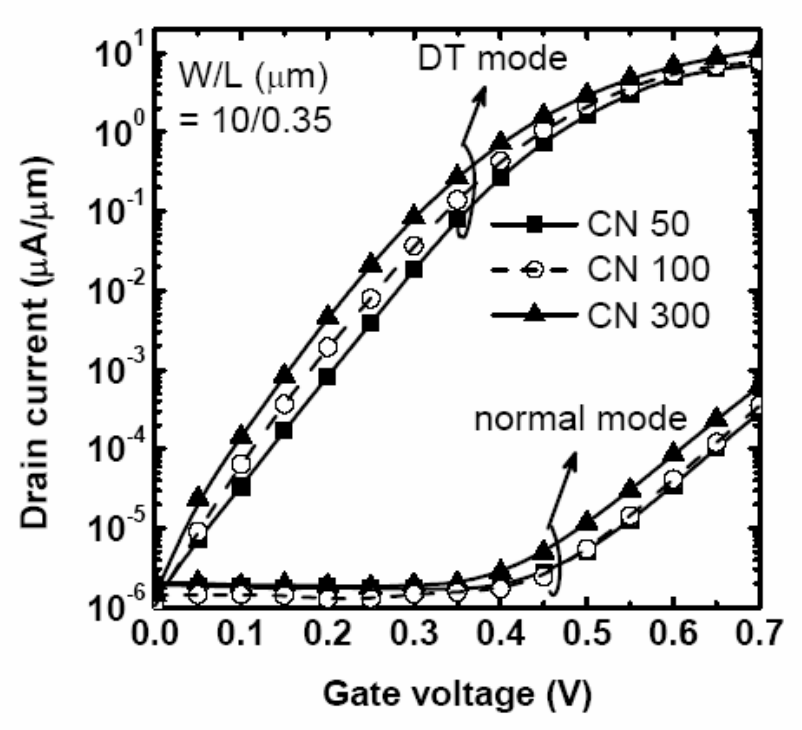


Fig. 5.15. The I_D-V_G transfer characteristics of CESL HfO_2 nMOSFETs with DT and normal operations.

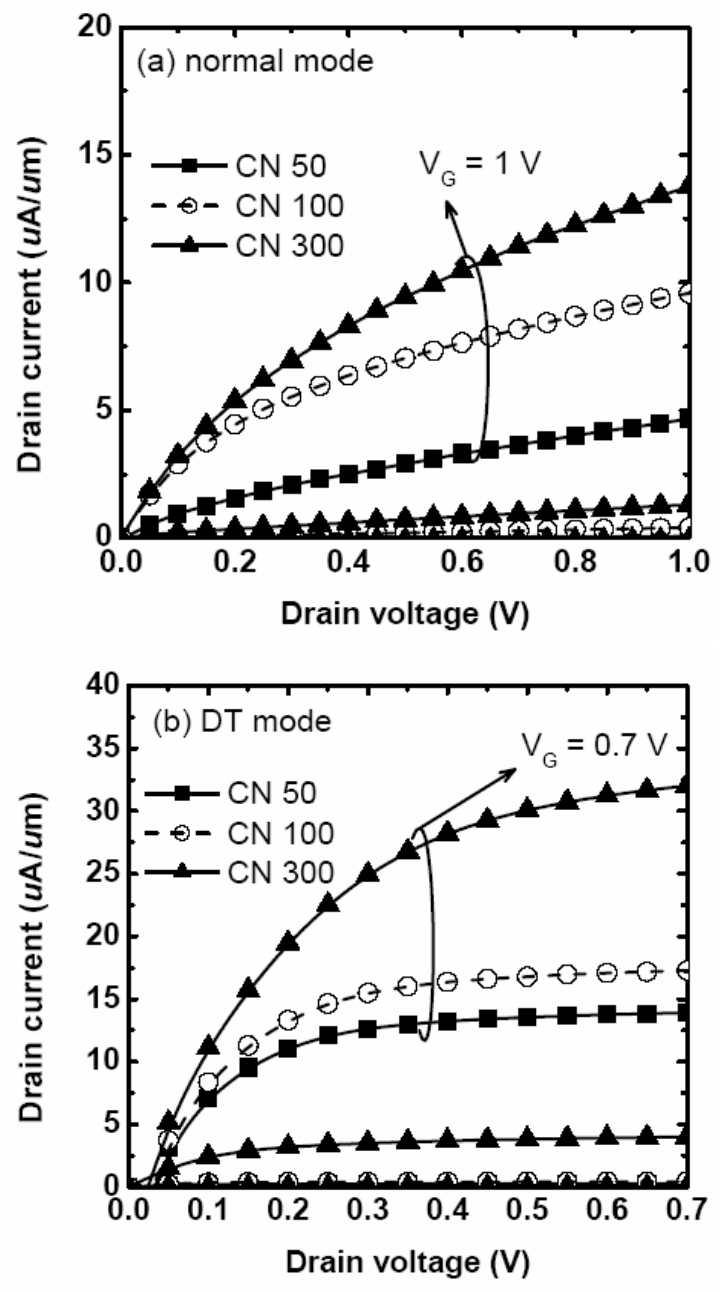


Fig. 5.16. The I_D-V_D characteristics of CESL HfO_2 nMOSFETs with (a) normal and (b) DT operations.

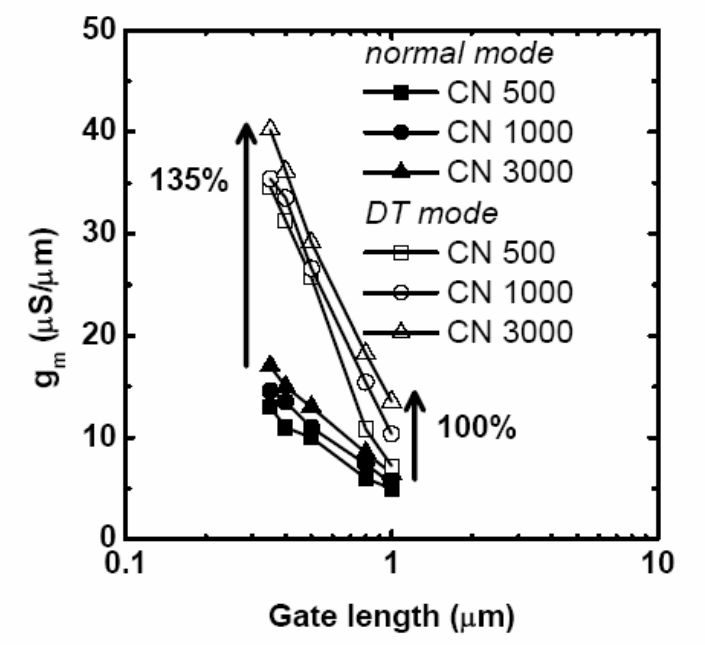


Fig. 5.17. The g_m enhancement can be observed for DT operation mode. g_m increases with channel length decreasing for all CESL HfO_2 nMOSFETs under both DT and normal modes.

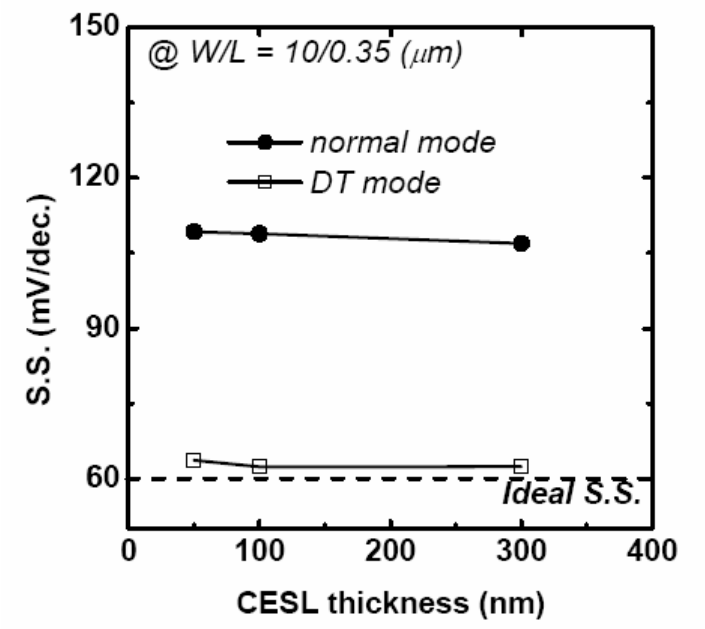


Fig. 5.18. The subthreshold swing can be much improved for all CESL HfO_2 nMOSFETs with DT operation mode.

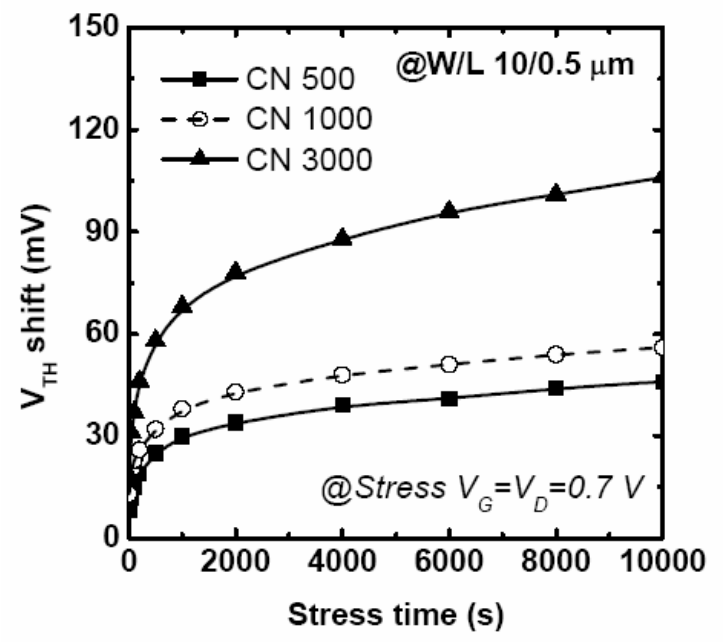


Fig. 5.19. Characteristics of V_{TH} shift for all CESL HfO_2 nMOSFETs with DT HC-stress. V_{TH} shift is only 105 mV for 300 nm nitride capped device after 10000 s HC stress.

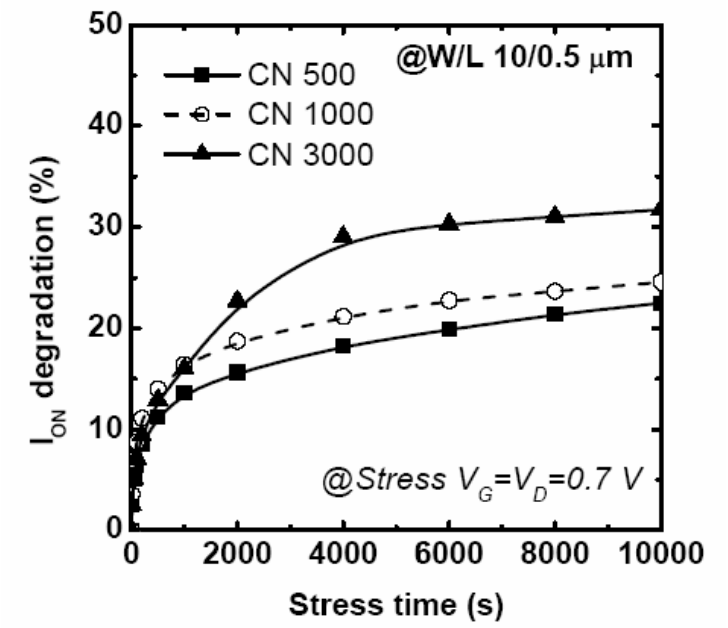


Fig. 5.20(a). Characteristics of I_{ON} degradation for all CESL HfO_2 nMOSFETs with DT HC-stress. I_{ON} degradation is only 32% for 300 nm nitride capped device after 10000 s HC stress.

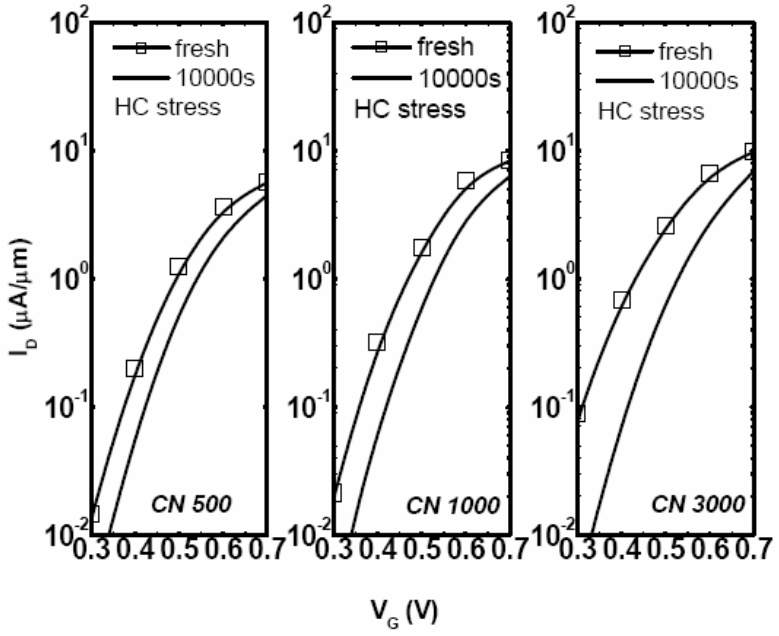


Fig. 5.20(b). I_D-V_G curves of all CESL HfO_2 nMOSFETs before and after DT HC-stress. Only I_{ON} degradation can be observed after 10000 s HC stress for all CESL-devices.

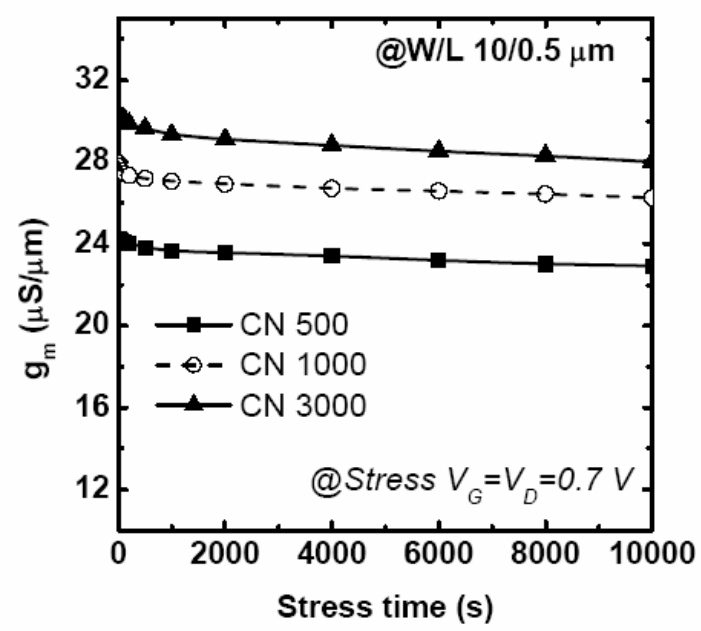


Fig. 5.21. g_m degradation of all CESL HfO_2 nMOSFETs during DT HC-stress.

Chapter 6 Conclusions and Recommendations for Future Works

6.1 Conclusions

In short, this dissertation has involved the CF_4 plasma treatment, fluorine implantation and CESL induced strain technique on HfO_2 gate dielectric, leading to the dielectric performance improvement. Moreover, some reliability issues such as hysteresis, current transport mechanism and charge trapping phenomenon are discussed. Major contributions of each subject in this work are summarized as follows.

First, we describe the characteristics of silicon surface fluorine implantation (SSFI) for HfO_2 films with high-temperature postdeposition annealing. The thermal stability of HfO_2 gate dielectrics is much improved owing to the incorporation of fluorine into HfO_2 thin films. The gate leakage current of the SSFI HfO_2 films is about three orders less than that of samples without any fluorine implantation. In addition, improvements in stress-induced leakage current (SILC) and charge trapping characteristics are realized in the HfO_2 films with the SSFI. The incorporation of fluorine atoms into the HfO_2 films reduces not only interface dangling bonds but also bulk traps, which is responsible for the improvements in properties. On the other hand, the current transportation mechanism of HfO_2 gate dielectrics with TaN metal gate and silicon surface fluorine implantation (SSFI) is also investigated. Based on the experimental results of the temperature dependence of gate leakage current and Fowler–Nordheim tunneling characteristics at 77 K, we have extracted the current transport mechanisms and energy band diagrams for TaN/HfO_2/IL/Si structures with fluorine incorporation, respectively. In particular, we have obtained the following physical quantities: i) fluorinated and as-deposited IL/Si barrier heights (or

conduction band offset): 3.2 eV & 2.7 eV; ii) TaN/ fluorinated and as-deposited HfO_2 barrier height: 2.6 eV & 1.9 eV; and iii) effective trapping levels at 1.25 eV (under both gate and substrate injections) below the HfOF conduction band, 1.04 eV (under gate injection) and 1.11 eV (under substrate injection) below the HfO_2 conduction band, which contributes to Frenkel–Poole conduction.

Second, a process-compatible CF_4 plasma treatment for fabricating high-performance HfO_2 gate dielectrics MOS capacitor is demonstrated. This CF_4 plasma treatment was divided into two parts, which are pre-CF_4 plasma treatment and post-CF_4 plasma treatment, respectively. The effective oxide thickness of high-k gate dielectrics was much reduced by using the pre-CF_4 plasma treatment due to the elimination of the interfacial layer between HfO_2 and Si-substrate. In addition, the Hf-silicide was suppressed and Hf-F bonding was observed for the CF_4 plasma pre-treated sample. On the other hand, the fluorine atoms were effectively incorporated into HfO_2 thin film and HfO_2/Si interface by post-CF_4 plasma treatment. The charge trapping would be eliminated and the interface of the HfO_2 gate dielectrics was also improved. The device post-treated by CF_4 plasma treatment would have low leakage current, higher breakdown voltage, and thinner effective oxide thickness. Besides, the C-V hysteresis was much reduced about 90 %. A physical model was presented to explain the improvement of hysteresis phenomenon and the elimination of charge trapping of the fluorinated HfO_2 gate dielectrics.

Then, a novel high-performance and excellent-reliability CMOS HfO_2 fluorinated by CF_4 plasma treatment was demonstrated. I_{ON}/I_{min} current ratio (~6.69×10^7), S. S. (~76 mV/dec), DIBL (<20 mV), and mobility (~165 $cm^2/V\cdot s$) can be observed for the HfOF nMOSFETs, and I_{ON}/I_{min} current ratio (~1.69×10^8), S. S. (~80 mV/dec), DIBL (<20 mV), and mobility (~67 $cm^2/V\cdot s$) can be observed for the HfOF pMOSFETs. The CMOS HfOF has better HfO_2/Si interface and dielectric

quality, including small GIDL current and less NBTI and PBTI effect. Reduced GIDL current was observed for the CMOS HfOF due to HfO_2/Si interface passivation by fluorine, resulting in less hole-electron pair generation. The fluorine incorporation into HfO_2 gate dielectrics effectively passivated the dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps.

Finally, new observation on SiN-cap strain-induced improved characteristics and PBTI reliability of nMOSFETs with HfO_2 gate dielectrics were reported for the first time. The "close-to-intrinsic" characteristics including driving current and g_m of SiN-capped HfO_2 nMOSFETs were much enhanced about 90% and 50%, respectively by pulse-IV measurement. The CESL-device has better HfO_2/Si interface and dielectric quality, including less charge pumping current (90% reduction) and less PBTI effect (55% reduction). Finally, the performance of CESL-HfO_2 nMOSFETs will have larger g_m (135% increase) and "close-to-ideal" subthresold swing (~62) using dynamic threshold (DT) operation mode with tolerant hot carrier-stress characterization. These results provide a valuable guideline for the future 45 nm and beyond CMOS device design with high-k and strain engineering.

6.2 Recommendations for Future Works

There are some topics that are suggested for future works.

As described in this work, CF_4 plasma treatment provides a good passivation of trap states near the HfO_2/Si interface. However, in this thesis, the CF_4 plasma is generated by a conventional PECVD system. High-density plasma (HDP) and electron cyclotron resonance (ECR) plasma are suggested to further dissociate the fluorine atoms and thus improve the efficiency of fluorine passivation. Furthermore, remote-plasma is believed that it can avoid plasma-induced damage in the Si-substrate

during plasma treatment, especially for the pre-CF_4 plasma treatment technique. Some further studies of this CF_4 plasma treatment can be done by adopting these three plasma systems.

We have demonstrated the high-performance and excellent-reliability HfO_2 nMOSFET fluorinated by CF_4 plasma treatment. However, the novel HfO_2 pMOSFET fluorinated by CF_4 plasma treatment can be further studied. The negative bias temperature instability (NBTI) is also an important issue for HfO_2 pMOSFET. Although fluorine incorporation into HfO_2 gate dielectrics can effectively passivate the dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps. The NBTI mechanism of HfO_2 pMOSFET with post-deposition or pre-CF_4 plasma treatment will be an interesting research topic.

Besides, the applications of HfO_2 gate dielectrics with or without post-deposition and pre-CF_4 plasma treatment to other fields such as silicon-oxide-nitride-oxide-silicon (SONOS) flash memory and Si-based thin film transistors (TFT) could be investigated. A novel SONOS memory structure used HfO_2 gate dielectrics as tunneling, blocking layer, or the charge trapping layer can be extensively studied. Suitable high-k materials and thickness, additional plasma treatment and annealing should be seriously considered.

We have studied the post and pre CF_4 plasma treatment, fluorine implantation and CESL induced strain technique can improve the HfO_2 gate dielectric characteristics. Other high-k gate materials such as ZrO_2, Al_2O_3, Gd_2O_3, La_2O_3, and HfSiON (Hf-silicate) with these advanced passivation technology and strain engineering can be aggressively investigated.

Reference

Chapter 1

[1.1] “International Technology Roadmap for Semiconductors” 2007 Update, published by the Semiconductors Industry Association.

[1.2] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, *IEEE Elec. Dev. Lett,* vol. 18, pp. 209-211, 1997.

[1.3] X. Yu, C. Zhu, M. Yu, M. F. Li, A. Chin, C. H. Tung, D. Gui, and D. L. Kwong : *Tech. Dig. - Int. Electron Devices Meet.,* pp. 30-33, 2005.

[1.4] S. Inumiya, Y. Akasaka, T. Matsuki, F. Ootsuka, K. Torii and Y. Nara : *Tech. Dig. - Int. Electron Devices Meet.*, pp. 26-29, 2005.

[1.5] H. N. Alshareef, H. R. Harris, H. C. Wen, C. S. Park, C. Huffman, K. Choi, H. F. Luan, P. Majhi, B. H. Lee, R. Jammy, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon : V*LSI Symp. Tech. Dig.,* pp. 5-6, 2006.

[1.6] Y. Gao, S. He, P. Alluri, M. Engelhard, A. S. Lea, J. Finder, B. Melnick, and R. L. Hance, *Journal of Appl. Phys.* Vol. 87, No. 1, pp. 124-132, 2000.

[1.7] H. Ono, and K. Koyanagi, *Appl. Phys. Lett.* Vol. 75, pp. 3521-3523, 1999.

[1.8] M. Houssa, R. Degraeve, P. W. Mertens, M. M. Heyns, J. S. Jeon, A. Halliyal, and B. Ogle, *Journal of Appl. Phys.* Vol. 86, No. 11, pp. 6462-6467, 1999.

[1.9] J. Robertson, Mrs Bulletin, vol. 27, no. 3, pp. 217-221, 2002.

[1.10] R. Choi, K. Onishi, C. S. Kang, H. J. Cho, Y. H. Kim, S. Krishnan, M. S. Akbar, and J. C. Lee, *IEEE Elec. Dev. Lett,* vol. 24, no. 3, pp. 144-146, 2003.

[1.11] K. Onishi, C. S. Kang, R. Choi, H. J. Cho, S. Gopalan, R. Neih, S. Krishnan, and J. C. Lee, V*LSI Symp. Tech. Dig.,* pp. 22-23, 2002.

[1.12] K. Onishi, C. S. Kang, R. Choi, H. J. Cho, S. Gopalan, R. Neih, E. Dharmarajan, and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.*, pp.

30.3.1-30.3.4, 2001.

[1.13] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi and A. Nishiyama, *Tech. Dig. - Int. Electron Devices Meet.* pp. 849-852, 2002.

[1.14] W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, *IEEE Elec. Dev. Lett,* vol. 23, no. 11, pp. 649-651, 2002.

[1.15] C. H. Choi, S. J. Ghee, T. S. Jeon, N. Lu, J. H. Sim, R. Clark, M. Niwa, and D. L. Kwong : *Tech. Dig. - Int. Electron Devices Meet.,* pp.857-860, 2002.

[1.16] C. S. Kang, H. J. Cho, K. Onishi, R. Choi, Y. H. Kim, R. Neih, J. Han, S. Krish, A. Mathewson, and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 30.3.1-30.3.4, 2001.

[1.17] B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, and M. R. Lin, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 937-939, 2001.

[1.18] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, and Y. Yoshihara, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 625-628, 2002.

[1.19] G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdahl, *Appl. Phys. Lett.* Vol. 73, pp. 1517-1519, 1998.

[1.20] J. H. Lee, Y. S. Kim, H. S. Jung, J. H. Lee, N. I. Lee, H. K. Kang, J. H. Ku, H. S. Kang, Y. K. Kim, K. H. Cho, and K. P. Suh, V*LSI Symp. Tech. Dig.,* pp. 84-85, 2002.

[1.21] E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. Dimara, S. Guha, A. Callegari, S. Zarfar, P. C. Jamison, D. A. Neumayer, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L. A. ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 451-454, 2001.

[1.22] L. Kang, Y. Jeon, K. Onishi, B. H. Lee, W. J. Qi, R. Neih, S. Gopalan, and J. C. Lee, *VLSI Symp. Tech. Dig.,* pp. 44-45. 2000.

[1.23] S. H. Bae, C. H. Lee, R. Clark, and D. L. Kwong, *IEEE Elec. Dev. Lett,* vol. 24, no. 9, pp. 556-558, 2003.

[1.24] T. Y. Chang, H. W. Chen, T. F. Lei, and T. S. Chao, *IEEE Trans. Electron Devices*, vol. 49, pp. 2163-2170, 2002.

[1.25] H. N. Chern, C. L. Lee, and T. F. Lei, *IEEE Trans. Electron Devices*, vol. 41, pp. 698-702, 1994.

[1.26] S. Maegawa, T. Ipposhi, S. Maeda, H. Nishimura, T. Ichiki, M. Ashida, O. Tanina, Y. Inoue, T. Nishimura and N. Tsubouchi, *IEEE Trans. Electron Devices*, vol. 42, pp. 1106-1111, 1995.

[1.27] J. W. Park, B. T. Ahn, and K. Lee, *Jpn. J. Appl. Phys.*, vol. 34, pp. 1436-1441, 1995.

[1.28] J. C. Wang, S. H. Chiao, C. L. Lee, T. F. Lei, Y. M. Lin, M. F. Wang, S. C. Chen, C. H. Yu, and M. S. Liang, *J. Appl. Phys.* **92,** pp. 3936-3939. 2002.

[1.29] L. Kim, J. Kim, and D. Jung, and Y. Roh, *Appl. Phys. Lett.* Vol. 76, pp. 1881-1883, 2000.

[1.30] Navakanta Bhat, and Krishna C. Saraswat, *J. Appl. Phys.* **84,** pp. 2722-2726. 1998.

[1.31] J. C. Wang, D. C. Shie, T. F. Lei and C. L. Lee, *Electrochem. Solid-State Lett.,* **6**, F34-F36, 2003.

[1.32] K. J. Choi, J. H. Kim, and S. G. Yoon, *J. Electrochem. Soc.* **151**, G262-G265, 2004.

[1.33] C. S. Kang, H. J. Cho, K. Onishi, R. Neih, R. Choi, S. Gopalan, S. Krishnan, J. H. Han, and J. C. Lee, *Appl. Phys. Lett.* **81**, pp. 2593-2595, 2002.

Chapter 2

[2.1] “International Technology Roadmap for Semiconductors” 2006 Update, published by the Semiconductors Industry Association.

[2.2] C. S. Lai and K. M. Fang, *Ext. Abstr. Solid State Device and Materials,* pp. 488 -489, (2003).

[2.3] J. C. Wang, S. H. Chiao, C. L. Lee, T. F. Lei Y. M. Lin, M. F. Wang, S. C. Chen, C. H. Yu, and M. S. Liang, *J. Appl. Phys.* Vol. 92, pp. 3936-3940, 2002.

[2.4] L. F. Schn, R. B. van Dover, and R. M. Fleming, *Appl. Phys. Lett.* Vol. 75, pp. 1967-1969, 1999.

[2.5] B. K. Park, J. Park, M. Cho, C. S. Hwang, K. Oh, Y. Han, and D. Y. Yang, *Appl. Phys. Lett.* Vol. 80, pp. 2368-2370, 2002.

[2.6] B. Tavel, X. Garros, T. Skotnicki, C. Leroux, D. Bensahel, M. N. Semeria, Y. Morand, J. F. Damlencourt, S. Descombes, F. Leverd, Y. L. Friec, P. Leduc, M. Rivoire, S.jullian and R. Pantel, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 429-432, 2002.

[2.7] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi and A. Nishiyama, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 849-852, 2002

[2.8] W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, *IEEE Elec. Dev. Lett,* vol. 23, no. 11, pp. 649-651, 2002

[2.9] T. P. Ma, *Ext. Abstr. Solid State Device and Materials,* p. 30-31, 2004.

[2.10] S. H. Lo, D. A. Buchanan and Y. Taur, *IEEE Elec. Dev. Lett,* vol. 18, pp. 209-211, 1997.

[2.11] J. H. Stathis, and D. J. Dimaria, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 167-170, 1998

[2.12] Y. Mitani, H. Satake, Y. Nakasaki, and A. Toriumi, *IEEE Trans. Electron Devices,* vol. 50, pp. 2221-2226, 2003.

[2.13] Y. Nishioka, K. Ohyu, Y. Ohji, N. Natsuaki, K. Mukai and T. P. Ma, *J. Appl. Phys.,* vol. 66, pp. 3909-3912, 1989.

[2.14] Hiroyuki Ohta, Masaru Hori, and Toshio Goto, *Appl. Phys. Lett.* Vol. 90, pp. 1955-1961, 2002.

[2.15] C. S. Lai, W. C. Wu, K. M. Fang, J. C. Wang and S. J. Lin, *Jpn. J. Appl. Phys.,* Vol.44, No. 4B, pp. 2307-2310, 2005.

[2.16] D. J. DiMaria and E. Cartier, *J. Appl. Phys.*, Vol. 78, pp. 3883-3894, 1995.

[2.17] S. W. Huang, and J. G. Hwu, *IEEE Trans. Electron Devices*, vol. 53, pp. 1608-1614, 2006.

[2.18] L. A. Ragnarsson, V. S. Chang, H. Y. Yu, H. J. Cho, T. Conard, K. M. Yin, A. Delabie, J. Swerts, T. Schram, S. D. Gendt, and S. Biesemans, *IEEE Electron Device Lett.*, vol. 28, pp. 486-488, 2007.

[2.19] Z. Ren, M. V. Fischetti, E. P. Gusev, E. A. Cartier, and M. Chudzik, in *IEDM Tech. Dig.*, pp. 33.2.1–33.2.4, 2003.

[2.20] W. Zhu and T. P. Ma, *IEEE Electron Device Lett.*, vol. 25, pp. 89–91, 2004.

[2.21] R. Singanamalla[1], C. Ravit, G. Vellianitis, J. Petry, V. Paraschiv, J.P. van Zijl, S. Brus, M.Verheijen, R.G.R. Weemaes, M. Kaiser, J.G.M. van Berkum, P. Bancken, R. Vos, H.Yu, K. deMeyer, S. Kubicek, S. Biesemans, and J.C. Hooker, in *IEDM Tech. Dig.*, pp. 23.6.1–23.6.4. 2006.

[2.22] X. Yu, M. Yu, and C. Zhu, *IEEE Electron Device Lett.*, vol. 27, no. 6, pp. 498-501, 2006.

[2.23] M. Cassé, L. Thevenod, B. Guillaumot, L. Tosti, F. Martin, J. Mitard, O. Weber, F. Andrieu, T. Ernst, G. Reimbold, T. Billon, M. Mouis, and F. Boulanger, *IEEE Trans. Electron Devices*, vol. 53, pp. 759-768, 2006.

[2.24] C. S. Lai, W. C. Wu, J. C. Wang and T. S. Chao, *Appl. Phys. Lett.* vol. **86,** pp. 22905-22907, 2005.

[2.25] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 408–410, 2004.

[2.26] S. Datta, G. Dewey, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau, in *IEDM Tech. Dig.*, pp. 28.1.1–28.1.4., 2003.

[2.27] M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, and M. Yoneda, in *IEDM Tech. Dig.*, pp. 17.1.1–17.1.4. 2005.

[2.28] K. Seo, R. Sreenivasan, P. C. McIntyre, and Krishna C. Saraswat, in *IEDM Tech. Dig.*, pp. 17.2.1–17.2.4. 2005.

[2.29] C. S. Lai, W. C. Wu, J. C. Wang and T. S. Chao, *Ext. Abstr. Solid State Device and Materials,* pp. 234-235, 2005.

[2.30] C. S. Lai, W. C. Wu, K. M. Fang, J. C. Wang, and S. J. Lin, *Jpn. J Appl. Phys.,* vol. 44, pp. 2307-2310, 2005.

[2.31] Y. Yasuda, and C. Hu, in *IEDM Tech. Dig.*, pp. 10.5.1–10.5.4. 2006.

[2.32] C. S. Lai, W. C. Wu, J. C. Wang, and T. S. Chao, *Jpn. J Appl. Phys.,* vol. 45, no. 4B, pp. 2893-2897, 2005.

[2.33] C. S. Lai, W. C. Wu, T. S. Chao, J. H. Chen, J. C. Wang, L. L. Tay, and N. Rowell, *Appl. Phys. Lett.,* vol. 89, pp. 072904-072906, 2006.

[2.34] W. C. Wu, C. S. Lai, J. C. Wang, J. H. Chen, M. W. Ma, and T. S. Chao, *J. Electrochem. Soc.,* vol. 154, no. 7, pp. 561-565, 2007.

[2.35] W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, *IEEE Electron Device Lett.*, vol. 23, pp. 97-99, 2002.

[2.36] Z. Xu, M. Houssa, S. D. Gendt and M. Heyns, *Appl. Phys. Lett.* vol. **80,** pp. 1975-1977, 2002.

[2.37] G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J Appl. Phys.,* vol. 89, pp. 5243-5275, 2001.

[2.38] S. M. Sze, *Physics of Semiconductor Devices*, p. 403, Wiley, New York (1981).

Chapter 3

[3.1] X. Yu, C. Zhu, M. Yu, M. F. Li, A. Chin, C. H. Tung, D. Gui, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, pp. 30-33, 2005.

[3.2] S. Inumiya, Y. Akasaka, T. Matsuki, F. Ootsuka, K. Torii and Y. Nara, *Tech. Dig. - Int. Electron Devices Meet.,* pp. 26-29, 2005.

[3.3] H. S. Baik, M. Kim, G. S. Park, S. A. Song, M. Varela, A. Franceschetti, S. T. Pantelides and S. J. Pennycook, *Appl. Phys. Lett.*, **85**, pp. 672-674, 2004.

[3.4] S. Toyoda, J. Okabayashi, H. Kumigashira, M. Oshima, K. Ono, M. Niwa, K. Usuda, and G. L. Liu, *Appl. Phys. Lett.*. **84**, pp. 2328-2330, 2004.

[3.5] S. J. Rhee, C. Y. Kang, C. S. Kang, R. Choi, C. H. Choi, M. S. Akbar, and J. C. Lee, *Appl. Phys. Lett*.. **85**, pp. 1286-1288, 2004.

[3.6] B. K. Park, J. Park, M. Cho, C. S. Hwang, K. Oh, Y. Han, and D. Y. Yang, *Appl. Phys. Lett.* **80**, pp. 2368-2370, 2002.

[3.7] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi, and A. Nishiyama : *Tech. Dig. - Int. Electron Devices Meet.,* pp. 849-851, 2002.

[3.8] W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, *IEEE Electron Device Lett.* **23**, pp. 649-651, 2002.

[3.9] C. H. Choi, S. J. Rhee, T. S. Jeon, N. Lu, J. H. Sim, R. Clark, M. Niwa, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.,* pp. 857-860, 2002.

[3.10] C. S. Kang, H. J. Cho, K. Onishi, R. Choi, R. Nieh, S. Goplan, S. Krishnan, and

J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet*., pp. 865-868, 2002.

[3.11] H. J. Cho, D. G. Park, I. S. Yeo, J. S. Roh, and J. W. Park, *Jpn. J. Appl. Phys.,* **40,** pp. 2814-2818, 2001.

[3.12] C. S. Lai, W. C. Wu, K. M. Fang, J. C. Wang and S. J. Lin, *Jpn. J. Appl. Phys.,* **44,** pp. 2307-2310, 2005.

[3.13] J. C. Wang, D. C. Shie, T. F. Lei and C. L. Lee, *Electrochem. Solid-State Lett.,* **6**, F34-F36, 2003.

[3.14] C. S. Lai, W. C. Wu, J. C. Wang and T. S. Chao, *Appl. Phys. Lett.*, **86,** pp. 22905-22907, 2005.

[3.15] J. E. Olsen, F. Shimura, *J. Appl. Phys.,* **66**, pp. 1353-1357, 1989.

[3.16] M. L. Green, E. P. Gusev, R. Degraeve, E L. Garfunkel, *J. Appl. Phys.*, **90**, pp. 2057-2011, 2001.

[3.17] "International Technology Roadmap for Semiconductors" 2005 Update, published by the Semiconductors Industry Association.

[3.18] J. C. Wang, D. C. Shie, T. F. Lei, and C. L. Lee, *J. Appl. Phys.*, **98,** pp. 024503-024507, 2005.

[3.19] C. S. Lai, W. C. Wu, T. S. Chao, J. H. Chen, J. C. Wang, L. Tay, and N. Rowell, *Appl. Phys. Lett.*, **89,** pp. 072904-072906, 2006.

[3.20] J. C. Wang, D. C. Shie, T. F. Lei, and C. L. Lee, *Electrochem. Solid-State Lett.,* **6**, F34-F36, 2003.

[3.21] C. H. Choi, S. J. Rhee, T. S. Jeon, N. Lu, J. H. Sim, R. Clark, M. Niwa, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.,* pp. 857-860, 2002.

[3.22] R. Choi, C. S. Kang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and Jack C. Lee, *VLSI Symp. Tech. Dig.,* pp. 15-16, 2001.

[3.23] T. P. Ma, *Ext. Abstr. Solid State Device and Materials,* pp. 30-31, 2004.

[3.24] Z. Zhang, M. Li, and S. A. Campbell, *IEEE Electron Device Lett.*, **26,** pp.

20-22, 2005.

[3.25] C. L. Cheng, C. Y. Lu, K. S. Chang-Liao, C. H. Huang, S. H. Wang, and T. K. Wang, *IEEE Trans. Electron Device,* **53,** pp. 63-68, 2006.

[3.26] C. S. Lai, W. C. Wu, J. C. Wang and T. S. Chao, *Appl. Phys. Lett.*, **86,** pp. 22905-22907, 2005.

[3.27] P. F. Lee, J. Y. Dai, K. H. Wong, H. L. W. Chan, and C. L. Choy, *Appl. Phys. Lett.*, **82,** pp. 2419-2411, 2003.

[3.28] M. H. Cho, D. W. Moo, S. A. Park, Y. K. Kim, K. Jeong, S. K. Kang and D. H. Ko, S. J. Doh, J. H. Lee, and N. I. Lee, *Appl. Phys. Lett.*, **84,** pp. 5243-5245, 2004.

[3.29] S. J. Rhee, C. Y. Kang, C. S. Kang, R. Choi, C. H. Choi, M. S. Akbar, and J. C. Lee, *Appl. Phys. Lett.*, **85,** pp. 1286-1288, 2004.

[3.30] C. S. Kang, H. J. Cho, K. Onishi, R. Nieh, R. Choi, S. Gopalan, S. Krishnan, J. H. Han, and J. C. Lee, *Appl. Phys. Lett.*, **81,** pp. 2593-2595, 2002.

[3.31] G. Q. Lo, W. Ting, D. L. Kwong, J. Kuehne, and C. W. Magee, *IEEE Electron Device Lett.,* **11,** pp. 511-513, 1990.

[3.32] P. J. Wright and K. C. Saraswat, *IEEE Trans. Electron Device,* **36,** pp. 879-883, 1989.

[3.33] L. Vishnubhotla, T. P. Ma, H. H. Tseng, and P. J. Tobin, *IEEE Trans. Electron Device,* **14,** pp. 196-201, 1993.

[3.34] S. Lee, and J. W. Park, *J. Appl. Phys.*, **80**, pp. 5260-5265, 1996.

[3.35] C. S. Lai, W. C. Wu, J. C. Wang and T. S. Chao, *Ext. Abstr. Solid State Device and Materials,* pp. 234-235, 2005.

[3.36] M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, and M. Yoneda, *Tech. Dig. - Int. Electron Devices Meet.,* pp. 402-405, 2005.

[3.37] K. Seo, R. Sreenivasan, P. C. McIntyre, and Krishna C. Saraswat, *Tech. Dig. -*

Int. Electron Devices Meet., pp. 406-4089, 2005.

[3.38] Y. Mitani, H. Satake, Y. Nakasaki, and A. Toriumi*, IEEE Trans. Electron Device,* **50,** pp. 2221-2226, 2003.

[3.39] J. C. Wang, S. H. Chiao, C. L. Lee, T. F. Lei, Y. M. Lin, M. F. Wang, S. C. Chen, C. H. Yu, and M. S. Liang, *J. Appl. Phys.*, **92,** pp. 3936-3940, 2002.

[3.40] I. Rahat and J. Shappir, *J. Appl. Phys.,* **76**, pp. 2279-2283, 1994.

Chapter 4

[4.1] S. W. Huang, and J. G. Hwu, *IEEE Trans. Electron Devices*, vol. 53, pp. 1608-1614, 2006.

[4.2] L. A. Ragnarsson, V. S. Chang, H. Y. Yu, H. J. Cho, T. Conard, K. M. Yin, A. Delabie, J. Swerts, T. Schram, S. D. Gendt, and S. Biesemans, *IEEE Electron Device Lett.*, vol. 28, pp. 486-488, 2007.

[4.3] C. S. Lai, W. C. Wu, T. S. Chao, J. H. Chen, J. C. Wang, L. L. Tay, and N. Rowell, *Appl. Phys. Lett.,* vol. 89, pp. 072904-072906, 2006.

[4.4] C. S. Lai, W. C. Wu, J. C. Wang, and T. S. Chao, *Jpn. J Appl. Phys.,* vol. 45, no. 4B, pp. 2893-2897, 2005.

[4.5] W. C. Wu, C. S. Lai, J. C. Wang, J. H. Chen, M. W. Ma, and T. S. Chao, *J. Electrochem. Soc.,* vol. 154, no. 7, pp. H561-H565, 2007.

[4.6] X. Yu, M. Yu, and C. Zhu, *IEEE Electron Device Lett.*, vol. 27, no. 6, pp. 498-501, 2006.

[4.7] M. Cassé, L. Thevenod, B. Guillaumot, L. Tosti, F. Martin, J. Mitard, O. Weber, F. Andrieu, T. Ernst, G. Reimbold, T. Billon, M. Mouis, and F. Boulanger, *IEEE Trans. Electron Devices*, vol. 53, pp. 759-768, 2006.

[4.8] C. S. Lai, W. C. Wu, J. C. Wang and T. S. Chao, *Appl. Phys. Lett.* vol. 86**,** pp.

22905-22907, 2005.

[4.9] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 408-410, 2004.

[4.10] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, pp. 1-18, 2003.

[4.11] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, *J. Electrochem. Soc.*, vol. 114, pp. 266-274, 1967.

[4.12] N. Shiono and T. Yashiro, *Jpn. J. Appl. Phys.*, vol. 18, pp. 1087-1095, 1979.

[4.13] K. Onishi, C. S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. C. Lee, in *Proc. IRPS*, pp. 419-420, 2002.

[4.14] J. F. Zhang and W. Eccleston, *IEEE Trans. Electron Devices*, vol. 45, pp. 116–124, 1998.

[4.15] M. Bourcerie, B. S. Doyle, J.-C. Marchetaux, J.-C. Soret, and A. Boudou, *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 708–717, 1990.

[4.16] W. T. Lu, P. C. Lin, T. Y. Huang, C. H. Chien, M. J. Yang, I. J. Huang, and P. Lehnen, *Appl. Phys. Lett.*, vol. 85, no. 16, pp. 3525–3527, 2004.

[4.17] R. Degraeve, A. Kerber, P. Roussel, E. Cartier, T. Kauerauf, L. Pantisano, and G. Groeseneken, in *IEDM Tech. Dig.*, pp. 935–938, 2003.

[4.18] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur and C. Parthasarathy, *IEEE Trans. Dev. Mat. Reliab.* pp. 5–19, 2005.

[4.19] M. Rosar, B. Leroy, and G. Schweeger*, IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 154-159, 2000.

[4.20] T. Wang, T. E. Chang, L. P. Chiang, C. H. Wang, N. K. Zous, and C. Huang, *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1511-1517, 1998.

[4.21] J. H. Chen, S. C. Wong, and Y. H. Wang, *IEEE Trans. Electron Devices*, vol.

48, no. 7, pp. 1400-1405, 2001.

[4.22] Y. Yasuda, N. Kimizuka, T. Iwamoto, S. Fujieda, T. Ogura, H. Watanabe, T. Tatsumi, I. Yamamoto, K. Ito, Y. Yamagata, and K. Imai, in *Symp. VLSI Tech. Dig.*, pp. 40-41, 2004.

[4.23] M. Gurfinkel, J. S. Suehle, J. B. Bernstein, and Y. Shapira, *Tech. Dig. - Int. Electron Devices Meet.,* pp. 402-405, 2006.

[4.24] K. Uwasawa, T. Yamamoto, and T. Mogami, in *IEDM Tech Dig.*, pp. 871–874, 1995.

[4.25] K. O. Jeppson and C. M. Svensson, *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, 1977.

[4.26] D. K. Schroder and J. A. Babcock, *J. Appl. Phys.*, vol. 94, no. 1, pp. 1–18, 2003.

[4.27] Y. Mitani, M. Nagamine, H. Satake, and A. Toriumi, in *IEDM Tech. Dig.*, 2002, pp. 509–512.

[4.28] Y. Mitani, in *IEDM Tech. Dig.*, pp. 117–120, 2004.

[4.29] S. Mahapatra, P. Bharath Kumar, and M. A. Alam, *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1371–1379, 2004.

[4.30] S. Mahapatra and M. A. Alam, in *IEDM Tech. Dig.*, pp. 505–509, 2002.

[4.31] S. Zafar, "Statistical mechanics based model for negative bias temperature instability induced degradation," *J. Appl. Phys.*, vol. 97, no. 10, pp. 103 709-1–103 709-9, 2005.

[4.32] A. Haggag, W. McMahon, K. Hess, K. Cheng, J. Lee, and J. Lyding, in *Proc. Int. Reliab. Phys. Symp.*, pp. 271–279, 2001.

[4.33] S. Ogawa and N. Shiono, *Phys. Rev. B, Condens. Matter*, vol. 51, no. 7, pp. 4218–4230, 1995.

[4.34] M. Alam, in *IEDM Tech. Dig.*, pp. 345–348, 2003.

[4.35] M. Alam and S. Mahapatra, *Microelectron. Reliab.*, vol. 45, no. 1, pp. 71–81, 2005.

[4.36] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, in *Proc. Int. Reliab. Phys. Symp.*, pp. 273–282, 2004.

[4.37] B. Kaczer, V. Arkhipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin, in *Proc. Int. Reliab. Phys. Symp.*, pp. 381–387, 2005.

[4.38] S. Tsujikawa, T. Mine, K. Watanabe, Y. Shimamoto, R. Tsuchiya, K. Ohnishi, T. Onai, J. Yugami, and S. Kimura, in *Proc. Int. Reliab. Phys. Symp.*, pp. 183–188, 2003.

[4.39] S. S. Tan, C. H. Ang, C. M. Lek, T. P. Chen, B. J. Cho, A. See, and L. Chan, in *Proc. Int. Symp. Phys. and Failure Anal. Intergr. Circuits*, pp. 254–258, 2002.

[4.40] D. Varghese, D. Saha, S. Mahapatra, K. Ahmed, F. Nouri, and M. Alam, in *IEDM Tech. Dig.*, pp. 701–704, 2005.

[4.41] S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, *IEEE Electron Device Lett.*, vol. 18, pp. 209–211, 1997.

[4.42] J. H. Stathis and D. J. DiMaria, in *IEDM Tech. Dig.*, pp. 167–170, 1998.

[4.43] Y. Harada, M. Niwa, S. Lee, and D.-L. Kwong, in *VLSI Tech. Dig.*, pp. 26–27, 2002.

[4.44] S. J. Lee, S. J. Rhee, R. Clark, and D. L. Kwong, in *VLSI Tech. Dig.*, pp. 78–79, 2002.

[4.45] A. Shanware, J. McPherson, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, H. Bu, M. J. Bevan, R. Khamankar, and L. Colombo, in *IEDM Tech. Dig.*, pp. 137–140, 2001.

[4.46] E. P. Gusev, D. A. Buchanan, E. Cartier,A. Kumar,D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. C. Jamison, D. A. Neumayer, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-Å. Ragnarsson,

P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, in *IEDM Tech. Dig.*, pp. 451–454, 2001.

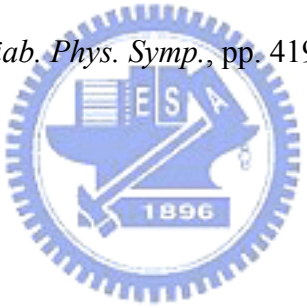
[4.47] A. Kumar, T. H. Ning, M. V. Fischetti, and E. Gusev, in *VLSI Tech. Dig.*, pp. 152–153, 2002.

[4.48] K. Onishi, C. S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, E. Dharmarajan, and J. C. Lee, in *IEDM Tech. Dig.*, pp. 659–662, 2001.

[4.49] R. Choi, C. S. Kang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. C. Lee, in *VLSI Tech. Dig.*, pp. 15–16, 2001.

[4.50] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C. S. Kang, B. H. Lee, R. Nieh, and J. C. Lee, in *VLSI Tech. Dig.*, pp.131–132, 2001.

[4.51] K. Onishi, C. S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. C. Lee, in *Proc. Int. Reliab. Phys. Symp.*, pp. 419–420, 2002.



Chapter 5

[5.1] C. S. Lai, W. C. Wu, J. C. Wang, and T. S. Chao, *Jpn. J Appl. Phys.,* vol. 45, no. 4B, pp. 2893-2897, 2005.

[5.2] W. C. Wu, C. S. Lai, J. C. Wang, J. H. Chen, M. W. Ma, and T. S. Chao, *J. Electrochem. Soc.,* vol. 154, no. 7, pp. 561-565, 2007.

[5.3] C. D. Young, G. Bersuker, G. A. Brown, P. Lysaght, P. Zeitzoff, R. W. Murto, and H. R. Huff, *IEEE 42" Annual International Reliability Physics Symposium.,* pp. 597-598, 2004

[5.4] B. H. Lee, J. H. Sim, R. Choi, G. Bersuker, K. Matthews, N. Moumen, J. J. Peterson, and L. Larson, *IEEE 42" Annual International Reliability Physics Symposium.,* pp. 691-692, 2004

[5.5] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews,

G. A. Brown, and G. Bersuker, *IEEE 43" Annual International Reliability Physics Symposium.,* pp. 75-79, 2005

[5.6] C. D. Young, Y. Zhao, M. Pendley, B. H. Lee, K. Matthews, J. H. Sim, R. Choi, G. A. Brown, R. W. Murto, and G. Bersuker, *Jpn. J Appl. Phys.,* vol. 44, no. 4B, pp.2437-2440, 2005.

[5.7] C. T. Lin, Y. K. Fang, W. K. Yeh, C. M. Lai, C. H. Hsu, L. W. Cheng, and G. H. Ma, *IEEE Electron Device Lett.,* vol. 28, pp. 376-378, 2007.

[5.8] S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, in *IEDM Tech. Dig.*, pp. 213–216. 2004.

[5.9] T. Y. Lu, and T. S. Chao, *IEEE Electron Device Lett.,* vol. 26, pp. 267-269, 2005.

[5.10] S. Ito, H. Namba, K. Yamaguchi, T. Hirata, K. Ando, S. Koyama, S. Kuroki, N. Ikezawa, T. Suzuki, T. Saitoh and T. Horiuchi, n *IEDM Tech. Dig.*, pp. 247-250, 2000.

[5.11] C. Ortolland, P. Morin, C. Chaton, E. Mastromatteo, C. Populaire, S. Orain, F. Leverd, P. Stolk, F. Boeuf and F. Arnaud, in *Symp. VLSI Tech. Dig.*, pp. 78-79, 2006.

[5.12] J. S. Goo, Q. Xiang, Y. Takamura, F. Arasnia, E. N. Paton, P. Besser, J. Pan, and M. R. Lin, *IEEE Electron Device Lett.,* vol. 24, pp. 568-570, 2003.

[5.13] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, *IEEE Trans. Electron Devices*, vol. 31, no. 1, pp. 42–53, 1984.

[5.14] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1318–1335, 1989.

[5.15] S. Inumiya, Y. Akasaka, T. Matsuki, F. Ootsuka, K. Torii and Y. Nara, *Tech. Dig. - Int. Electron Devices Meet.,* pp. 26-29, 2005.

[5.16] M. L. Green, E. P. Gusev, R. Degraeve, E. L. Garfunkel, *J. Appl. Phys.*, **90**, pp. 2057-2011, 2001.

[5.17] J. C. Wang, D. C. Shie, T. F. Lei, and C. L. Lee, *Electrochem. Solid-State Lett.,* **6**, F34-F36, 2003.

[5.18] J. C. Wang, D. C. Shie, T. F. Lei, and C. L. Lee, *J. Appl. Phys.*, **98,** pp. 024503-024507, 2005.

[5.19] T. S. Chao, Y. J. Lee, C. T. Huang, H. C. Lin, Y. Li, and T. Y. Huang, *Jpn. J. Appl. Phys.,* **43,** pp. 1300-1304, 2004.

[5.20] S. J. Chang, C. Y. Chang, T. S. Chao, and T. Y. Huang, *IEEE Electron Device Lett.*, **21,** pp. 127-129, 2000.

[5.21] M. Takamiya, and T Hiramoto, *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1633-1640, 2001.

[5.22] W. C. Lo, S. J. Chang, C. Y. Chang, and T. S. Chao, *IEEE Electron Device Lett.*, **23,** pp. 497-499, 2002.

[5.23] M. S. Shieh, P. S. Chen, M. J. Tsai, and T. F. Lei, *IEEE Electron Device Lett.*, **26,** pp. 740-742, 2005.

[5.24] F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. K. KO, and C. Hu, *IEEE Electron Device Lett.*, **15,** pp. 510-512, 1994.

[5.25] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. KO, and C. Hu, *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414-422, 1997.

[5.26] W. Jin, Philip, C. H. Chan, and M. Chan, *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1717-1724, 1998.

[5.27] T. L. Hsu, Denny D. L. Tang, and J. Gongi, *IEEE Electron Device Lett.*, **20,** pp. 532-534, 1999.

[5.28] S. M. Sze, and C. Y. Chang, *ULSI Devices*: Wiley, 2000.

Publication List

International Journal:

[1] Chao Sung Lai**,** **Woei Cherng Wu,** Kung Ming Fan, Jer Chyi Wang, and Shian Jyh Lin, "Effects of Post CF_4 Plasma Treatment on the HfO_2 Thin Film," *Japanese Journal of Applied Physics,* Vol. 44, No. 4B, pp. 2307–2310, 2005.

[2] Chao Sung Lai**,** **Woei Cherng Wu**, Jer Chyi Wang, and Tien Sheng Chao, "Characteristics of Fluorine Implantation for HfO_2 Gate Dielectrics with High-Temperature Postdeposition Annealing," *Japanese Journal of Applied Physics,* Vol. 45, No. 4B, pp. 2893-2897, 2006.

[3] **Woei Cherng Wu**, Chao Sung Lai**,** Jer Chyi Wang, Ming Wen Ma, and Tien Sheng Chao, "High Performance HfO_2 Gate Dielectrics Fluorinated by Post-deposition CF_4 Plasma Treatment," *Journal of the Electrochemical Society,* Vol. 154, No. 7, pp. H561-H565, 2007.

[4] **Woei Cherng Wu**, Tien Sheng Chao, Wu Ching Peng, Wen Luh Yang, Jian Hao Chen, Chao Sung Lai, and Tsung Yu Yang, Chien Hsing Lee, Tsung Min Hsieh, Jhyy Cheng Liou, Tzu Ping Chen, Chien Hung Chen, Chih Hung Lin, Hwi Huang Chen, and Joe Ko, "Optimized ONO Thickness for Multi-level and 2-bit/cell Operation for Wrapped-Select-Gate (WSG) SONOS Memory," *Semiconductor Science and Technology,* vol. 23, p. 015004, 2008.

[5] **Woei Cherng Wu**, Chao Sung Lai, Zhu Ming Wang, Jer Chyi Wang, Ming Wen Ma, and Tien Sheng Chao "Carrier Transportation Mechanism of $TaN/HfO_2/IL/Si$ Structure with Silicon Surface Fluorine Implantation (SSFI)" had been **revised** to *IEEE Trans. on Electron Device.*

International Letter:

[1] Chao Sung Lai**,** **Woei Cherng Wu**, Jer Chyi Wang, and Tien Sheng Chao, "Characterization of CF_4-Plasma Fluorinated HfO_2 Gate Dielectrics with TaN Metal Gate," *Applied Physics Letters,* **86**, pp. 222905-222907, 2005.

[2] Chao Sung Lai**,** **Woei Cherng Wu,** Tien Sheng Chao, Jian Hao Chen, Jer Chyi Wang, Li-Lin Tay, and Nelson Rowell, "Suppression of Interfacial Reaction for HfO_2 on Silicon by Pre-CF_4 Plasma Treatment," *Applied Physics Letters,* **89**, pp. 072904-072906, 2006.

[3] **Woei Cherng Wu**, Tien Sheng Chao, Wu Chin Peng, Wen Luh Yang, Jer Chyi Wang, Jian Hao Chen, Chao Sung Lai, and Tsung Yu Yang, "Highly Reliable Multi-level and 2-bit/cell Operation of Wrapped-Select-Gate (WSG) SONOS Memory," *IEEE Electron Device Letters,* vol. 28, pp. 214-216, 2007.

[4] **Woei-Cherng Wu**, Chao-Sung Lai, Zhu Ming Wang, Jer-Chyi Wang, Ming Wen Ma, and Tien-Sheng Chao "Current Transport Mechanism of HfO_2 Gate Dielectric with Fluorine Incorporation," *Electrochemical and Solid-State Letters,* Vol. 11, No. 1, pp. H15-H18. 2008.

[5] **Woei Cherng Wu,** Tien Sheng Chao, Te Hsin Chiu, Jer Chyi Wang, Chao Sung Lai, Ming Wen Ma, Wen Cheng Lo, and Yi Hsun Ho "Performance Enhancement for Contact Etch Stop Layer (CESL) Strained nMOSFET with HfO_2 Gate Dielectrics under Pulsed-IV Measurement," had been **revised** to *Electrochemical and Solid-State Letters.*

International Conference:

[1] Chao Sung Lai**,** **Woei Cherng Wu,** Kung Ming Fan, Jer Chyi Wang and Shian Jyh Lin, "Hysteresis Improvements for HfO_2 by CF_4 Plasma Treatment," *International Solid State Devices and Materials (SSDM)*, pp. 742-743, 2004.

[2] Chao Sung Lai, **Woei Cherng Wu**, Hui Hsin Hsu, Pai Chi Chou and Shu Jen Wu,

"The Polarity Dependence of Capacitances for HfO_2 Affected by Post-CF_4 Plasma Treatment," *IEEE International Conference on Semiconductor Electronics (ICSE) proceedings,* pp. 565-568, 2004.

[3] Chao Sung Lai**,** **Woei Cherng Wu**, Jer Chyi Wang and Tien Sheng Chao, "Thermal Stability Improvements for HfO_2 by Fluorine Implantation," *International Solid State Devices and Materials (SSDM)*, pp. 234-235, 2005.

[4] Jer Chyi Wang, **Woei Cherng Wu**, Chao Sung Lai, Jam Wem Lee, Kuo Cheng Chiang, De Ching Shie, Tan Fu Lei and Chung Len Lee, "Characterization of Novel HfTiO Gate Dielectrics Post-treated by NH_3 Plasma and Ultra-violet Rays," *International Solid State Devices and Materials (SSDM)*, pp. 242-243, 2005.

[5] **Woei Cherng Wu**, Chao Sung Lai**,** Kuan Ti Wang, Jer Chyi Wang and Tien Sheng Chao, "Current Transportation Mechanism and Interface States Characterization of Sputtered Gd_2O_3 Gate Dielectrics for ULSI Application," *International Solid State Devices and Materials (SSDM)*, pp. 1100-1101, 2006.

[6] **Woei Cherng Wu**, Tien Sheng Chao, Wu Chin Peng, Wen Luh Yang, Jer Chyi Wang, Jian Hao Chen, Chao Sung Lai, and Tsung Yu Yang, "Highly Reliable Multi-level and 2-bit/cell Operation of Wrapped-Select-Gate (WSG) SONOS Memory with Optimized ONO Thickness," *IEEE International Symposium on VLSI Technology, System & Applications (VLSI-TSA),* pp. 1-2, 2007.

[7] **Woei Cherng Wu**, Chao Sung Lai**,** Zhu Ming Wang, Jer Chyi Wang, Ming Wen Ma, and Tien-Sheng Chao, "Current Transport Mechanism of HfO_2 Gate Dielectric with Silicon Surface Fluorine Implantation (SSFI) in CMOS Application," *International Solid State Devices and Materials (SSDM)*, pp. 408-409, 2007.

[8] **Woei Cherng Wu,** Tien Sheng Chao, Te Hsin Chiu, Jer Chyi Wang, Chao Sung Lai, Ming Wen Ma, Wen Cheng Lo, and Yi Hsun Ho, "Performance Enhancement for Strained HfO_2 nMOSFET with Contact Etch Stop Layer (CESL) under Pulsed-IV

Measurement," *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC),* 2007.

[9] Kuan Ti Wang**,** Tien Sheng Chao, **Woei Cherng Wu,** Chao Sung Lai, Chien Hsing Lee, Tsung Min Hsieh, Jhyy Cheng Liou, Tzu Ping Chen, Chien Hung Chen, Chih Hung Lin, Hwi Huang Chen, and Joe Ko, "The Polarity Dependence of ONO Thickness for Wrapped-Select-Gate (WSG) SONOS Memory," *IEEE International Workshop on Memory Technology, Design and Testing (MTDT),* 2007.

Local Conference:

[1] **Woei Cherng Wu**, Chao Sung Lai**,** Jer Chyi Wang and Tien Sheng Chao, "High-Quality Fluorinated HfO_2 Gate Dielectrics" *Symposium in Nano Device Technology (SNDT),* 2006. **(Silver Medal Award)**

[2] **Woei Cherng Wu**, Tien Sheng Chao, Kuan Ti Wang, Jer Chyi Wang and Chao Sung Lai "Interface Characterization of Sputtered Gd_2O_3 Gate Dielectrics on Silicon with High Temperature Postdeposition Annealing in CMOS Application," *Symposium in Nano Device Technology (SNDT),* 2007.

學經歷

姓名: 吳偉成

性別: 男

出生: 民國67 年12 月26 日

籍貫: 台灣台北市

住址: 新竹縣竹北市勝利七街一段196號10樓

學歷: 長庚大學電子工程學系［87 年9 月- 91 年6 月］

長庚大學電子工程研究所碩士班［91 年9 月- 93 年6 月］

國立交通大學電子物理所博士班［93 年9 月- 97 年3 月］

博士論文題目:

氧化鉿閘極介電層之氟鈍化製程與應力工程的研究

Study on Fluorine Passivation Techniques and Strain Engineering for HfO_2 Gate Dielectrics