

國立交通大學

光電工程學系 光電工程研究所
碩士論文

五環素有機薄膜電晶體之
操作原理與可靠度分析

Device Mechanism and Reliability of
Pentacene-based OTFTs



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中華民國九十五年七月

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摘要

有機薄膜電晶體在面板技術的應用上，由於其具有可彎曲、低溫下製作和低成本優勢，所以是非常合適用來製作低成本的電子元件。通常製作有機元件時會利用表面處理的方式來增加載子的移動率。但卻沒有人針對處理過後元件的可靠度做分析。因此論文研究利用兩種不同的表面處理過的元件和標準元件在DC及AC Stress下的變化。

首先，我們設計Gate Four-Probe(GFP)結構來萃取通道內部的電性特性，由此萃取出薄膜的本質參數。我們分析由Gate Four-Probe(GFP)所得到的電位可發現有機元件的傳輸機制與載子漂移的機制相當類似。之後我們將Gate Four-Probe(GFP)結構做在不同表面處理過後的基板上。論文中的元件分為標準和兩種不同表面處理的元件。標準元件只利用RCA清洗，其他的元件分別用HMDS或ODMS處理。一開始使用DC Stress，可發現標準元件對於負偏壓的Stress， V_{TH} 漂移量小但是對於正偏壓 V_{th} 漂移量大。而有表面處理的元件不管是正負偏壓， V_{th} 漂移量都比標準片大。由Gate Four-Probe(GFP)所分析出的參數顯示pentacene薄膜並不隨Stress時間有所改變。因此 V_{th} 的改變應該是來自於Oxide或是表面處理layer所貢獻的。利用AC Stress，標準片的 V_{th} 漂移量大幅下降顯示出標準片在AC操作下具有較好的可靠度。但是有處理的HMDS和ODMS的 V_{th} 卻仍然有著較大的漂移量。經HMDS處理後的元件對於頻率和duty-cycle的相關性較大而利用ODMS處理的元件相關性較小。

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Abstract

Due to fixable, low temperature process and low cost, application of organic thin film transistor on flat plane display is very suitable to fabricate low cost device. Usually, surface treatment is used to increase mobility of carrier transport in organic thin film transistor. Until now, without anyone analyze reliability of device which is treated. Therefore this paper studies variation of device with and without surface treatment under different DC and AC stress condition.

Firstly, we design Gated-Four-Probe (GFP) structure to extract characteristic of device in channel. Analysis of voltage distribution from Gated-Four-Probe can find that carrier transport mechanism of OTFT is consistent with carrier drift mechanism. Subsequently we fabricate Gated-Four-Probe (GFP) structure on different surface treatment substrate. The devices in this paper are separate to standard and two kinds of surface treatment. Standard device is cleaned by RCA clean and the other devices are treated by HMDS or ODMS. Initially, under DC stress condition we can find threshold voltage shift at positive gate bias stress is larger than at negative gate bias stress. Whether at positive or negative gate bias stress condition, V_{th} shift of devices

with surface treatment are larger than standard devices. The extracted parameters from Gated-Four-Probe (GFP) indicate that pentacene film is not changed with time. Therefore reliability issues lie in the gate insulator or SAM layer degradation. Under AC stress condition, V_{th} shift of standard devices are obvious decrease. It appears that standard devices have better reliability at AC operation. But V_{th} shift of devices with HMDS and ODMS still have lager value.



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Contents

Chinese Abstract	I
English Abstract	II
誌謝	IV
Contents	V
Figure Captions	VII

Chapter 1. Introduction

1-1 Overview of Organic TFT Technology	1
1-2 Organic semiconducting materials	2
1-3 Operating mode of organic thin film transistor	2
1-4 Contact resistance in Organic thin film transistors	4
1-5 Surface treatment	5
1-6 Reliability	6
1-7 Motivation	7
1-8 Thesis	7



Chapter 2. Experiment

2-1 Overview of Organic TFT Structure	8
2-1.1 Shadow mask process	8
2-1.2 Surface treatment	9
2-2 Gated four-probe measurements	9
2-2.1 Theory of gated four-probe measurements	9
2-2.2 Gated four-probe structure	12
2-2.3 Current-voltage characterization	12
2-2.4 Potential measurements	13
2-3 Reliability	
2-3.1 Configuration of Measurement Equipments	14
2-3.2 Waveform of the AC Signal	14
2-3.3 Measurement Methods	15

Chapter 3. Analysis and Result

3-1	Gated four-probe analysis	16
3-1.1	Current-Voltage characterization	16
3-1.2	Potential measurements	16
3-1.3	Contact resistance	17
3-1.4	Film Resistance Analysis	18
3-1.5	Mobility Analysis	19
3-2	DC reliability analysis	20
3-2.1	DC bias stress analysis	20
3-2.2	Influence of bias stress on thermal Oxide insulator Pentacene-based TFT	21
3-2.3	Influence of bias stress on HMDS surface treatment	22
3-2.4	Influence of bias stress on ODMS surface treatment	23
3-3	AC reliability analysis	24
3-3.1	Without Surface Treatment	24
3-3.1.1	Frequency dependence	24
3-3.1.2	Duty-cycle dependence	25
3-3.2	HMDS Surface Treatment	26
3-3.2.1	Frequency dependence	26
3-3.2.2	Duty-cycle dependence	26
3-3.3	ODMS Surface Treatment	27
3-3.3.2	Frequency dependence	27
3-3.3.3	Duty-cycle dependence	28

Chapter 4. Conclusion

4-1	Gated-Four-Probe measurement	29
4-2	Reliability of organic thin film transistor	30

Reference	31
------------------	-----------

Figures	34
----------------	-----------

Figure Captions

Chapter 1

Fig. 1.1 Molecular structure of (a) sexithiophene and (b) pentacene.

Fig. 1.2 Semilogarithmic plot of mobility vs. year

Fig. 1.3 (a) Top contact structure and (b) Bottom contact structure.

Fig. 1.4 Work function of various metals and ionization potential of pentacene.

Fig. 1.5 Schematic view of a bottom-gate thin-film transistor.

Chapter 2

Fig. 2.1 Top view and cross section of the gated-four-probe a-Si:H TFT structure.

Fig. 2.2 show a schematic of the four-probe geometry used to determine film and contact resistance.

Fig. 2.3 Measurement configuration for the organic thin film transistor

Fig. 2.4 Waveform and definition of the AC signal

Chapter 3

Fig. 3.1 Current V.S voltage plots for pentacene thin films with (a) Standard (b) HMDS and (c) ODMS surface treatments.

Fig. 3.2 Potential data and surface plots for devices with Standard, HMDS and ODMS surface treatment. (a), (b) and (c) potential data acquired via the channel potential probes as a function of V_G . Shown are the probe data, V_1 and V_2 , along with the extrapolated contact potential

differences at the contacts ΔV_S and ΔV_D .

Fig. 3.3 Potential drops at the source with (a) Standard (b) HMDS and (c) ODMS surface treatments.

Fig. 3.4 Potential drops at the drain with (a) Standard (b) HMDS and (c) ODMS surface treatments.

Fig. 3.5 The corresponding energy band of the OTFT operated at different region

Fig. 3.6 Show the film resistances (R_{Film}) and contact resistances (R_D and R_S) as a function of gate voltage for (a) Standard (b) HMDS and (c) ODMS surface treatments top-contacted devices.

Fig. 3.7 illustrate R_{Film} V.S Channel length at $V_G = -60V$.

Fig. 3.8 illustrate R_{Film} V.S $1/(V_G - V_T)$ for (a) Standard (b) HMDS and (c) ODMS surface treatments top-contacted devices.

Fig. 3.9 (a) and (b) show that mobility which was extracted by gated-four-probe method was not depend on channel length variation.

Fig. 3.10 The transfer characteristic I_D vs. V_G expose in atmosphere without stress.

Fig. 3.11 Measured transfer curves of a pentacene TFTs deposited on thermal oxide with DC bias stress of -40 V.

Fig. 3.12 Measured transfer curves of a pentacene TFTs deposited on thermal oxide with DC bias stress of 30 V.

Fig. 3.13 Threshold voltage shift vs. bias stress time for positive bias stress of +30 and +40 V, and negative bias stress of -10 and -30 V.

Fig. 3.14 Normalize film mobility of pentacene TFTs after DC bias stress.

- Fig. 3.15** The transfer characteristic I_D vs. V_G expose in atmosphere without stress.
- Fig. 3.16** Measured transfer curves of a pentacene TFTs deposited on HMDS surface treatment with DC bias stress of -40 V.
- Fig. 3.17** Measured transfer curves of a pentacene TFTs deposited on HMDS surface treatment with DC bias stress of 30 V.
- Fig. 3.18** Threshold voltage shift vs. bias stress time for positive bias stress of +30 and +40 V, and negative bias stress of -10 and -30 V.
- Fig. 3.19** Normalize film mobility of pentacene TFTs after DC bias stress.
- Fig. 3.20** The transfer characteristic I_D vs. V_G expose in atmosphere without stress.
- Fig. 3.21** Measured transfer curves of a pentacene TFTs deposited on ODMS surface treatment with DC bias stress of -40 V.
- Fig. 3.22** Measured transfer curves of a pentacene TFTs deposited on ODMS surface treatment with DC bias stress of 30 V.
- Fig. 3.23** Threshold voltage shift vs. bias stress time for positive bias stress of +30 and +40 V, and negative bias stress of -10 and -30 V.
- Fig. 3.24** Normalize film mobility of pentacene TFTs after DC bias stress.
- Fig. 3.25** Pulse voltage was applied to the gate electrode and source and drain were grounded.
- Fig. 3.26** The pulse swing region was separated into two parts; one was the ON region, and the other was the OFF region.
- Fig. 3.27** Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on thermal oxide during ON region AC bias-stress with a duty-cycle of

50% and frequency of (a) 5 Hz (b) 50Hz (c) 200Hz

Fig. 3.28 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different frequencies.

Fig. 3.29 Mobility variation versus effective stress time.

Fig. 3.30 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on thermal oxide during OFF region AC bias-stress with a duty-cycle of 50% and frequency of (a) 5 Hz (b) 50Hz (c) 200Hz.

Fig.3 .31 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different frequencies.

Fig. 3.32 Mobility variation versus effective stress time.

Fig. 3.33 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on thermal oxide during (a) ON region (b) OFF region AC bias-stress with a duty-cycle of 25% and frequency of 50Hz.

Fig. 3.34 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

Fig. 3.35 Mobility variation versus effective stress time.

Fig. 3.36 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

Fig. 3.37 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

Fig. 3.38 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different frequencies.

Fig. 3.39 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different duty-cycles.

- Fig. 3.40** Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on HMDS surface treatment during ON region AC bias-stress with a duty-cycle of 50% and frequency of (a) 50Hz (b) 200Hz.
- Fig. 3.41** Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different frequencies.
- Fig. 3.42** Mobility variation versus effective stress time induced by ON region AC bias-stress with different frequencies.
- Fig. 3.43** Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on HMDS surface treatment during OFF region AC bias-stress with a duty-cycle of 50% and frequency of (a) 50Hz (b) 200Hz.
- Fig. 3.44** Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different frequencies.
- Fig. 3.45** Mobility variation versus effective stress time induced by OFF region AC bias-stress with different frequencies.
- Fig. 3.46** Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on HMDS during (a) ON region (b) OFF region AC bias-stress with a duty-cycle of 25% and frequency of 50Hz.
- Fig. 3.47** Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different duty-cycles.
- Fig. 3.48** Mobility variation versus effective stress time induced by ON region AC bias-stress with different duty-cycles.
- Fig. 3.49** Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.
- Fig. 3.50** Mobility variation versus effective stress time induced by OFF region

AC bias-stress with different duty-cycles.

Fig. 3.51 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different frequencies.

Fig. 3.52 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different duty-cycles.

Fig. 3.53 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on ODMS surface treatment during ON region AC bias-stress with a duty-cycle of 50% and frequency of (a) 5Hz (b) 50Hz (c) 200Hz.

Fig. 3.54 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different frequencies.

Fig. 3.55 Mobility variation versus effective stress time induced by ON region AC bias-stress with different frequencies.

Fig. 3.56 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on ODMS surface treatment during OFF region AC bias-stress with a duty-cycle of 50% and frequency of (a) 5Hz (b) 50Hz (c) 200Hz.

Fig. 3.57 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different frequencies.

Fig. 3.58 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different frequencies.

Fig. 3.59 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on ODMS treatment during (a) ON region (b) OFF region AC bias-stress with a duty-cycle of 25% and frequency of 50Hz.

Fig. 3.60 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

Fig. 3.61 Mobility variation versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

Fig. 3.62 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

Fig. 3.63 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

Fig. 3.64 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different frequencies.

Fig. 3.65 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different duty-cycles.



Chapter 1

Introduction

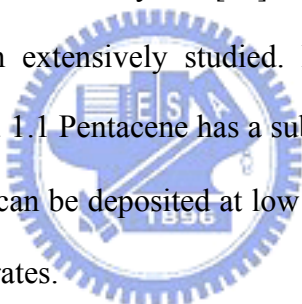
1-1 Overview of Organic TFT Technology

Organic semiconductors have been known since the late 1940s.[1] However, apart from a very small number of preliminary works on conjugated small molecules [2,3] and polymers[4], the first transistor based on an organic semiconductor was only reported in 1986,[5] with a device made on an electrochemically grown polythiophene film. Polythiophene belongs to the family of the conducting polymers that were discovered in the late 1970s.[6] The inventors of polyacetylene, an archetypal model of conducting polymers, were awarded the Nobel Prize in chemistry in 2000. The possibility of fabricating organic TFT (OTFT) with small conjugated molecules was shown in 1989[7] with sexithiophene, an oligomer of polythiophene made of six thiophene rings linked at alpha position (see Fig. 1.1). Interestingly enough, the organic TFT grew in parallel with another device, the organic light-emitting diode (OLED). As in the case of OTFTs, OLEDs can be made with small molecules[8] or polymers.[9] However, the development of OLEDs has been much faster than that of OTFTs, so that commercial products based on OLEDs are now available on the market, which is not yet the case for OTFTs. In spite of considerable improvements during the last years, the performance of OTFTs remains far beyond that of their inorganic counterpart, except for a-Si:H. For this reason, applications are envisioned where low fabrication costs and large area are of primary importance. These include electronic bar codes and identification tags, and, to a lesser extent, active matrix elements for organic flat panel displays. With this in mind, more and more industrial groups have recently initiated research programs in the field of organic transistors.

Until recently, much of the research effort has been directed at improving the charge-carrier mobility. Several papers have reviewed this search for better materials and device architecture[10-14].

1-2 Organic semiconducting materials

A number of organic materials such as polythiophene, α -sexithiophene (α -6T) have been investigated for use in field effect transistors (FETs) [15]. Polycrystalline molecular solids such as α -sexithiophene (α -6T) or amorphous/semi-crystalline polymers such as polythiophene or acenes such as pentacene, teracene show the highest mobility [16]. Figure 1.2 shows the evolution of organic materials and the improvement in their mobility over the years [17]. Pentacene based FETs show the high mobility and have been extensively studied. Pentacene is made up of five benzene rings as shown in Fig. 1.1 Pentacene has a sublimation temperature of 300 . Well ordered pentacene films can be deposited at low temperatures making it suitable for deposition on plastic substrates.



1-3 Operating mode of organic thin film transistor

A thin film transistor is composed of three basic elements: (i) a thin semiconductor film; (ii) an insulating layer; and (iii) three electrodes. Two of them, the source and the drain, are in contact with the semiconductor film at a short distance from one another. The third electrode, the gate, is separated from the semiconductor film by the insulating layer. Figure 1.3(a) and (b) illustrate a widely used configuration of these elements, but as will be shown in the following, there exist several alternative ways of arranging the elements of the device. The Fermi level of gold and HOMO-LUMO levels of pentacene are shown in Fig. 1.4 When a positive voltage is applied to the gate, negative charges are induced at the source electrode. As

can be seen in Fig. 3, the Fermi level of gold is far away from the LUMO level, so that electron injection is very unlikely. Accordingly, no current passes through the pentacene layer, and the small measured current essentially comes from leaks through the insulating layer. When the gate voltage is reversed, holes can be injected from the source to the semiconductor, because the Fermi level of gold is close to the HOMO level of pentacene. Accordingly, a conducting channel forms at the insulator-semiconductor interface, and charge can be driven from source to drain by applying a second voltage to the drain. For this reason, pentacene is said to be a *p*-type semiconductor. However, it should be pointed out that this concept differs from that of doping in conventional semiconductors, which can be made either *n*-type or *p*-type by introducing tiny amounts of an electron donating or electron withdrawing element. Symmetrically, an organic semiconductor will be said *n*-type when the source and drain electrodes can inject electrons in its LUMO level, provided electron transport does occur, i.e., electron mobility is not too low. Basically, the thin-film transistor operates like a capacitor. When a voltage is applied between source and gate, a charge is induced at the insulator-semiconductor interface. This charge forms a conducting channel (Fig. 1.5), the conductance of which is proportional to the gate voltage. At low drain voltages, the current increases linearly with drain voltage, following Ohm's law. When the drain voltage is compared to gate voltage, the voltage drop at drain contact falls to zero and the conducting channel is pinched off. This corresponds to the so-called saturation regime where the current becomes independent of the drain voltage. Below a given threshold, the current increases exponentially. This corresponds to the below-threshold regime. In the above threshold regime, the current becomes proportional to the gate bias, as expected from the above description of the operating mode of the transistor.

1-4 Contact resistance in Organic thin film transistors

Ongoing efforts to improve the performance of organic thin-film transistors focus on identifying the relationships between the device structure, film morphology, and charge transport properties. It has been shown that, depending on the device geometry, contact resistances at the source and drain terminals in organic TFTs can be a significant bottleneck to current flow. In the last years, work by a number of research groups has shown that the properties of the source and drain contacts in organic TFTs can have an important effect on the overall devices performance. Jackson, for example, has published a transmission line study of contact resistance in pentacene TFTs [18] showing significant differences in the contact properties for top versus bottom contact devices. In an earlier study, Dimitrakopoulos and co-workers demonstrated that for bottom contact TFTs there is a region of disorder in the pentacene thin film near the contact interface, though the disorder can be mitigated by thiolating the contacts.[19]

A powerful alternative to the transmission line method is to map the potential profile across operating OTFTs, as can be done using Kelvin probe force microscopy (KFM).[20–22] Sharp voltage drops, which are observed in the profiles, highlight the resistive bottlenecks to current flow. For example, large contact resistances lead to large voltage drops at the contact-semiconductor interfaces. Dividing the voltage drop by the current yields the contact resistance. Recently Nichols *et al.*[20] and Puntambekar *et al.*[21] have reported potential profiling of pentacene OTFTs by KFM. In addition, Burgi *et al.* have demonstrated potential mapping of polythiophene OTFTs as a function of temperature, which allows a better assessment of the carrier transport mechanisms at the contacts and in the film.[22]

Another contact resistance measurement OTFTs is using the gated four-probe technique, in which the channel potential is sensed at two points between the source and the drain. While this approach does not provide the exquisite detail of a full potential mapping by KFM, it is relatively easy to implement and allows variable-temperature resistance measurements without the need for a UHV-AFM. Four-terminal measurements on a-Si:H TFTs have been extensively reported,[23–26] and recent studies of field-effect transistors based on organic single crystals have also exploited four-probe geometries,[27–30] but so far there have been very few four-terminal measurements on OTFTs. Recently, Yagi et al. reported an initial study of four-terminal pentacene OTFTs.[31]

1-5 Surface treatment

The surface properties such as frictional or abrasion, permeability, insulating properties, wettability and chemical reactivity are strongly dependent on a molecular aggregation state of the surface [32,33]. Therefore, the control of a molecular aggregation state on the film is important to construct a highly functionalized surface. One of the most effective ways of studying surface properties is contact angle measurement. The contact angle is the angle between the tangent to the drop's profile and the tangent to the surface at the intersection of the vapor, the liquid, and the solid. The contact angle is an index of the wettability of the solid surface. A low contact angle between solid surface water-drop indicates that the surface is hydrophilic and has a high surface energy. On the contrary, a high contact angle means that the surface is hydrophobic and has a low surface energy. The surface free energy was traditionally quantified by contact angle measurements [34,35].

In this work, we fabricated the electrical properties of the OTFTs using

pentacene fabricated by thermal evaporation in high vacuum with the three kinds of dielectric surface treatments; as-prepared (wet cleaning only), hexamethyldisilane ((CH₃)₃-Si-O-Si-(CH₃)₃) (HMDS), and ODMS.

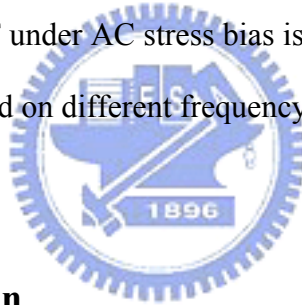
1-6 Reliability

The threshold voltage, and in particular its shift with prolonged application of gate bias stress, is an important parameter for the characterization of thin film transistors. It is well known that bias stress shifts the threshold voltage in both organic and inorganic TFTs [38-41]. The shift in threshold voltage for amorphous and polycrystalline silicon TFTs has been extensively investigated [39, 40]. Its effect can arise from low trapping in the dielectric and/or surface states at the semiconductor/dielectric interface, or the creation of defects in the semiconductor. Recently, bias stress effects have been reported for transistors based on pentacene, polythiophene vinylene [42-44], *α*-sexithiophene [45], poly-9,9-dioctyl-fluorene-cobithiophene and regioregular-polythiophene [45,46]. In an attempt to understand the physical origin of this instability and the exact location of the trapped charges, several authors have studied the effect using different dielectric materials [42,44] different types of SiO₂, and different surface dielectric treatments [45]. It is well established that ionic movements in thermally grown SiO₂ do not occur. Therefore, the data available in the literature suggest that stress in devices using thermally grown SiO₂ is related to the properties of the organic semiconductor itself. Recent work has also shown that the bias stress effect can be reversed by band gap light [45] confirming the view that the stress effect is due to trapped charges located within the semiconductor film, near the dielectric interface. Several authors have also reported that the threshold voltage shift is reversible, and that the recovery process can be enhanced by a positive gate bias [41, 47].

1-7 Motivation

The source/drain contact series resistances not only influence the electrical performance of OTFTs, but also make it difficult to optimize the channel material. To understand the intrinsic performance of OTFT, there is a need for a new structure and/or method which allows exclusion of the effect of source/drain series resistance.

OTFT is advantage to make low-cost circuit. But only a few papers were published in reliability field. In order to understand degradation of OTFT, we design three kinds of insulator surface. First, the instability mechanisms of OTFT under DC bias stress have been widely discussed. Because circuits are operated on different frequency, reliability of OTFT under AC stress bias is needed to study. OTFTs treated different methods are measured on different frequency and duty-cycle.



1-8 Thesis Organization

In Chapter 1, we describe the introduction of OTFTs and motivation of the thesis. In Chapter 2, the fabrication, structure and parameter extraction of OTFTs are presented. In Chapter 3, gated-four-probe analysis, DC and AC gate bias stress at OTFTs are investigated. Finally, we describe the conclusion in Chapter 4.

Chapter 2

Experiment

2-1 Overview of Organic TFT Structure

In this study, we fabricated top-contact and bottom-contact structures. The silica substrates consisted of 2000 Å of thermal oxide on *p*-doped (Boron) silicon wafers. As received, the wafers had an oxide on each side: one side polished and the other unpolished. Below the following sections, we would detail introduce the process of different structures.

2-1.1 Shadow mask process

Step1. Substrate and gate electrode

4-inch P-type heavily-doped single crystal silicon wafer (100) was used as the substrate and the gate electrode.

Step2. Gate oxide formation

After the initial RCA cleaning, the 2000Å thermally grown SiO₂ layer was deposited in furnace.



Step3. Pentacene film deposition through shadow mask

Pentacene, which was obtained from Aldrich Chemical Company without any purification, was used as an active layer. The deposition was started at a pressure lower than 3×10^{-6} torr. The deposition rate was controlled at 0.5Å/s. The temperature we used in depositing pentacene films is 70°C. We used shadow mask to define the active region of each device.

Step4. Au deposition for Top Contact

The step formed the Top-Contact in OTFT. We used shadow mask to define top contact of each device. The top electrodes were Au. Au was deposited on the active layer by ULVAC thermal coater at deposition pressure 3×10^{-6} torr. The thicknesses of

the metal layer were 500Å.

The figure 1.3 (a) show the configuration of structures.

2-1.2 Surface treatment

In order to obtain different surface of oxide layer, we used HMDS and ODMS to modify the surface.

HMDS treatment: Before deposited S/D metal or pentacene film, wafer was put into the oven with HMDS steam for 20mins at 150 degree celcius.

ODMS treatment: Before deposited S/D metal or pentacene film, wafer was dip in ODMS solution.

2-2 Gated four-probe measurements

2-2.1 Theory of gated four-probe measurements

The conventional equations describing a-Si:H TFT performance can be derived from the charge control model [37]. In this model the concentration of free carriers, n_{ss} , induced into the conducting channel is given by

$$n_{ss} = \frac{C_i [V_G - V_T - V_C(x)]}{q} \quad (1)$$

where C_i is the geometrical capacitance of the gate insulator; V_T is the applied gate bias; V_G is the effective threshold voltage; $V_C(x)$ is the channel potential; and q is the electronic charge. In this approximation, the dependence of the charge in the depletion layer on the surface channel potential has been neglected. Based on the gradual channel approximation, the drain current then can be expressed as

$$I_D = C_i \mu_{FE} \left(\frac{dV_C(x)}{dx} \right) [V_G - V_T - V_C(x)] W \quad (2)$$

where W is the channel width and μ_{FE} is the field-effect mobility. This equation can be rewritten as

$$dx = \left(\frac{C_i \mu_{FE} W}{I_D} \right) [V_G - V_T - V_C(x)] dV_C(x) \quad (3)$$

Integration of the above gives

$$\int_0^L dx = \left(\frac{C_i \mu_{FE} W}{I_D} \right) \int_0^{V_D} [V_G - V_T - V_C(x)] dV_C(x) \quad (4)$$

where L is the channel length and V_D is the drain voltage. The above equation leads to the following equation:

$$I_D = \mu_{FE} \left(\frac{W}{L} \right) C_i \left(V_G - V_T - \frac{V_D}{2} \right) V_D \quad \text{for } V_D \leq (V_G - V_T) \quad (5)$$

For small V_D , this equation can be simplified to

$$G = \mu_{FE} C_i (V_G - V_T) \quad (6)$$

where $G \left(= \frac{I_D L}{W V_D} \right)$ is the normalized channel conductance.

Equation (6) is traditionally used to extract the field-effect mobility and threshold voltage of a-Si:H TFT operating in a linear region. However, the above derivation does not include the effect of source/drain series resistances. In fact, the source/drain series resistances cannot be ignored in a real a-Si:H TFT. To exclude the voltage drops at source/drain series resistances, the range of integration for in (3) should start from $I_D R_S$ to $(V_D - I_D R_D)$, where R_S and R_D are series resistances at source and drain terminals, respectively.

By assuming $R_S = R_D$, the integration of (3) yields

$$I_D = \mu_{FE} \left(\frac{W}{L} \right) C_i \left(V_G - V_T - \frac{V_D}{2} \right) (V_D - 2I_D R_S) \quad (7)$$

This equation shows that the existence of series resistances make the I_D - V_G characteristics become nonlinear. If R_S is ohmic and is independent of V_G , I_D , and V_D , the intrinsic mobility, threshold voltage, and series resistances can be extracted by least square fit to (7). However, this ideal case is not representative for a-Si:H TFT. In

a-Si:H TFT, R_s is V_G , I_D , V_D , and source/drain-gate overlap dependent, which makes the extraction of the intrinsic mobility and threshold voltage from (7) difficult.

In order to extract intrinsic mobility and intrinsic threshold voltage of a-Si:H TFT, the measurement must exclude the effect of source/drain series resistances. For this reason, we have developed the new gated-four-probe a-Si:H TFT structure described in this letter.

Fig. 2.1 shows top view and cross section of this new gated-four-probe a-Si:H TFT structure. It is similar to conventional bottom-gate back-channel-etched a-Si:H TFT but two additional narrow metal electrodes (probe A and probe B) have been added between the source and drain contacts to probe the potential at $x = X_A$ and $x = X_B$, respectively. Integration of (3) from $x = X_A$ to X_B yields

$$(X_B - X_A) = \frac{C_i \mu_{FE} W}{I_D (V_B - V_A) \left[V_G - V_T - \frac{(V_B + V_A)}{2} \right]} \quad (8)$$

where V_A and V_B are the probed channel potential at $x = X_A$ and X_B , respectively. This equation can be rewritten as

$$I_D = C_i \mu_{FE} \left(\frac{W}{L'} \right) (V_{G'} - V_T) \Delta V \quad (9)$$

where $\Delta V = V_B - V_A$, $V_{G'} = V_G - \frac{(V_B + V_A)}{2}$, and $L' = (X_B - X_A)$ or

$$G' = C_i \mu_{FE} (V_{G'} - V_T) \quad (10)$$

where $G' \left(= \frac{I_D L'}{W \Delta V} \right)$ is the effective normalized channel conductance. Since probes A and B sense only the potential but not the current, and there is no current flow through these two probes, V_A and V_B will represent the true channel potential without being influenced by the source/drain series resistances. The width of probes A and B should be as narrow as possible to avoid influence of these probes on the electrical field

inside the conducting channel.

2-2.2 Gated four-probe structure

Figure 2.2(a) depicts the final bottom gate, inverted-staggered (top contact) TFT configuration with the in-channel probes used to measure the channel potential of the operating TFT. Fig. 2.2(b) show a schematic of the four-probe geometry used to determine film and contact resistance. The probes were typically 50 μm in width, and penetrate into the channel less than 150 μm . The sense probes make up less than 10% of the channel length and penetrate less than 10% of the channel width. The sense probes float at a voltage (V_1, V_2) corresponding to the channel voltage at the position, thus, the voltage drop at the source and drain electrodes can be determined by extrapolating the channel voltage gradient back to the source and drain. Fig. 2.2(c) illustrates how the channel probe contacts were aligned with the edge of the masked pentacene film. Here, the potential probes only contact the film directly in and near the channel area.

2-2.3 Current-voltage characterization

Electrical characterization was carried out by sweeping the drain voltage (V_D) at a constant gate voltage (V_G) or sweeping V_G at a constant V_D while monitoring the drain current (I_D) and probe potentials (V_1, V_2). HP 4156 source-measure units were used to apply V_D and to measure the source (I_S) and drain currents. HP 4156 high-impedance ($> 10^{14}$) electrometers were used to monitor V_1 and V_2 via channel probes and to source V_G . All leads except the gate used guarded-shielded triaxial cables instead of shielded coaxial cables to minimize electrical noise and leakage currents. A computer connected to all instrumentation via a general purpose

interface bus running ICS was used to control the operation of all units. The data were exported to and analyzed in ICS. Typical I_D-V_G parameters used are as follows: for SiO_2 dielectric, $V_D = -3 \text{ V}$, -6 V and -9 V , $V_G = +20 \sim -70 \text{ V}$, voltage step = 1 V , and $C_{\text{OX}} = 10 \text{ nF/cm}^2$.

2-2.4 Potential measurements

During the standard three-terminal current-voltage measurements, the channel potential was monitored in situ at two points in the channel via the potential probes. At a constant V_D , V_G was swept and the channel potential was measured at each V_G step. Knowing the channel potential at two points, V_1 and V_2 , a linear extrapolation of the potential profile to each contact was performed. From the difference between the applied potential at each contact and the extrapolated potential values for the contacts, the potential drops at the source and drain, ΔV_S and ΔV_D , were calculated according to the following equations:

$$\Delta V_S = \left[V_1 - \frac{(V_2 - V_1)}{(L_2 - L_1)} L_1 \right] - V_S,$$

$$\Delta V_D = V_D - \left[V_2 + \frac{(V_2 - V_1)}{(L_2 - L_1)} (L - L_2) \right]$$

where V_S , V_D , V_1 , and V_2 are the voltages at the source/drain, and potential probes, respectively. L_1 , L_2 , and L are the distances from the source electrode to the first potential probe, the second potential probe, and the drain electrode, respectively. Since we are also interested in examining the potential drop across the film, we define

$$\Delta V_{\text{Film}} = \frac{(V_2 - V_1)}{(L_2 - L_1)} L$$

where ΔV_{Film} is the actual drain bias across the film (i.e., the applied drain bias less the drops at the contacts).

2-3 Reliability

2-3.1 Configuration of Measurement Equipments

The measurements used in this study consist of HP 4156A precise semiconductor parameter analyzer, HP41501B pulse generator and HP 16440A SMU/PGU selector. The HP41501B is used to generate the AC pulse signal, including pulse amplitude, frequency, and duty ratio to stress Organic TFTs. After AC signal stress, the OTFT is measured by HP4156A to extract the electrical parameter, including threshold voltage, subthreshold swing, and mobility. Fig. 2.3 illustrates the diagram of the bias stress measurement equipment.

2-3.2 Waveform of the AC Signal

The AC signal used in this study consists of signal amplitudes, frequencies, and duty ratios. We can adjust these parameters and then perform various stress conditions on the gate electrode to realize the instability of Pentacene-based TFTs under different swing regions. Fig. 2-4 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is give as follow:

$$t_c = t_{vp} + t_f + t_{vb} + t_r \quad (11)$$

$$f = \frac{1}{t_c} \quad (12)$$

$$D.R. = \frac{(t_{vp} + t_r)}{t_c} \quad (13)$$

Where t_c is the signal period, f is the signal frequency and D.R. is the duty ratio.

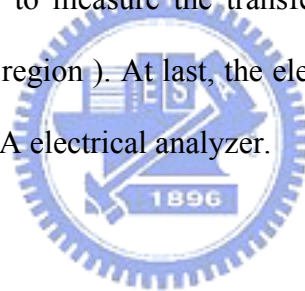
In the waveform of AC signal, V_P is the defined as the peak voltage, while V_b is defined as the base voltage. The frequency (f) is equal to $1/t_c$, where the t_c is the signal

period and the duty ratio is defined a eq. (13). The t_{vp} is the time of peak voltage and the t_{vb} is the time of base voltage. The t_f is the falling time. The t_r is the rising time. The sum of t_{vp} , t_{vb} , t_f , t_r is equal to t_c .

2-3.3 Measurement Methods

HP 4156A precise semiconductor parameter analyzer was used to perform the stress measurement on the OTFTs and extract the transfer characteristic after DC bias stress. Besides, combining the HP41501B pulse generator with HP 4156A precise semiconductor parameter analyzer, the stress measurement were performed on the TFTs and the transfer characteristics were extracted after AC bias stress.

Both of the DC and AC bias stress measurement were performed up to 1000s and interrupted at a specific time to measure the transfer curves at the drain-to-source voltage (V_{ds}) of 6V (in linear region). At last, the electrical characteristics of OTFTs were extracted by an HP 4156A electrical analyzer.



Chapter 3

Analysis and Result

3-1 Gated four-probe analysis

3-1.1 Current-Voltage characterization

We fabricated three differential oxide interfaces of organic thin film transistors. The standard devices were only cleaned by RCA clean. The other devices were treated by HMDS and ODMS. For most devices, transfer curves were taken in 1 V gate steps from -20 V up to +70 V. Figure 3.1 (a), (b) and (c) show that transfer curves of devices with different surface treatments. The curves obtained for all other OTFTs which had same oxide interface were similar to that observed for this device and were not shown. For different surface treatments, the threshold voltages of devices were different. The threshold voltage of devices with surface treatment were shift to more negative. Because the different surface treatments make oxide interface to have different surface state, like surface energy, roughness and trap density of states. Therefore, we used gated-four-probe structure to extract the mobility of devices and to map the potential in the channel.

3-1.2 Potential measurements

Figures 3.2(a), 3.2(b) and 3.2(c) represent plots of measured channel potentials V_1 and V_2 and calculated ΔV_S and ΔV_D as a function of V_G for standard, HMDS and ODMS surface treatment devices. Here, the potential data are truncated just after V_{on} , where the device initially begins to conduct. Before this point, the voltage probes measure potentials that are outside the range of the applied source or drain biases. We believe that these results from static charge buildup on the pentacene film surface and in the cables of the measurement system while the film is relatively nonconductive.

As soon as an appreciably conducting channel is established, the probes report potentials characteristic of the channel. Data on standard, HMDS and ODMS show the same trends. In chapter 2-4-2, we had explained how extract the potential drops at the source and drain, ΔV_S and ΔV_D . The potential drops at the source and drain, ΔV_S and ΔV_D , were calculated according to the following equations:

$$\Delta V_S = \left[V_1 - \frac{(V_2 - V_1)}{(L_2 - L_1)} L_1 \right] - V_S ,$$

$$\Delta V_D = V_D - \left[V_2 + \frac{(V_2 - V_1)}{(L_2 - L_1)} (L - L_2) \right]$$

Figure 3.3 (a), (b) and (c) show that the potential drops at the source, ΔV_S with different surface treatment. In above figures, we found that source side voltage drop turns from positive value to negative value. Figure 3.4 (a), (b) and (c) show that the potential drops at the drain, ΔV_D with different surface treatments. The Figure 3.5 (a), (b) and (c) show that the potential maps of channel from $V_G = V_{ON}$ to $V_G = -70V$. The corresponding energy band was depicted in Fig. 3.4. In Fig. 3.5(a), hole injected from source electrode face a barrier due to the difference of metal work function and the pentacene HOMO band. When gate bias is applied as in Fig. 3.5(b), the injection barrier is reduced and even removed when ΔV_S becomes negative. In addition to standard devices, devices with HMDS and ODMS treatment had same behavior.

3-1.3 Contact resistance

With the knowledge of the total current flowing through the device and the potential drops across the film and contacts, the resistance of the source contact, drain contact, and the film can be calculated using Ohm's Law, $R_i = \Delta V_i / I_D$, where i is S , D , and Film. Therefore we can obtain ΔR_S , ΔR_D and R_{Film} by

$$R_{Film} = \frac{(V_2 - V_1)}{I_D (L_2 - L_1)} L$$

$$R_S = \frac{\left[V_I - \frac{(V_2 - V_I)}{(L_2 - L_I)} L_I \right] - V_S}{I_D},$$

$$R_D = \frac{V_D - \left[V_2 + \frac{(V_2 - V_I)}{(L_2 - L_I)} (L - L_2) \right]}{I_D}$$

Figures 3.6(a) 3.6(b) and 3.6(c) for Standard, HMDS and ODMS top-contacted devices, respectively, show plots of resistance as a function of gate voltage. Initially, at low V_G , the film resistances (R_{Film}) and contact resistances (R_D and R_S) all begin at large values of resistance with R_D much larger than R_S . As V_G is increased, the resistance of both the film and contacts decrease rapidly and finally saturate. Note that the data at low V_G (less than V_T) could be misleading because when $|V_G - V_T| < |V_D|$, the device is in saturation and pinch off occurs. The depletion region associated with pinch-off introduces a high-resistance region near the drain electrode, and the potential profile across the film is not linear. The gated-four-probe technique presented here does not decouple the resistance due to the saturation-induced depletion region from the contact resistance.

3-1.4 Film Resistance Analysis

The figures 3.7 show that the dependence of the normalized film resistance on channel length at $V_G = -60$ V with $V_D = -6$ V. Obviously film resistance changed with channel length increasing. When devices were operated in linear region, the drain current I_D can be written as

$$I_D = \frac{W}{L} \mu_{FE} C_{ox} (V_G - V_T) V_D$$

Therefore the film resistance can be induced as

$$R_{Film} = \frac{L}{W \mu_{FE} C_{ox} (V_G - V_T)}$$

Above equation was induced by $J = \sigma E = qvn = q\mu nE$ (current drift equation) .

In figure 3.8 (a) (b) and (c), we found that R_{Film} depend on $\frac{I}{(V_G - V_T)}$. According to current drift equation, we can demonstrate the drift mechanism which was suitable for organic thin film transistor.

3-1.5 Mobility Analysis

In general, extracted mobility of devices which were fabricated simultaneously has different value at different channel length and drain bias. For the gated-four-probe measurement, the mobility μ_{FE} had been extracted using the equations:

$$G_M = \frac{W}{L_{12}} C_{ox} \mu_{FE} (V_1 - V_2)$$

$$\mu_{FE} = \frac{G_M \times L_{12}}{WC_{ox}(V_1 - V_2)}$$



Where the G_M is the channel conductivity, C_{ox} is the gate insulator capacitance per unit area, and V_1 and V_2 are the potentials measured by the voltage probing electrodes. L_{12} is the length of distance between two probes.

And the μ_0 is extracted by a general method from linear region. Figure 3.9 (a) and (b) show that mobility which was extracted by gated-four-probe method was not depend on channel length variation. The mobility was not affected by parasitic resistance. Therefore gated-four-probe method was convenient to monitor the variation of pentacene film.

3-2 DC reliability analysis

One of the most important stability issues in organic transistors is the shift in the threshold voltage upon applying a bias to the gate electrode, so-called stressing. The shift in threshold voltage induced by gate bias stress has been well studies in

amorphous silicon [48], and has recently been studied in pentacene-based TFTs [49]. Gate bias stress in amorphous silicon TFTs is ascribed to several mechanisms including: charge trapping in the insulator, surface state creation at the semiconductor/insulator interface, or creation of metastable traps within the semiconductor [50]. Gate bias stress in OTFTs has been studied very little.

In this study, we fabricated three kinds of interface of pentacene-based devices. These devices were treated by HMDS or ODMS. On the other hand, we also fabricated standard devices which were clean only RCA clean. Three kinds of devices were given different bias stress to observe the difference after stress. The experiment was divided into two parts. One was DC (direct current) stress, and the other was the AC (alternating current) stress.

3-2.1 DC bias stress analysis

Under DC stress, the gate bias stress measurements were performed in atmosphere and darkness on Pentacene-based TFTs on SiO₂ substrates with Au contacts. The stress gate voltage were -40V, -60V (negative bias stress), 30V, and 40V (positive bias stress), respectively. Between transfer curves, the device was stressed for a time interval (t) at a fixed gate voltage ($V_{G,Bias}$) with a drain voltage of $V_D = 0 V$. HP 4156A precise semiconductor parameter analyzer was used to perform the stress measurement on the transfer characteristics after DC stress. Typically, transfer curves were taken from, $V_G = +20$ to $-70 V$ at $1V$ steps. Between transfer curves, the device was stressed for a time interval (t) at a fixed gate voltage ($V_{G,Bias}$) with a drain voltage of $V_D = 0 V$

3-2.2 Influence of bias stress on thermal Oxide insulator

Pentacene-based TFT

First, we measured the electric characteristics of OTFTs without any stress in the atmosphere as the control sample. The transfer characteristic I_D vs. V_G was illustrated in Fig. 3.10. We can find the threshold voltage was not shift with time increase.

Fig. 3.11 show a series of transfer curves at $t = 0, 10, 100, 500$ and 1000 sec , between which $V_{G, Bias} = -40 \text{ V}$ (negative bias stress). The arrow in Fig.3.11 indicates the increase of stress time from 0 to 10, 100, 500, and 1000 sec , respectively, and these cause a shift in threshold voltage of about -2V . Fig. 3.12 show a series of transfer curves at $t = 0, 10, 100, 500$ and 1000 sec , between which $V_{G, Bias} = +30 \text{ V}$ (positive bias stress), respectively. The same, in Fig. 3.12., the arrow indicates the increase of stress time and these cause a shift in threshold voltage of about 9V .

Fig. 3.13 plots the shift of the threshold voltage for different stress times, and includes data for negative gate bias stress and positive gate bias stress at different stress levels. Positive bias stress moves the threshold voltage towards positive voltages, whereas for negative stress the threshold voltage shift towards negative threshold voltage. The threshold voltage increase over time but with a nonlinear dependence, and the shift increases with a nonlinear dependence, and the shift increase with stress bias. There is more pronounced shift of threshold voltage for positive gate voltages, but the form of the data for negative bias is otherwise rather similar.

Fig. 3.14 shows the normalize film mobility which extracts from gated-four-probe measurement. The film mobility of pentacene-based TFTs after DC bias stress was not change conspicuously. Negative gate bias stress cause a negative threshold shift and positive gate bias stress cause a positive threshold shift, while the

mobility remain unchanged. This effect was assigned to trapping of charges at the interface to the insulator, or in the insulator itself. In our device, Electron trapping is more pronounced than hole trapping. Similar result were previously obtained on amorphous silicon thin-film transistors and attributed to charge injection into the SiO₂ insulator [51].

3-2.3 Influence of bias stress on HMDS surface treatment

The same, we measured the electric characteristics of OTFTs without any stress in the atmosphere as the control sample. The transfer characteristic I_D vs. V_G was illustrated in Fig. 3.15.

Fig. 3.16 shows a series of transfer curves at $t = 0, 10, 100, 500$ and 1000 sec , between which $V_{G, Bias} = -40 \text{ V}$ (negative bias stress). The arrow in Fig.3.16 indicates the increase of stress time from 0 to 10, 100, 500, and 1000 sec , respectively, and these cause a shift in threshold voltage of about -8V. Fig. 3.17 shows a series of transfer curves at $t = 0, 10, 100, 500$ and 1000 sec , between which $V_{G, Bias} = +30 \text{ V}$ (positive bias stress), and these cause a shift in threshold voltage of about 12V.

Fig. 3.18 plots the shift of the threshold voltage for different stress times, and includes data for negative gate bias stress and positive gate bias stress at different stress levels. Fig. 3.19 shows the normalize film mobility which extracts from gated-four-probe measurement. The film mobility of pentacene-based TFTs after DC bias stress was not change conspicuously. Reliability issues lie in the HMDS layer degradation. HMDS may enhance the degradation since HMDS is more capable of trapping carriers than SiO₂.

3-2.4 Influence of bias stress on ODMS surface treatment

We measured the electric characteristics of OTFTs without any stress in the atmosphere as the control sample. The transfer characteristic I_D vs. V_G was illustrated in Fig. 3.20.

Fig. 3.21 and Fig. 3.22 show a series of transfer curves at $t = 0, 10, 100, 500$ and 1000 sec, between which $V_{G, Bias} = -40$ V (negative bias stress), $+30$ V (positive bias stress), respectively. The arrow in Fig. 3.21 and Fig. 3.22 indicates the increase of stress time from 0 to 10, 100, 500, and 1000 sec, respectively.

Fig. 3.23 plots the shift of the threshold voltage for different stress times, and includes data for negative gate bias stress and positive gate bias stress at different stress levels. Positive bias stress moves the threshold voltage towards positive voltages, whereas for negative stress the threshold voltage shift towards negative threshold voltage. Fig. 3.24 shows the normalized film mobility which extracts from gated-four-probe measurement. The film mobility of pentacene-based TFTs after DC bias stress was not change conspicuously. Reliability issues lie in the ODMS layer degradation.

3-3 AC reliability analysis

Under AC stress, pulse voltage was applied to the gate electrode and source and drain were grounded, which is shown in Fig. 3.25. A rectangular pulse was used with various frequencies and duty cycles to observe the devices degradation under different operating regions. The signal frequencies ranged from 5Hz to 200Hz, and the duty-cycle ranged from 50% to 25%. The pulse swing region was separated into two parts; one was the ON region, and the other was the OFF region as shown in Fig. 3.26. The ON region means pulse swing over threshold voltage where the channel region was

formed. The OFF region means pulse swing under threshold voltage where the channel region was fully depleted. At last, the electrical characteristics of OTFTs were extracted by an HP 4156A electrical analyzer. The field effect mobility is extracted from gated-four-probe measurement. The V_{th} shift is defined as the difference between V_{th2} and V_{th1} , where V_{th1} is the threshold voltage before stress and V_{th2} is the threshold voltage after stress.

3-3.1 Without Surface Treatment

3-3.1.1 Frequency dependence

In order to observe degradation of the device at the ON region stress and the OFF region stress, various frequencies range from 5Hz to 200Hz were applied at a fixed $t_r = t_f = 100\text{ns}$ and D.R = 50%. Fig. 3.27 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 *sec*, between which V_G (AC bias) = -40 V was applied at various frequencies. Fig 3.28 shows the threshold voltage shift versus effective stress time under ON region AC bias-stress for different frequency conditions. The effective stress time is the accumulated time when gate voltage is high. For the ON region bias-stress, AC and DC bias-stress induce a similar evolution of I_D - V_G characteristic and the threshold voltage shift dose not depends apparently on AC bias frequency. The mobility variation under the ON region at various frequencies was shown in Fig.3.29. The mobility variation is expressed as the ratio of stressed mobility (μ_{stress}) to initial mobility ($\mu_{initial}$). Fig 3.29 indicates the mobility was not changed under ON region stress. Fig. 3.30 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 *sec*, between which V_G (AC bias) = 30 V was applied at various frequencies. Fig 3.31 shows the threshold voltage shift versus effective stress time under OFF region AC bias-stress for different frequency conditions. For the OFF region AC bias-stress, threshold voltage shift is slightly smaller than that for DC bias-stress and depends

weekly on AC bias frequency. The mobility variation under the OFF region at various frequencies was shown in Fig. 3.32. Like the ON region AC bias stress, the mobility is almost constant under OFF region AC bias-stress.

3-3.1.2 Duty-cycle Dependence

Fig. 3.33 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 *sec*, between which V_G (AC bias) = -40 V and +30 V were applied at duty-cycle of 25%, respectively. Fig 3.34 shows the threshold voltage shift versus effective stress time under ON region AC bias-stress for different duty-cycles conditions. Fig. 3.35 shows the mobility variation under the ON region AC bias stress at various duty-cycles. Fig 3.36 shows the threshold voltage shift versus effective stress time under OFF region AC bias-stress for different duty-cycles conditions. Fig. 3.37 shows the mobility variation under the OFF region AC bias stress at various duty-cycles. Fig. 3.38 gives a summary of NO region and OFF region AC bias stress measurements at different frequencies. Fig. 3.39 shows the threshold voltage shift versus effective stress time under both ON region and OFF region AC bias stress for different duty-cycle conditions.

It was reported previously that detrapping during pulsed operation can explain the smaller threshold voltage shift induced by DC bias stress. The detrapping mechanism can be applied to OTFTs if the electrical instability mechanism is mainly associated with the charge-trapping in the gate insulator. During the OFF-cycle of the AC bias-stress, some of the trapped charge which is not deeply trapped could be relaxed from the trap centers.

3-3.2 HMDS Surface Treatment

3-3.2.1 Frequency dependence

Fig. 3.40 shows the evolution of I_D - V_G characteristic of HMDS surface treatment pentacene-based TFTs during ON region AC bias stress with a duty-cycle of 50% at various frequencies. The arrow in Fig. 3.40 indicates the increase of stress time from 0 (unstressed) to 100, 500, 1000 sec, respectively. Fig 3.41 shows the threshold voltage shift versus effective stress time under ON region AC bias-stress for different frequency conditions. For the ON region AC bias-stress, the threshold voltage shift has strong frequency dependence, the greater the magnitude of threshold voltage shift. The mobility variation under the ON region at various frequencies was shown in Fig. 3.42. Fig 3.42 indicates the mobility was almost constant under ON region stress. Fig. 3.43 show the evolution of I_D - V_G characteristic of HMDS surface treatment pentacene-based TFTs during OFF region AC bias stress with a duty-cycle of 50% at various frequencies. The arrow in Fig. 3.43 indicates the increase of stress time from 0 (unstressed) to 100, 500, 1000 sec, respectively. Fig 3.44 shows the threshold voltage shift versus effective stress time under OFF region AC bias-stress for different frequency conditions. The mobility variation under the OFF region at various frequencies was shown in Fig. 3.45. Like the ON region AC bias-stress, the threshold voltage shift also has strong frequency dependence and the mobility was not changed at different frequency condition.

3-3.2.2 Duty-cycle Dependence

Fig. 3.46 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 sec, between which V_G (AC bias) = -40 V and +30 V were applied at duty-cycle of 25%, respectively. Fig 3.47 shows the threshold voltage shift versus effective stress time under ON region AC bias-stress for different duty-cycles conditions. Fig. 3.48 shows

the mobility variation under the ON region AC bias stress at various duty-cycles. Fig 3.49 shows the threshold voltage shift versus effective stress time under OFF region AC bias-stress for different duty-cycles conditions. Fig. 3.50 shows the mobility variation under the OFF region AC bias stress at various duty-cycles.

Fig. 3.51 gives a summary of NO region and OFF region AC bias stress measurements at different frequencies. Fig. 3.52 shows the threshold voltage shift versus effective stress time under both ON region and OFF region AC bias stress for different duty-cycle conditions.

3-3.3 ODMS Surface Treatment

3-3.3.1 Frequency dependence

Fig. 3.53 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 sec, between which V_G (AC bias) = -40 V was applied at various frequencies. Fig 3.54 shows the threshold voltage shift versus effective stress time under ON region AC bias-stress for different frequency conditions. For the NO region bias-stress, AC and DC bias-stress induce a similar evolution of I_D - V_G characteristic and the threshold voltage shift dose not depends apparently on AC bias frequency. The mobility variation under the ON region at various frequencies was shown in Fig. 3.55. Fig 3.55 indicates the mobility is almost constant under ON region stress. Fig. 3.56 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 sec, between which V_G (AC bias) = 30 V was applied at various frequencies. Fig 3.57 shows the threshold voltage shift versus effective stress time under OFF region AC bias-stress for different frequency conditions. The mobility variation under the OFF region at various frequencies was shown in Fig. 3.58. Like the ON region AC bias stress, the mobility is almost constant under OFF region AC bias-stress.

3-3.3.2 Duty-cycle Dependence

Fig. 3.59 shows a series of transfer curves (I_D - V_G) at 0, 100, 500, 1000 sec, between which V_G (AC bias) = -40 V and +30 were applied at duty-cycle of 25%, respectively. Fig 3.60 shows the threshold voltage shift versus effective stress time under ON region AC bias-stress for different duty-cycles conditions. Fig. 3.61 shows the mobility variation under the ON region AC bias stress at various duty-cycles. Fig 3.62 shows the threshold voltage shift versus effective stress time under OFF region AC bias-stress for different duty-cycles conditions. Fig. 3.63 shows the mobility variation under the OFF region AC bias stress at various duty-cycles. Fig. 3.64 gives a summary of NO region and OFF region AC bias stress measurements at different frequencies. Fig. 3.65 shows the threshold voltage shift versus effective stress time under both ON region and OFF region AC bias stress for different duty-cycle conditions.



Chapter 4

Conclusion

4-1 Gated-Four-Probe measurement

In this study, we successfully fabricate gated-four-probe structure to extract parameters of organic thin film transistor. Analyses of devices with different surface treatments show the variation of voltage drop at source/drain. Although devices have three kinds of surfaces, different surfaces do not affect the voltage drop at source/drain. From Fig. 3.5, we understand that the injection barrier is reduced and even removed when V_G is large enough. In section 3-1.4, we found that R_{Film} which was extracted by gated-four-probe depends on $\frac{I}{(V_G - V_T)}$.

4-2 Reliability of organic thin film transistor

We used gated-four-probe structure to monitor variation of devices with different surface treatments during stress. First, devices were operated under DC stress. The standard devices which were stressed under negative voltage have smaller value of V_{th} shift than under positive voltage. The devices with surface treatment show that HMDS and ODMS may enhance the degradation since HMDS and ODMS are more capable of trapping carriers than SiO_2 . Subsequently, devices were operated under AC stress. The V_{th} shift values of standard devices which are stressed by positive voltage are obviously decreased. But devices with HMDS treatment strongly depend on frequency and duty-cycle, the V_{th} shift of devices is still larger than standard ones. Although the V_{th} shift of devices with ODMS treatment are still larger than standard ones, the shift values weakly depend on frequency and duty-cycle. All data of devices were measured by gated-four-probe structure, variation of devices were monitored. The extracted parameters of devices show that pentacene film is not degraded. Therefore, the V_{th} shift of devices may be come from variation of SAM

layer. The different results of devices with different surface treatment may be due to that chain length or polarization of SAM materials. Polarized SAM can selectively trap charges. For polarized SAM, opposite electric field is needed to release the trap charges.



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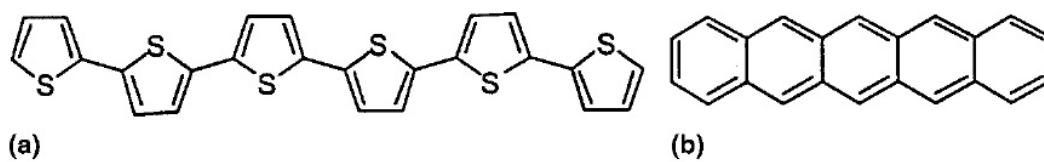


Fig. 1.1 Molecular structure of (a) sexithiophene and (b) pentacene.

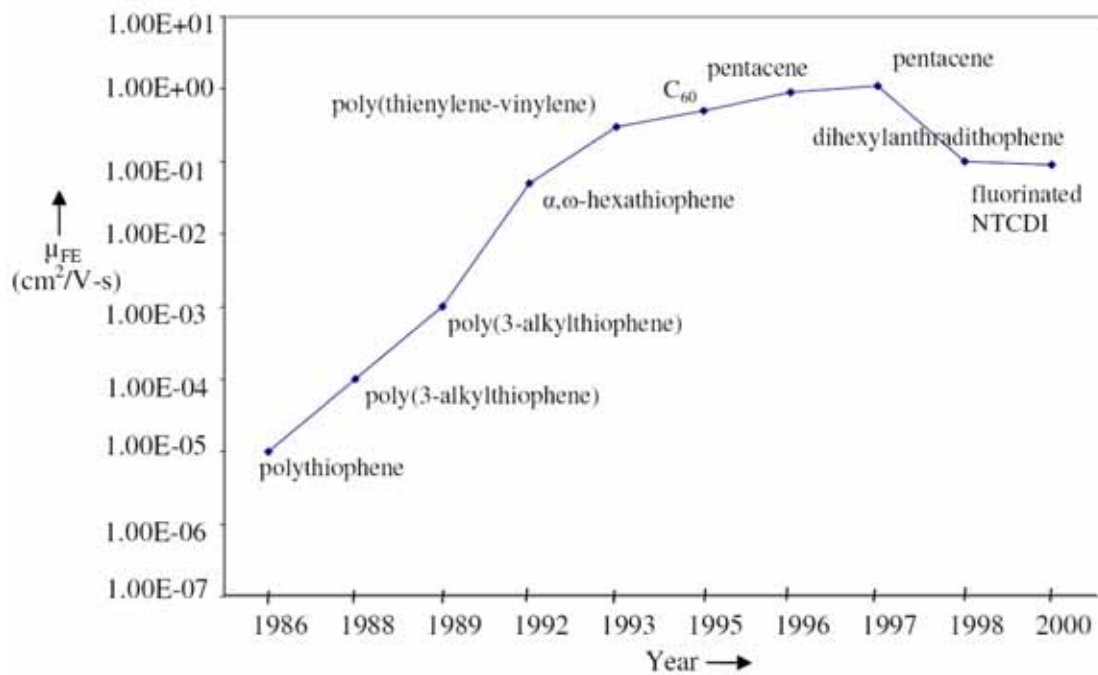


Fig. 1.2 Semilogarithmic plot of mobility vs. year.

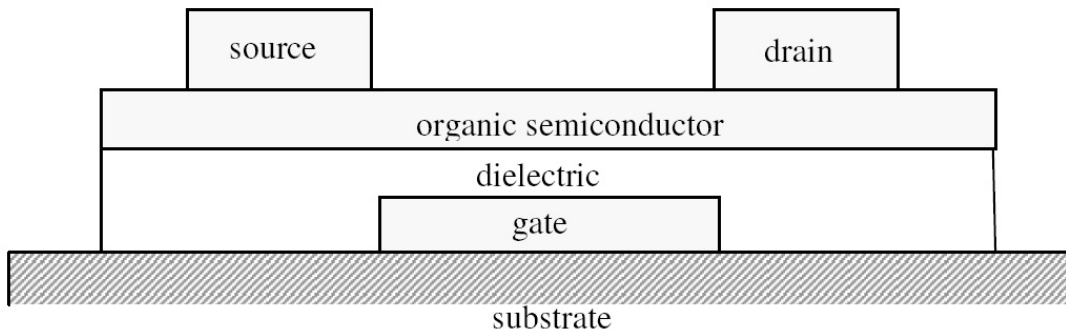


Fig. 1.3 (a) Top contact structure.

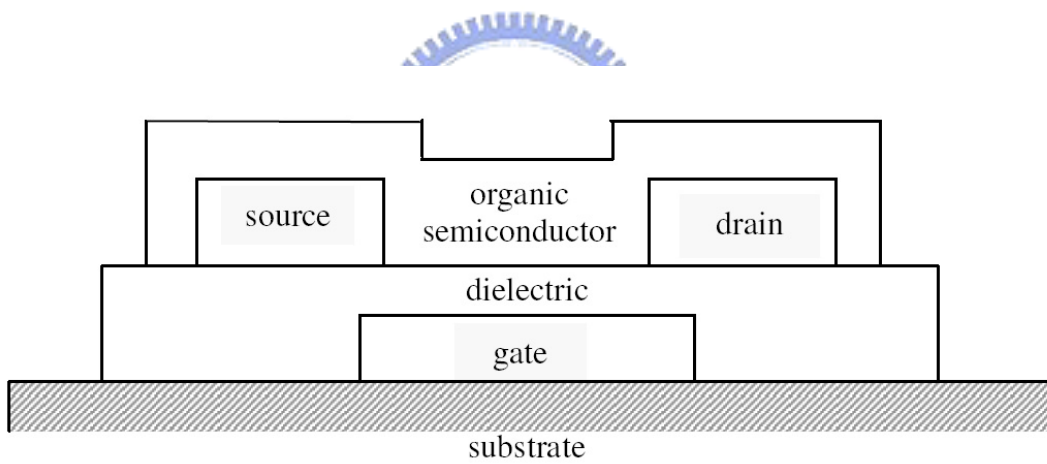


Fig. 1.3 (b) Bottom contact structure.

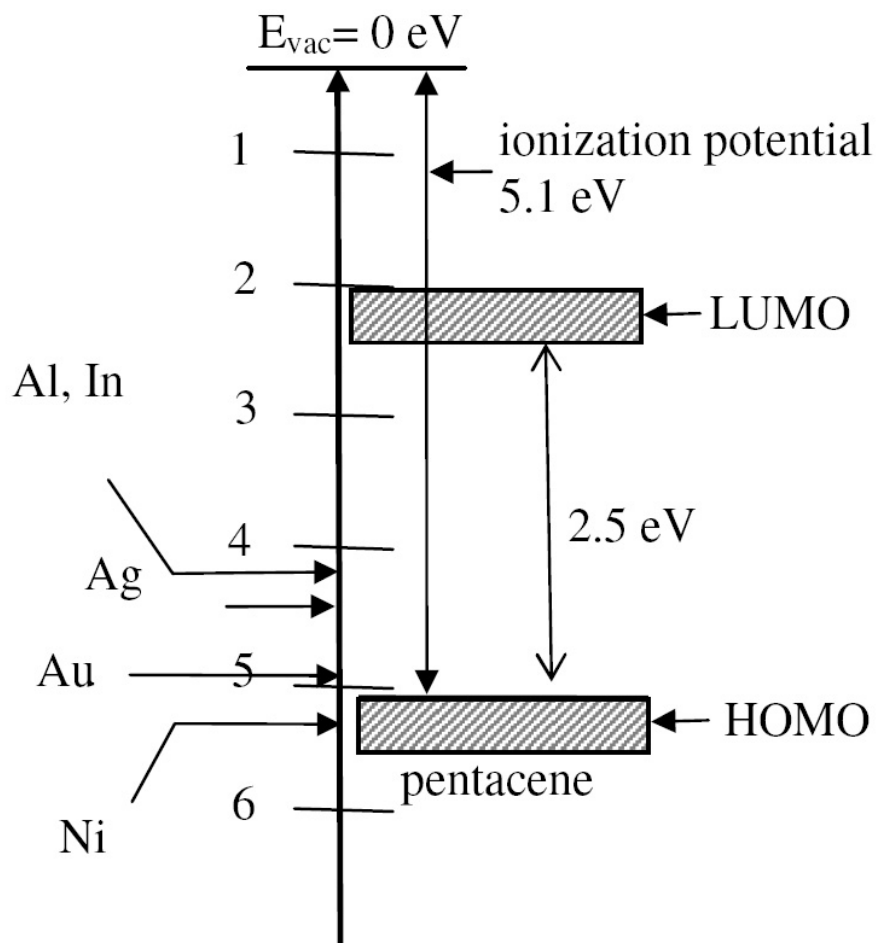


Fig. 1.4 Work function of various metals and ionization potential of pentacene.

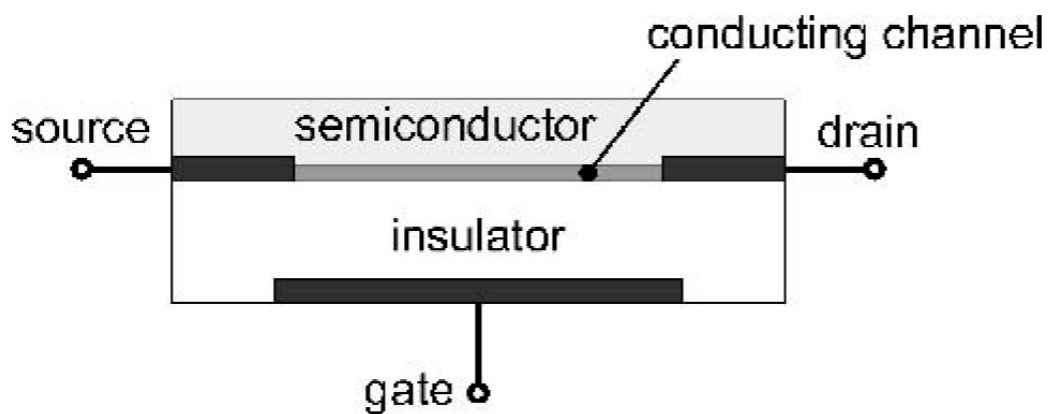


Fig. 1.5 Schematic view of a bottom-gate thin-film transistor.

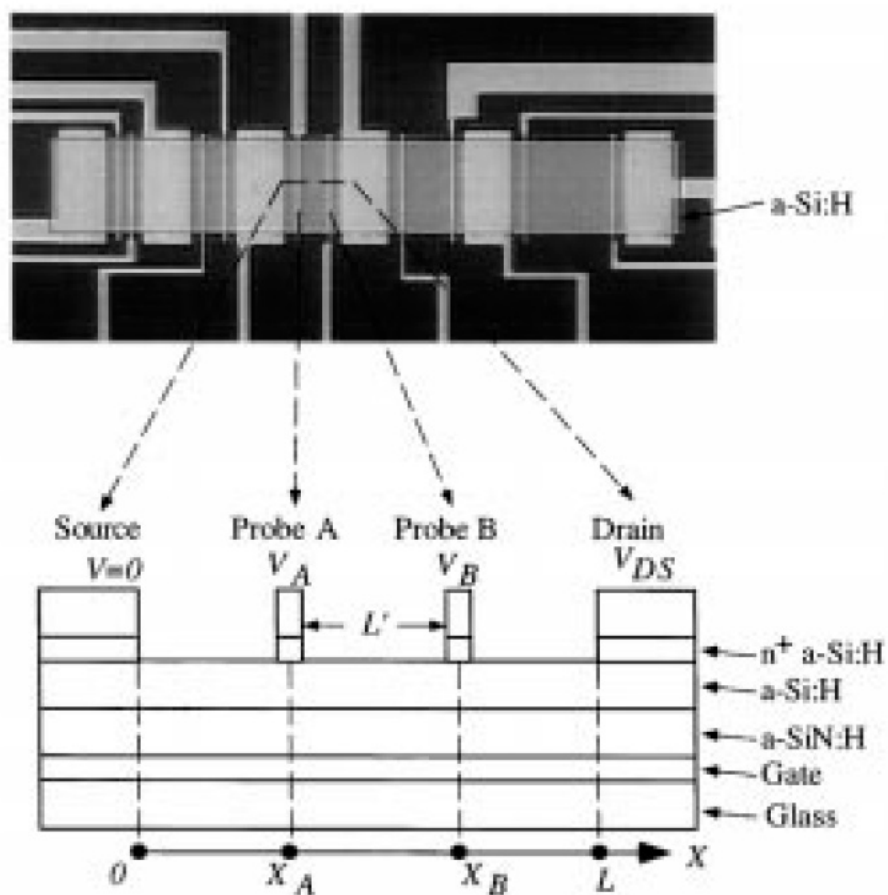
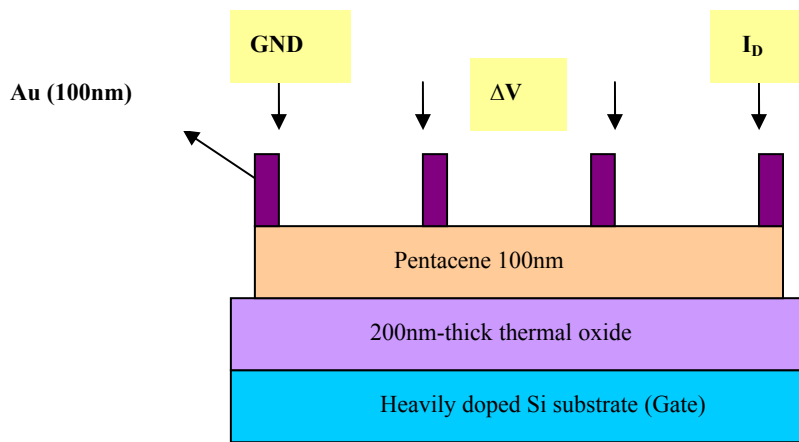
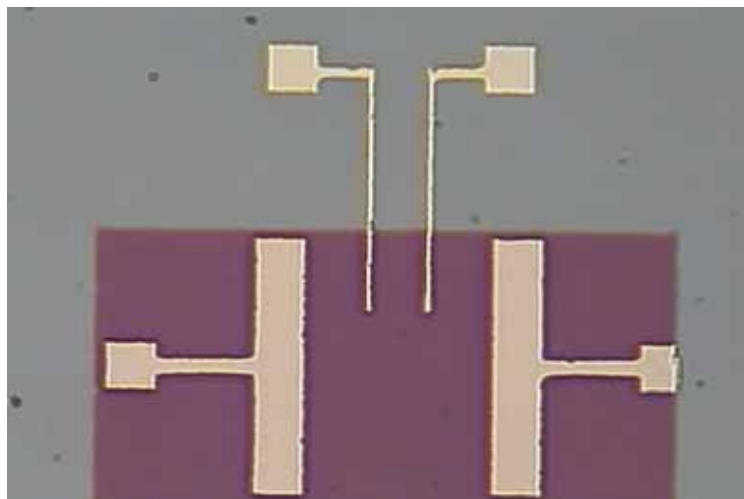


Fig. 2.1 Top view and cross section of the gated-four-probe a-Si:H TFT structure.



(a)



(b)

Fig. 2.2 show a schematic of the four-probe geometry used to determine film and contact resistance.

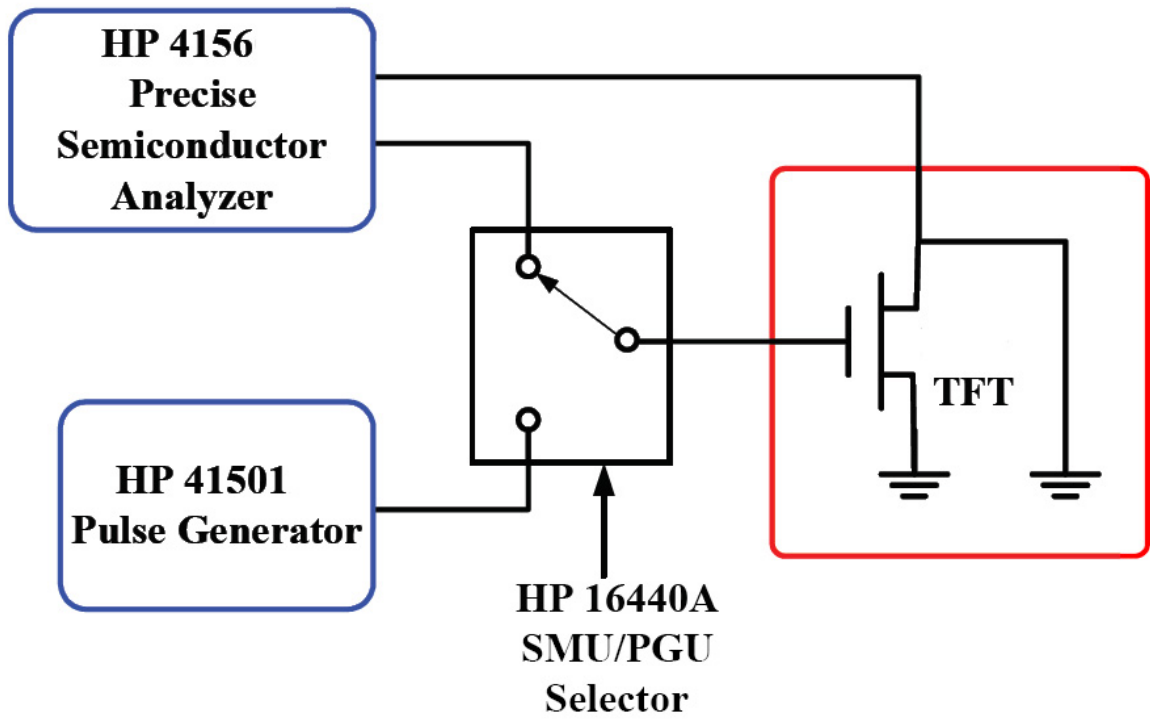


Fig. 2.3 Measurement configuration for the organic thin film transistor



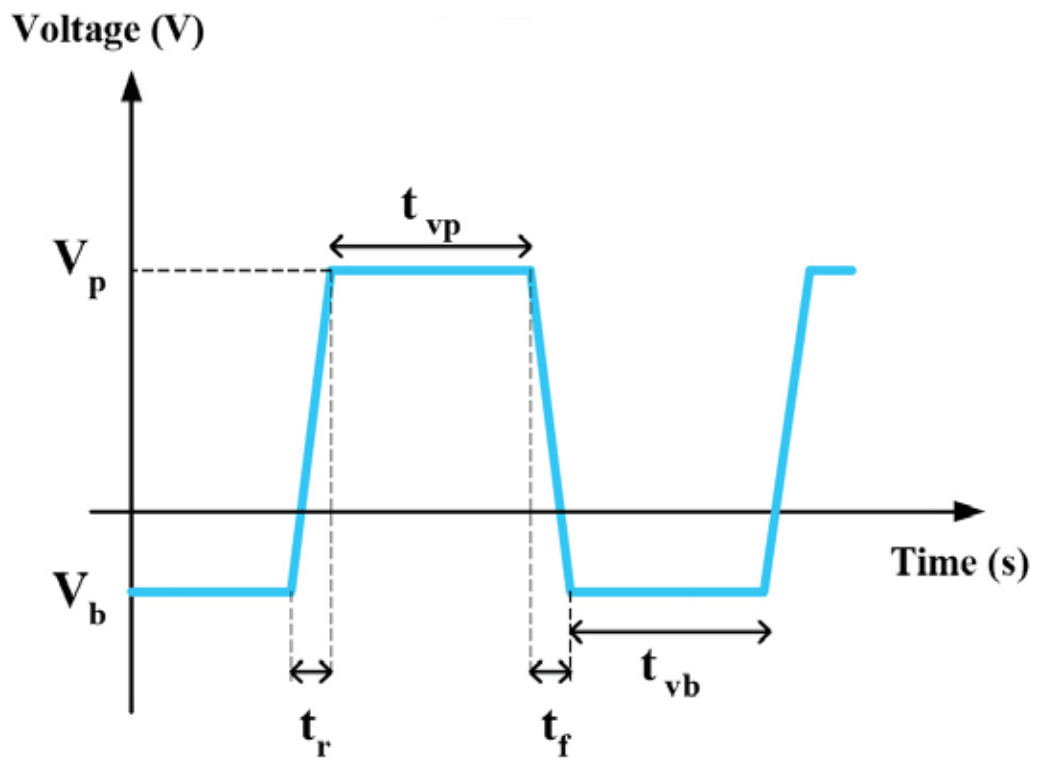
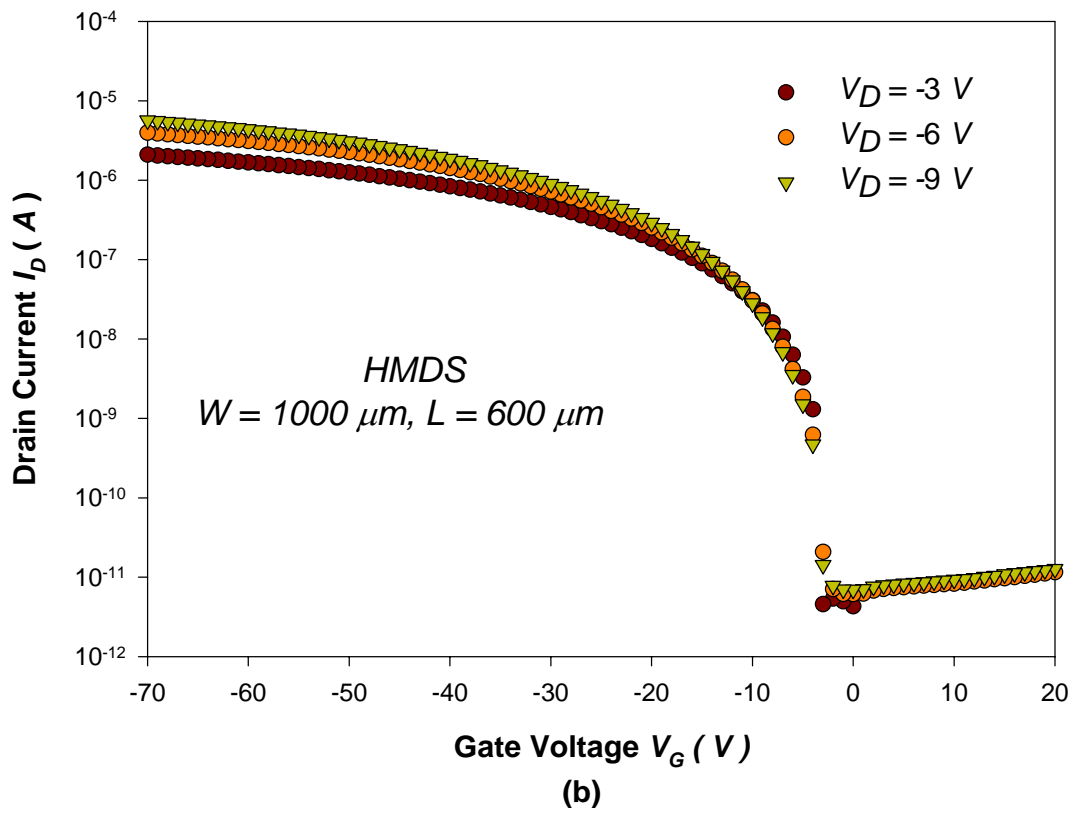
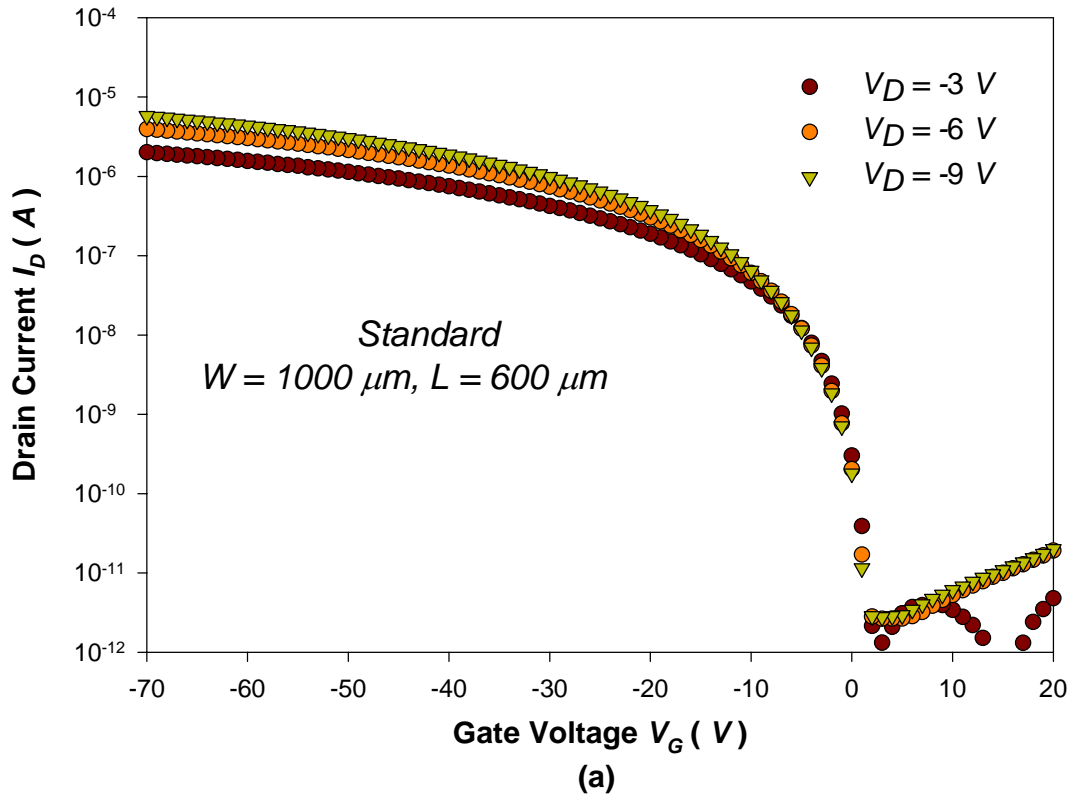
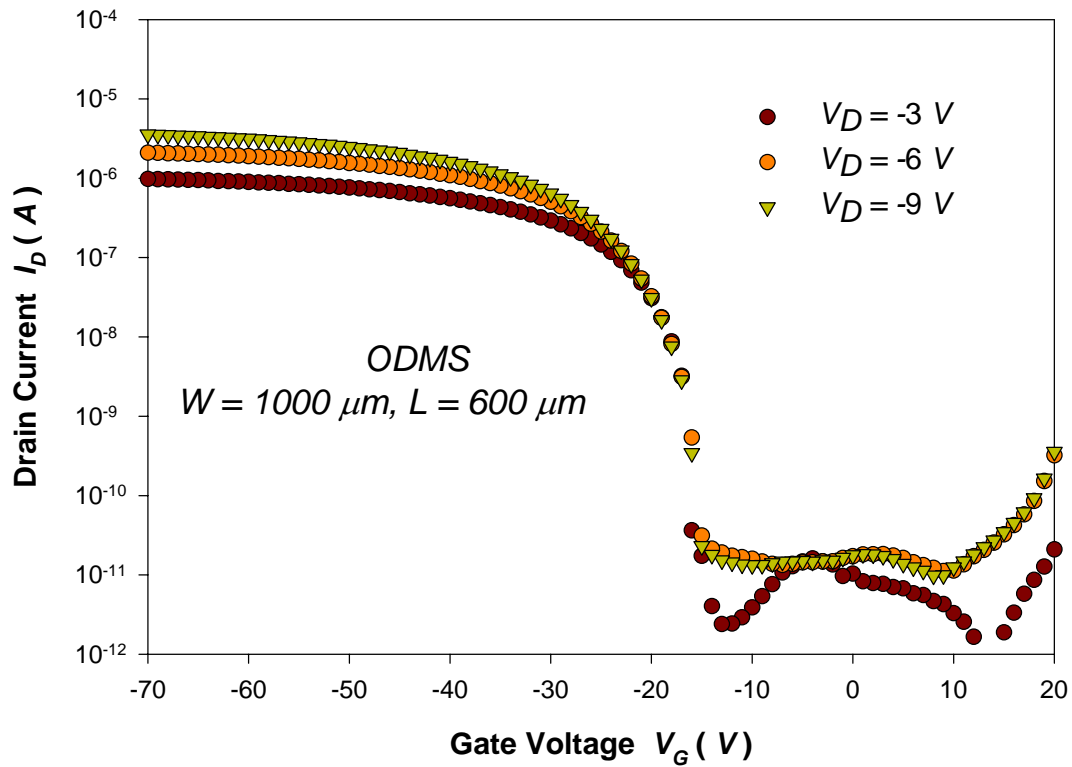


Fig. 2.4 Waveform and definition of the AC signal

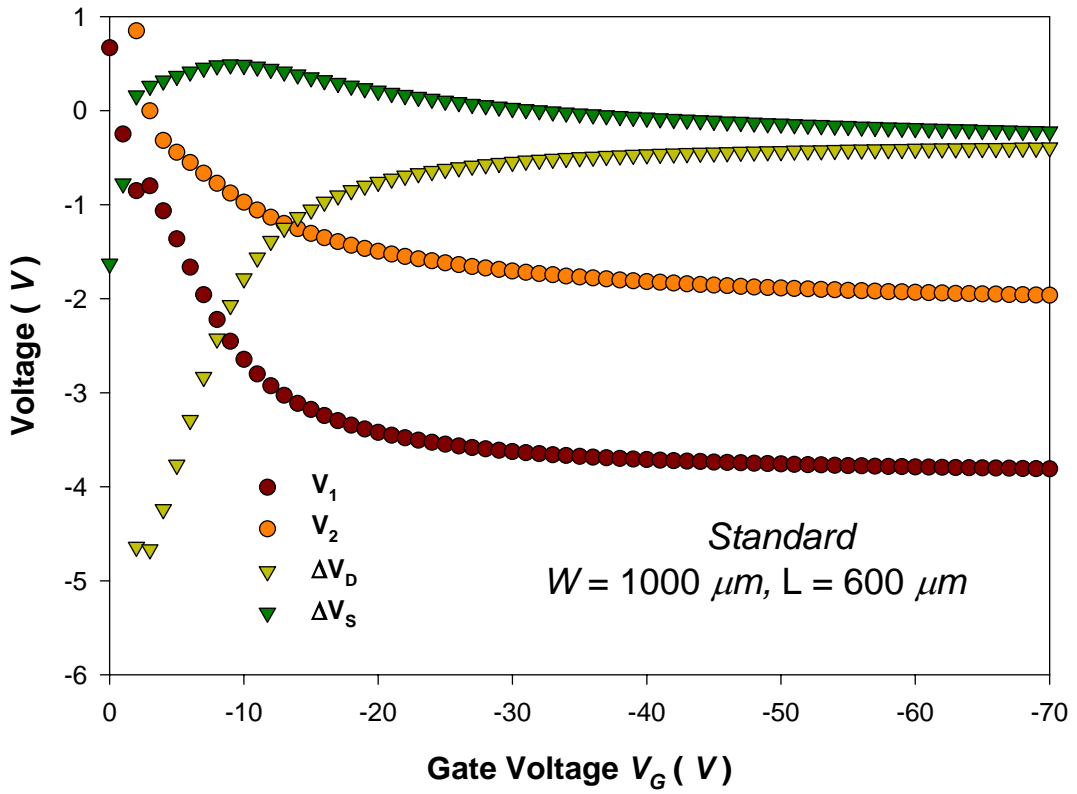




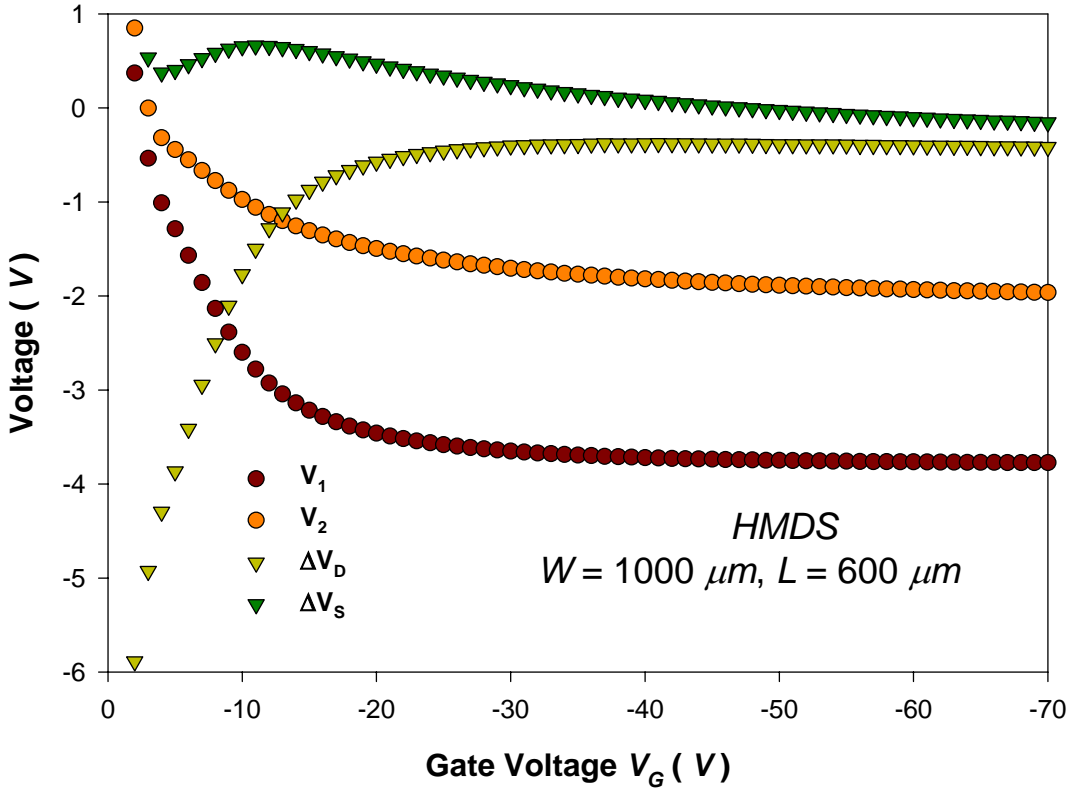


(c)

Fig. 3.1 Current V.S voltage plots for pentacene thin films with (a) Standard (b) HMDS and (c) ODMS surface treatments.



(a)



(b)

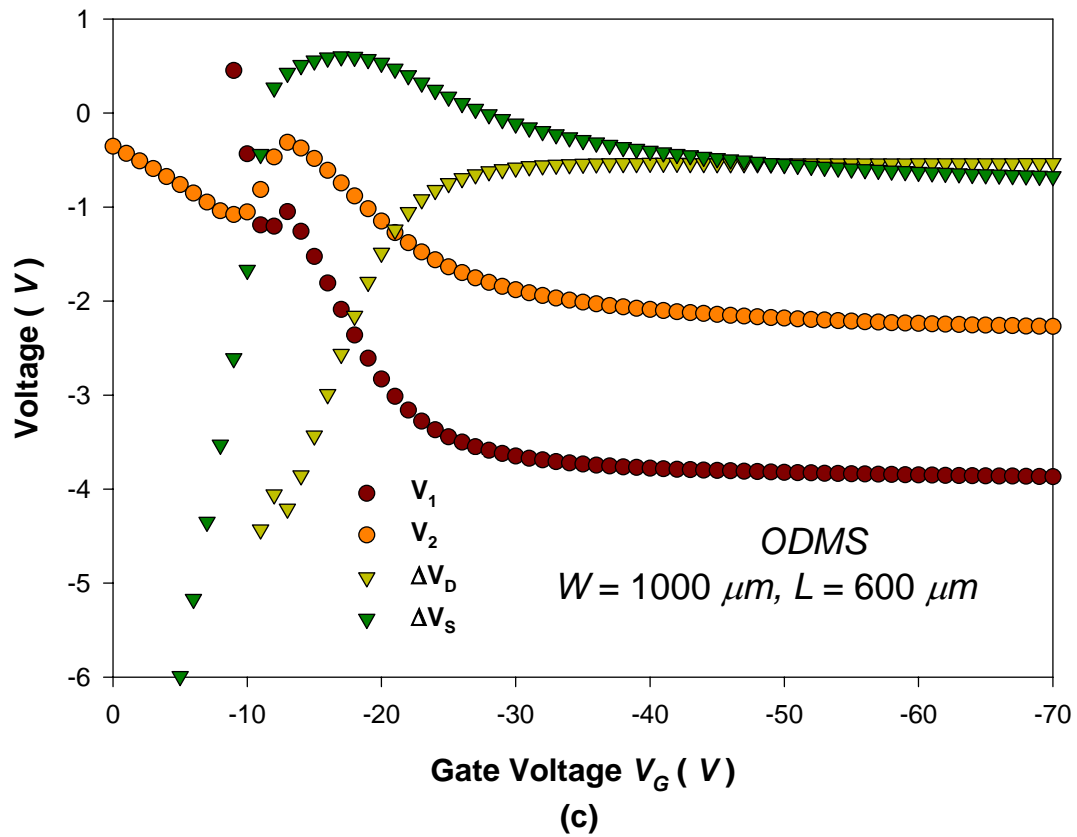
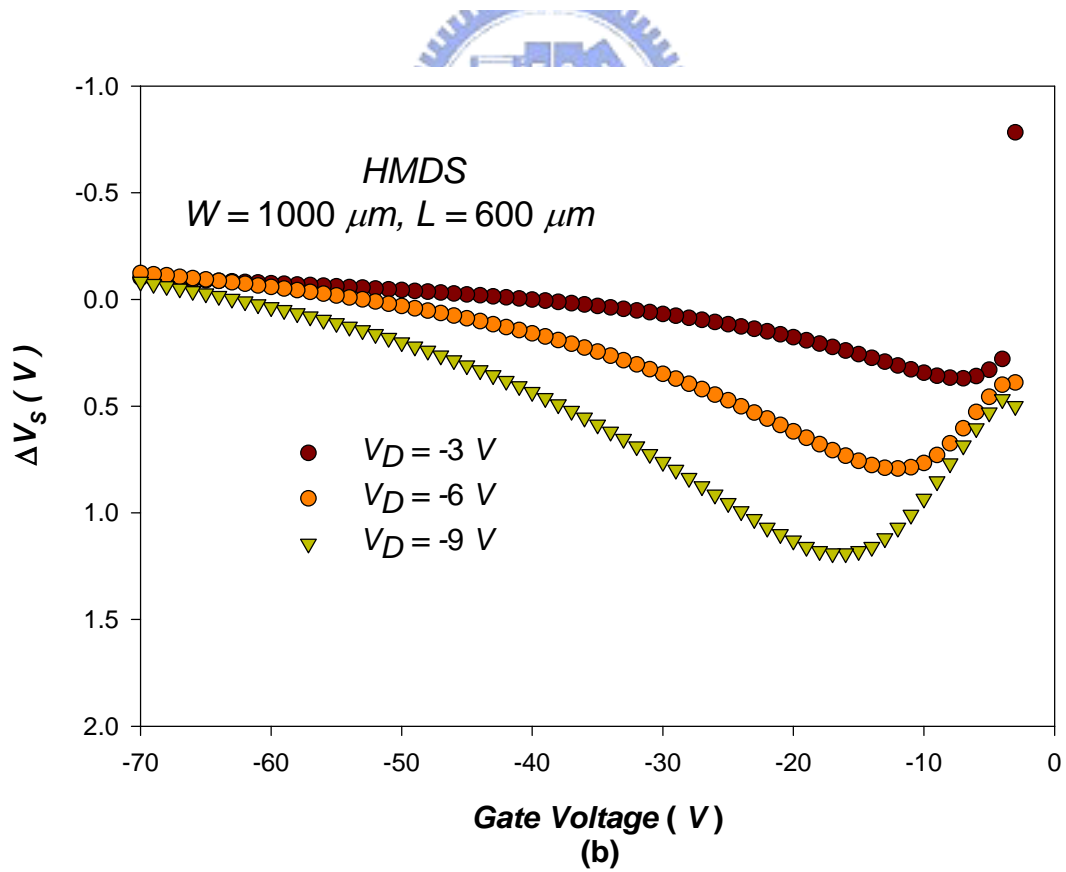
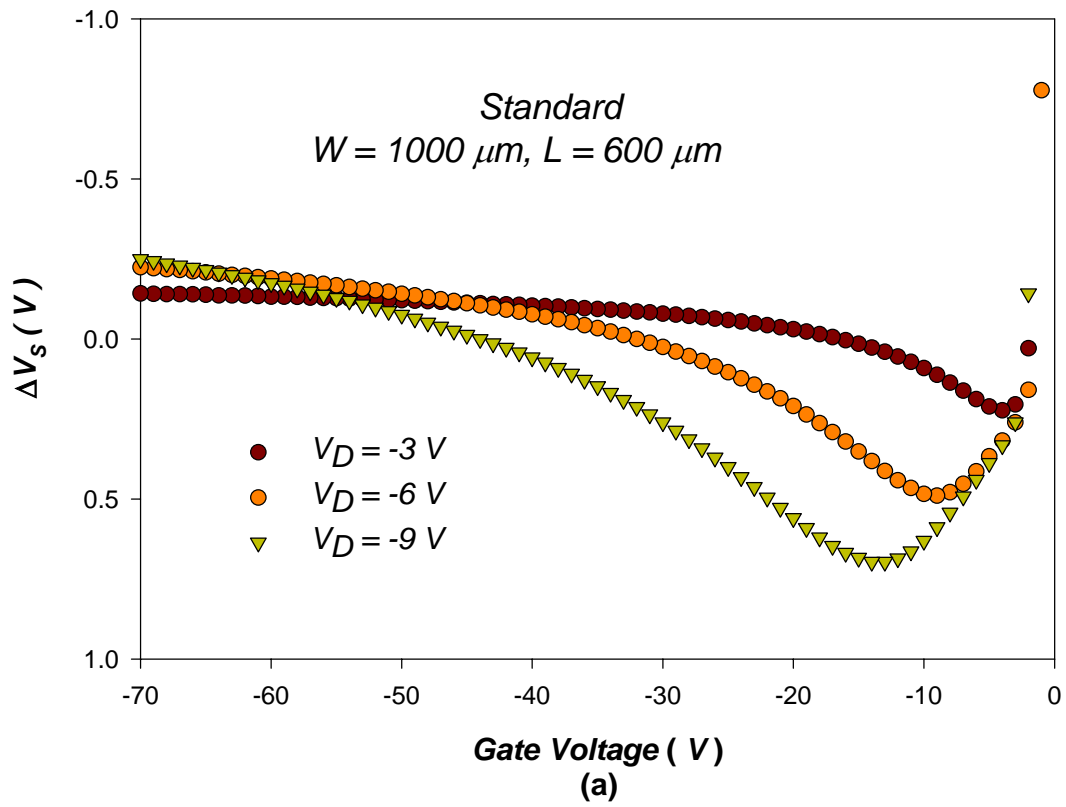


Fig. 3.2. Potential data and surface plots for devices with Standard, HMDS and ODMS surface treatment. (a), (b) and (c) potential data acquired via the channel potential probes as a function of V_G . Shown are the probe data, V_1 and V_2 , along with the extrapolated contact potential differences at the contacts ΔV_S and ΔV_D .



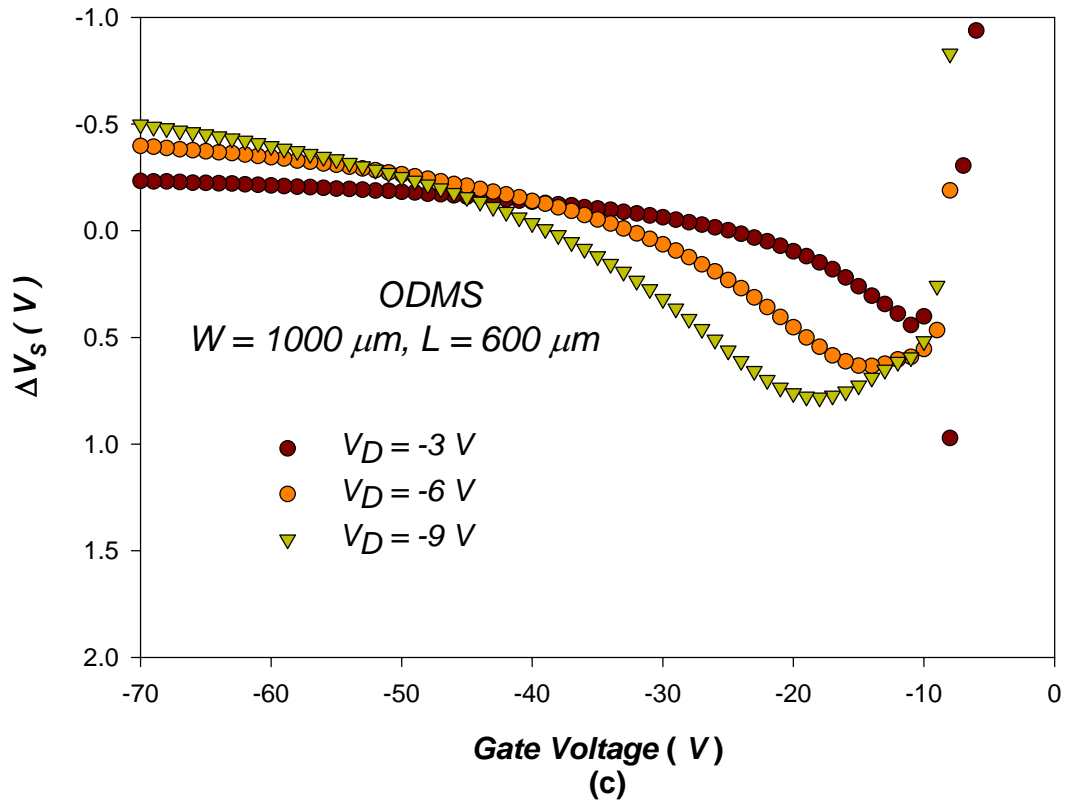
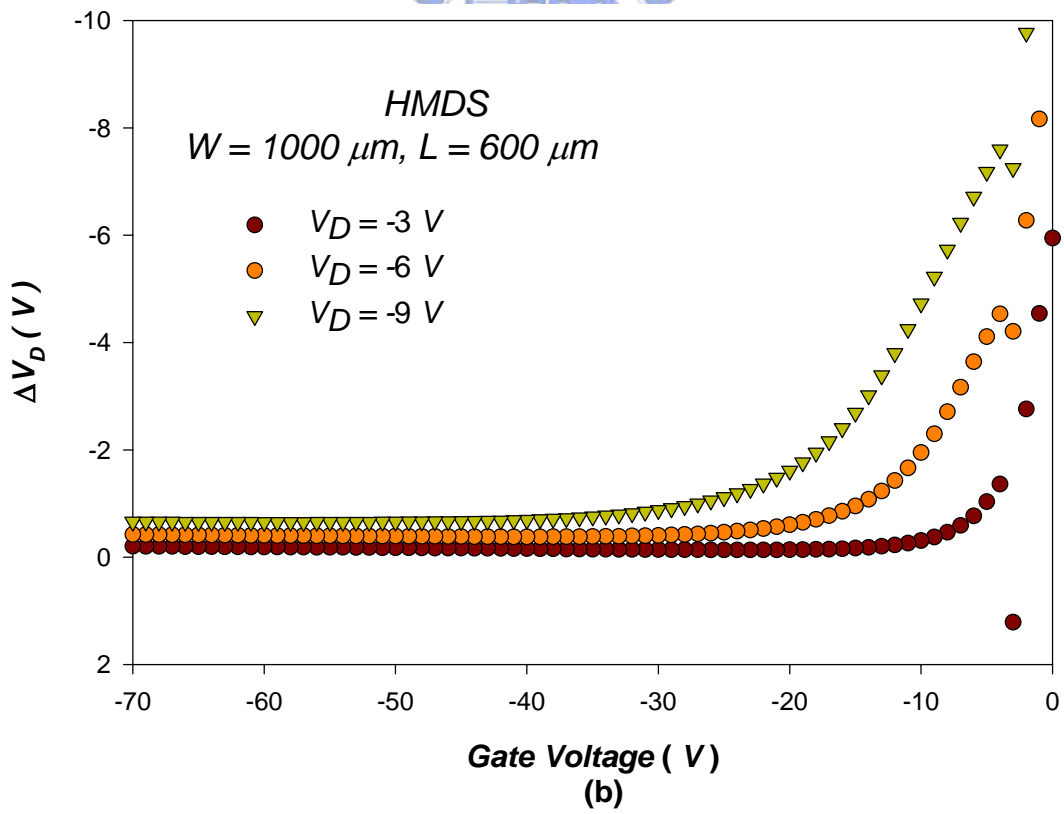
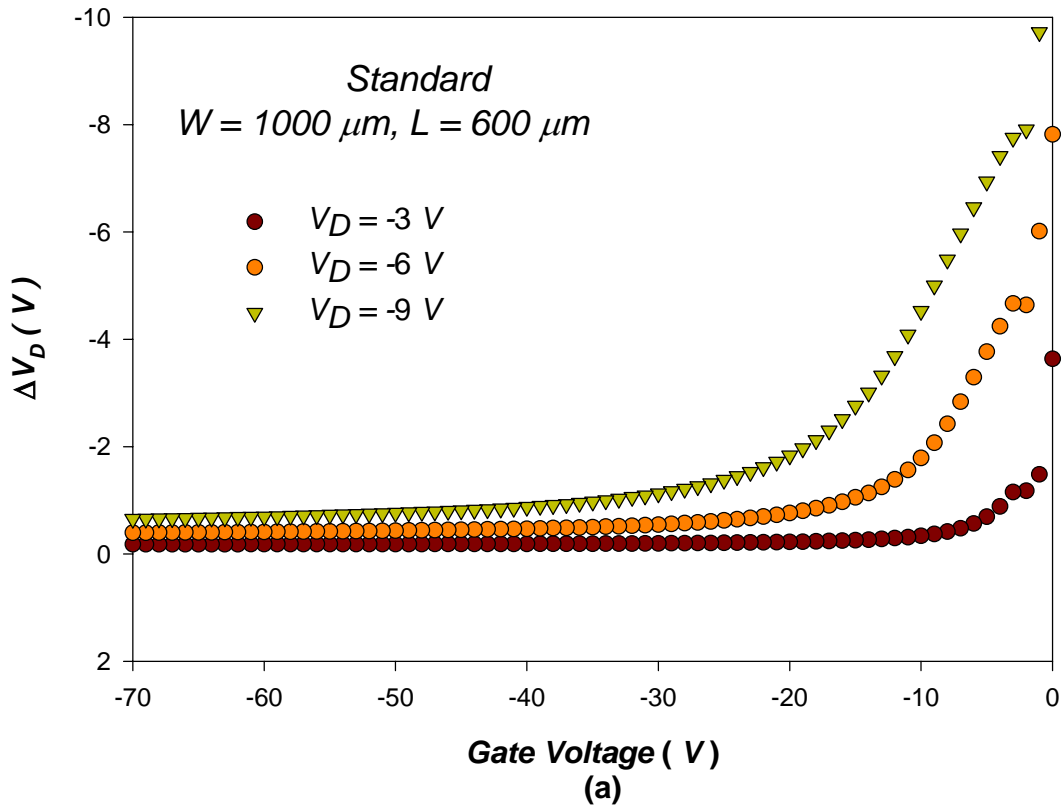


Fig. 3.3 Potential drops at the source with (a) Standard (b) HMDS and (c) ODMS surface treatments.





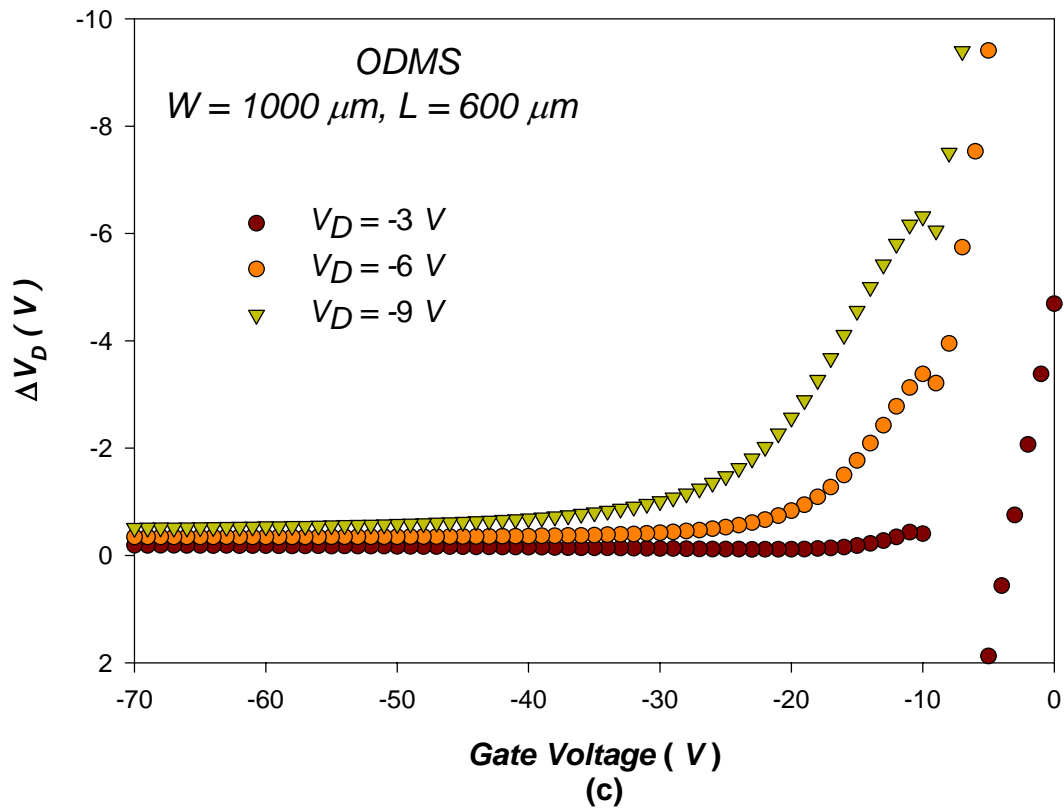


Fig. 3.4 Potential drops at the drain with (a) Standard (b) HMDS and (c) ODMS surface treatments.



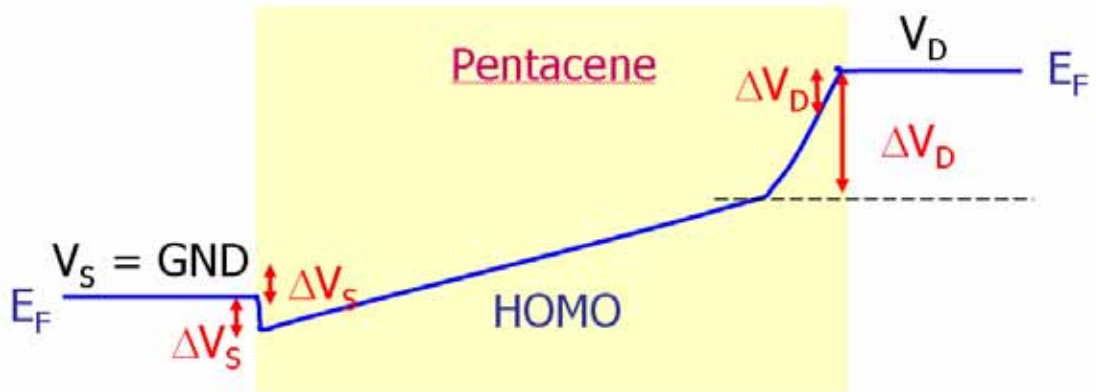


Fig.3.5. (a)

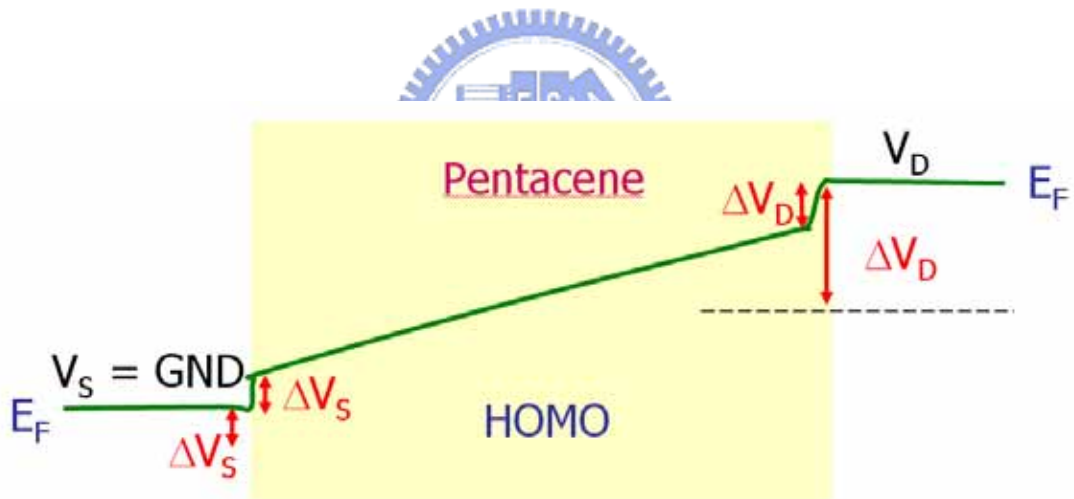
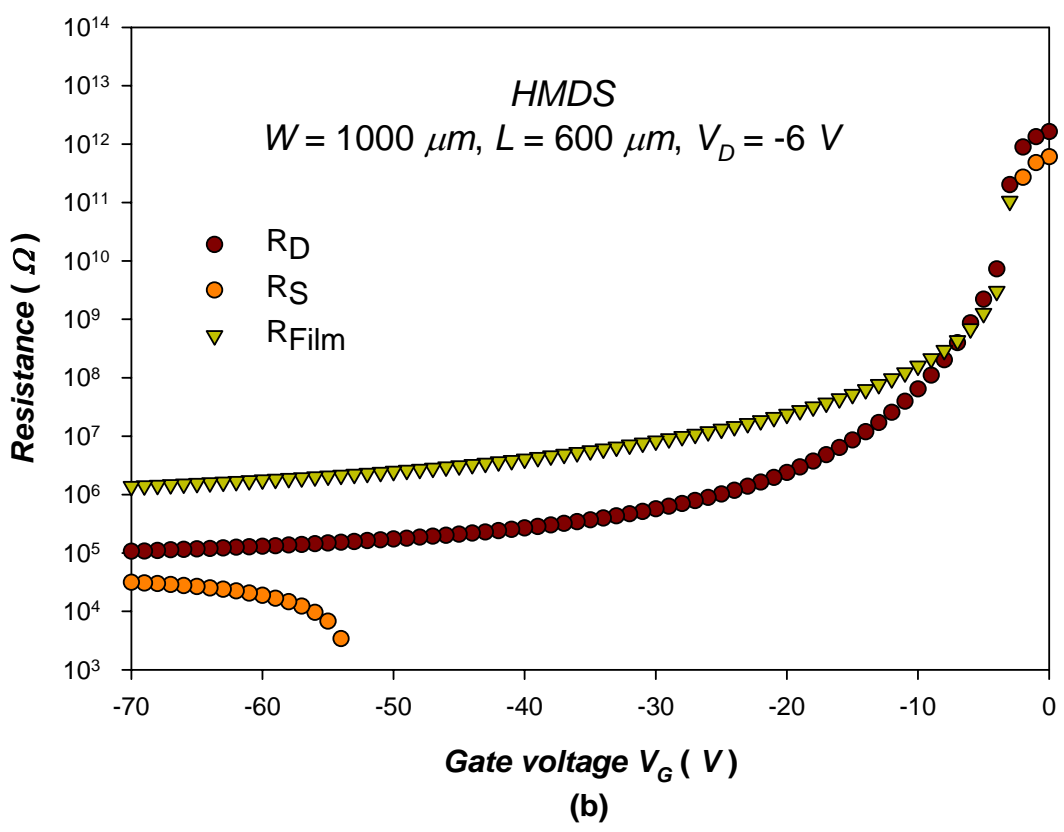
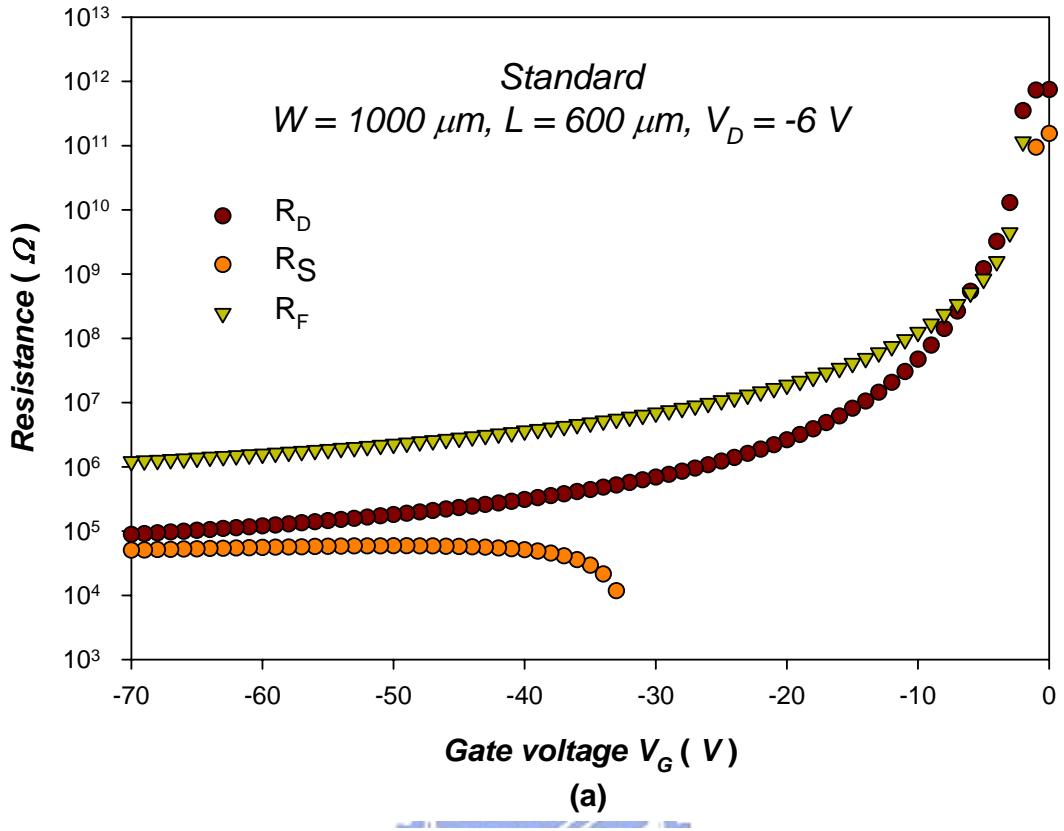


Fig.3.5. (b)

Fig. 3.5 The corresponding energy band of the OTFT operated at different region



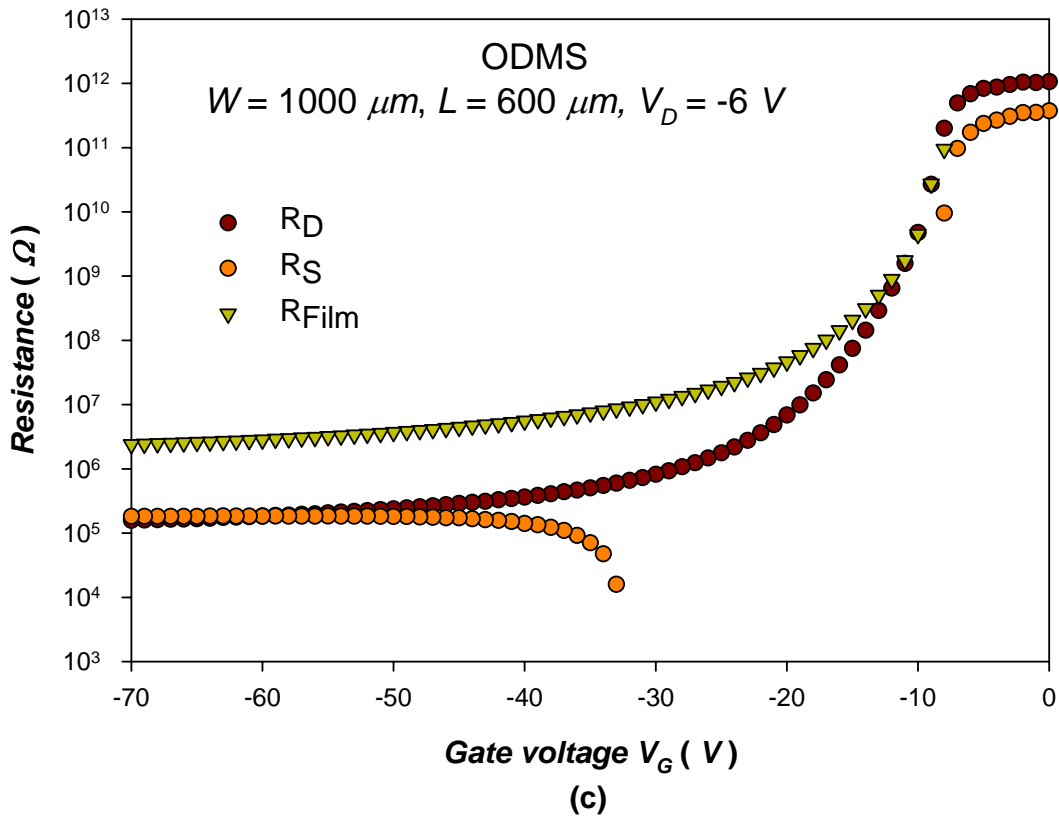


Fig. 3.6 Show the film resistances (R_{Film}) and contact resistances (R_D and R_S) as a function of gate voltage for (a) Standard (b) HMDS and (c) ODMS surface treatments top-contacted devices.

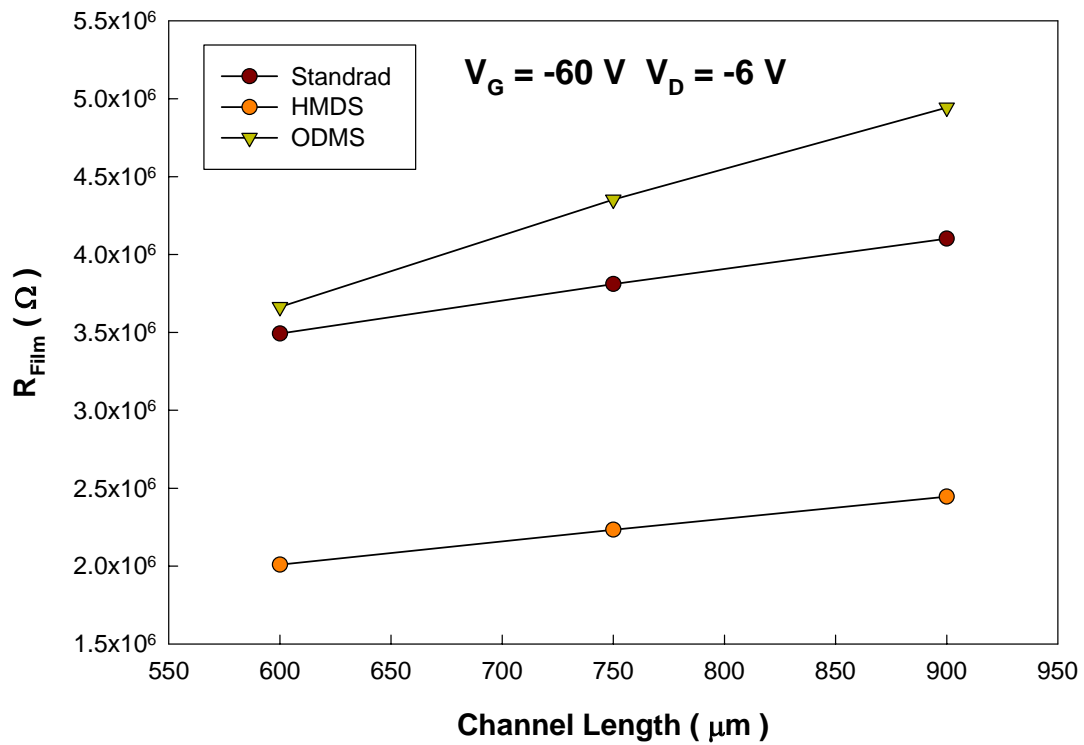
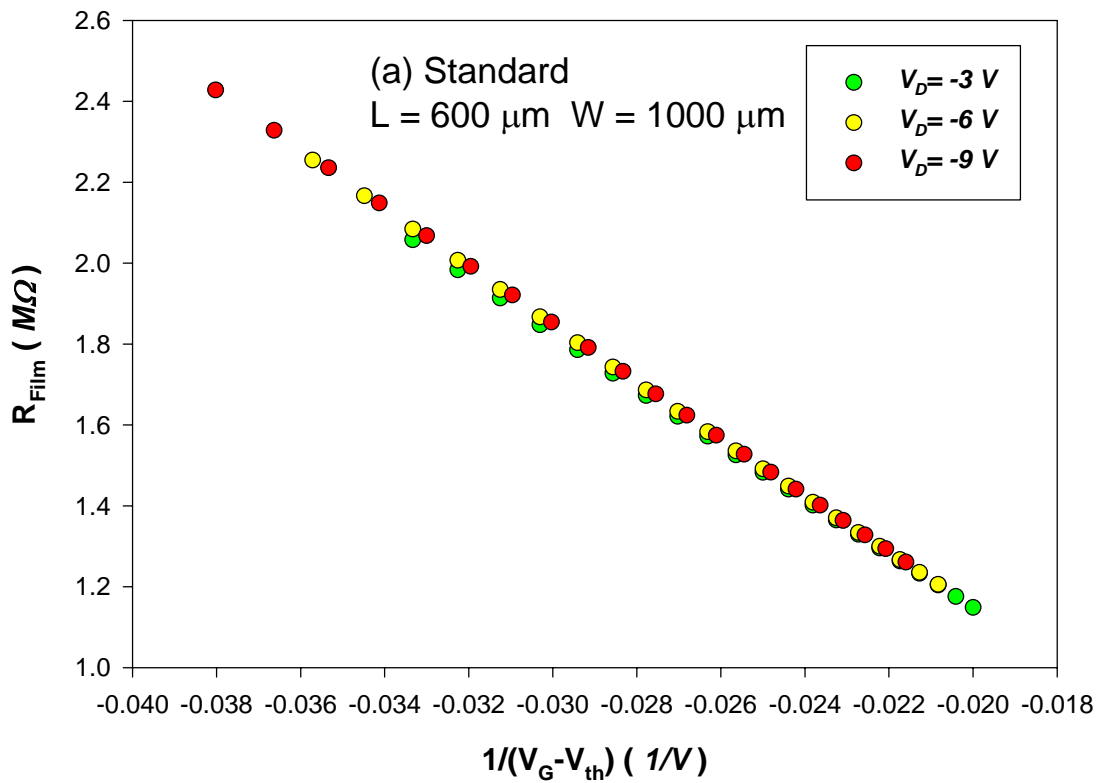


Fig. 3.7 illustrate R_{Film} V.S Channel length at $V_G = -60\text{V}$.



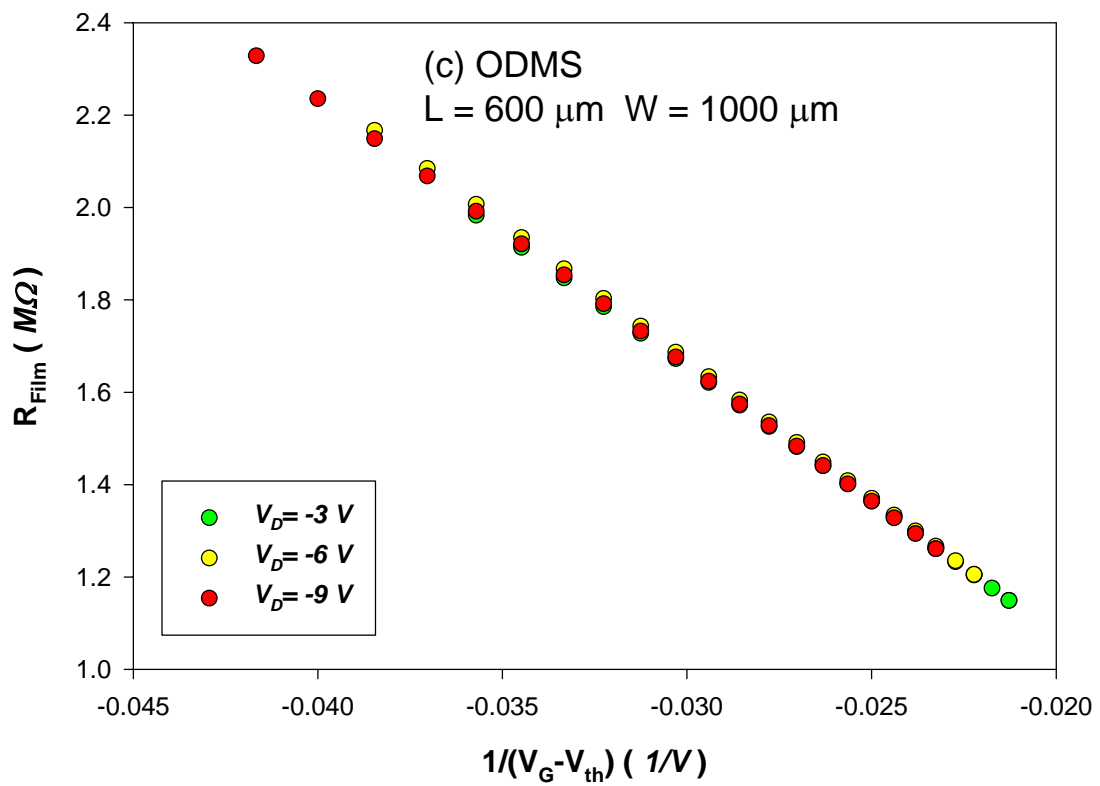
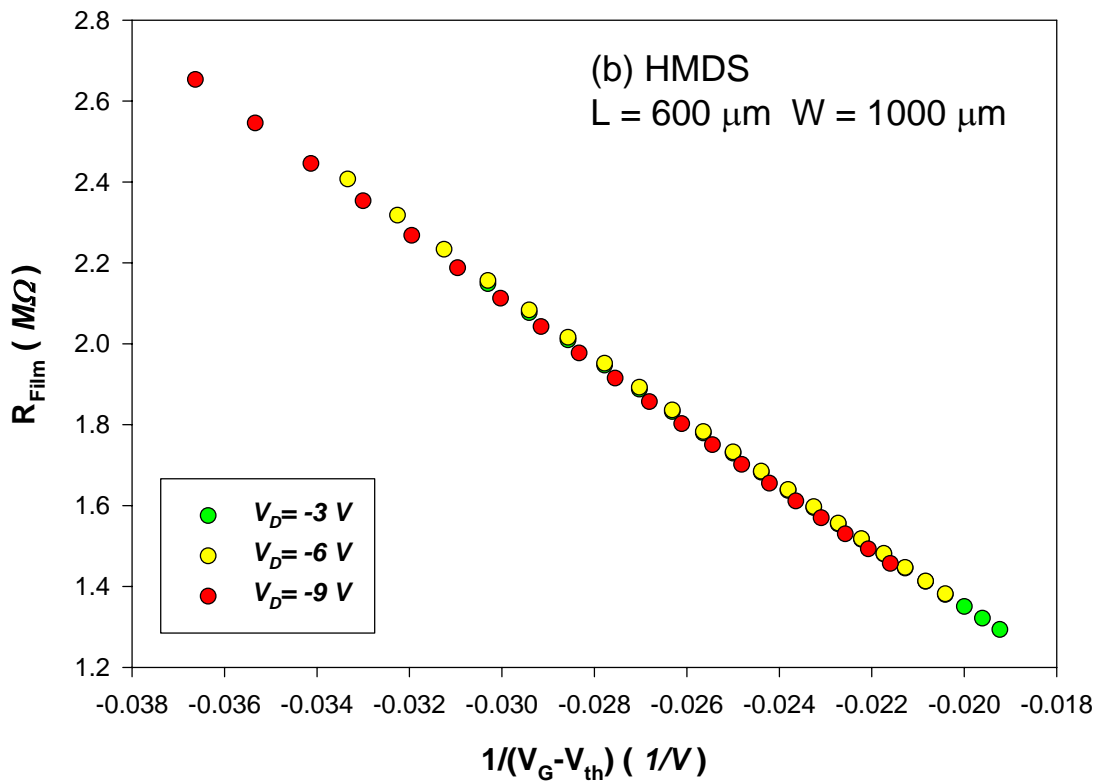


Fig. 3.8 illustrate R_{Film} V.S $1/(V_G - V_T)$ for (a) Standard (b) HMDS and (c) ODMS surface treatments top-contacted devices.

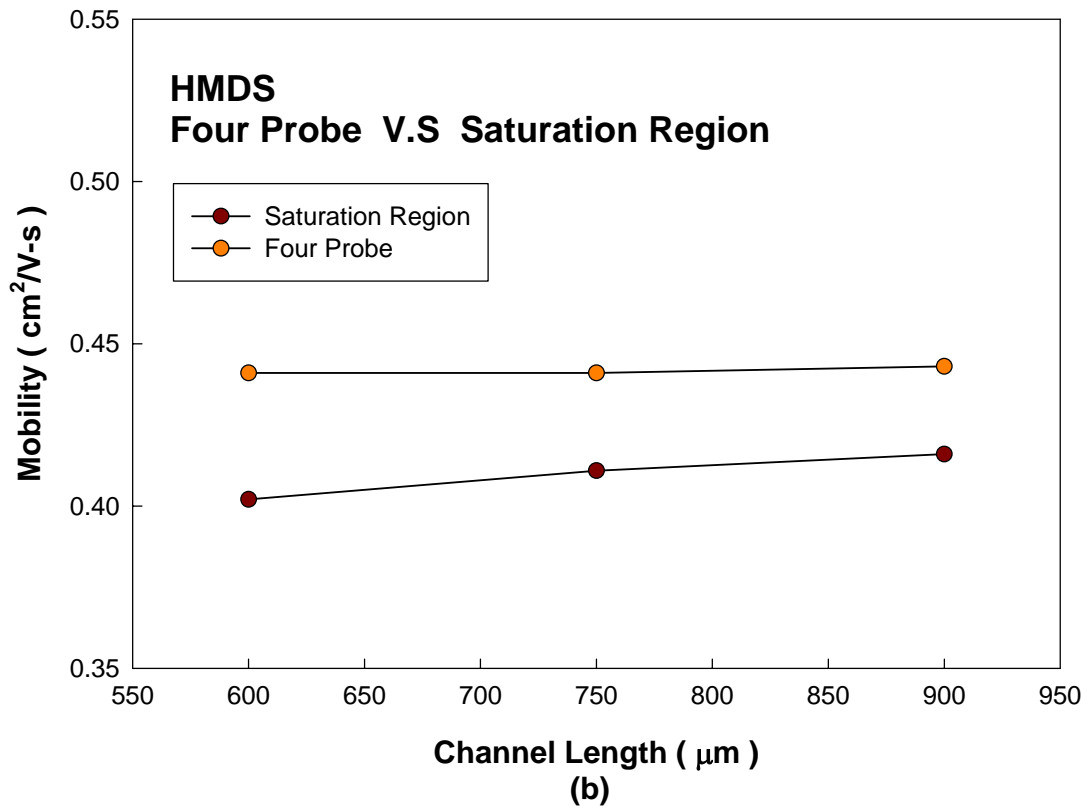
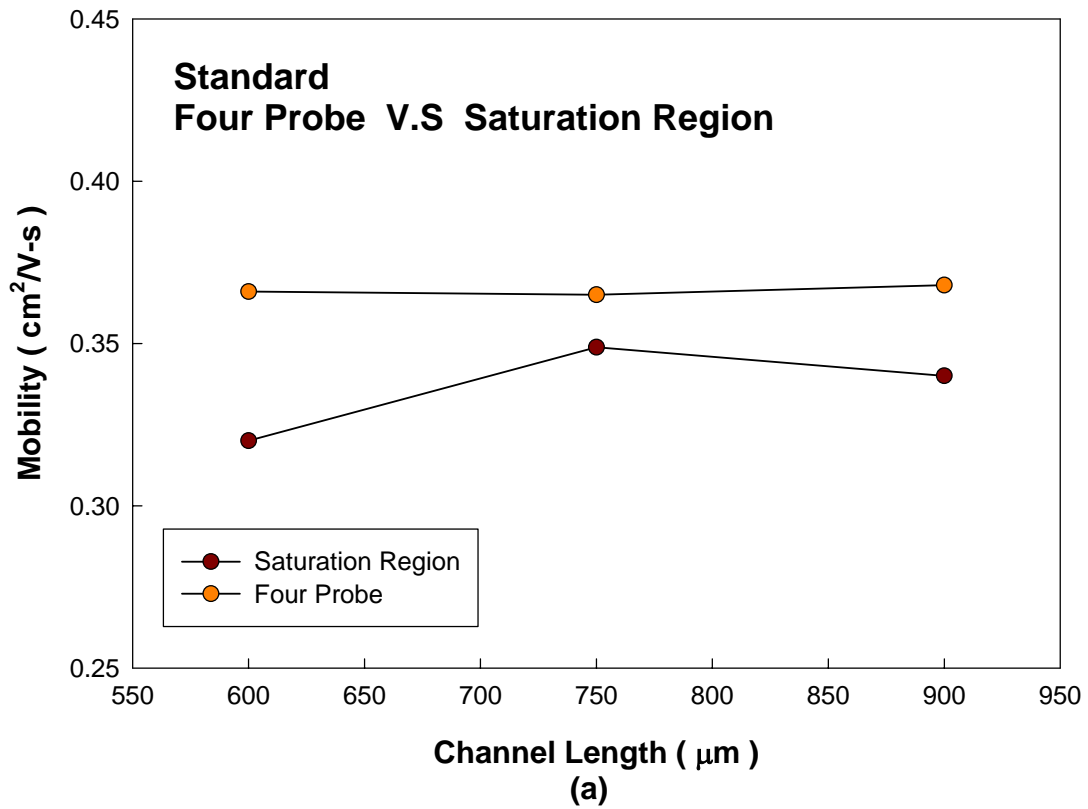


Fig. 3.9 (a) and (b) show that mobility which was extracted by gated-four-probe method was not depend on channel length variation.

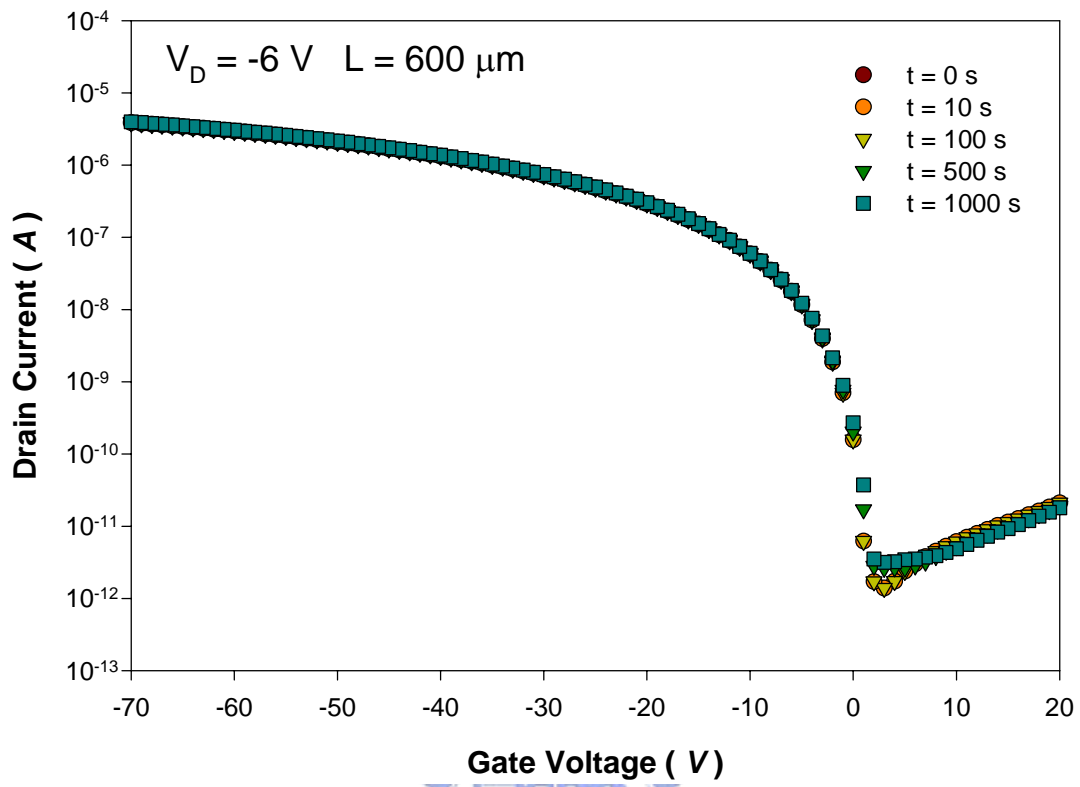


Fig. 3.10 The transfer characteristic I_D vs. V_G expose in atmosphere without stress.



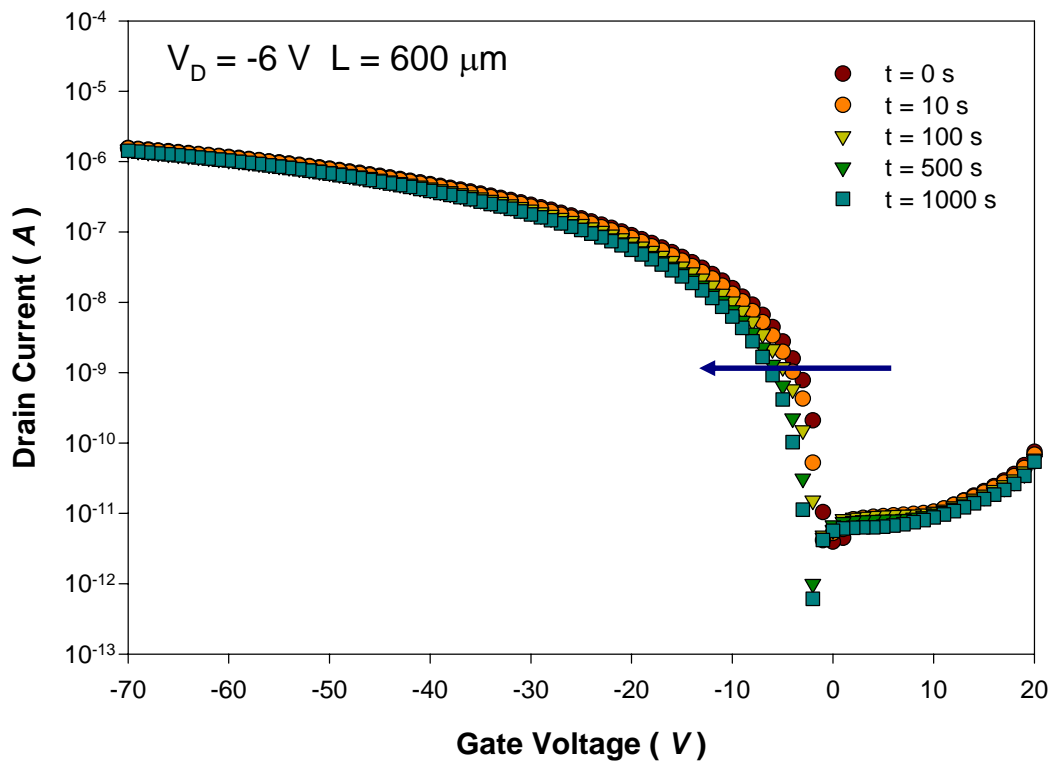


Fig. 3.11 Measured transfer curves of a pentacene TFTs deposited on thermal oxide with DC bias stress of -40 V.

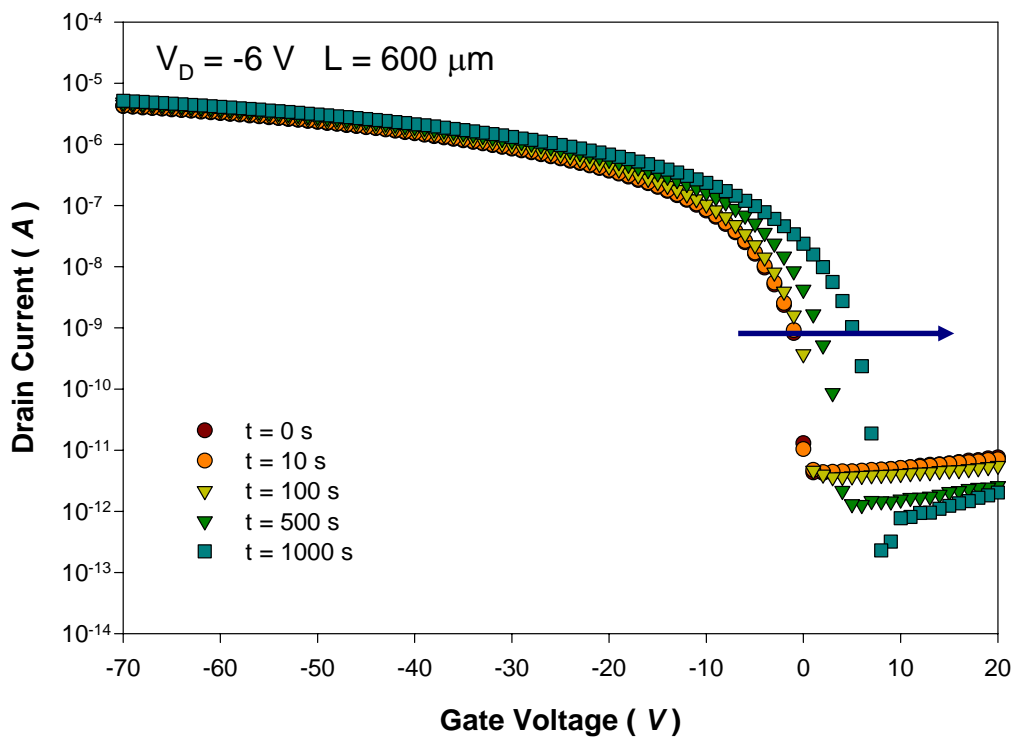


Fig. 3.12 Measured transfer curves of a pentacene TFTs deposited on thermal oxide with DC bias stress of 30 V.

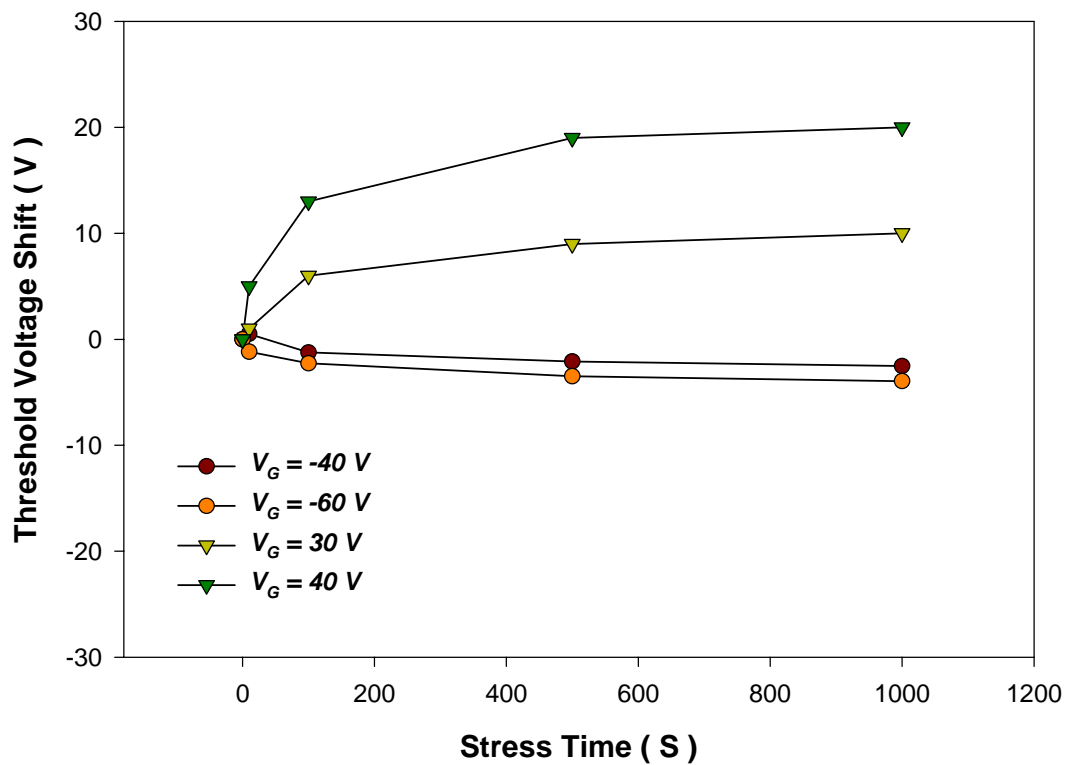


Fig. 3.13 Threshold voltage shift vs. bias stress time for positive bias stress of +30 and +40 V, and negative bias stress of -10 and -30 V.

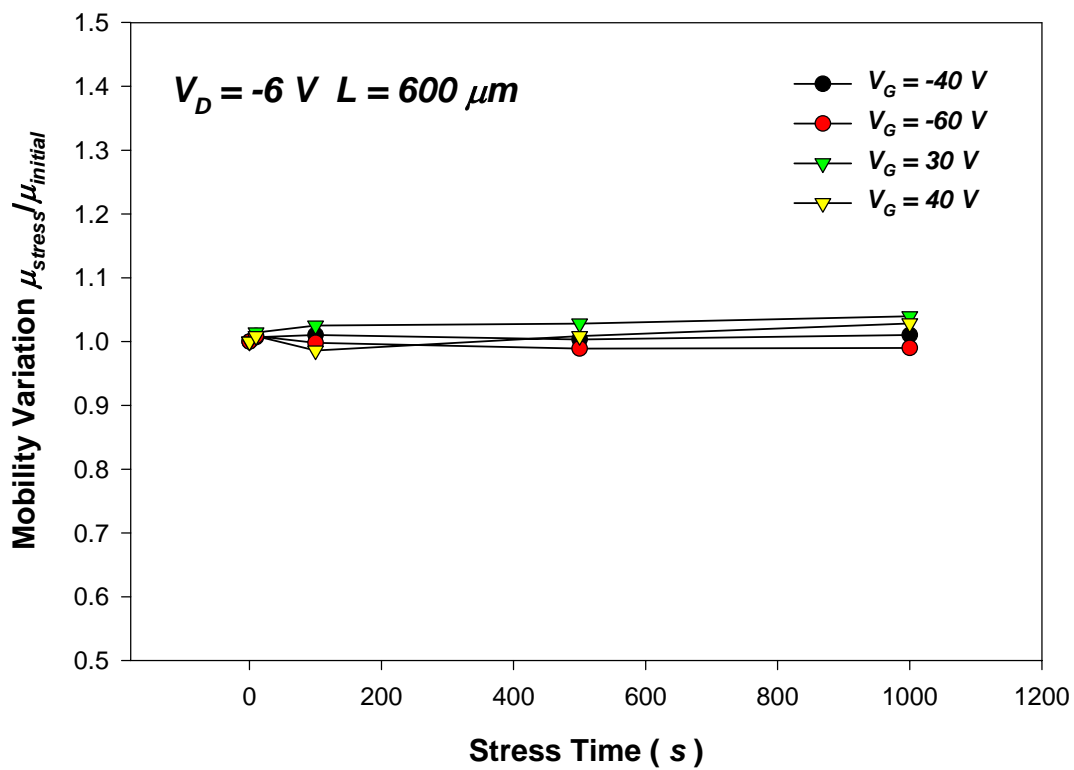


Fig. 3.14 Normalize film mobility of pentacene TFTs after DC bias stress.

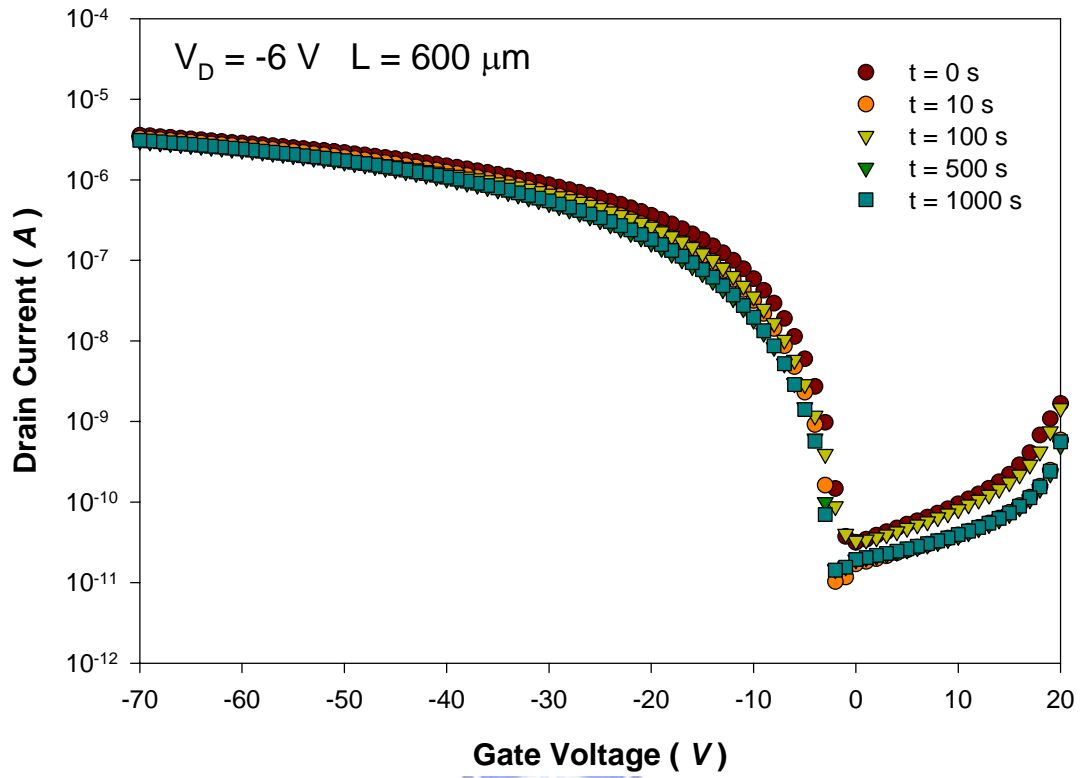


Fig. 3.15 The transfer characteristic I_D vs. V_G expose in atmosphere without stress.



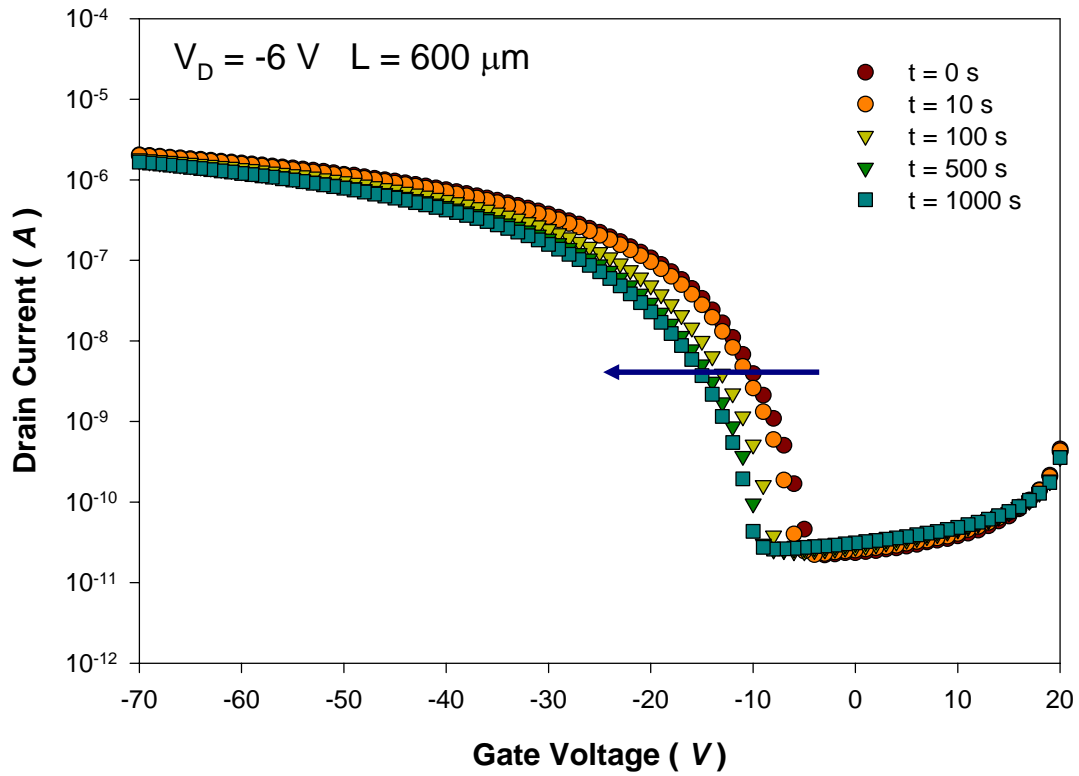


Fig. 3.16 Measured transfer curves of a pentacene TFTs deposited on HMDS surface treatment with DC bias stress of -40 V.

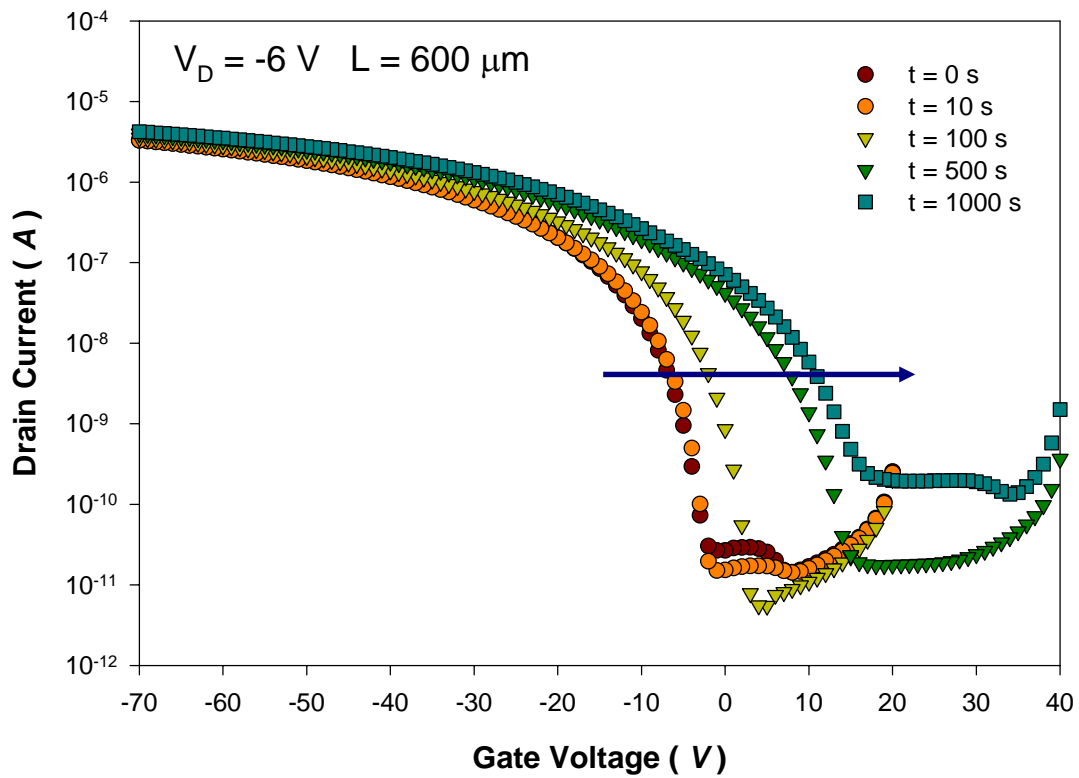


Fig. 3.17 Measured transfer curves of a pentacene TFTs deposited on HMDS surface treatment with DC bias stress of 30 V.

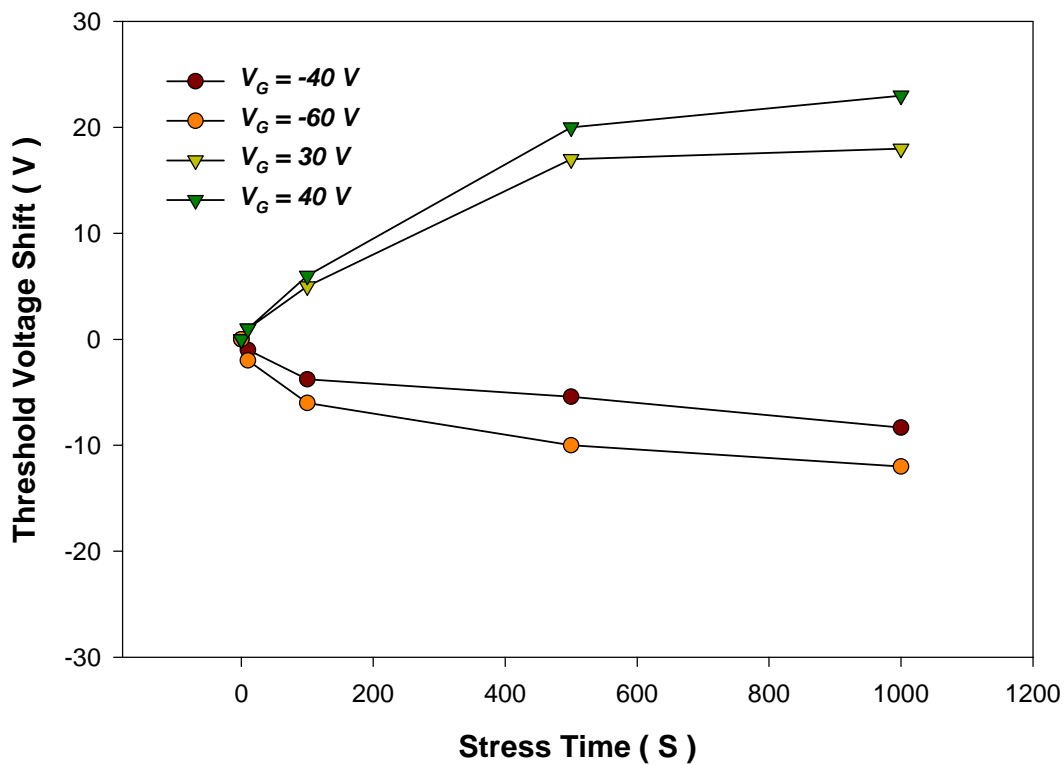


Fig. 3.18 Threshold voltage shift vs. bias stress time for positive bias stress of +30 and +40 V, and negative bias stress of -10 and -30 V.

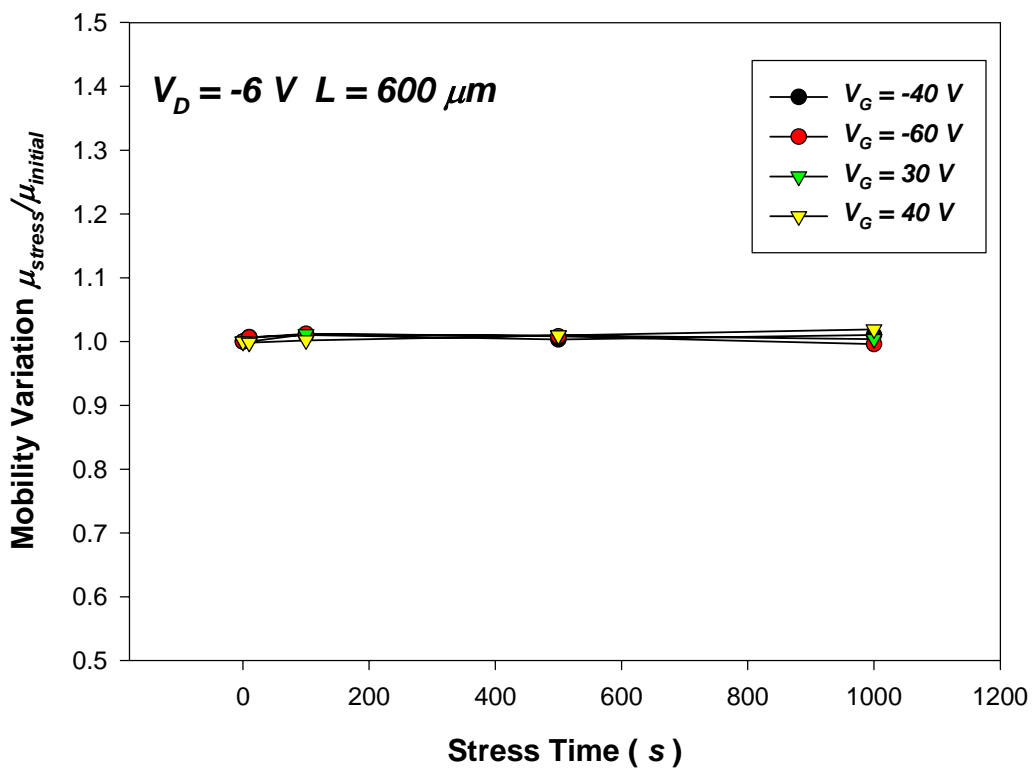


Fig. 3.19 Normalize film mobility of pentacene TFTs after DC bias stress.

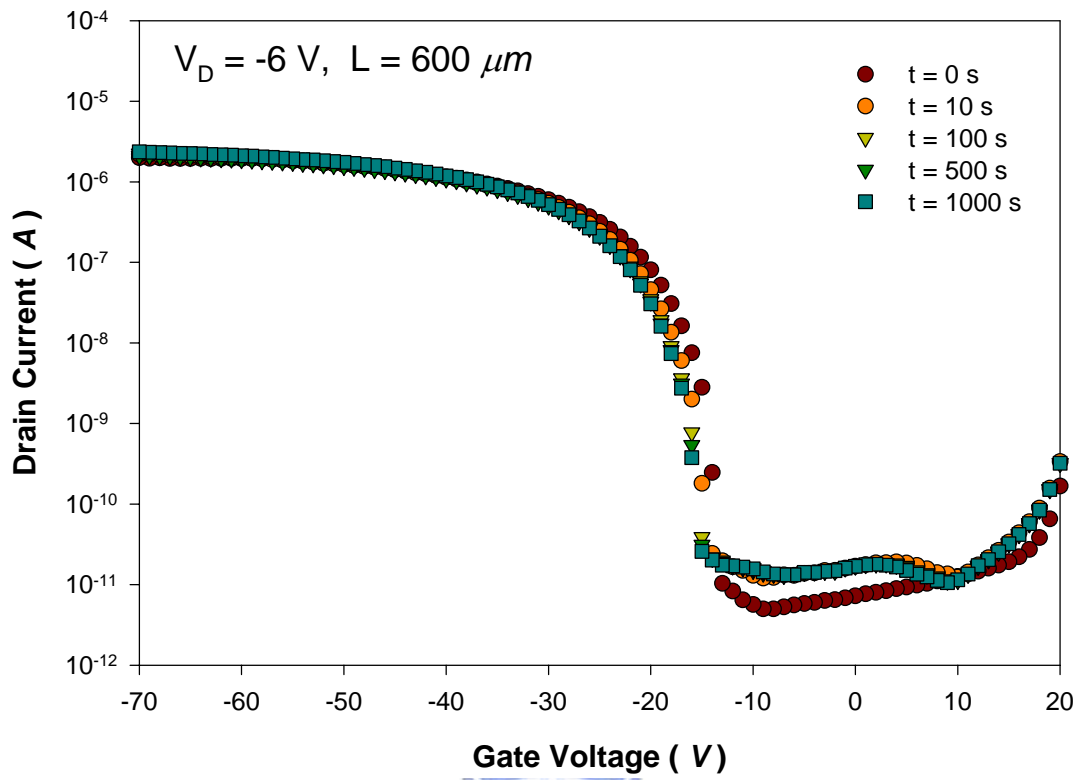


Fig. 3.20 The transfer characteristic I_D vs. V_G expose in atmosphere without stress.



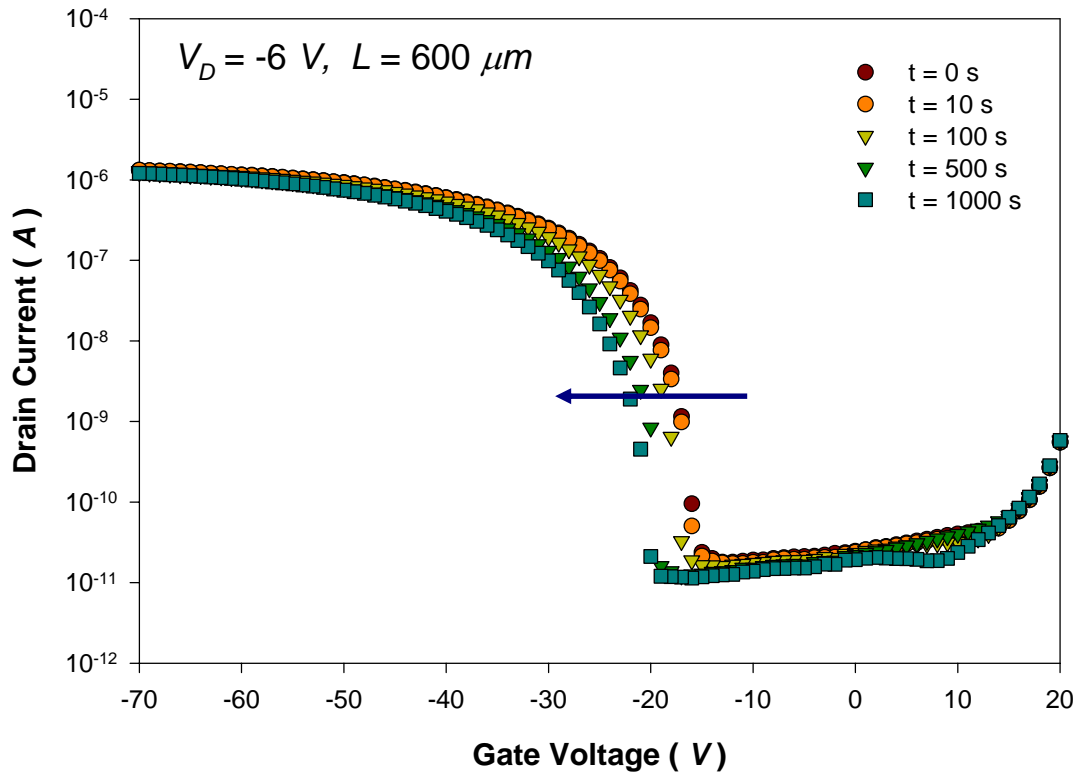


Fig. 3.21 Measured transfer curves of a pentacene TFTs deposited on ODMS surface treatment with DC bias stress of -40 V.

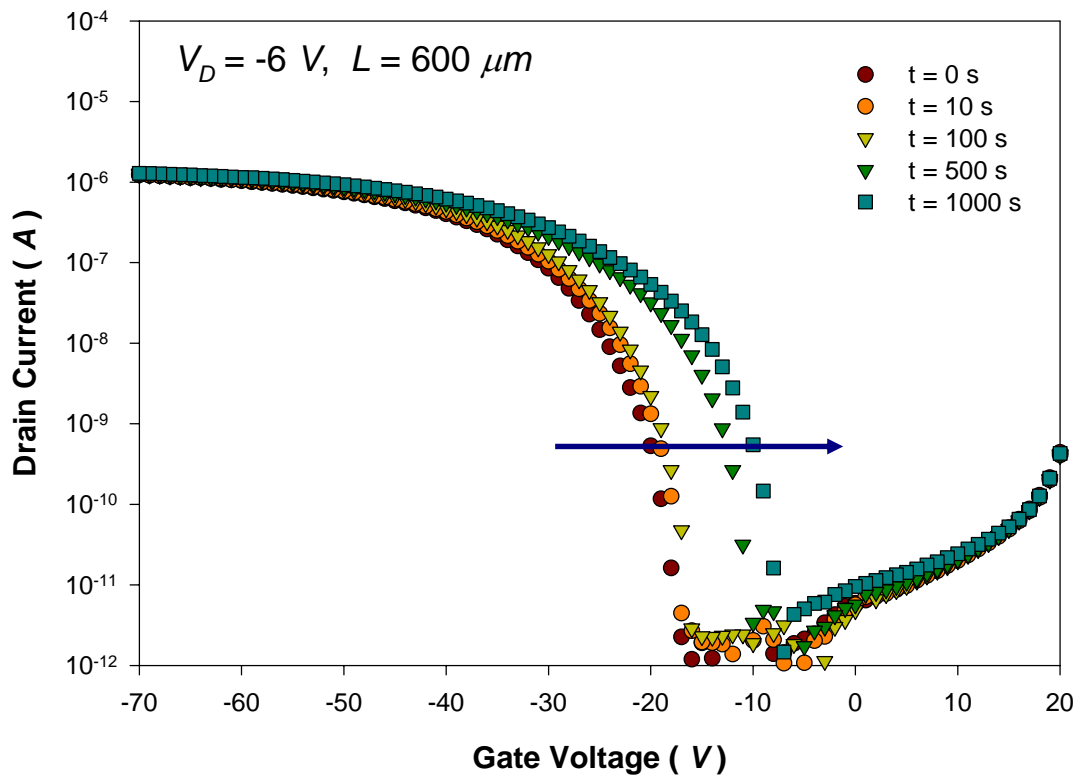


Fig. 3.22 Measured transfer curves of a pentacene TFTs deposited on ODMS surface treatment with DC bias stress of 30 V.

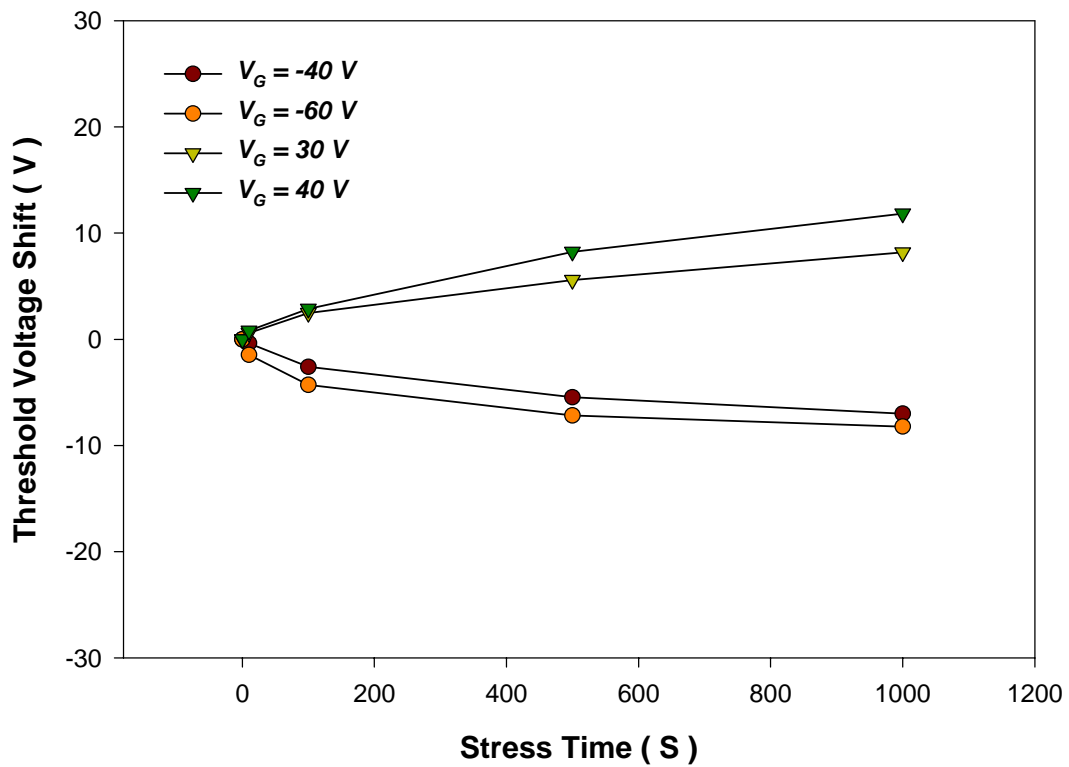


Fig. 3.23 Threshold voltage shift vs. bias stress time for positive bias stress of +30 and +40 V, and negative bias stress of -10 and -30 V.

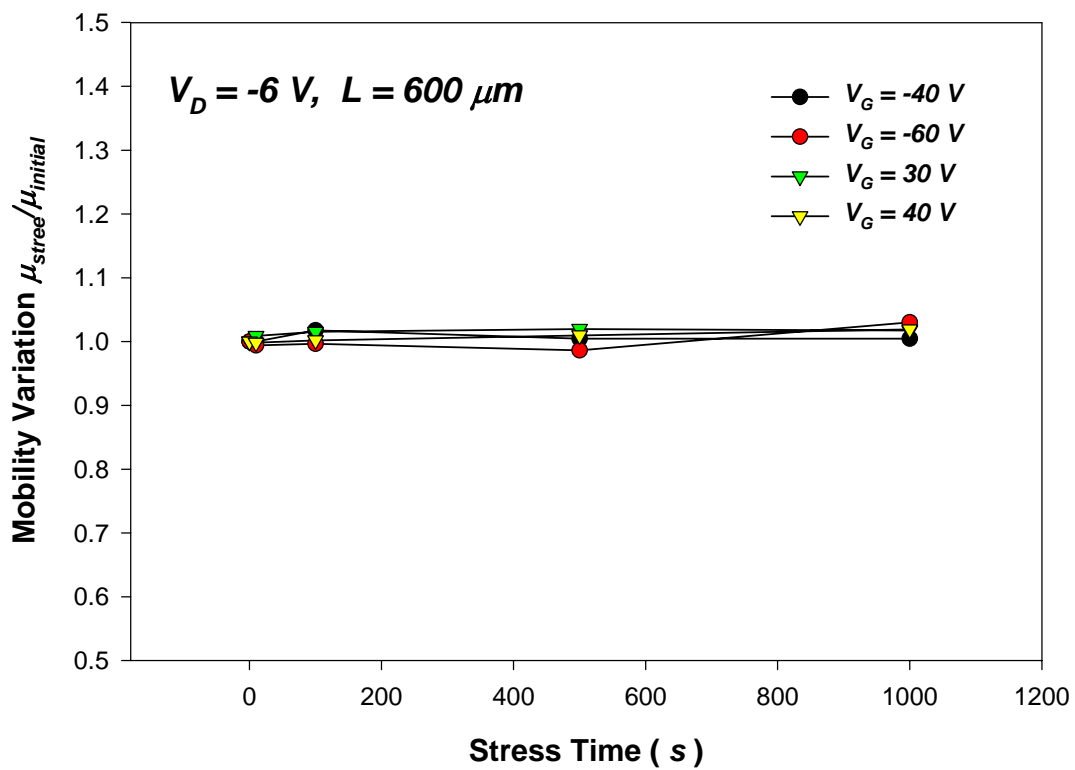


Fig. 3.24 Normalize film mobility of pentacene TFTs after DC bias stress.

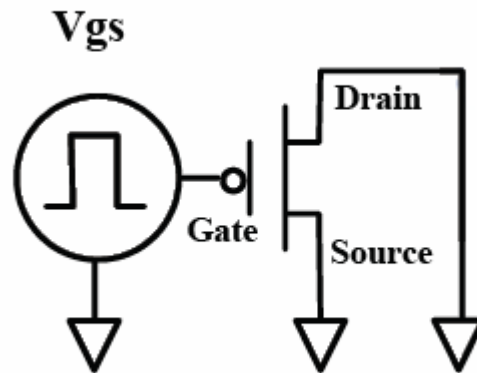


Fig. 3.25 Pulse voltage was applied to the gate electrode and source and drain were grounded.



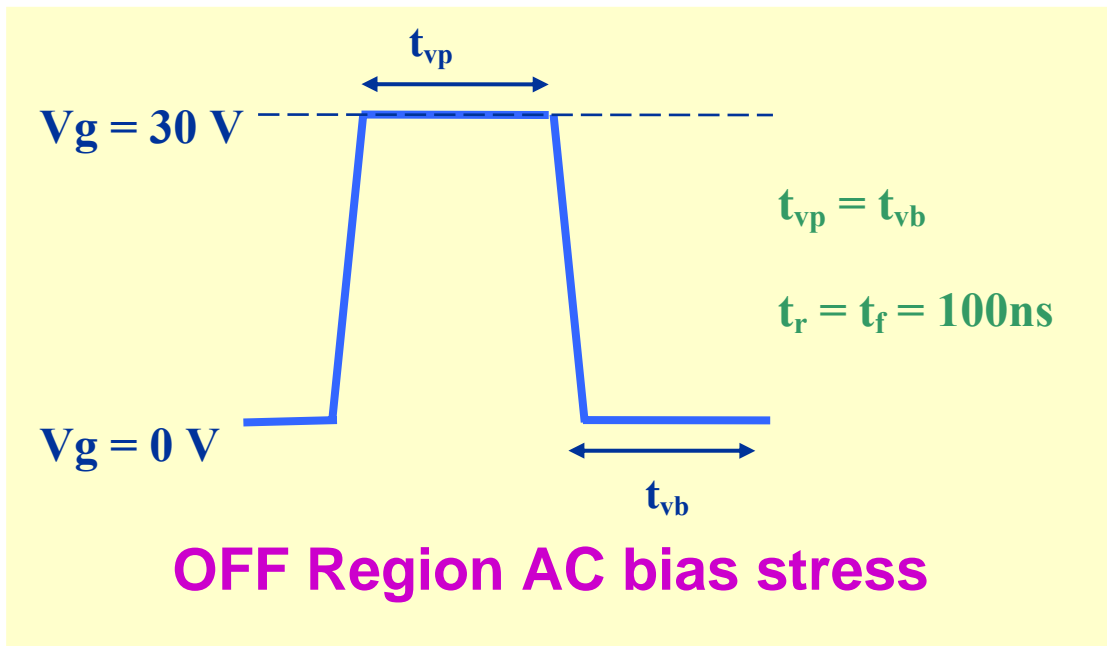
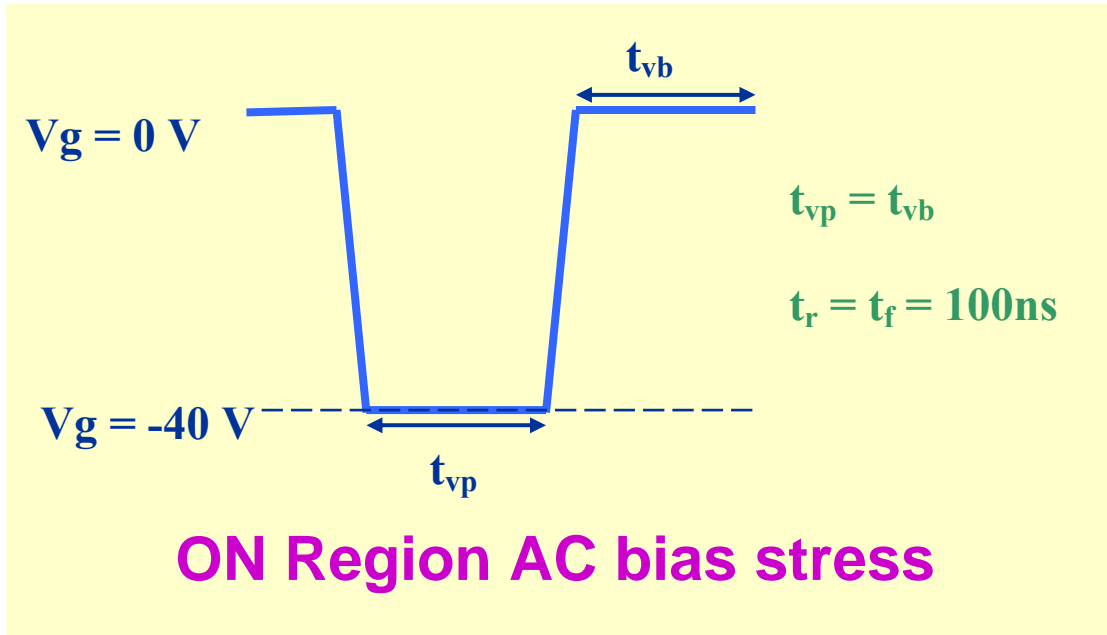
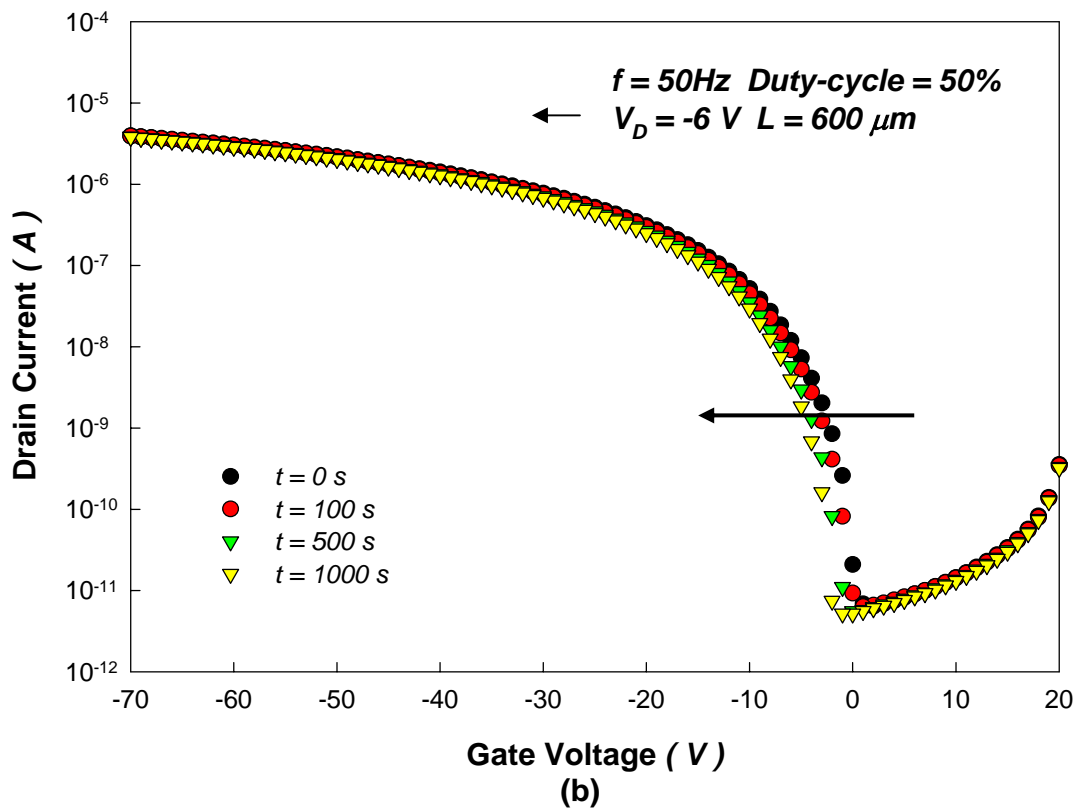
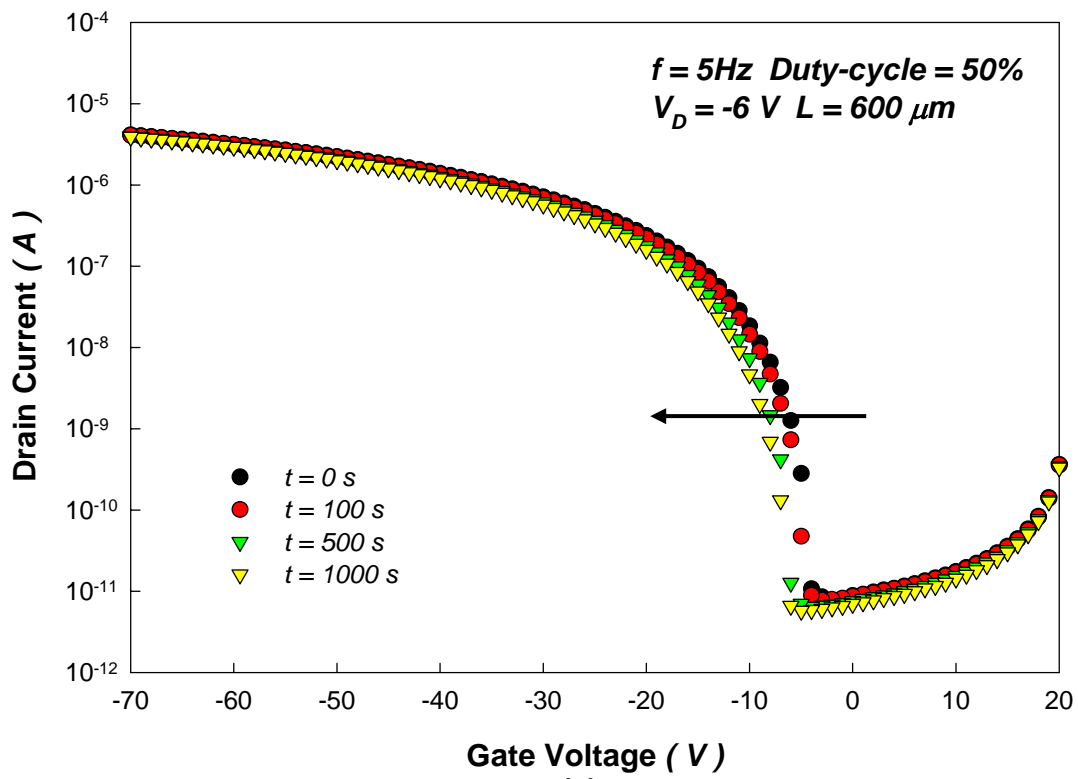


Fig. 3.26 The pulse swing region was separated into two parts; one was the ON region, and the other was the OFF region.



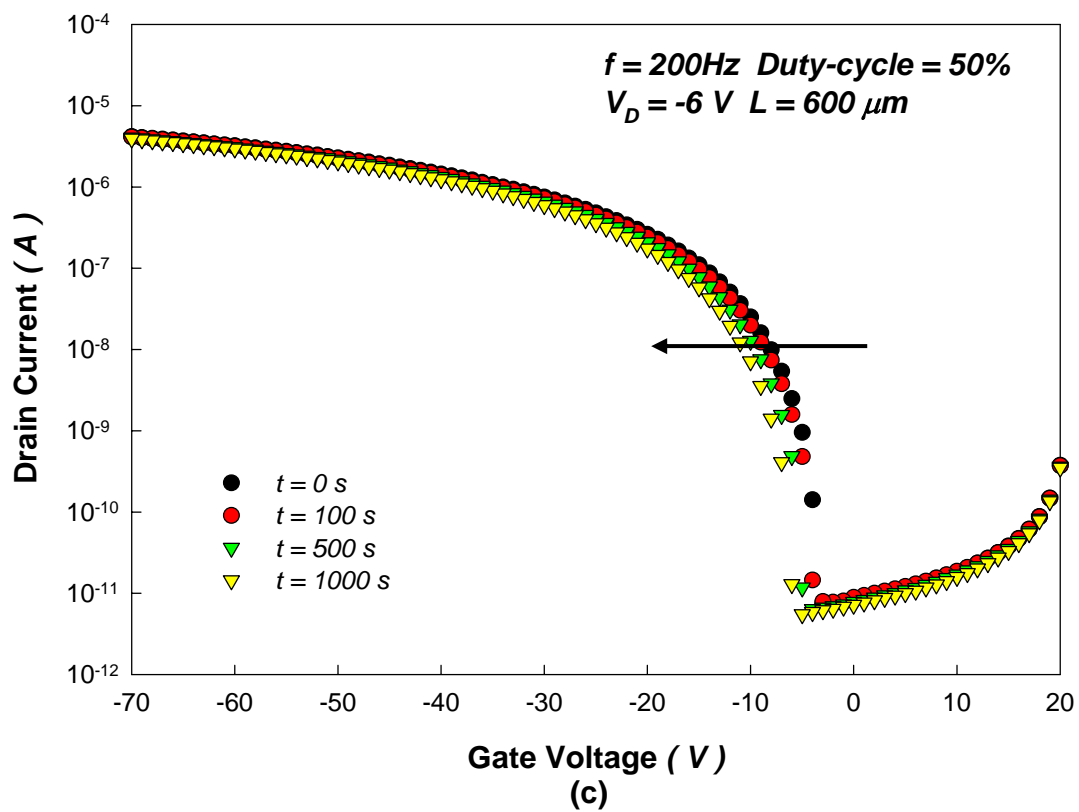


Fig. 3.27 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on thermal oxide during ON region AC bias-stress with a duty-cycle of 50% and frequency of
(a) 5 Hz (b) 50Hz (c) 200Hz

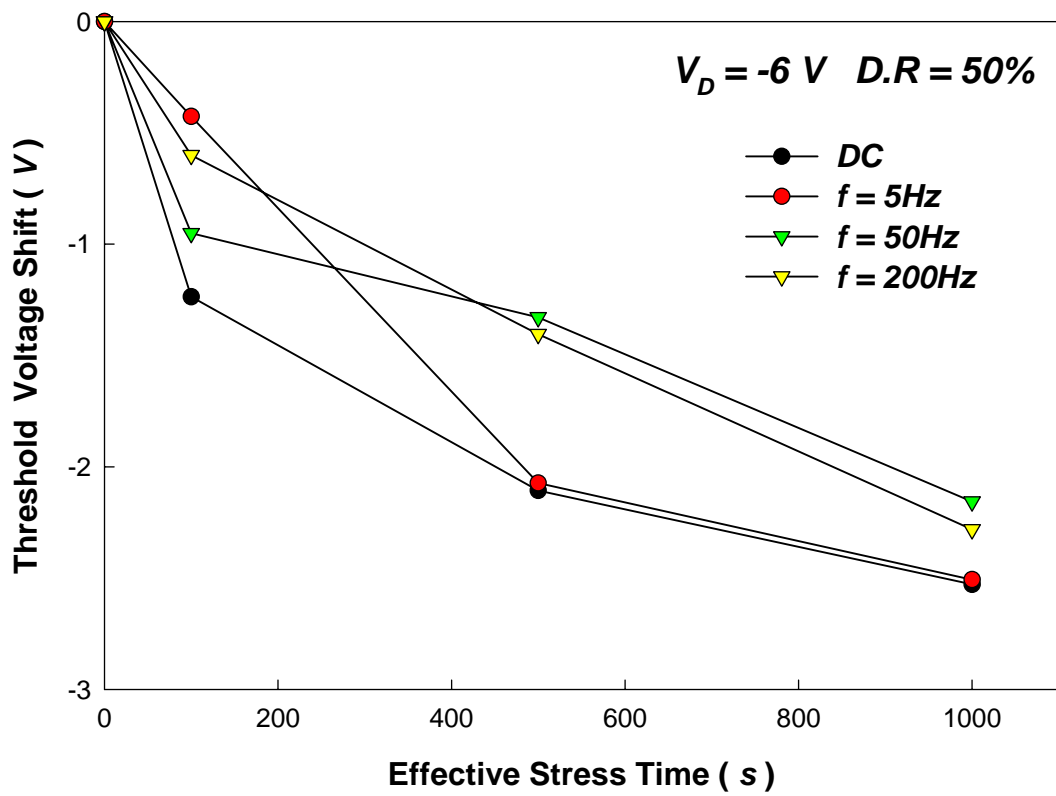


Fig. 3.28 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different frequencies.

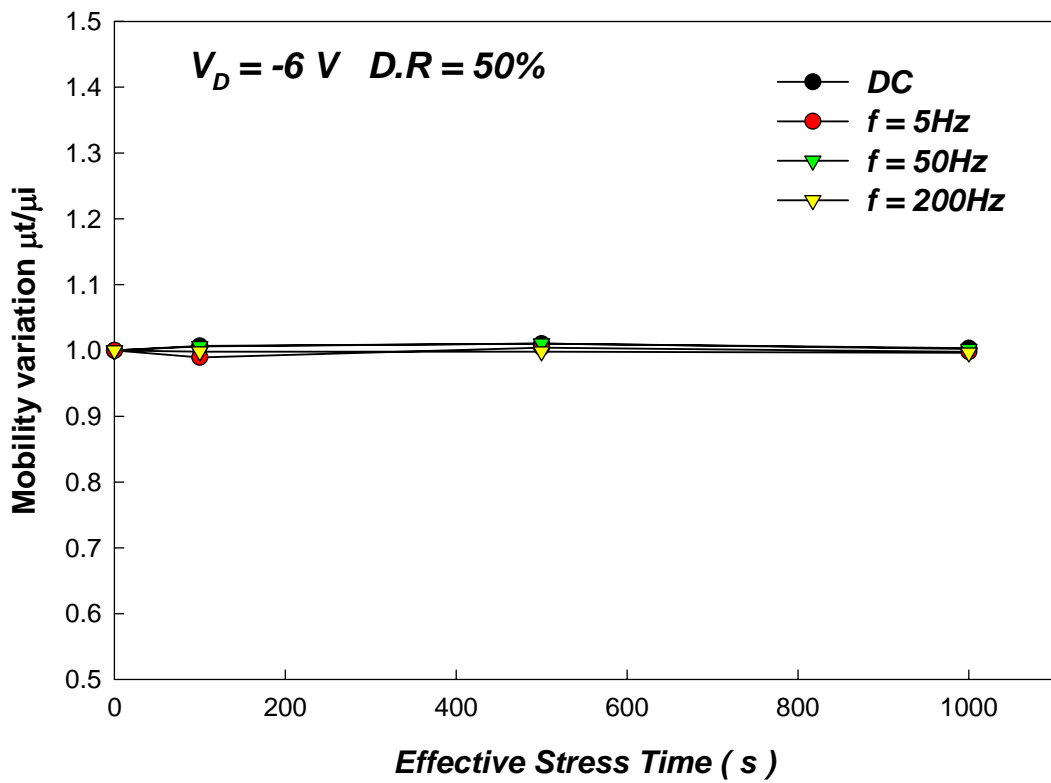
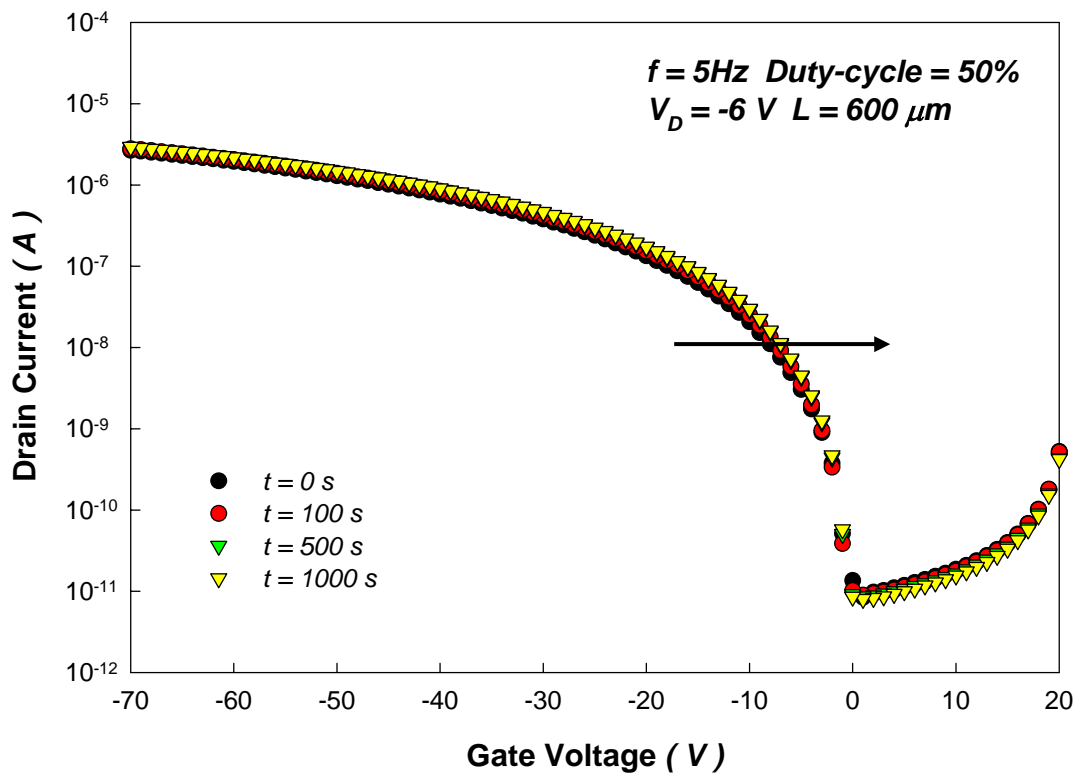
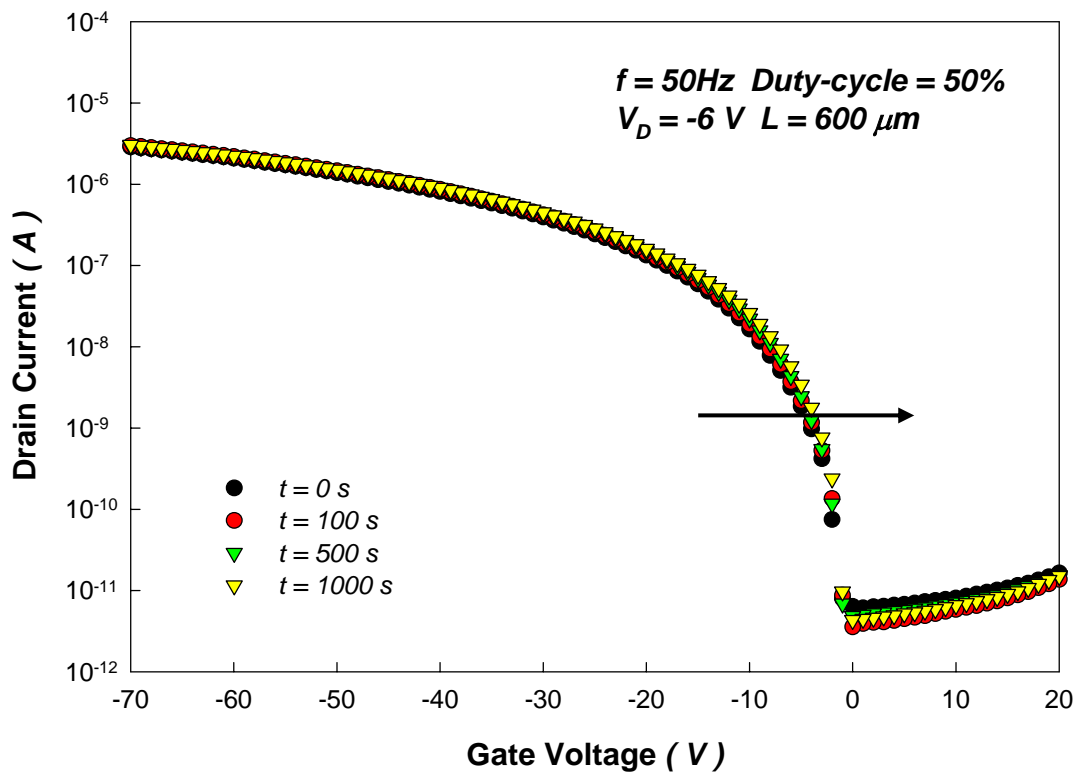


Fig. 3.29 Mobility variation versus effective stress time



(a)



(b)

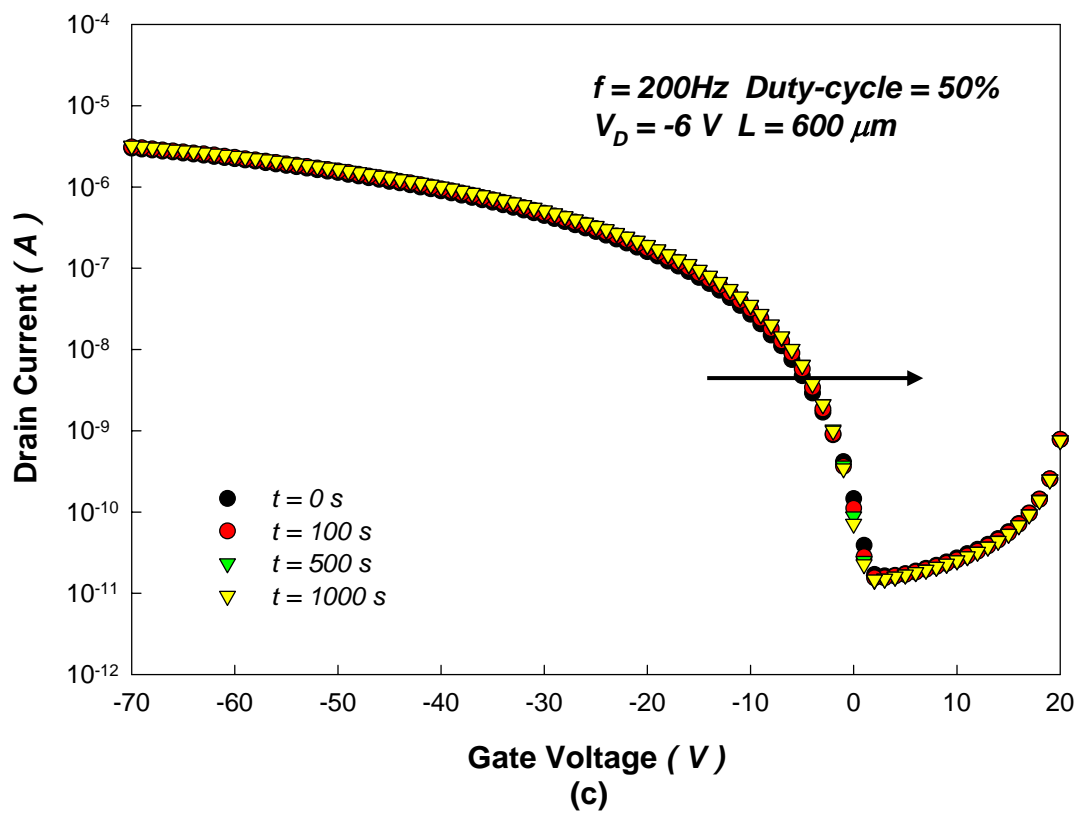


Fig. 3.30 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on thermal oxide during OFF region AC bias-stress with a duty-cycle of 50% and frequency of

(a) 5 Hz (b) 50Hz (c) 200Hz.

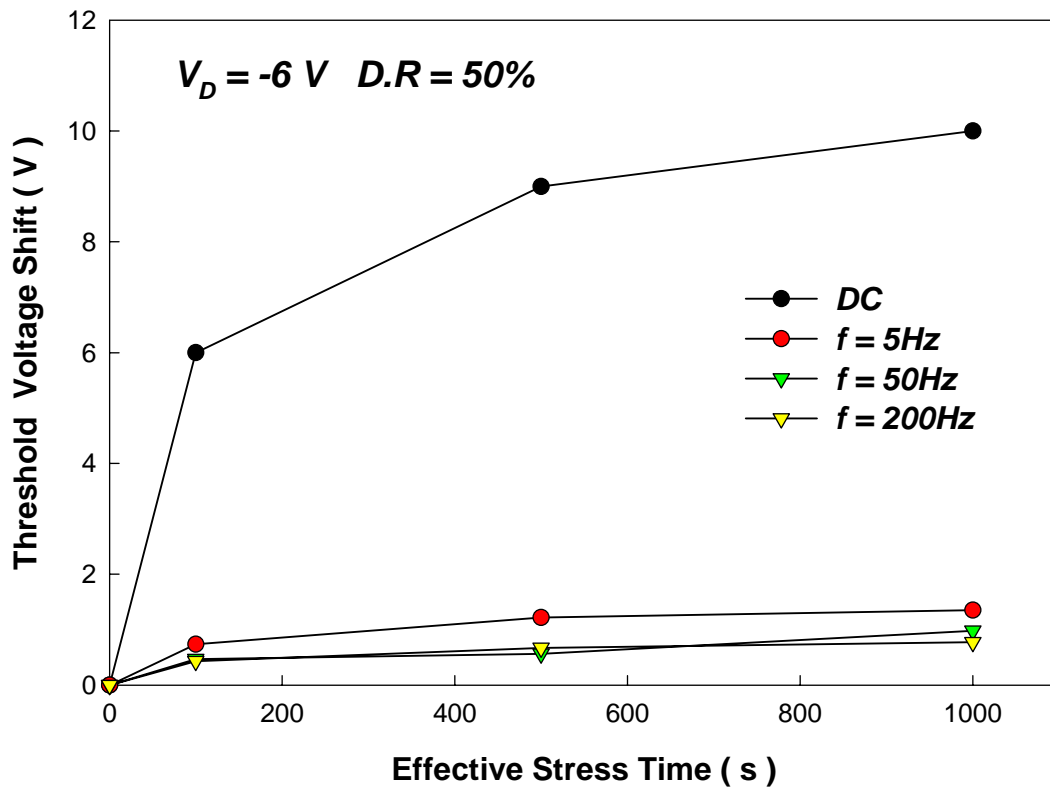


Fig. 3.31 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different frequencies.

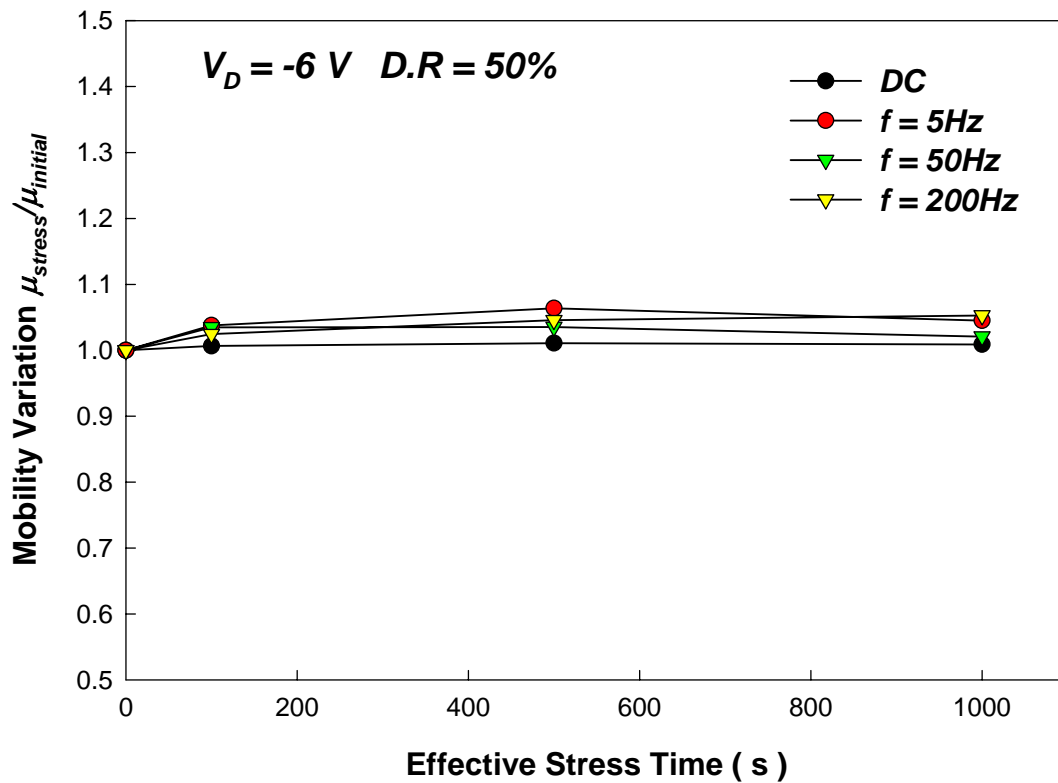


Fig. 3.32 Mobility variation versus effective stress time.

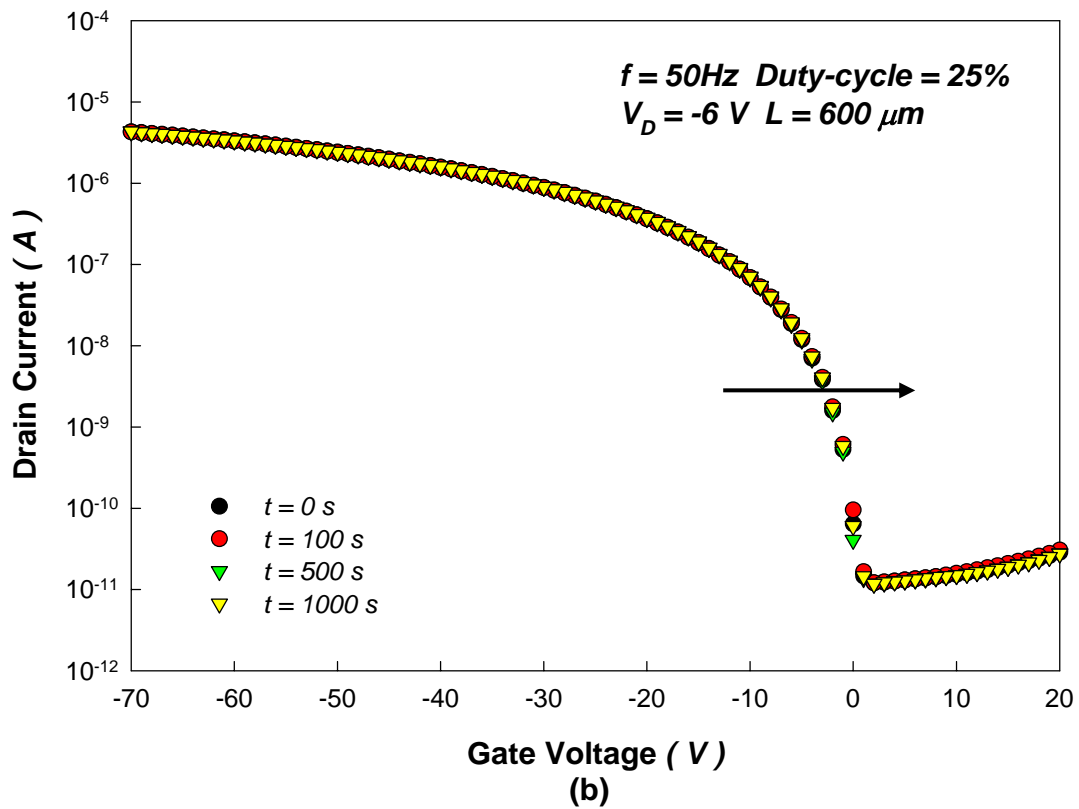
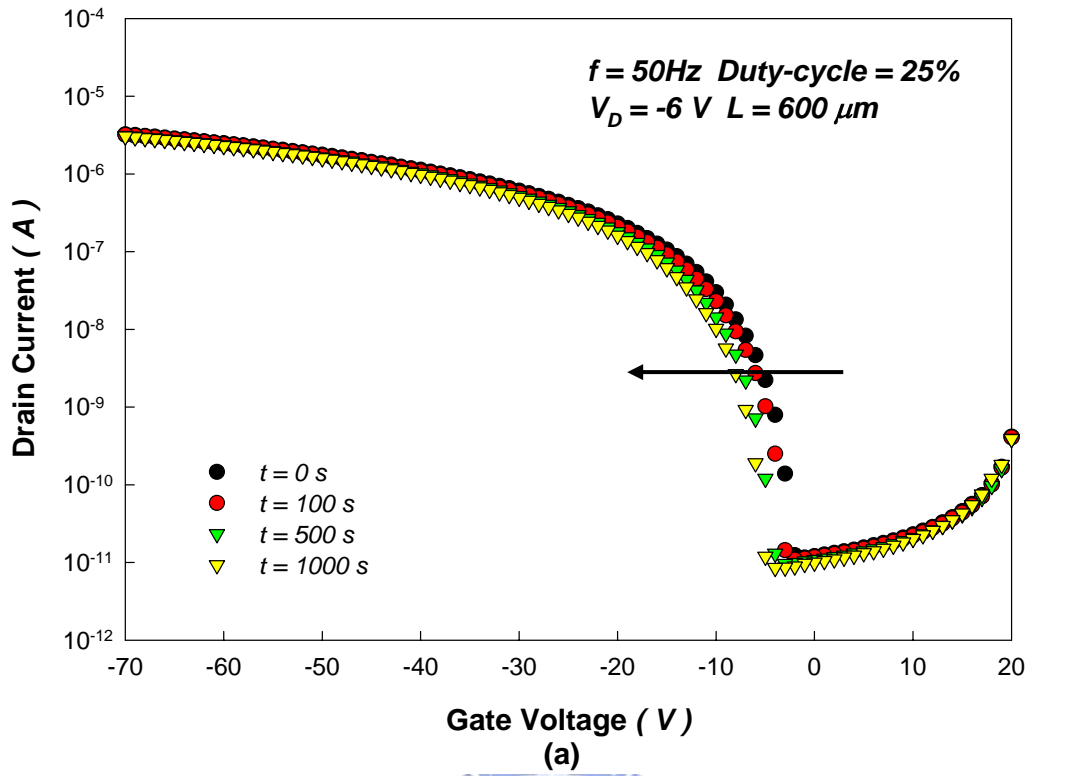


Fig. 3.33 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on thermal oxide during (a) ON region (b) OFF region AC bias-stress with a duty-cycle of 25% and frequency of 50Hz.

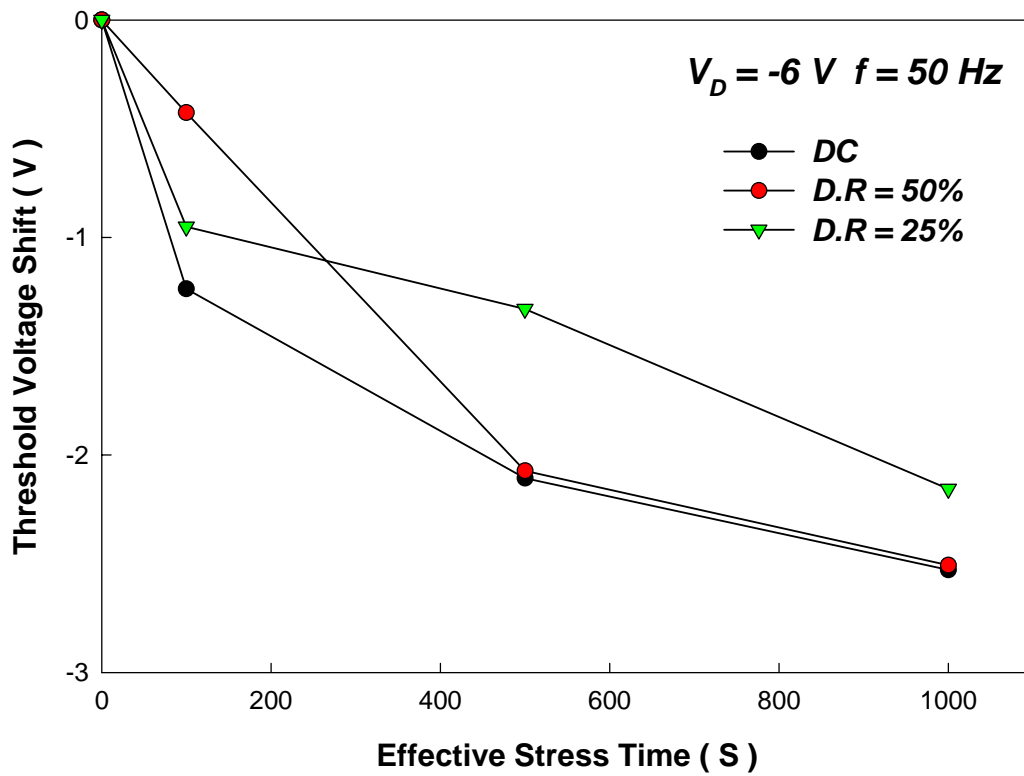


Fig. 3.34 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

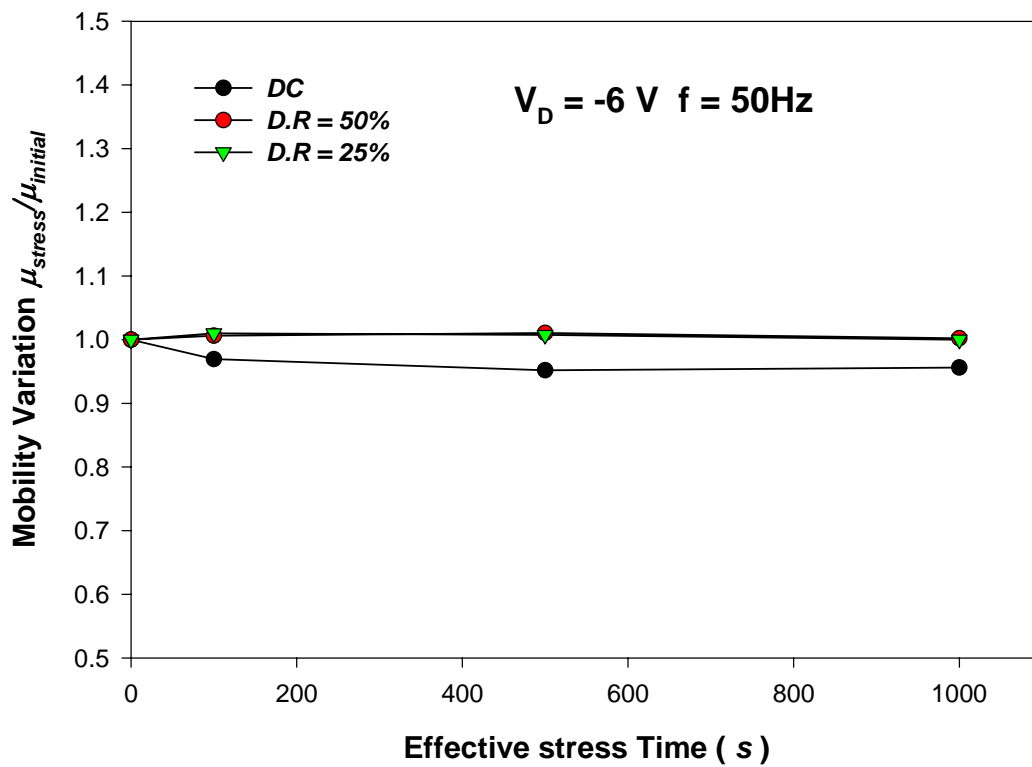


Fig. 3.35 Mobility variation versus effective stress time.

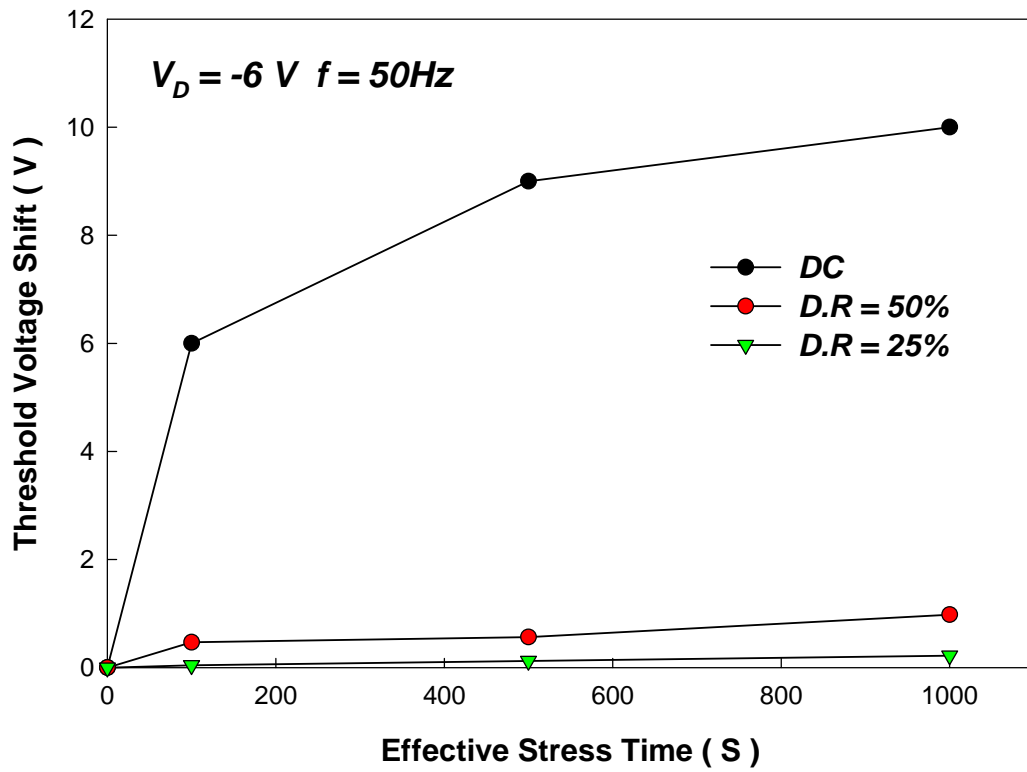


Fig. 3.36 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

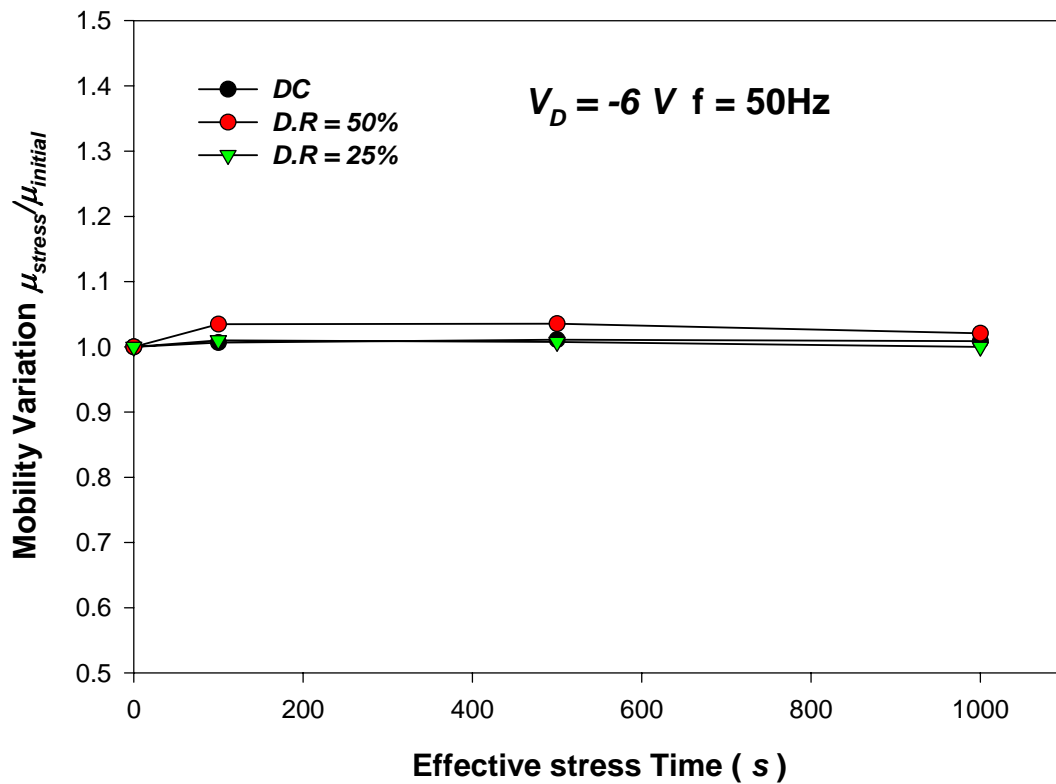


Fig. 3.37 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

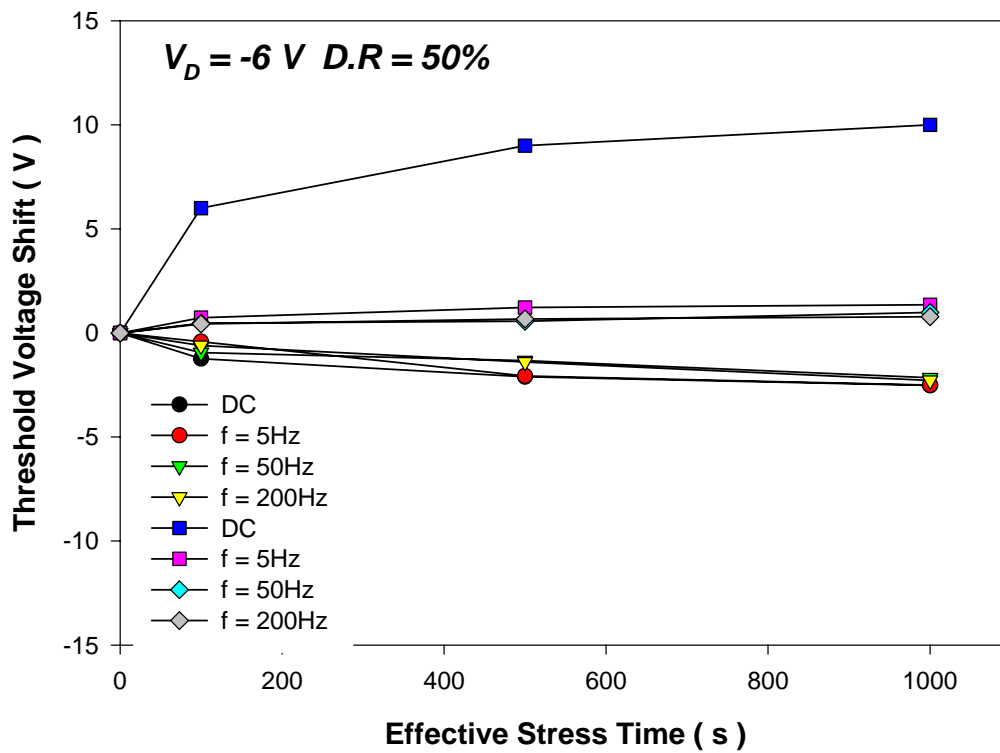


Fig. 3.38 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different frequencies.

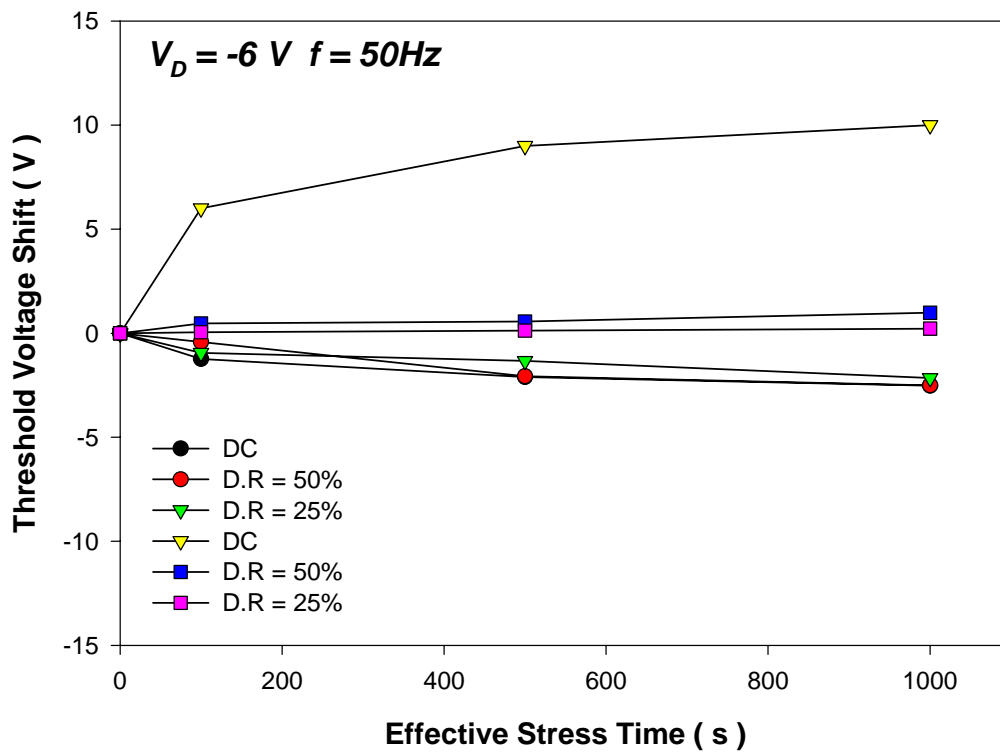


Fig. 3.39 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different duty-cycles.

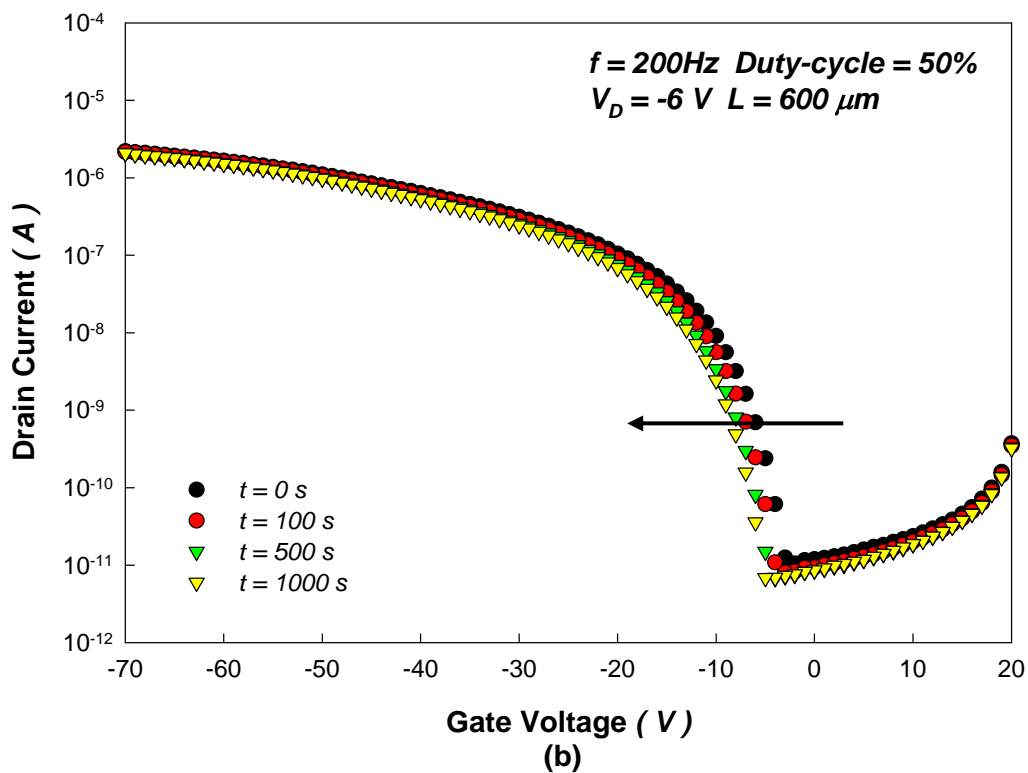
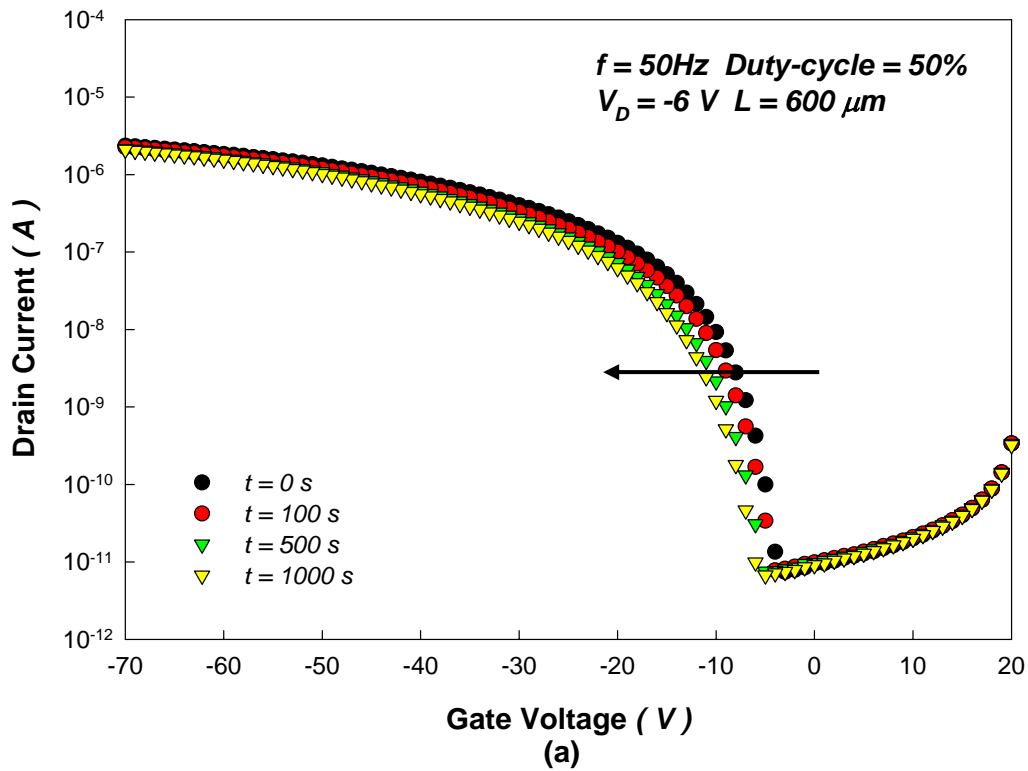


Fig. 3.40 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on HMDS surface treatment during ON region AC bias-stress with a duty-cycle of 50% and frequency of (a) 50Hz (b) 200Hz.

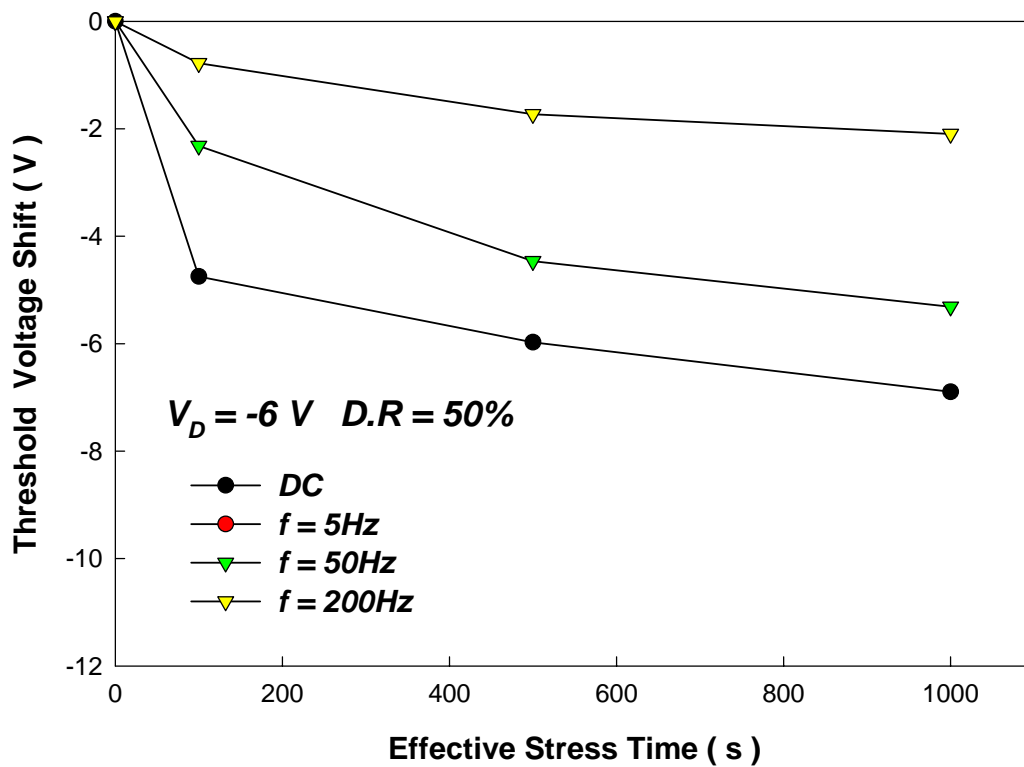


Fig. 3.41 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different frequencies.

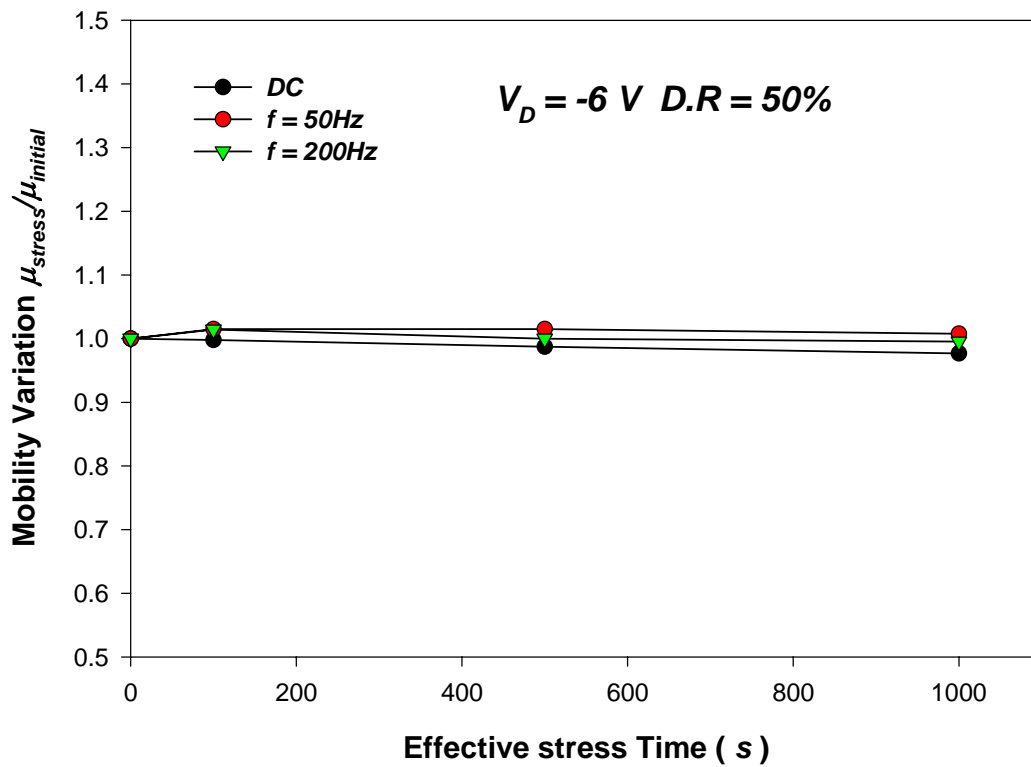


Fig. 3.42 Mobility variation versus effective stress time induced by ON region AC bias-stress with different frequencies.

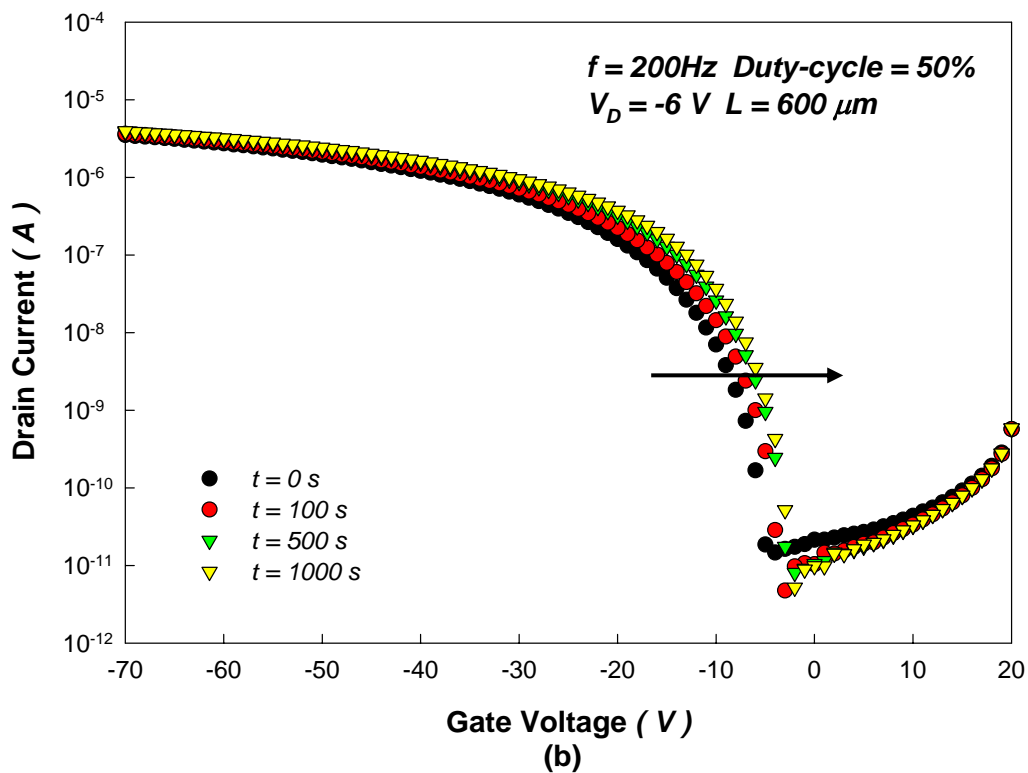
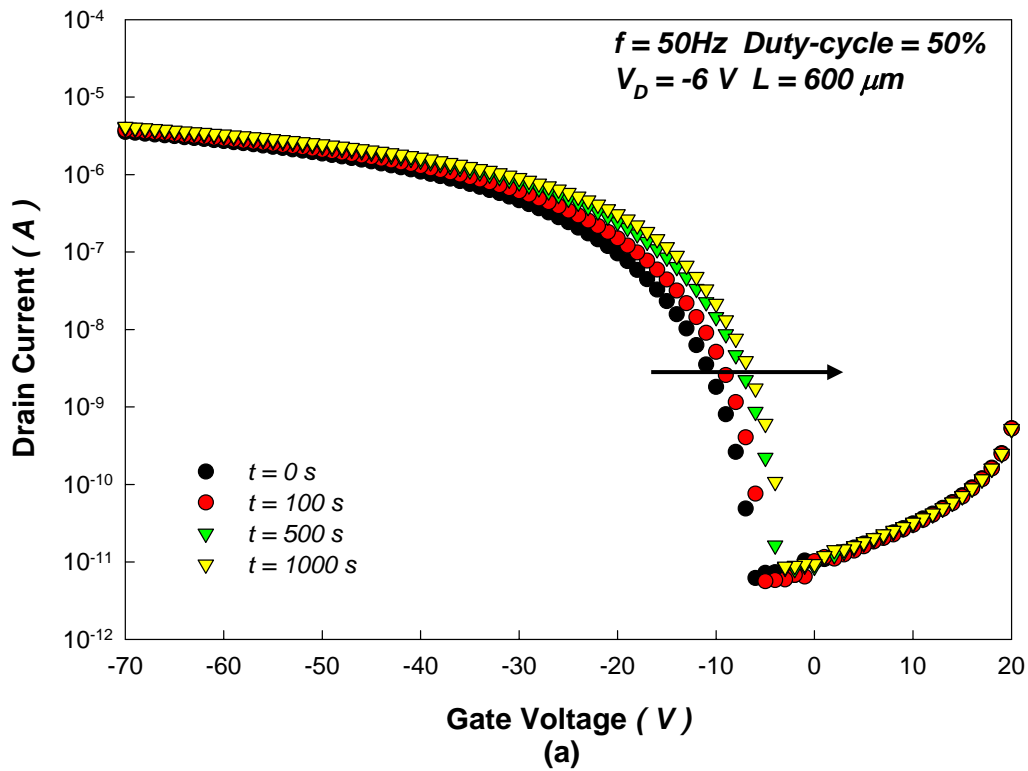


Fig. 3.43 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on HMDS surface treatment during OFF region AC bias-stress with a duty-cycle of 50% and frequency of (a) 50Hz (b) 200Hz.

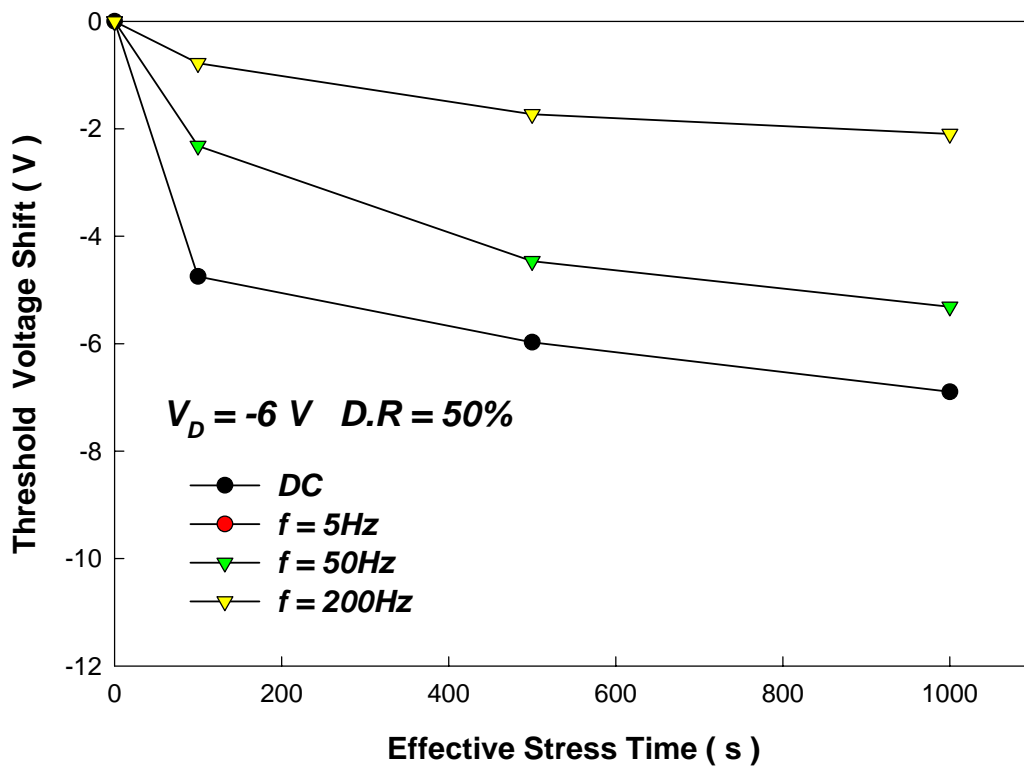


Fig. 3.44 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different frequencies.

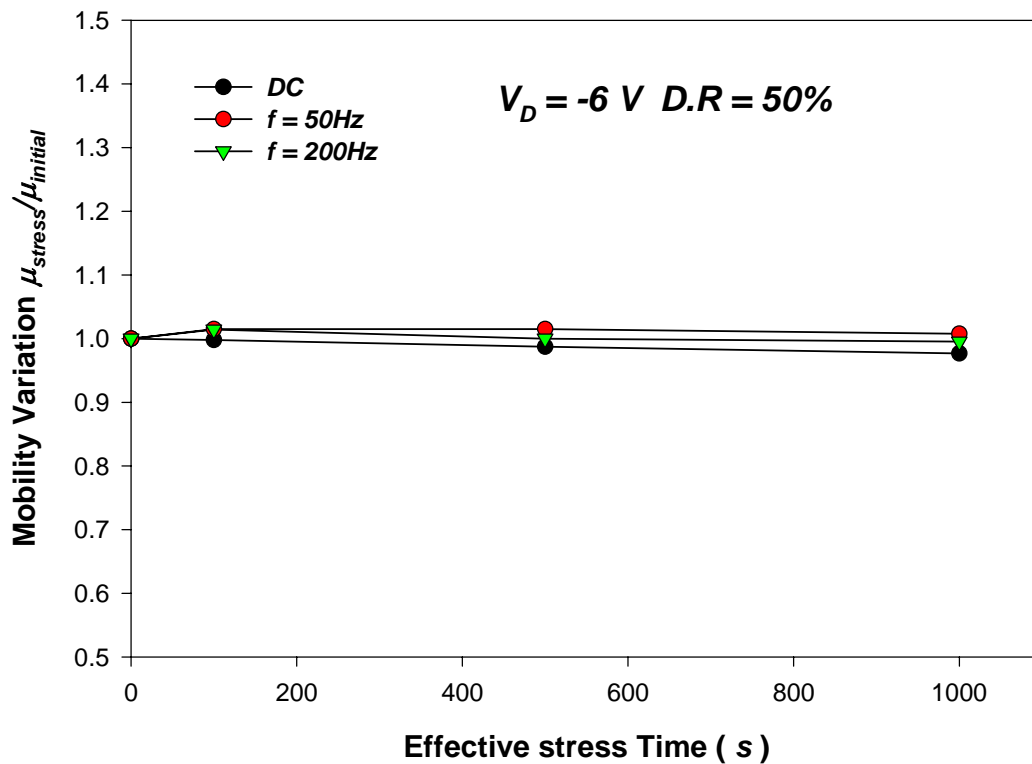


Fig. 3.45 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different frequencies.

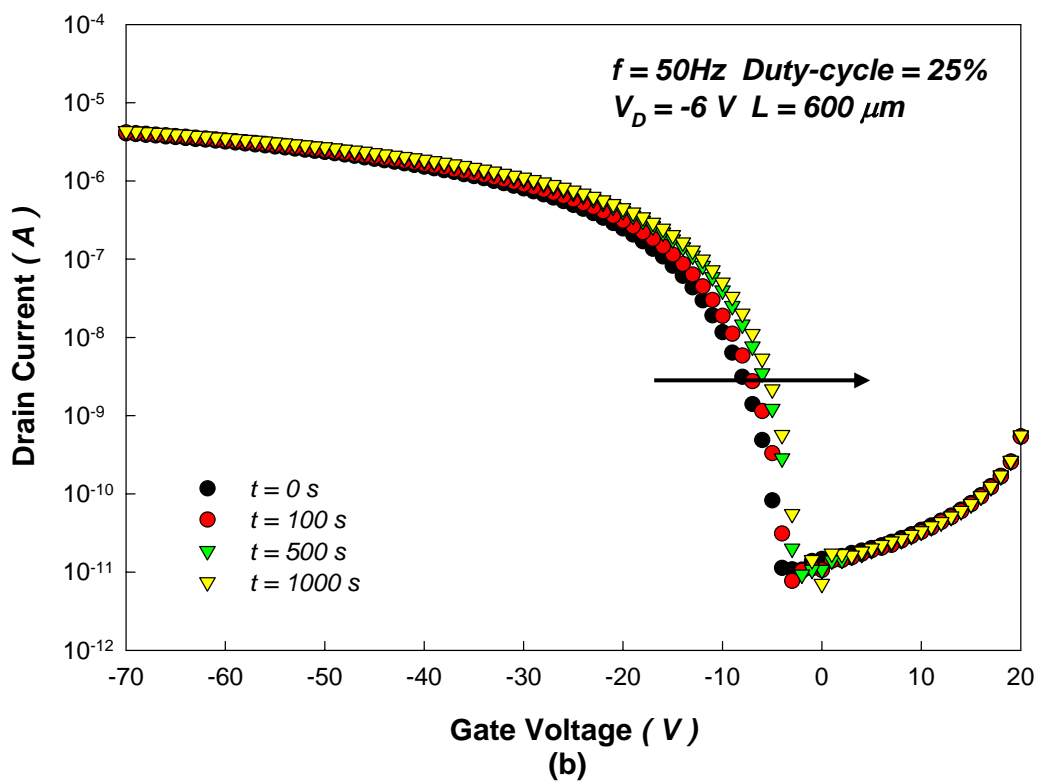
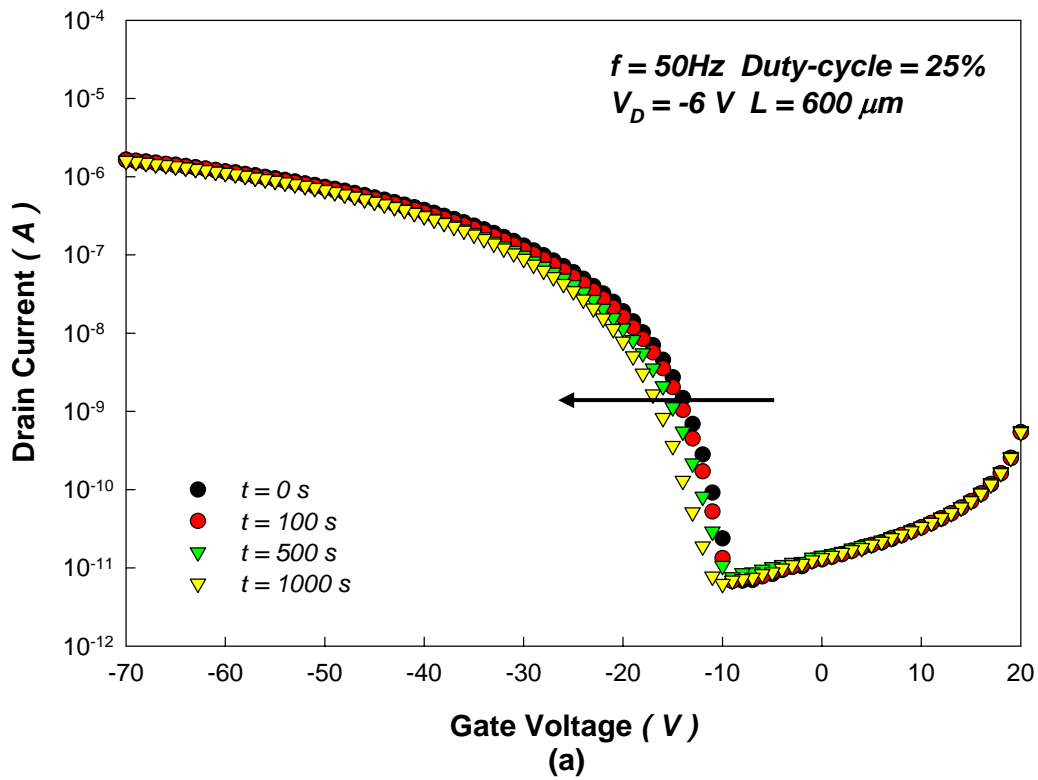


Fig. 3.46 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on HMDS during (a) ON region (b) OFF region AC bias-stress with a duty-cycle of 25% and frequency of 50Hz.

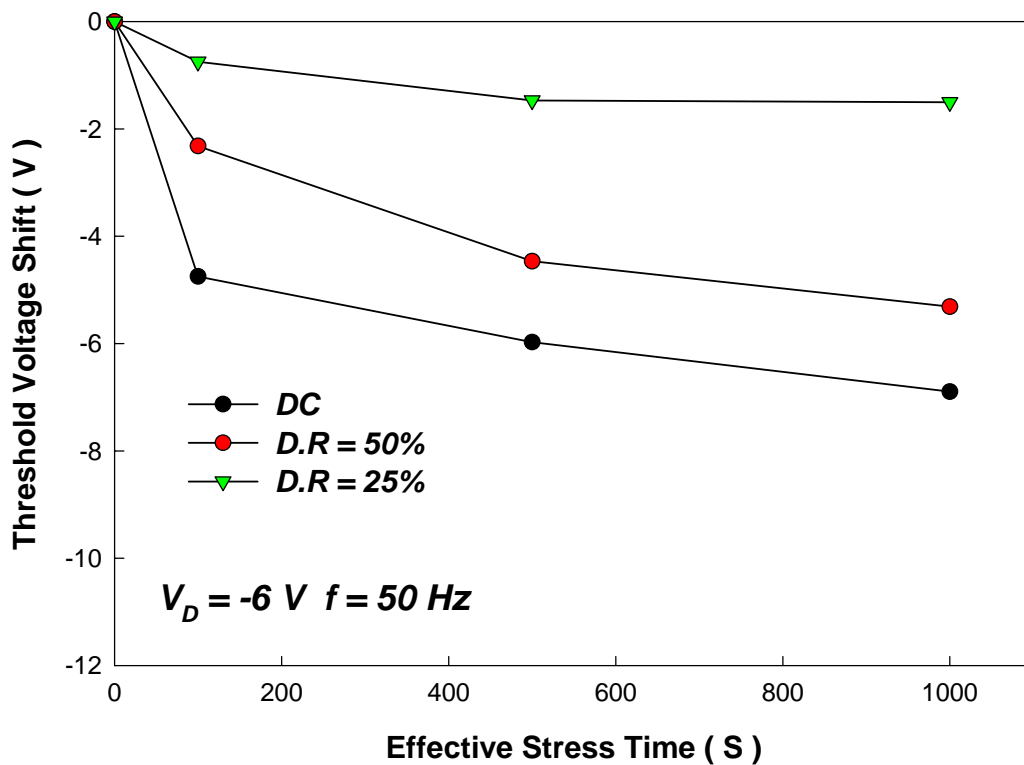


Fig. 3.47 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

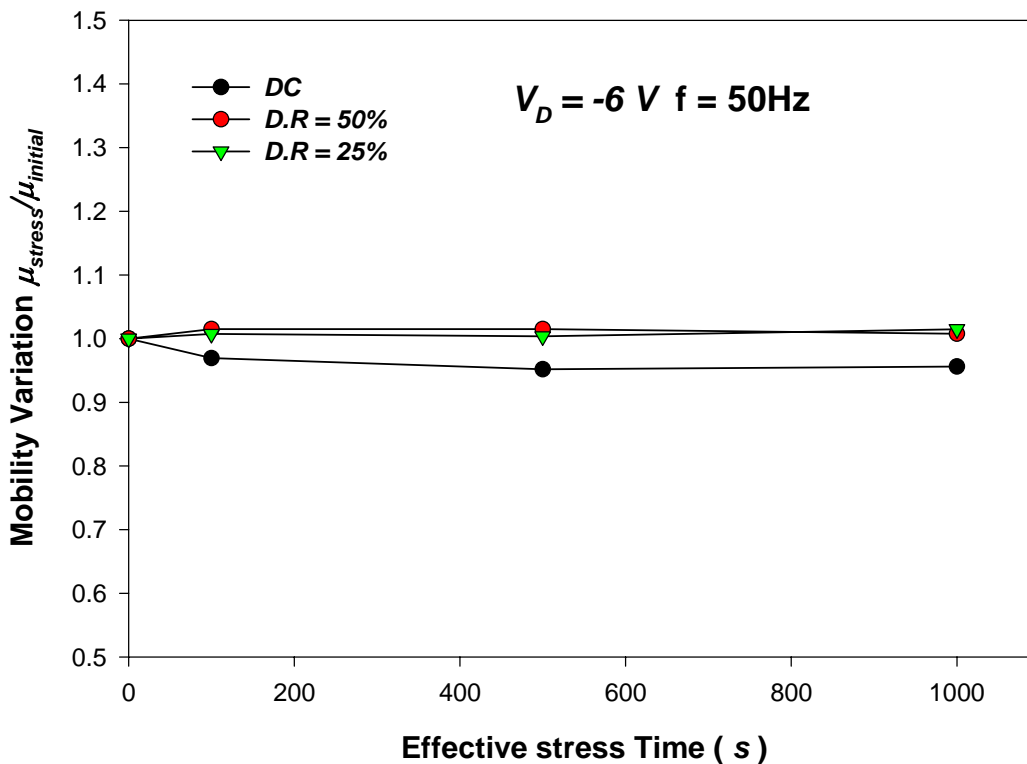


Fig. 3.48 Mobility variation versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

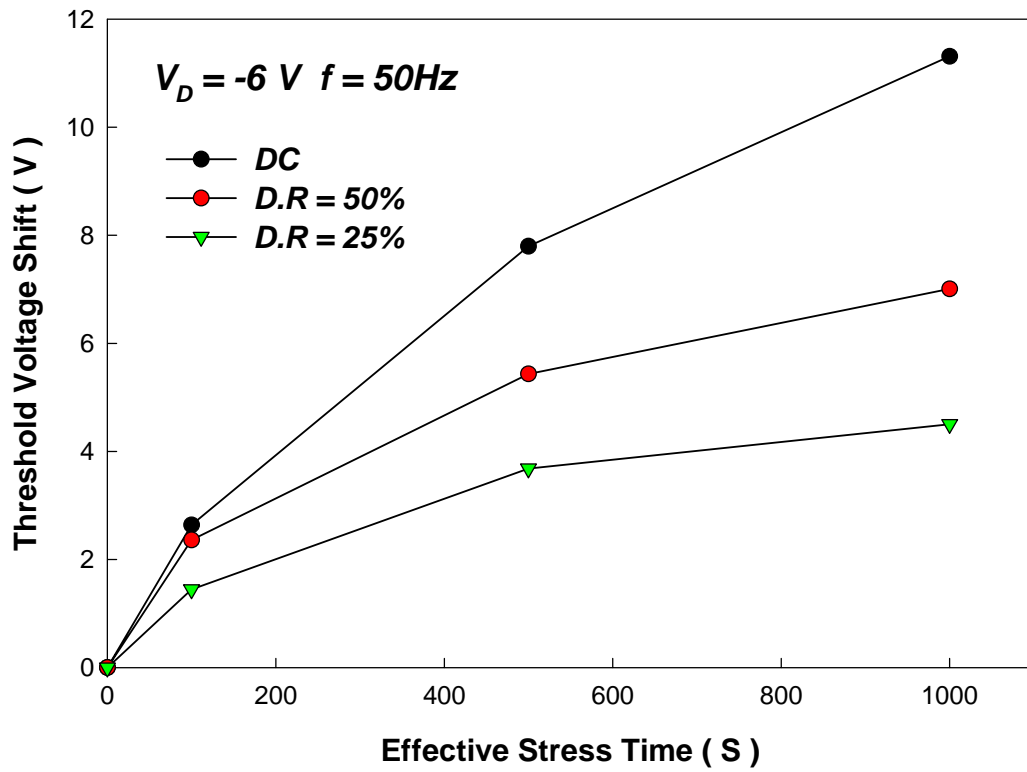


Fig. 3.49 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

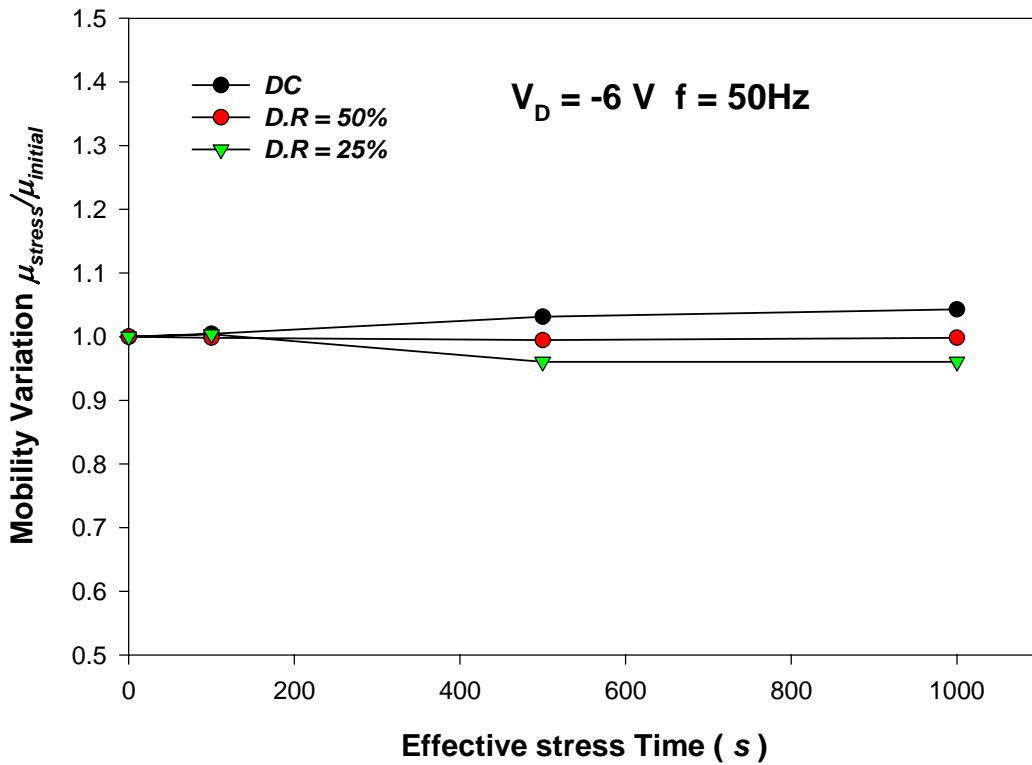


Fig. 3.50 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

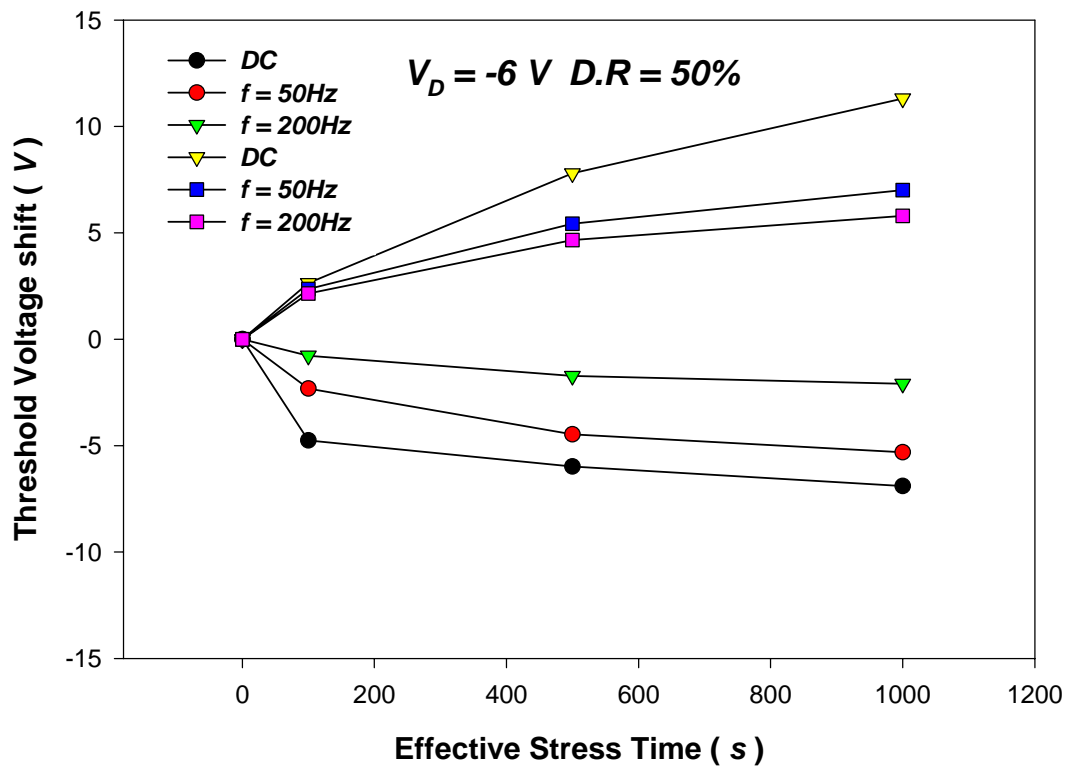


Fig. 3.51 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different frequencies.

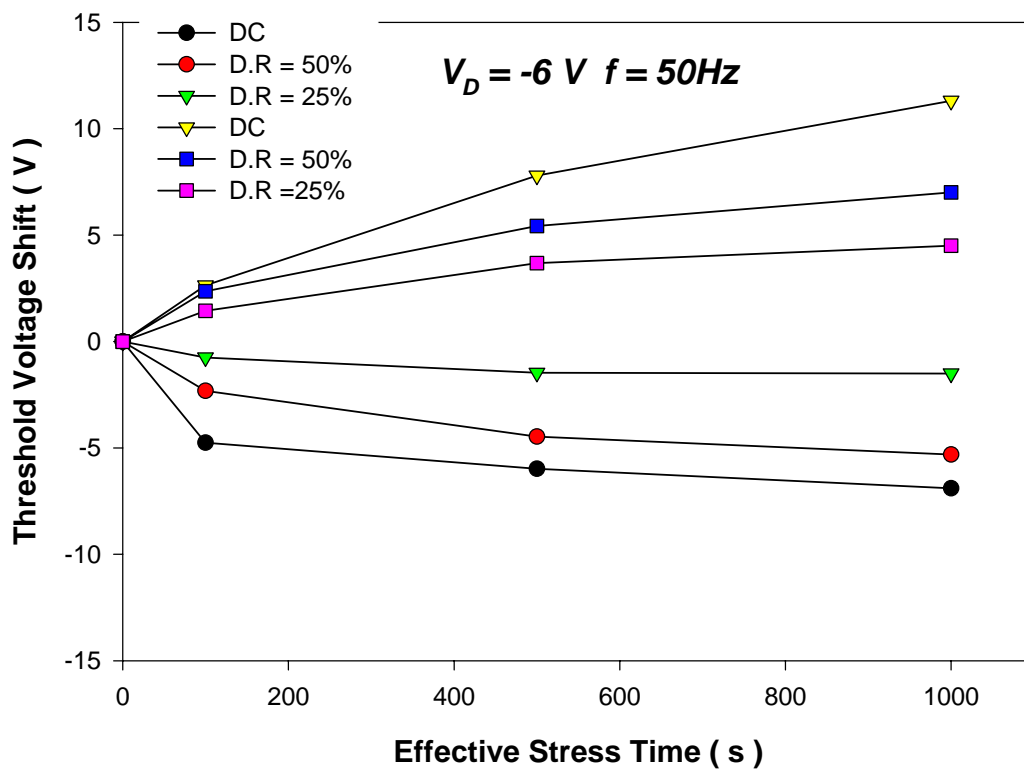
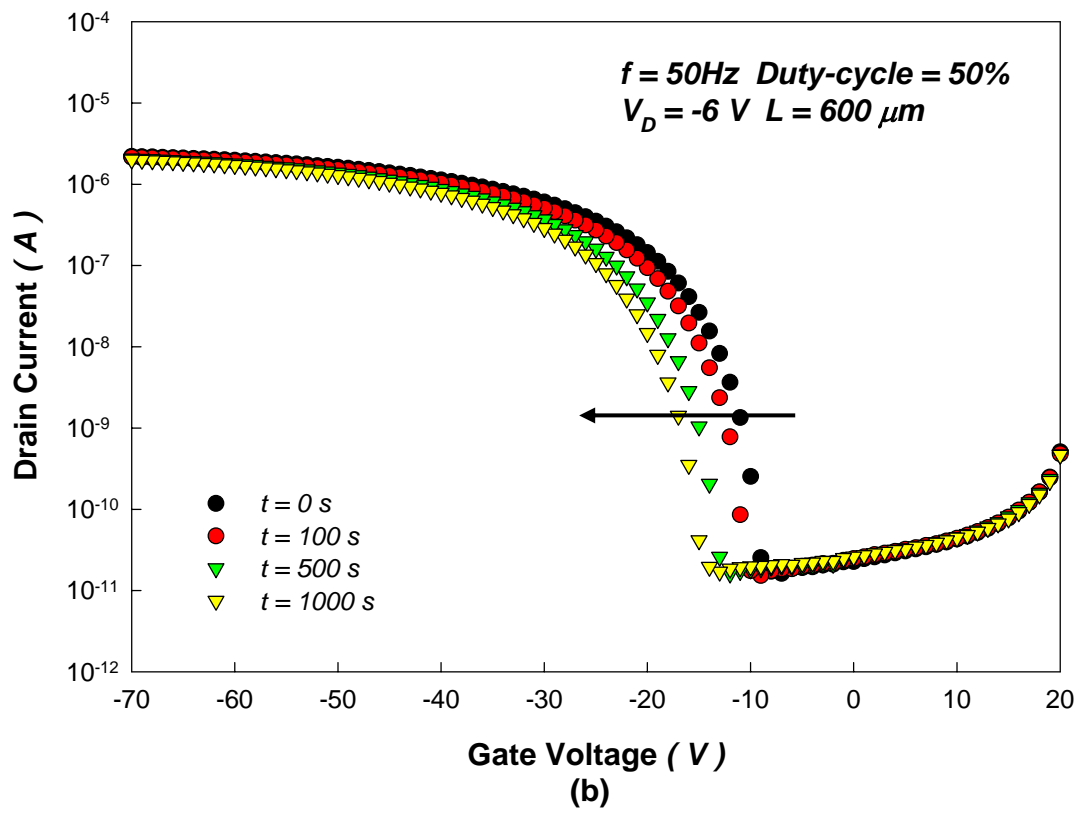
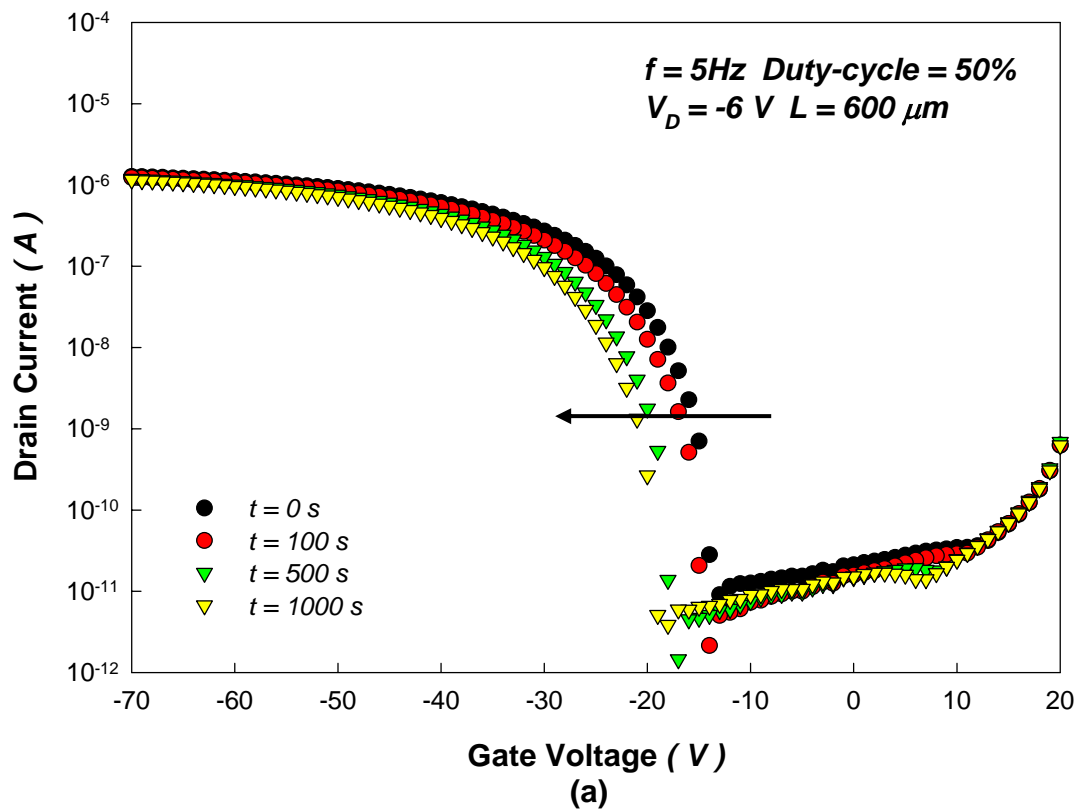


Fig. 3.52 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different duty-cycles.



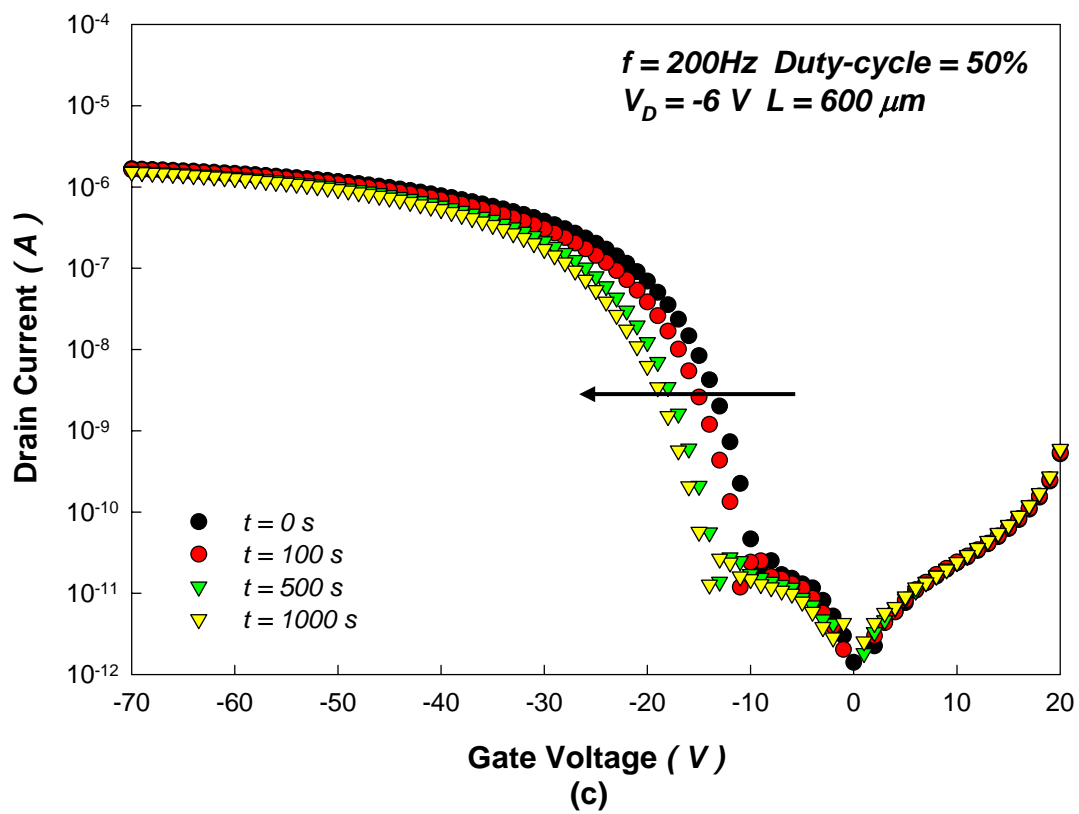


Fig. 3.53 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on ODMS surface treatment during ON region AC bias-stress with a duty-cycle of 50% and frequency of (a) 5Hz (b) 50Hz (c) 200Hz.

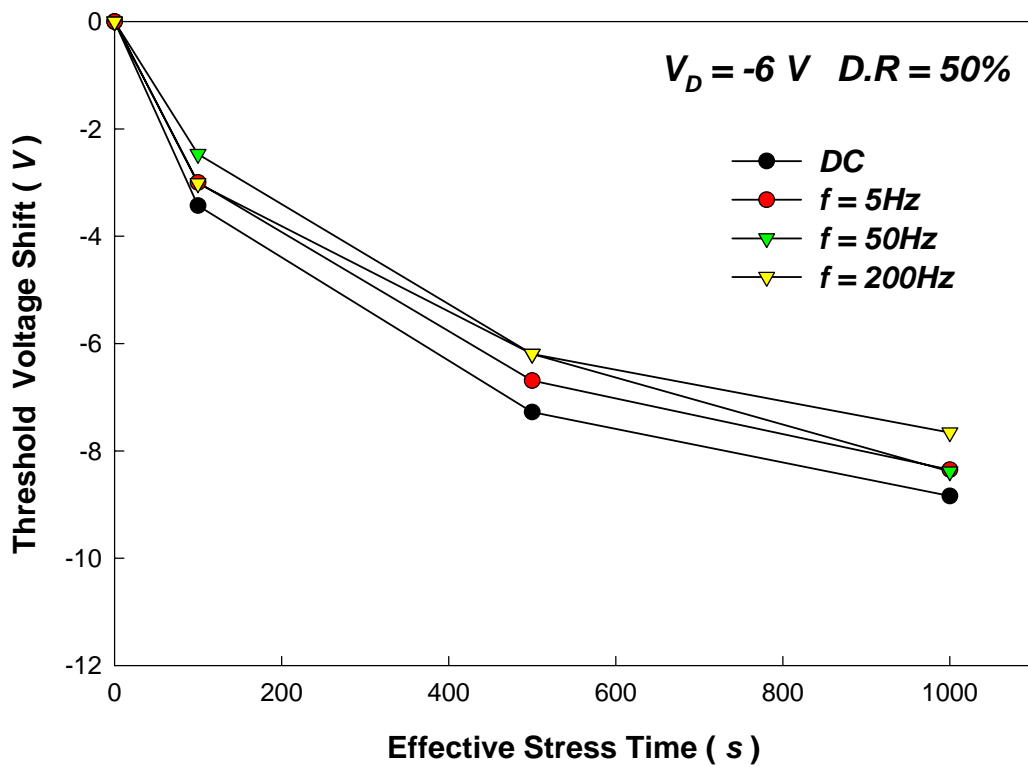


Fig. 3.54 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different frequencies.

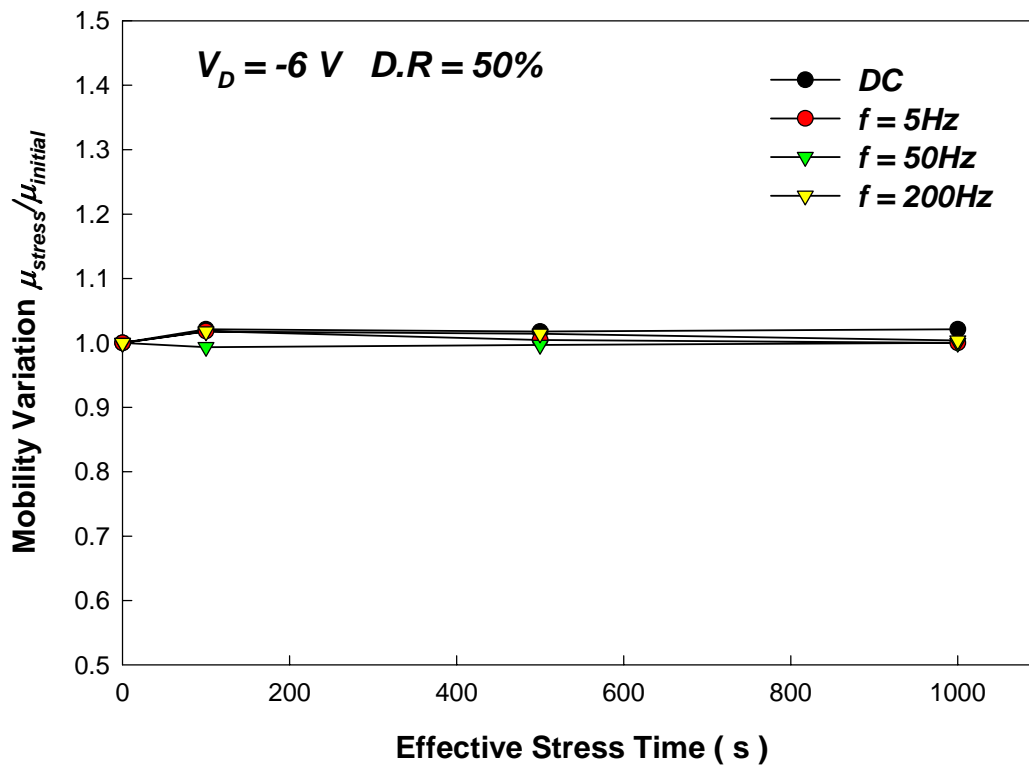
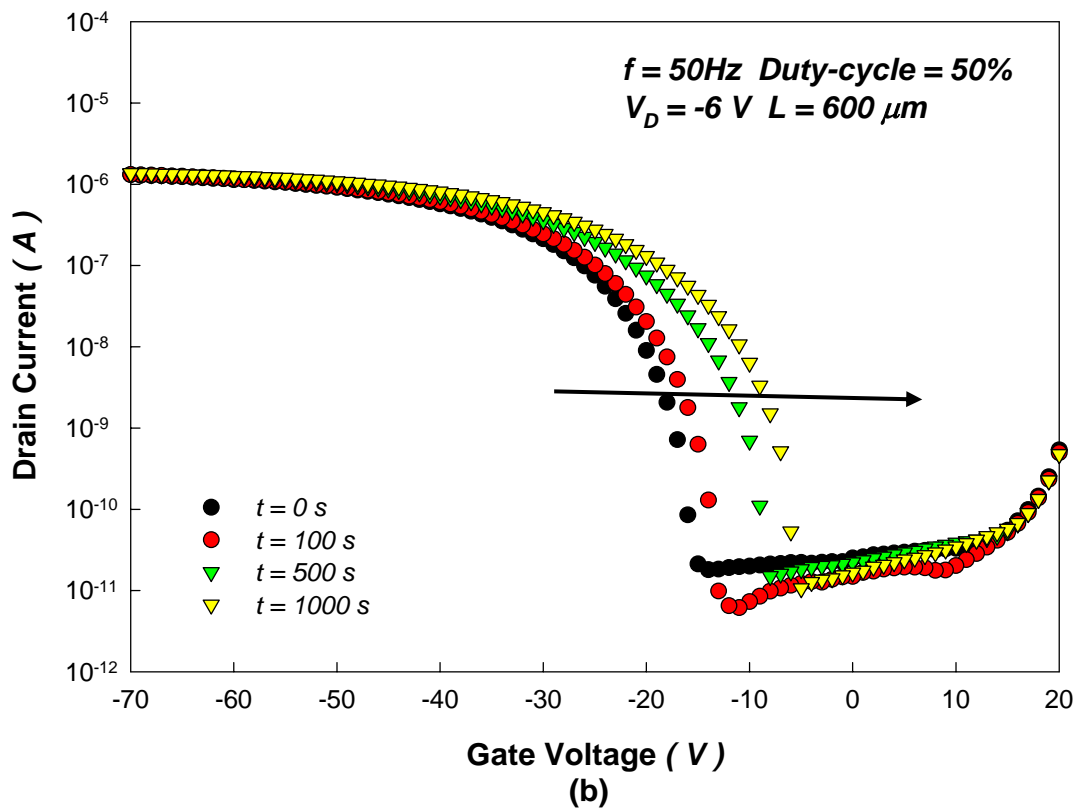
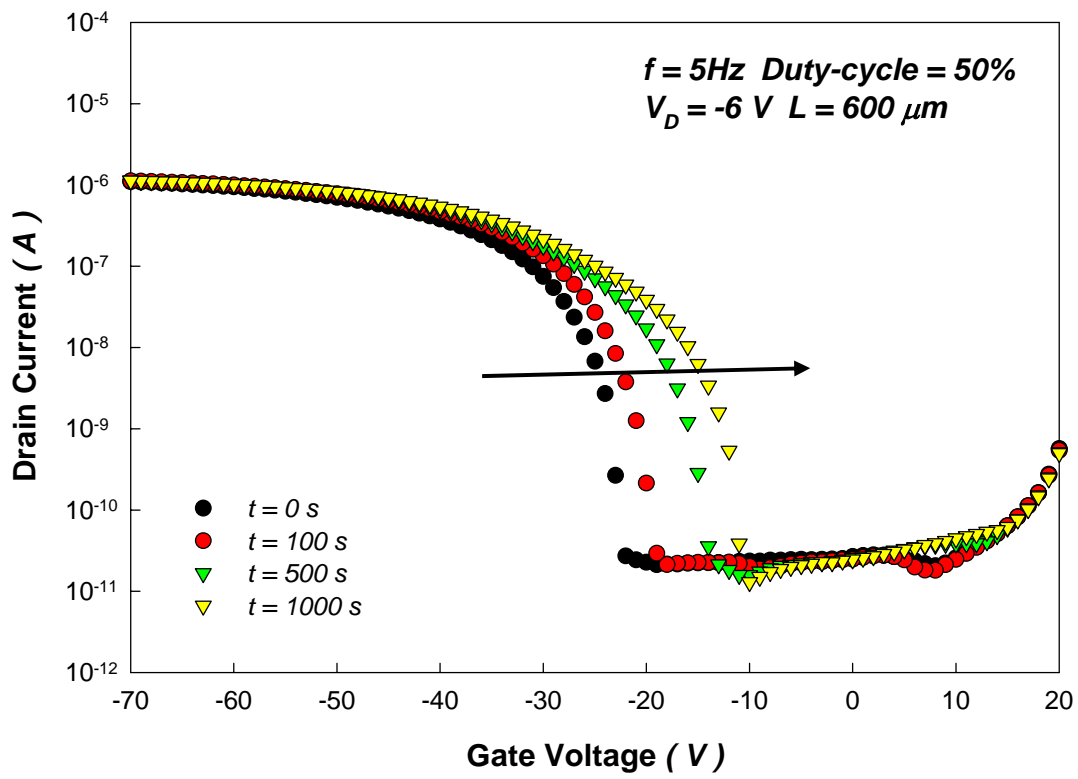


Fig. 3.55 Mobility variation versus effective stress time induced by ON region AC bias-stress with different frequencies.



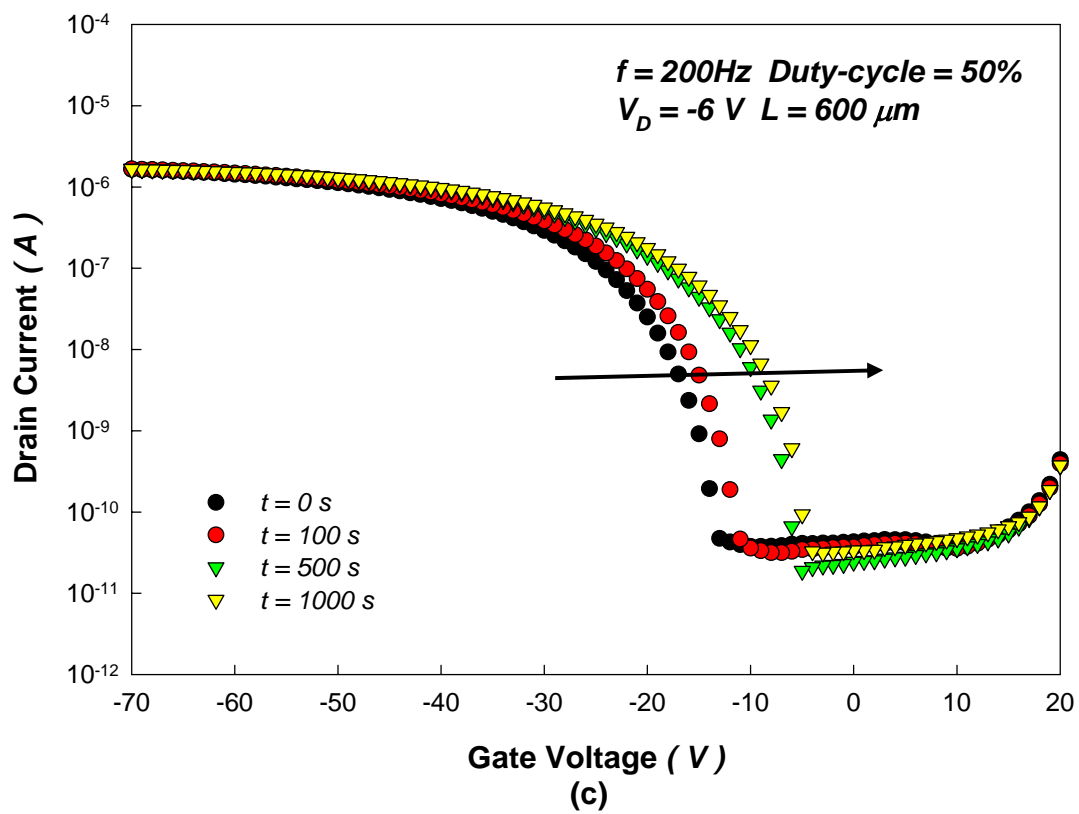


Fig. 3.56 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on ODMS surface treatment during OFF region AC bias-stress with a duty-cycle of 50% and frequency of (a) 5Hz (b) 50Hz (c) 200Hz.

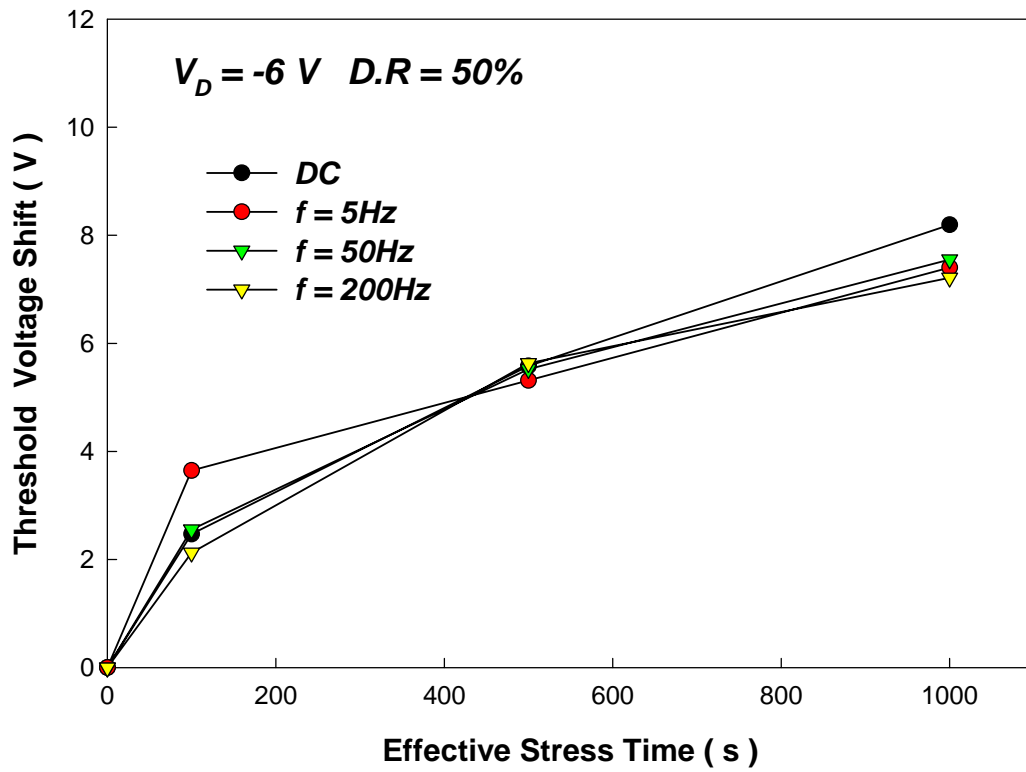


Fig. 3.57 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different frequencies.

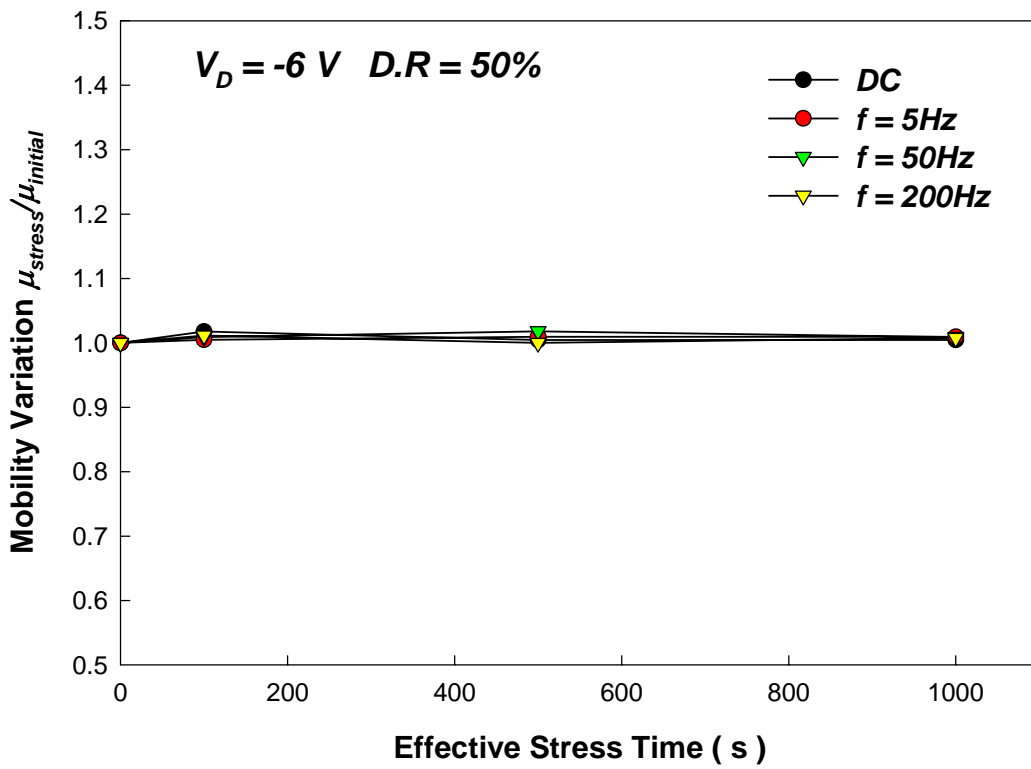


Fig. 3.58 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different frequencies.

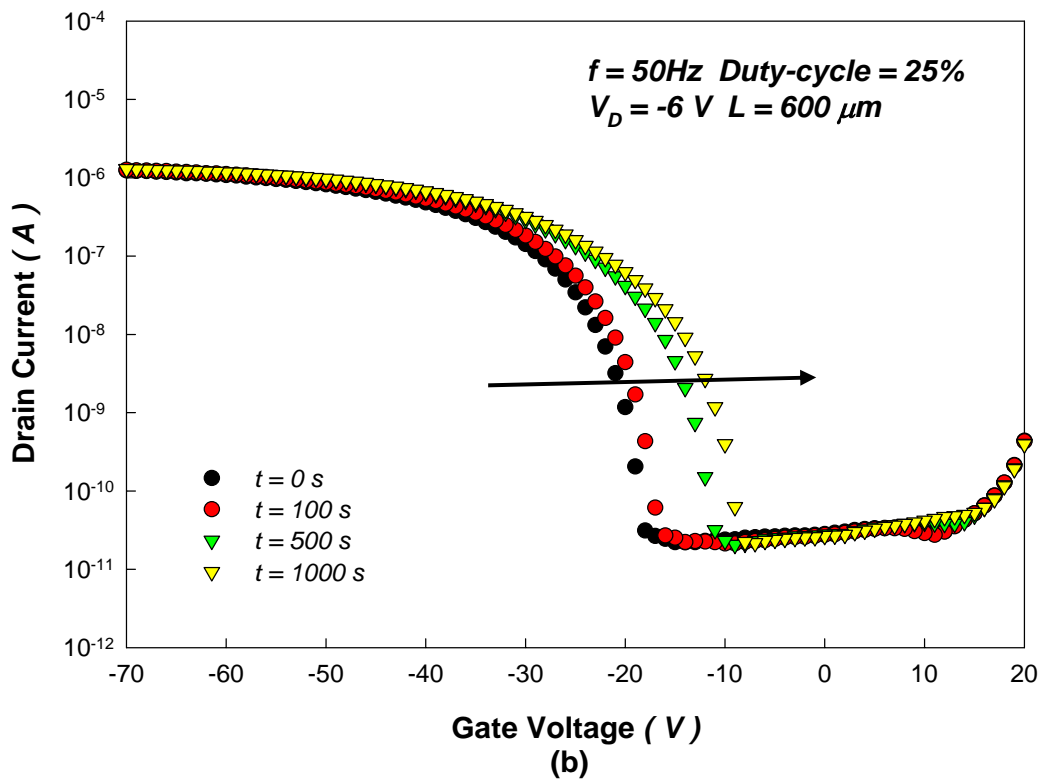
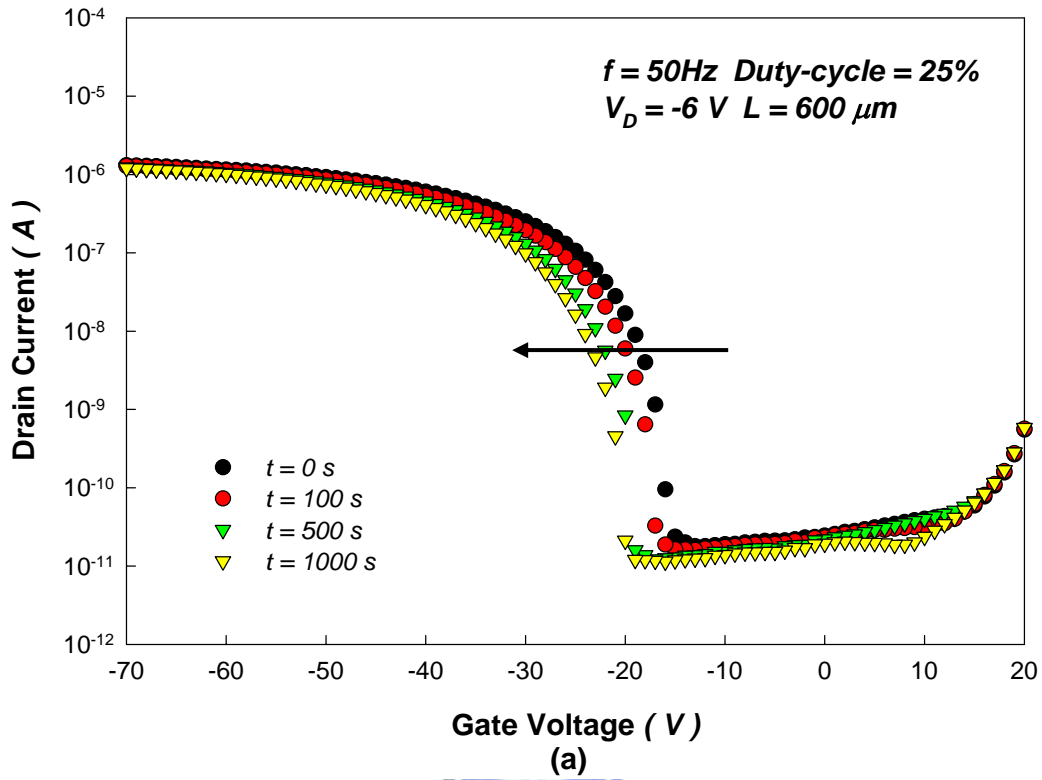


Fig. 3.59 Evolution I_D - V_G characteristic of pentacene-based TFTs deposited on ODMS treatment during (a) ON region (b) OFF region AC bias-stress with a duty-cycle of 25% and frequency of 50Hz.

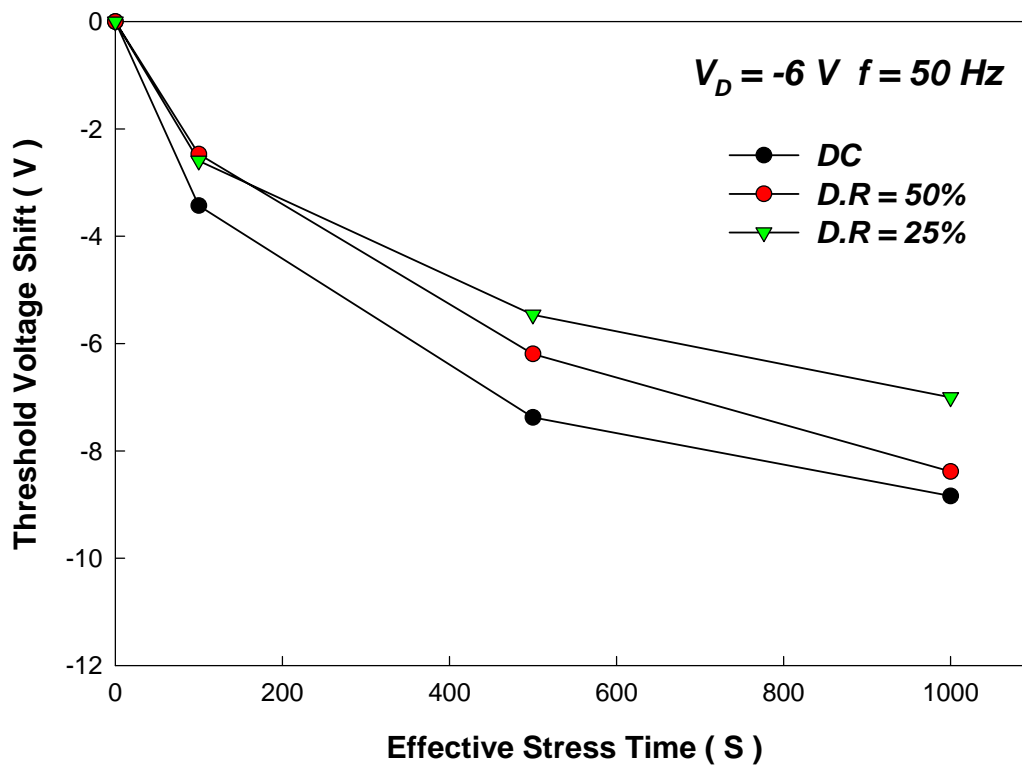


Fig. 3.60 Threshold voltage shift versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

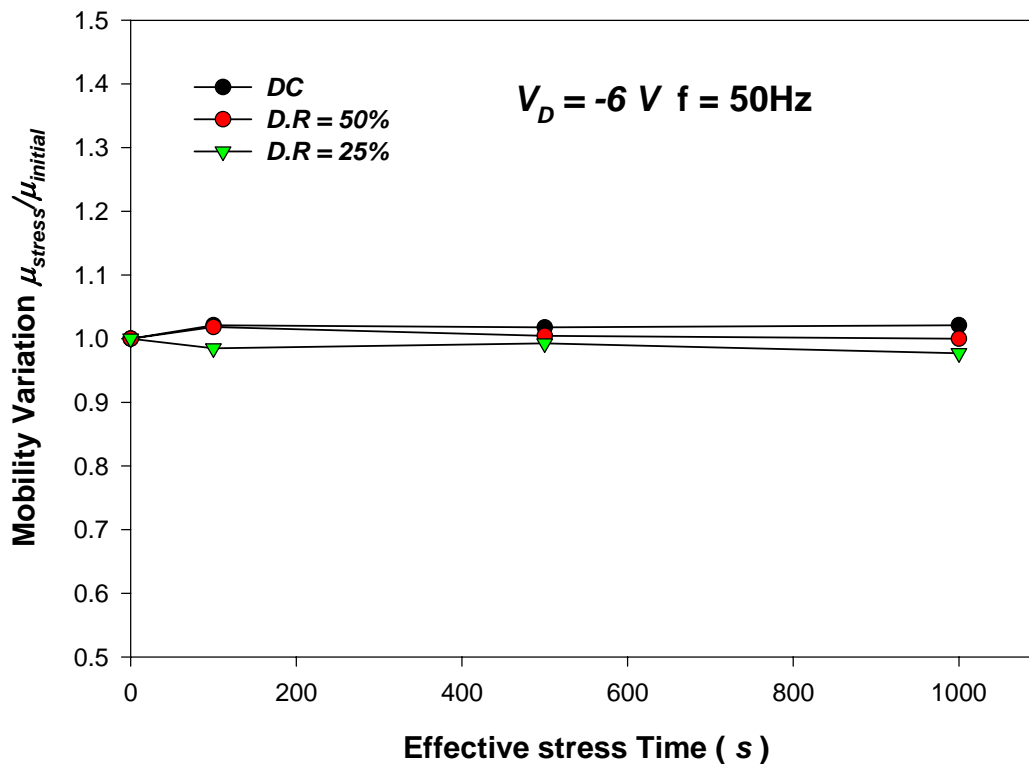


Fig. 3.61 Mobility variation versus effective stress time induced by ON region AC bias-stress with different duty-cycles.

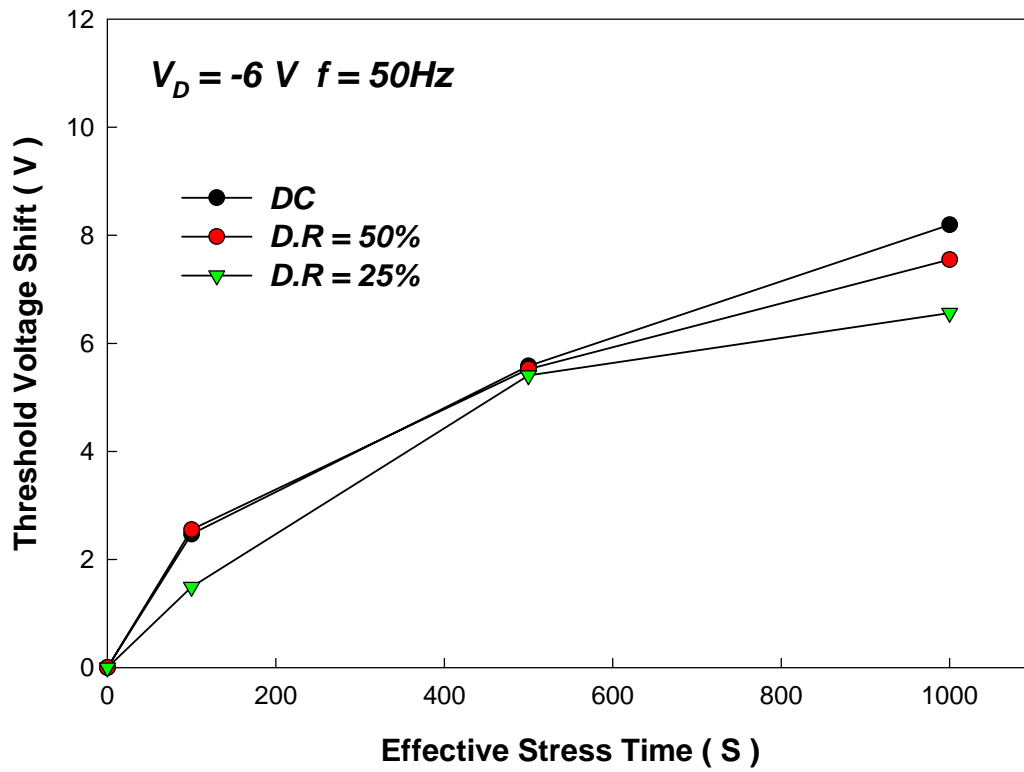


Fig. 3.62 Threshold voltage shift versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

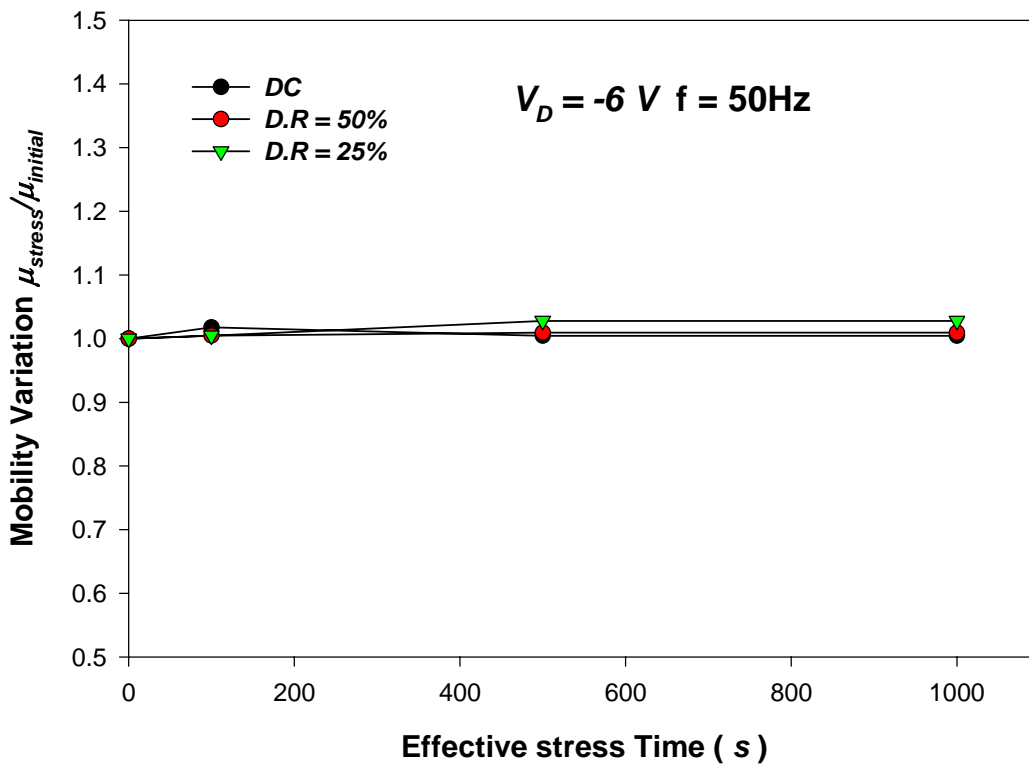


Fig. 3.63 Mobility variation versus effective stress time induced by OFF region AC bias-stress with different duty-cycles.

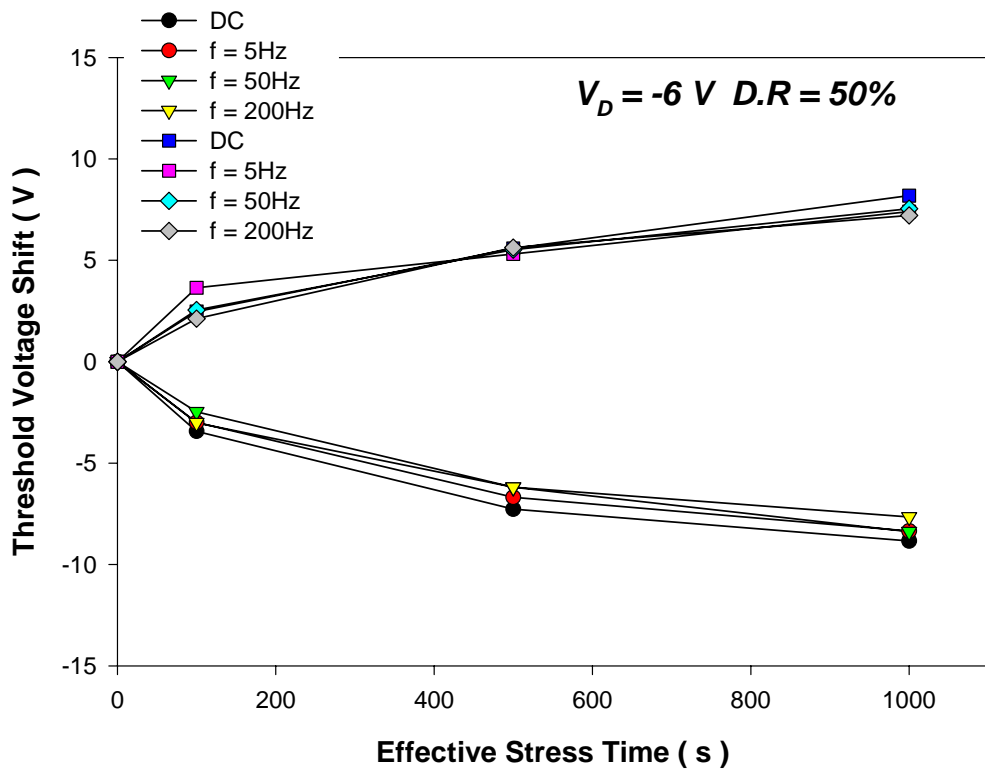


Fig. 3.64 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different frequencies.

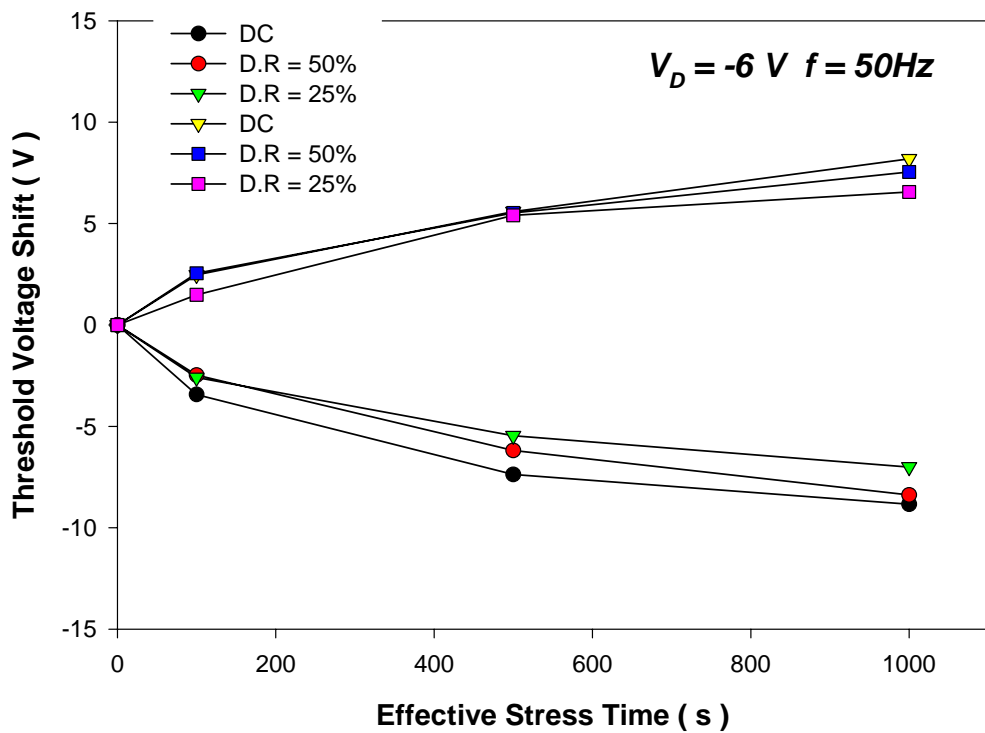


Fig. 3.65 Threshold voltage shift versus effective stress time induced by ON region and OFF region AC bias-stress with different duty-cycles.

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(2004.09-2006.07)

論文題目：

五環素有機薄膜電晶體之操作原理與可靠度分析

Device Mechanism and Reliability of pentacene-based OTFTS