Chapter 1
Introduction

1-1 Introduction of Organic Thin Film Transistors (OTFTs)

The concept of using organic materials as semiconductors layer in transistors are realized at least since the 1980s [1,2]. Recently, the organic thin film transistors (OTFTs) are of interest for the fabrication of low-cost, large-area, flexible displays and low-end electronics. The OTFTs performance has been improved in the past decade and comparable to the hydrogenated amorphous silicon transistors (a-Si:H TFT) [3]. To fabricate organic transistors on glass or flexible substrate, it is essential to lower down the process temperature. Many researchers have proposed individual methods to fabricate the pentacene-transistors and the reported field-effect mobilities are in the range of 10^{-3} ~ 3cm^2/V-sec [4]. However, the OTFTs still face several problems: low-mobility, low-temperature gate dielectrics, and reliably large area processes, etc. Among these issues, a suitable gate dielectric is a major obstacle that must be overcome.

However, the high operating voltage was still a limitation on organic transistors such as the portable applications, especially for RFID requiring low power consumption, it is necessary to reduce the operating voltage to below 7V [5]. A high operating-voltage not only results in high power-consumption, and higher cost on driving circuits; but also damages the organic material. Therefore, to achieve the low-voltage and high performance OTFTs, high-capacitance gate-dielectrics are important demands. Because the accumulated charge density in channel region influenced OTFTs mobility significantly [6]. According to MOSFET theory, the

higher capacitance would accumulate more charge in semiconductor layer under a given gate-voltage. Thus higher capacitance permitted the OTFTs to be operated at lower voltage.

Recently, the high-capacitance gate dielectrics can be achieved by the two methods. One is reducing the gate-dielectric thickness [7], the other was using the high-k material as the gate-dielectrics [8]. However, the high-k materials may arise in high leakage current and low dielectric strength in the utilization of OTFTs. The pinhole may be another question when reducing the dielectric thickness. So, a new dielectric is provided with higher dielectric permittivity, controllable leakage current and tunable thickness. That will be very desirable for OTFTs.

Besides increasing the capacitance, the surface polarity of the gate-dielectric is another concern. Several researchers had verified the hydrophobic surface was more suitable for organic film deposition [9]. Since the hydrophobic polymer dielectric has lower or similar surface energy to organic films. The similar concept was also realized by self-assembled monolayer (SAM) on inorganic dielectrics. If the inorganic dielectrics with lower surface-energy, that may provide better performance and resulted in lower interface traps in OTFTs [10].

However, several reports have dicussed the effects of the gate dielectric roughness on OTFTs [11]. The roughness of the gate dielectric can affect the pentacene film deposition and the OTFTs performance.

Finally, if the novel dielectrics with fine surface property and high dielectric quality on which a good organic film could be deposited on, it can overall improve the properties of OTFTs.

1-2 Deposition Methods of AlN

As for Ⅲ-Ⅴ compounds, the related researches were focused on the applications of high-power and light-emitting devices [12]. However, the single-crystal compounds can only be grown by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) systems…etc [13]. Nevertheless, the high growing temperature and expensive equipment was essentially required. On the other hand, the polycrystalline or amorphous Ⅲ-Ⅴ compounds are also utilized in many applications. Low-temperature deposition systems such as sputtering or e-gun evaporation are used to deposit polycrystalline or amorphous III-V compounds [14]. Among the previous systems, the sputtering was chosen for the thin film deposition because of its simplicity and low-temperature processes. In our experiment, with the RF/ICP (Inductively Coupled Plasma) sputtering system, high quality AlN can also be deposited under relatively low temperature (~150℃) and room temperature (~25℃).

1-3 Motivation

To improve the mentioned issue, we fabricated the OTFT with the AlN film as a new gate dielectric. The AlN film has high chemical stability, high physical stability, and high dielectric permittivity [15]. Moreover, while compared to the oxide-based dielectrics, the wetting property on AlN film was more hydrophobic and the surface free energy was similar to that of the pentacene film.

We also demonstrate two methods to control the gate leakage and the improve of surface roughness in AlN film. Thus, the AlN film shows a low leakage current and a smooth surface.

In this experiment, with the RF sputtering system, the dielectric thickness could be controlled precisely. When reducing the AlN film thickness, the AlN-OTFTs can be operated at low-voltage and exhibit low threshold voltage and extremely low

subthreshold swing.

1-4 Thesis Organization

In Chapter 1, we describe the introduction of OTFTs, deposition methods of AlN, and motivation of the thesis. In Chapter 2, we introduce the transportation mechanisms of organic semiconductor, operation of OTFTs, and parameter extraction. In Chapter 3, the fabrication and the structure of OTFTs are presented. In Chapter 4, electrical properties of AlN dielectric, effects of AlN dielectric roughness, surface polarity of AlN film, low-voltage OTFTs with AlN dielectric, and high-performance AlN-OTFTs are investigated. Finally, we describe the conclusion and future work in Chapter 5.

Chapter 2
Theoretical Background of OTFTs

2-1 Introduction

OTFTs are based on the conjugated polymers, oligoacenes, or fused aromatics. Then, the organic materials can function either as p-type or n-type. In p-type semiconductors, the majority carriers are holes; while in n-type the majority carriers are electrons. Among, p-type semiconductors are the most widely studied organic semiconductors. Recently, many molecular semiconductors, such as pentacene, thiophene oligomers, and regioregular poly(3-alkyl-thiophene) are proposed. The pentacene ($C_{22}H_{14}$) is a promising candidate for future electronic devices and an interesting model system, due to its superior field effect mobility and environmental stability [16].

2-2 Transportation Mechanisms of Organic Semiconductor

Carrier transportation in the organic semiconductors have been investigated on the theory and modeling in the past years [17]. Organic conductors are conjugated materials, where the π-electrons are conducted intra the molecular. Its crystalline is formed by relatively weak Van der Waals interaction between molecules, where the molecular-stacking determines the carrier behavior. Thus, the carrier transport were described by different models than the covalent-bonded semiconductors. In covalent-bonded semiconductors, carriers move as highly delocalized plane waves in wide bands and have a very high mobility. But in weak-bonded organic semiconductors, the high-mobility model is no longer valid.

Recently, two principal types of theoretical model are used to describe the transport in organic semiconductors : “The band-transport model” and “The hopping models”. However, band transport may not suit for some disordered organic semiconductors, in which carrier transport is govern by the hopping between localized states. Hopping is assisted by phonons and the mobility increases with temperature. Typically, the mobility is very low, usually much lower than $1cm^2$/V-sec. The boundary between “band transport” and “hopping” is divided by materials mobilities (~$1cm^2$/V-sec) at room-temperature (RT) [18]. Many kinds of polycrystalline organic semiconductors , such as several members of the acene series including pentacene, rubrene, have RT mobility over the boundary [19]. Sometimes, temperature-independent mobility was found in some polycrystalline pentacene devices [20]. Thus, this observation argued that the simply thermal activated hopping process governed the whole carrier transport behaviors in high quality polycrystalline pentacene film, despite that the temperature independent mobility has been observed in exceptional cases [20].

The understanding of carrier transport in single crystals of organic semiconductors will help us to understand the transport mechanism in polycrystalline organic semiconductors. The coherent band-like transport of delocalized carriers becomes the prevalent transport-mechanism in the single crystals of organic semiconductors, such as pentacene, tetracene, under the low-temperature environments. The very high hole mobility values have been measured by time-of-flight experiments [21]. Thus, the temperature dependence of the carrier mobility was found below 100K and following with a power law of $\mu \propto T^{-n}$, n~1, [22], in single crystals of organic semiconductors, consistent with the band-transport model. However, between 100K and 300K, the carrier mobility show a constant value [22], that has been described as the superposition of two independent carrier transport

mechanisms. The first mechanism was small molecular polaron (MP). According to this model the carriers were treated as the heavy; polaron-type; quasi-particles. It is formed by the interaction of the carriers with intra-molecular vibrations of the local lattice environment, and move coherently via tunneling. In this model, the mobility follows the power law $\mu_{MP}=aT^{-n}$. The other involves a small lattice polaron (LP), which moves by thermally activated hopping and exhibits a typical exponential dependence of mobility on temperature : $\mu_{LP}=bexp[-Ea/kT]$. The superposition of these two mechanisms could get a good consistence with experimentally measurement of temperature-dependence mobility from room temperature to a Kelvin degrees (K) [23].

Finally, the exact nature of the charge carrier transport in organic molecular crystals is still not well-understood, which has been the focus in many theoretical studies [24].

2-3 Operation of OTFTs

Figure 2-1 show two kinds of standard OTFT device configurations, (a) is the top-contact device and (b) is the bottom-contact device, respectively. Actually, the general operation concepts are originated from MOSFET theory. In traditional MOSFET, most devices are operated in inversion mode. However, the operation of OTFTs is generally in accumulation mode [25]. In Fig. 2-2 presents the schematic operation of OTFTs, showing a p-type semiconductor; + indicates a positive charge; - indicates a negative charge. When zero bias was applied to OTFTs, the schematic diagram is shown in Fig. 2-2(a). When a bias, V_G, is applied to the gate electrode shown in Fig. 2-2(b), (c), the voltage-drop over the insulator and the semiconductor accumulates charges near the insulator/semiconductor interfaces. The typical I-V

characteristics can be used to calculate the important parameters such as mobility, threshold voltage, and on/off current ratio.

Since the pentacene is a p-type semiconductor. Thus, negative bias is applied to the gate, the voltage-drop between insulator and semiconductor cause the band bending in the organic semiconductor. The additional positive charges will accumulate between the interfaces. The energy band diagrams for p-type and n-type OTFT are shown in Fig. 2-3. The insulator serves as a capacitance per unit area which stores charges and can be represented as C_{OX}, then the accumulated charge per unit area is about $V_G C_i$. Additionally, assuming that a negligibly small voltage, V_{th}, is dropped across the semiconductor. In this situation, the applied drain bias can drive the current from source to drain. The conduction is determined by the mobility (μ) which represents the driving ability of the electrical field on the accumulated charges. Therefore, the increased gate voltage δV_G accounts for the increased charges $C_{OX}\delta V_G$ and the total charges accumulated over the channel region are $WLC_{OX}\delta V_G$, where W and L corresponds to the channel width and length,respectively. If the increment of charge has a mobility: μ, and a small drain bias: V_D is applied then an incremental current δI_D is represented as

$$\delta I_D \approx \frac{W}{L}\mu C_{OX} V_D \delta V_G \tag{2.1}$$

In general, we can divide the operation of OTFTs into two regions, linear and saturation regions. The drain current in the linear region is determined from the following equation:

$$I_D = \frac{W}{L} C_{OX}\mu(V_G - V_{TH} - \frac{V_D}{2})V_D \tag{2.2}$$

Since the drain voltage is quite small, sometimes equation (2.2) can be simplified as

$$I_D = \frac{W}{L} C_{OX}\mu(V_G - V_{TH})V_D \tag{2.3}$$

For $-V_D > -(V_G - V_{TH})$, I_D tends to saturate due to the pinch-off of the

accumulation layer. The current equation is modified as:

$$I_D = \frac{W}{2L} C_{OX} \mu (V_G - V_{TH})^2 \tag{2.4}$$

2-4 Parameter Extraction

In this section, the methods of extraction the mobility, the threshold voltage, the on/off current ratio, the subthreshod swing, the maximum interface trap density, and the surface free energy is characterized, respectively.

2-4-1 Mobility

Generally, mobility can be extracted from the transconductance maximum g_m in the linear region:

$$g_m = \left[\frac{\partial I_D}{\partial V_G} \right]_{V_D = constant} = \frac{WC_{OX}}{L} \mu V_D \tag{2.5}$$

Mobility can also be extracted from the slope of the curve of the square-root of drain current versus the gate voltage in the saturation region, i.e. $-V_D > -(V_G - V_{TH})$:

$$\sqrt{I_D} = \sqrt{\frac{W}{2L} \mu C_{OX}} (V_G - V_{TH}) \tag{2.6}$$

2-4-2 Threshold voltage

Threshold voltage is related to the operation voltage and the power consumptions of an OTFT. We extract the threshold voltage from equation (2.6), the intersection point of the square-root of drain current versus gate voltage when the device is in the saturation mode operation.

2-4-3 On/Off current ratio

Devices with high on/off current ratio represent large turn-on current and small off current. It determines the gray-level switching of the displays. High on/off current ratio means there are enough turn-on current to drive the pixel and sufficiently low off current to keep in low power consumption.

2-4-4 Subthreshod swing

Subthreshold swing is also important characteristics for device application. Its is a measure of how rapidly the device switches from the off state to the on state in the region of exponential current increase. Moverover, the subthreshold swing also represents the interface quality and the defect density [26].

$$S = \frac{\partial V_G}{\partial(\log I_D)}\bigg|_{V_D=\text{constant}} \quad \text{, when } V_G < V_T \text{ for p-type.} \tag{2.7}$$

If we want to have good performance TFTs, we need to lower subthreshold swing of transistors.

2-4-5 Maximum interface trap density

The maximum number of interface traps density, at the pentacene/dielectric interface can be estimated from the value of the subthreshold swing [26]. Assuming that the densities of deep bulk states and interface states are independent of energy [27]:

$$N_{SS} = [\frac{S \cdot \log(e)}{kT/q} - 1] \cdot \frac{C_i}{q} \tag{2.8}$$

where S is the subtheshold swing, C_i is the capacitance density, k is Boltzmann's constant, and T is the absolute temperature.

2-4-6 Surface free energy

The surface-free-energy of gate dielectrics is a characteristics factor, which affects the performance of the OTFTs. The surface-free-energy was calculated from the contact-angle measurement by using different liquid-drops with different polarities. In our experiments, the Owens, Wendt, Rabel and Kaelble's method (the modified Fowkes' equation) is used to estimate the surface energy [28]:

$$(1+\cos\theta)\gamma_L = 2(\gamma_S^d \gamma_L^d)^{1/2} + 2(\gamma_S^p \gamma_L^p)^{1/2} \tag{2.9}$$

where θ is the contact angle between probing liquid and solid surface; γ_L, γ_L^d and γ_L^p is the total surface-free-energy, dispersion, and polar component of probing liquid, respectively. From this approximation, the total surface free energy γ_S of the solid surface is:

$$\gamma_S = \gamma_S^d + \gamma_S^p$$

It is characterized by the sum of dispersion γ_S^d and polar γ_S^p components.

2-4-7 Poole-Frenkel (P-F) mechanism

The P-F emission is due to the field-enhanced thermal excitation of the trapped electrons in the insulator into the conduction band [29,30]. The current density is given by

$$J = J_0 \exp\left(\frac{\beta_{PF} E^{1/2} - q\phi_{PF}}{k_B T}\right) \tag{2.10}$$

where $J_0 = \sigma_0 E$ is the low-field current density, σ_0 the low-field conductivity, $\beta_{PF} = (q^3/\pi\varepsilon_0\varepsilon_r)^{1/2}$, and ϕ_{PF} the height of trap potential well.

Chapter 3
Experiments

3-1 AlN Deposition

The low temperature AlN films were deposited by a radio frequency inductively coupled plasma (RF-ICP) system [31]. In this system, a 2-inch Al target (purity 99.999%) of the RF gun was immerged in a 4-inch inductive coil which can be controlled by an independent RF coil power. Before the AlN films deposition, the n^+-Si wafer used as the substrate was rinsed in the deionization water, followed by the initial RCA cleaning. Right before we transferred the wafer into the RF-ICP system, we used acetone with ultrasonic to remove the particles and the impurities and dipped the wafer in the dilute HF solution ($HF:H_2O=1:100$) to remove the native oxide on the Si wafer. The system was pumped down to a base pressure less than 2×10^{-6}torr before admitting gas in. A mixed gas of argon and nitrogen was monitored by mass flow controllers at different Ar/N_2 ratio. AlN films were deposited at a total pressure of 2.5mtorr and at a substrate temperature varied from room temperature to 250℃. The RF gun and the inductively coupled coil power can be varied from 0 to 200W and 0 to 180W, respectively. All the relative experiment details were published in our previous reports [31]. The thickness of AlN was estimated by the cross-section image of the scanning electron microscopy (SEM).

3-2 OTFTs Fabrication

The devices used in this series of experiments are the top contact (TC) structure,

which means the organic semiconductor layer is deposited on the bottom of the contact electrodes. The detail fabrication processes are following:

Step1. Substrate and gate electrode

4-inch n-type heavily-doped single crystal silicon wafer with (100) orientation is used as substrate and gate electrode.

Step2. Gate dielectric formation

After the initial acetone cleaning and dilute HF solution, the gate dielectric layer is formed in RF-ICP sputter system. High quality AlN film can be formed under low temperature.

Step3. Pentacene film deposition through the shadow mask

The pentacene material obtained from Aldrich without any purification was directly placed in the thermal coater for the deposition. It is well known that the deposition pressure, deposition rate, and deposition temperature are the three critical parameters to the quality of the organic film [32]. The deposition is started at the pressure around 1×10^{-6}torr. The deposition rate is controlled at ~0.5Å/sec and the thickness of pentacene film was about 100nm, monitored by the quartz crystal oscillator. Slower deposition rate is expected to result in smoother and better ordering of the organic molecules. The deposition temperature is also a factor influencing the pentacene film formation. The temperature we use in depositing pentacene films is 70 ^{o}C. We use shadow mask to define the active region of each device.

Step4. Source/Drain deposition through the shadow mask

The injection barrier of the OTFT device is determined by the materials of the source and drain electrodes. Materials with large work function are preferred to form Ohmic contact [33]. The Au with work function ~5.1eV does help to provide a better injection. Then, we deposited Au as the source/drain electrodes on the pentacene film. The thickness of the electrode pad is 1000Å.

The top contact structure is shown in figure 2-1(a). In this study, all the measured data were obtained from the semiconductor parameter analyzer (HP 4156A) in the darks at room temperature. And we measure the OTFTs immediately when the samples were unloaded from the evaporation chamber.

3-3 Capacitance Structure Fabrication

In this study, the structures of metal-insulator-silicon (MIS)-Au/AlN/Si capacitors was fabricated using the following procedure. First, heavily doped n-type silicon (100) substrates were degreased and acid cleaned using an initial RCA cleaning and an HF solution dip. The AlN film was deposited by RF-ICP system. A mixture gas of argon and nitrogen at different Ar/N_2 ratio and the substrates were heated during deposition at different temperature. The top electrode (Au) was defined by shadow mask. The area of the Au pad is $500\times500\mu m^2$. The Au thickness is about 700Å. In the MIS capactors, AlN films were deposited on blank silicon wafers, and subsequently covered with Au. The MIS structure is shown in figure 3-1.

The MIS was electrically characterized in terms of leakage current and dielectric

constant. Current-voltage (I-V) measurements were done with an HP 4156A parameter analyzer. Capacitance-voltage (C-V) curves were obtained by an HP 4284A C-V meter. The frequency dependence of the capacitances was measured at frequencies from 50Hz to 960KHz.

Chapter 4
Result and Discussion

4-1 Electrical Properties of AlN Dielectric

The high-k gate dielectric generally caused a high leakage current [34]. Therefore, how to suppress the leakage current has become an important subject in the study of transistors [35]. It is know that the processing conditions have an important effect on the properties of high-k materials [36]. During the RF sputtering process, the parameters, such as the substrate temperature, the deposition rate, and the gas flow rate, have a significant influence on the dielectric films. In this study, the effects of nitrogen flow rate and substrate temperature are investigated. Thus, we characterize the permittivity and leakage current in AlN film under different substrate temperatures and Ar/N_2 gas ratio.

4-1-1 Dependence of dielectric leakage on substrate temperature

In past years, many investigations have been carried out concerning the influence of dielectric deposition temperature on the current-voltage characteristics [37,38]. These researchers demonstrated that the dielectric film grown at high deposition temperature shows higher leakage current due to increasing surface roughness.

According to the theory, we tried to control the leakage current by decreasing the substrate temperature during the sputtering process. We deposit three distinct AlN-MIS structure at a Ar/N_2 ratio of 2/9 for the leakage experiment. The AlN film was deposited at the three temperature 250°C, 200°C, and 150°C, respectively. In Fig. 4-1 the change of surface roughness on AlN films could be observed from the

atomic force microscopy (AFM) images with the increase of temperature. The leakage current measured from the MIS structure with 95nm-thick AlN was shown in Fig. 4-2. AlN films deposited under different substrate temperatures are compared. The leakage current densities of the AlN films are about 1×10^{-9}A/cm^2, 2.4×10^{-9}A/cm^2, 6.2×10^{-9}A/cm^2 at electric field as 1MV/cm for deposition temperatures of 150℃, 200℃, 250℃, respectively. The breakdown fields are more than 5MV/cm, respectively. The AlN deposited at 150℃ shows a low leakage current. Whereas the 200℃-AlN and 250℃-AlN dielectrics exhibited larger leakage current, yet these value are acceptable for the device fabrication. These dielectric properties are comparable to those of the thermal SiO_2, high-k, or polymer gate dielectrics in some reports [8,39,40].

The capacitance-frequency characteristic is also shown in the inset of Fig. 4-2. The frequency dependence of the dielectric capacitances was measured in the range 50Hz to 960KHz. However, under a wide frequency operation range, from 50Hz to 1KHz, the capacitance and the calculated dielectric permittivity are around ~64 nf/cm^2 and ~7, respectively.

Thus, the result indicates that the leakage current density can be reduced by decreasing the substrate temperature. The leakage current density decreased mainly due to the reduction of surface roughness with decreasing substrate temperature. Because of in the rough surface, the electric field is much stronger than in the smooth surface [41]. The higher electric field can result in higher leakage current. In addition to this, we can also observe that the different substrate temperature of AlN gate dielectric layers with constant capacitance was obtained by adjusting the substrate temperature.

4-1-2 Dependence of dielectric leakage on nitrogen gas flow rate

In past years, some investigations exhibited that repair the vacancies in the dielectric may improve the leakage. As proposed in the metal-oxide dielectrics, the oxygen vacancies were the dominated defects that degraded the dielectric properties. Some researchers introduced the oxygen flow to restore the defects [42]. The dielectric leakage was significantly improved in their results.

According to the theory, we also tried to control the leakage current by increasing the N_2 gas flow rate during the sputtering process. We deposit three distinct AlN-MIS structure at 150℃ for the leakage experiment. The AlN film was deposited under different Ar/N_2 gas ratio and each thickness was ~95nm. In Fig. 4-3, it shows that the AFM images of AlN surface roughness from different nitrogen gas flow rate (2/5, 2/7, 2/9). The result indicating that very similar surface roughness was all obtained from different of nitrogen gas flow rate, respectively. As shown in Fig. 4-4, the x-ray photoemission spectrum (XPS) signal from nitrogen (N 1s) was extracted. When the nitrogen flow rate increased, the nitrogen signal also increased. That implied the nitrogen component could be increased by nitrogen flow rate. The results were also compared as the leakage current density vs. the electric field in Fig. 4-5. As show in the figure, the leakage current increased rapidly in the sample of gas ratio Ar/N_2: 2/5. When the applied electric field was exceeded 3MV/cm, the leakage current density was more than $10^{-4}A/cm^2$. Though there was no significantly dielectric breakdown observed in high electric field. But the leakage resulted in instable and low device yield in our early stage studies. For further reducing the leakage, the Ar/N_2 gas ratio was changed from 2/5 to 2/7 and 2/9. As we could observe, the leakage current was suppressed from $10^{-4}A/cm^2$ to $10^{-9}A/cm^2$. Besides, when the capacitance operated at low electric field (1-2MV/cm), the leakage

current was kept at very low level ~10^{-10}A/cm^2. The result can come up with other novel low temperature dielectrics [8,43].

To further study the conduction mechanism in AlN, the leakage current-density was plotted as the function of electric field in log-log scale (log(J) vs. log(E)) in Fig. 4-6(a). Clearly, two transports in AlN film were observed. A good Ohmic-conduction could be fitted under low electric field, but the conduction transferred into nonlinear under high electric field. If the Ar/N_2 gas ratios was changed from 2/5 to 2/7 and 2/9, the transfer point of the electric filed was also changed from 0.8 to 1.2 and 2.7MV/cm, respectively. Thus, the J-E curves was plotted as Poole-Frenkel plots (ln(J/E) vs. $E^{1/2}$) in Fig. 4-6(b). The slope ($\beta / k_B T$) of the straight line in Fig. 4-6(b) is:

$$\beta / k_B T = \sqrt{\frac{q^3}{\pi \varepsilon_0 \varepsilon_r}}$$

where q is the electron charge, k_B is the Boltzmann's constant, T is the absolute temperature, ε_0 is the absolute dielectric constant, ε_r is the relative dielectric constant. By fitting the slope ($\beta / k_B T$) in Fig. 4-6(b), the slope is 11.2, 11, 10.9 (cm/MV)$^{1/2}$ at the Ar/N_2 ratio: 2/5, 2/7, 2/9, respectively. The relative dielectric constant determined from the slope is 6.8, 7.1, 7.2, respectively. From the capacitance measurement of the impedance analyzer (HP 4284A), the estimated dielectric constant was about 6.28, 6.82, 7.32 at Ar/N_2 ratio: 2/5, 2/7, 2/9, respectively. They yield the various values of the dielectric constant and the constant $\beta_{PF} / k_B T$, as shown in Table I. It was good agree with the proposed Poole-Frenkel transport in AlN. If we consider the defect distribution in AlN film, it is investigated that the corresponding defects near the conduction band were the nitrogen vacancies [44,45]. Thus, the increase of nitrogen flow rate in the sputtering process may be an affective way to compensate the nitrogen vacancies and suppress the potential leakage path in

AlN.

Thus, the result indicates that the leakage current density can be reduced by increasing the nitrogen gas flow rate. Therefore, according to the hypothesis, by compensating the none-metallic element in the compound dielectric should be a practicable method for reducing leakage. The dielectric leakage was significantly improved.

In the short summary, the leakage current density decreased can be improved by increasing nitrogen flow rate and decreasing substrate temperature.

4-2 Effects of AlN Dielectric Roughness

Current research on gate dielectric is improving the performance of organic thin film transistors (OTFTs). It is generally accepted that the surface roughness of the gate dielectric is an important parameter that affects the electrical performance of OTFTs [11,46]. In recent work, rougher gate dielectrics have been shown to result in smaller grains and lower the mobility in OTFTs. According to the result, we might try to deduce the AlN surface roughness.

In the experiments, we compare the morphology of pentacene and devices characteristics to the different roughness of AlN gate dielectrics. The devices structure and the fabrication procedure were described in section 3-2.

Firstly, by changing the deposition temperature of the AlN gate dielectric, the surface morphologies were obtained from their atomic force microscopy (AFM) images, as shown in figures 4-7 (a) (b) and (c). Clearly, the average surface roughness decreased from 0.43, 0.31, to 0.17nm while the deposition temperature was varied from 250°C, 200°C, to 150°C and at a Ar/N_2 ratio: 2/9. It is also known that the dielectric surface roughness has a strong influence on the pentacene deposition

[11,47]. In figures 4-7 (d) (e) and (f), we compare the morphology of pentacene film grown on these three of AlN films, correspondingly. As the AlN surface becomes smoother, the grown pentacene film turns to be dendritic structure and exhibits larger grain size.

In order to determine the influence of roughness on OTFTs, the electrical properties of OTFTs from different gate dielectric roughness were characterized. The transfer characteristics of the OTFTs with AlN dielectrics grown at different temperatures and at a Ar/N_2 ratio: 2/9 are shown in Fig. 4-8. The drain voltage is biased as -3V to keep the devices operated under linear region. The gate voltage was scanned from +2V to -10V. When the AlN deposition temperature is varied from 250°C, 200°C, to 150°C, the device subthreshold swing is improved from 0.6V/decade to 0.4V/decade and the device output current is enlarged more than one order. Since the subthreshold swing represents the interface quality and the defect density, we calculate the maximum interface trap density by equation (2.8).

$$N_{SS} = [\frac{S \cdot \log(e)}{kT/q} - 1] \cdot \frac{C_i}{q}$$

By assuming C_i=64nf/cm^2 and S = 0.4, 0.5, 0.6V/decade, respectively. The approximate interface trap density in our devices is 2.28×10^{12}, 2.95×10^{12}, and 3.62×10^{12}cm^{-2}eV^{-1}, respectively. This result is comparable to other dielectrics in OTFTs [10,26,39,48].

Additionally, lowering the AlN temperature also reduces the device threshold voltage. The Fig. 4-9 depicts the curves of $\sqrt{I_D}$ vs.V_G, the x-axis interval reveals that OTFTs with 250°C AlN film have higher threshold voltage as -6V while those with 200°C and 150°C AlN films have lower threshold voltage as -2V. The output characteristics of the proposed OTFTs with AlN-dielectric grown at different temperatures are also shown in Fig. 4-10, Fig. 4-11, Fig. 4-12, respectively.

The improvement of the device performance by reducing the AlN deposition temperature can be further studied by comparing their field effect mobility in Fig. 4-13. The mobility is extracted from the linear region transconductance as equation (2.5).

$$\mu = \frac{L}{V_D W C_i} \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = constant}$$

It is compared that the mobility of devices with 150°C AlN film, 200°C AlN film, and 250°C AlN film, the former two have larger maximum mobility such as 0.24 cm^2/V-sec for 150°C AlN-OTFT and 0.04cm^2/V-sec for 200°C AlN-OTFT. Those devices with AlN deposited at 250°C, however, exhibit much lower maximum mobility around $10^{-3}cm^2$/V-sec. It is also observed that the filed effect mobility of devices with 250°C AlN film suffers pronounce degradation under high gate bias due to surface irregular causes locally strong electric field and results in leakage and also increases the surface scattering effect.

In the short summary, it can be concluded that lowering the AlN deposition temperature gives smoother surface and larger pentacene grain size. The field effect mobility is also accordingly improved.

4-3 Surface Polarity of AlN Film

In general, the pentacene deposition and the OTFTs performance are strongly influenced by the organic/dielectric interaction. To enhance the performance, the surface polarity was one of the key issues. Recently, researchers showed interface defects can be minimized by altering dielectric polarity such as SAM-treatment or the polymer dielectric [9,10,49]. Base on the suggestion, we might try to investigate the AlN surface polarity.

In this experiment, we used de-ionized water and glycerol as the polar liquid pair, and di-iodomethane was chosen as the none-polar liquid. According to our measurement, the contact angle between AlN-D.I. water, AlN-glycerol, AlN-diiodomethane was 77.0°±2° , 56.1°±1° , 40.4°±4°. By equation (2.9)

$$(1+\cos\theta)\gamma_L = 2(\gamma_S^d \gamma_L^d)^{1/2} + 2(\gamma_S^p \gamma_L^p)^{1/2}$$

, the total surface free energy of AlN was 38.5±1 (mJ/m^2). As summarized in Table II, the AlN had low surface energy. The results indicate that the surface in AlN gate dielectric was hydrophobic and had a low polarity. To our surprise, the surface free energy was lower than polymer dielectrics, pentacene, and the HMDs treated SiO_2. It was almost close to the OTS-treated SiO_2 [49,50,51]. The particular characteristic is contrary to the other ceramic-based dielectrics. The similar affinity between pentacene and dielectrics may be helpful for reducing traps when depositing organic film on dielectrics [52]. That may be a reasonable explaining for AlN-OTFTs having the outstanding sub-threshold swing and low interface trap density.

In the short summary, we have demonstrated that the surface of AlN gate dielectric was very hydrophobic and lowly polar. Thus, this result indicates that the AlN gate dielectric with well-defined surface property and more compatible the growth of pentacene.

4-4 Low-Voltage OTFTs with AlN Dielectric

Recently, one of the key problems with existing organic TFTs is their large operating voltage, which often exceeds 20V. Thus, to further decrease the operating voltage, increasing the dielectric capacitance is effectively [7,8,53]. Base on the method, we might try to increase the AlN dielectric capacitance. In this experiment, the thickness of AlN dielectric would be reduced to achieve a high capacitance to

operate OTFTs at a low voltage.

According to previous sections, it is known that the 150℃ AlN film with Ar/N_2 gas ratio about 2/9 showed the potential for reducing the thickness to increase the OTFTs capacitance. Thus, for further improving the operating voltage of AlN-OTFTs, we used the thinner AlN film as the gate dielectric. It is confirmed that the thickness of AlN film from scanning electron microscopy (SEM) in Fig. 4-14. The thickness of AlN film was about 60nm.

From the MIS structure, the capacitances were measured at the frequency of 50Hz to 960KHz in the inset of Fig. 4-15. The corresponding capacitance was about 93nf/cm^2 from 50Hz to 1KHz. The gate leakage was characterized in Fig. 4-15, the leakage was as low as ~10^{-8}A/cm^2 under electric field at 1MV/cm. The plot of $\mathrm{Log}\ I_D$ vs. V_G and $\sqrt{I_D}$ vs. V_G was shown in Fig. 4-16(a) and 4-16(b), respectively. In Fig. 4-16(a), the AlN-OTFT was operated less than 5V. The high on/off current ratio more than 5 was also achieved even under extremely low drain bias -0.5V. Additionally, the subthreshold swing can be as low as ~0.13V/decade at a drain voltage of -3V. From Fig. 4-16(b), the extracted threshold voltage and the field effect mobility in saturation region was about -1.5V and 0.02cm^2/V-sec, respectively. On the other hand, the output characteristics were shown in Fig. 4-17, the transistor could be easily operated in saturation region at low drain voltage about -3V. For further investigating, we may focus on the interface quality of semiconductor (pentacene) and insulator (AlN) from the AlN-OTFTs performance. Since the maximum interface trap density could be estimated by the previous equation. By assuming C_i ~ 93nf/cm^2 and S = 0.13V/decade. From our calculation, the approximated interface trap density in our devices is 6.8×10^{11}cm^{-2}eV^{-1}. This trap density was quite low and comparable with other dielectrics in OTFTs [10,26,39,48].

In the short summary, the key to low-voltage operation is the reduction of dielectric thickness. The high capacitance of the thin AlN dielectric make the OTFTs to operate at a relative low voltage about 5V and exhibit low threshold voltage and a extremely low subthreshold swing. Thus, the AlN-OTFTs showed the potential application as low-voltage and rapid switched organic transistors.

4-5 High-Performance AlN-OTFTs

In recent years, organic thin film transistors (OTFTs) exhibit great potential for mass production of active-matrix displays and organic electronics. In the future, the OTFTs will be fabricated on clothes or paper substrate for flexible application and battery-powered device application [5,54]. Thus, to develop an low-voltage OTFTs at low process temperature (below 100℃) is very desirable.

According to above sections, the author demonstrated the control of gate leakage of AlN film. As the result of these optimized parameters, thus, in this experiment, we tried to fabricate thin AlN film as the gate insulator at higher Ar/N_2 ratio and/or at room temperature(~25℃).

4-5-1 AlN dielectric with higher Ar/N_2 ratio

We deposited AlN at a higher Ar/N_2 ratio: 2/12 and at a substrate temperature 150℃. In Fig. 4-18, we showed the AFM image of AlN film. The AlN film was smooth at higher Ar/N_2 ratio. The surface roughness was only about 0.18nm. In Fig. 4-19, shows the pentacene grains on the AlN insulator. The pentacene films exhibited a large grain size, too. Actually, the roughness degradation and pinhole may arise when reducing the dielectric thickness. In the higher Ar/N_2 ratio

sputtered-AlN film, no significant surface irregular and pinholes were appeared in our observation. Additionally, the higher Ar/N_2 ratio AlN film showed good dielectric properties. From the MIS structure, the capacitances were measure at the frequency of 50Hz to 960KHz in the inset of Fig. 4-20. The capacitance was about 104nf/cm^2 from 50Hz to 1KHz. The gate leakage was characterized in Fig. 4-20, the leakage was about 9.8×10^{-9}A/cm^2 under electric field at 1MV/cm.

Subsequently, we exhibited the transistor characteristics. The channel width and length were defined as 600μm and 100μm. The AlN-OTFT was fabricated on the extremely thin AlN film. From the SEM image in Fig. 4-21, we estimate the thickness of AlN film is about 50nm. The transfer characteristic was showed in Fig. 4-22. The AlN-OTFTs could be operated at relative low voltage (~5V), the on/off current ratio was also remained highly (~10^5). The field effect mobility in the linear region were 1.29cm^2/V-sec, and 1.41cm^2/V-sec at drain bias were -0.5, and -1V, respectively. In Fig. 4-23, shows the plot of $(I_D)^{1/2}$ vs. V_G at a drain voltage of -3V. The threshold voltage was only -2.1V and the field effect mobility in saturation region was about 1.67cm^2/V-sec. The subthreshold swing was 350mV/decade at a drain voltage of -3V. The mobility of ~1.67cm^2/V-sec was close to the averaged best records for OTFTs [39]. Output characteristics were also showed in Fig. 4-24, the AlN-OTFTs could be operated in saturation region at low drain bias (~3V). Since the subthreshold swing represents the interface quality and the traps behavior [26], we may calculate the maximum interface trap density by previous equation. By assuming C_i=104nf/cm^2 and S = 350mV/decade, the approximate interface trap density in our devices is $3.16\times10^{12}cm^{-2}eV^{-1}$.

4-5-2 Room temperature AlN dielectric

In early stage, we deposited the AlN film at higher substrate temperature. The AlN film has grains and is highly c-axial oriented [31]. As for gate dielectrics, grain boundaries could influence the surface roughness and reduce the uniformity. Generally, the grain boundaries may also serve as leakage paths. Since the dielectric roughness and leakage are essential demands for OTFTs fabrication. In this experiments, we deposited AlN at lower substrate temperature and at a Ar/N_2 ratio: 2/9. In Fig. 4-25, we showed the AFM image of room temperature AlN film. In contrary to our former results, the room temperature AlN film was smooth. The surface roughness was only about 0.2nm. In Fig. 4-26 shows the pentacene grains on the AlN insulator. The pentacene films exhibited a large grain size. Actually, the roughness degradation and pinhole may arise when reducing the dielectric thickness. In the room temperature sputtered-AlN film, no significant surface irregular and pinholes were appeared in our observation. Additionally, the room temperature AlN film showed good dielectric properties. From the MIS structure, the capacitances were measure at the frequency of 50Hz to 960KHz in the inset of Fig. 4-27. The capacitance was about $104nf/cm^2$ from 50Hz to 1KHz. The gate leakage was characterized in Fig. 4-27, the leakage was about $9.5\times10^{-9}A/cm^2$ under electric field at 1MV/cm.

Subsequently, we exhibited the transistor characteristics. The channel width and length were defined as 600μm and 50μm. The AlN-OTFT was fabricated on the extremely thin AlN film. From the SEM image in Fig. 4-28, we estimate the thickness of AlN film is about 50nm. The transfer characteristic was showed in Fig. 4-29. The AlN-OTFTs could be operated at relative low voltage (~5V), the on/off current ratio was also remained highly ($>10^6$). The field effect mobility in the linear region was $0.16cm^2/V\text{-sec}$, and $0.14cm^2/V\text{-sec}$ at drain bias -0.5V, and -1V, respectively. In Fig. 4-30 shows the plot of $(I_D)^{1/2}$ vs. V_G at a drain voltage of -3V.

The threshold voltage was only -1.8V and the field effect mobility in saturation region was about 0.082cm^2/V-sec. The promising subthreshold swing was only 190 mV/decade at a drain voltage of -3V. The magnitude was almost approximately the theoretical minimum ~58mV/decade ($kT/q \cdot \ln(10)$) [55]. Output characteristics were also showed in Fig. 4-31, the AlN-OTFTs could be operated in saturation region at low drain bias (~3V). Since the subthreshold swing represents the interface quality and the traps behavior [26], we may calculate the maximum interface trap density by equation (2.8). By assuming C_i=104nf/cm^2 and S = 190mV/decade, the approximate interface trap density in our devices is 1.4×10^{12}cm^{-2}eV^{-1}. The trap density was almost close to the lowest trap density reported for organic transistors.

4-6 Summary

The pentacene-based OTFTs with low temperature (~25℃) and high Ar/N_2 ratio (2/12) AlN gate insulator had been fabricated and characterized. With the combination of favorable properties, demonstrates that OTFTs successfully at voltages about 5V and exhibited very high field effect mobility.

Chapter 5
Conclusion and Future Work

5-1 Conclusion

A new low-temperature gate-dielectric, AlN film, is proposed for OTFTs. The pinhole free, smooth and extremely thin AlN film can be deposited by the RF-sputtering system at low deposition temperature (from 150℃ to 25℃). The dielectric leakage was significantly low, and the AlN has a surface free energy that is similar to that of the pentacene film. It can be concluded that lowering the AlN deposition temperature gives smaller leakage current and larger pentacene grain size. The field effect mobility is accordingly improved. The process is promising for the development of low-temperature OTFTs. The Ar/N_2 flow ratio in the sputtering process was demonstrated to be a key parameter in reducing AlN gate leakage. Poole-Frenkel-related leakage is suppressed as the electric field increased.

Based on experimental result, the low-voltage and high performance OTFTs are realized. With the thinner AlN gate-dielectric, lower substrate temperature, and higher Ar/N_2 ratio, the AlN-OTFTs can be operated at low-voltage (about 5V). From the series of the experiments, the highest field effect mobility is 1.67cm^2/V-sec, the lowest subthreshold swing is 130mV/decade, and the lowest threshold voltage -1.5V, respectively. The high on/off current ratio about 10^6 were all observed from these AlN-OTFTs. According to the mentioned electric properties, it is demonstrated that the AlN-OTFT has potential application in low-voltage and rapid-switching organic transistors.

5-2 Future Work

Since the AlN-OTFTs on silicon substrate was successfully fabricated. Further studies will focus on realizing the AlN-OTFTs on glass and on flexible substrates. The leakage mechanism needs more detail experimental result to verify the influence of nitrogen-related defect. The growth of pentacene film on AlN is still a un-discovered evidence. The growing mechanism should be a interesting study. However, the improvement is also expected by pentacene purification and S/D resistance reduction in future studies.

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