低溫多晶矽薄膜電晶體元件C-V特性劣化行為之研究

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摘要

多晶矽薄膜電晶體(poly-Si TFTs)基於其優於非晶矽薄膜電晶體(amorphous silicon TFTs)的電流驅動能力，最近在液晶顯示器(AMLCD)及有機發光二極體(AMOLED)顯示器的週邊電路整合應用上皆備受矚目。

論文的第二章對元件的可靠度以各種不同的偏壓條件及偏壓時間來衡量。我們將以本文所提出之枕木型佈局的電晶體作可靠度的量測以避免元件間初始特性差異過大，導致在同一偏壓條件下得到發散的結果。經由這些實驗資料將會對估計元件的生命週期和安全的操作區域將是十分有幫助的。另外，我們將針對低溫多晶矽薄膜電晶體(low temperature poly-Si TFTs)的元件C-V特性作的研究。對於在特定外加偏壓下的元件C-V特性，會做進一步的討論。以元件在自發熱效應(Self-Heating Effect)偏壓條件下的閘極/源極(C_{GS})與閘極/汲極(C_{GD})的電容電壓特性為例，可以發現，在這個操作條件前後，其C_{GS}、C_{GD}均呈現明顯的飄移，且C_{GS}曲線在起始電壓附近呈現約 40%的增加，而C_{GD}曲線則僅呈現約 10%的增加。經由模擬結果顯示，元件兩端的電容特性的差異主要來自於在自發熱效應操作條件下，其閘極/源極跨壓甚大，因此造成介面缺陷的增加，形成C_{GS}後半段上升的

行為。而閘極/汲極的跨壓較小，因此所受到的影響也較小。另一方面關於元件在熱載子效應下所受的電容電壓特性，可以發現其C_{GS}曲線並未出現明顯的改變，然而C_{GD}曲線則在起始電壓附近下降，並呈現明顯的頻率相依性。這些元件劣化行為的描述將可以用我們所提出的劣化模型加以描述，並以模擬軟體模擬其趨勢。最後，將劣化的電容模型代入環形震盪器裡並以H-SPISE模擬電容效應，發現電容對於電路的影響是甚為巨大的。

Statistical Study on the Characteristics and Reliability Behaviors of N-type LTPS TFTs

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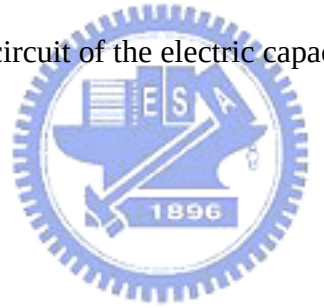
Abstract

Low Temperature Polycrystalline Silicon (LTPS) thin film transistors (TFTs) have attracted much attention in the application on the integrated peripheral circuits of display electronics such as active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diodes (AMOLEDs) due to its better current driving compared with a-Si (amorphous silicon) TFTs.

In the chapter two of this thesis, the reliability of LTPS TFTs is studied in form of stress map by adopting the crosstie layout TFTs to get the more consistent reliability behaviors. This database of reliability is very helpful to evaluate the lifetime and operation conditions of LTPS TFTs. In addition, we will focus on the C-V characteristic of the low temperature poly-Si TFTs and have further discussion of C-V characteristic under the specific bias voltage. As the example with the characteristic of voltage of C-V curve, it is found that before and after this condition of operating, its C_{GS} & C_{GD} presented obvious shift, and about 40% of the increase appears near the initial voltage in C_{GS} curve, but only about 10% of the increase appears in C_{GD} curve.

The result shows the difference of characteristics of the C-V curve of both ends of the device comes from self-heating stress condition, the voltage difference between gate/source is very large, so cause the increase of the defect of interfaces, form one section of behaviors of rising of C_{GS} latter half. And the voltage between gate and drain is smaller than that of gate and source, so the influence is slightly. Characteristic of C-V curve received under the hot carrier effect can find that its C_{GS} curve has not presented the obvious change, but C_{GD} curve drops near the initial voltage, and it is interdependent to present obvious frequency. The description of these component degradation behaviors can be described with the degradation model that we propose, and in order to imitate its trend of simulation. Finally , take the place of the model of C-V curve with the degradation one in ring oscillator and with H-SPISE simulation, find that the influence on the circuit of the electric capacity is very enormous.



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