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Chapter 1

Introduction

1-1. Introduction to LTPS TFTs

Nowadays, the amorphous silicon thin film transistors (a-Si TFTs) are commonly used to be the switches of the pixel in active matrix liquid crystal displays (AMLCDs). Fig. 1-1 shows the block diagram of active matrix display. All the driver chips are buried together with the other application-specified ICs on PCB because the current driving capacity of a-Si TFTs is not good enough for the system integration. However, the integration of driver circuitry with display panel on the same substrate is very desirable not only to reduce the module cost but to improve the system reliability.

For this reason, the polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention because of their widely applications in AMLCDs and organic light-emitting diodes (OLEDs) due to its high electron mobility. In polysilicon film, the carrier mobility larger than 100 cm^2/Vs can be easily achieved, which is about 100 times larger than that of the conventional amorphous-silicon TFTs (typically below 1 cm^2/Vs). This characteristic allows the pixel-switching elements made by smaller TFTs size, resulting in higher aperture ratio and lower parasitic gate-line capacitance for the improvement of display performance. Furthermore, the integration of peripheral circuits in display electronics can be achieved by poly-Si TFTs due to its higher current driving capability, which is illustrated in Fig. 1-2. In addition to flat panel displays, poly-Si TFTs have also been applied into some memory devices such as dynamic random access memories (DRAMs), static random access memories (SRAMs), high programming read only memories (EPROM), and

electrical erasable programming read only memories (EEPROMs) and three-dimensional(3D) ICs. Among the poly-Si technologies, low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are primarily applied on glass substrates for the display electrons since higher process temperature may cause the substrate bent and twisted.

However, there are still some issues in LTPS TFTs such as reliability, device variation, and the speed limitation of device, etc. On the other hand, there are some disadvantages in TFT's AC model for SPICE simulation, such as the insufficiency of C-V model's frequency dependence, the accuracy of TFT's DC model, etc. Our thesis will focus on the behavior of device's C-V characteristics and its model implantation in SPICE.

1-2. Diverse reliability behaviors & device variation

The Fig. 1-3 and Fig. 1-4 show the variation of threshold voltage and mobility degradation under different stress conditions. These figures reveal that diverse degradation behaviors occur even under the same stress condition [1]. These degradation phenomenons are deeply affected by the initial parameters of the devices. In order to obtain the more identical experimental results, the initial parameters of the devices should be more uniform and form the same glass substrate. The experiment for the reliability will be discussed in detail in chapter 2.

The LTPS TFTs are found to suffer serious variation of their electrical parameters. The poly-Si material is a heterogeneous material made of very small crystals of silicon atoms in contact with each other constituting a solid phase material. These small crystals are called crystallites or grains. The presence of these crystallites with irregular boundaries means the break in the crystal from one crystallite to the

other. Because the material remains solid, the atoms at the border of a crystallite are also linked to the neighbor crystallite ones. However, these atom bonds are disoriented in comparison with a perfect lattice of silicon. This border is called a grain boundary. As the result of various distributions of grain boundary in the channel of TFTs, the initial characteristics of LTPS TFTs are different from one another, which are shown in Fig. 1-5. The Fig. 1-6 shows site variation of the threshold voltage variation for an LTPS TFT fabrication line plotted in the format of lot trend and the degree of variation can be up to four times of their standard deviation. These variations can be also observed in MOSFETs (Metal-Oxide-Silicon Field Effect Transistors) but they are critical in LTPS TFTs due to the existence of grain boundary. The device variation will lead to the variation of the circuit performance. It will be reflected directly on the image uniformity of the display. For the circuit design, the device variation must be taken into consideration. This condition causes the difficulty in the study of LTPS TFT's device physics since TFT degradation behaviors also become diverse due to device variation.

1-3. Defects in poly-Si TFT

Because of the granular structure of poly-Si film, there are many grain boundaries and intragranular defects exist in the film and the interface of poly-Si film and oxide. The break in the lattice at grain boundary creates dangling bonds and also breaks the periodicity of the potential in the material. In other words, the energy states are created at grain boundaries or the interfaces between poly-Si film and oxide. They act as acceptor-like or donor-like states which depending on the position of the Fermi level in the band gap. Carriers trapped by these trap states can no longer contribute to conduction, which forms local depletion region and potential barriers. Therefore, the

basic characteristics such as subthreshold swing, mobility, ON current and threshold voltage of poly-Si TFTs are inferior to those of the MOSFETs.

1-4. Motivation

The Poly-Si TFTs displays with integrated driving circuits have recently been developed. At present, the poly-Si TFTs are the best candidate to realize system on panel (SOP) and is widely considered for AMLCDs and active matrix organic light-emitting diodes (AMOLEDs).From above discussion, we have known some non-ideal characteristics such as device variation and diverse reliability behaviors. These variations are due to the defects in poly-Si TFTs.

However, before LTPS TFTs can be widely-applied in mass production, yield of the production should be evaluated firstly. The aggressive design strategy will get lower yield while conservative design strategy will underestimate the circuit performance.

Since the variation of device's initial parameters have strong dependence with degradation behavior, the TFTs which have very close layout positions with very slight variation of initial parameters called "crosstie TFTs" are used the to make the diverse degradation behavior become more consistent under the same stressing condition and their impacts for circuit performance will be demonstrated in chapter 2 and 3. The purpose of these studies is to establish reliable C-V models for degradation behavior after stressing and to consider the impacts on the circuit performance influenced by the device C-V curve's degradation. These models will improve the accuracy of the simulation result in HSPICE. Besides, another key factor for application, reliability of LTPS TFTs will be analyzed by means of stress mapping. We will get the identical reliability behaviors and the safe operation conditions for

circuit in the chapter 2.

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Chapter 2

The study of crosstie TFT device's C-V characteristics

2-1.Experimental

As mentioned in section 1-4, the curve of C-V characteristics after certain stressing condition is aimed to be studied. The traditional I-V parameters' extraction of initial condition & after stressing and TFT fabrication are mentioned firstly.

2-1-1. Introduction to crosstie TFTs & device fabrication

Since the device variation is a serious issue in LTPS, it is essential to classify the source of variation. In MOSFETs (Metal-Oxide-Silicon Field Effect Transistors), the local variations can be characterized by short correlation distances and global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performances. If this distance is lower than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g. a charge trapped in the gate oxide layer). For the global variation, which is characterized by process disturbances with longer correlation distances (e.g. the gate oxide thickness across the wafer surface), affects all the devices within a defined region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other.

In order to investigate the relationship between uniformity issue and device distance, a special layout of the devices we adopted in our work is shown in Fig 2-1. The red, blue and yellow regions respectively represent the polysilicon film, the gate

metal and the source/drain metal. The structure of the poly-Si film and the gate metal are in the order that resembles the crosstie of the railroad and therefore this layout is called the crosstie type layout of LTPS TFTs. The distance of two nearest active regions is equally-spaced 40μm. In this small distance the macro variation may be ignored, and the variation of device behavior can therefore be reduced to only micro variation.

Top gate LTPS TFTs with width/length dimension of 20μm / 5μm were fabricated using low temperature process. The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates, then XeCl excimer laser was used to crystallize the a-Si:H film, followed by poly-Si active area definition.

Subsequently, a gate insulator was deposited. Next, the metal gate formation and source/drain doping were performed. A Lightly doped drain (LDD) structure was used on the devices. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. The Fig. 2-2 and Fig 2-3 shows the schematic cross-section structure of the N-type poly-Si TFT with lightly doped drain (LDD) and P-type TFT respectively.

2-1-2. Parameter extraction method

For most of the researches on TFT, the constant current method is widely-used to determine the threshold voltage (V_{th}). The threshold voltage in the thesis is determined from this method, which extracts V_{th} from the gate voltage at the normalized drain current $I_N = I_D/(W_{eff} - L_{eff}) = 10nA$ for V_D=0.1V.

The field effect mobility (Mu, μ_{FE}) is derived from the transconductance g_m. The

transfer characteristics of poly-si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si. The MOSFETs can be applied to the poly-si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \quad (2\text{-}1)$$

Where

C_{ox} is the gate capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If the drain voltage V_D is much smaller compared with $V_G - V_{th}$ (i.e. $V_D << V_G$ - Vth), then the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \quad (2\text{-}2)$$

And the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D$$

Therefore, the field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox}WV_D} g_m \quad (2\text{-}3)$$

We can get the field-effect mobility by taking the maximum value of the g_m into (2-3) when V_D = 0.1V

The subthreshold swing S.S (V/dec) is a typical parameter to describe the gate control toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. For the LTPS TFTs, the subthreshold swing might increase with drain voltage due to short-channel effects. It might as well be affected by the serial resistance and interface traps and therefore

become related to the gate voltage. In our thesis, it is defined as the minimum of the gate voltage required to increase drain current by one order of magnitude for V_D = 0.1V.

$$S.S = \left[\frac{\partial (\log I_{ds})}{\partial V_{gs}} \right]^{-1} \quad (2\text{-}4)$$

2-2. Behavior of C-V curve after stressing

Since it is impossible to observe the defect position in TFTs, what we can do is to stress the TFTs then using C-V measurement checking the position of defect states. The detail procedure will be mentioned in the following.

2-2-1. Stress mapping of N-type and P-type TFTs

In order to use the C-V measurement checking the position of defect states, we have to stress our devices to generate defects in LTPS TFTs. However, the existence of grain boundary in channel will dominate the degradation behavior, so the consistence of the degradation behavior after stressing with different devices becomes an important issue. In prior study [1], the diverse degradation behaviors occur due to different sources of LTPS TFTs and variation of the initial value of extracted parameter. In this work, crosstie layout was adopted to obtain the uniform results. The stress mapping under different stress voltages, including different gate voltage (V_G) and drain voltage (V_D) for the different stress time will be established in this section.

2-2-1-a. Grids of stress map

The Fig. 2-4 shows the four regions of the stress map. The stress condition for region I is defined as the ranges of the stress bias applied to gate (V_G) and the stress

bias applied to drain (V_D), which are from 0V to ±10V and 0V to ±10V, respectively. The region II is defined as the ranges of V_G and V_D, which are from 0V to ±10V and ±10V to ±20V, individually. In the same way, the region III is defined as the ranges of V_G and V_D, which are from ±10V to ±20V and 0V to ±10V. The region IV is defined as the ranges of V_G and V_D, which are ±10V to ±20V and ±10V to ±20V, respectively. The stress condition of region I for V_G is from 0V to ±10V by taking 5V for a step. For the stress condition of V_D is also swept with the same step as V_G. The stress condition of region II for V_G is from 0V to ±10V by taking 2V for a step, and the V_D is from -10V to -20V by also taking 2V for a step. The stress condition of region III for V_G and V_D are from -10V to -20V and 0V to -10V, and the all steps in this region is 2V. The stress condition of region IV for V_G and V_D are both from ± 10V to ±20V and the step is 2V. Furthermore, the condition of stress time is 10sec, 50sec, 100sec, and 1000sec, respectively. We take the fewer grids for stress measurement in region I because the slighter degradation phenomenon we expected in this region. It will be proven in the result we will discuss later.

2-2-1-b. Degradation mechanism & experiment result discussion

The mechanism of degradtion under DC stress for the LTPS TFTs will be introduced in this section. There are several kinds of degradation phenomena in poly-Si TFTs have already been reported [8-16]. The sources of degradation are, for example, hot carriers, self-heating, water, contamination, and electrostatic discharge. The two main sources of degradation are hot carrier and self-heating, which will be described in detail as follows.

Hot carrier effects [10] result from the high electric field near the drain junction have been widely investigated in LTPS TFTs. Conduction carriers can obtain energy from the high electric field and become “hot”. Thus, the carriers with high kinetic

energy can easily break the weak bonds existing in poly-Si, creating many defect states and oxide charges. Serious degradation of N-type TFTs can be generated in the hot carrier operation mode, and the degree of degradation depends on the strength of the electric field. In poly-Si, since the number of trap is larger, the hot carrier effect is accordingly worse. Since the number of trap is larger in poly-Si, the hot carrier effect is accordingly worse. Introducing electric-field-relief TFT structures, such as lightly doped drain (LDD), offset drain, and gate-drain overlapped LDD (GO-LDD), can reduce the hot carrier degradation.

As the gate voltage increases and correspondingly the equivalent lateral electrical field decreases, the hot carrier effect will be reduced. Instead, the power dissipation in the device is becoming high, causing the increase of device temperature due to Joule heat, which is known as self-heating or thermal effects [11]. Since TFTs are fabricated on glass substrate, the heat dissipation to the substrate is relatively low compared with Si substrate and makes the degradation worse. Besides, the influence of self-heating effects will increase with the width of TFTs.

The stress maping under different stress conditions of V_G and V_D is demostrated in Fig. 2-5, Fig. 2-6, Fig. 2-7. The stress maps for threshold voltage under different stress time for P-type TFTs :100sec, 200sec, 500sec,1000sec and for N-type TFTs : 10sec, 50sec, 100sec, and 1000sec, is shown in Fig. 2-5 (a) and 2-5 (b), respectively. Likewise the stress maps for mobility and subthreshold swing under different stress time are shown in Fig. 2-6 (a) and 2-6 (b) and Fig. 2-7 (a) and 2-7 (b).

For the region I, owing to the low electric field and the low power dissipation, we can not obviously observe the phenomenon of device degradation. The operation of TFTs in this region are more reliable for normal circuit purpose.

As for the region II, we can obviously observe the phenomenon of the mobility degradation and V_{th} shift, but slight degradation in S.S. The hot carrier effect

dominates in this region, which generates the hot carrier of the electrons by high lateral electric field in N-type TFTs. They can create interface-trapped charge or some defects near the drain region. We consider that the V_{th} shift owing to fixed charge in oxide, and the mobility degradation due to Coulomb scattering of the fixed chatge. However, there is almost no degradation of S.S in this region, which implies that the device during the stress has few changes in the deep states. This phenomenon also implies that the dangling bonds are neither increased nor created. Moreover, the degradation behaviors apear in a few tens of seconds and tend to saturation as the stress time increasing. We belive that defects generated initially can reduce the electric field and retard the further creation of new defects.

In the region III of stress map, we observe the slighter V_{th} shift and S.S degradation, but it is seem to be no degradation or even slight increase in the mobility. In contrast to region II, the degrees of the degradation in V_{th} shift and S.S are higher than the region I but lower than the region II. The proposed explanation for the different degrees of the degradation phenomena is the lower lateral electric field and the less power than those in the region II. The lateral electric field and the power in this region is relative small compared to region II and IV. Consequently, the hot-carrirer effect and self-heating effect are not so obvious.

For region IV, the degradation phenomena are more complicated. We can obviously observe the serious Vt shift, mobility and S.S degradation. According to these behaviors, we can speculate not only hot carrier effect but also self-heating effect occuring in this region. Owing to the larger power, joule heat drives the hydrogen runs away and dangling bonds are left. For the reason of the increase of the deep states, S.S in this region is suffered form severe degradation. Under the condition of $|V_G|$ and $|V_D|$ which are both higer than 18V, the devices will be burn out during our experiment time. In addition, we can see the continuous

degradation in this region. In other words, the created defects can not slow down or stop the generation of more defects. This observation is consistent with the hypothetic degradation mechanism of the lasting diffusion of hydrogen.

The crosstie layout LTPS TFTs was adopted in our work. In the relative short range, the initial characteristics in these TFTs we used to compelete our stress test are very similar. For this reason, we got the more identical degradation behaviors in our bias stress tests. On the basis of our stress maps, the gate and drain bais (V_G and V_D) will be applied above ±10V for the safe continous opreation for LTPS TFTs. Besides, from the stress mapping, we can find that the serious degradation is occurred in region II and IV. We will use the C-V measurement in these two region.

2-2-3. N-type TFT's C-V characteristic degradation behavior

In this study, the N-type TFTs with a channel width of 20 um and a channel length of 5 um with an LDD structure of length 1.2 um are fabricated. These devices are stressed with a self-heating condition, that is, the gate to source voltage V_{GS} and the drain to source voltage V_{GD} are both 18V. The C-V curves of the gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}) before and after stress with different frequencies are measured with the Agilent 4284A precision LCR meter.

Figure 2-8 shows the I-V transfer curves of the poly-Si TFTs after self heating stress with the time duration of 500s. The higher threshold voltage, lower on current and smaller sub-threshold slope are observed. Y. Uraoka *et, al.* previously reported that the self-heating effect causes the release of hydrogen in the poly-Si film and therefore increases the deep states, resulting in the degradation of sub-threshold region of the I-V transfer characteristics[4]. However, T. Fuyuki *et,al.* also reported that the degradation from self heating may not only increase the trap states in the

poly-Si film but also raise the interface states between poly-Si film and gate oxide, as well as the trap charges in the oxide.

Since the I-V transfer characteristics could not distinguish the dominant degradation mechanism, C-V measurements were therefore employed. Figure 2-9(a) shows the normalized gate-to-source capacitance C_{GS} curves before and after stress with different frequencies, while Figure 2-9(b) shows the corresponding curves of the normalized gate-to-drain capacitance C_{GD}. The C_{GS} is measured with a floating drain and C_{GD} is measured with a floating source. The normalized capacitance is the ratio of the measured capacitance to a constant of 40 fF, which is the gate oxide capacitance of the TFT under test. As shown in Fig.2-9(a), the normalized C_{GS} curves significantly stretch out and shift in the positive direction after stress. In addition, the capacitance of the device after stress increases dramatically as the gate voltage is smaller than the flat band voltage (V_{FB}). Similar degradation behavior may also be observed in the normalized C_{GD} curves, as shown in Fig.2-9(b). For the curves of C_{GS} and C_{GD} after self heating stress, the stretch and shift in the positive direction for the gate voltage near V_{FB} can be explained by the increase of the deep states during stress. However, the additional increase of the capacitance below V_{FB} and the different degrees of the increases in C_{GS} and C_{GD} suggest that there may be another mechanism in the device during self heating stress, which implies the inference from T. Fuyuki [5].

The increases of the C_{GS} and C_{GD} curves for the gate voltage smaller than V_{FB} may come from the interface states near source and the trapped charge in the gate insulator. Nevertheless, it is observed that both C_{GS} and C_{GD} curves for the stressed devices shift in the positive direction at the higher frequency. Since the trapped charges in the gate insulator would not respond to different frequencies, the increases of the C_{GS} and C_{GD} curves for the lower gate voltage may be attributed to the interface states. Moreover, the more apparent increase of C_{GS} below V_{FB} than the one of C_{GD}

may also be attributed to the interface states induced by the higher local electric field between the gate and the source than that between the gate and the drain. It hints of a spatial creation of interfacial states according to the electric field distribution. Furthermore, it is reported that the temperature increase due to the self heating stress near the drain is higher than that near the source and exhibits a spatial distribution[5]. Since the high temperature in the poly-Si film will release hydrogen and increase the deep states, it may be expected that the increase of deep states near the drain will be more obvious. Therefore, a device under self heating stress is expected to suffer the temperature effect near the drain, and the high electric field near the source.

To verify the hypothesis about the damaged regions, a two-dimensional (2-D) numerical simulation program DESSIS was used to simulate the device characteristics. The model of the cross section of the device after self heating stress is shown in Fig.2-10. In the simulation, the grain boundaries inside the poly-Si film are accounted by using the "effective medium approach," which treats the poly-Si film as a uniform material with the density of localized states in the forbidden gap[6]. The deep states are arranged to be gradually decreasing from drain to source according to the temperature distribution under self heating condition. The deep states in the poly-Si film are modeled by a Gaussian distribution near the midgap. The peak value of the deep state density changes from 5×10^{18} to 3×10^{17} cm^{-3} in the range of 0.3um at the drain edge, corresponding to the temperature distribution. On the other hand, the interface states of 1×10^{15} cm^{-2} decreasing to 1×10^{14} cm^{-2} are arranged from the source edge, reflecting the electric field between the gate and source. Fig.2-11 shows the simulation results with different degraded regions in the device. Curve A is the C-V curve with no degraded region, while curve B is the one only with interface states near the source region. Comparing to curve A, curve B increases drastically for the gate voltage below V_{FB}. It reveals that the interface states between the source and the

gate influence the induced carriers in channel depletion and weak inversion conditions. Although the effective medium approach is used in this simulation, the generated surface states may come from the grain boundaries of the poly-Si film near source region. Curve C further includes the increase of deep states in the poly-Si film near the drain. It can be seen that the capacitance not only increases below V_{FB} but also shifts in the positive direction for the gate voltage near V_{FB}. Thus, the shift of curve C near V_{FB} is attributed to more deep states to be filled during weak and strong inversion. The similarity of Curve C and the measured C_{GS} and C_{GD} indicates that the degradation due to self heating stress causes the increases of deep states in the poly-Si film and the interface states near the source. This finding via the C-V measurements may be important for the further comprehension of the degradation caused by self heating stress.

Another stressing condition is called hot carrier stressing condition, that is, the gate to source voltage V_{GS} =2V~threshold voltage and the drain to source voltage V_{GD} is 20V. The degradation of I-V transfer characteristic after stressing 500sec is that the on current decreases significantly but no change is observed in subthreshold region and threshold voltage shown in Fig.2-12.

Previous studies suggest that hot electrons generated by the high electric field around the drain cause the degradation of drain current and channel mobility. Generally, hot electrons induce charge trapping at interface and/or grain boundaries. Hence, there are two possible models: (1) Hot electrons generated by drain avalanche generate electron traps at interface between the gate oxide and poly-Si. (2) Hot electrons generate electron traps at grain boundaries in the poly-Si. In order to verify which hypothesis can explain the experiment result as mentioned above , Y. Uraoka *et, al.* used the two-dimensional simulator ”Medici” analyzing these models.

With increasing the density of states (DOS) locally around drain region in their

simulation, the simulated on current was decreased and no change was observed in subthreshold region shown in Fig.2-13. Previous study's hypothesis can explain the I-V curve's degradation after hot carrier stress but they don't exam their suggestion by C-V measurement or simulation. As shown in Fig.2-14, the normalized C_{GS} curves don't change obviously before and after stress but the normalized C_{GD} curves have a slightly stretch out after stressing 500sec with measurement frequency 1MHz. This phenomenon indicates that only around the drain region does degradation occur. By increasing the density of states (DOS) locally around drain region in our simulation, we find that the simulated Capacitance-Voltage curve has stretch out slightly as shown in Fig.2-15. The simulation result and model structure shown in Fig.2-16 is quite consistent with our experiment result and have a perfectly response to the previous study. In crystal silicon, hot carriers increase the interface states density or generate traps in the oxide. However, in the case of poly-Si TFT, hot carriers increase the DOS of poly-Si near drain, causing the decrease of mobility.

2-2-2. P-type TFT's C-V characteristic degradation behavior

Since the I-V behaviors of the N-type TFTs were studied in previous section, for the DC stress condition of V_G = -18V and V_D = -18V, we want to find what mechanism dominate the degradation behavior compared to the N-type TFTs. Fig.2-17 shows the I-V transfer curves of the P-type poly-Si TFTs after self heating stress with the time duration of 1000s. The larger threshold voltage value, lower on current and shifting of sub-threshold slope are observed.

C-V measurements are also further employed to investigate the asymmetry electric fields at the source and drain of TFTs during the stress. Fig. 2-18(a) shows the gate-to-drain capacitance C_{GD} curves before and after stress with different frequencies,

while Fig 2-18(b) shows the corresponding curves of the gate-to-source capacitance C_{GS}. The C_{GD} curve is measured with a floating source and C_{GS} curve is measured with a floating drain. The C-V curves are plotted with normalized value of capacitances as mentioned in previous section. Observed from Fig. 2-18(b), all curves remain unity and show no obvious differences as the gate voltage is larger than the flat band voltage V_{FB}, and fall to almost zero sharply around the flat band voltage V_{FB}. However, the extra increase for the positive gate voltage of C_{GS} curve may be attributed to the interface trapped charges, which may be caused by the high voltage difference between gate and source during the stress. And the increase of lower part of C_{GD} is the same mechanism as mentioned in n-type TFT under self-heating.

In the case of P-type TFTs as shown in Fig. 2-18, the C-V curve shift in the negative direction parallel to the C-V curve before stressing, may be attributed to the increase of the effective trap charges. Different from that of N-type TFTs, the increase of C_{GS} of P-type TFTs for the positive gate voltage is almost independent of the frequency. It reveals whether the dominant degradation mechanism is trap states or fixed traps. The trap states generated by the DC stress respond to the small signal while the fixed trap charges are not affected by the applied frequencies [6]. The hot electrons in the N-type TFTs are easier generated than the hot holes in the P-type TFTs. Thus, unlike the N-type TFTs, the dominant instability mechanism for the P-type TFTs would be the trapped charges induced by electric filed instead of the trap states generated by the hot carrier.

For the gate voltage of -18V is much higher than the source voltage of 0V during stressing, holes would be attracted by the gate and trapped at the interface between the oxide and the poly-Si film near the source region.

As for the overall channel of the TFTs, it is believed that the generation of defect states are not created in poly Si film since the substhreshold swing is not altered. The

C-V measurement results further support the creation of the trap states at the surface near source. The slightly increase of C_{GS} for the positive gate voltage indicates the increase of capacitance which may be induced by the traps near source. However, C_{GD}'s lower part does not change after stress because the electric field between gate and drain is lower than that between gate and source.

In order to verify the hypothesis that the traps at the interface near the source is owing to the gate to source electric field, another experiment is planned. For the DC stress condition of V_G = -18V and V_D = V_S = 0V, we want to verify that our hypothesis is valid. As shown in Fig 2-19(a) and (b), gate-to-drain capacitance C_{GD} curves before and after stress with different frequencies and gate-to-source capacitance C_{GS} curves before and after stress all have the extra increase for the positive gate voltage. The experiment result is consist with the hypothesis that it is attributed to the interface trapped charges, which may be caused by the high voltage difference between gate to source and gate to drain during the stress.

A two-dimensional (2-D) numerical simulation program DESSIS was also used to simulate the device characteristics. The model of the cross section of the device after DC stress is shown in Fig 2-20. In the simulation, the grain boundaries inside the poly-Si film are accounted by using the "effective medium approach," which treats the poly-Si film as a uniform material with the density of localized states in the forbidden gap. In this simulation, the maximum interface charges of 1 x 10^{14} cm^{-2} decreasing to 1 x 10^{13} cm^{-2} are arranged near the source edge, which is the influence of voltage difference between the gate and drain (we demonstrate only the side : gate to drain because the degradation is symmetrical). Fig 2-21 shows the simulation results with and without degraded regions in the device. Curve A is the C-V curve with no degraded region, while curve B is the one with interface charges near the drain region. Comparing to curve A, curve B increases slightly for the positive gate

voltage. It reveals that the interface charges between the drain and the gate influence the number of induced carriers in channel depletion and weak inversion conditions.

Hot carrier stressing condition, that is, the gate to source voltage V_{GS} = -2V~threshold voltage and the drain to source voltage V_{GD} is -20V is also discussed. Previous study of p-type TFT's degradation behavior under hot carrier stress is that the increase of mobility, the increase of on current and no obvious degradation on subthreshold swing. Our p-type TFT under hot carrier stress also shows the same degradation behavior as mentioned before shown in Fig 2-22. The degradation mechanism of p-type TFT is commonly considered as: the increase of on current and the increase of transconductance without any variation of subthreshold slope and threshold voltage maybe attributed to facts that the interface characteristics of the channel was not affected and the effective channel length was reduced during hot carrier stress. It has been reported that these phenomenon are caused with the electron trapping into gate insulator near the drain. When the electrons are trapping into gate insulator near the drain, the holes are accumulated in the channel edge near the drain due to local electrical field so that the effective drain region is extended to the active channel.

C-V measurements are also further employed to investigate the degradation mechanism. If the charge trapping phenomenon occurs, the shifting of C-V curve should be observed. But our measurement result shown in Fig 2-23(a) and (b), gate-to-drain capacitance C_{GD} curves after stress with different frequencies have the extra increase for the positive gate voltage and gate-to-source capacitance C_{GS} curves before and after stress all almost no variation. The hypothesis of previous study doesn't commit with our experiment result since the C-V curve doesn't shift. The increase of C_{GD}'s lower part may be the interface damage between gate and drain. It is supposed that the acceptor like traps dominates the degradation behavior when the

gate voltage sweeps to the positive bias. Under the condition that the gate bias is positive, the damaged region and the drain region forms effectively as a pn junction. Thus the additional increase of C_{GD} may be the capacitance of this effective pn junction. But this may be an abrupt pn junction since the capacitance-voltage curve is proportional to the gate bias not to the inverse of the square of gate bias' value. The roughly calculation of the degradation length in channel is shown in Fig 2-24. It is concluded that the degradation channel length is 0.1um, and the acceptor like trap concentration is 10^{16} cm^{-3} . The simulation structure is shown in Fig 2-25 with the parameters mentioned above. The I-V simulation result is quite consistent with measurement resul shown in Fig 2-26.

2-4. Discussion

The C-V behaviors of the N-type TFTs were studied in our previous work [4]. For the critical DC stress condition of V_G = 18V and V_D = 18V, it was found that the degradation contains not only the increase of the deep states inside the poly-Si film but also the increase of interface states between the poly-Si film and the gate insulator, owing to the high voltage difference between gate and source and heat of the device during the stress.

Besides, the degradation of C-V behavior is due to the tail states' generation near the drain edge, by increasing the density of states (DOS) locally around drain region in our simulation, we find that the simulated result is quite consistent with the experiment result as mentioned in the previous sections.

It was reported that the activation energy of electron to inject into the gate oxide is about 3.2 eV and that of hole is about 4.3 eV [8], which means that the probability of electron trapping is larger than hole trapping. But the trapped holes in gate oxide

lead to the degradation of P-type TFT can be considered as a degradation factor from our measurement of C-V curve's shifting after stress. On the other hand, the hot holes are so few that the states creation in the P-type TFT is much less than that in the N-type TFT. Therefore, the electrical degradation of the P-type TFTs is very different from that of N-type TFTs.

Chapter 3

Effects of parasitic capacitance on circuit performance

3-1. Introduction to the ring oscillator

One of the most popular ways of realizing digital-output MOS VCOs is to use a ring oscillator and add voltage control to it. A ring oscillator is realized by placing an odd number of open-loops inverting amplifiers in a feedback loop. The simplest type of amplifier that can be used is a simple digital inverter, as shown in Fig 3-1. This circuit is a form of negative feedback, but since each inverter has approximately 90 degrees phase shift as its unity-gain frequency (assuming that all the loads on the inverters are matched and that the there are at least three inverters in the loop) it is guaranteed that the loop gain will still be greater than unity when the phase shift around the loop becomes greater than 180 degrees. As a result, the circuit is unstable and oscillations occur. Each half-period, the signal will propagate around the loop with an inversion.

In most integrated ring oscillators, fully-differential inverters are used to obtain better power-supply insensitivity. When this is done, an even number of inverters are used to obtain better power-supply insensitivity. When this is done, an even number of inverters can be used and the inversion required around the loop can be achieved by simply inter-changing the outputs of the last inverter before feeding them back to input, as shown in Fig 3-2. These quadrature outputs are very useful in many communication applications such as quadrature modulators and some clock-extraction circuits.

Besides the application in phase-locked loops and clock and data recovery

circuits, the RO is sensitive to the device's parameters. When it comes to analysis and modeling, RO is a proper circuit for estimating what parameter's modification dominates the output waveform's oscillation frequency. That's the reason why we choose ring oscillator for the observation of capacitance effect on circuit performance.

3-2. Impact of the circuit performance with the consideration of proposed parasitic capacitance models

When compared to CMOS, LTPS TFTs suffered form more serious device model's non-accuracy. In order to evaluate the circuit performance of ring oscillator done by LTPS TFTs, the degradation models we mentioned before can be adopted to simulate the circuit performance. The detail of circuit simulation and the comparison of other simulation skills and models will be discussed in the next section.

In this section, we use a commonly-used ring oscillator configuration, which maybe the simplest function block, to examine the circuit performance affected by device's C-V model. The simulation will be done by different model and different stage numbers. There are several factors having influence on C-V curve modeled in H-spice as shown in the table.

Parameter's name	Unit	Default value	Description
CAPMOD	-	0	Model capacitance selector (zero is recommended)
CGDO	F/m	0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0	Gate-source overlap capacitance per meter channel width
ETAC00	1/V	0	Capacitance subthreshold coefficient of

			drain bias
RDX	Ω	0	Resistance in series with C*gd*
RSX	Ω	0	Resistance in series with C*gs*

For the C-V model, ETAC00 has almost no influence on curve's shifting or stretching. Since the TFT doesn't have overlap capacitance, CGSO and CGDO are set to the value of zero. The parameter RDX and RSX can shift the C-V curve with the value about 10^16 Ω, but the resistance value is too large. From the mention above, it is not reasonable to modify the degraded C-V model with built-in parameters.

Now we proposed a new modification method as following: (1) shift the threshold voltage (2) fitting the measurement value of additional degradation capacitance with polynomial function of V_G (3) add a switch between degradation capacitance and gate. The modified C-V curve and measured C-V curve are compared in the Fig 3-3. We can observe that the modeling C-V is quite consist with the measurement curve.

With the implantation of the modified capacitance model, we are going to see the impact on circuit performance. The circuit structure of simulation is shown in Fig 16, that is an inverter chain of even number and a NAND logic gate which acts as another inverter connecting chain's input and output. The size of the N-Type and P-Type TFT is W/L = 20/5 um. The threshold voltage in spice model is the average value of measurement. As shown in Fig 16, we can find that with consideration of degraded capacitance, the output waveform have serious delay compared to the normally ring oscillator. Even with lager threshold voltage or smaller mobility (with only half value of the measured mobility), the degradation degree is not comparable to the capacitance degradation's impact on circuit performance.

3-3. Discussion and conclusion

We have proposed a model of the device capacitance describing the degraded capacitance. It provides a simulation result of the circuit performance compared with non-degraded circuit simulation or other degradation simulation with changing parameters in TFT's spice model. The modification model can be applied to the simulation for the consideration of capacitance effect using a capacitance as a polynomial of gate voltage and a switch without changing the TFT model in SPICE.

Chapter 4

Conclusion

In this thesis, the electrical reliability and the degradation behaviors of LTPS TFT's C-V characteristics are investigated. In prior study, reliability behaviors will be strongly relative to initial characteristics of TFTs. For this reason, a special layout of TFTs called "crosstie" is adopted in this work. By introducing this kind of TFTs, we can get the more consistent reliability behaviors. Besides, most degradation mechanisms are discussed by I-V transfer characteristics rather than C-V transfer characteristics. Two kinds of degradation behaviors' mechanism are discussed by I-V transfer characteristics and C-V transfer characteristics means of not only measurement result but also the simulation tool. It is found out that not only the hot carrier stress degradation but also the self heating stress in N-type TFT and P-type TFT is quite different. Interface damage near drain edge is the degradation dominant mechanism in P-type TFT but the deep states creation in poly-silicon grain boundary near drain dominates N-type TFT. Further more, the self-heating degradation in P-type TFT having a shift in C-V curve implies the possibility of oxide trapping and so does the N-type TFT. Nevertheless, N-type TFT suffers not only temperature effect near drain but also high electrical field's damage near the source. These mentions above are proved by measurement result and simulation. The fitting of proposed models in SPICE with measurement result is also concluded. In the fitting model we, it can be observed that the shape of curve is almost consistent with the measurement result. In addition, the implementation of degraded capacitance in the ring oscillator is simulated. The simulation with the consideration of capacitance effect due to the

stress and the comparison with normal working ring oscillator are demonstrated. It is observed that the capacitance effect have serious influence on the oscillation frequency. Finally a simulation method of reliability model is provided, and the modification model can be applied to the simulation for the consideration of capacitance effect using a capacitance as a polynomial of gate voltage and a switch without changing the TFT model in SPICE.

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Figure Captions

power-supply rejection

Fig. 3-3 Effect of degraded capacitance in circuit simulation

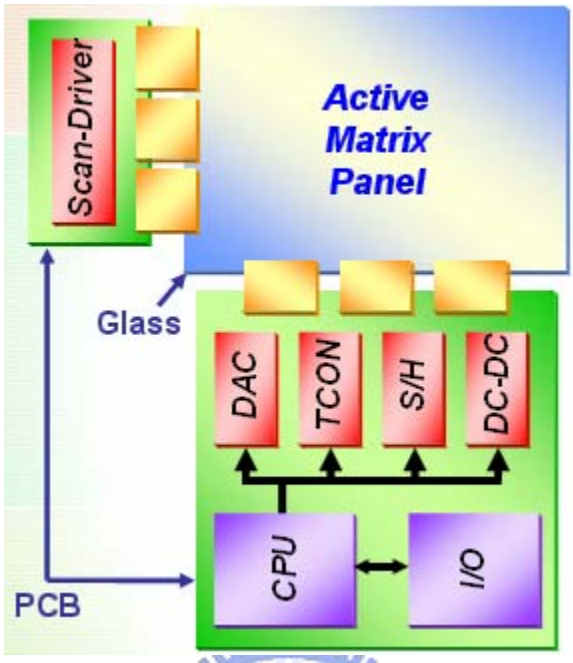


Fig. 1-1 The block diagram of active matrix display

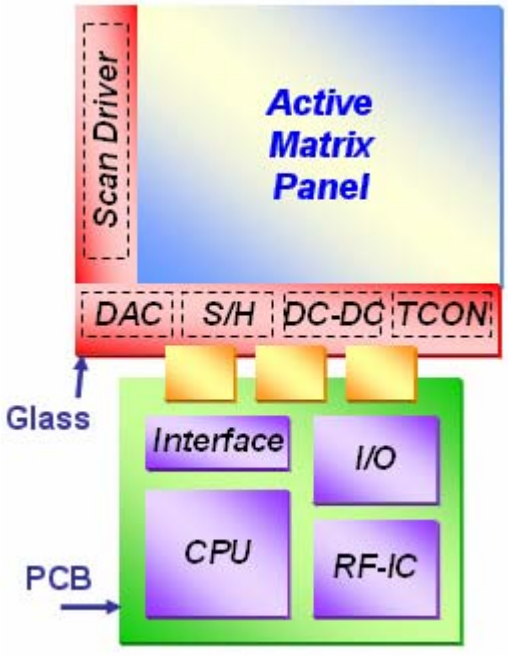


Fig. 1-2 The integration of peripheral circuits in display achieved by poly-Si TFTs

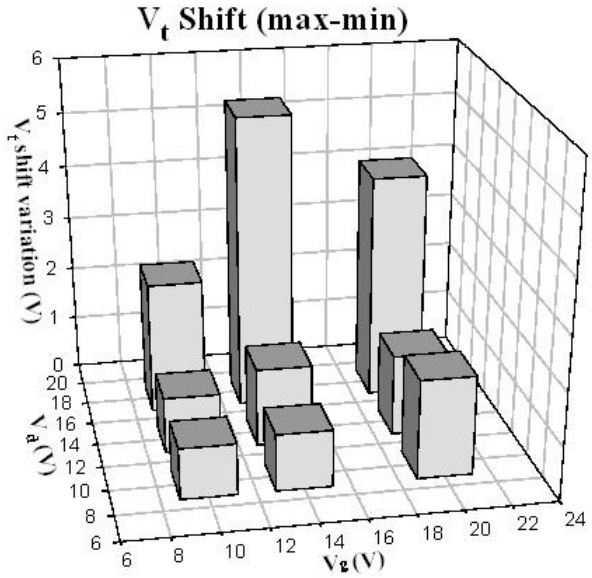


Fig. 1-3 The variation of threshold voltage shift under different stress conditions

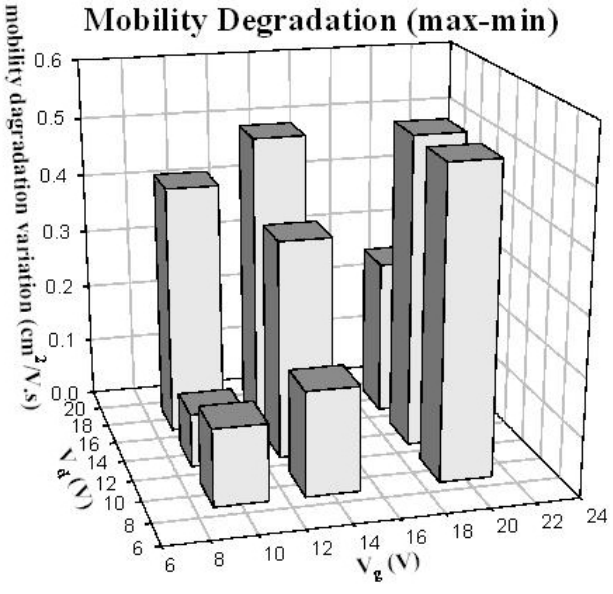


Fig. 1-4 The variation of mobility degradation under different stress conditions

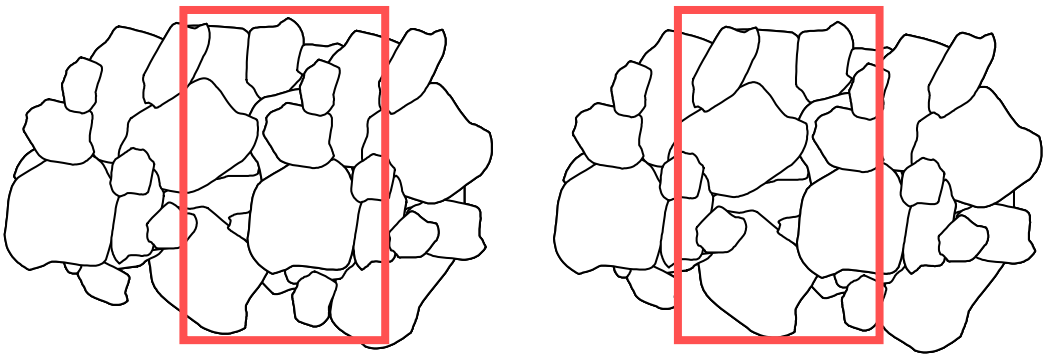
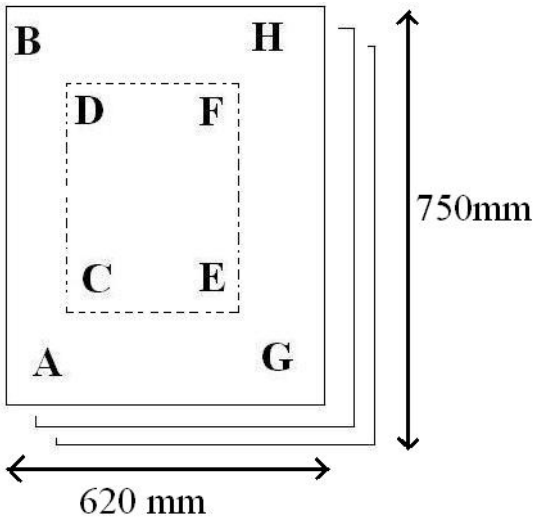


Fig. 1-5 The initial characteristics of LTPS TFTs are different from one another due to various distributions of grain boundaries



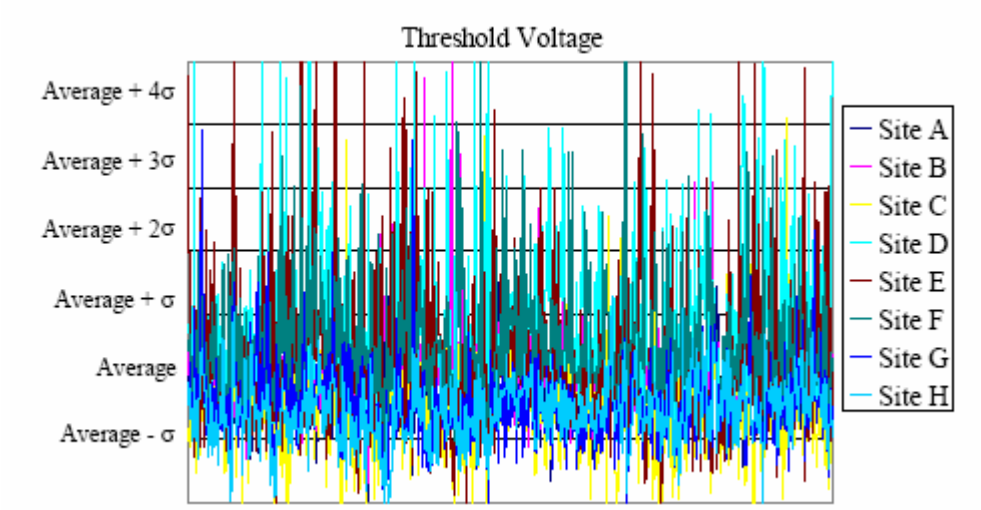


Fig. 1-6 The site variation of the threshold voltage variation for an LTPS TFT fabrication line plotted in the format of lot trend

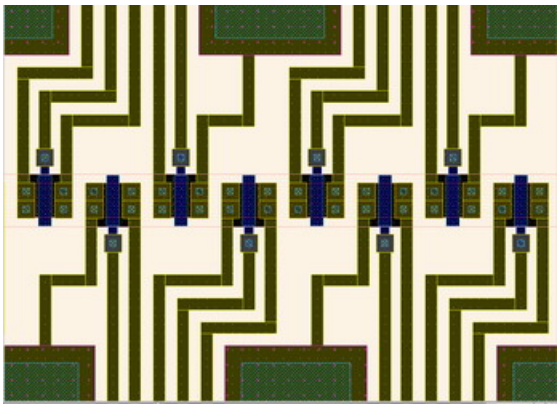


Fig. 2-1 The layout of the crosstie TFTs

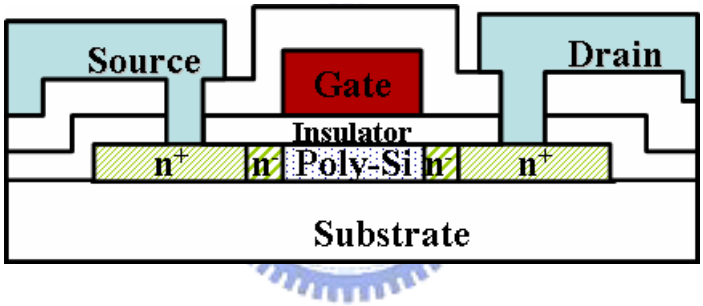


Fig. 2-2 The schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain

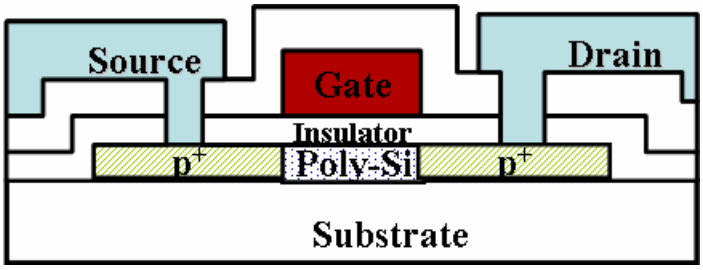


Fig. 2-3 The schematic cross-section structure of the p-type poly-Si TFT

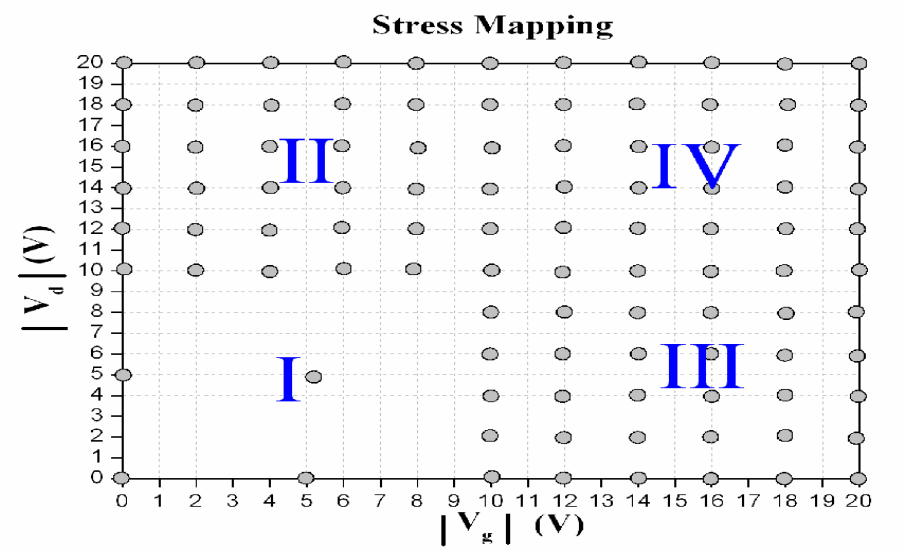


Fig. 2-4(a) The grids of stress mapping for p-type crosstie TFTs

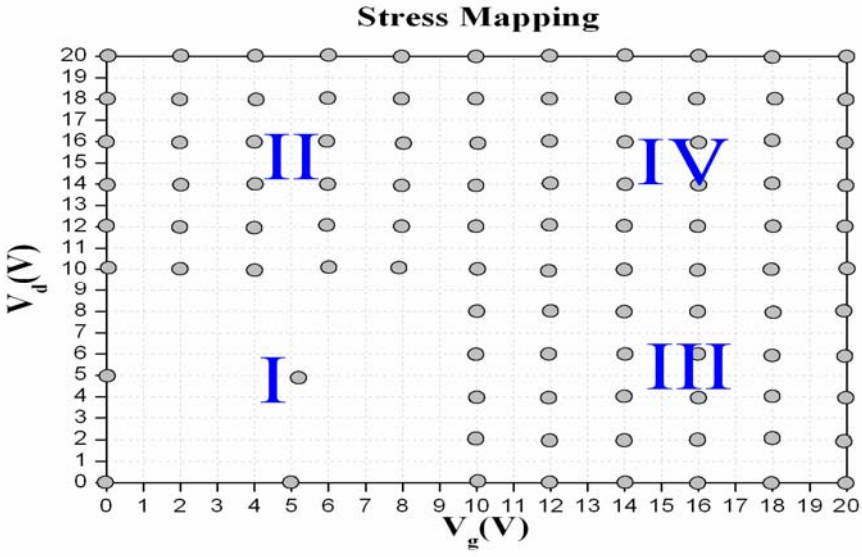


Fig. 2-4(b) The grids of stress mapping for n-type crosstie TFTs

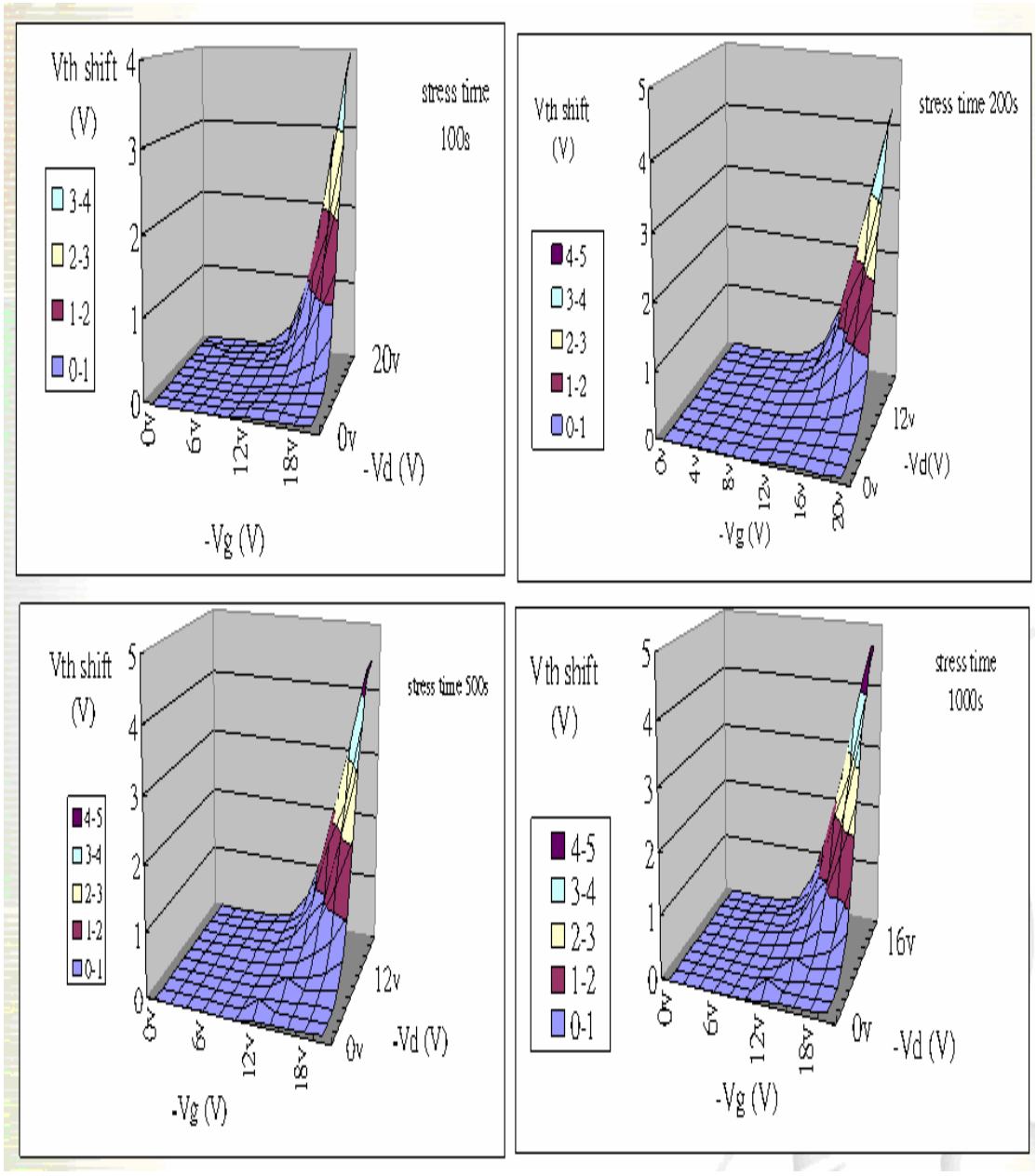


Fig. 2-5(a) The distributions of the threshold voltage's shifting for p-type crosstie TFTs after 100sec, 200sec, 500sec, 1000sec stress respectively

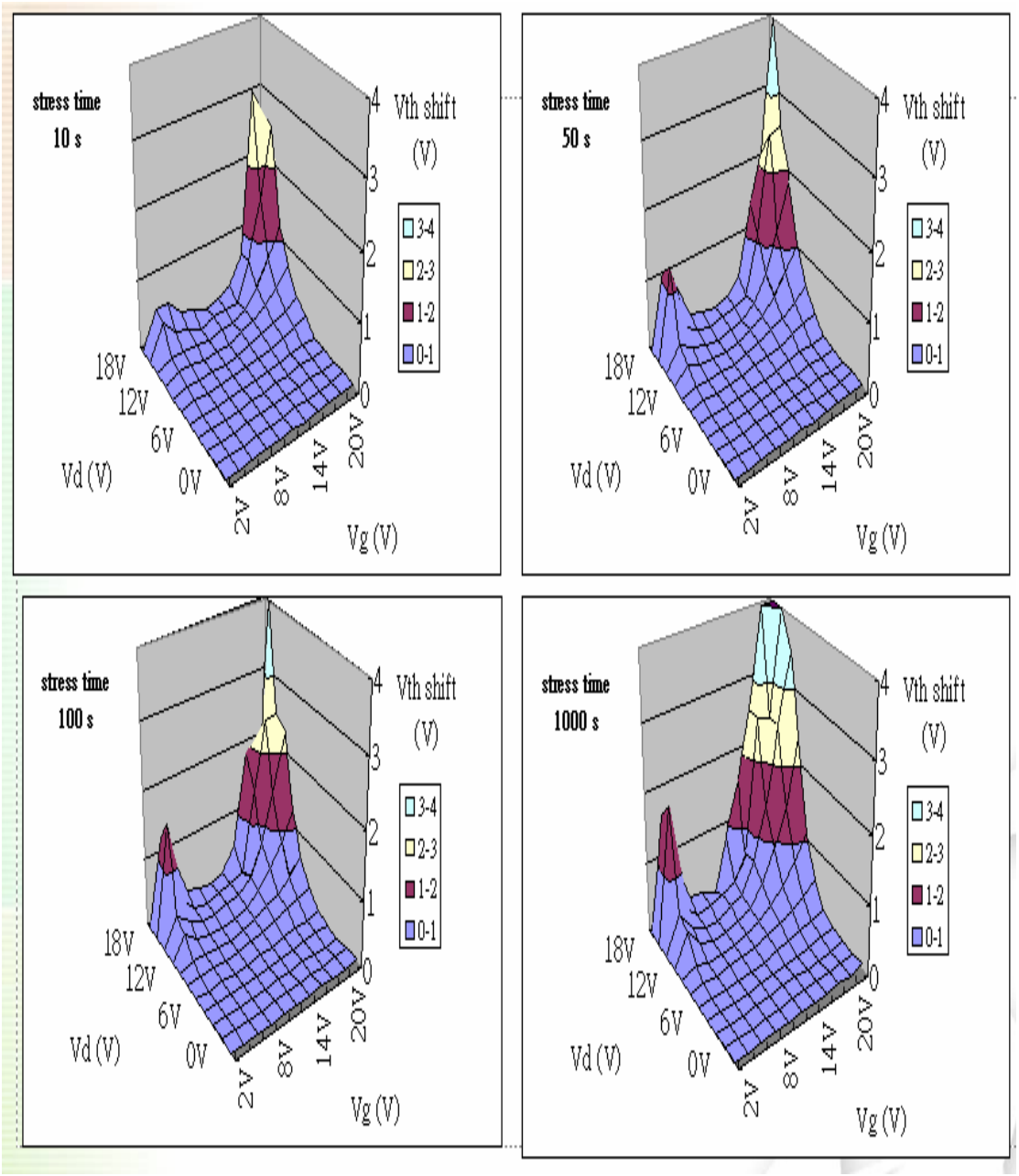


Fig. 2-5(b) The distributions of the threshold voltage's shifting for n-type crosstie TFTs after 10sec, 50sec, 100sec, 1000sec stress respectively

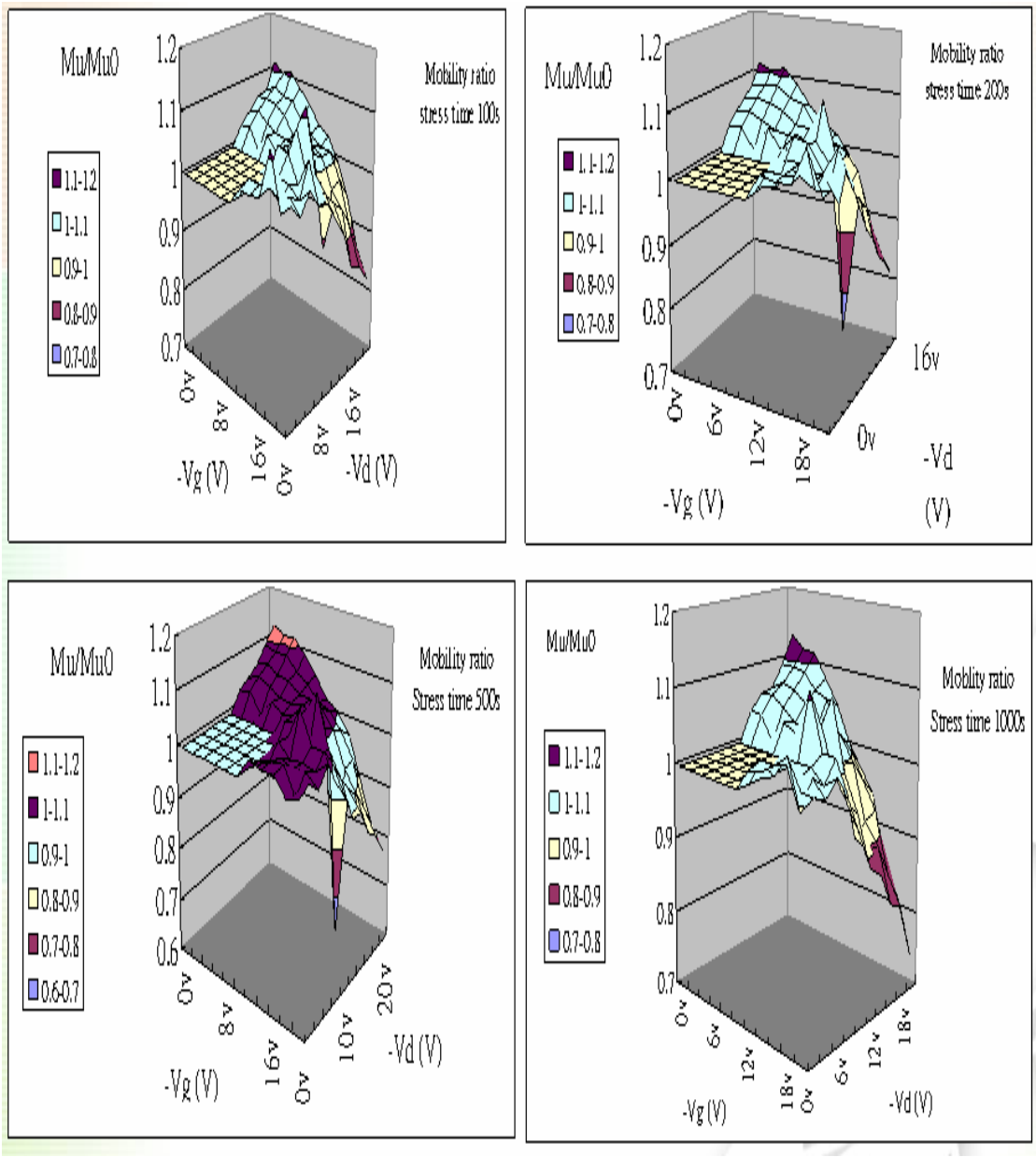


Fig. 2-6(a) The distributions of the mobility's degradation for p-type crosstie TFTs after 100sec, 200sec, 500sec, 1000sec stress respectively

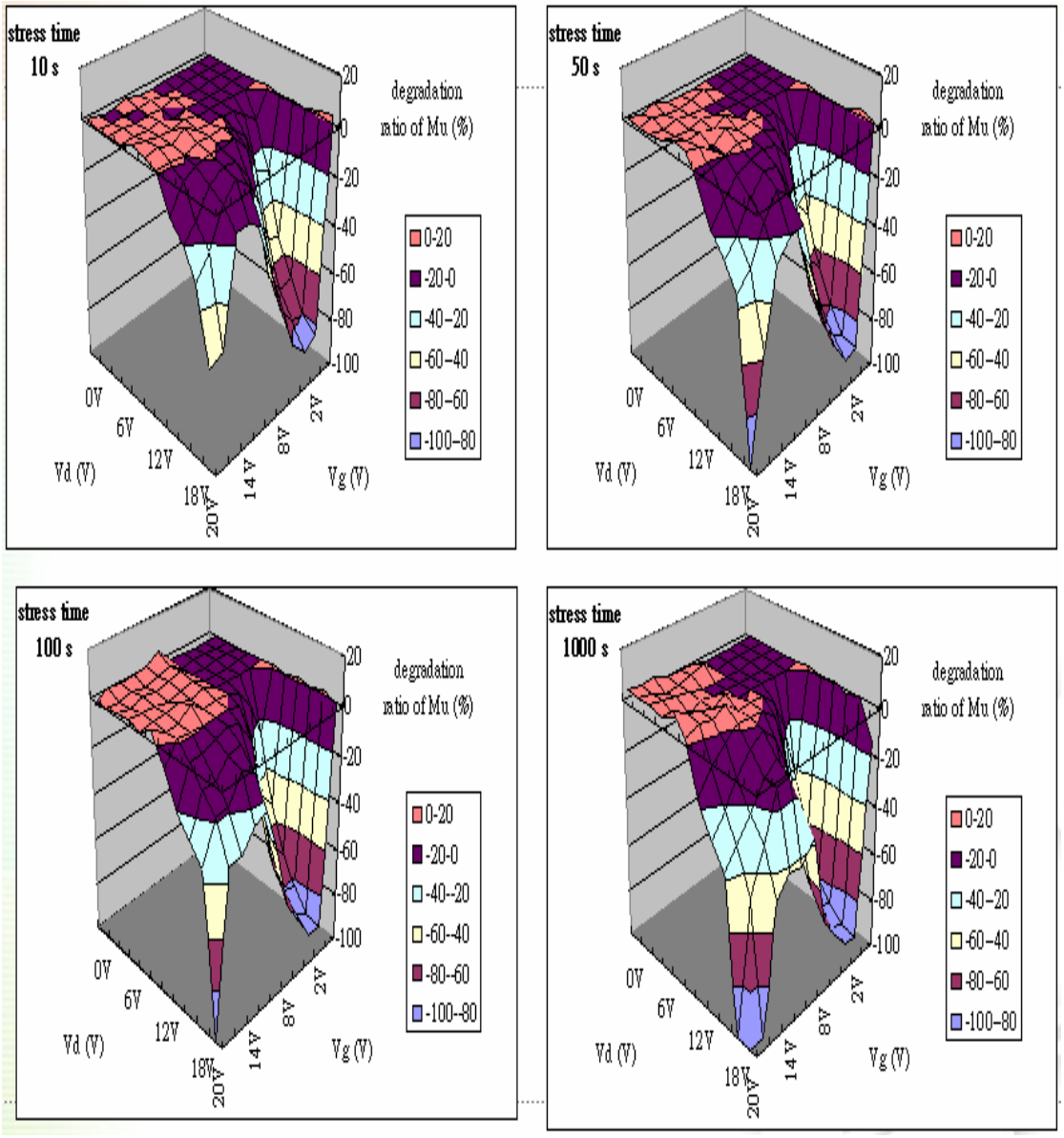


Fig. 2-6(b) The distributions of the mobility's degradation for n-type crosstie TFTs after 10sec, 50sec, 100sec, 1000sec stress respectively

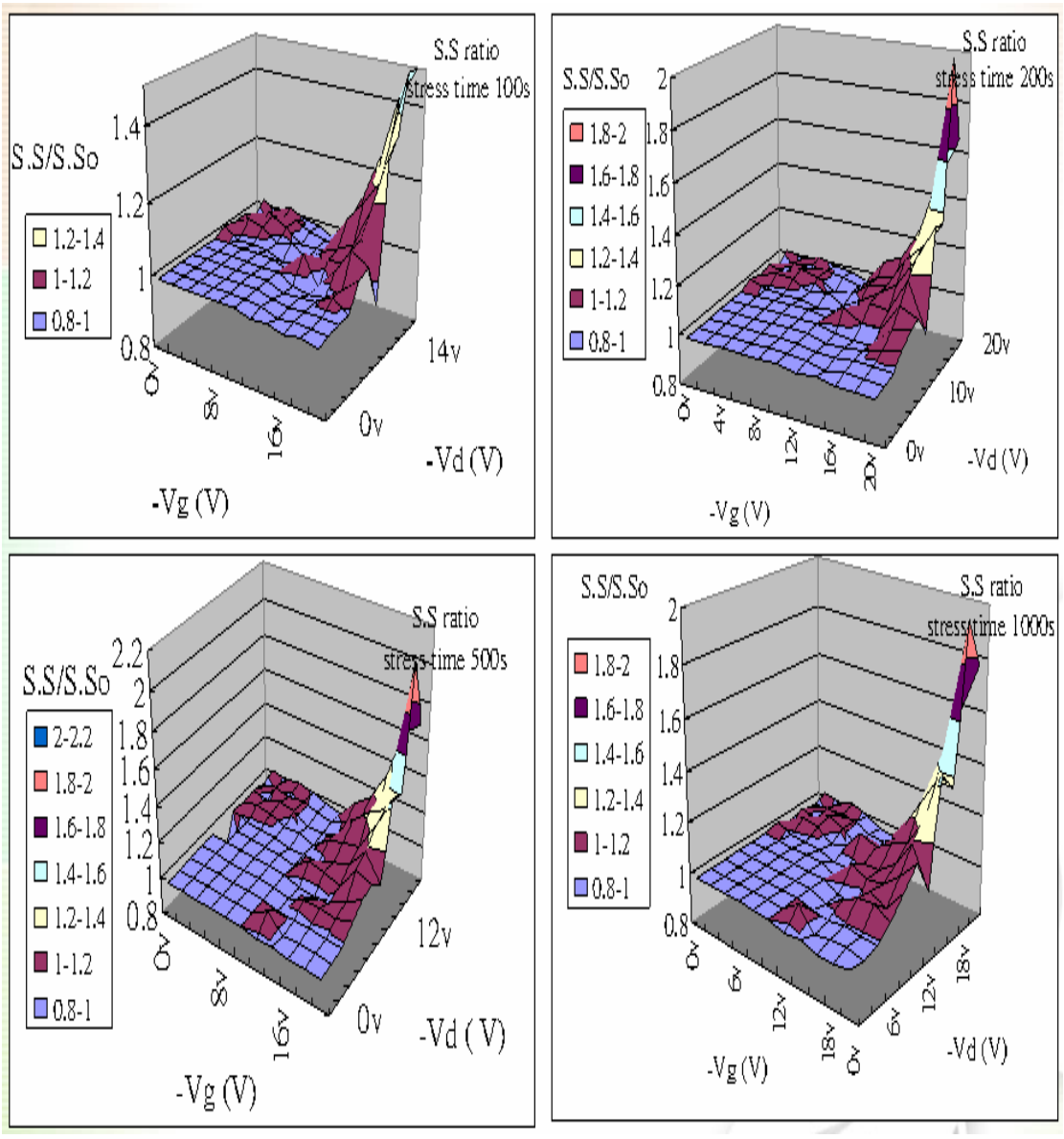


Fig. 2-7(a) The distributions of the subthreshold swing's degradation for p-type crosstie TFTs after 100sec, 200sec, 500sec, 1000sec stress respectively

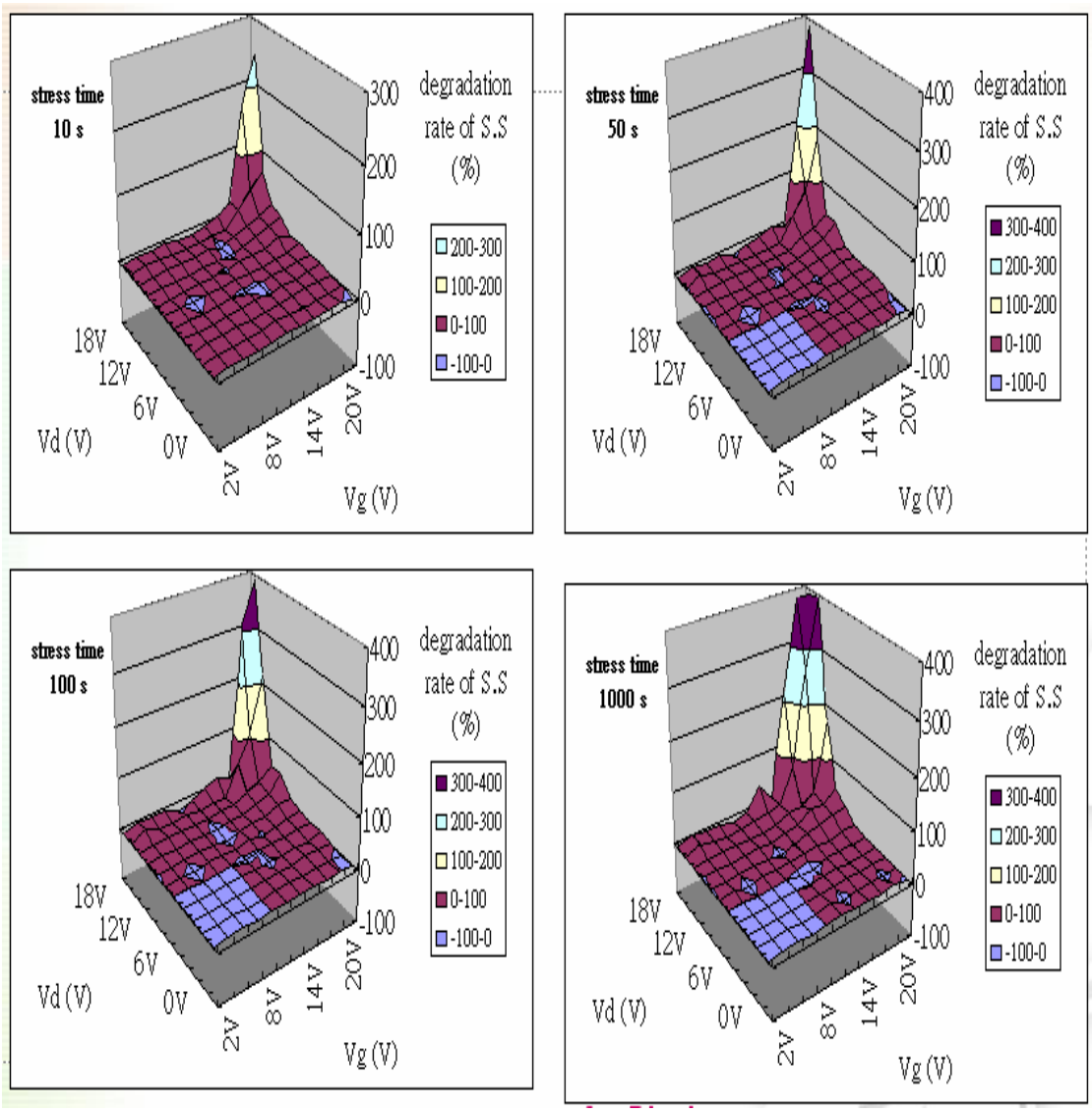


Fig. 2-7(b) The distributions of the subthreshold swing's degradation for n-type crosstie TFTs after 10sec, 50sec, 100sec, 1000sec stress respectively

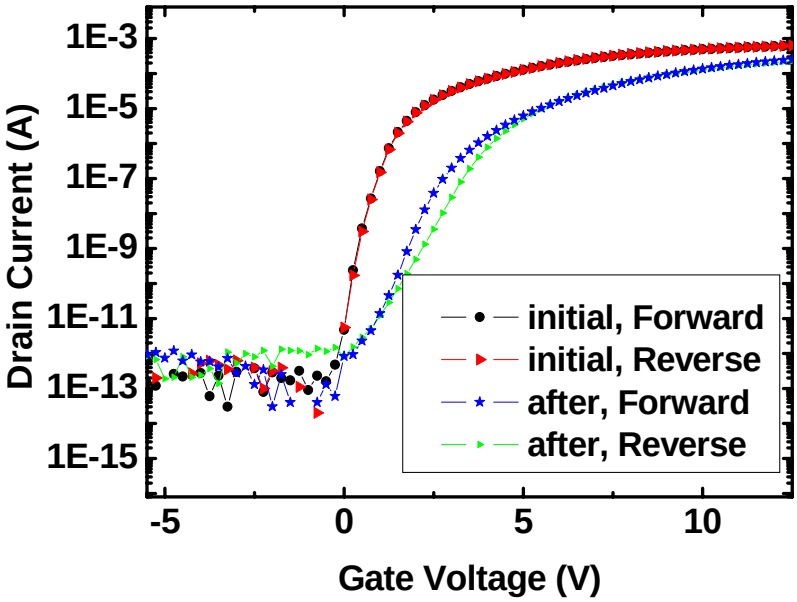


Fig. 2-8 I-V transfer curves of the poly-Si TFTs after self heating stress with the time duration of 500s

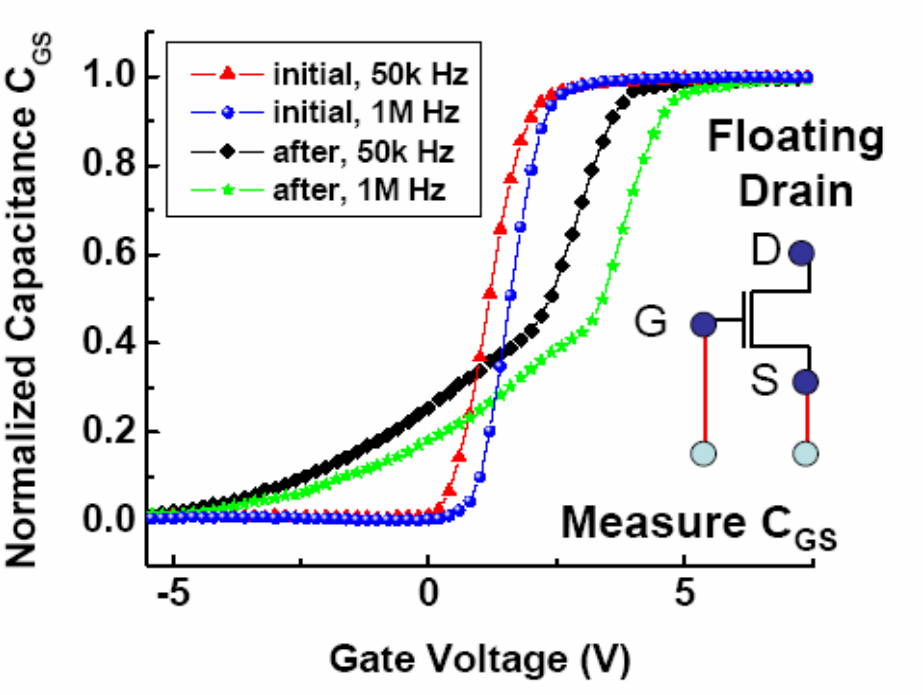


Fig. 2-9(a) The normalized gate-to-source capacitance C_{GS} curves before and after stress with different frequencies

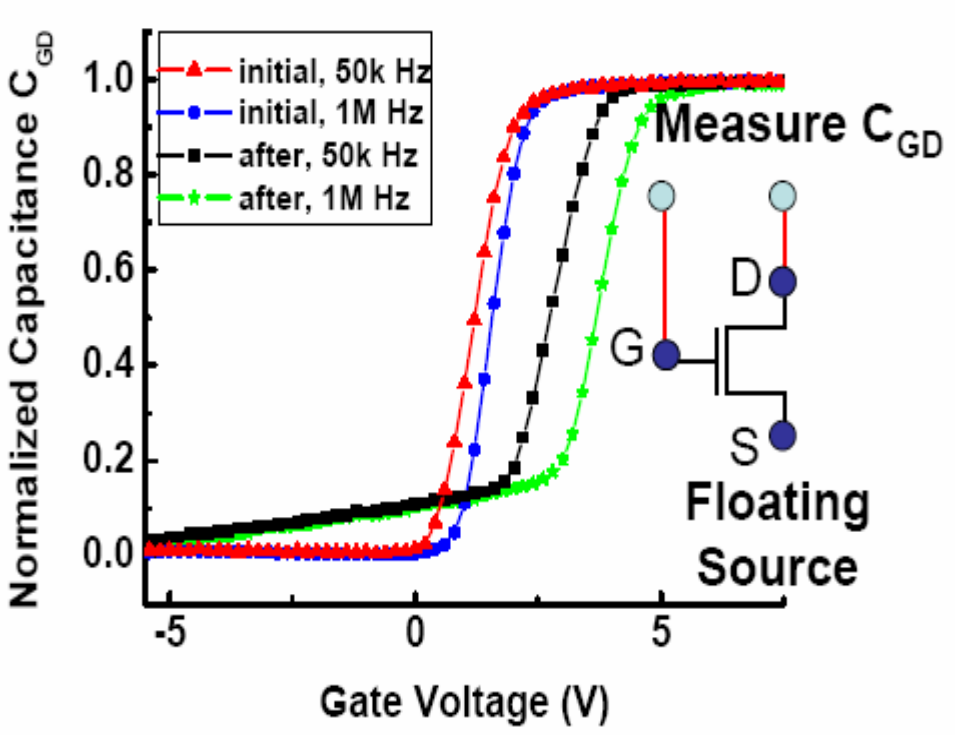


Fig. 2-9(b) The normalized gate-to-source capacitance C_{GD} curves before and after stress with different frequencies

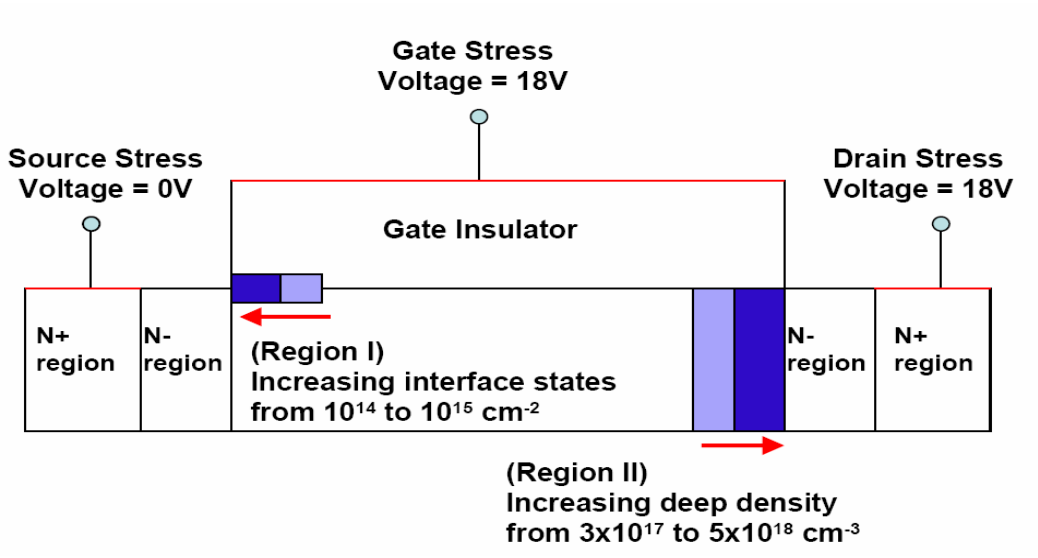


Fig. 2-10 The model of the cross section of the device after self heating stress

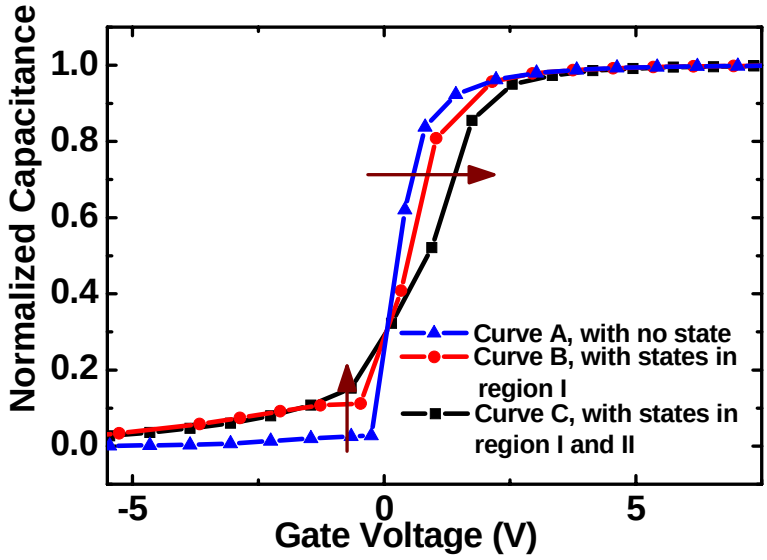


Fig. 2-11 Simulation results with different degraded regions in the device. Curve A is the C-V curve with no degraded region, while curve B is the one only with interface states near the source region

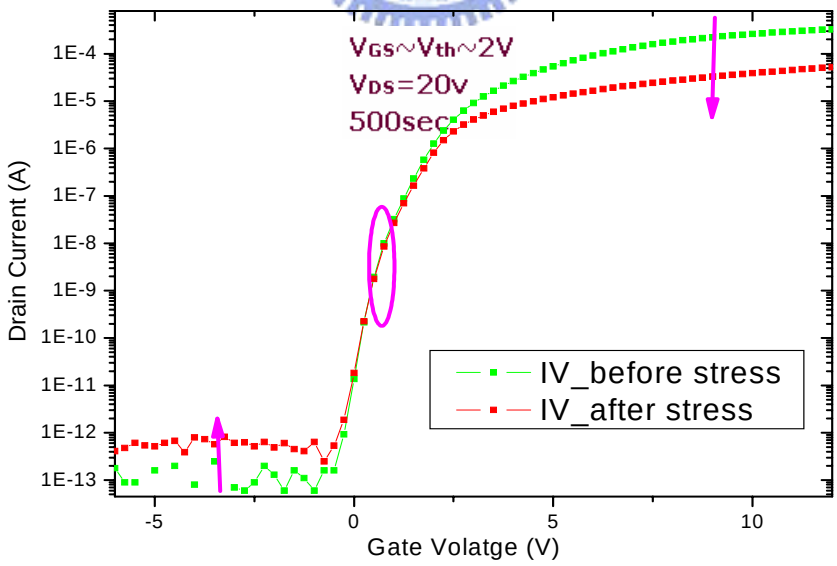


Fig. 2-12 The degradation of I-V transfer characteristic after hot carrirer stressing 500sec

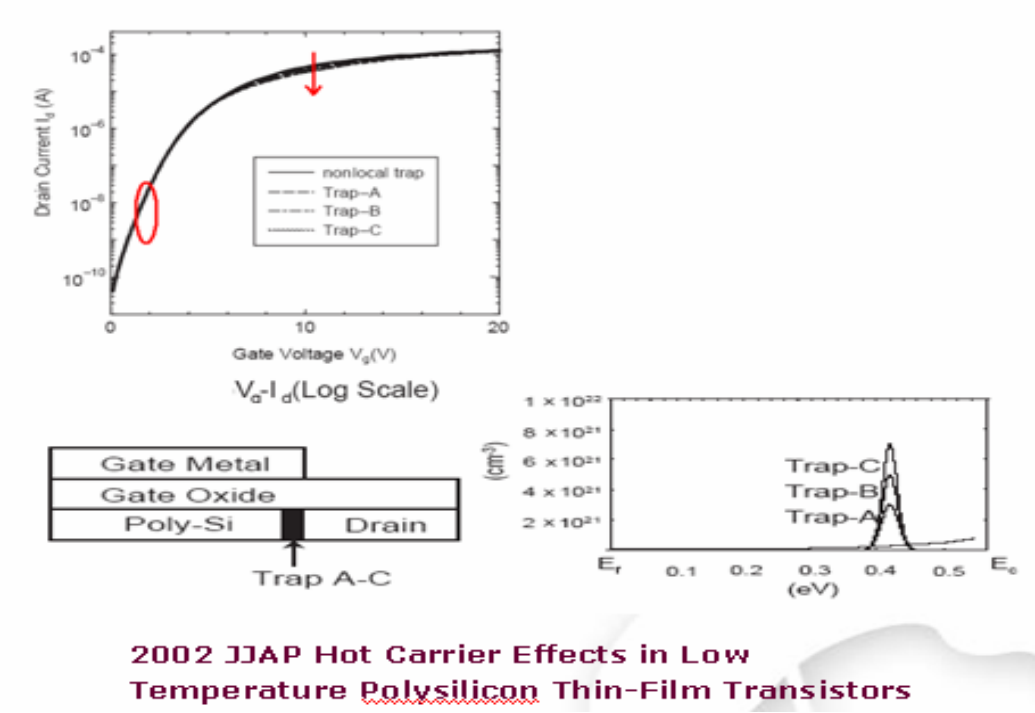


Fig. 2-13 With increasing the density of states (DOS) locally around drain region in previous paper's simulation, the simulated on current was decreased and no change was observed in subthreshold region

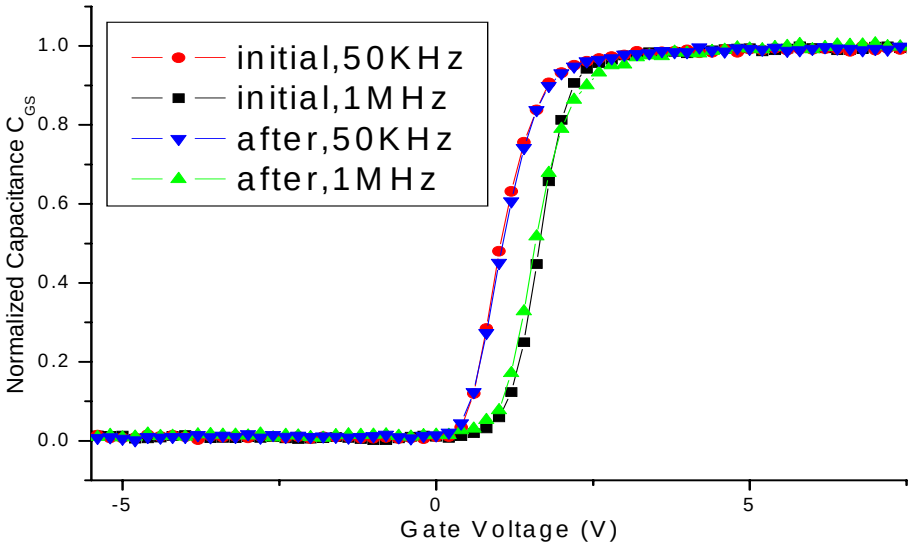


Fig. 2-14 Normalized C_{GS} curves don't change obviously before and after hot carrier stress 500sec

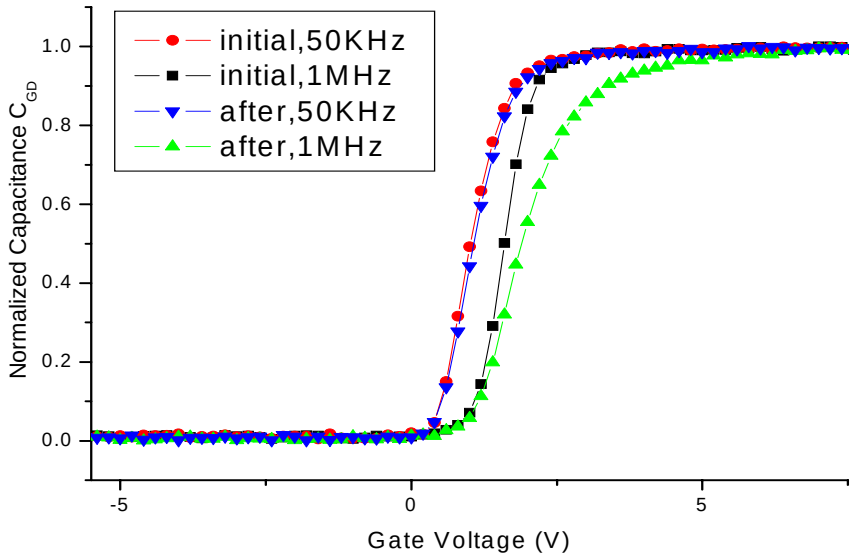


Fig. 2-15 Normalized C_{GD} curve stretchs out before and after hot carrier stress 500sec at measurement frequency 1MHz

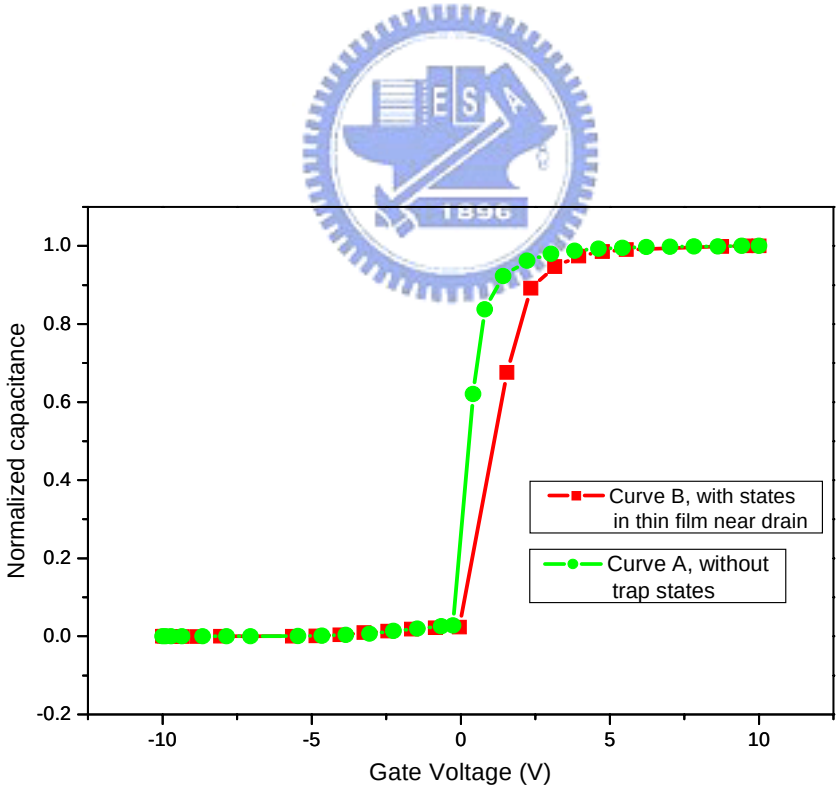


Fig. 2-16(a) The simulation result of C-V curve before and after hot carrier stress

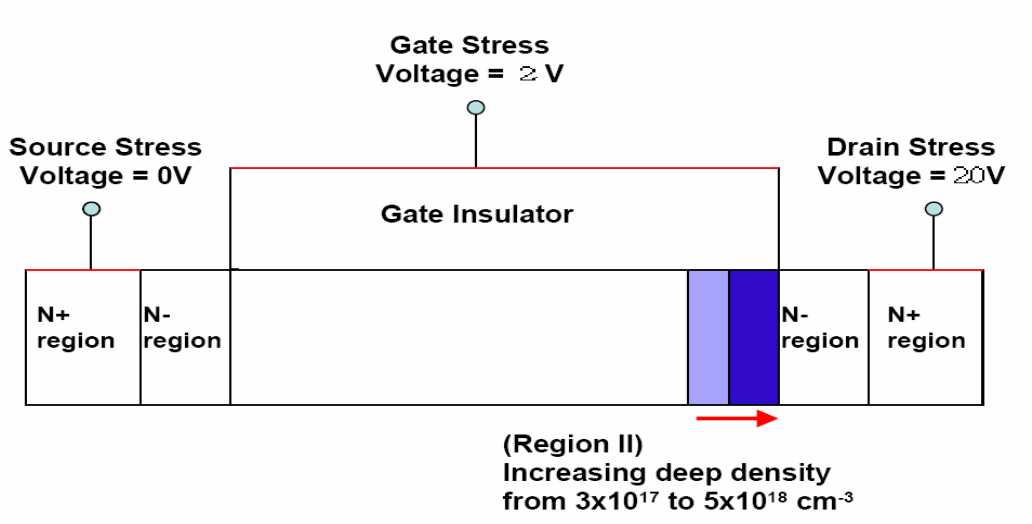


Fig. 2-16(b) The model of the cross section of the device after hot carrier stress

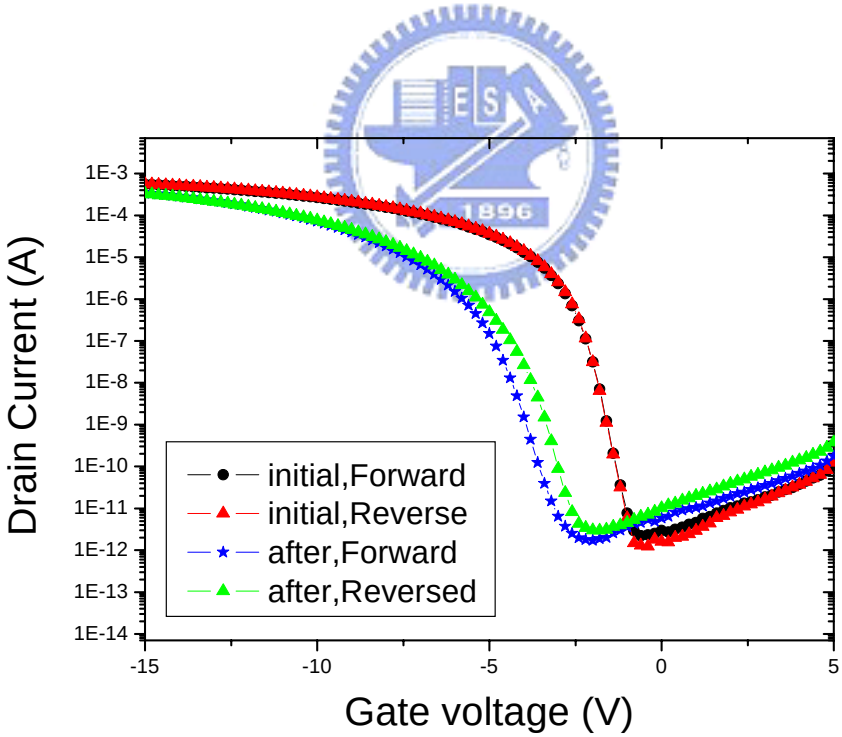


Fig.2-17 The I-V transfer curves of the p-type poly-Si TFTs after self heating stress with the time duration of 1000s

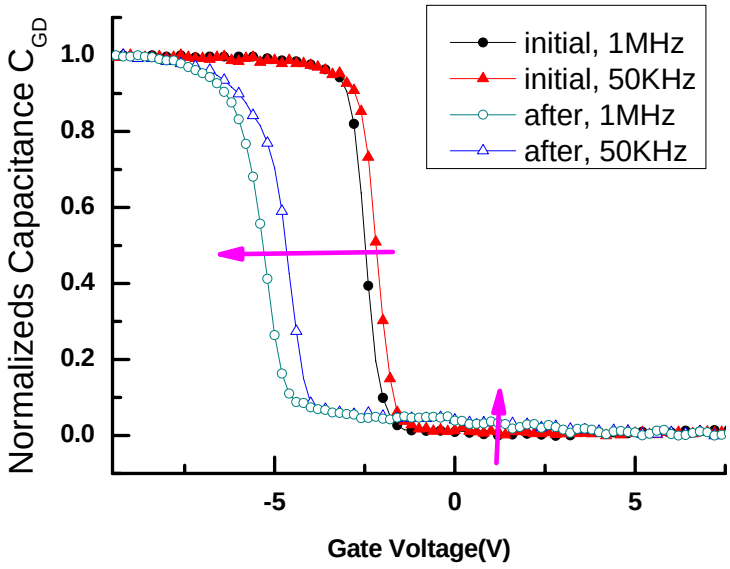


Fig. 2-18 (a) The gate-to-drain capacitance C_{GD} curves of p-type crosstie TFT before and after self-heating stress with different frequencies

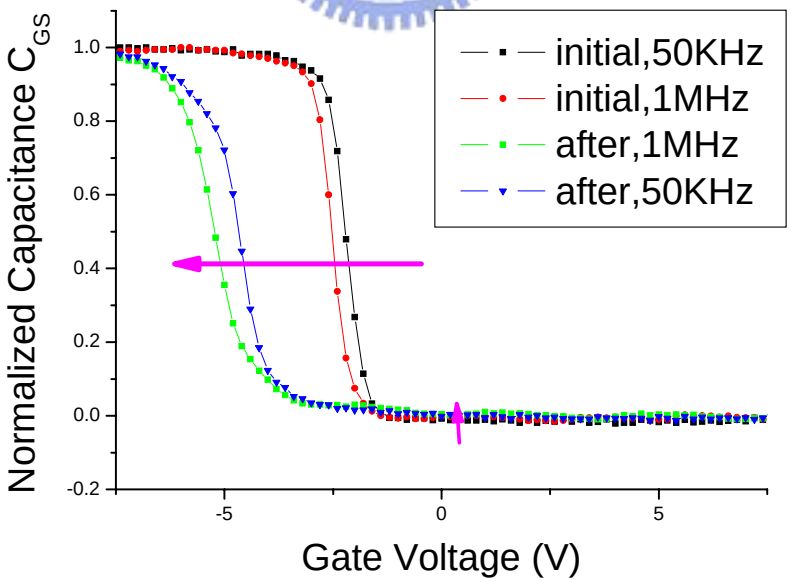


Fig. 2-18 (b) The gate-to-source capacitance C_{GS} curves of p-type crosstie TFT before and after self-heating stress with different frequencies

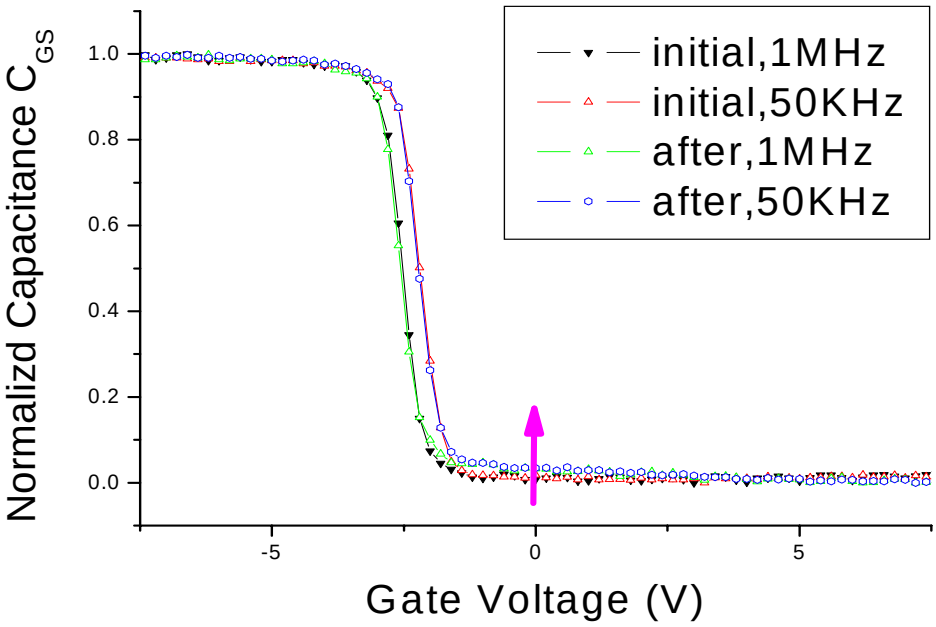


Fig. 2-19(a) The gate-to-source capacitance C_{GD} curves of p-type crosstie TFT before and after stress (V_G = -18V and V_D = V_S = 0V)with different frequencies

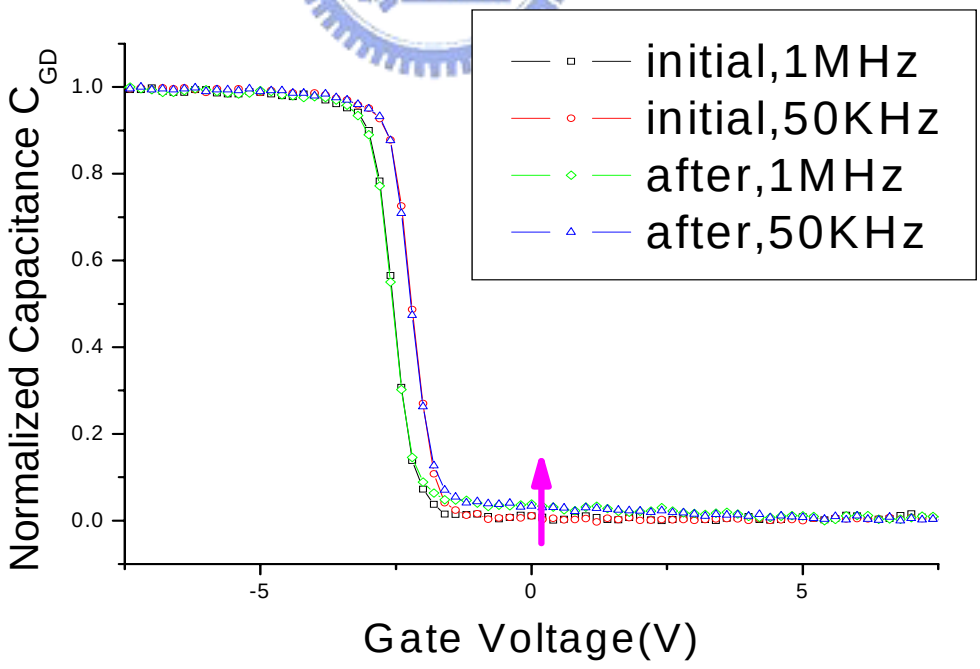


Fig. 2-19(b) The gate-to-drain capacitance C_{GD} curves of p-type crosstie TFT before and after stress (V_G = -18V and V_D = V_S = 0V)with different frequencies

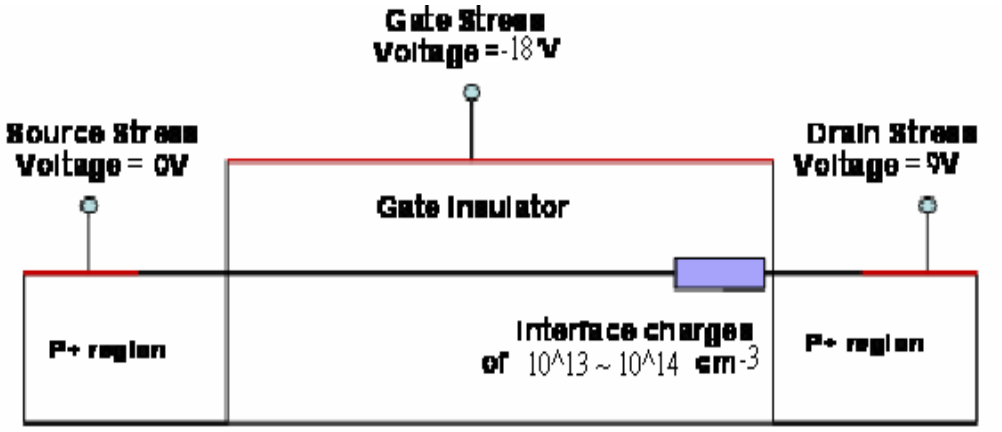


Fig. 2-20 The model of the cross section of the device after stress

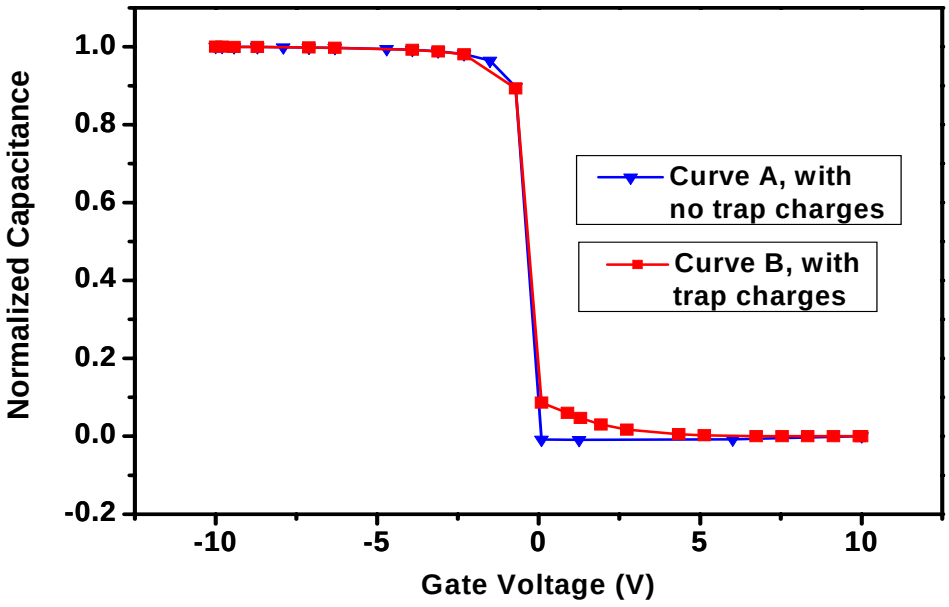


Fig. 2-21 The simulation result of C-V curve before and after stress

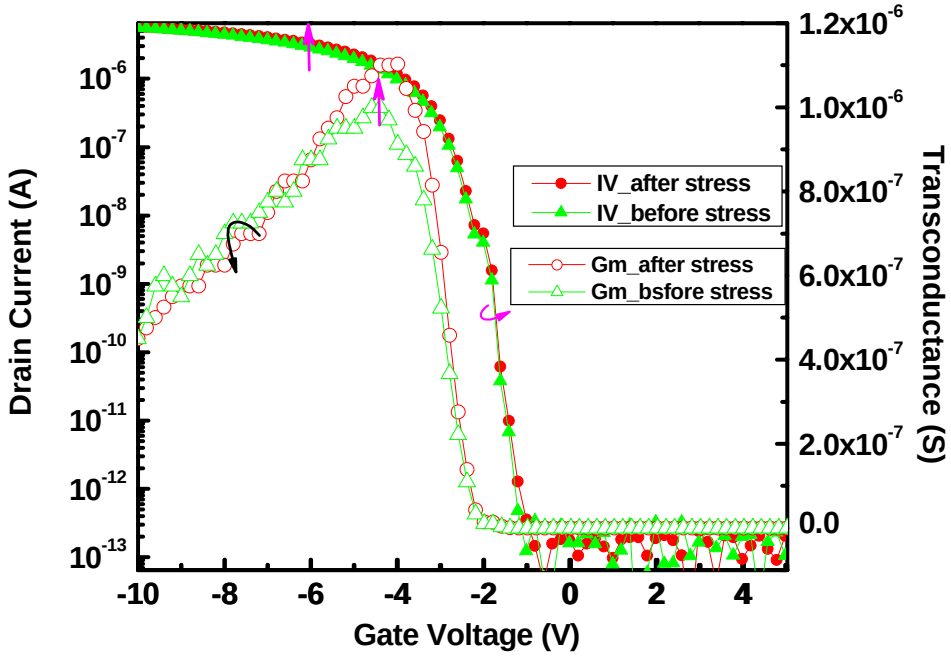


Fig. 2-22 The degradation of I-V transfer characteristic of p-type TFT after hot carrier stressing (V_{GS} = -2V~threshold voltage and V_{GD}= -20V) 1000sec

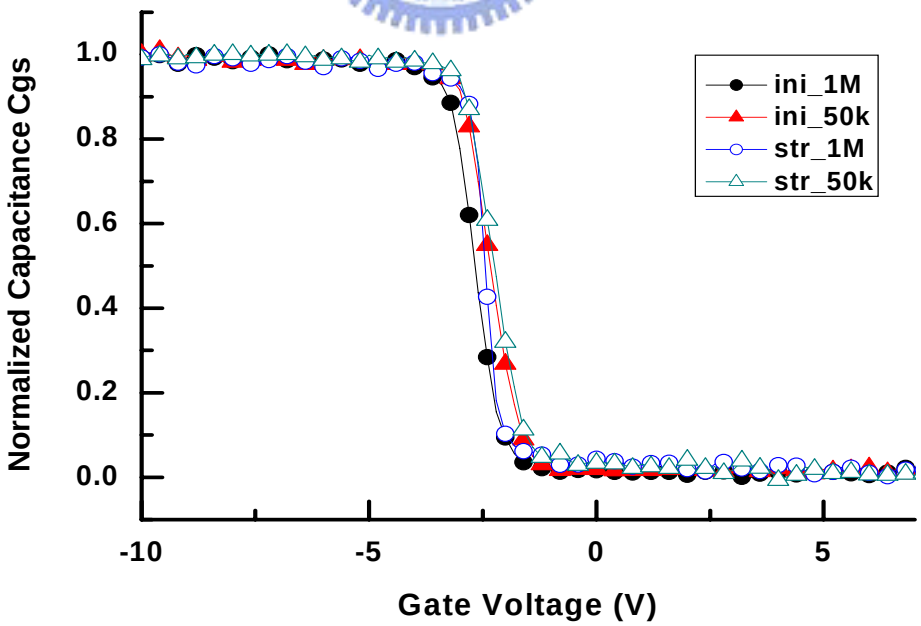


Fig. 2-23(a) The gate-to-source capacitance C_{GS} curves of p-type crosstie TFT before and after stress (V_G = -2V and V_D = -20V)with different frequencies

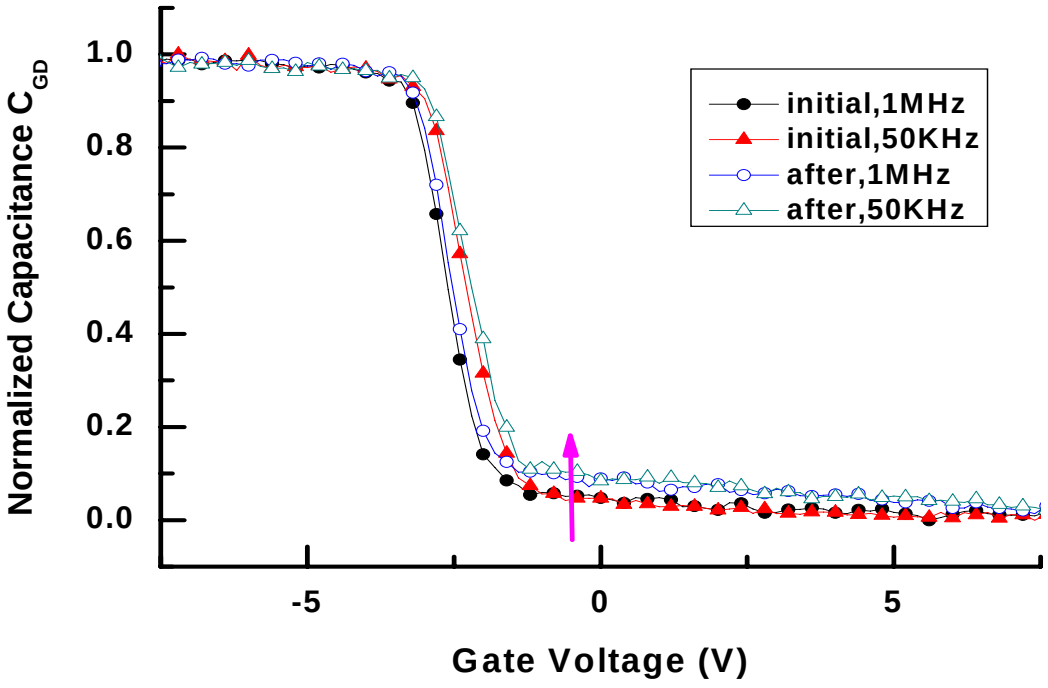


Fig. 2-23(b) The gate-to-drain capacitance C_{GD} curves of p-type crosstie TFT before and after stress (V_G = -2V and V_D = -20V)with different frequencies

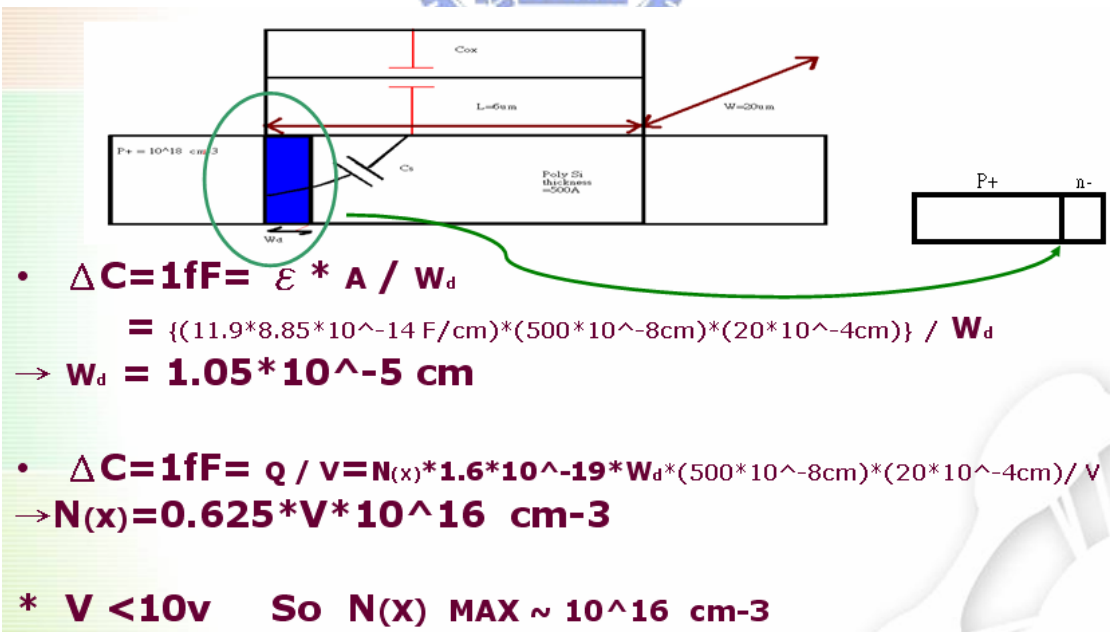


Fig. 2-24 The roughly calculation of the degradation length in channel

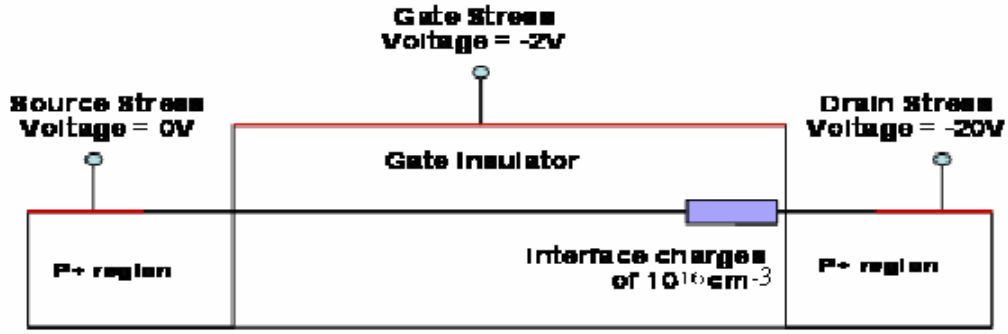


Fig. 2-25 The model of the cross section of the device after stress (V_G = -2V and V_D = -20V) 1000sec

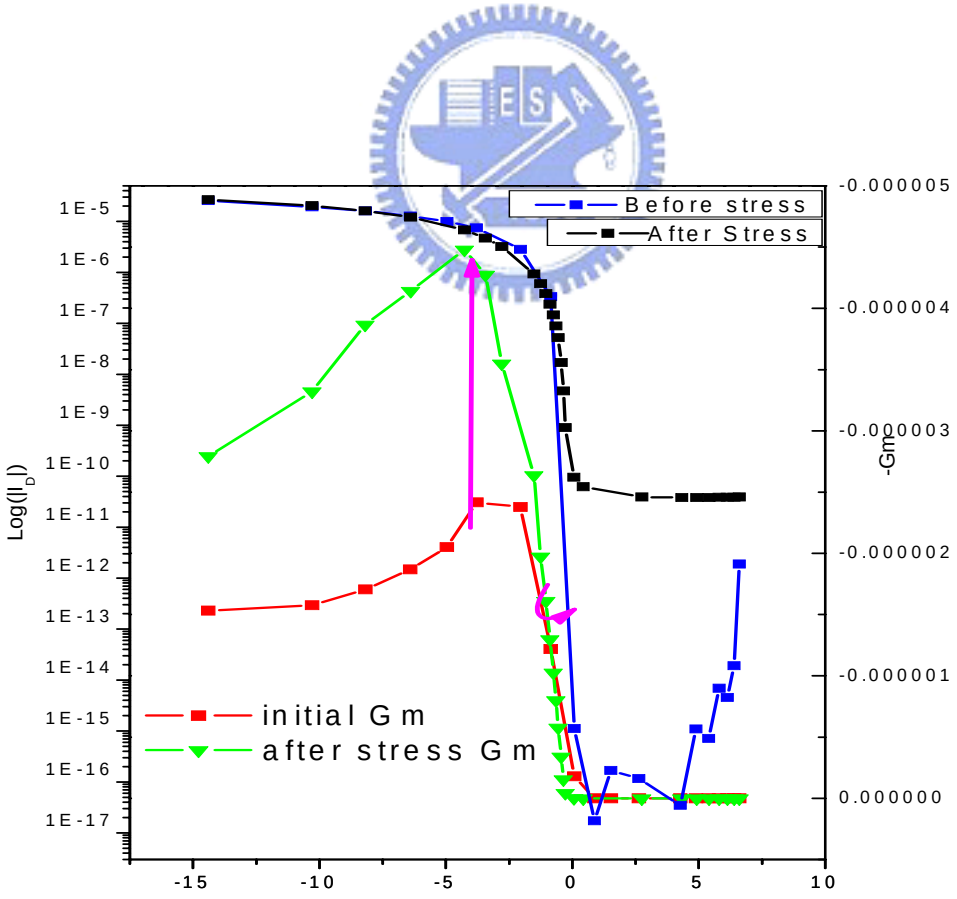


Fig. 2-26 The simulation result of p-type TFT's I_d-V_g before and after hot carrier stress

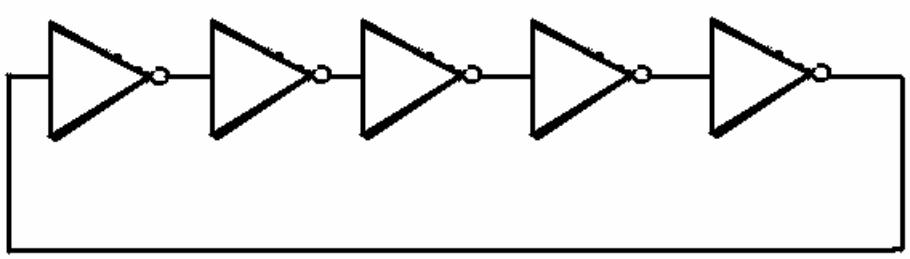


Fig. 3-1 A ring oscillator realized using five digital inverters

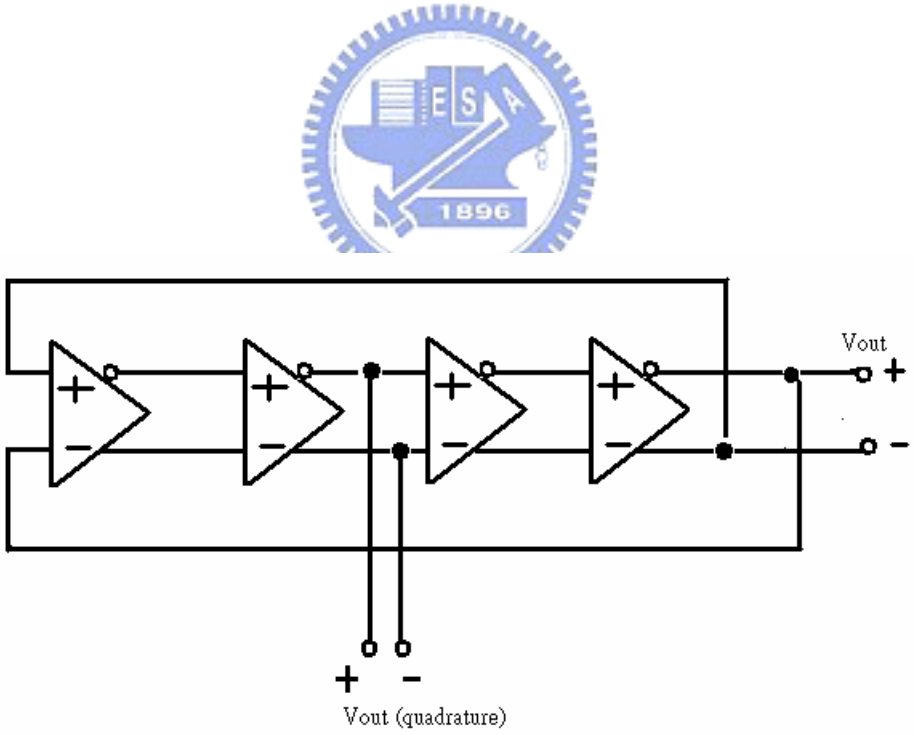


Fig. 3-2 Realizing a ring oscillator using fully differential inverters for improved power-supply rejection

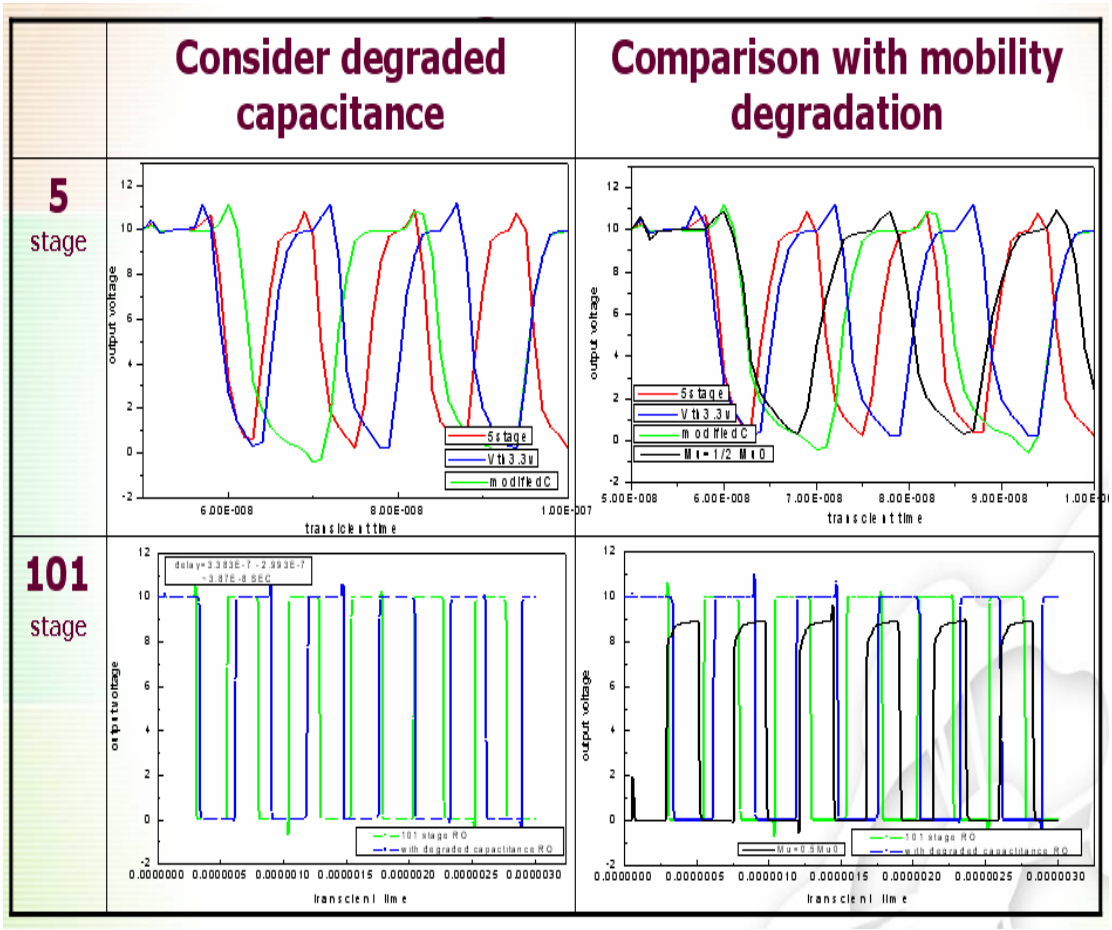


Fig. 3-3 Effect of degraded capacitance in circuit simulation