CHAPTER 3 EXPERIMENT

3.1 Electrical Degradation of N-Channel Poly-Si TFT under Dynamic Stress by Capacitance-Voltage (C-V) Measurement

First of all, the characteristic of metal-insulator-semiconductor capacitor will be mentioned below. The theory of metal-insulator-semiconductor capacitor is the fundamental of the electrical degradation of n-channel polycrystalline silicon (poly-Si) thin film transistor (TFT) under dynamic stress by capacitance-voltage (C-V) measurement. The metal-insulator-semiconductor capacitor structure is shown in Fig. 3-1, where V is the applied voltage on the metal electrode with respect to the ohmic contact. The energy-band diagram of ideal metal-insulator-semiconductor capacitor at V=0 for p-type semiconductor is shown in Fig. 3-2, where Φ_m is the metal work function, Φ_B the potential barrier between the metal and the insulator, χ_i the insulator electron affinity, χ the semiconductor electron affinity, E_g the bandgap, Ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. When the applied voltage is biased with positive or negative voltages ($V \neq 0$), the basic three cases may occur at the semiconductor surface, which are shown in the Fig. 3-3 for p-type semiconductor example. In Fig. 3-3(a), the metal plate is biased by a negative voltage ($V<0$), while the conduction band and the valence band bend upward, and the valence band near the insulator is closer to the Fermi level. This is called the "accumulation", because an accumulation of majority carriers (holes) in semiconductor near the insulator (i.e. the semiconductor surface) is attributed to the band bending. When in the "depletion", a small positive voltage is

applied to the metal electrode. Therefore, the conduction and valence bands of the semiconductor surface bend downward, and the applied voltage deplete the majority carriers (holes). This is shown in Fig. 3-3(b). In Fig. 3-3(c), a larger positive voltage is applied, and the conduction and valence bands of the semiconductor surface bend more downward leading to the intrinsic energy level E_i at the surface crossing over the Fermi level E_F. In this case, the minority carriers (electrons) concentration at the surface is larger than that that of the majority carriers (holes), thus the surface is inverted, and this is called the "inversion". [3.1]

Subsequently, the surface space-charge region and the capacitance-voltage characteristics of the metal-insulator-semiconductor structure are stated as following. The regions of surface potential in Fig. 3-3(c) can be discriminated:

$\Psi_S < 0$: accumulation of majority carriers (holes) and the bands bend upward

$\Psi_S = 0$: flat-band condition

$\Psi_B > \Psi_S > 0$: depletion of majority carriers (holes) and the bands bend downward

$\Psi_S = \Psi_B$: midgap with intrinsic concentration ($n_s=p_s=n_i$)

$\Psi_S > \Psi_B$: inversion of minority carriers (electron concentration larger than hole concentration) and the bands bend more downward

The differential capacitance of the semiconductor depletion layer can be obtain by

$$C_D \equiv \frac{\partial Q_s}{\partial \Psi_s} = \frac{\varepsilon_s}{\sqrt{2}L_D} \frac{[1-e^{-\beta\Psi_s} + (n_{po}/p_{po})(e^{\beta\Psi_s}-1)]}{F(\beta\Psi_s, n_{po}/p_{po})} \tag{3.1}$$

where

Q_s the space charge per unit area, Ψ_S the surface potential, L_D is the extrinsic Debye length for holes. The abbreviations of L_D and F are defined as:

$$L_D \equiv \sqrt{\frac{kT\varepsilon_s}{p_{po}q^2}} \equiv \sqrt{\frac{\varepsilon_s}{p_{po}q\beta}} \tag{3.2}$$

and

$$F(\beta\Psi, \frac{n_{po}}{p_{po}}) \equiv [(e^{-\beta\Psi} + \beta\Psi - 1) + \frac{n_{po}}{p_{po}}(e^{-\beta\Psi} - \beta\Psi - 1)]^{1/2} \geq 0 \tag{3.3}$$

Therefore, the total capacitance per unit area (C) of the ideal metal-insulator-semiconductor is equal to the sum of the series combination of the semiconductor depletion layer capacitance per unit area (C_D) and the insulator capacitance per unit area (C_i).

$$C = \frac{C_i C_D}{C_i + C_D} \tag{3.4}$$

Of all the metal-insulator-semiconductor structure, the metal-SiO_2-Si is the most common structure in not only metal-oxide-semiconductor field effect transistor but also polycrystalline silicon thin film transistor. For this reason, it is important to understand the nature of the SiO_2-Si interface. There are four basic kinds of traps and charges in the SiO_2 layer or at the interface [3.2]: (1) fixed oxide charges Q_f, which are positive charges, are due to structural defects in oxide layer near SiO_2-Si interface, and are immobile under an applied electric field; (2) mobile ionic charges Q_m, which are mobile and come to ionic impurities such as sodium ions, lithium ions, and kalium ions; (3) oxide trapped charges Q_{ot}, which originate in charges trapped in the oxide; (4) interface trapped charges Q_{it}, which are also called surface states, fast states, interface states, etc.. Interface trapped charges are located at the SiO_2-Si interface with energy states in the silicon-forbidden bandgap, and can be charged or discharged. Thus, they have different effects on capacitance-voltage curve.

The capacitance-voltage curve may shift along the voltage axis to negative direction due to positive fixed oxide charge and to positive direction due to negative fixed oxide charge for p-type semiconductor. It is similar for n-type semiconductor, but the polarity may change. Moreover, the fixed

oxide charge may be unaffected by alternative current signal while employing capacitance-voltage measurement. In other words, the fixed oxide charge may be independent of measurement frequency [3.3]. Nevertheless the interface-trapped charge (also called the interface state, fast state, or surface state) can exchange charges with silicon in a period of time and with the energy level in the silicon-forbidden bandgap. The capacitance-voltage curve may stretch-out due to interface-trapped charges. That is to say, the curve may be dependent of measurement frequency through interface-trapped charge (or interface state, etc.). An interface trap is regarded as "donor-like" if it is neutral or positive by offering an electron. An interface trap is considered as "acceptor-like" if it can become neutral or negative by accepting an electron. Thus, the total capacitance including insulator, depletion, and interface trap capacitance can be expressed as following:

$C = C_i + C_p$ and $C_p = C_D // (C_s + R_s)$.

The parallel branch can be converted into a frequency-dependent capacitance (C_p) and a frequency-dependent conductance (G_p) in parallel, where:

$$C_p = C_D + \frac{C_s}{1+\omega^2\tau^2} \quad (3.5)$$

and

$$\frac{G_p}{\omega} = \frac{C_s\omega\tau}{1+\omega^2\tau^2}. \quad (3.6)$$

Thus, the frequency-dependent capacitance explained the capacitance stretch-out. In addition, the capacitance theory of polycrystalline silicon thin film transistor is similar to that of the metal-insulator-semiconductor structure. The capacitance-voltage curve degradation of n-channel polycrystalline silicon thin film transistor is analogy and comes from grain boundary, interface state, and so on. [3.3] But in our experience, the gate to drain and the gate to source capacitance can be expressed as:

$C = C_i // C_{GD}$ and $C = C_i // C_{GS}$, where C_{GD} is the gate to drain capacitance, C_{GS} is the gate to source capacitance.

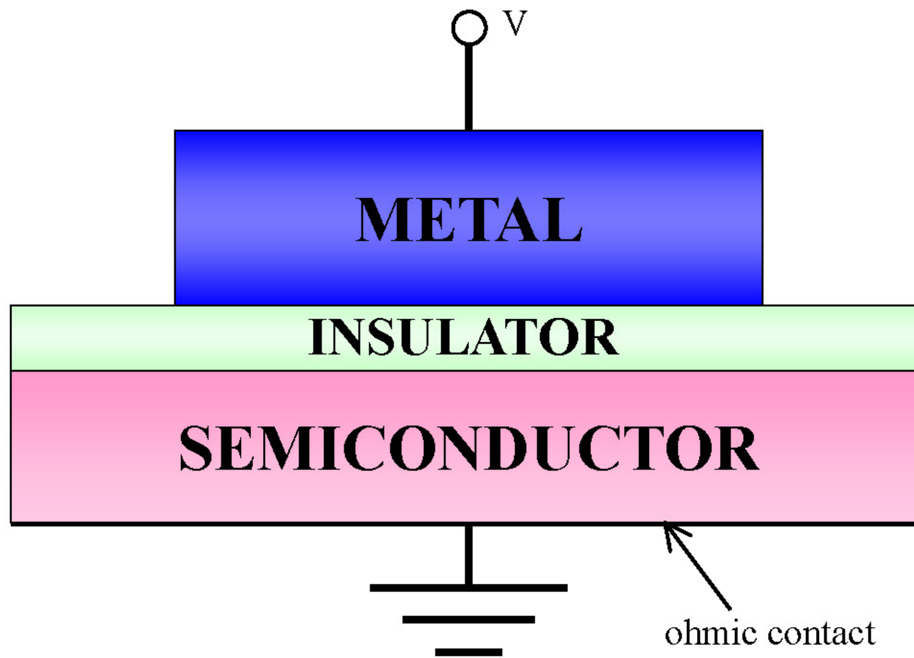

Fig. 3-1 metal-insulator-semiconductor capacitor

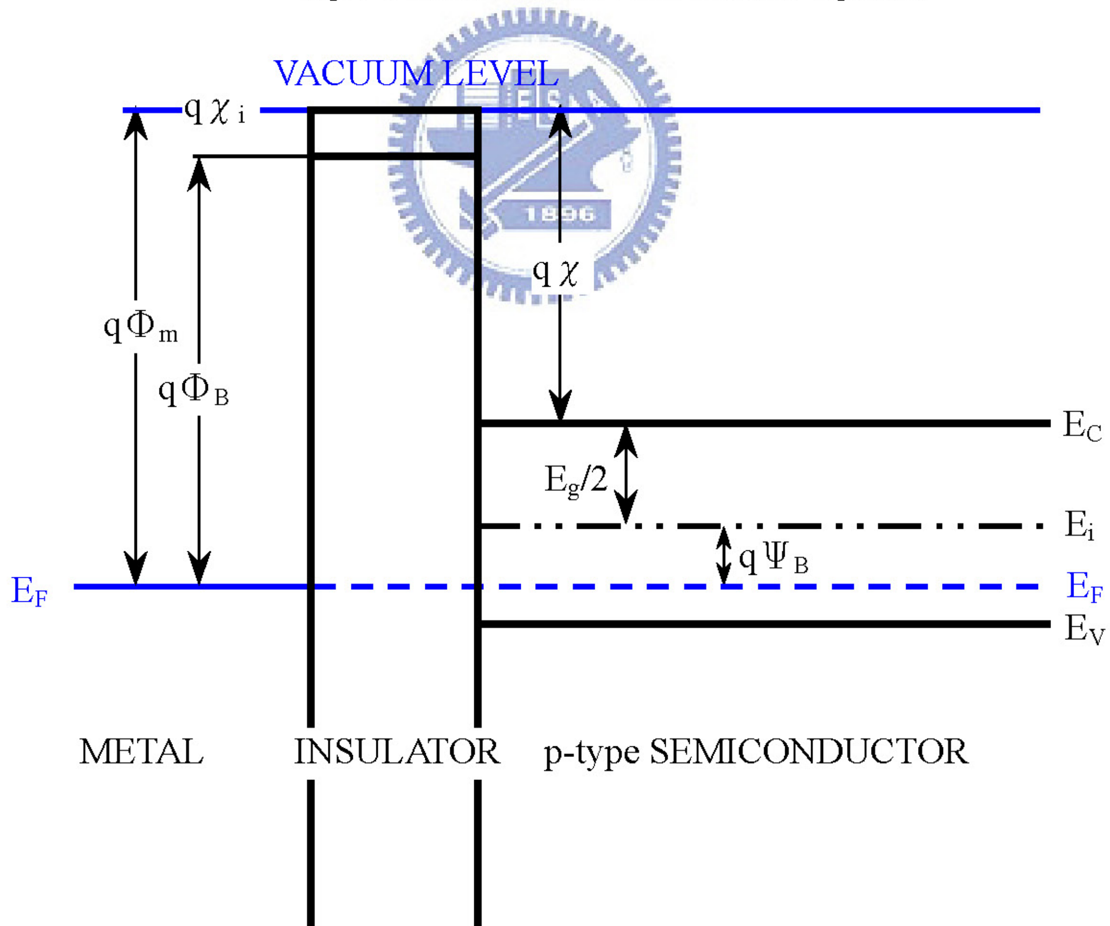

Fig. 3-2 energy-band diagram of ideal metal-insulator-semiconductor capacitor at V=0 for p-type semiconductor

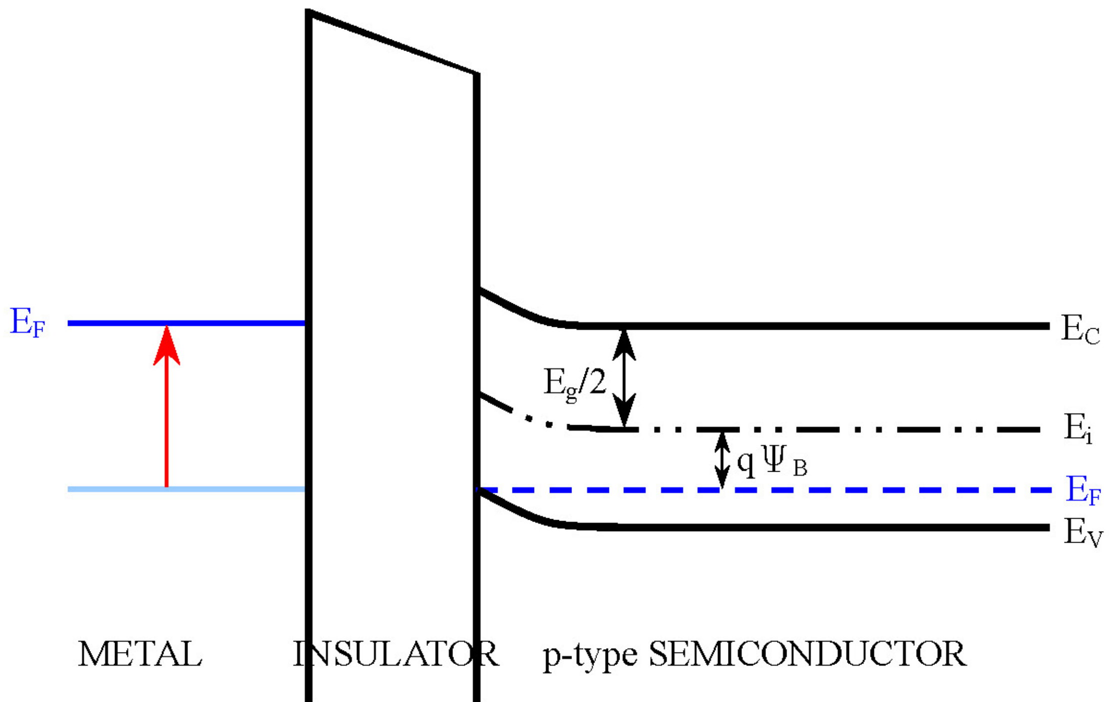

Fig. 3-3(a) energy-band diagram of ideal metal-insulator-semiconductor (p-type semiconductor) capacitor when V≠0 (V<0)) for accumulation

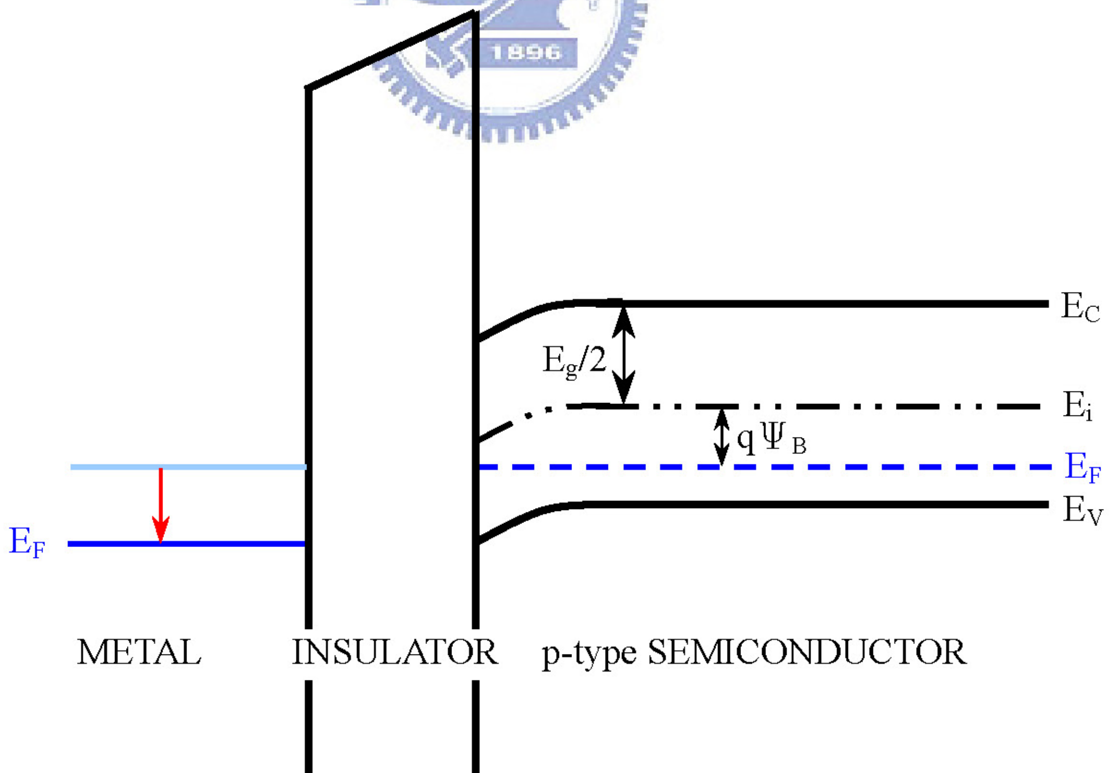

Fig. 3-3(b) energy-band diagram of ideal metal-insulator-semiconductor (p-type semiconductor) capacitor when V≠0 (V>0) for depletion

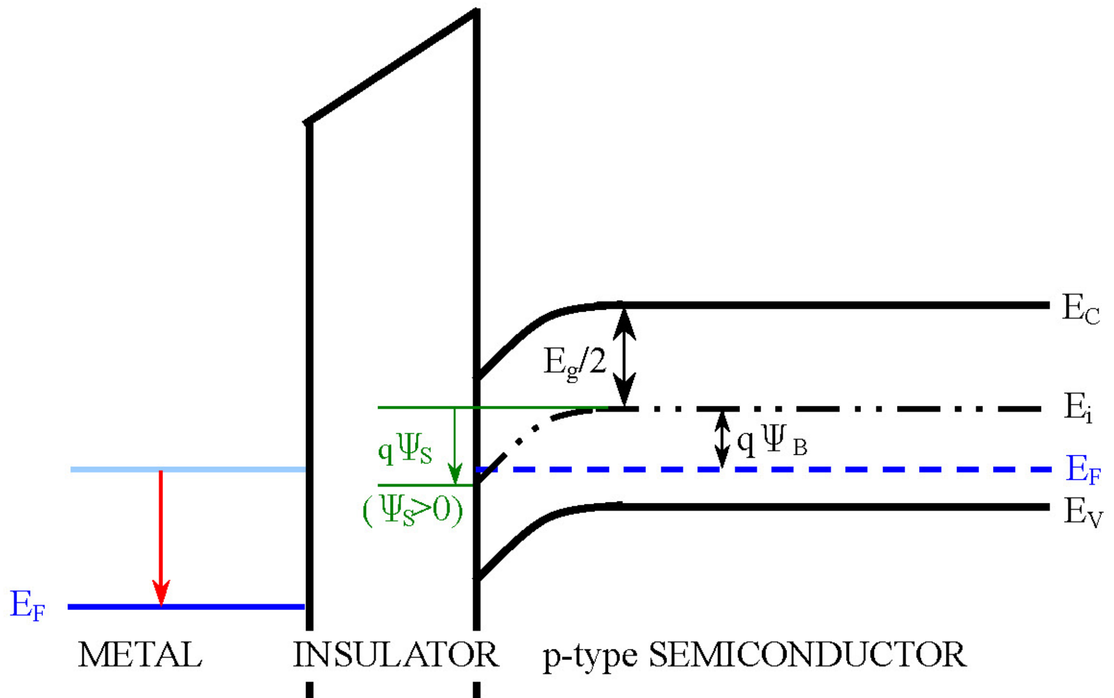

Fig. 3-3(c) energy-band diagram of ideal metal-insulator-semiconductor (p-type semiconductor) capacitor when $V \neq 0$ ($V > 0$) for inversion