3.2 Electrical Degradation of N-Channel Poly-Si TFT With and Without Grain Boundary in Channel under Dynamic Stress by Current-Voltage (I-V) Measurement

The drain current formula of polycrystalline silicon thin film transistor is similar to metal-oxide-semiconductor field effect transistor, but not the same. In metal-oxide-semiconductor field effect transistor, the drain current can be expressed as:

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \qquad (3.7)$$

where

W is the channel width,

L is the channel length,

μ_n is electron mobility,

C_{OX} is the gate oxide capacitance per unit area,

V_T is the threshold voltage.

In long channel polycrystalline silicon thin film transistor, the drain current above threshold region developed by Jacunski et al. [3.4] is given by:

$$I_a = \frac{W}{L}\mu_{FET} C_{ox}[(V_{GS} - V_T)V_{des} - \frac{1}{2\alpha_{sat}}V_{dse}^2] \qquad (3.8)$$

W is the gate width,

L is the gate length,

μ_{FET} is the field-effect mobility,

C_{OX} is the gate oxide capacitance per unit area,

V_T is the extrinsic gate-source threshold voltage,

α_{sat} is the body constant,

V_{dse} is the effective extrinsic drain-source voltage.

In addition, the field-effect mobility μ_{FET} is gate voltage dependent and

includes the effects of the trap states. V_{dse} is given by the function that combines V_{ds} in the linear region and V_{sat} in saturation region:

$$V_{dse} = \frac{V_{ds}}{(1+(V_{ds}/V_{sat})^{m_{ss}})^{1/m_{ss}}} \tag{3.9}$$

where m_{ss} is the parameter controlling the transition at saturation.

Below threshold, the drain current is given by:

$$I_a = \frac{W}{L}\mu_s C_{ox}(\eta V_{th})^2 \exp(\frac{(V_{GS}-V_T)}{\eta V_{th}})[1-\exp(\frac{-V_{ds}}{\eta V_{th}})] \tag{3.10}$$

where

μ_s is the subthreshold mobility,

η is the subthreshold ideality factor,

$V_{th}=k_B T/q$ is the thermal voltage.

The drain current (I_D) developed by a unified model combined the above-threshold and the subthreshold currents as follows:

$$\frac{1}{I_D} = \frac{1}{I_{sub}} + \frac{1}{I_a} \tag{3.11}$$

Although the drain current in polycrystalline silicon thin film transistor has a similar formulation as in metal-oxide-semiconductor field effect transistor, the conduction mechanism in polycrystalline silicon thin film transistor is more complex than in crystalline transistor, metal-oxide-semiconductor field effect transistor. The main conduction mechanisms in metal-oxide-semiconductor field effect transistor are drift and diffusion in the above-threshold regime and in the subthreshold regime, respectively. However, the existence of grain boundaries in the polycrystalline silicon film causes that the carriers have to overcome the grain boundary barrier by thermionic emission and thermionic field in order to become conduction-current from source to drain or drain to source. Therfore, the effect of grain boundary has to be considered in both subthreshold and above-threshold. [3.5]

The mechanisms of electrical degradation under dynamic stress are different between metal-oxide-semiconductor field effect transistor and polycrystalline silicon thin film transistor. The degradation mechanisms in metal-oxide-semiconductor are carrier injection, chare trapping [3.6], and interface state creation [3.7]. However, enhanced device degradations of polycrystalline silicon thin film transistors under exposure to dynamic stress are mainly attributed to impact ionization effect [3.8], hot carriers [3.9] [3.10], and grain boundary effect [3.11]. Furthermore, the electric parameters g_m is degraded due to tail state in the interface and grain boundaries, and V_T is affected by deep state. Similarly, the subthreshold swing depends on the deep state, and the current crowding phenomenon suggests the large parasitic resistance. Therefore, these key points can be itemized in the Table 3-1.

Table 3-1 electrical parameters variation correspond to possible degradation reason

electrical parameter altered after stressing	***main reason***
ΔV_T *(threshold voltage)*	■ *charges trapped in gate oxide* ■ *deep state generation (at interface and/or in grain boundary)*
ΔSS *(subthreshold swing)*	■ *interface deep state creation* ■ *intra-grain defect density of state generation*
Δg_m ($\Delta \mu$) *(transconductance/mobility)*	■ *tail state generation in grain boundary* ■ *interface state creation*