CHAPTER 4 RESULTS AND DISCUSSION

4.1 Lightly Doped Drain Effects of Low-Temperature Polycrystalline Silicon Thin Film Transistors

In the section, we use two methods, capacitance-voltage (C-V) analysis and current-voltage (I-V) analysis, to analyze the samples made by excimer laser annealing (ELA). The result of capacitance-voltage (C-V) analysis is the first part, and the second part is current-voltage (I-V) analysis. Fig. 4-1(a) and Fig. 4-1(b) show the initial gate-source (C_{GS}) and gate-drain (C_{GD}) capacitance-voltage curves. In virtue of the symmetric structure of the top-gate polycrystalline thin film transistor, the capacitance-voltage of gate-source (C_{GS}) and gate-drain (C_{GD}) are symmetric.

In addition, the capacitance-voltage curve in our experiment is different from that of metal-oxide-semiconductor capacitor. Fig. 4-2(a) and Fig. 4-2(b) are the comparison figures. Fig. 4-2(a) is a conventional p-Si metal-oxide-semiconductor capacitor capacitance-voltage curve, and Fig. 4-2(b) is a typical polycrystalline silicon thin film transistor gate-drain capacitance-voltage (C_{GD}) curve in our experiment. For p-type substrate silicon and negative gate bias, the capacitances are maximum and minimum for a metal-oxide-semiconductor capacitor and a polycrystalline silicon thin film transistor gate-drain/gate-source capacitance, respectively. Fig. 4-3(a) illustrates an equivalent total capacitance circuit of metal-oxide-semiconductor capacitor and Fig. 4-3(b) shows an equivalent total capacitance circuit of polycrystalline silicon thin film transistor. They indicate the differences between a conventional metal-oxide-semiconductor capacitor and

a polycrystalline silicon thin film transistor. The total capacitance is measured. The total capacitance in a metal-oxide-semiconductor capacitor is equal to an oxide capacitance in serial with a channel capacitance, but that in a polycrystalline silicon thin film transistor is equal to a gate-drain overlap capacitance in parallel with an oxide capacitance. Although the gate-drain/gate-source capacitance is not equal to total capacitance in our experiment, we will use gate-drain/gate-source capacitance instead of total capacitance to represent the total capacitance in this thesis. Therefore, the capacitance-voltage curve we measured is different from that of a metal-oxide-semiconductor capacitor.

In Fig. 4-1(a) and Fig. 4-1(b), the capacitance-voltage curve is degraded with increasing the measurement frequency, which is equivalent to Fig. 4-4. When measuring the capacitance-voltage characteristic, the period of applied small signal may correspond to the trap emission time. Hence, the measurement frequency can be assumed:

$$\frac{1}{f} = \tau_n(E = E_{state}) \tag{4.1}$$

where $\tau_n(E)$ is the acceptor-like trap state emission time as a function of E and τ_{no} is a time constant.[4.1]

$$\tau_n(E) = \tau_{no}\exp(\frac{E_c - E}{kT}) \tag{4.2}$$

Moreover, deep trap state, E_{deep}, is close to the middle of the band gap, and tail trap state, E_{tail}, is close to the conduction band. If the measurement frequencies were equal to 10 KHz and 1 MHz, it would correspond to the emission time of deep state and tail state, respectively [4.2]. Fig. 4-5(a) shows that while the measurement frequency is lower (ex. 10 KHz), the deeper state may have larger probability to detrap corresponding to larger τ. On the contrary, Fig. 4-5(b) indicates when the frequency is higher; the tail state corresponds to smaller τ. As a result of the detrapping time of the

traps at deep state may be longer, the high frequency (ex. 1 MHz) capacitance-voltage curve may stretch more. The low frequency (ex. 10 KHz) one may not stretch severe.

Fig. 4-6(a), Fig.4-6(b) and Fig. 4-6(c) are the gate-drain capacitance-voltage curves of n-channel excimer laser annealing polycrystalline thin film transistor without lightly doped drain, which are measured at 10 KHz, 100 KHz, and 1 MHz versus stress time, respectively. Similarly, Fig. 4-7(a), Fig. 4-7(b), Fig. 4-7(c) are the gate-source capacitance-voltage characteristic measured at 10 KHz, 100 KHz, and 1 MHz, respectively. The gate-drain capacitance-voltage characteristics are similar to the gate-source ones owing to the symmetric structure. Comparison with applied lower frequency (ex. 10 KHz) and higher frequency (ex. 1 MHz), with increasing stress time the curves of lower frequency are less stretched; on the contrary, the curves at higher frequency are degraded more with increasing stress time. The phenomenon can be investigated between Fig. 4-6(a) to Fig. 4-6(c), and Fig. 4-7(a) to Fig. 4-7(c). Traps at states below deep state E_{deep} should not have enough time to respond to the applied small signal at 10 KHz, but the emission time of traps at states near conduction band may be shorter. If the amount of traps at states below deep state generated with increasing stress time, it should lead to more serious RC delay effect to stretch out at the 10 KHz capacitance-voltage characteristics. Therefore, the unchanged capacitance-voltage characteristics at 10 KHz shown in Fig. 4-6(a) and Fig. 4-7(a) imply that the number of deep states may be not markedly increased after dynamic stress. We suppose that the severe degradation of capacitance-voltage characteristics at 1 MHz is attributed to an increase of the amount of traps at tail state near conduction band as stress time increased. Besides, it is supposed that the main reason responsible for the electrical degradation of n-channel polycrystalline silicon thin film transistor after dynamic stress is

the tail states produced by the strained bounding in polycrystalline silicon film.

Above-mentioned devices are excimer laser annealing polycrystalline silicon thin film transistors without lightly doped drain, but devices we will discuss about as following are with 1.5 μm lightly doped drain in order to investigate the lightly doped drain effect under dynamic stress.

Fig. 4-8(a) and Fig. 4-8(b) are the initial gate-source and gate-drain capacitance-voltage curves of an n-channel excimer laser annealing thin film transistor with lightly doped drain at different measurement frequencies, respectively. The gate-source and gate-drain capacitance-voltage characteristics are identical because of symmetric structure of these polycrystalline silicon thin film transistors with lightly doped drain. Besides, the characteristic are degraded symmetrically even after 1000s stress as shown in Fig. 4-9(a) and Fig. 4-9(b). With increasing stress time, the capacitance-voltage characteristics are not stretched out significantly from 10 KHz to 1 MHz measurement frequency. Fig. 4-10(a), Fig. 4-10(b), and Fig. 4-10(c) show the gate-drain capacitance-voltage curves with increasing stress time at 10 KHz, 100 KHz, and 1 MHz, respectively. Fig. 4-11(a), Fig. 4-11(b), and Fig. 4-11(c) show the similar results of gate-source capacitance-voltage characteristics. The polycrystalline silicon thin film transistors with lightly doped drain are less degraded under dynamic stress in virtue of the capacitance-voltage cures not stretched out seriously and different measurement frequencies corresponding to different depth trap states. Consequently, the polycrystalline silicon thin film transistors with lightly doped drain may not generate as much tail state as that without lightly doped drain. We infer that the lightly doped region reduces the high electrical field at source/drain junction under dynamic stress and the region can suppress the dynamic stress at source/drain junction. Thus, the degradation