in devices with lightly doped drain is less than that without lightly doped drain.

The second part is current-voltage analysis of low-temperature polycrystalline silicon thin film transistors under dynamic stress. After stress, Fig. 4-12 shows the $I_{DS}$–$V_{GS}$ characteristic of an n-channel excimer laser annealing thin film transistor without lightly doped drain at $V_{DS}$=0.1V. The drain current is obviously degraded on larger gate bias, namely on-region. Moreover, the subthreshold swing seems to be unchanged. We calculated the degraded on-current ratio versus stress time of an n-channel excimer laser annealing thin film transistor without lightly doped drain at $V_{DS}$=0.1V, which is shown in Fig. 4-13. With increasing stress time, the on-current degraded serious and notably the on-current of polycrystalline silicon thin film transistor after 1000s stress degraded to 4.76% of initial value. Furthermore, the field-effect-mobility of polycrystalline silicon thin film transistor also suffered from severe degradation under dynamic stress, as Fig. 4-14 illustrated. The field-effect-mobility is reduced to 7.73% of non-stressed one. The results may imply that the on-current degradation is due to tail state creation.

Another important parameter is subthreshold swing. The subthreshold swings of polycrystalline silicon thin film transistors without and with lightly doped drain after dynamic stress are listed in Table 4-1. In Table 4-1 and Fig. 4-12, it is clear that the subthreshold swing of thin film transistor without lightly doped drain does not alter much. The result may be attributed to the amount of traps at deep state does not increase with dynamic stress time. Consequently, the generated trap near tail state is responsible for the degradation of polycrystalline silicon thin film transistor under dynamic stress. Besides, Fig. 4-15 also gives the evidence of trap state creation with increasing stress time.

Comparison to polycrystalline silicon thin film transistors with lightly doped drain region, Fig. 4-16 shows the $I_{DS}$-$V_{GS}$ curves of an n-channel excimer laser annealing thin film transistor with 1.5 μm lightly doped drain at $V_{DS}$=0.1V. The degradation of on-current of thin film transistor with lightly doped drain is less than that without lightly doped drain, which is shown as Fig. 4-13 and Fig. 4-17. The degraded on-current ratio of thin film with lightly doped drain is 61.05% after 1000s stress more slight than 4.76% of ones without lightly doped drain after 1000s stress. With increasing the stress time, the degraded on-current ratio decreases. The degradation of degraded mobility ratio of thin film transistor with lightly doped drain is also less than that without lightly doped drain, which is shown in Fig. 4-14 and Fig. 4-18. What is more, the subthreshold swing is kept unchanged like the without lightly doped drain case. Table 4-1 shows the subthreshold swing of polycrystalline silicon thin film transistors with lightly doped drain after dynamic stress. The maximum variation to average subthreshold swing ($MAX(\frac{SS-\overline{SS}}{\overline{SS}})$) is about 4.4%.

In current-voltage analysis, the variation of on-current represents the change of tail state, and the deformation of subthreshold swing implies the change of deep state. As a result, the amount of trap at deep state may be almost unchanged, which is similar to the thin film transistor without lightly doped drain case. Besides, the creation of tail state in polycrystalline silicon thin film transistor with lightly doped drain under dynamic stress is slighter than that without lightly doped drain.

The extracted trap density of state is illustrated in Fig. 4-19. Consequently, the trap density of state is increased with stress time. Uraoka et al. [4.3] proposed a degradation model of dynamic stress illustrated as Fig.4-20. When we apply a high gate voltage, the electrons gather to form

the conduction channel. Once the gate voltage entering the transition period from high to low, the electrons in the channel are swept out to the source and drain rapidly. Therefore, the high electric field leads to some of trapped electrons gain energy and become hot electrons. Finally, the hot electrons damage the regions and generate traps near source/drain junction. Fig. 4-21 shows the $I_{DS}$–$V_{DS}$ curves of an n-channel excimer laser annealing thin film transistor without lightly doped drain at $V_{GS}$=10V.

The current crowding phenomenon is significantly with increasing stress time. Fig. 4-22 is the extracted parasitic resistance versus time curve of thin film transistor without lightly doped drain. The parasitic resistance is increased with stress time increased, which means the main damage regions are located near source/drain junction and grain boundaries. On the contrary, the current crowding effect of low temperature polycrystalline silicon thin film transistor with 1.5 μm lightly doped drain is not as remarkable as that without lightly doped drain, as illustrated in Fig. 4-23. Also, the extracted parasitic resistance in Fig. 4-24 is not as conspicuous as one without lightly doped drain. The lightly doped drain region reduces the high electric field and suppresses the trap generation near source/drain junction.