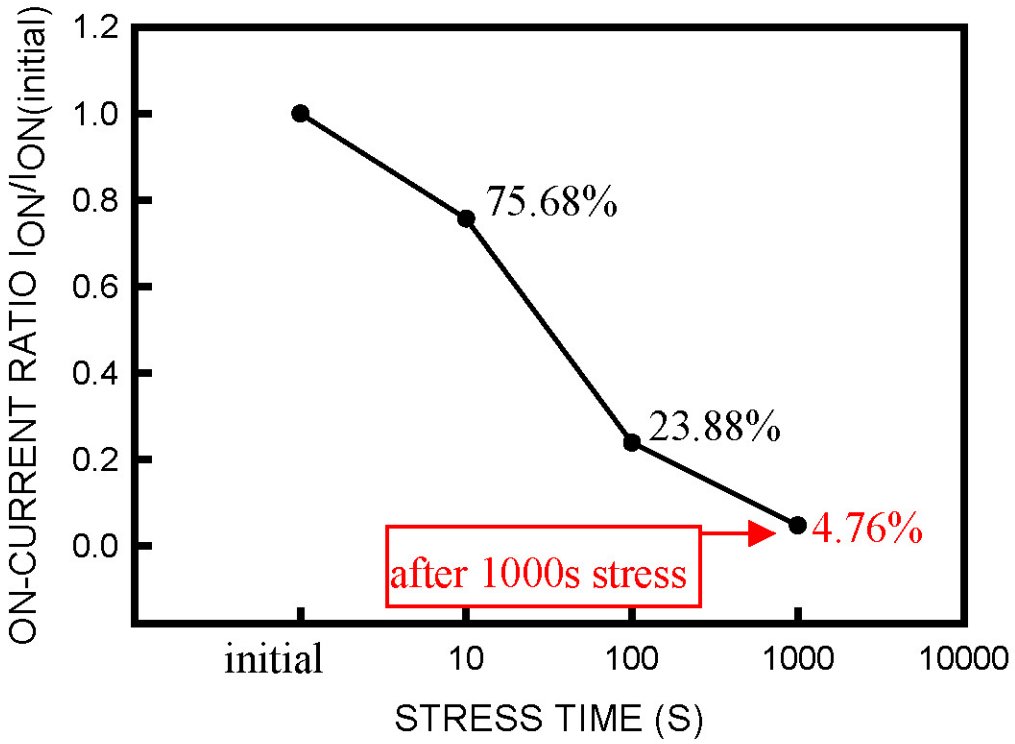

Fig. 4-13 the degraded on-current ratio versus stress time curve of an n-channel ELA TFT without LDD at V_{DS}=0.1V

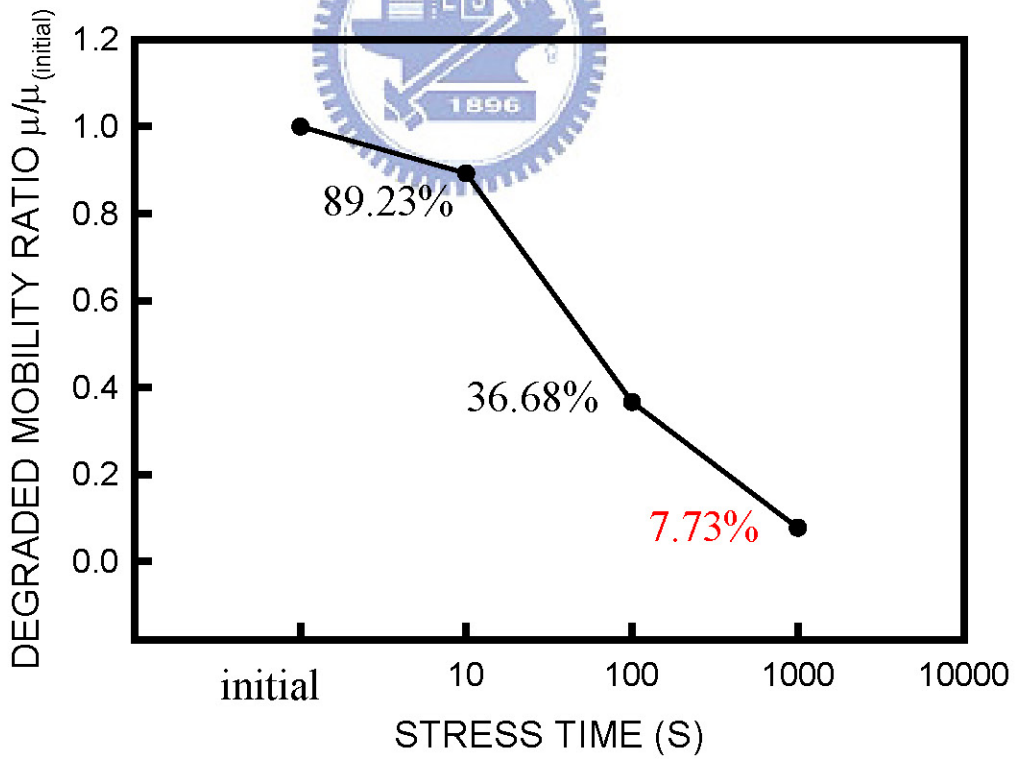

Fig. 4-14 the degraded mobility ratio versus stress time curve of an n-channel ELA TFT without LDD at V_{DS}=0.1V

	initial	*10s stress*	*100s stress*	*1000s stress*
POLY-SI TFT WITHOUT LDD	*0.611(V/dec)*	*0.578(V/dec)*	*0.585(V/dec)*	*0.662(V/dec)*
POLY-SI TFT WITH 1.5 μm LDD	*0.592(V/dec)*	*0.555(V/dec)*	*0.553(V/dec)*	*0.567(V/dec)*

Table 4-1 the subthreshold swings of poly-Si TFTs without and with LDD after dynamic stress

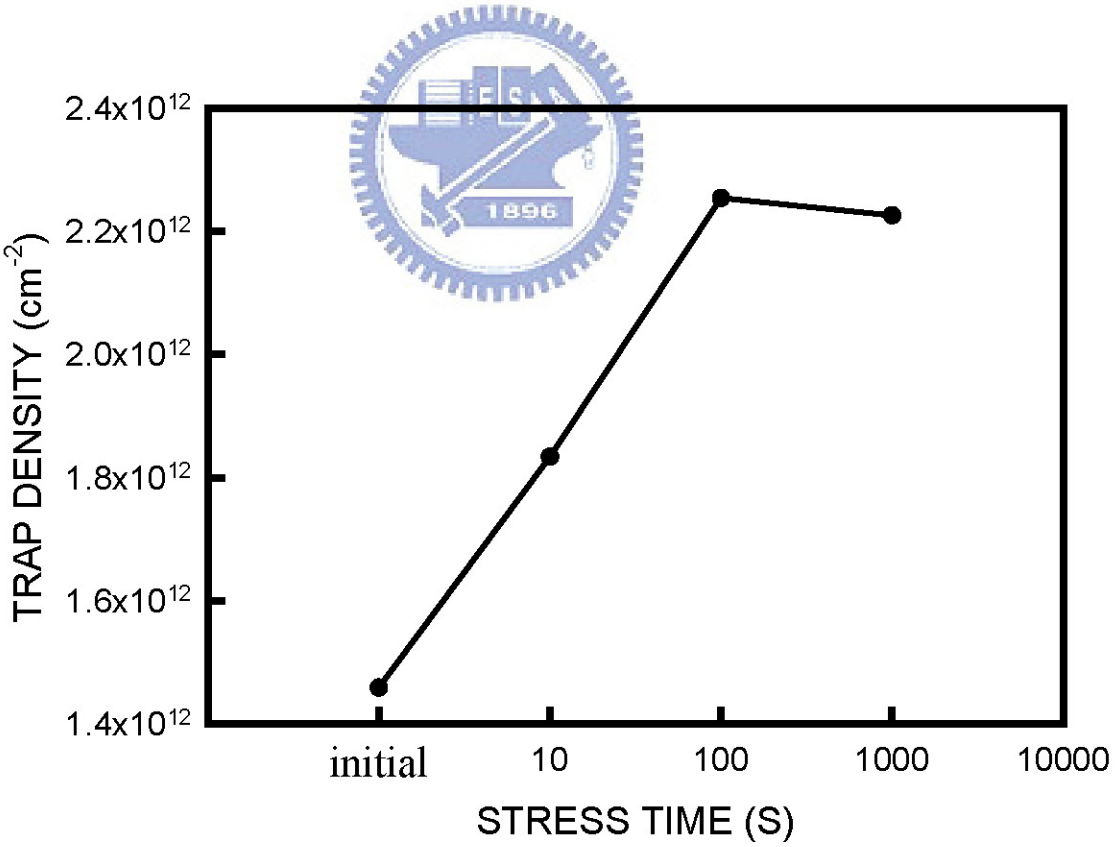

Fig. 4-15 the trap density versus stress time curve of an n-channel ELA TFT without LDD

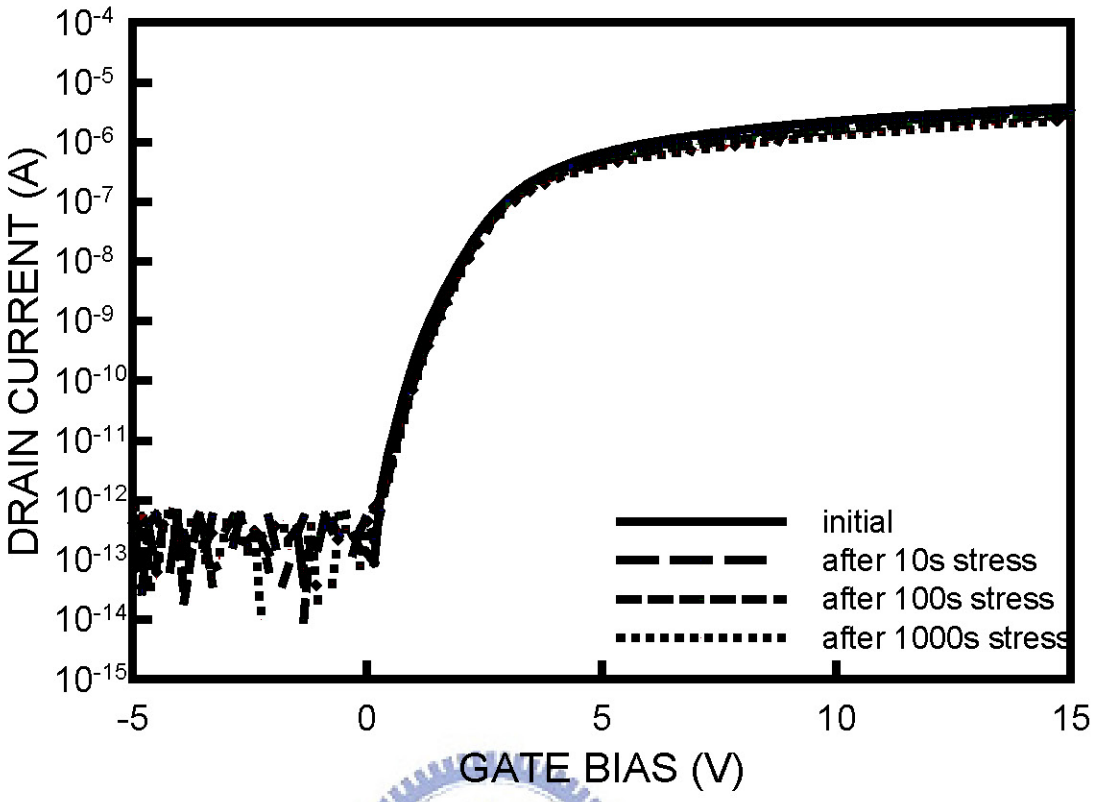

Fig. 4-16 the I_{DS}–V_{GS} curves of an n-channel ELA TFT with 1.5 μm LDD at V_{DS}=0.1V

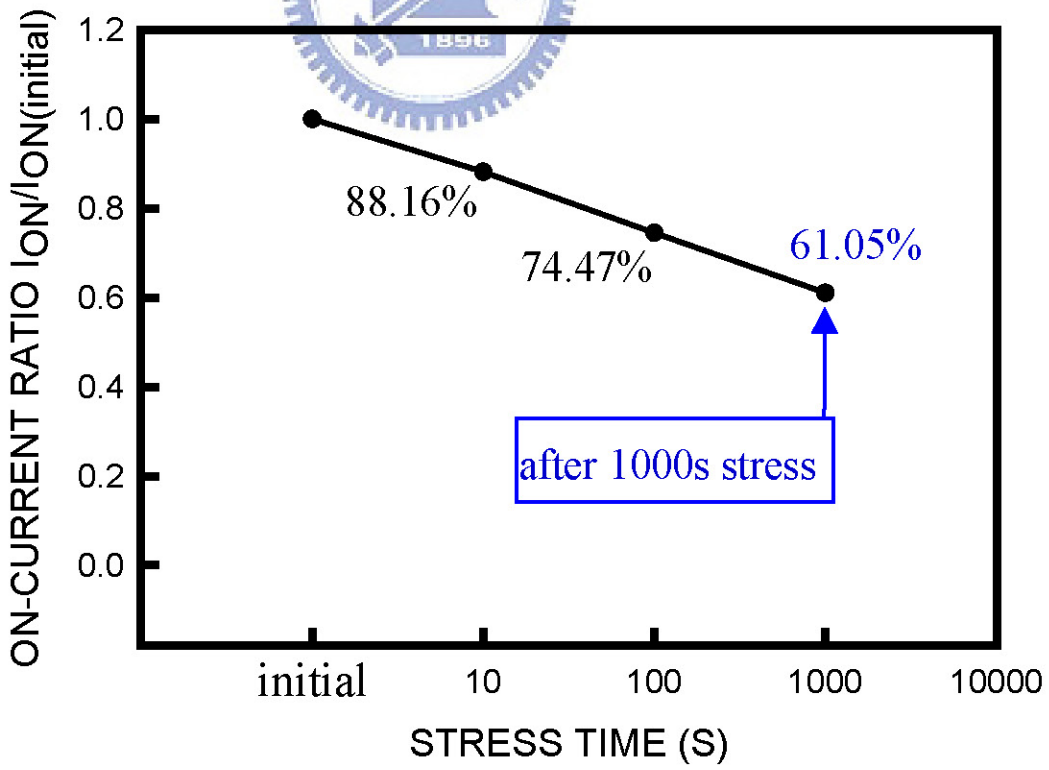

Fig. 4-17 the degraded on-current ratio versus stress time curve of an n-channel ELA TFT with 1.5 μm LDD at V_{DS}=0.1V

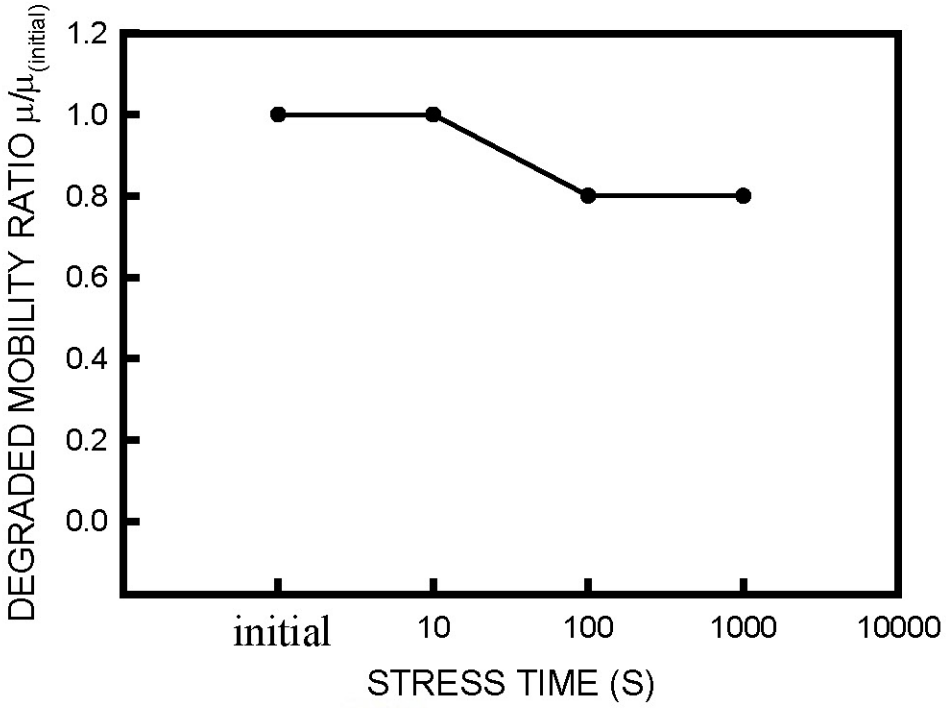

Fig. 4-18 the degraded mobility ratio versus stress time curve of an n-channel ELA TFT with 1.5 μm LDD at V_{DS}=0.1V

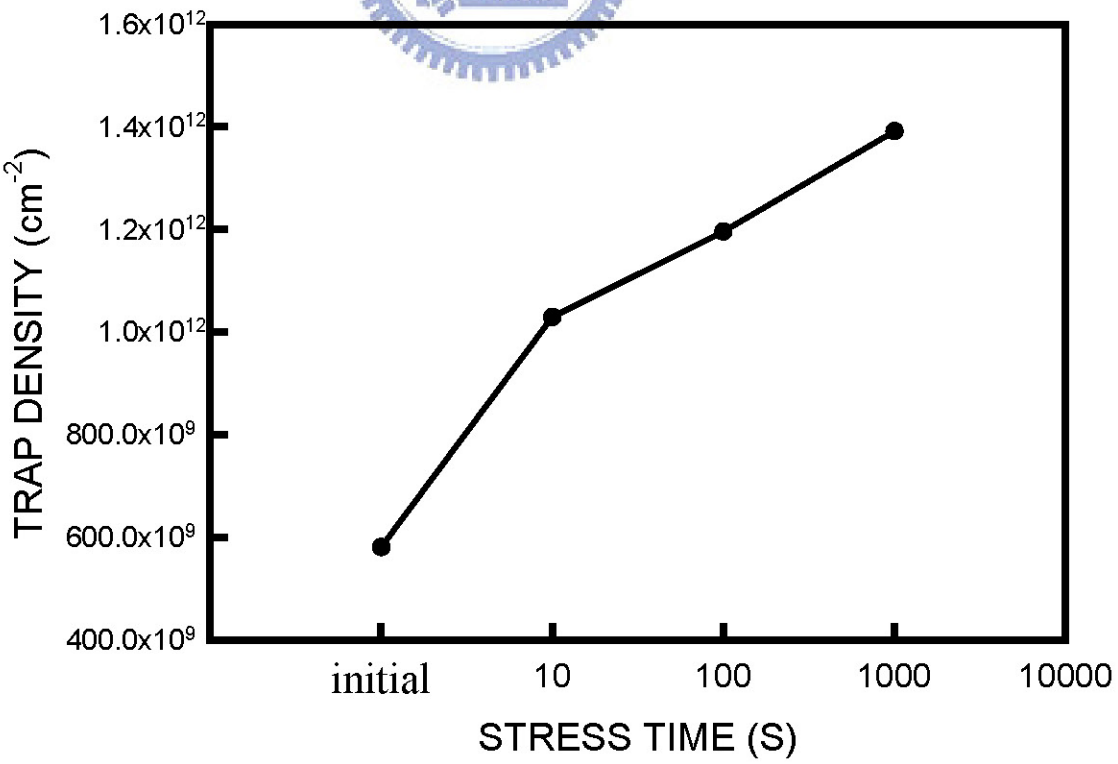

Fig. 4-19 the trap density versus stress time curve of an n-channel ELA TFT with 1.5 μm LDD

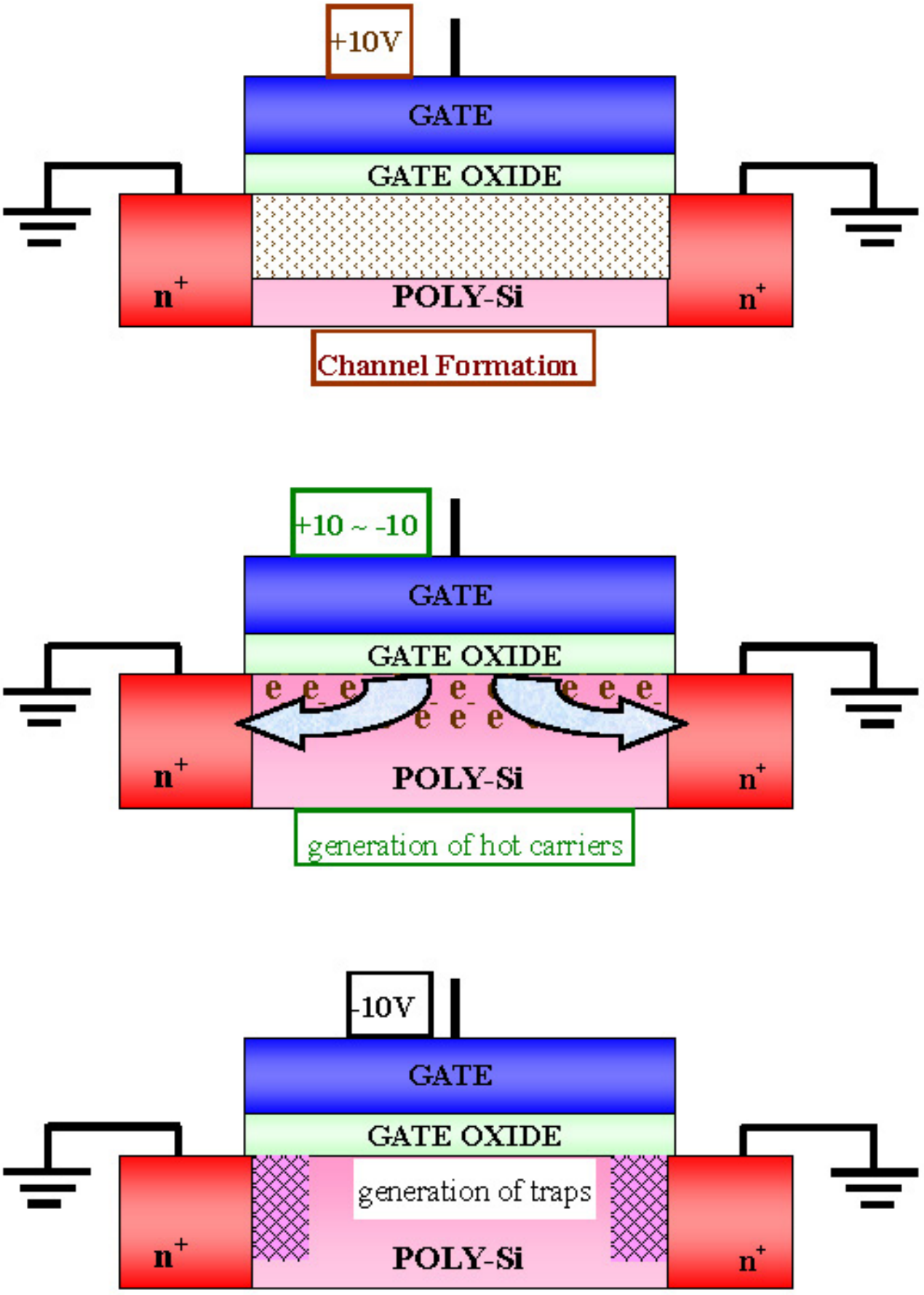

Fig. 4-20 the degradation model under dynamic stress

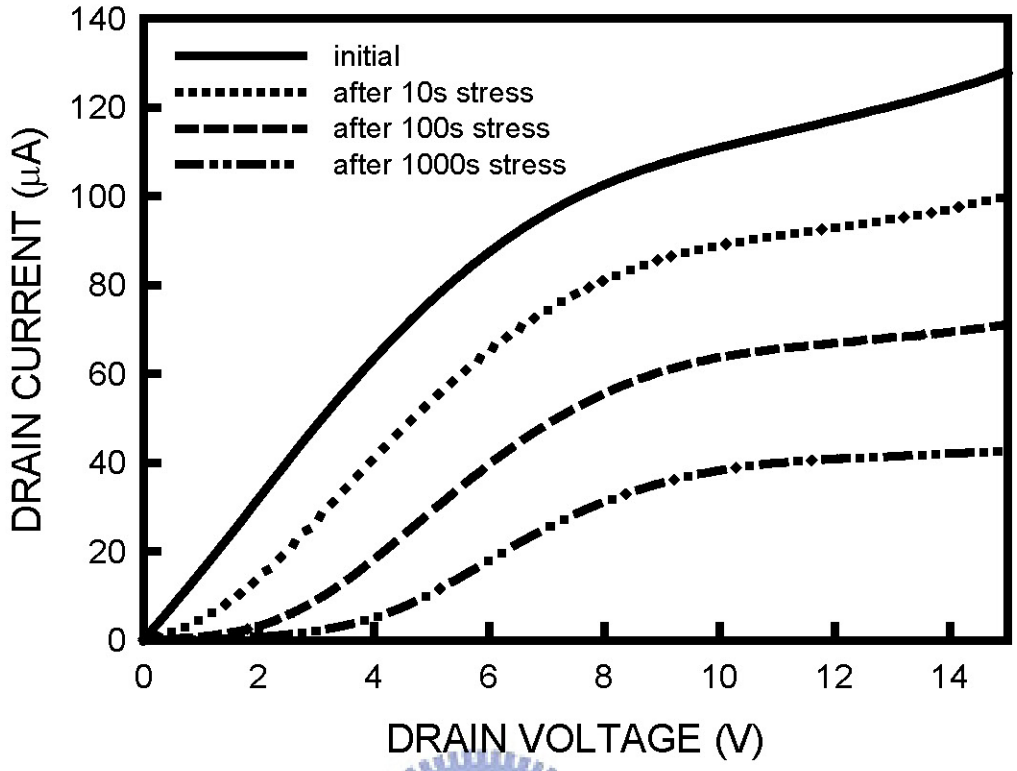

Fig. 4-21 the I_{DS}–V_{DS} curves of an n-channel ELA TFT without LDD at V_{GS}=10V

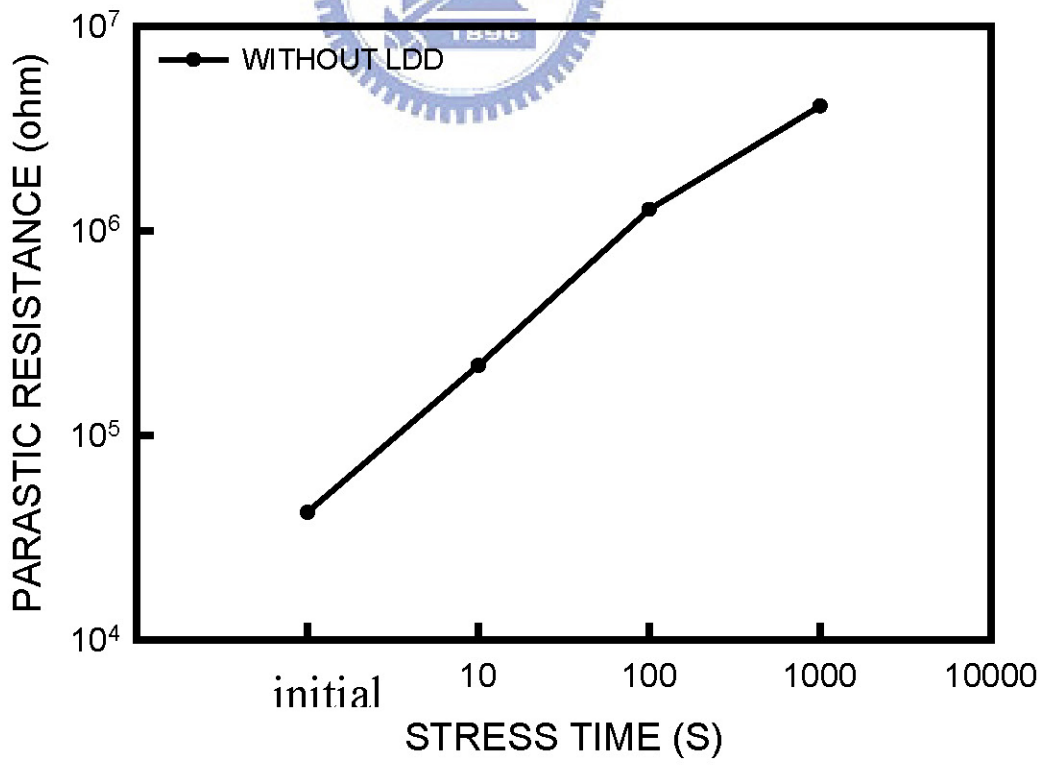

Fig. 4-22 the parasitic resistance versus stress time curve of an n-channel ELA TFT without LDD

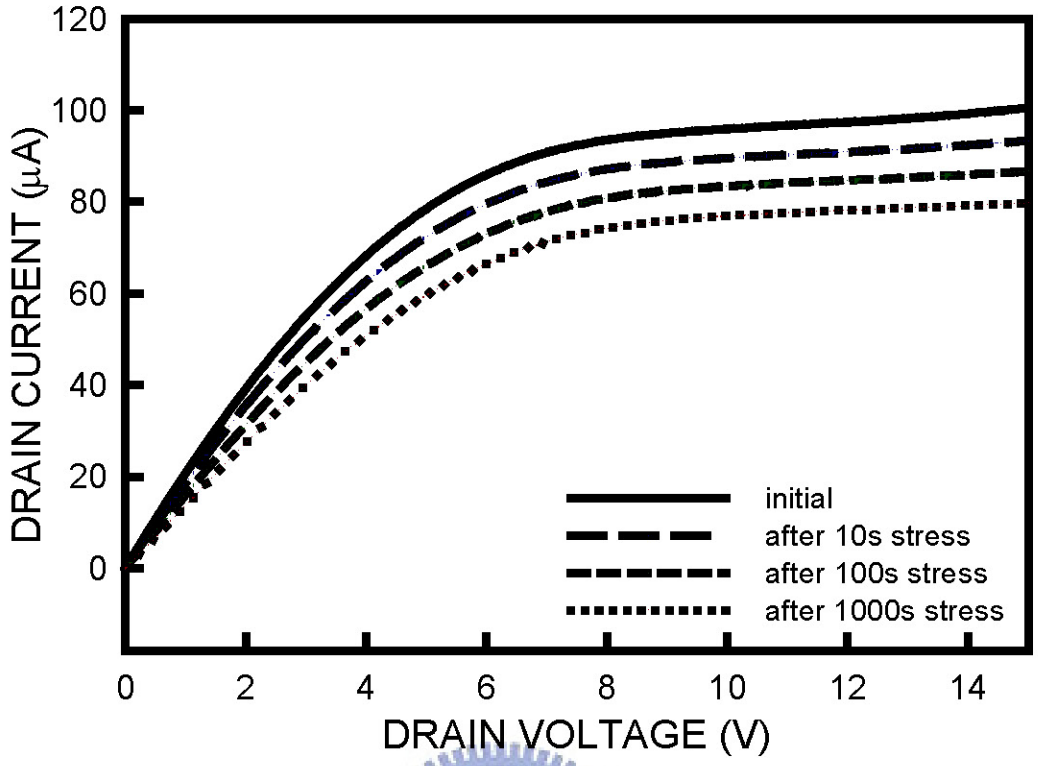

Fig. 4-23 the I_{DS}–V_{DS} curves of an n-channel ELA TFT with 1.5 μm LDD

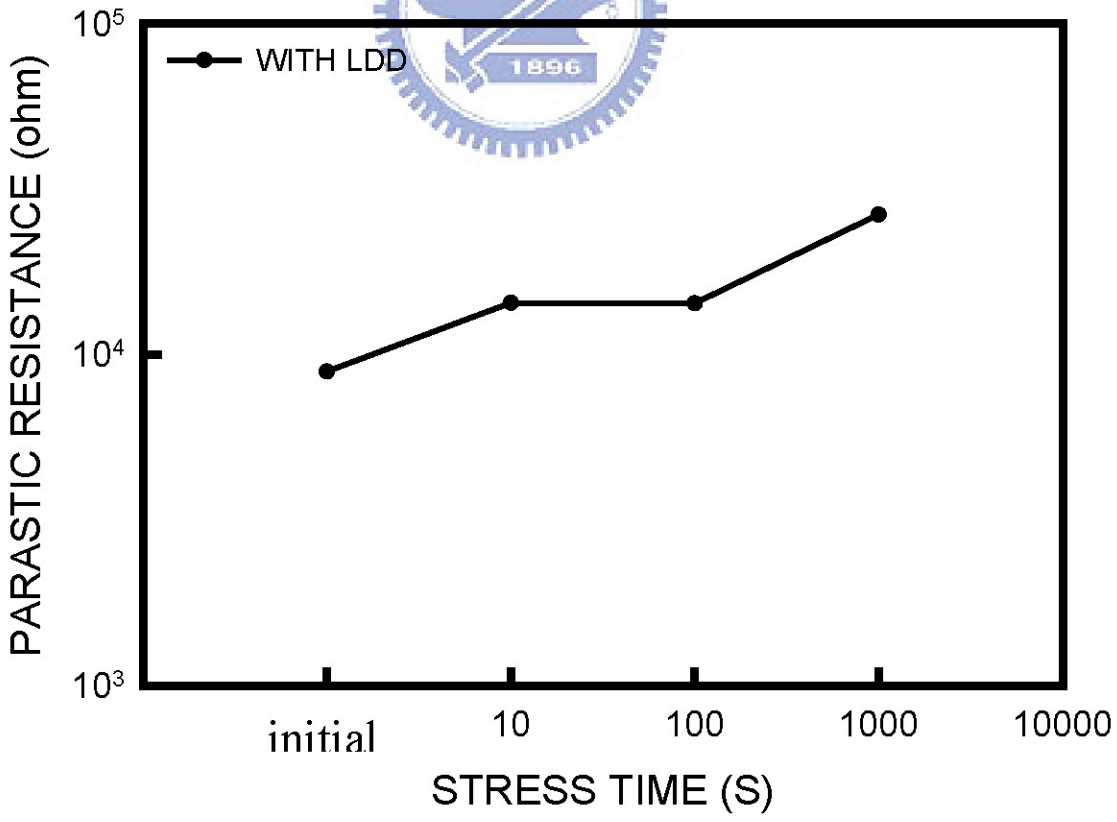

Fig. 4-24 the parasitic resistance versus stress time curve of an n-channel ELA TFT with 1.5 μm LDD