

4.2 Grain Boundaries Effects of Low-Temperature Polycrystalline Silicon Thin Film Transistors

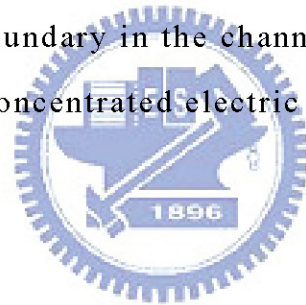
There are four kinds of low temperature thin film transistors fabricated by novel process illustrated as Fig. 4-25. One group is devices with and without lightly doped drain, and the other is with and without main grain boundary in the channel. The main grain boundary is different from the conventional random grain boundary. The SEM picture of the polycrystalline silicon thin film made by novel process is shown as Fig. 4-26. The main grain boundary may exist in the thin film transistors channel owing to the process of hard control. Therefore, we classify these devices into GB (devices with main grain boundary in the channel) and NGB (devices without main grain boundary in the channel). Fig. 4-27 shows the definition and location of GB and NGB devices. The main grain boundary may play an important role under dynamic stress.

In order to investigate the main grain boundary effect under dynamic stress, the GB and NGB devices are employed. First, Fig. 4-28(a) and Fig. 4-28(b) are the $N_{ID_S}-V_{GS}$ curves of polycrystalline silicon thin film transistor with (GB) and without (NGB) main grain boundary in the channel without LDD, respectively. It is obvious that the degradation of polycrystalline silicon thin film transistor with main grain boundary in the channel (GB) is more sever than that of without main grain boundary (NGB), after 1000s dynamic stress. It may be attributed to the main grain boundary causes more concentrated electric field at the gate oxide interface. The simulation result is shown as Fig. 4-29. In Fig.4-29, the left is NGB gate oxide interface, and the right is GB gate oxide interface.

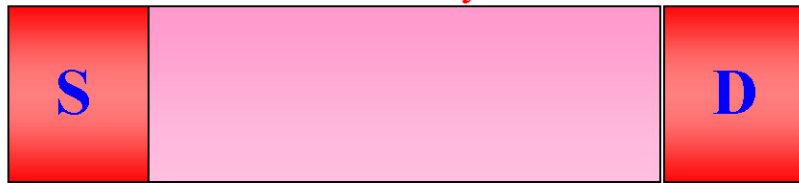
In order to reduce the effect of lightly doped drain, the polycrystalline

silicon thin film transistors with lightly doped drain are introduced. Fig. 4-30(a) and Fig. 4-30(b) reveal the $I_{DS}-V_{GS}$ curves of polycrystalline silicon thin film transistors without (NGB) and with (GB) main grain boundary in the channel with $1.0\mu\text{m}$ lightly doped drain at $V_{DS}=0.1\text{V}$. Notably, the on-current is also degraded more serious in GB than in NGB. Fig. 4-31(a) (NGB) and Fig. 4-31(b) (GB) exhibit the degraded on-current ratio are 27.62% and 22.08%, respectively.

Besides, the subthreshold swing of each device does not change much. The deep state may not be responsible for the degradation mechanism under dynamic stress, and the tail state may be generated after stress. These states may be located at source/drain junction, grain boundaries, and the main grain boundary caused damage at gate oxide interface. Consequently, the device with main grain boundary in the channel degrades more serious, which may be attributed to the concentrated electric field at the gate oxide interface.



device **without LDD** and **WITHOUT**
Main Grain Boundary in the channel



device **without LDD** and **WITH**
Main Grain Boundary in the channel



device **with LDD** and **WITHOUT**
Main Grain Boundary in the channel



device **with LDD** and **WITH**
Main Grain Boundary in the channel

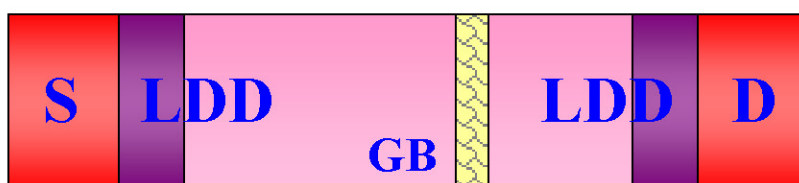


Fig. 4-25 four kinds of low temperature thin film transistors fabricated by novel process

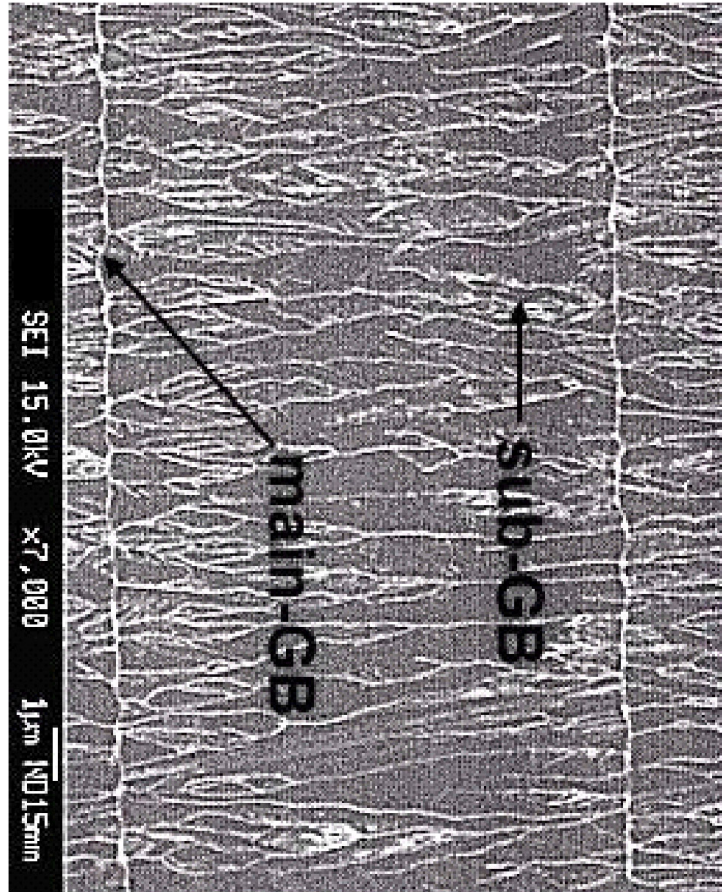


Fig. 4-26 SEM picture of the polycrystalline silicon thin film made by novel process

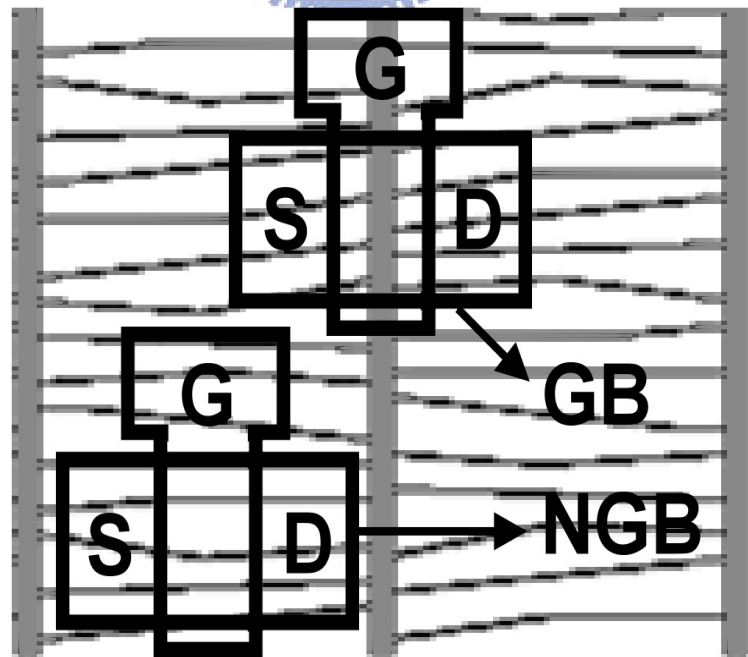


Fig. 4-27 the definition of GB (devices with main grain boundary in the channel) and NGB (devices without main grain boundary in the channel)