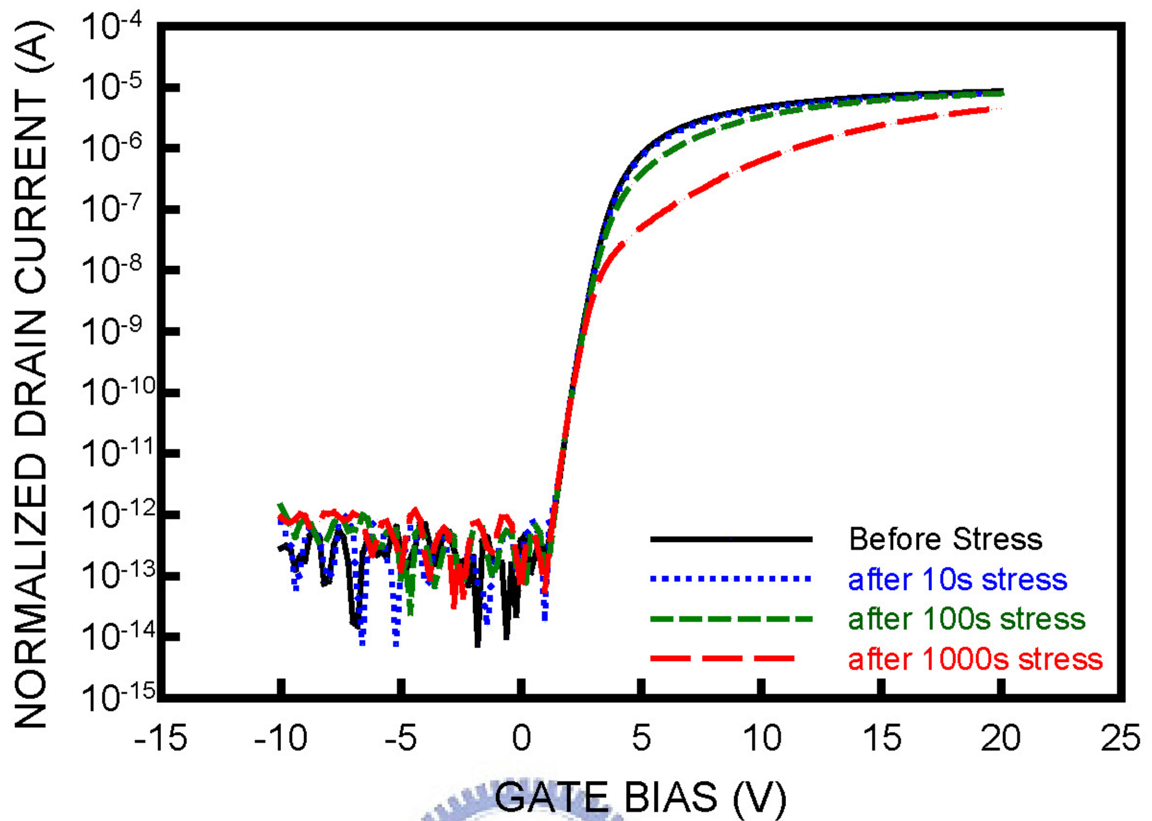

Fig. 4-28(a) the NI_{DS}-V_{GS} curves of poly-Si TFT with main grain boundary in the channel (GB device) without LDD

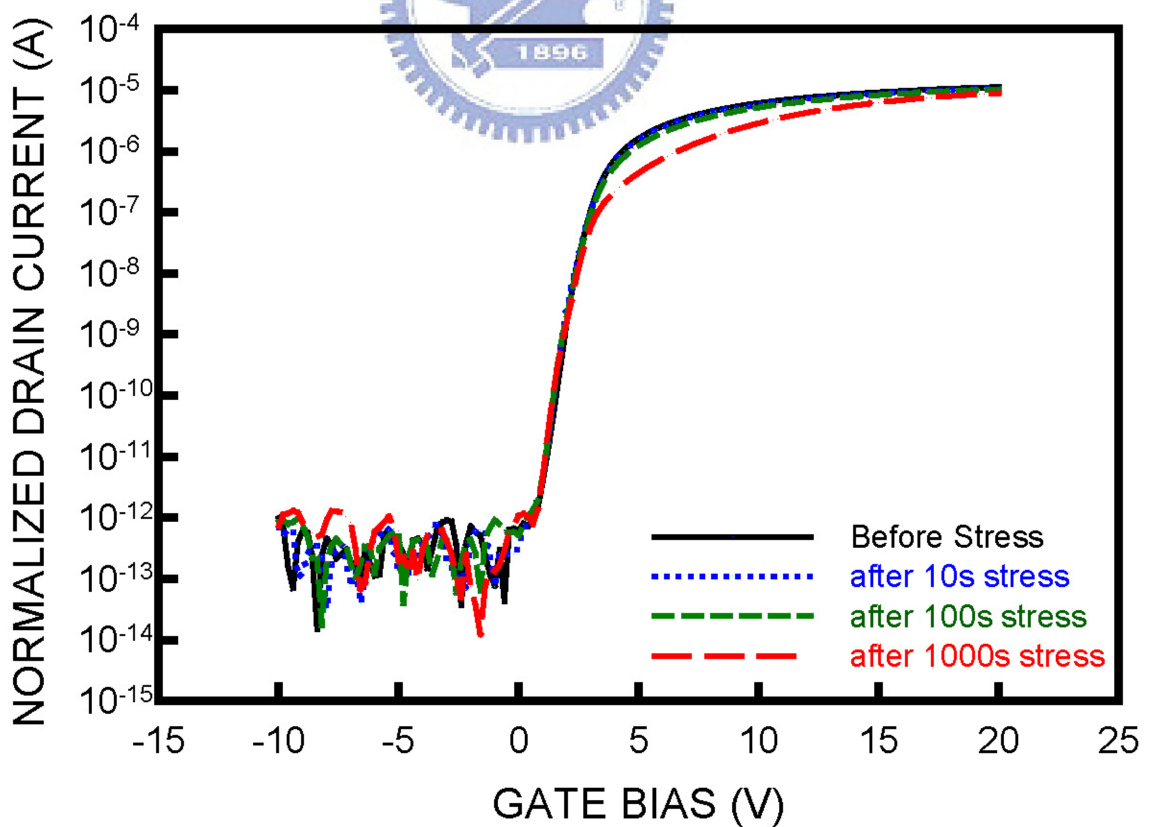

Fig. 4-28(b) the NI_{DS}-V_{GS} curves of poly-Si TFT without main grain boundary in the channel (NGB device) without LDD

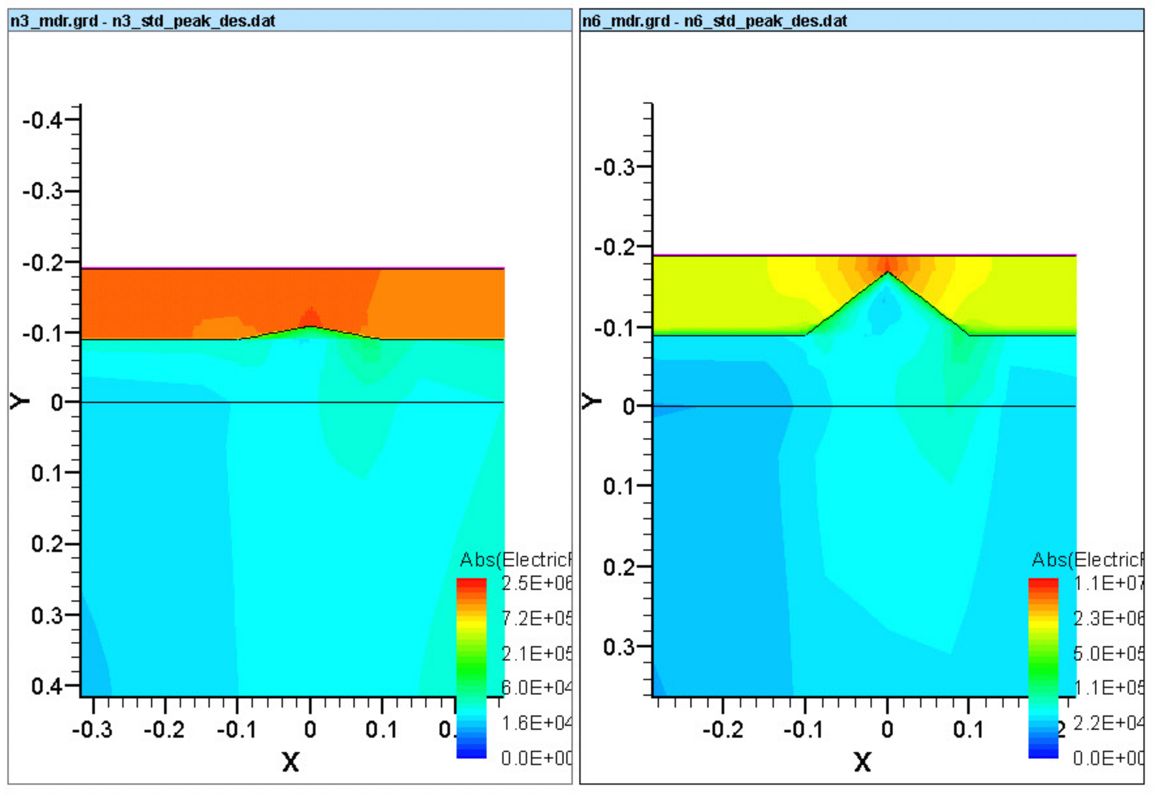

Fig. 4-29 the electrical field simulation of NGB and GB at gate oxide interface, the left is NGB, and the right is GB

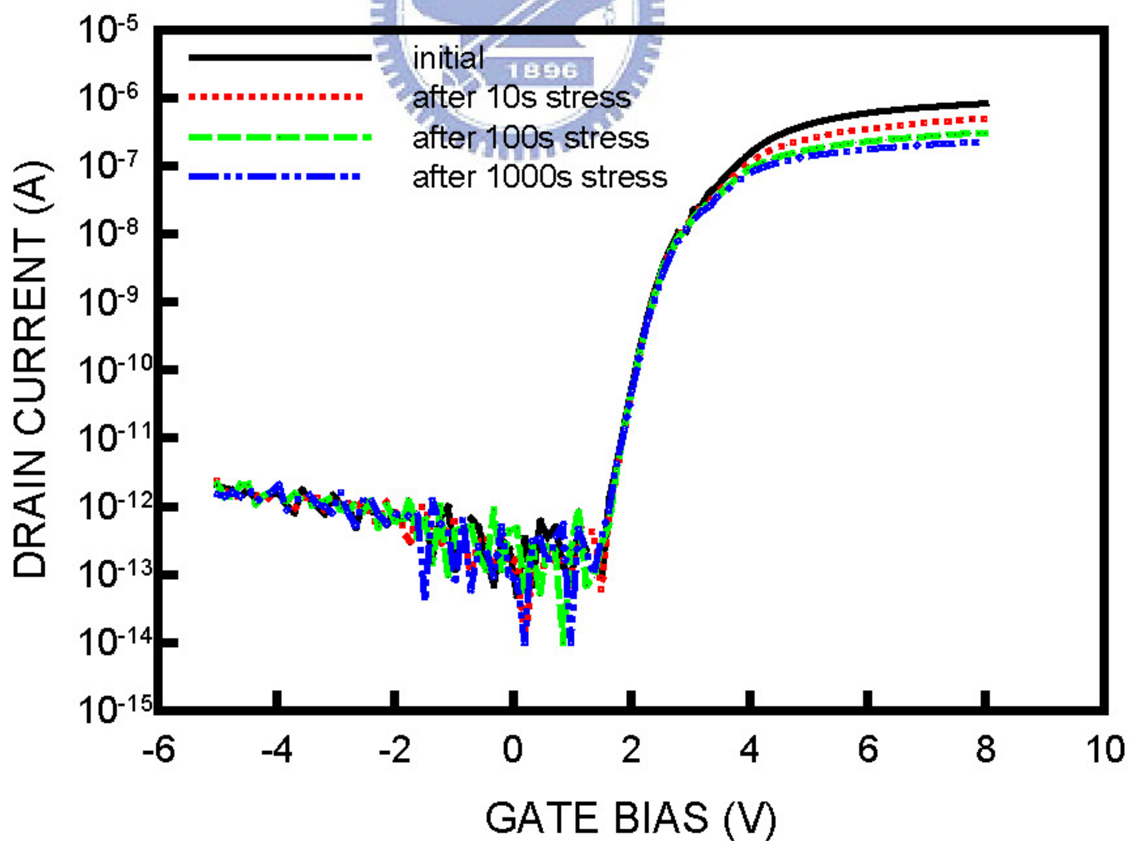

Fig. 4-30(a) the I_{DS}-V_{GS} curves of poly-Si TFT without main grain boundary in the channel (NGB device) with 1.0 μm LDD LDD

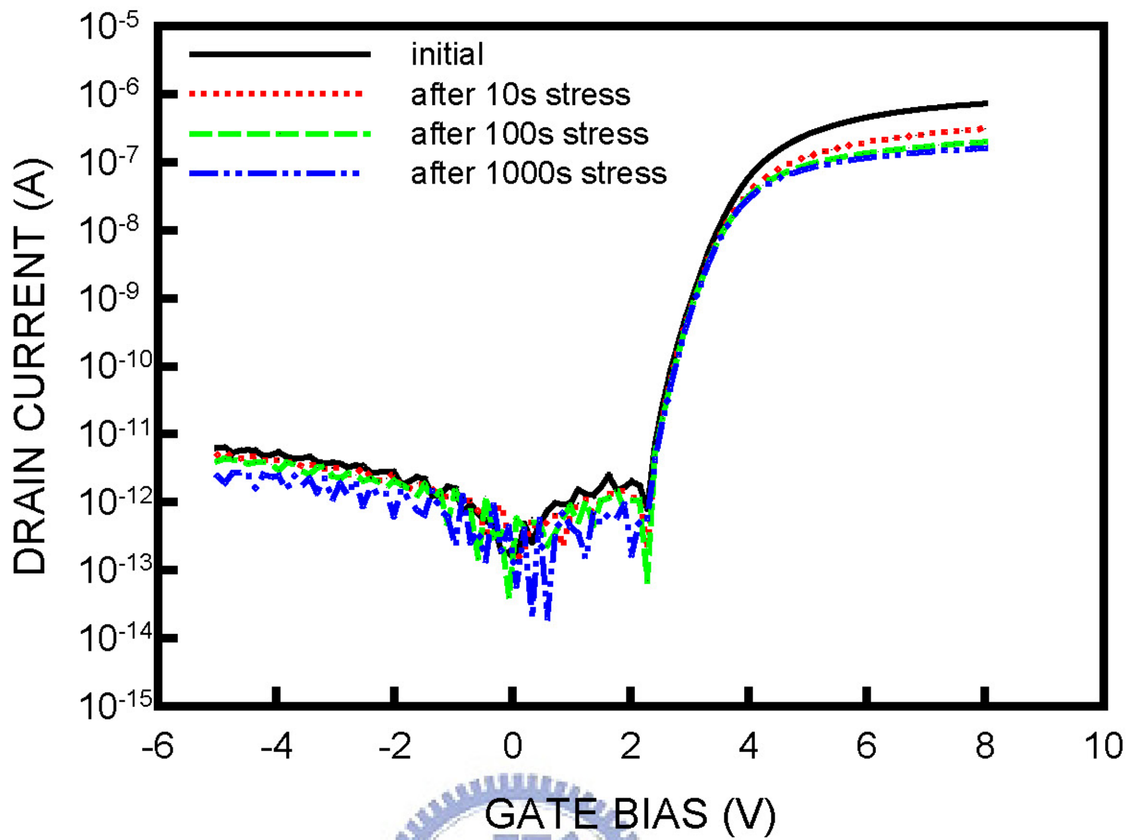

Fig. 4-30(b) the I_{DS}-V_{GS} curves of poly-Si TFT with main grain boundary in the channel (GB device) with 1.0 μm LDD LDD

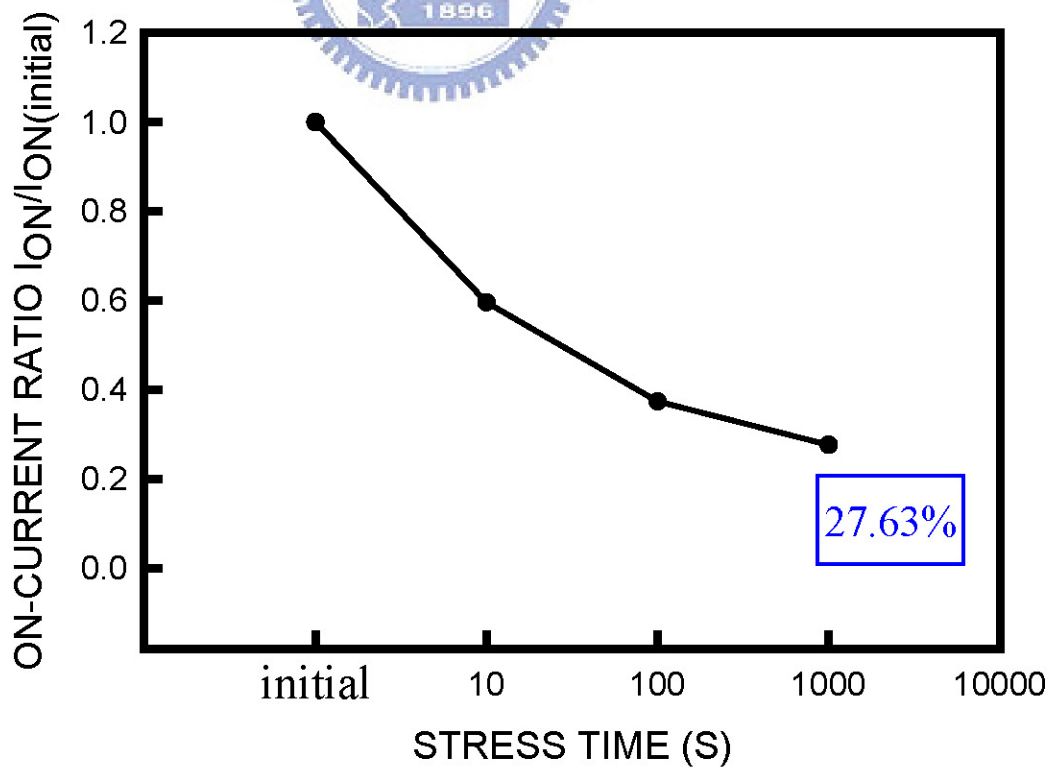

Fig. 4-31(a) the degraded on-current ratio versus stress time curve of an NGB TFT with 1.0 μm LDD at V_{DS}=0.1V

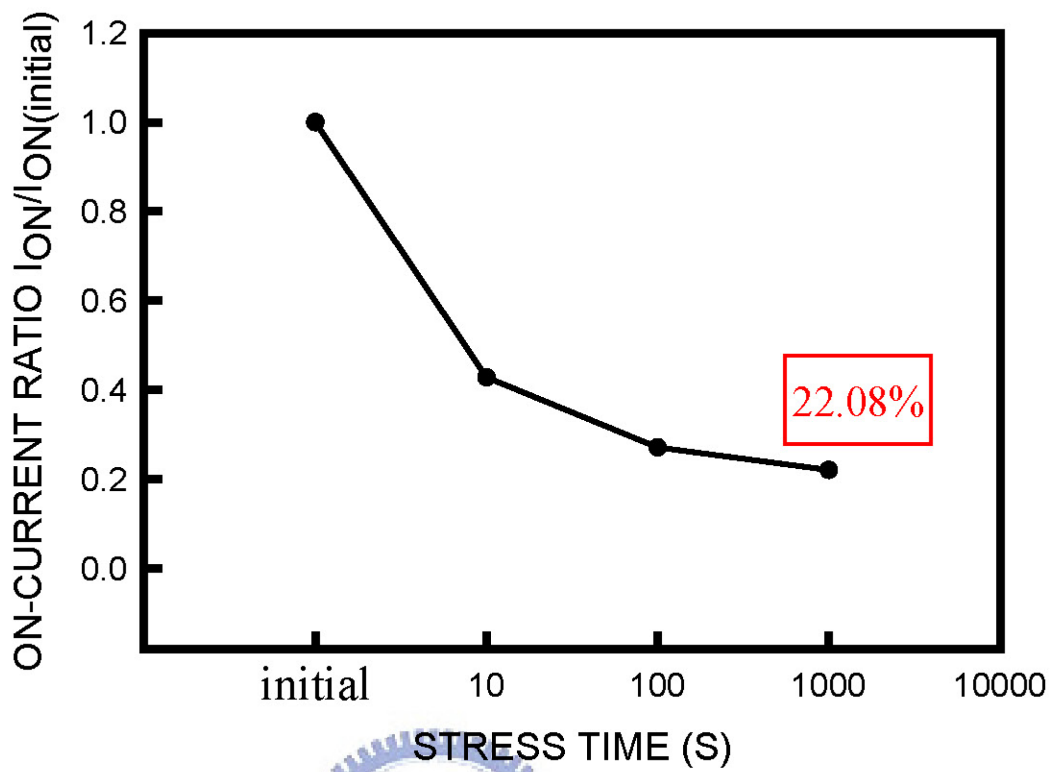

Fig. 4-31(b) the degraded on-current ratio versus stress time curve of an GB TFT with 1.0 μm LDD at V_{DS}=0.1V