CHAPTER 5 CONCLUSION

The degradation phenomenon and instability mechanisms of n-channel low temperature polycrystalline silicon thin film transistors under dynamic stress were investigated in detail by means of capacitance-voltage and current-voltage analysis. In addition, the instability mechanisms of novel process fabricated thin film transistors were also studied.

In capacitance-voltage analysis, the curves were stretched out with increasing measurement frequency due to different depth of trap state. Each frequency may correspond to different location of trap state. For example, 10 KHz measurement frequency corresponds to deep state, and 1 MHz measurement frequency is mainly attributed to tail state. Moreover, the capacitance-voltage characteristics were also stretched out with increasing stress time at the same measurement frequency, especially at 1 MHz. Increasing the amount of trap state may introduce serious RC delay effect. If the stretched out capacitance-voltage curve is measured at high frequency, the generated traps may be at the location near conduction band, namely tail state. Consequently, the trap at tail state is increased for polycrystalline silicon thin film transistors after dynamic stress.

In current-voltage analysis, the results are similar to the capacitance-voltage analysis. The generated traps may be at tail state after dynamic stress. Besides, the on-current in I_{DS}-V_{GS} curves degraded with dynamic stress time, which implied the creation of tail state. The subthreshold swing in I_{DS}-V_{GS} characteristics seemed unchanged, which supposed the amount of deep state might not be responsible for degradation under dynamic stress. Then the extracted trap density of state also revealed the amount of trap state increasing with stress time.

The lightly doped drain effects of low temperature polycrystalline silicon thin film transistors were investigated. The thin film transistors with lightly doped drain were less degraded under dynamic stress in virtue of the lightly doped drain can reduce the maximum electric field at source/drain junction. Not only the excimer laser annealing transistors with lightly doped drain, but also the transistors novel process made are less degraded.

With novel process, the main grain boundary may exist in the channel of polycrystalline silicon thin film transistors, and the main grain boundary may play an import role of transistor degradation. The geometry of the novel process fabricated thin film transistors is prominent at the polycrystalline silicon and gate oxide interface. Since the shape of the main grain boundary is unusual, the concentrated electric field at the main grain boundary gate oxide interface may be the main degradation mechanism. Therefore, the region is subjected more stress under dynamic stress. The polycrystalline silicon thin film transistors with main grain boundary in the channel (GB) were degraded more than that without main grain boundary in the channel (NGB).