低溫多晶矽薄膜電晶體在動態操作下之可靠度研究

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摘要

利用低溫多晶矽薄膜電晶體作為主動陣列液晶顯示器及主動陣列有機發光二極體的畫素電晶體以及驅動電路已經成為主要的關鍵技術。有幾種新式的結晶方式可以製作出高遷移率、高驅動電流的低溫多晶矽薄膜電晶體，然而有些新式結晶方法將使得通道中產生一些主要的晶粒邊界有別於一般的晶粒邊界。這種主要的晶粒邊界在元件操作時造成的劣化佔主要的角色。當低溫多晶矽薄膜電晶體應用為驅動電路時，將操作於閘極交流訊號，低溫多晶矽薄膜電晶體將被施與電性應力的破壞。因此低溫多晶矽薄膜電晶體晶粒邊界對元件在閘極交流訊號下可靠度研究具有相當的重要性。

在本篇論文中，我們採用準分子雷射製作以及新式結晶方法製作的低溫多晶矽薄膜電晶體作可靠度的測試。除此之外，我們利用電容-電壓量測方法研究準分子雷射製作的低溫多晶矽薄膜電晶體經過閘極交流訊號的電性應力破壞後的劣化情形。也利用

電流-電壓量測方法研究新式結晶方法製作的低溫多晶矽薄膜電晶體在閘極動態電性應力破壞後的劣化情形。

準分子雷射製作的 n 型-低溫多晶矽薄膜電晶體在電容-電壓量測方法中，電容-電壓量測方法所施加的小訊號不會對固定氧化層電荷造成影響，而能隙中的缺陷狀態由於狀態深度不同，會對不同頻率的量測頻率有所反應。深層的缺陷狀態需要較長的輻射時間，對應於較小的量測頻率；淺層的缺陷狀態需要較短的輻射時間，對應於較長的量測頻率。因此我們利用不同的頻率 10KHz、100KHz、1MHz 以及不同的電性應力破壞時間 10s、100s、1000s 來探討當低溫多晶矽電晶體在閘極交流訊號下缺陷狀態的劣化情形。

在電流-電壓量測方法中，我們採用的是利用新式結晶方法製作的 n 型-低溫多晶矽薄膜電晶體，並選擇有主要晶粒邊界在通道區域以及沒有主要晶粒邊界在通道區域的元件作為研究的對象。經由閘極動態電性應力破壞後，沒有輕參雜汲極的元件導通電流迅速下降、遷移率下降；反之，有輕參雜汲極的元件裂化比較不嚴重。此外，有主要晶粒邊界在通道中的元件，裂化情形也較嚴重，這是由於主要晶粒邊界在表面的幾何形狀較為尖凸，且主要晶粒邊界有大量的缺陷，造成較強的電場，使得元件裂化較嚴重。

Study on Reliability of Low-Temperature Polycrystalline Silicon Thin Film Transistors under Dynamic Stress

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Abstract

The low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) have become the main technology and are applied for active matrix liquid crystal display (AMLCD), organic light emitting diode, and driving circuits. Recently, the low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) with high field-effect mobility and high driving current can be fabricated by several novel crystallization technologies. However, the main grain boundaries different from the general grain boundaries made by solid phase crystallization (SPC) are generated in the channel due to these novel technologies. The main grain boundaries play an important role of the degradation of the devices under dynamic operation. The low temperature polycrystalline (poly-Si) thin film transistors (TFTs) are operated under gate bias alternative current signal and subjected to electrical stress while it is applied for driving circuits. Thus, the study of influence of grain boundaries on reliability of low-temperature polycrystalline silicon thin film transistors under dynamic gate bias stress becomes important.

In this thesis, we adopt the low temperature polycrystalline silicon thin film transistors fabricated by the excimer laser annealing and the novel process for the instability research. In addition, the capacitance-voltage

analysis was employed to study on the degradation of excimer laser annealing low temperature polycrystalline silicon thin film transistors under dynamic stress. We also used current-voltage analysis to investigate on the degradation of thin film transistors fabricated by novel process under dynamic stress.

In capacitance-voltage analysis, the applied small signal does not affect the fixed oxide charge. However, the traps at different states were responded to different measurement frequency due to different depth of states. Deeper trap states need longer emission time corresponding to larger measurement frequency; shallow trap states need shorter emission time corresponding to smaller measurement frequency. Therefore, we used not only different measurement frequency, 10 KHz, 100 KHz, 1 MHz, but also different stress time, 10 s, 100 s, 1000 s, to investigate the degradation of trap density of state of low temperature polycrystalline silicon thin film transistors.

In current-voltage analysis, we also studied on the novel process thin film transistors whose main grain boundary may exist in the channel. After dynamic stress, not only excimer laser annealing but also novel process thin film transistors without lightly doped drain were degraded more severe than ones with lightly doped drain, that exhibits on rapid degradation of on-current and mobility. Furthermore, the geometry of the novel process fabricated thin film transistors is prominent at the polycrystalline silicon and gate oxide interface. Since the shape of the main grain boundary is unusual, the electric field at the main grain boundary is concentrated on gate oxide interface. Therefore, the region is subjected more stress under dynamic stress. The polycrystalline silicon thin film transistors with main grain boundary in the channel (GB) were degraded more than that without main grain boundary in the channel (NGB).