

Contents

Abstract (Chinese)	i
Abstract (English)	iii
Acknowledgement	v
Contents	vi
Figure Captions	viii
Table Captions	xiii
CHAPTER 1 INTRODUCTION	1
1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)	1
1.2 Motivation	3
1.3 Thesis Organization	5
CHAPTER 2 FABRICATION AND CHARACTERIZATION	6
2.1 Fabrication Methods of Low-Temperature Polycrystalline Silicon Thin Film Transistors	6
2.2 Set Up Instruments	9
2.2.1 Stress Setup	
2.2.2 Current-Voltage (I-V) Measurement	
2.2.3 Capacitance-Voltage (C-V) Measurement	
2.3 Methods of Device Parameter Extraction	14
2.3.1 Determination of the On/Off Ratio	
2.3.2 Determination of the Subthreshold Swing	
2.3.3 Determination of the Field-Effect Mobility	
2.3.4 Determination of the Threshold Voltage	
2.3.5 Determination of the Trap Density	

CHAPTER 3 EXPERIMENT	20
3.1 Electrical Degradation of N-Channel Poly-Si TFT under Dynamic Stress by Capacitance-Voltage (C-V) Measurement	20
3.2 Electrical Degradation of N-Channel Poly-Si TFT With and Without Grain Boundary in Channel under Dynamic Stress by Current-Voltage (I-V) Measurement.....	27
 CHAPTER 4 RESULTS AND DISCUSSION	 30
4.1 Lightly Doped Drain Effects of Low-Temperature Polycrystalline Silicon Thin Film Transistors	30
4.2 Grain Boundaries Effects of Low-Temperature Polycrystalline Silicon Thin Film Transistors	57
 CHAPTER 5 CONCLUSION	 65
 REFERENCE	 67
 RESUME	 71

