Figure Captions

- Fig. 2-1 the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain
- Fig. 2-2 the top-gate structure of low temperature polycrystalline silicon thin film transistor with lightly doped drain
- Fig. 2-3 the stress setup of the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain (LDD)
- Fig. 2-4 the waveform of the stress setup
- Fig. 2-5 the current-voltage (I-V) measurement of the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain (LDD)
- Fig. 2-6 the capacitance-voltage (C-V) measurement of the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain (LDD)
- Fig. 3-1 metal-insulator-semiconductor capacitor
- Fig. 3-2 energy-band diagram of ideal metal-insulator-semiconductor capacitor at V=0 for p-type semiconductor
- Fig. 3-3(a) energy-band diagram of ideal metal-insulator-semiconductor (p-type semiconductor) capacitor when $V\neq 0$ (V<0)) for accumulation
- Fig. 3-3(b) energy-band diagram of ideal metal-insulator-semiconductor (ptype semiconductor) capacitor when $V\neq 0$ (V>0) for depletion
- Fig. 3-3(c) energy-band diagram of ideal metal-insulator-semiconductor (p-type semiconductor) capacitor when $V\neq 0$ (V>0) for inversion
- Fig. 4-1(a) the initial C_{GS}-V curves of an n-channel ELA TFT without LDD at different measurement frequency

- Fig. 4-1(b) the initial C_{GD}-V curves of an n-channel ELA TFT without LDD at different measurement frequency
- Fig. 4-2(a) a conventional p-Si metal-oxide-semiconductor capacitor capacitance-voltage curve
- Fig. 4-2(b) a typical polycrystalline silicon thin film transistor gate-drain capacitance-voltage curve in our experiment
- Fig. 4-3(a) a equivalent total capacitance circuit of metal-oxidesemiconductor capacitor
- Fig. 4-3(b) a equivalent total capacitance circuit of polycrystalline silicon thin film transistor
- Fig. 4-4 A diagram of that with increasing the measurement frequency, the capacitance-voltage curve is degraded.
- Fig. 4-5(a) When the measurement frequency is lower, deep state corresponds to larger emission time τ.
- Fig. 4-5(b) When the measurement frequency is higher, tail state corresponds to smaller emission time t.
- Fig. 4-6(a) The C_{GD}-V curves of n-channel poly-Si ELA TFT without LDD at the 10KHz measurement frequency
- Fig. 4-6(b) The C_{GD}-V curves of n-channel poly-Si ELA TFT without LDD at the 100KHz measurement frequency
- Fig. 4-6(c) The C_{GD}-V curves of n-channel poly-Si ELA TFT without LDD at the 1000KHz measurement frequency
- Fig. 4-7(a) The C_{GS} -V curves of n-channel poly-Si ELA TFT without LDD at the 10KHz measurement frequency
- Fig. 4-7(b) The C_{GS}-V curves of n-channel poly-Si ELA TFT without LDD at the 100KHz measurement frequency
- Fig. 4-7(c) The C_{GS}-V curves of n-channel poly-Si ELA TFT without LDD at the 1000KHz measurement frequency

- Fig. 4-8(a) the initial C_{GS}-V curves of an n-channel ELA TFT with LDD at different measurement frequency
- Fig. 4-8(b) the initial C_{GD}-V curves of an n-channel ELA TFT with LDD at different measurement frequency
- Fig. 4-9(a) the C_{GS}-V curves of an n-channel ELA TFT with LDD at different measurement frequency after 1000s stress
- Fig. 4-9(b) the C_{GD}-V curves of an n-channel ELA TFT with LDD at different measurement frequency after 1000s stress
- Fig. 4-10(a) the $C_{\rm GD}-V$ curves of an n-channel ELA TFT with LDD at the 10KHz measurement frequency
- Fig. 4-10(b) the C_{GD}-V curves of an n-channel ELA TFT with LDD at the 100KHz measurement frequency
- Fig. 4-10(c) the $C_{\rm GD}-V$ curves of an n-channel ELA TFT with LDD at the 1000KHz measurement frequency
- Fig. 4-11(a) the C_{GS}-V curves of an n-channel ELA TFT with LDD at the 10KHz measurement frequency
- Fig. 4-11(b) the C_{GS} -V curves of an n-channel ELA TFT with LDD at the 100KHz measurement frequency
- Fig. 4-11(c) the C_{GS}-V curves of an n-channel ELA TFT with LDD at the 1000KHz measurement frequency
- Fig. 4-12 the $I_{DS}{-}V_{GS}$ curves of an n-channel ELA TFT without LDD at $V_{DS}{=}0.1V$
- Fig. 4-13 the degraded on-current ratio versus stress time curve of an n-channel ELA TFT without LDD at $V_{\rm DS}{=}0.1{\rm V}$
- Fig. 4-14 the degraded mobility ratio versus stress time curve of an n-channel ELA TFT without LDD at $V_{\rm DS}{=}0.1V$
- Fig. 4-15 the trap density versus stress time curve of an n-channel ELA TFT without LDD

- Fig. 4-16 the $I_{DS}-V_{GS}$ curves of an n-channel ELA TFT with 1.5 μ m LDD at V_{DS} =0.1 V
- Fig. 4-17 the degraded on-current ratio versus stress time curve of an n-channel ELA TFT with 1.5 μ m LDD at V_{DS} =0.1V
- Fig. 4-18 the degraded mobility ratio versus stress time curve of an n-channel ELA TFT with 1.5 μ m LDD at V_{DS} =0.1V
- Fig. 4-19 the trap density versus stress time curve of an n-channel ELA TFT with 1.5 μ m LDD
- Fig. 4-20 the degradation model under dynamic stress
- Fig. 4-21 the $I_{\rm DS}{-}V_{\rm DS}$ curves of an n-channel ELA TFT without LDD at $$V_{\rm GS}{=}10\,{\rm V}$$
- Fig. 4-22 the parasitic resistance versus stress time curve of an n-channel ELA TFT without LDD
- Fig. 4-23 the I_{DS} - V_{DS} curves of an n-channel ELA TFT with 1.5 μ m LDD
- Fig. 4-24 the parasitic resistance versus stress time curve of an n-channel ELA TFT with 1.5 μ m LDD
- Fig. 4-25 four kinds of low temperature thin film transistors fabricated by novel process
- Fig. 4-26 SEM picture of the polycrystalline silicon thin film made by novel process
- Fig. 4-27 the definition of GB (devices with main grain boundary in the channel) and NGB (devices without main grain boundary in the channel)
- Fig. 4-28(a) the $\rm NI_{DS}\text{-}V_{GS}$ curves of poly-Si TFT with main grain boundary in the channel (GB device) without LDD
- Fig. 4-28(b) the NI_{DS} - V_{GS} curves of poly-Si TFT without main grain boundary in the channel (NGB device) without LDD
- Fig. 4-29 the electrical field simulation of NGB and GB at gate oxide interface, the left is NGB, and the right is GB

- Fig. 4-30(a) the I_{DS} - V_{GS} curves of poly-Si TFT without main grain boundary in the channel (NGB device) with 1.0 μ m LDD LDD
- Fig. 4-30(b) the I_{DS} - V_{GS} curves of poly-Si TFT with main grain boundary in the channel (GB device) with 1.0 μ m LDD LDD
- Fig. 4-31(a) the degraded on-current ratio versus stress time curve of an NGB TFT with 1.0 μ m LDD at V_{DS} =0.1V
- Fig. 4-31(b) the degraded on-current ratio versus stress time curve of an GB TFT with 1.0 μ m LDD at V_{DS} =0.1V



Table Captions

Table 3-1 electrical parameters variation correspond to possible degradation reason

Table 4-1 the subthreshold swings of poly-Si TFTs without and with LDD after dynamic stress

