CHAPTER 1 INTRODUCTION

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In recent years, the attraction in polycrystalline silicon (poly-Si) thin film transistor (TFT) technology has increased drastically.[1.1] Low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) have been widely used for many applications such as personal digital assistants (PDAs), digital cameras, cellular phones, laptops, PCs, and so on.[1.2] Currently, the main application of polycrystalline silicon (poly-Si) thin film transistors (TFTs) is the flat panel display (FPD), for instance, active matrix liquid crystal displays, active matrix organic light emitting diode displays, and etc.[1.3] Except for the display field, polycrystalline silicon (poly-Si) thin film transistors (TFTs) have been successfully applied to the static random access memories (SRAMs)[1.4], the dynamic random access memories (DRAMs)[1.5], the electrically erasable programmable read only memories (EEPROMs)[1.6], the one-transistor single electron memory devices[1.7], the nonvolatile analog memories (NVM)[1.8], the magnetic sensors[1.9], and the fingerprint sensors[1.10].

Generally speaking, the electron field-effect-mobility of low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) is about 100 times larger than that of the conventional hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs). As a result of such a high electron field-effect-mobility, the low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) can provide higher turn-on-current than the

hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) in the same dimension. The higher electron field-effect-mobility leads to a higher driving current implies that the low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) make the time of charging the liquid crystal storage capacitors shorter. Therefore, as the low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) being the pixel-switching element, the dimension of that can be shrunk, which conduce to the higher aperture ratio, lower parasitic capacitance, and faster switching speed. Furthermore, the electron field-effect-mobility of low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) is much higher than that of the hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs), which represents the low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) are more suitable for the realization of system on panel (SOP) that will integrate display, memory, and central processing unit (CPU).[1.11]

In order to fabricate the high-performance polycrystalline silicon (poly-Si) thin film transistors (TFTs) in flat panel display (FPD), low temperature technology is required, since the strain point of the common active matrix liquid crystal display glass substrate, Croning 1737, is 666℃ [1.12]; therefore, the maximum process temperature is restricted to less than about 666℃, usually 600℃. In general, polycrystalline silicon (poly-Si) thin film transistors (TFTs) are also called low temperature polycrystalline silicon thin film transistors (LTPS) in the liquid crystal display industry. There are many techniques to achieve the goal of high performance such as amorphous silicon (a-Si) crystallization including solid phase crystallization (SPC)[1.13], metal induced crystallization (MIC)[1.14], laser crystallization (LC), and novel structure including multiple gates, offset gate, lightly doped drain (LDD), field induced drain (FID), gate-drain overlapped LDD (GO-LDD)[1.15], active

gate, double gates, hetero thin film transistors, vertical thin film transistors, and self-aligned silicide.

Among these technologies, solid phase crystallization (SPC) abounds grain boundaries in the channel regions, and even laser crystallization (LC). It is very difficult to eliminate grain boundaries in the channel regions for large dimension devices. The morphology of the grain boundaries are amorphous and the grain boundaries are filled with defects which results in that low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) operating under high drain electric field bring about an increase in a kink effect, the leakage current, and a pool hot carrier stress endurance. What is more, the grain boundaries in the channel region also reduce the electron field-effect-mobility of the polycrystalline silicon (poly-Si) thin film transistors (TFTs) by virtue of the electrons scattering or the trapping of defect states. Consequently, the grain boundaries in the channel region of the low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) cause the degradation in device performance, especially in the driving current and the electron field-effect-mobility, under gate-bias alternative current signal stressing.

1.2 Motivation

Although the electron field-effect-mobility of low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) is better than that of conventional hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs), the efforts of improving the electron field-effect-mobility and the reliability of low temperature polycrystalline silicon (poly-Si) thin

film transistors (TFTs) will not stop to make in order to realize high-performance display and system on panel (SOP). Hence, developing a means of reliability testing of polycrystalline silicon (poly-Si) thin film transistors (TFTs) becomes more and more important. To compare with conventional hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs), low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) can perform not only the role of pixel thin film transistors (TFTs) but also the role of driving circuits which are subjected to severe alternative current pulse stress. Therefore, the lack of reports interested in polycrystalline silicon (poly-Si) thin film transistors (TFTs) reliability of gate-bias alternative current signal stressing cause the degradation under dynamic operation should be understood.

Recently, many crystallization technologies are developed to form higher quality polycrystalline silicon (poly-Si), but no one can avoid the existences of grain boundaries in the channel region, especially for large dimension devices. To take the operation mode into account, the grain boundaries, the weaker structures and full of defect state, should be responsible for the degradation under gate-bias voltage dynamic stressing. For this reason, understanding the degradation mechanism under dynamic operation is a significant topic while polycrystalline silicon (poly-Si) thin film transistors (TFTs) as a driving circuit.

Consequently, in this thesis we study on the electrical degradation under gate-bias dynamic voltage stress of n-channel polycrystalline silicon (poly-Si) thin film transistors (TFTs) by two means, capacitance-voltage (C-V) measurement and current-voltage (I-V) measurement.

1.3 Thesis Organization

In the thesis, we use means of capacitance-voltage (C-V) measurement and current-voltage (I-V) measurement to study the electrical degradation under gate-bias dynamic voltage stress of n-channel polycrystalline silicon (poly-Si) thin film transistors (TFTs).

In chapter 2, how to fabricate low temperature polycrystalline silicon thin film transistors will be introduced. In addition, the instruments for current-voltage (I-V) and capacitance-voltage (C-V) measurement will be introduced including the methods of device parameter extraction such as the threshold voltage, subthreshold swing, electron field-effect-mobility, and On/Off ratio.

The experiment procedure will be mentioned in detail in chapter 3, which contains the capacitance-voltage (C-V) measurement and the current-voltage (I-V) measurement. Furthermore, we also studied the electrical degradation of n-channel polycrystalline silicon (poly-Si) thin film transistors (TFTs) with and without main grain boundaries in channel region under gate-bias dynamic voltage stress.

In chapter 4, the capacitance-voltage (C-V) measurement can clarify the electric degradation of low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs), and the current-voltage (I-V) measurement can also explain that if there is main grain boundary in channel region, the device will be degraded more. Hence, the instability of polycrystalline silicon thin film transistor devices with novel fabrication process will be investigated.

Finally, conclusions and future work will be described in chapter5.