CHAPTER 2 FABRICATION AND CHARACTERIZATION

2.1 Fabrication Methods of Low-Temperature Polycrystalline Silicon Thin Film Transistors

The low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) used in the experiment were fabricated by the conventional excimer laser annealing and the sequential laser on the glass substrates. These thin film transistors (TFTs) were the conventional n-channel and top-gate structure devices with or without lightly doped drain (LDD). The structures are shown in Fig. 2-1 and Fig. 2-2. The basic fabrication procedure of the conventional n-channel top-gate polycrystalline silicon (poly-Si) thin film transistors (TFTs) without lightly doped drain (LDD) is described as following. First, a thin layer of amorphous silicon (50 nm thick) was formed by plasma enhanced chemical vapor deposition (PECVD), and, subsequently, the film was dehydrogenated by furnace annealing. After dehydrogenation, the amorphous silicon (a-Si) film was crystallized by the XeCl excimer-laser (308 nm wavelength) with 350 mJ/cm^2 power of the line-shaped beam. Then, 100 nm thick gate oxide was deposited by plasma enhanced chemical vapor deposition (PECVD). Following the laser process, the gate oxide deposition, and, the implantation were adopted to define the source/drain (S/D) n$^+$ region and to have the ohmic contacts. Afterward an annealing process was carried out to activate the dopant impurities and MoW as gate metal was deposited by sputter. The dimensions of ELA thin film transistors in the capacitance-voltage measurement were with length 30 μm, width 30 μm and the overlap between gate and source/drain junction is 1 μm.

There are several methods to fabricate polycrystalline silicon thin film transistors such as continuous wave laser crystallization, solid phase crystallization, metal induced crystallization, and direct deposition. Hara et al. proposed diode pumped solid state (DSPP) continuous wave laser to produce lateral crystallization thin film transistors [2.1]. They fabricated polycrystalline silicon thin film with grain size larger than 5 μm and the thin film transistors with an electron mobility of 566 cm^2/Vs and a hole mobility of 200 cm^2/Vs. Solid phase crystallization is a common method to transform amorphous silicon (a-Si) to polycrystalline silicon (poly-Si). Usually, it is performed by furnace annealing at around 600℃ or rapid-thermal annealing (RTA) system. Ni is a kind of metal used by metal induced crystallization. The low formation temperature of Ni silicide is one of the benefits to fabricate thin film transistors. The mismatch lattice constant between Ni silicide (5.406 Å) and Si (5.430 Å) and $NiSi_2$ being nuclei for crystallization of amorphous silicon are the mechanism of silicide-mediated crystallization (SMC). Additionally, there are some special methods which can make single grain or few grains in channel region, such as Jae-Hong Jeon proposed [2.2] one and sequential lateral solidification one [2.3].

The devices used in current-voltage analysis were fabricated by novel process with or without main grain boundaries in the channel and were with various dimensions described lately. Briefly, we have two kinds of samples made by different process. They all have lightly doped drain ones and standard ones but the devices fabricated by special process additionally have samples with and without grain boundaries in the channel.

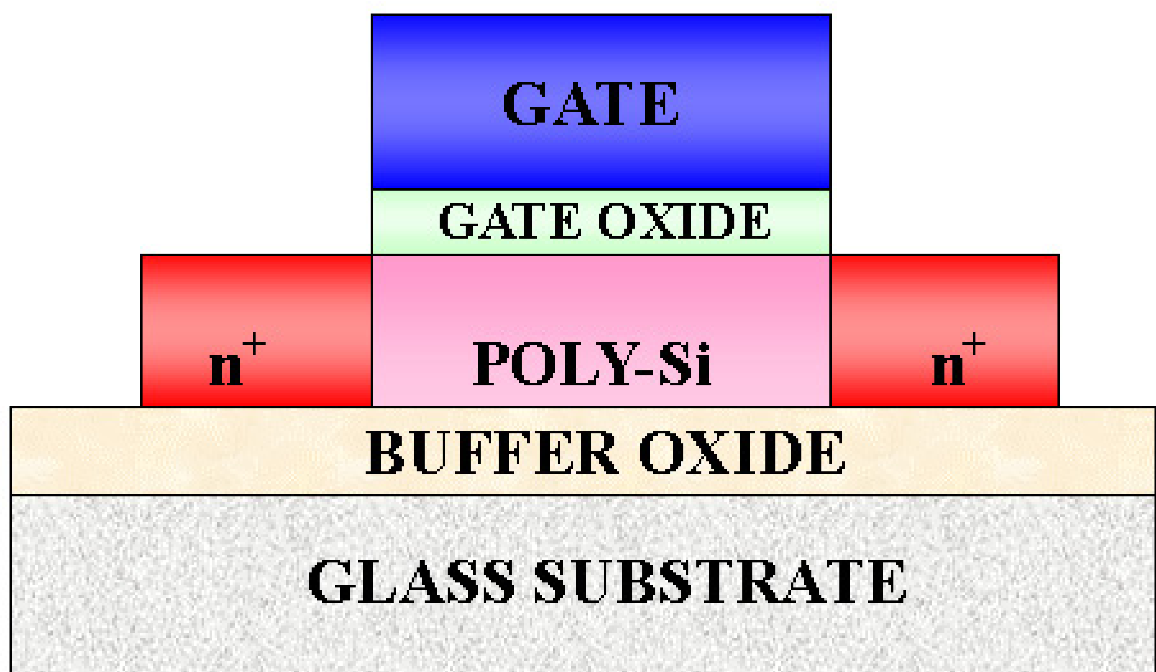

Fig. 2-1 the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain

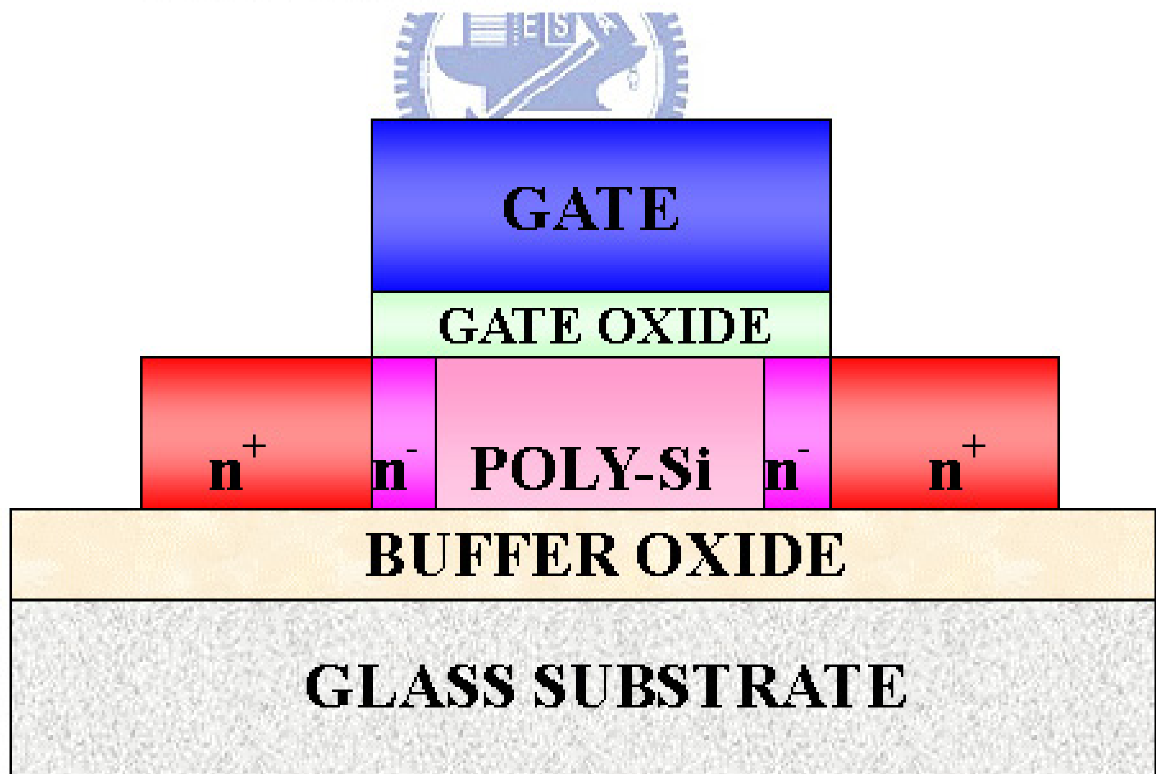

Fig. 2-2 the top-gate structure of low temperature polycrystalline silicon thin film transistor with lightly doped drain