2.2 Set Up Instruments

2.2.1 Stress Setup

In the study, the stress setup is shown as Fig. 2-3. To simplify our analysis of dynamic stress, the gate was connected to the pulse generator while the source and the drain were grounded. The pulse generator used in the study was HP4156 and the devices including the devices made by ELA and novel process with and without lightly doped drain. The stress waveform is shown in Fig. 2.4. The parameters of the waveform are defined as follow:

$$t_{period} = t_{base\text{-}width} + t_{leading} + t_{peak\text{-}width} + t_{trailing} \quad (2.1)$$

$$f = 1/\, t_{period} \quad (2.2)$$

$$D.R. = (\, t_{leading} + t_{peak\text{-}width}\,) / \, t_{period} \quad (2.3)$$

Where t_{period}, f, and $D.R.$ are the waveform period, frequency, and duty ratio, respectively.

According to Fig. 2-4, base is defined, as the base voltage of the waveform and peak is the peak voltage. Moreover, the base-width and peak-width are the duration of the base voltage and the peak voltage. The leading (rising) and trailing (falling) mean the leading time and trailing, respectively. Furthermore, the period of the waveform defined as (2.1) is the sum of base-width, leading, peak-width, and trailing. The frequency shown in (2.2) is equal to $1/\, t_{period}$. Most of our stress condition is that base equals –10 V, peak equals +10V, and the frequency of waveform is applied to 500 KHz.

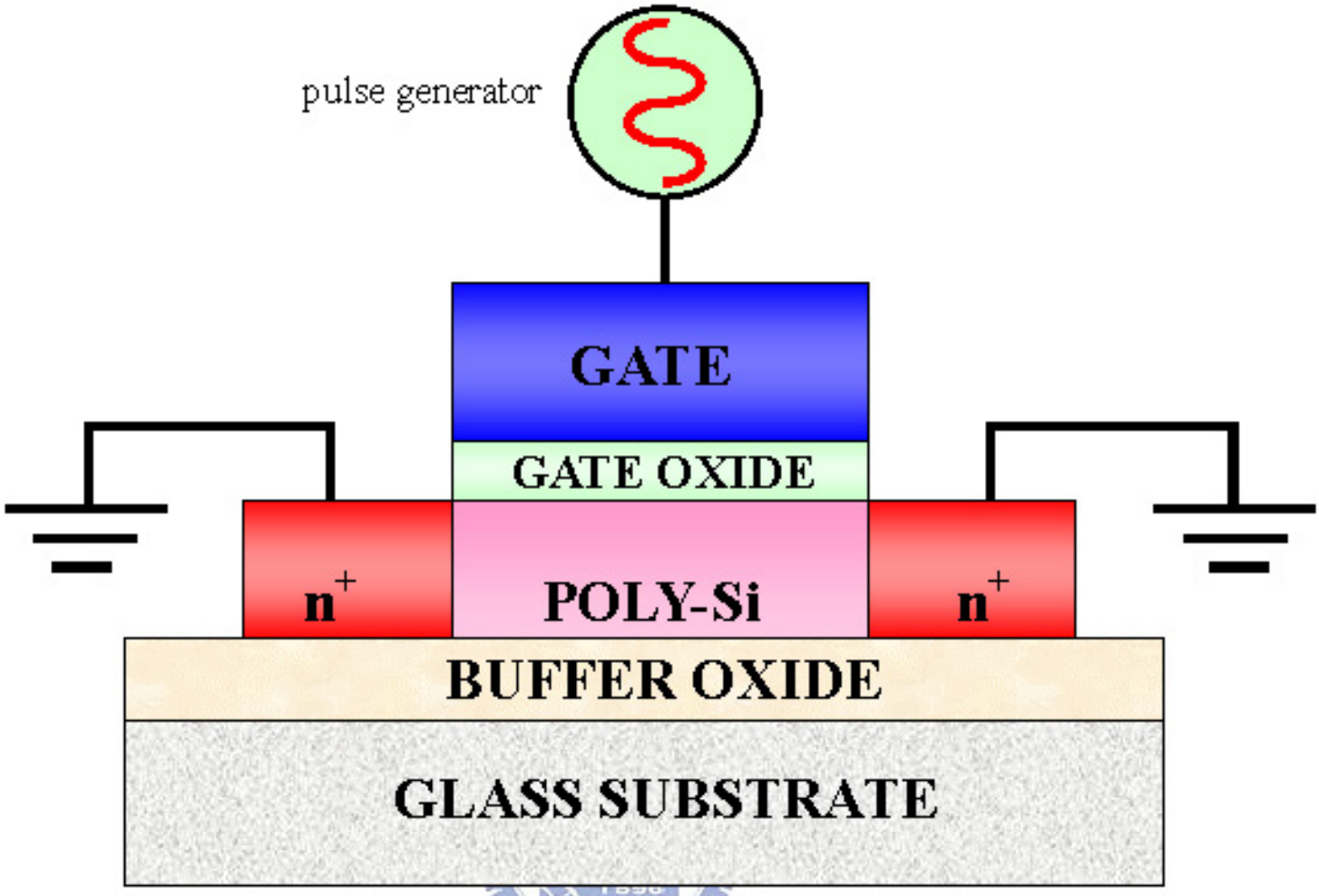

Fig. 2-3 the stress setup of the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain (LDD)

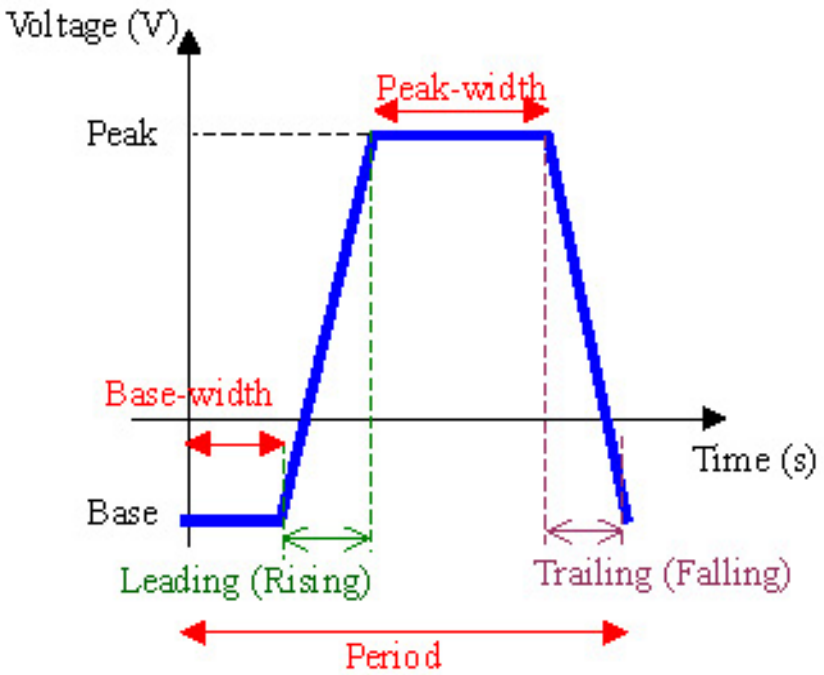

Fig. 2-4 the waveform of the stress setup

2.2.2 Current-Voltage (I-V) Measurement

The current-voltage (I-V) measurement is illustrated in Fig. 2-5. The instrument used here was HP4156 semiconductor parameter analyzer. The current-voltage measurement in the thin film transistor (TFT) is alike to that in the metal-oxide-silicon field effect transistor (MOSFET). To obtain the transfer characteristic, the drain was given by a constant voltage, and the gate voltage was set to sweep while the source was grounded. Simultaneously, we measured the drain current and the gate voltage. To get the output characteristic, the source was grounded; at the same time, the drain and the gate were applied by the sweep voltage and a constant voltage, respectively. Similarly, we measured the drain current and the drain voltage.

The thin film transistors used in the study were fabricated by the conventional ELA process and the novel process. Both of the two methods were consist of the devices with and without lightly doped drain (LDD). However, the thin film transistors made by the novel process were noticed in particular. The main grain boundaries may be existed in the channel region of the top-gate polycrystalline silicon thin film transistors fabricated by the novel process. Therefore, these devices were degraded not only in the source/drain junction but also the on the main grain boundaries.

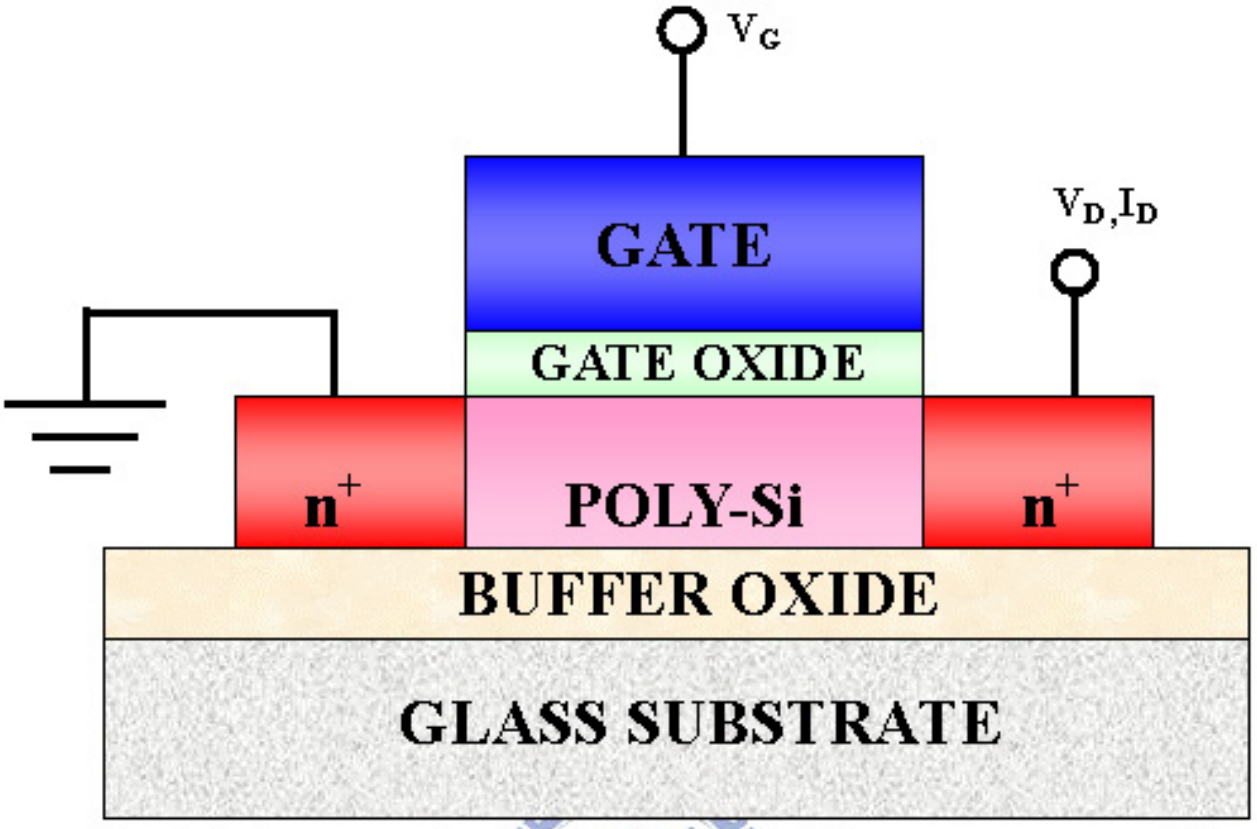

Fig. 2-5 the current-voltage (I-V) measurement of the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain(LDD)

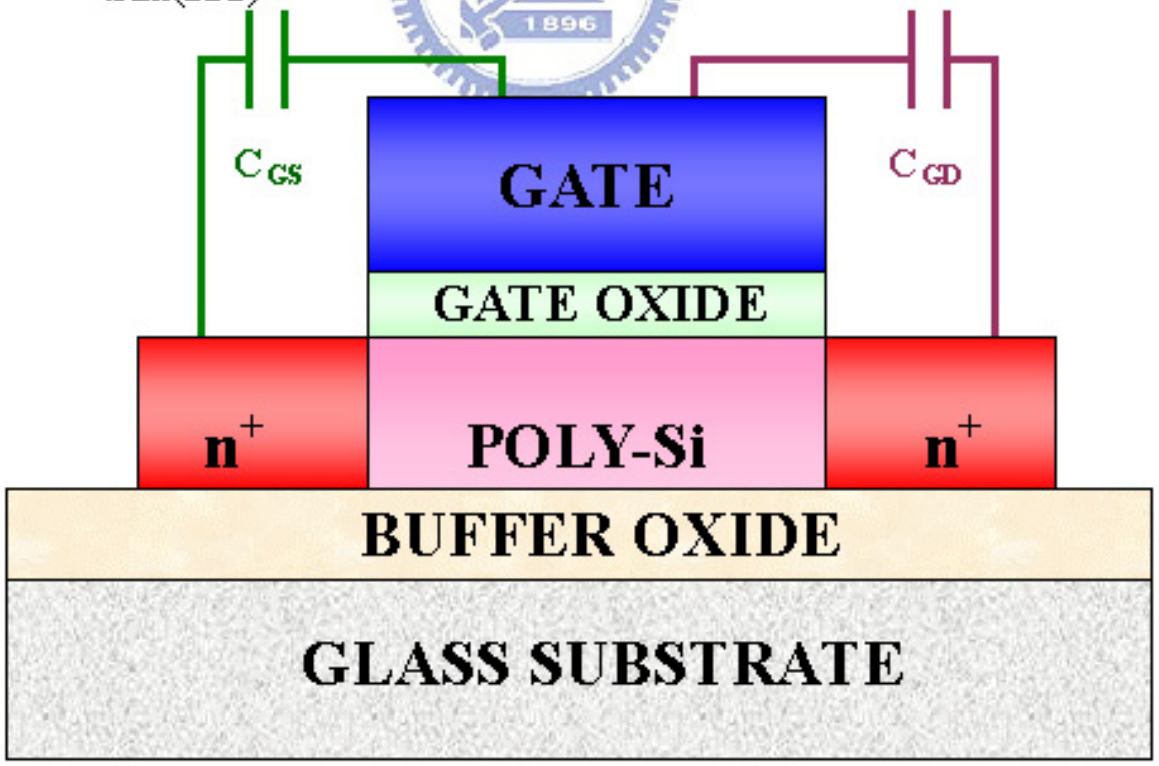

Fig. 2-6 the capacitance-voltage (C-V) measurement of the top-gate structure of low temperature polycrystalline silicon thin film transistor without lightly doped drain(LDD)

2.2.3 Set Up Instruments for Capacitance-Voltage (C-V) Measurement

The set up for capacitance-voltage measurement is shown in Fig. 2-6. Compared with the capacitance-voltage method used in metal-oxide-semiconductor field effect transistors (MOSFETs), the measurement in low temperature polycrystalline silicon thin film transistors (LTPS) was unable to contact the gate and the body so that it was difficult to measure the gate-body capacitance in a traditional top-gate polycrystalline thin film transistor. However in a conventional metal-oxide-semiconductor field effect transistor, it is able to contact the gate and the body electrode to such an extent that it is convenient to measure the gate-body capacitance. Therefore, we measured the gate-drain and the gate-source capacitances, respectively. The gate-drain capacitance (C_{GD}) was measured and at the same time the source was floating while the gate-source capacitance (C_{GS}) was measured with floating drain.

In this thesis, the dimensions of the top-gate low temperature polycrystalline silicon thin film transistors were 30 μm in width and 30 μm in length. The polycrystalline silicon film was formed from amorphous silicon crystallized by XeCl excimer-laser (308 nm wavelength) and with the 350 mJ/cm^2 power of line-shaped beam. Besides, the gate oxide was 100 nm thick and the amorphous silicon film was 50 nm thick; both of them were deposited by plasma enhanced chemical vapor deposition (PECVD). The instrument used to perform the capacitance-voltage measurement was HP4284, which was able to change various measurement frequencies. When measuring the polycrystalline silicon thin film transistors, it was applied various frequencies from 10 KHz to 1MHz in order to investigate the degradation mechanism after dynamic stress.