Chapter 1

Introduction

1.1 Development of X-ray Sensor

Conventional X-ray imaging remains a largely analog technology. Digital X-rays or digital radiology [1] (see figure 1.1-1) would be advantageous because it would permit image processing to improve aspects of image quality such as image contrast; make it easier to compare radiological images with those obtained from other imaging modalities; permit image networking within the hospital for remote access and archiving; facilitate the work of radiologists by making computer-aided diagnosis [2] possible; and permit teleradiology wherein highly qualified personnel could service remote or poorly populated regions from a central facility [3]. A large area detector is essential in medical radiology since the lack of a practical means to focus X-rays necessitates a shadow image which is larger than the body part to be imaged [4]. There are currently two major commercial approaches to digital radiography—the digitization of a signal from a video camera optically coupled to an X-ray image [5] intensifier which is very bulky, and the stimulable phosphor system [6]. Both systems are available in forms which permit instant readout although the most usual form of the stimulable phosphor system requires carrying the cassette to a laser scanner for readout. However neither system has an image quality which makes it acceptable for all uses. In contrast, there are emerging digital detectors which could perform all current radiological modalities—radiography (including rapid sequence radiography) and the real-time imaging modality—fluoroscopy. The detector would be a large area, flat panel which could easily fit into the conventional Bucky tray of any X-ray room. It would employ a layer (or layers) to

absorb X-rays and convert their energy to charge, and an active matrix array (a very large area integrated circuit) for self-scanned (i.e., in situ) readout of the charge image. There are two possible approaches. The direct method uses a photoconductor to directly convert X-rays to charge in contrast with the indirect method using photodiodes and a phosphor layer [7]. The basic concept of a direct readout active matrix detectors is shown in figure 1.1-2. During X-ray exposure, energy is absorbed by the photoconductor layer (e.g.,amorphous selenium) and the charge created is drawn to the surfaces by the internal electric field. The image charge is collected by the pixel electrode and accumulated onto the pixel capacitance(i.e., self-capacitance and integrated storage capacitor). The pixel electrode and storage capacitor are connected to the TFT switch of each pixel. During readout, the scanning control circuit generates pulses to turn on all the TFT switches on the first row of the array and transfers charge from the pixel capacitors to the readout rails (columns). The charge is then collected and amplified by an amplifier on each rail and the data for the entire row is multiplexed out. This sequence is repeated for each subsequent row until the entire array is read out. The indirect method, shown in figure 1.1-3, is an alternative X-ray imaging detector concept based on active matrix arrays. In the indirect method a phosphor screen is used to absorb X-rays and the resultant light photons are detected by an active matrix array with a single photodiode and TFT switch at each pixel [8]–[11]. In this thesis, we use indirect-type flat panel detector with the p-i-n photodiode.

In addition to X-ray image system, this active matrix sensor (AMS) technology is becoming very attractive in a range of different applications such as digital lensless cameras, [12]. In AMS application, a system is required to read out the information sensed at each pixel location. This thesis focuses on the readout circuitry of large area X-ray sensors used in diagnostic medical imaging such as radiography and mammography (static medical imaging) and fluoroscopy (dynamic imaging). The new AMS technology has the potential to fully replace film based analog technology and to make the system instantly available for use and diagnostic

by radiologist.

In these applications, the active matrix is based on a 2-dimensional array of amorphous silicon (a-Si) or polycrystalline silicon (poly-Si) pixels. The basic elements of each pixel are the X-ray detector and the thin film transistor (TFT). Pixel signals are read out using analog circuitry. Conventional designs use single crystal ICs externally connected to the matrix sensor for reading the stored information. These external connections are often the reason for sensor malfunction (loss of signal or increase of noise). Furthermore they increase the cost of the panel.

1.2. LTPS TFTs

In order to improve the sensor resolution and integrate system for reducing the final system cost, integration of some (if not all) of the readout circuitry on the glass itself is needed. This is only possible in either a-Si or poly-Si technology, as single crystal Si (c-Si) cannot be deposited onto glass. Poly-Si technology has superior properties compared to a- Si, which has a very low field effect mobility and requires larger driving voltages, and is therefore more suitable for this application.

One of the most promising approaches is to use excimer laser to recrystallize amorphous silicon (a-Si), the poly-Si TFTs can have very high performance. However, the resulting poly-Si TFTs have poor uniformity and suffer from huge variations due to the narrow laser process window for producing large-grained poly-Si thin film. The fluctuation of pulse-to-pulse laser energy and non-uniform laser beam profile make laser energy density hard to hit the super lateral growth regime everywhere. The random grain boundaries and traps exist in the channel region [13]. This will lead to many problems in real product applications such as output variation in analogue circuit, and thus non-uniform brightness in panel. Since the device-to-device uniformity is difficult to control, it would be essential to develop circuits to

compensate the variation.

1.3. Integrated Circuit of System on Panel

Poly-Si TFT displays with integrated driving circuits have recently been developed. At present, the poly-Si TFT is the best candidate to realize system on panel and is widely considered for active matrix LCDs and active matrix OLEDs. However, for X-ray read out circuits such as analogue switches and double sample and hold are integrated only partially.

Until now, these attempts appear to be unsuccessful in the display application due to the problems in poly-Si TFTs. Especially, the poly-Si TFT suffers from significant variation in the threshold voltage due to the nature of the polysilicon crystal growth and represents different electrical characteristics with their locations in panel. The threshold voltage variation could even as large as 1V in some high performance TFT devices across a large substrate area. This results in the output non-uniformity in analogue circuits such as charge sensitive amplifier (CSA) and analogue buffers over the whole panel.

The readout of a capacitive sensor involves the conversion of the sensor capacitance or its changes to an electrical signal such as voltage, current or frequency. This paper presents a (CSA) that is used to convert the charge in sensor capacitance to voltage. The function of the analogue buffer in the data driver is to act as a buffer to drive the load capacitance of the data bus in the panel. To implement CSA circuit with poly-Si devices, several critical issues must be considered, such as output voltage accuracy, layout area and power consumption, and so on. Thus, it is necessary to develop a CSA which not only has high immunity to the variation of poly-Si TFT characteristics but also a very simple configuration for high resolution detector.

The circuit design has to take into account the fact that adjacent transistors may not be closely matched [14] and some schemes for the cancellation of the mismatch effect (such as offset) should be applied. In previously study, correlated double sampling (CDS) poly-Si

circuit was presented. In addition, X-ray readout systems should have a CSA between the pixel array and CDS to enlarge the signal to noise ratio. In this thesis, a CSA poly-Si TFT circuit that can be used for readout electronic system in active matrix X-ray sensors is proposed.

The proposed X-ray read out circuit has not only high immunity to the variation of poly-Si TFT characteristics but also a simple configuration for high-resolution image system.

1.4 Thesis organization

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Figure caption – Chapter1

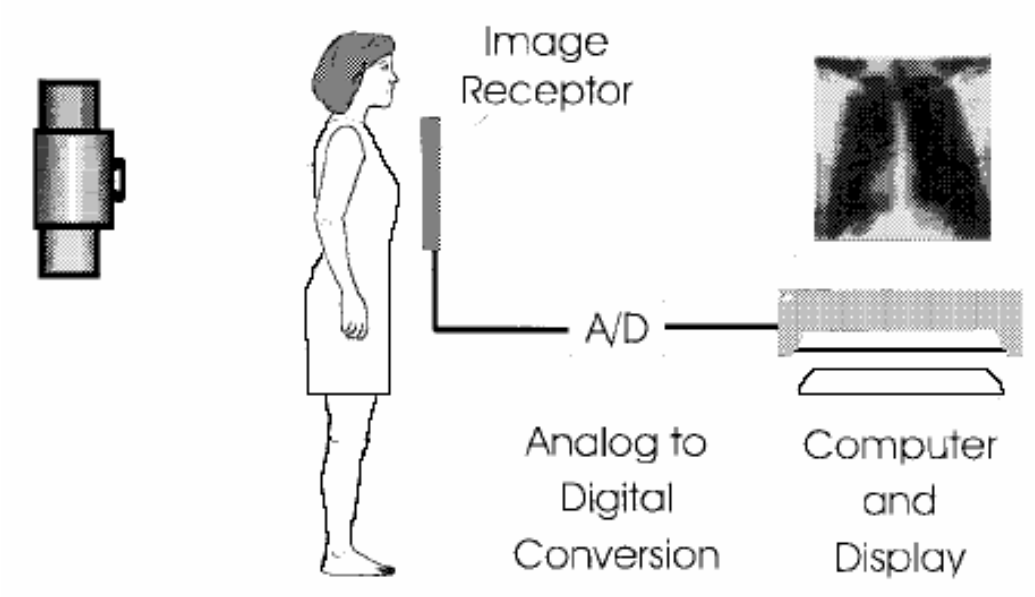


Fig. 1.1-1. Concept of digital X-ray imaging.

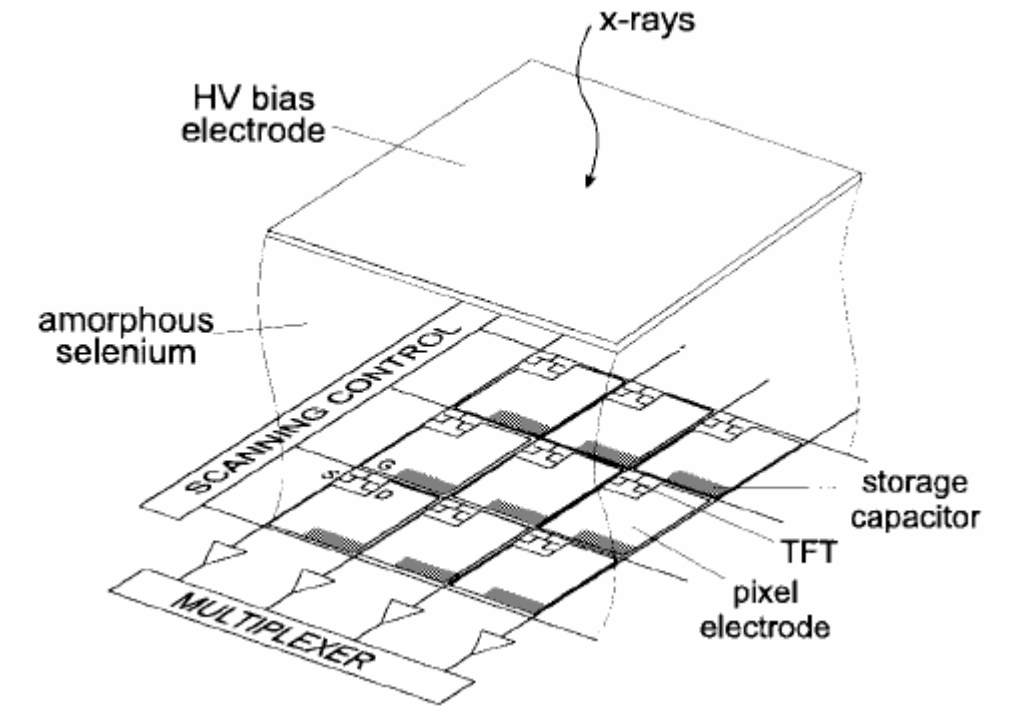


Fig. 1.1-2. Large area flat panel system for digital radiography and fluoroscopy based on direct conversion active matrix readout system using a photoconductor.

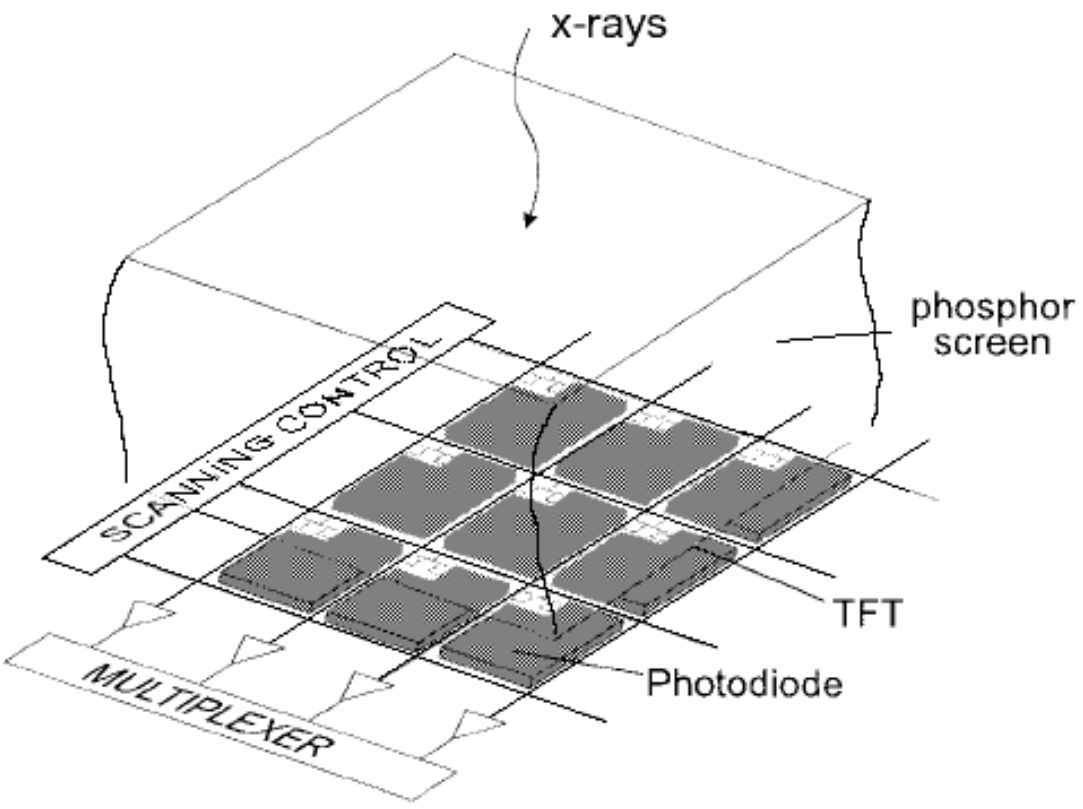


Fig. 1.1-3. Large area flat panel system for digital radiography and fluoroscopy based on indirect conversion active matrix readout system using a powder phosphor screen or structured CsI phosphor layer.

Chapter 2

System Architecture

2.1 Introduction

The active matrix sensor (AMS) block diagram is shown in figure 2.1-1. The core pixel array consists of photodiode active pixels are accessed in the row-wise fashion using the scan driver. The X-ray signal is transformed by the photodiode and stored in the charge domain. All pixel charges in the row are read out into column analog readout circuits in parallel. Because of high resolution and fine pixel, the multiplexer is used to reduce bus number and increase pitch. The charge sensitive amplifier (CSA) provides a fixed gain for the column charges being read in the voltage domain using the column select logic. Each of the column-parallel readout circuits performs correlated double sampling (CDS) functions [12] to eliminate pixel offset variations and pixel noise. The analog-to-digital converter (ADC) generates the digital output according to the amplified signal for the consequent processing and storage.

In this thesis, the simulation is based on an p-i-n type of photodiode [15], whose cross-section view and simple equivalent circuit in pixel are shown in figure 2.1-2(a) and 2.1-2(b), respectively. For this kind of p-i-n photodiode stacked with a SiNx dielectric capacitor layer, the corresponding detector capacitor Cd is about 10 pF. The sensitivity of the X-ray sensor is assumed to be 1-3 (μCoul/cm2·R). For a usual exposure dose of 100-600 (mR/s) and exposure time of 40 ms to 200 ms, the injection of charge signal could be several picocoulombs.

The CSA provides a fixed transform for the column charges to the voltage signal being read using the column select logic. The detail operation amplifier circuit of CSA would be discussed

in chapter 3. The pure pixel signal voltage is then delivered to ADC. Since the output signal is amplified and the pitch is enlarged after CSA, CDS and ADC could use ICs externally connected, but might not necessarily integrate onto glass substrate with LTPS TFTs.

2.2 Analog Multiplexer

The analog multiplexer has three main function : (1) to preprocess the signal coming from the sensors or to guide the signal coming from the sensors to the appropriate signal processing units, (2) to multiplex the incoming signal in time domain, and (3) to build the system by applying some simple concepts of micro-electronic circuit. The analog multiplexer also must send the signal out with no distortion to the processing units, must minimize the complexity of the circuit, must be cost effective. The analog multiplexer is important not only for sensor detection, but also for image processing, face recognition, and electronic military and civilian application.

A 4:1 multiplexer (MUX) can be used to reduce the readout circuit required and enlarge their layout pitch. This multiplexer is made of transistors MN1 to MN4 as the main switches to select the four inputs and shown in figure 2.2-1. When high signal is applied to the n-type TFT gate, the switch will close and input signal is able to transmit through. Besides, transistors MN5 to MN12 are the “dummy” switches for the charge injection cancellation [16].

Figure 2.2-2 and figure 2.2-3 show the gate signal of main switches and the simulation result of mux output signal while the four input voltage of multiplexer are 6V, 6.5V, 7V, 7.5V. It is obvious that when the main switch turns on, the input signal transmits to the output accurately.

2.3 Charge Sensitive Amplifier

2.3.1 Conventional charge sensitive amplifier architecture and its read out operating principles

The CSA provides a fixed transform for the column charges to the voltage signal being read using the column select logic. Referring to figure 2.3-1, the conventional process of reading the charge information from the detector capacitance Cd to CSA voltage output is conducted in the following way:

In the initialization period, the charge previously stored on Cd should be released. When the switching TFT turns on, Vref is set at low voltage so that the photodiode is in forward bias and thus the pixel voltage Vc discharges toward V_L till a difference of photodiode threshold voltage is reached.

After initialization, sensors in the whole matrix are exposed to X-rays and the charges corresponding to the X-ray image are stored on Cd in pixels respectively. During this period, Vref turns to high voltage V_H and thus the p-i-n diode is reverse-biased for the pile-up of the sensed charge from the photodiode. After exposure, all the switching TFTs are turned off to isolated the pixel charge from CSA and the charges are held. In the readout period, the switching TFTs are turned on row-by-row to read out the charge information from the matrix. Before each row-wise readout operation, the CSA is reset by turning on the reset TFT. Then, Vref goes back to V_L and the photodiodes are in forward bias again. Therefore, the stored charges in a row are transferred from Cd onto the CSA feedback capacitance (Cf), resulting in the output voltage Vo.

The detector capacitance Cd and the feedback capacitance Cf selected as 10pF and 2pF, respectively, which provides a gain of -5. As an example, for an X-ray generated charge of 2pC stored on Cd, the input signal Vin for the CSA will be 0.2V. It corresponds to the CSA output

signal of -1V, which will be added to the reference voltage Vref of 7V. Thus, the ideal output voltage of CSA should be 6V.

2.3.2 Proposed charge sensitive amplifier architecture

For such a conventional CSA configuration to be adapted in poly-Si TFT circuit, it suffers from the high supply voltage of the amplifier which may lead to more power consumption and TFT device degradation. Therefore, a path selecting circuit as shown in the figure 2.3-1(c) is inserted before the input of CSA. It requires two additional switches and one voltage source V_H to supply reverse-bias voltage of diode at appropriate time. Thus, Vref can be fixed at V_L and the supply voltage could be reduced.

2.4 Correlated double sampling

Correlated double sampling (CDS) is a widespread noise reduction method for discrete-time output signals. Its application is indispensable as a front end for a capacitive sensor, such as an accelerometer, a pressure sensor and the most common, image sensors. The basic intention of CDS has been the elimination of the offset noise and the reduction of 1/f noise generated in the front-end amplifier [12]. The use of CDS integrator often requires voltage sampling at two or more different time points and records the differences. As a result, the effectiveness of the CDS technique is strongly influenced by the available voltage swing. With the significant reduction of power supply voltage in advanced CMOS processes, the application of CDS demands the use of A/D converters with resolution of several mV.

The CDS schematic is shown in figure 2.4-1 and the operation include two steps. At the first

step, signal retaining information about offset, background noise and reset noise is stored on one sampling capacitor Cs1. At the second step, the voltage which contains both the pixel signal, as well as the noise and offset components common to both sampling step and stored onto the other capacitor Cs2. The differential amplifier subtracts these two sampled signal eliminating common noise components from the pixel information signal.

A. Rankov propose a CDS poly-Si circuit for readout systems in large area X-ray sensors shown in Fig.2.4-2 [12]. This circuit is based on a current mirror structure, which produces the differential signal (free from above mentioned noise and offset) at the output (out2) that can then be sampled and sent to the ADC through the multiplexing column switch (Smux). The transistors M1 and M2 are of the same size, as are M3 and M4, M1c and M2c, M3c and M4c.

The operation of Rankov's circuit is based on the charge conservation law applied to nodes 2 and 4 and can be expressed by:

$$V(2)_1 + \frac{C_{s1}}{C_{t1}} \cdot (V_{in2} - V_{in1}) = V(4)_1 + \frac{C_{s2}}{C_{t2}} \cdot (V(3)_2 - V(3)_1) + \frac{C_{gd2}}{C_{t2}} \cdot (V(40)_2 - V(40)_1) + V_{offset} \quad (1)$$

Subscripts '1' and '2' are used to refer to phases φ1 and φ2 respectively. It follows from here that $V(2)_1 = Vr_1$, $V(3)_1 = V_b$ and $V(3)_2 = V(out2)$. Voltage V_{in1} is the input signal during phase φ1 representing noise and offset. Voltage V_{in2} is the input signal during the phase φ2 representing the information signal plus the noise and offset. Capacitances C_{t1} and C_{t2} are the total capacitances seen by the gates of M1 and M2, whilst C_{gd2} is gate-to-drain capacitance of M2. After re-arranging (1) and inserting the voltage values given above the output voltage of the differential amplifier V(out2) is:

$$V(out2) = \underbrace{\frac{C_{t2}}{C_{s2}} \cdot (V_{r1} - V(4)_1 - V_{offset})}_{a} + \underbrace{\frac{C_{s1} \cdot C_{t2}}{C_{t1} \cdot C_{s2}} \cdot (V_{in2} - V_{in1})}_{b} + \underbrace{V_b}_{c} - \underbrace{\frac{C_{gd2}}{C_{s2}} \cdot (V(40)_2 - V(40)_1)}_{d} \quad (2)$$

The offset term V_{offset} appears due to the mismatch of technological parameters of ideally

identical transistors. The most important contribution to this term in polysilicon technology is due to the mismatch between the threshold voltages of the devices. If other sources of mismatch are ignored, this term can be approximated by (3), where V_{thi} is the threshold voltage of transistor Mi for i =1,2,3,4.

$$V_{offset} = (V_{th2} - V_{th1}) + \sqrt{\frac{\beta_4}{\beta_2}} \cdot (|V_{th3}| - |V_{th4}|) \quad (3)$$

During the phase φ1 the transistors are connected in such a way that the difference (V_{r1}-$V(4)_1$) will sense this offset and hence will cancel out the term 'a' in (2). Cascode transistors have been added to the circuit in order to make the offset cancellation strategy more robust. Without them the term 'd' in (2) would modify the gain (in such a case: $V(40)_2$ = $V(4)_2$ =V(out2)) due to the gate-to-drain parasitic coupling and there would also be a remaining offset.

Besides, the cascode transistor reduces the voltage variation in node 40 for different operating points at the gate and can therefore be assumed that $V(40)_2 \approx V(40)_1$. With all these considerations and also taking into account the fact that the total capacitances seen by the gates of transistors M1 and M2 differ very little from the values of the input capacitances, equation (2) simplifies and the output voltage is:

$$V(out2) = (V_{in2} - V_{in1}) + V_b \quad (4)$$

The simulation results observed change in output voltage is ΔV(out2) =±0.09V.

2.5 Analog to digital converter

The ADC is ideally suited to pixel-level implementation in a CMOS image sensor. Note that an ADC maps an analog signal S into a digital representation (codeword) according to a

quantization table. A 3-bit Gray coded example is given in Table I, where S is assumed to take on values in the unit interval (0, 1]. The table lists the assignment of each input range to a 3-bit codeword. The observation is that we can generate each bit of the codeword independently. For example, consider the generation of the least significant bit (LSB). From the table, the LSB is a one when $S \in (1/8, 3/8] \cup (5/8, 7/8]$ and a zero otherwise. To generate the LSB, any bit-serial Nyquist-rate ADC must be able to answer the following question: Is $S \in (1/8, 3/8] \cup (5/8, 7/8]$? Thus, the ADC is essentially a one-detector that indicates the input ranges resulting in a one. The most natural way to implement this quantization table is to use a flash ADC. Figure 2.5-1 depicts a 3-bit gray-code flash ADC in which each bit of the codeword is independently generated. The most significant bit (MSB) is generated y comparing with a value of 1/2, whereas the LSB is generated by comparing with

1/8, 3/8, 5/8, and 7/8. Note that to generate the LSB, four clocked comparators and some decoding logic, which converts thermometer code into gray code, are needed. This makes the flash ADC too large to fit in a pixel. Interestingly, a 1-bit comparator and a 1-bit latch can perform the same function as the seven clocked comparators in the flash ADC in a bit-serial fashion. The key to the operation is the judicious selection of the sequence of comparisons to be made.

A block diagram of a 1-bit comparator/latch pair is shown in figure. 2.5-2. The waveforms in the figure illustrate how a comparator/latch pair performs bit-serial ADC. The analog signal S is connected to the positive terminal of the comparator, and the signal RAMP, which is an increasing staircase waveform, is connected to the negative terminal. The output of the comparator feeds into the gate of the latch, and the digital signal BITX connects to the data terminal of the latch. The MSB can be generated in exactly the same manner as for the flash ADC by comparing S to a RAMP value of 1/2. To generate the LSB, which requires four comparators in a flash ADC, is more challenging. We need to compare S to all four values (1/8,

3/8, 5/8, 7/8) using a single comparator. To do so, RAMP starts at zero and monotonically steps through the boundary points (1/8, 3/8, 5/8, 7/8). At the same time, as shown in the figure, BITX starts a zero and changes whenever RAMP changes. As soon as RAMP exceeds S , the comparator flips, causing the latch to store the BITX value just after the RAMP changes. The stored value is the desired LSB. After the comparator flips, RAMP continues on, but since RAMP is monotonic, the comparator flips exactly once so that the latch keeps the desired value. For example, for input1, which is between 3/8 and 5/8, the comparator flips when RAMP steps to 5/8, which is just above the input1 value, and BITX also changes to zero. When the comparator output goes low, a zero, which is the desired LSB, is latched. After that, RAMP continues to increase and BITX continues to change. Since the latch is closed, however, BITX can no longer influence the output. After RAMP completes stepping through the boundary points, the latched output is read out. Then RAMP and BITX are reset to zero in preparation for another sequence of comparisons. In this fashion, all bits from MSB to LSB are generated. The next most significant bit (NMSB) is similarly generated by comparing input1 to 2/8 and to 6/8, which yields a one. This 3-bit example can be easily generalized to perform any m-bit ADC [17].

Figure caption – Chapter2

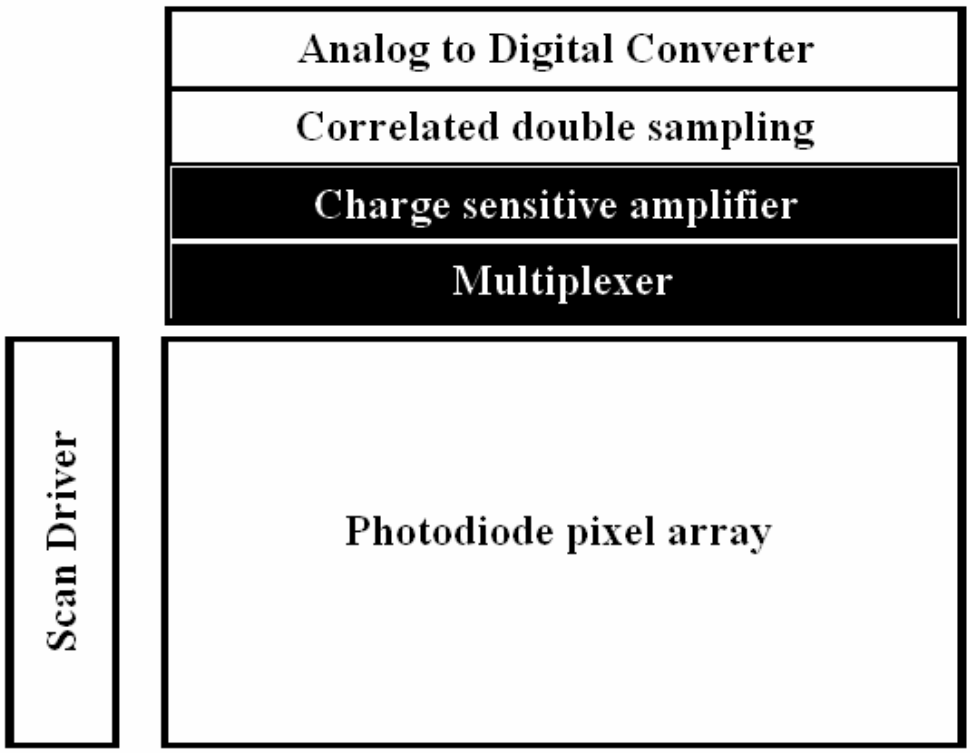


Fig 2.1-1 Active matrix sensor system block.

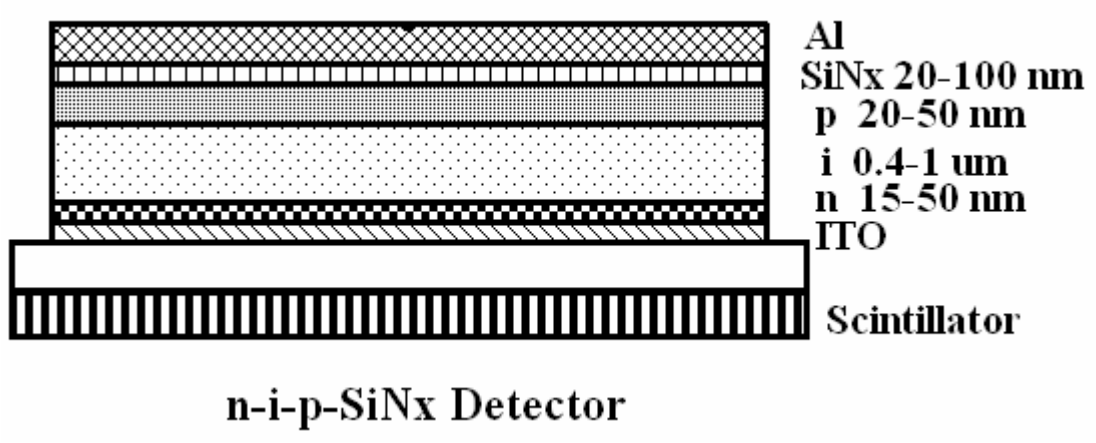
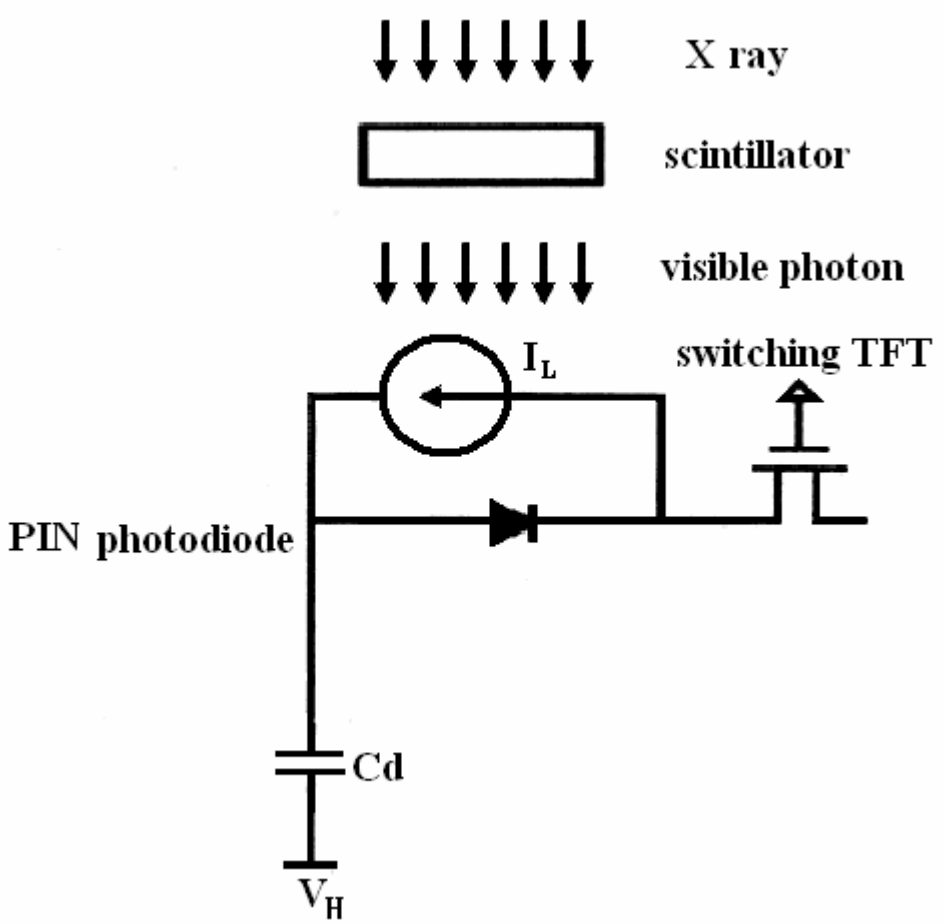


Fig 2.1-2 P-i-n photodiode (a) cross-section view.



(b) simple equivalent pixel circuit

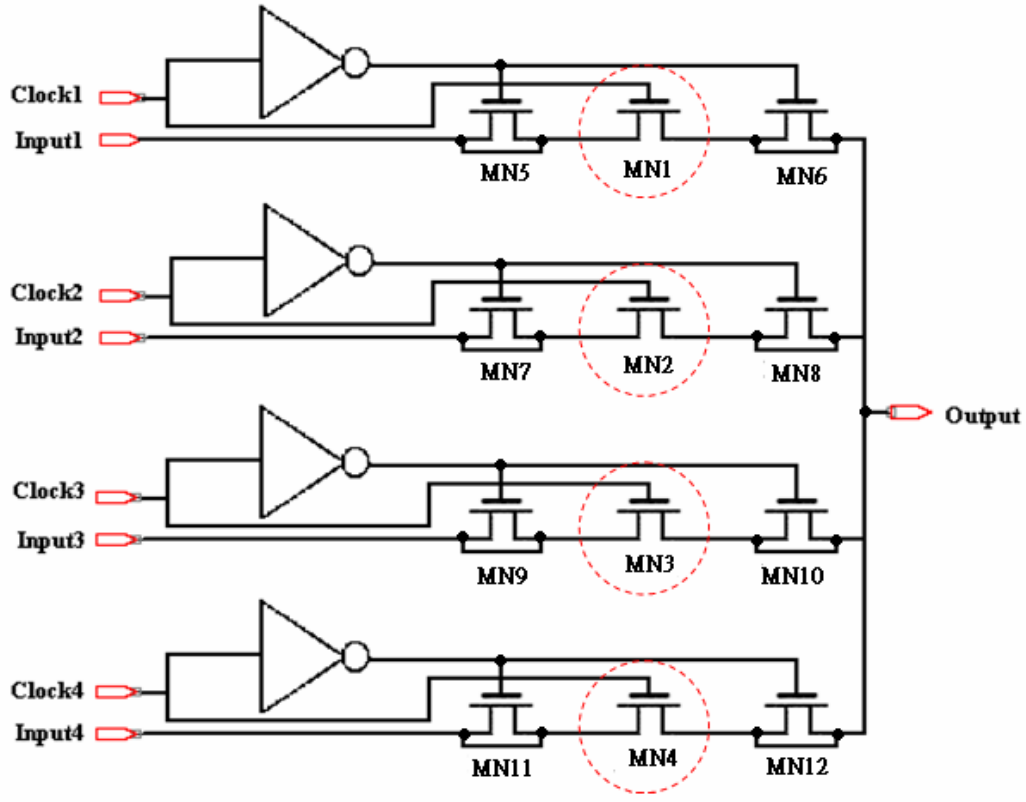


Fig 2.2-1　4:1 multiplexer with dummy TFTs

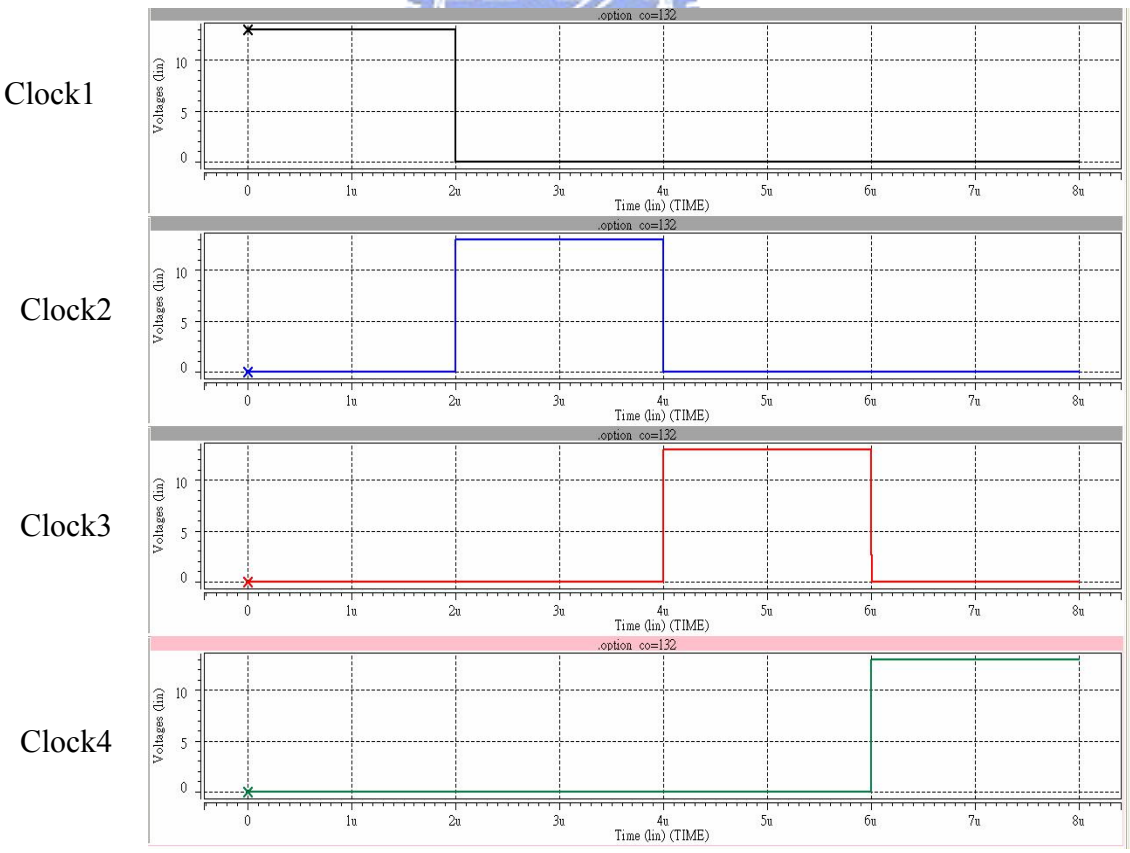


Fig 2.2-2　The gate signal of main switches

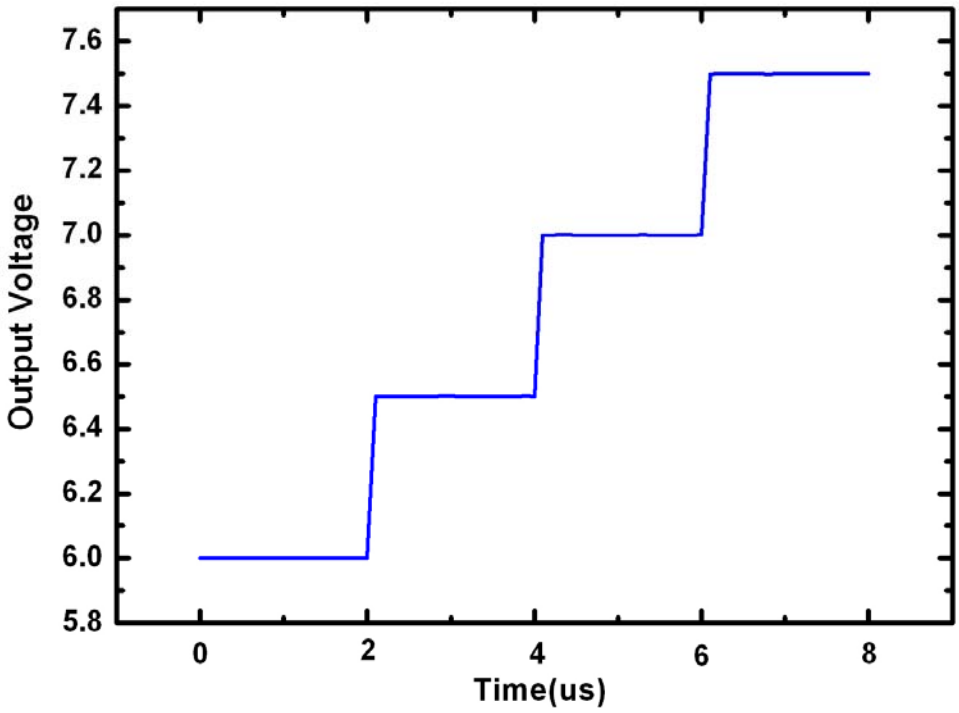


Fig 2.2-3 The simulation result of mux output signal while the four input voltage of multiplexer are 6V, 6.5V, 7V, 7.5V.

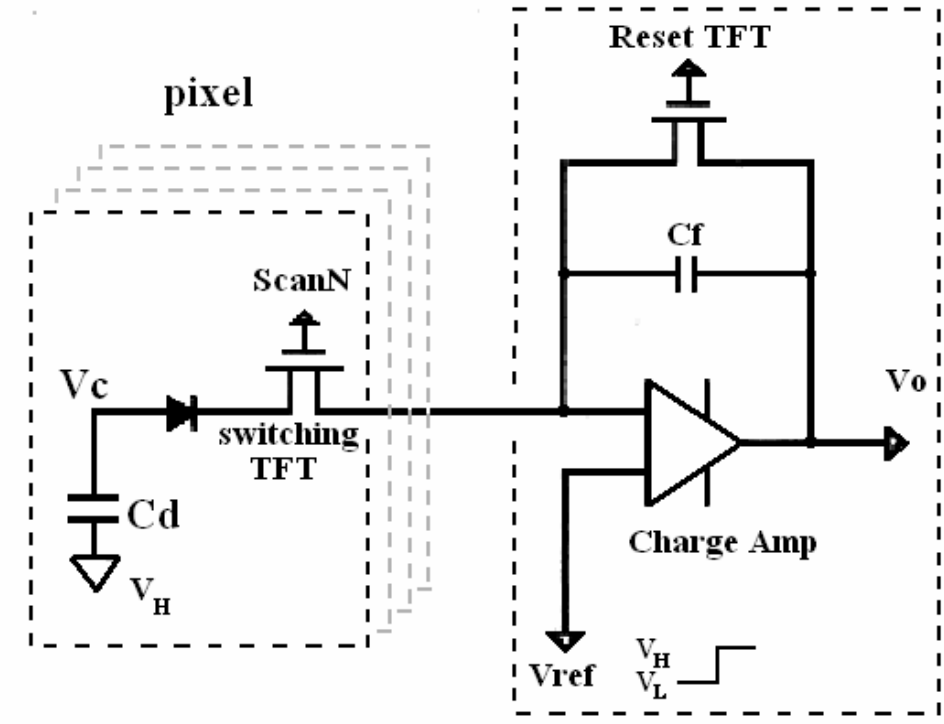
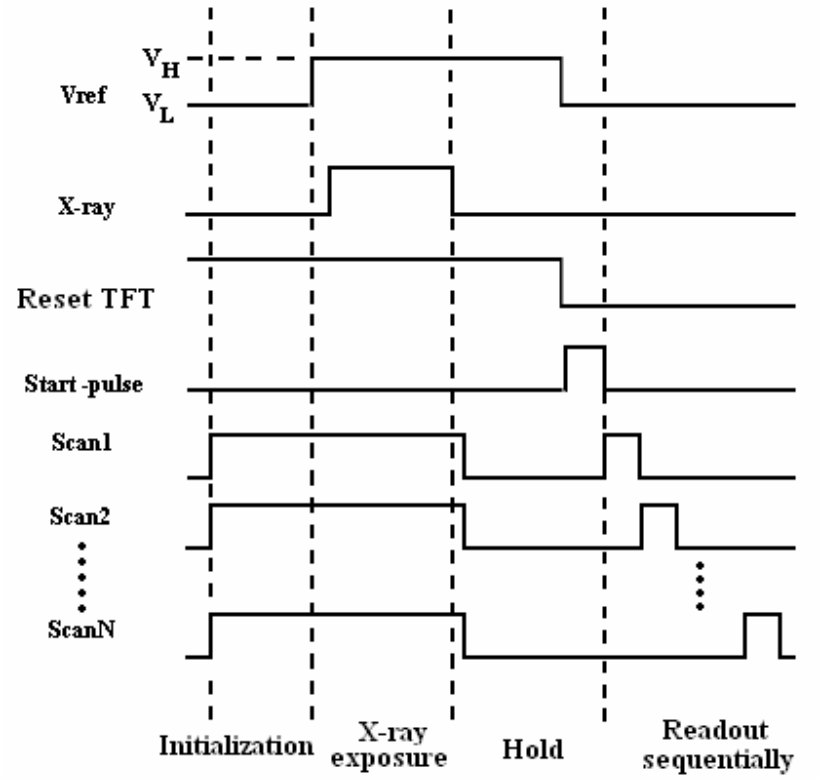
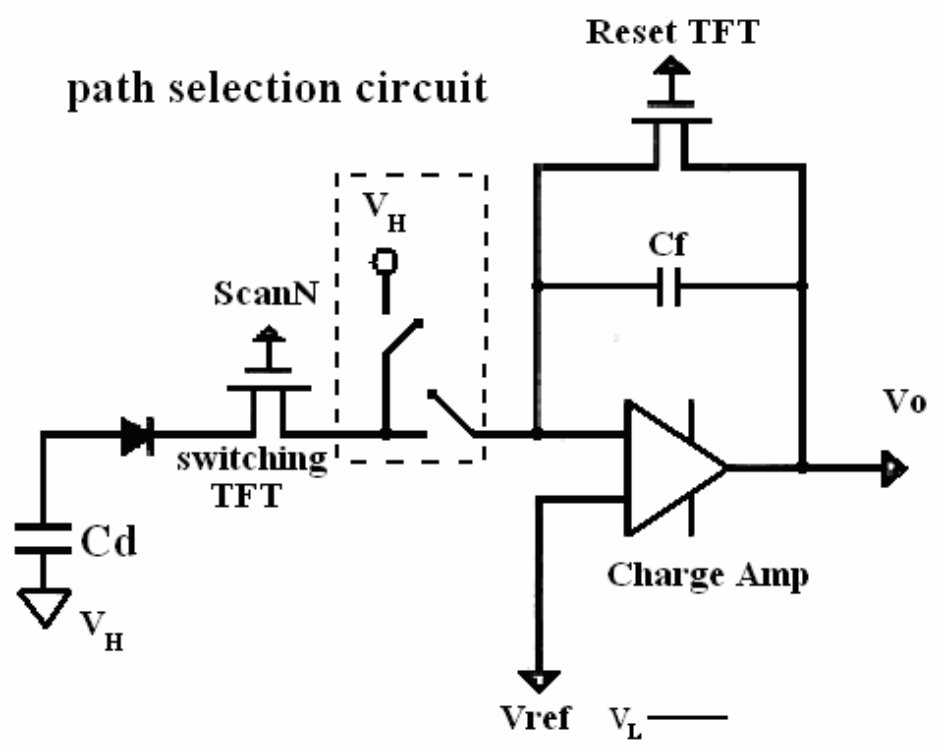


Fig 2.3-1 The readout operation of charge sensitive amplifier from a sensor pixel (a) conventional circuit.



(b) timing chart



(c) with path selection circuit.

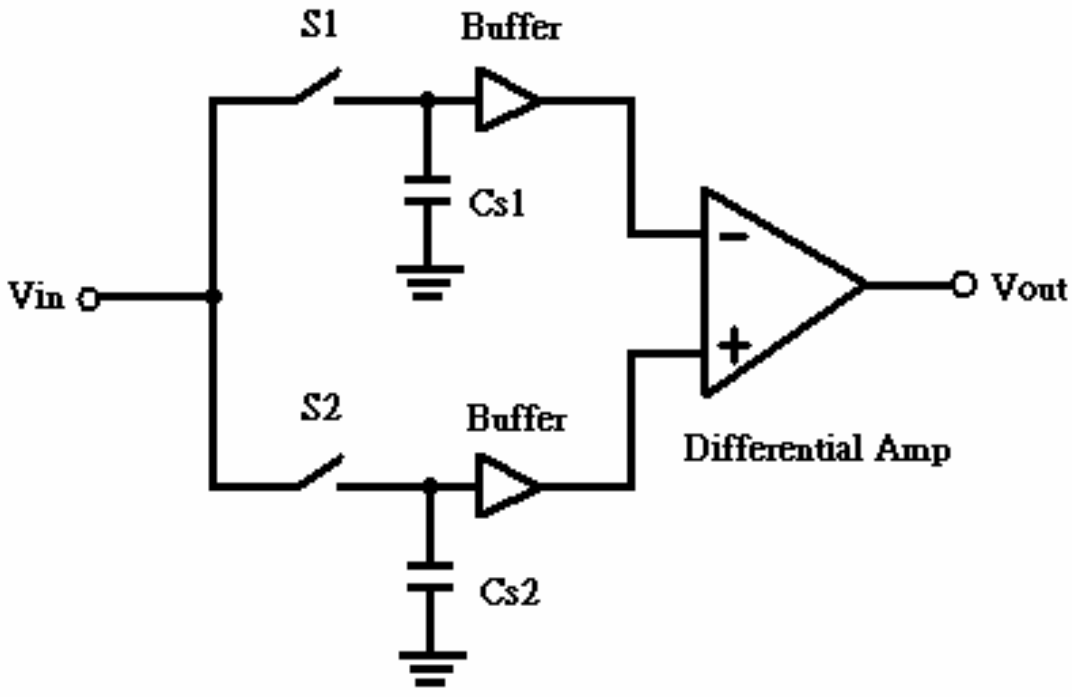


Fig 2.4-1 Schematic of correlated double sampling (CDS)

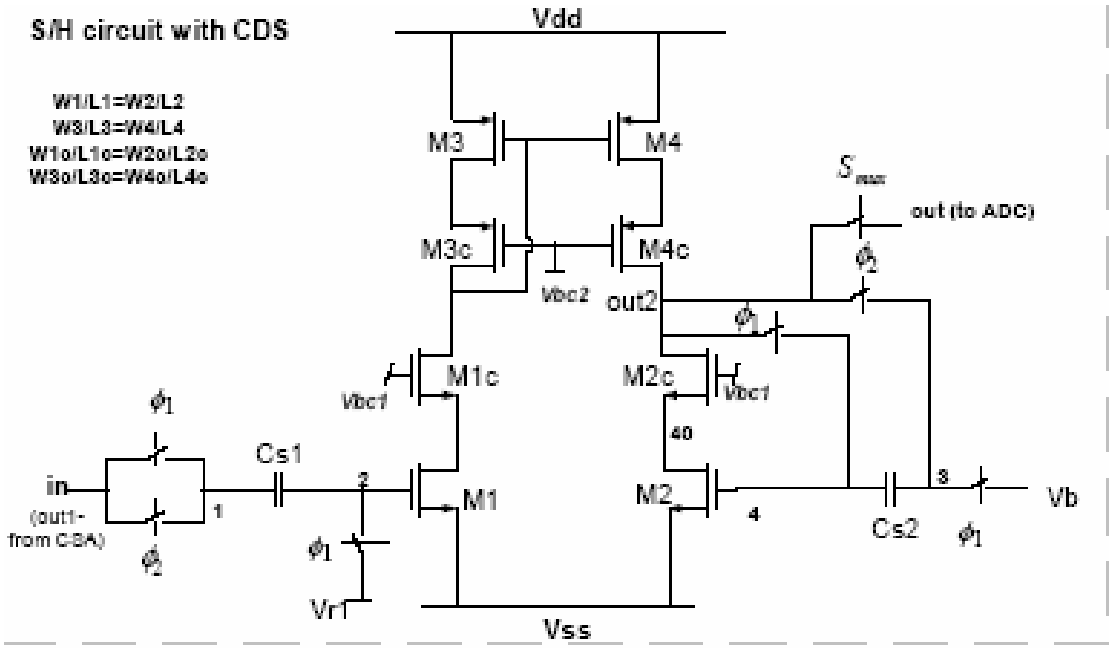


Fig 2.4-2 A CDS poly-Si circuit for readout systems.

TABLE I

Gray-code Quantization Table for the m = 3 example

ADC Input Range	Codeword
0- $\frac{1}{8}$	0 0 0
$\frac{1}{8}$ - $\frac{2}{8}$	0 0 1
$\frac{2}{8}$ - $\frac{3}{8}$	0 1 1
$\frac{3}{8}$ - $\frac{4}{8}$	0 1 0
$\frac{4}{8}$ - $\frac{5}{8}$	1 1 0
$\frac{5}{8}$ - $\frac{6}{8}$	1 1 1
$\frac{6}{8}$ - $\frac{7}{8}$	1 0 1
$\frac{7}{8}$ -1	1 0 0

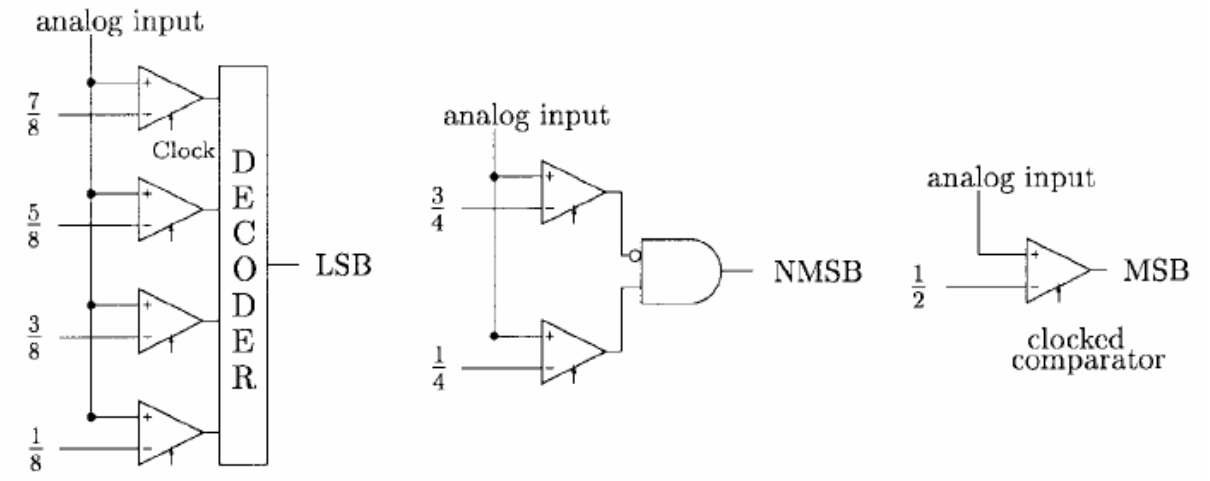


Fig 2.5-1 Three-bit flash ADC.

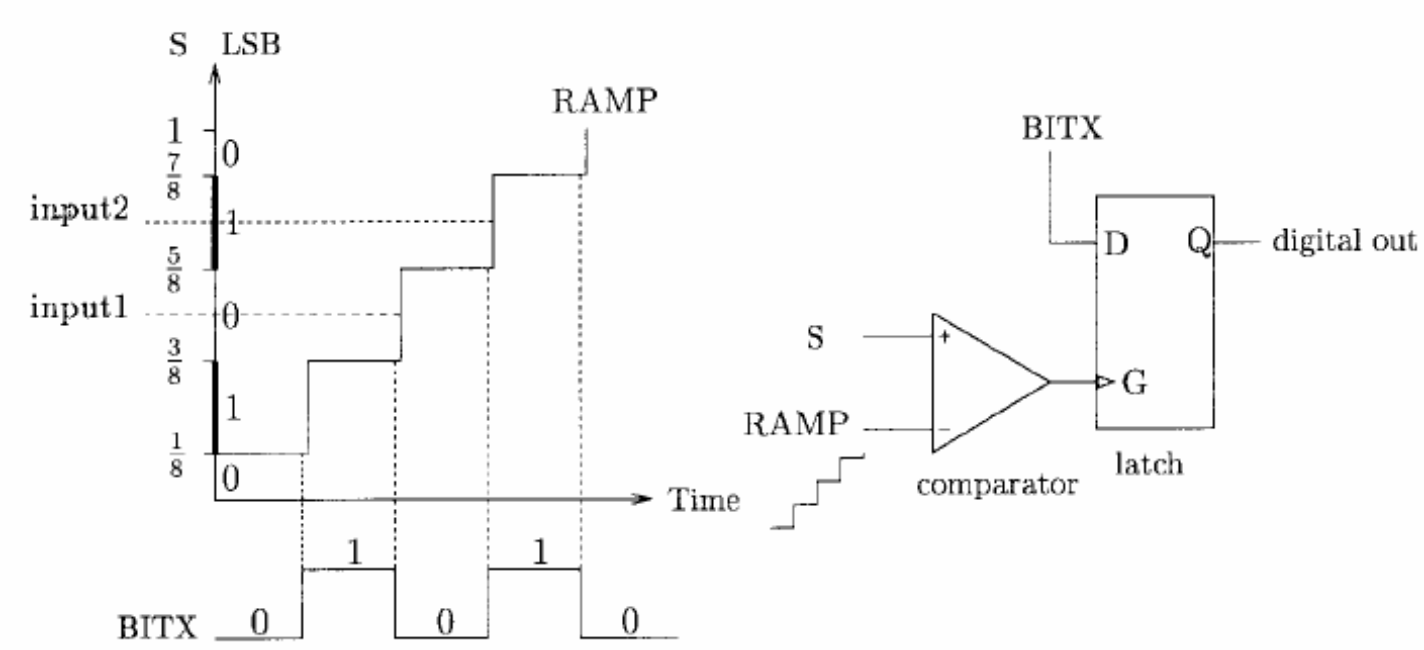


Fig 2.5-2 Comparator/latch pair operation.

Chapter 3

Charge Sensitive Amplifier Circuit

3.1 Introduction of Operation Amplifier

Operational amplifiers (op amps) are an integral part of many analog and mixed-signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering. Thedesign of op amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies.

We loosely define an op amp as a "high-gain differential amplifier." By "high," we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5. Since op amps are usually employed to implement a feedback system, their open-loop gain is chosen according to the precision required of the closed-loop circuit.

Up to two decades ago, most op amps were designed to serve as "general-purpose" building blocks, satisfying the requirements of many different applications. Such efforts sought to create an "ideal" op amp, e.g., with very high gain, high input impedance, and low output impedance, but at the cost of many other aspects of the performance, e.g., speed, output voltage swings, and power dissipation.

By contrast, today's op amp design proceeds with the recognition that the trade-offs between the parameters eventually require a multi-dimensional compromise in the overall implementation, making it necessary to know the adequate value that must be achieved for each parameter. For example, if the speed is critical while the gain error is not, a topology is chosen that favors the former, possibly sacrificing the latter.

Figure 3.1-1 shows two op topologies with single-ended and differential outputs. The small signal, low-frequency gain of both circuit is equal to g_{mN} (r_{ON} || r_{OP}), where the subscripts N and P denote NMOS and PMOS, respectively. This value hardly exceeds 20 in submicron device with typical current levels. The bandwidth is usually determined by the load capacitance, $C_{L.}$

In order to achieve a high gain, the differential cascade topologies can be used. Shown in figure 3.1-2 for single-ended output generation, such circuits display a gain on the order of g_{mN} [(g_{mN} r^2_{ON} || g_{mP} r^2_{OP})], but at the cost of output swing and additional poles. This configuration is also called "telescopic" cascade op amp to distinguish them from another cascade op amp. However, one drawback is that the output swings of telescopic op amps are relatively limited. Another drawback is the difficulty in shorting their inputs and outputs, e.g., to implement a unity-gain buffer similar to the circuit of figure 3.1-3. To understand the issue, let us consider the unity-gain feedback topology shown in figure 3.1-4. Under what conditions are both M_2 and M_4 in saturation? We must have Vout $\leq$ Vx + V_{TH2} and Vout $\geq$ Vb – V_{TH4}. Since Vx = Vb – V_{GS4} , Vb - V_{TH4} $\leq$ Vout $\leq$ Vb – V_{GS4} + V_{TH2}. Depicted in figure 3.1-5, this voltage range is simply equal to $V_{max} - V_{min} = V_{TH4} - (V_{GS4} - V_{TH2})$, maximized by minimizing the overdrive of M_4 but always less than V_{TH2}.

3. 2 Folded-Cascade Operation Amplifier

In order to alleviate the drawbacks of telescopic cascade op amps, namely, limited output swings and difficulty in shorting the input and output, a "folded cascade" op amp can be used. In an NMOS or PMOS cascade amplifier, the input device is replaced by the opposite type while still converting the input voltage to a current. In the four circuits shown in figure 3.2-1, the small-signal current generated by M_1 flows through M_2 and subsequently the load,

producing an output voltage approximately equal to $g_{m1}R_{out}Vin$. The primary advantage of the folded structure lies in the choice of the voltage levels because it does not “stack” the cascade transistor on the top of the input device.

The folding idea depicted in figure 3.2-1 can easily be applied to differential pairs and hence operational amplifiers as well. Shown in figure 3.2-2, the resulting circuit replaces the input NMOS pair with a PMOS counterpart. Note two important differences between the two circuits. (1) In figure 3.2-2(a), one bias current, Iss, provides the drain current of both the input transistors and the cascade devices, whereas in figure 3.2-2(b) the input pair requires an additional bias current. In other words, $Iss_1 = Iss/2 + I_{D3}$. Thus, the folded-cascode configuration generally consumes higher power. (2)In figure 3.2-2(a), the input common mode (CM) level cannot exceed $Vb_1 - V_{GS3} + V_{TH1}$, whereas in figure 3.2-2(b), it cannot be less than $Vb_1 - V_{GS3} + |V_{THP}|$. It is therefore possible to design the latter to allow shorting its input and output terminals with negligible swing limitation. This is in contrast to the behavior depicted in figure 3.1-2. Let us now calculate the maximum output voltage swing of the folded-cascode op amp shown in figure 3.2-3, where M_5-M_{10} replace the idea current sources of figure 3.2-2(b). With proper choice of Vb_1 and Vb_2, the lower end of the swing is given by $V_{OD3} + V_{OD5}$ and the upper end by $V_{DD} - (|V_{OD7}|+|V_{OD9}|)$. Thus, the peak-to-peak swing on each side is equal to $V_{DD} - (V_{OD3}+V_{OD5}+|V_{OD7}|+|V_{OD9}|)$. In the telescopic cascade of 3.2-2(a), on the other hand, the swing is less by the overdrive of the tail current source.

We now determine the small-signal voltage gain of the folded-cascode op amp of figure 3.2-3. Using the half circuit depicted in Fig 3.2-4(a) and writing $|Av| = G_mR_{out}$, we must calculate G_m and R_{out}. As shown in figure 3.2-4(b), the output short-circuit current is approximately equal to the drain current of M_1 because the impedance seen looking into the source of M_3, that is , $(g_{m3} + g_{mb3})^{-1} \parallel r_{O3}$, is typically much lower than $r_{O1} \parallel r_{O5}$. Thus, $Gm \approx g_{m1}$. To calculate $R_{out,}$ we use figure 3.2-4(c), with $R_{OP} \approx (g_{m7} + g_{mb7})r_{O7}r_{O9}$, to write $R_{out} \approx R_{OP} \parallel [(g_{m3} + g_{mb3})r_{O3}(r_{O1}\parallel r_{O5})]$. It follows that

$$|Av| \approx g_{m1}\{ [(g_{m3} + g_{mb3})r_{O3}(r_{O1}||r_{O5})] \,||\, [(g_{m7} + g_{mb7})r_{O7}r_{O9}] \}$$

A folded-cascode op amp may incorporate NMOS input devices and PMOS cascade transistors.[18]

To study the effect of the poly-Si TFT device variation on circuit uniformity, Monte Carlo simulation is executed and the parameters used in the simulation are shown in Table II. According to the measurement database, the threshold voltage V_{TH} distributions of the TFTs are with the mean values of 1.6V for n-type and -1.3V for p-type and the deviation for both type is 1V. The schematic of a folded-cascode operation amplifier used for CSA is shown in figure 3.2-5(a) [19]. As can be seen, many TFT pairs are used and represented by Ma*n* and Mb*n*. They are assumed to be perfectly matched in this section. For an X-ray generated charge of 2pC stored on Cd, the input signal Vin for the CSA will be 0.2V. It corresponds to the CSA output signal of -1V, which will be added to the reference voltage Vref of 7V. Thus, the ideal output voltage of CSA should be 6V. 30 times Monte Carlo simulation results of the output waveform are shown in figure 3.2-5(b). The diverse behaviors are attributed to the V_{TH} variation of the TFTs under fixed bias voltages, Therefore, the drain currents of the TFTs can be very different, and the output voltage of CSA largely deviate from the ideal 6V.

TABLE II. Parameters used in the charge sensitive amplifier circuit simulation.

Ma-b_1 W/L	1000μm/5μm
Ma_2 W/L	100μm/5μm
Ma-b_3 W/L	200μm/5μm
Ma-b_4 W/L	200μm/5μm
Ma-b_5 W/L	50μm/5μm
Ma-b_6 W/L	50μm/5μm
ΔV_{TH}	+/-1V
$\Delta \mu$	+/-20 cm^2/Vsec
Vdd	13V

3.3 Match-TFT VTH-self-compensated operation amplifier

3.3.1 Proposed Charge Sensitive Amplifier

In order to diminish the effects of V_{TH} variation, the circuit shown in figure 3.3-1(a) is proposed in this work to replace the fixed bias voltage for the n-type TFT. A diode-connected TFT, a capacitor Cvt and two switches S1 and S2 are used. The TFT is also assumed to be match to the corresponding TFT to be biased. The operation consists of two periods. In the first period, only S1 turns on so that a high voltage VDD is stored in Cvt. In the second period, only S2 turns on to discharge the stored voltage to Vbias1 + V_{TH}, which makes the new bias voltage Vbias1' compensate the V_{TH} variation. The bias current I_{Ma2} :

$$I_{Ma2} = K(V_{GS2} - V_{tha2})^2 = K(V_{bias1'} + V_{thb2} - 0 - V_{tha2})^2$$
$$= K(V_{bias1'})^2$$

Similarly, the bias voltage on the p-type TFTs can be compensated by the circuit shown in figure 3.3-1(b). The bias current I_{Ma3} :

$$I_{Ma3} = K\left(V_{SG3} - |V_{th3a}|\right)^2 = K\left[V_{S3} - V_{bias2} - |V_{tha3}|\right]^2$$
$$= K\left[V_{S3} - \left(V_{bias2'} - |V_{thc3}|\right) - |V_{tha3}|\right]^2$$
$$= K(V_{S3} - V_{bias2'})^2$$

Another 30 times Monte Carlo simulation results for the output voltage of the new CSA with compensation circuit is shown in figure 3.3-2 and its non-uniformity range in the CSA output voltage can be reduced to as low as 0.08V.

Figure 3.3-3(a) shows the output voltages of the new CSA with respect to the different input signal. Figure 3.3-3(b) compares the standard deviations of the output voltages for the circuits with different bias voltage compensations. The merits of the proposed circuit are distinguished, including the wide operation range and the small deviation below 0.033V. Furthermore, the deviation is less dependent on the input voltage, reflecting the effectiveness of the proposed circuit.

3.3.2 Proposed Charge Sensitive Amplifier with internal bias

The method to compensate three bias points still have some issues : It requires additional three additional capacitances and nine TFTs compared to the original circuit. The way to solve the issue is using internal-bias circuit shown in figure 3.3-4. The current I_{Ma3} and I_{Mb3} are controlled by I_{Mc3} and I_{Ma4} equal to I_{Ma3} minus I_{Ma1} .Therefore, only M_{a2} is needed to use compensation circuit. Figure 3.3-5 shows the simulation result of Monte Carlo. The variation of output voltage is 0.08V. Considering variation of resistor due to process, variation of resistor is simulated which shown in figure 3.3-6. The result shows that tolerance of resistor could be 115KΩ ± 30%. Figure 3.3-7(a) shows the output voltages of the CSA with respect to the different input signal. Figure 3.3-7(b) compares the standard deviations of the output voltages for the circuits with different bias voltage compensations and with internal-bias method.

3.4 Discussion

A novel charge sensitive amplifier circuit employing poly-Si TFTs is proposed for the readout system of the active matrix sensor. It can considerably reduce the circuit's sensitivity to unavoidable threshold voltage variations of the poly-Si TFTs.

Figure caption – Chapter3

different input signal and (b) comparison of the circuits with different bias voltage compensation methods and with internal-bias method

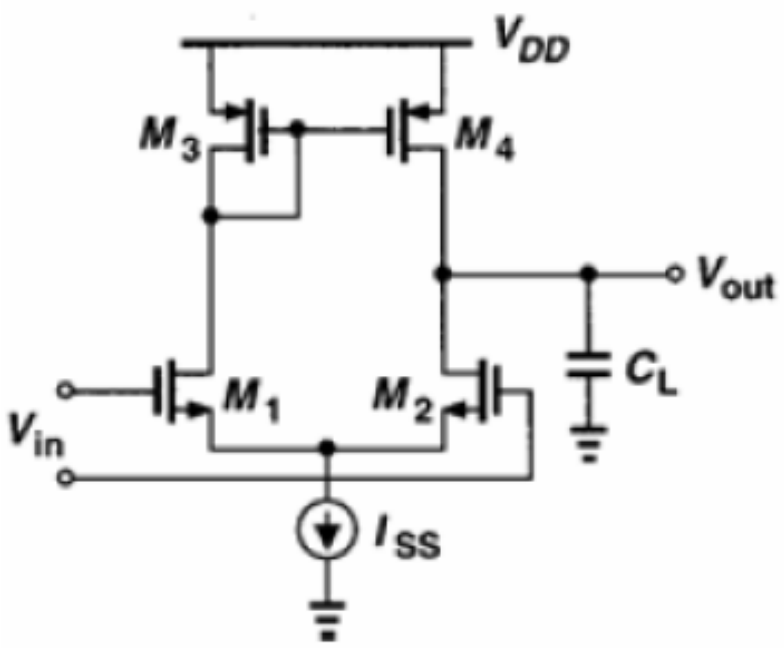
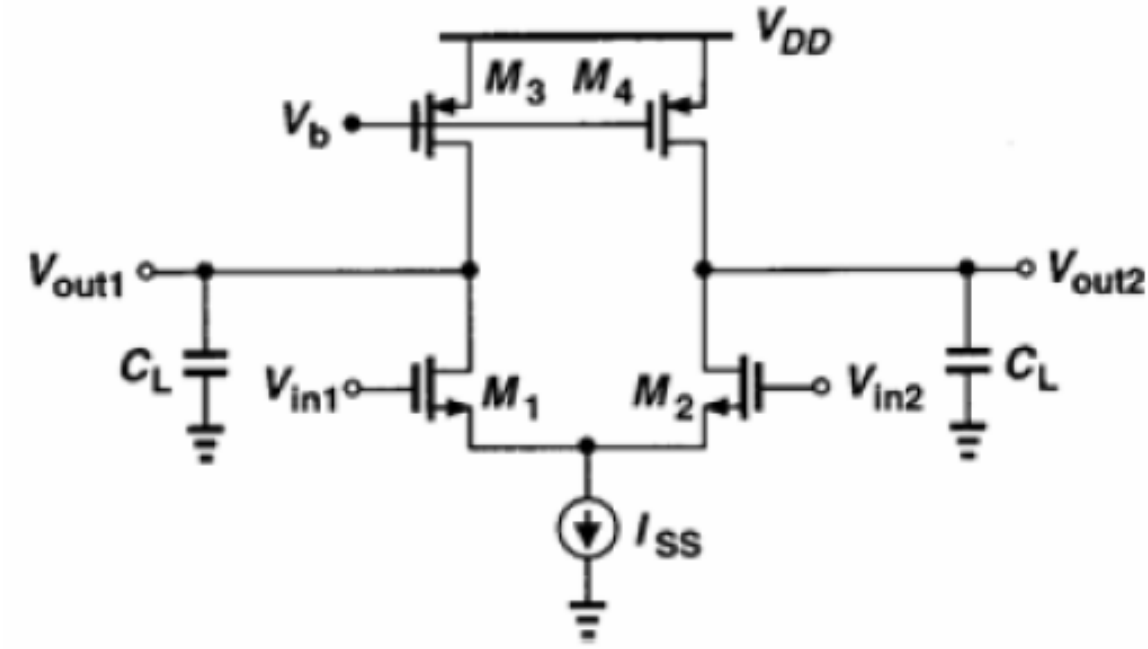


Fig 3.1-1 Two op topologies with (a)single-ended and



(b)differential outputs.

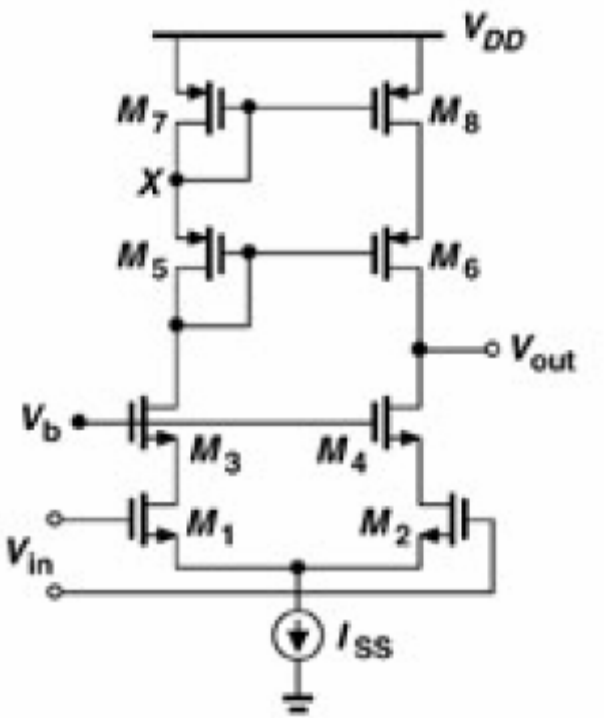


Fig 3.1-2 The configuration of "telescopic" cascade op amp.

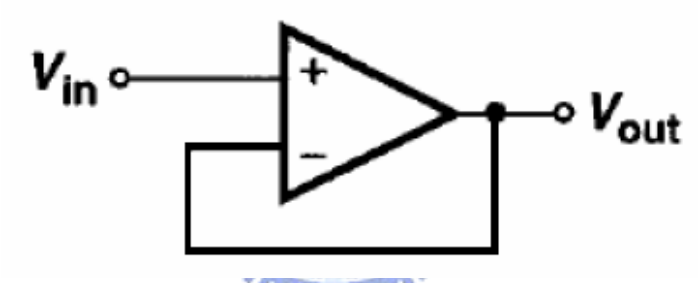


Fig 3.1-3 A unity-gain buffer

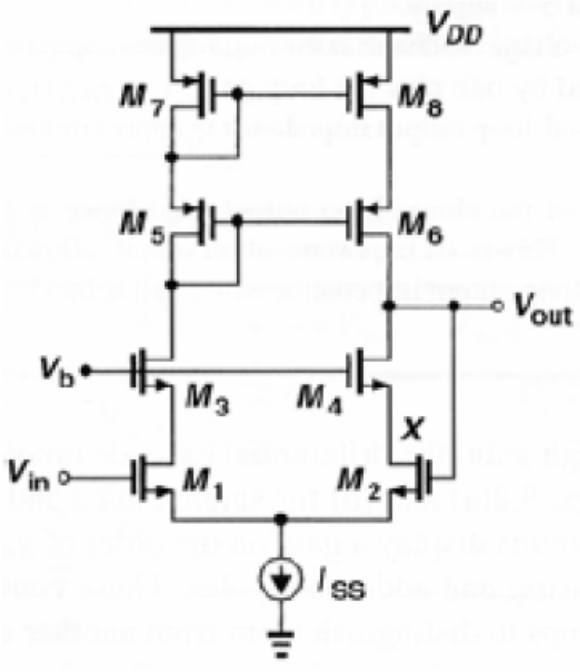


Fig 3.1-4 The unity-gain feedback topology

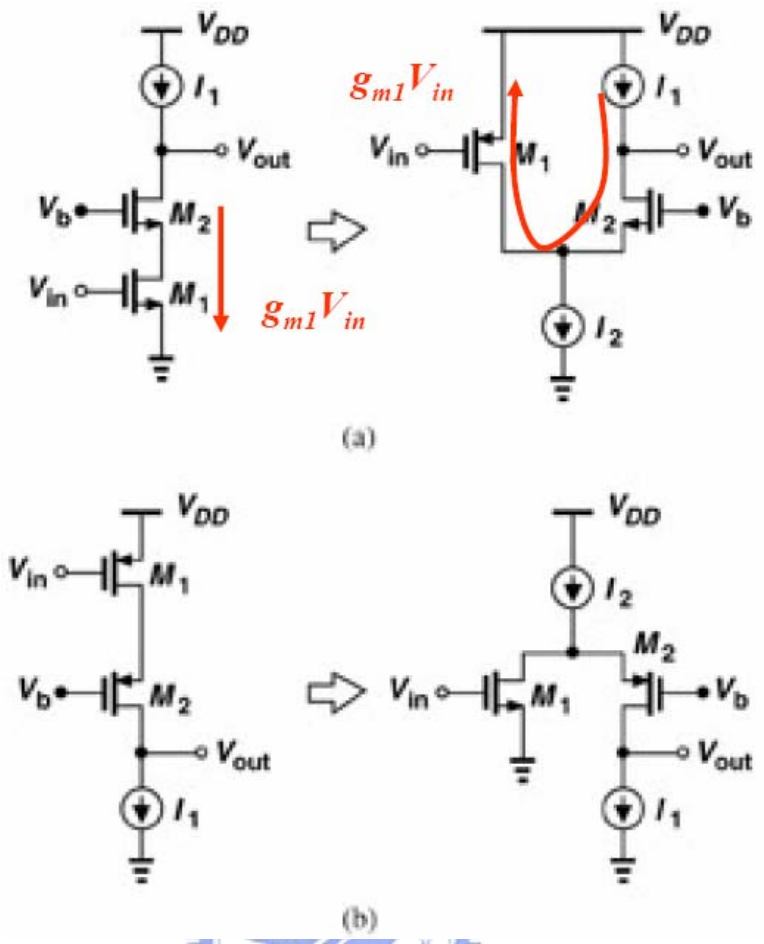


Fig 3.2-1 The input device is replaced by the opposite type

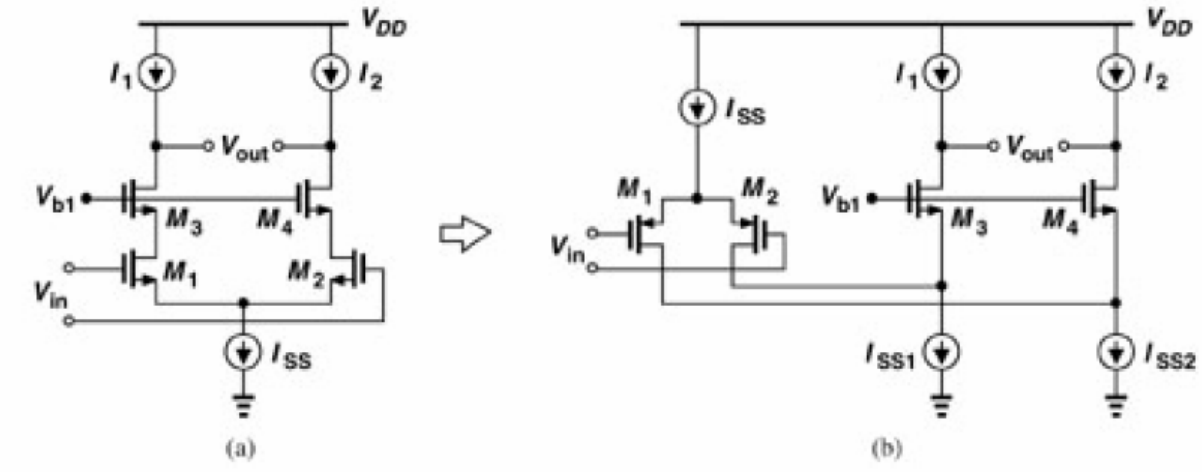


Fig 3.2-2 The resulting circuit replaces the input NMOS pair with a PMOS counterpart (a) one bias current, Iss, provides the drain current of both the input transistors and the cascade devices. (b) the input pair requires an additional bias current

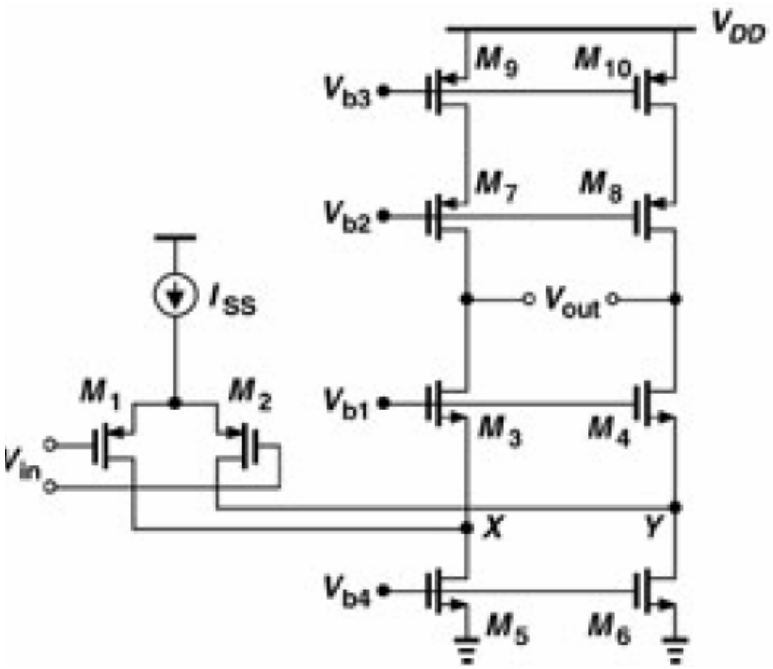


Fig 3.2-3 The folded-cascode op amp

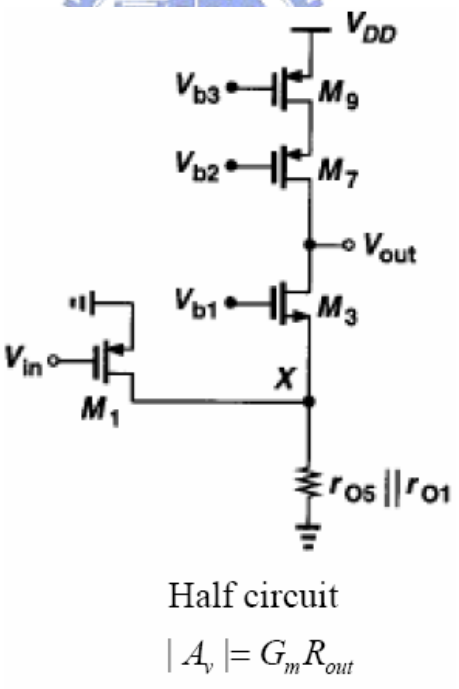
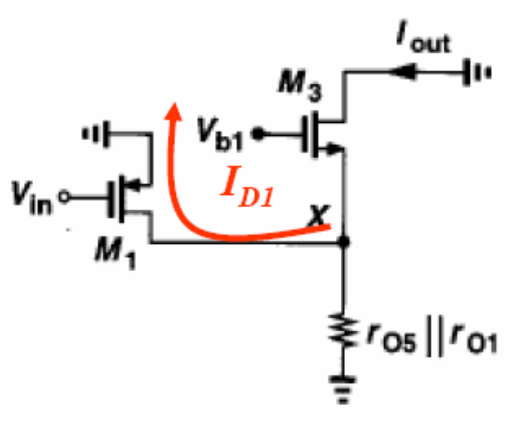
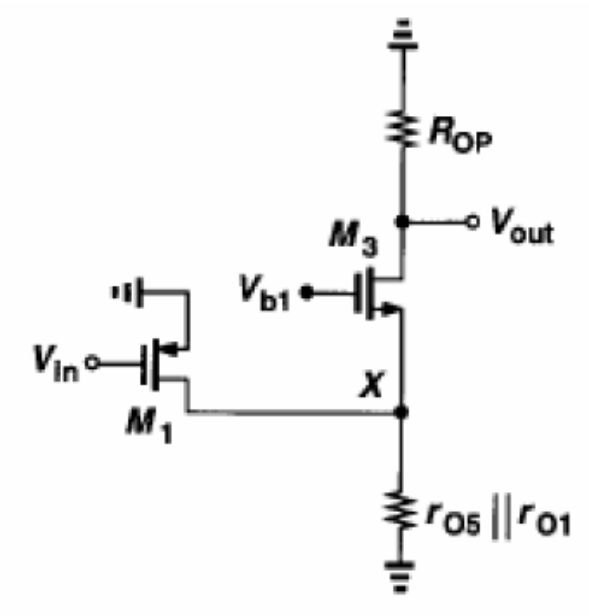


Fig 3.2-4 (a) the half circuit of the folded-cascode op amp



(b) Equivalent circuit with output shorted to ground.



(c) Equivalent circuit with output open.

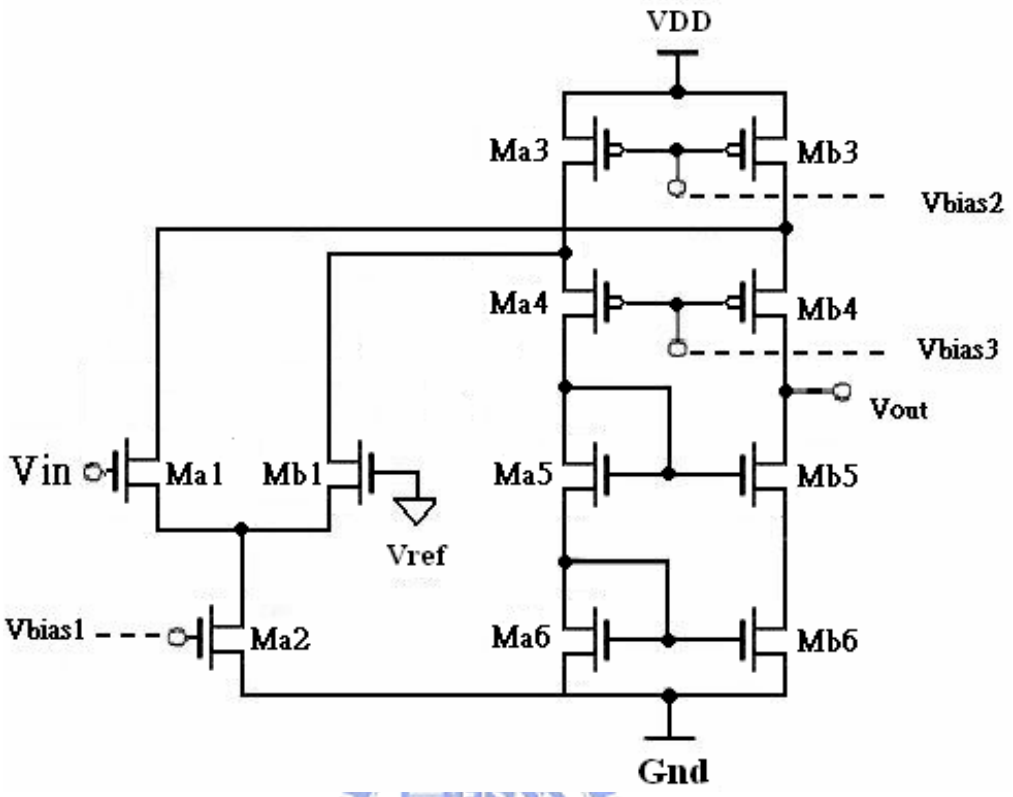
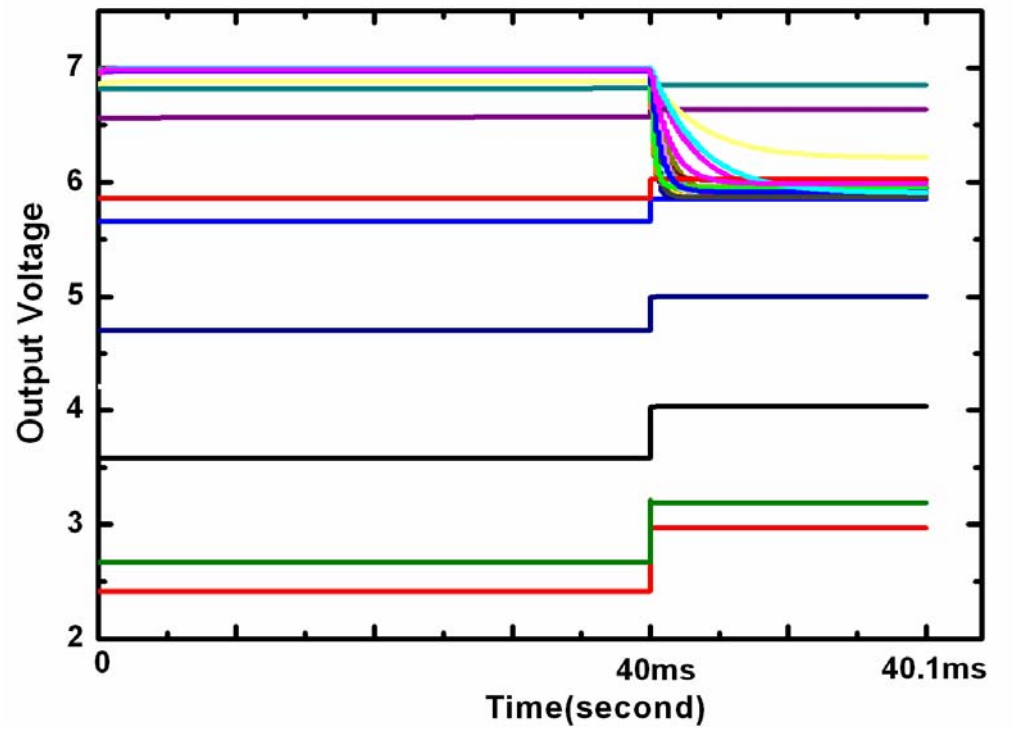


Fig 3.2-5 (a) The schematic of a folded-cascode operation amplifier used for CSA.



(b) 30 times Monte Carlo simulation results for CSA output voltage.

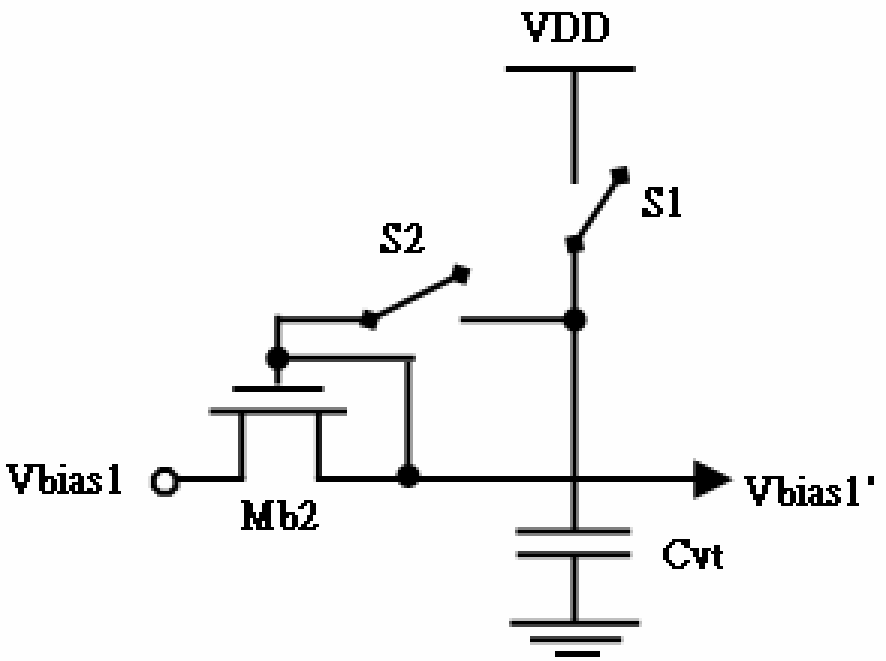
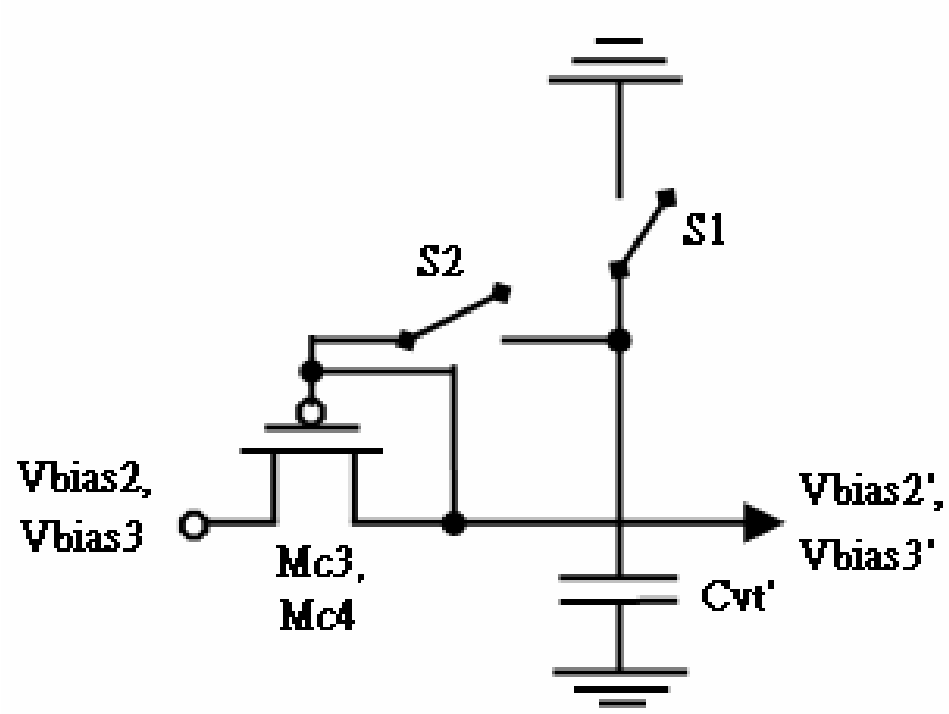


Fig 3.3-1 Compensation circuits of the bias voltages for (a) n-type.



(b) p-type TFTs

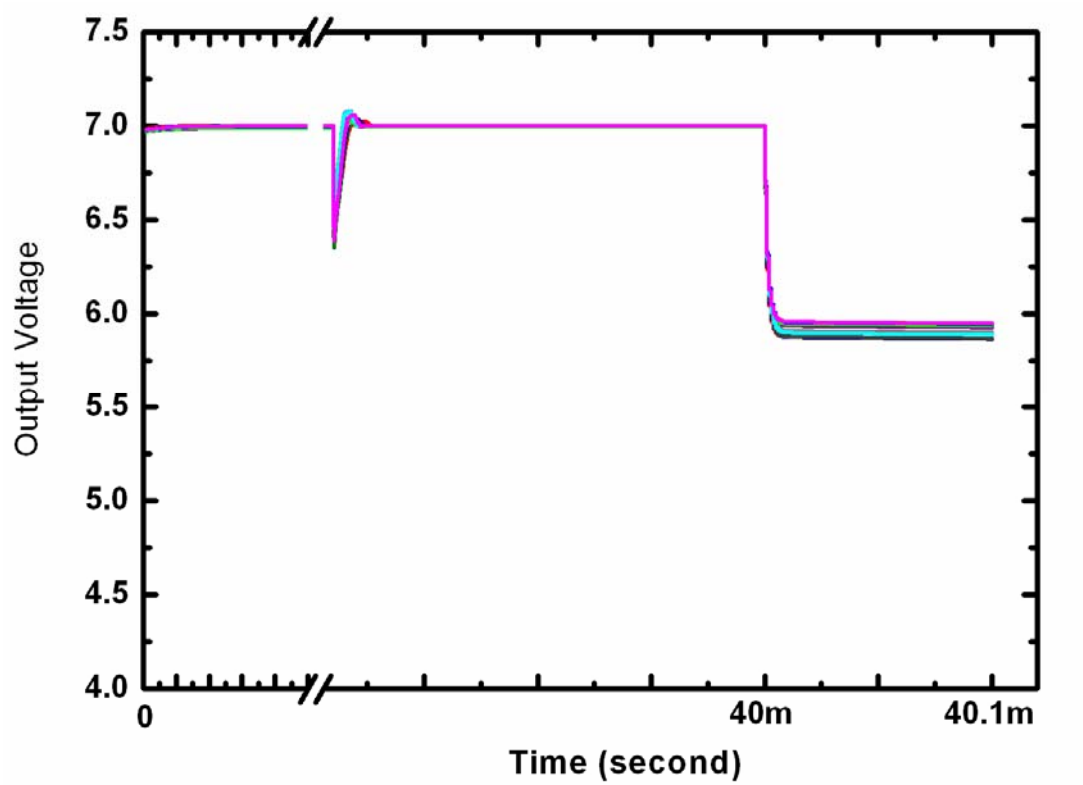


Fig 3.3-2 30 times Monte Carlo simulation results for CSA output voltage with compensation circuit

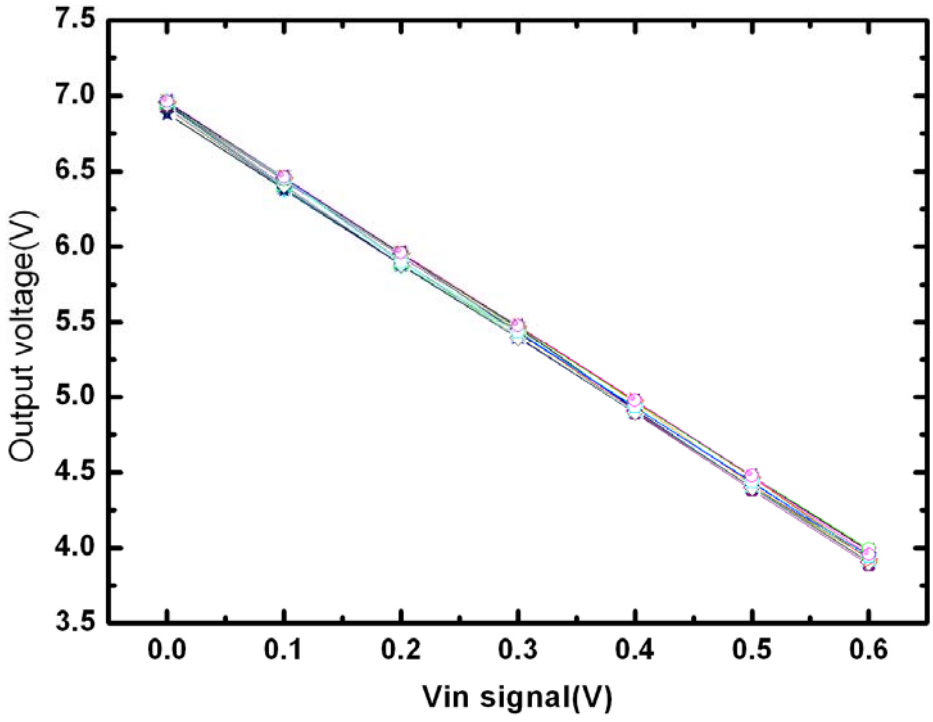
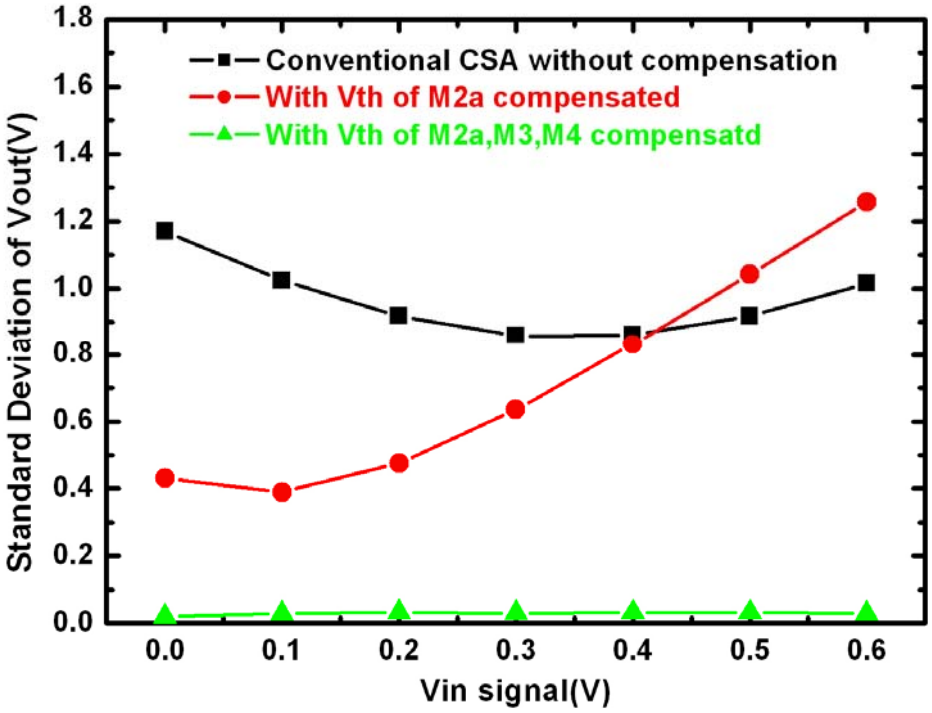


Fig 3.3-3 30 times Monte Carlo simulation results of (a) output voltage with respect to the different input signal.



(b) Comparison of the circuits with different bias voltage compensation methods.

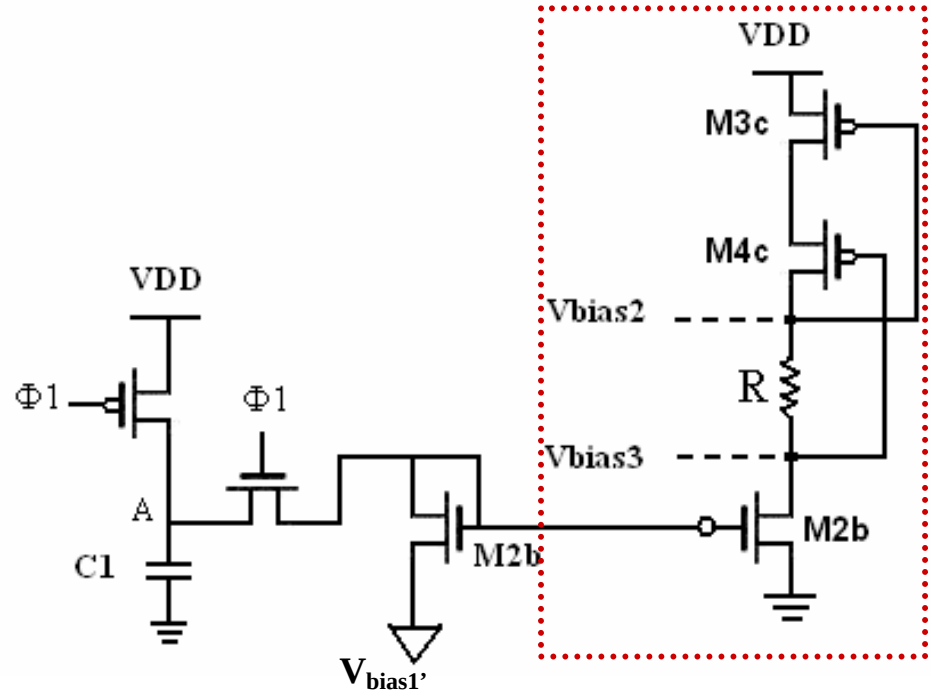


Fig 3.3-4 Internal-bias with compensation circuit.

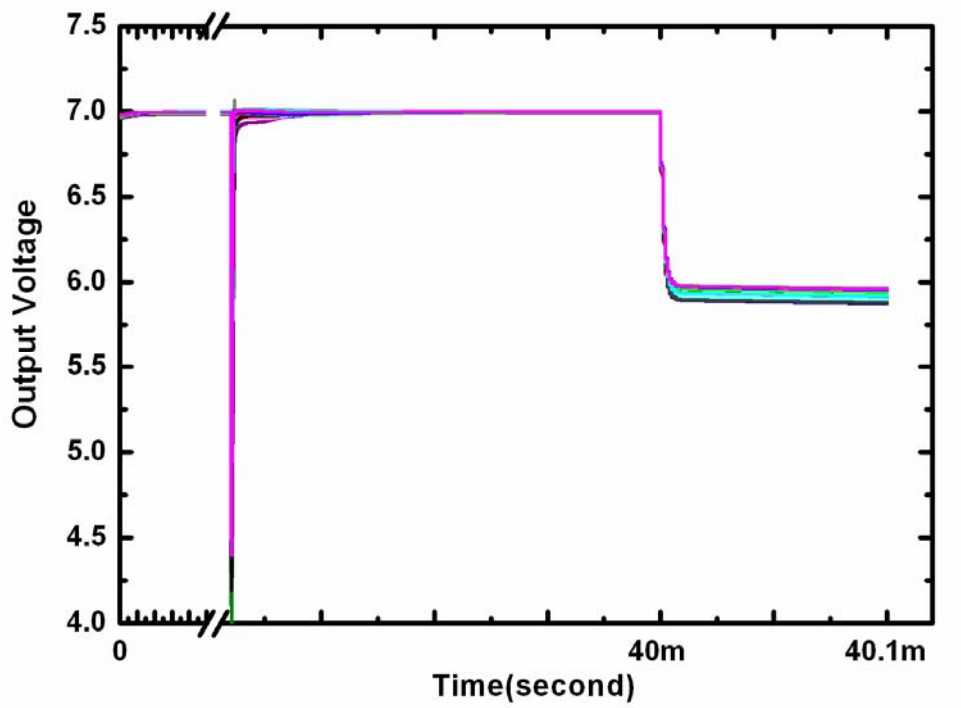


Fig 3.3-5 30 times Monte Carlo simulation results for CSA output voltage with internal-bias and compensation circuit

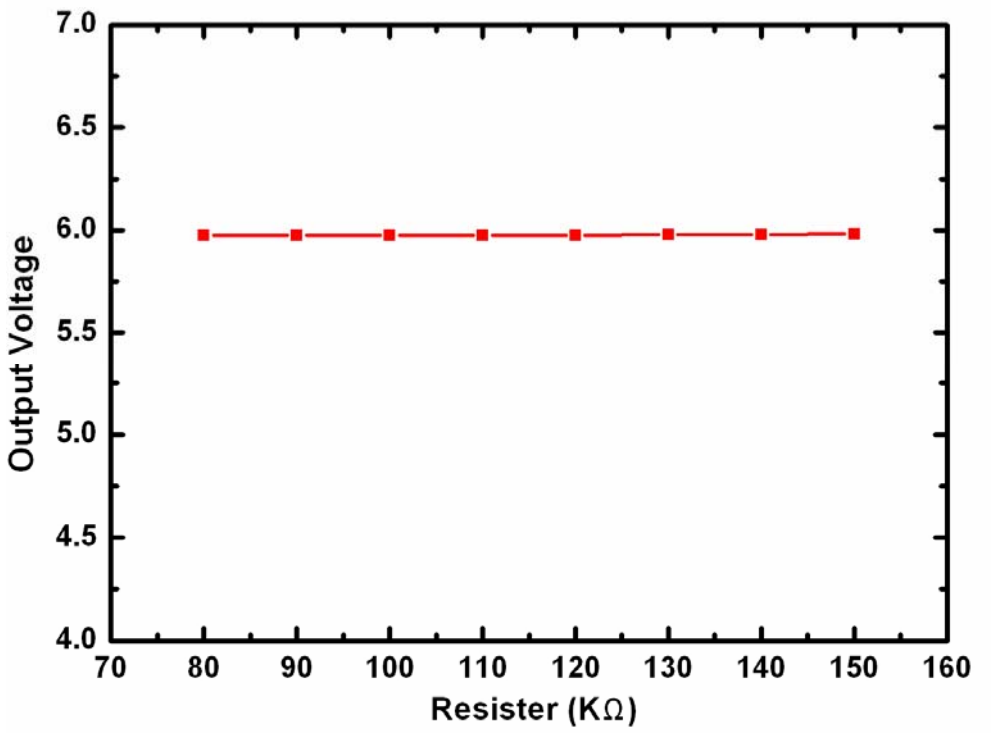


Fig 3.3-6 Simulation results for CSA output voltage with variation of resistor.

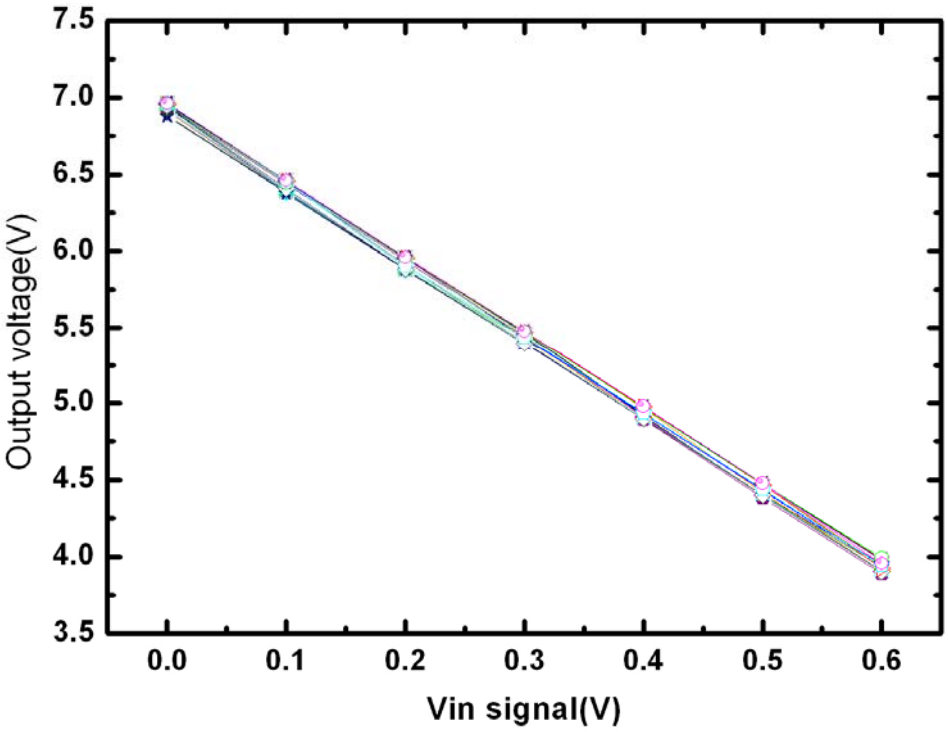
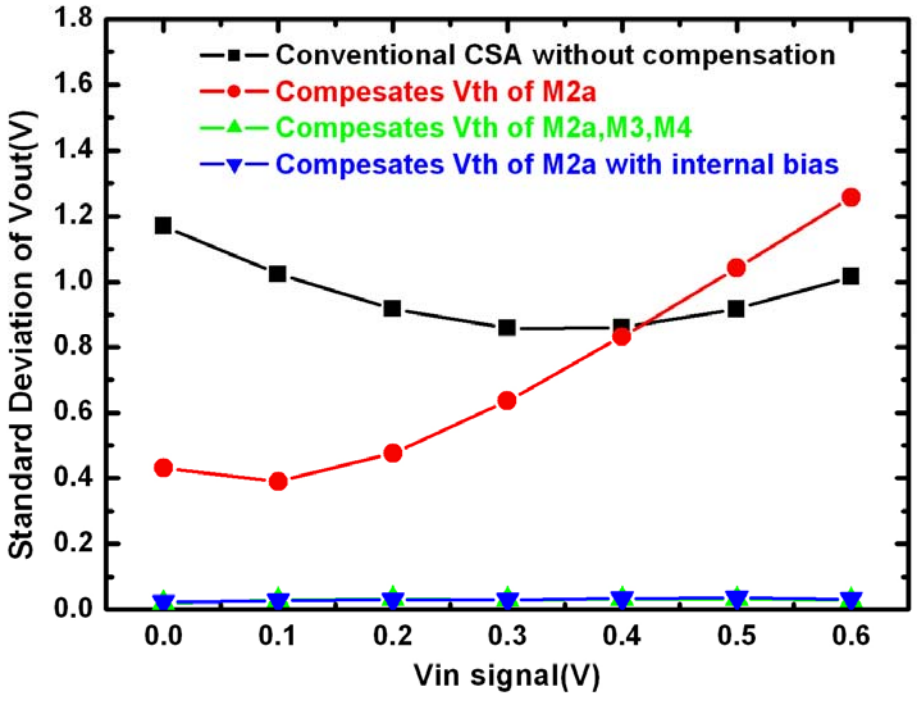


Fig 3.3-7 30 times Monte Carlo simulation results of (a) output voltage with respect to the different input signal



(b) Comparison of the circuits with different bias voltage compensation methods and with internal-bias method

Chapter 4

Effect of Mismatch on Circuit Performance

4.1 Introduction

In prior studies, it is known that LTPS TFTs suffered from severe device variation even under well-controlled process. Since the device variation is inevitable in LTPS TFTs, it is essential to classify the sources of variation. In MOSFETs (Metal-Oxide-Silicon Field Effect Transistors), the local variations can be characterized by short correlation distances and global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performances. If this distance is lower than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g. a charge trapped in the gate oxide layer). For the global variation, which is characterized by process disturbances with longer correlation distances (e.g. the gate oxide thickness across the wafer surface), affects all the devices within a defined region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other.

In order to identify the effects of the global and local variation, the parameters differences of two devices under certain distance are divided with several groups according to the distance between two devices. In prior studies [14], the averages of parameters differences stand for global variation of LTPS TFTs, while the standard deviation of parameter differences shows the local variation in the devices. In this chapter, we characterize the micro variation for the analysis of LTPS TFTs, respectively.

4.2 Mismatch Effect and Simulated Results

With the method in the previous chapter, the circuit's sensitivity to the threshold voltage variation is considerably reduced. However, even if the two devices are very closely placed, the micro variation is still observed as shown in figure 4.2-1 [14]. For simulation, offset voltage V_{OS} is put at the input node to represent the V_{TH} and μ mismatch of the pair TFTs. The output voltage in the period before the X-ray exposure is simulated to examine the offset noise. Figure 4.2-2 shows the statistical simulation results with Vref set at 7V. The output voltage with TFT mismatch of V_{OS} exhibits a large variation range about 0.6V. Thus, another circuit is necessary to accommodate the mismatch effect

4.3 Offset voltage cancellation

The circuit shown in figure 4.3-1 is used to cancel the offset voltage. Firstly, only switches T1 turns on to make the capacitor Cst store V_{OS}. Secondly, only T2 turns on to compensate the voltage Vin^{-} with the voltage stored in Cst. With this compensation, V_{OS} between Vout and Vref can be reduced to 0.02V, as shown by the solid circles in figure 4.2-2.

Furthermore, the mismatch effect at different input signals is shown in figure 4.3-2. As can be seen, the standard deviation of output voltage with V_{OS} compensation is below 0.08V and become higher for the higher the input signal. For the worst case, the noise arisen from the V_{TH} and μ mismatch effect is about 3 times larger than that from V_{TH} and μ variation effect after compensation and can not be ignored.

Figure caption – Chapter4

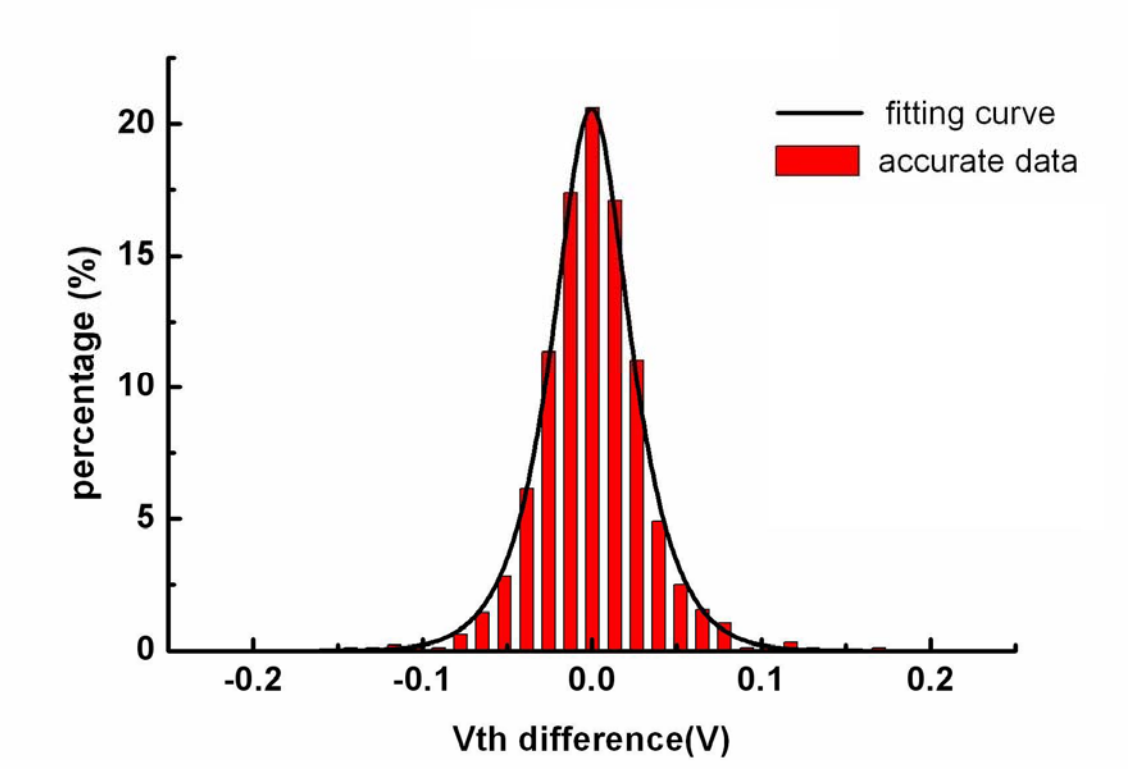


Figure 4.2-1 The distribution of Vth difference between two closely placed TFTs.

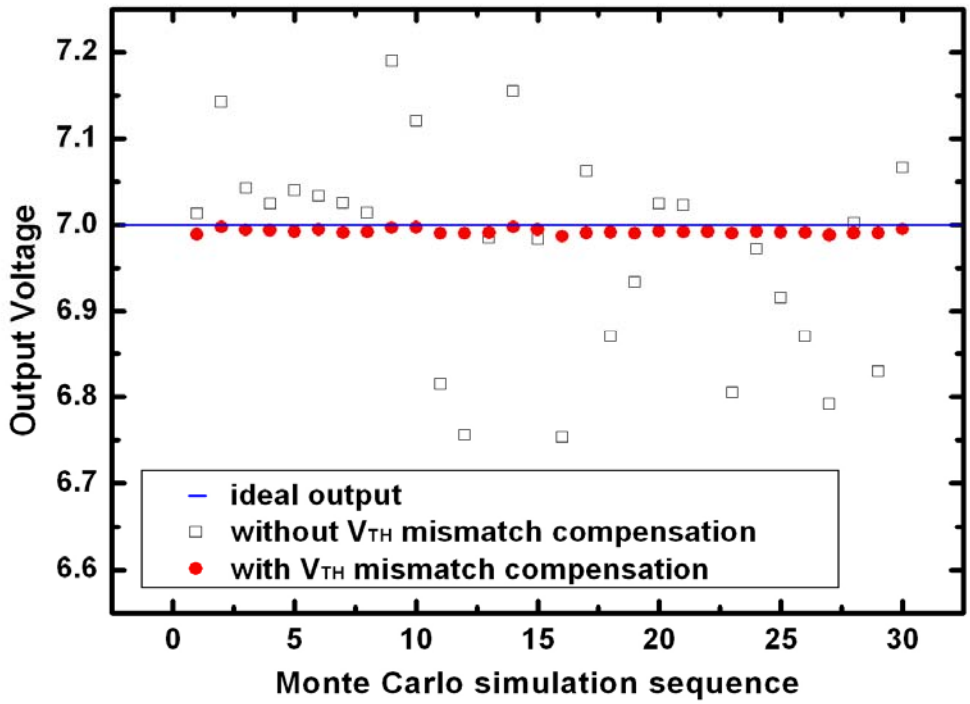


Figure 4.2-2 30 times Monte Carlo simulation results for the output voltages of CSA in the period before X-ray exposure.

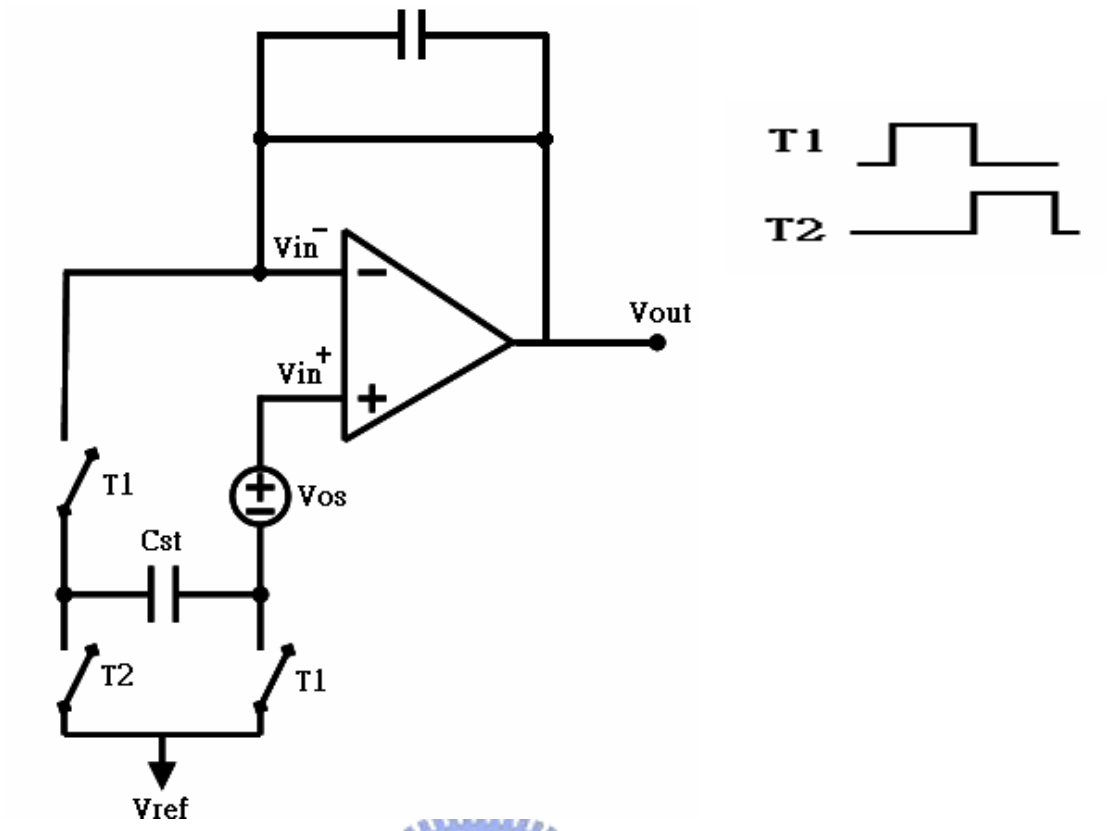
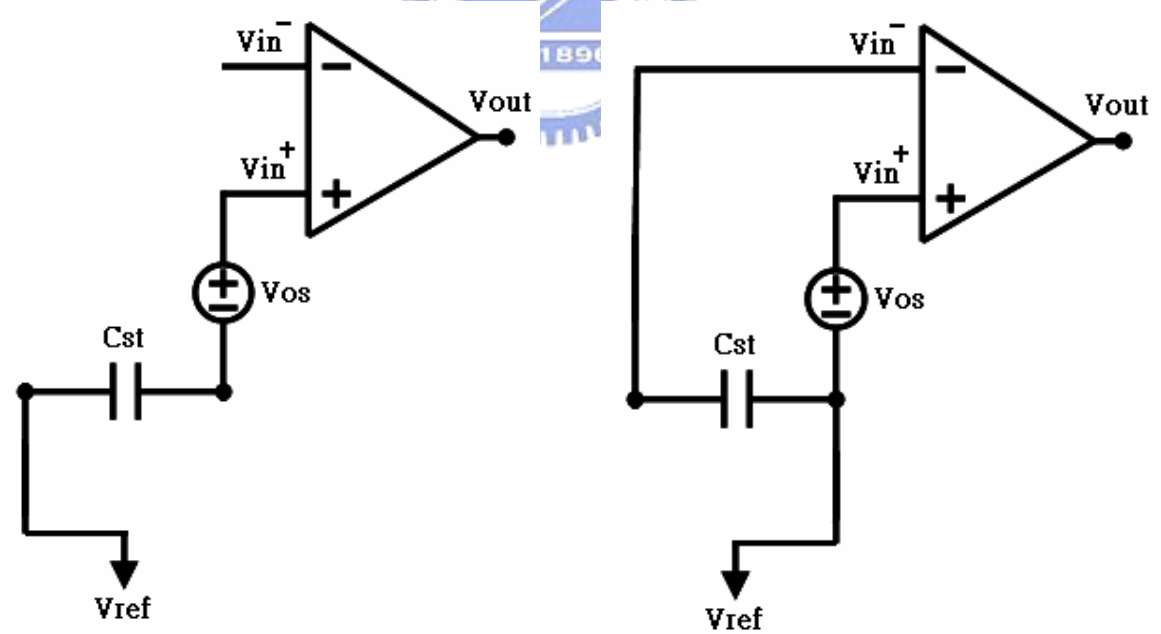


Figure 4.3-1(a) CSA circuit with input offset cancellation



(b) (c)

(b) only switches T1 turns on to make the capacitor Cst store V_{OS}

(c) only T2 turns on to compensate the voltage Vin^- with the voltage stored in Cst.

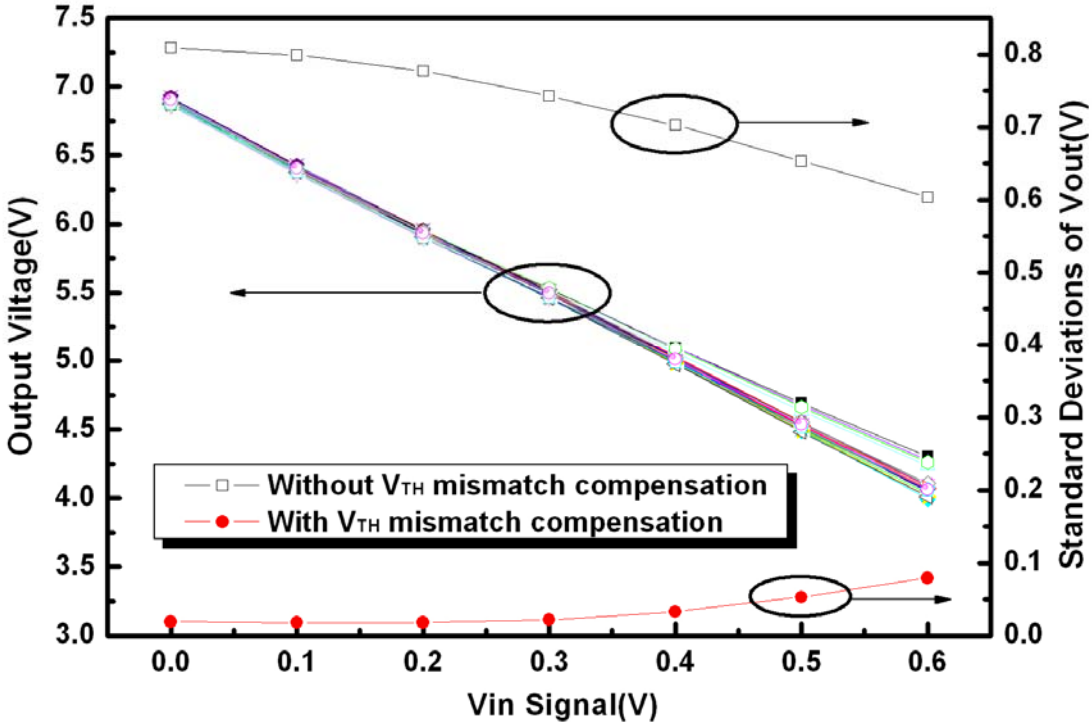


Figure 4.3-2 Mismatch effect of the output voltage with respect to the different input signal and comparison of the circuits with or without V_{TH} mismatch compensation.

Chapter 5

Conclusion

A poly-Si TFT circuit with V_{TH} compensation and offset cancellation capabilities that can be employed in active matrix systems has been presented and its operation described and simulated base on the really measured database. The proposed circuit can provide high immunity to the variation of poly-Si TFT characteristics and reduce the output voltage deviation to as low as 0.08V. The TFT mismatch effect is even larger than the variation effect for the circuit with compensation. The improvements of poly-Si TFT in both variation and mismatch control are required for the digital X-ray image with higher bit.

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