國立交通大學

光電工程學系 光電研究所碩士班

碩士論文

低溫多晶矽薄膜電晶體非匹配效應之研究

Study of Mismatch Effect for Low Temperature Polysilicon Thin Film Transistors

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中 華 民 國 九 十 五 年 六 月

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中文摘要

本論文主要研究低溫多晶矽薄膜電晶體的非匹配效應。首先我們探討在小尺寸元件叉合(Interfigitated)效應對尺寸的影響，發現非匹配因素隨著元件面積的增加而遞減。為了進一步探討叉合效應的非匹配特性，我們使用了大量相同面積的枕木型元件以作為實驗的依據。藉由分析元件參數差值的標準差，我們發現叉合方法比傳統方法具有更優良的特性，其中位障電壓與遷移率差值的標準差與叉合數目呈現反比，特別是位障電壓，因此我們提出一個公式以準確預測叉合方法的效能。此外，我們也探討了叉合方法中的距離效應，發現距離遠近與非匹配效應並沒有明顯的關聯性。接著我們利用電容量測的方法來加以驗證非匹配效應，實驗方法是採取電容對電壓的微分並觀察其最大值與相對應的電壓。我們發現叉合方法的標準差明顯地減少，進一步的驗證了叉合方法對非匹配效應的改良。

Study of Mismatch Effect for Low Temperature Polysilicon Thin Film Transistors

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Abstract

In this thesis, we investigate the mismatch issue for LTPS TFTs. Firstly we aim at the size and interdigit effects for small area TFTs. It is observed that the mismatching factor decreases rapidly with the increase of the device's area. To further investigate the mismatching properties of the interdigitated arrangements, a huge number of crosstie devices with the same dimension are utilized. By analyzing standard deviations of parameters' differences, it is found that the interdigitated method is indeed superior than the original. Besides, Vth and Muo are inversely proportional to the interdigit's finger numbers, especially the threshold voltage. Therefore, a model is proposed to predict the performance of the interdigitated method, which has high accuracy with the real data. As far as distance analysis is concerned, almost no correlations between the distance and mismatch effect could be observed. Next, the mismatching properties are examined by C-V measurements. We take the derivatives of capacitance versus gate voltage to observe the maximum value and its corresponding voltage. As a consequence, standard deviations with

interdigitated method are smaller than those of original devices, which is consistent with the conclusion of I-V measurement.

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鈺函 2006.07.11

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Chapter 1

Introduction

1-1. Mismatch of Differential Amplifiers in IC design

The differential amplifier is among the most important circuit inventions, dating back to the vacuum tube era. Offering many useful properties, differential operation has become the dominant choice in today's high-performance analog and mixed-signal circuits. An important attributes of differential amplifiers is their ability to suppress the effect of common-mode perturbations.

In a symmetric circuit, input CM (common-mode) variations disturb the bias points, altering the small-signal gain and possibly limiting the output voltage swings. However, considering the asymmetry resulting from mismatches between M_1 and M_2 in Fig. 1-1(a), the two transistors would carry slightly different currents and exhibit unequal transconductances, which owes to the mismatches of dimension and threshold voltage[1]. To calculate the gain from $Vin_{,CM}$ to V_{out1} and V_{out2}, an equivalent circuit is used in Fig. 1-1(b) with $I_{D1} = g_{m1}(V_{in,CM} - V_p)$ and $I_{D2} = g_{m2}(V_{in,CM} - V_p)$. That is,

$$(g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} = V_P, \tag{1-1}$$

and

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}\,. \tag{1-2}$$

Then output voltages could be obtained as

$$V_X = -g_{m1}(V_{in,CM} - V_P)R_D = \frac{-g_{m1}}{(g_{m1}+g_{m2})R_{SS}+1} R_D V_{in,CM} \quad (1\text{-}3)$$

$$V_Y = -g_{m2}(V_{in,CM} - V_P)R_D = \frac{-g_{m2}}{(g_{m1}+g_{m2})R_{SS}+1} R_D V_{in,CM} \quad (1\text{-}4)$$

The differential component at the output is therefore given by

$$V_X - V_Y = -\frac{g_{m1}-g_{m2}}{(g_{m1}+g_{m2})R_{SS}+1} R_D V_{in,CM} \quad (1\text{-}5)$$

In other words, the circuit converts input CM variations to a differential error by a factor equal to

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1}+g_{m2})R_{SS}+1}, \quad (1\text{-}6)$$

where A_{CM-DM} denotes common-mode to differential-mode conversion.

For meaningful comparison of differential circuits, the undesirable differential component produced by CM variations must be normalized to the wanted differential output resulting from amplification. We define the “common-mode rejection ratio” (CMRR) as

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right| \quad (1\text{-}7)$$

If only g_m mismatch is considered, it can be showed from the analysis of Fig. 1-2 that

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{1+(g_{m1}+g_{m2})R_{SS}} \quad (1\text{-}8)$$

where it is assumed $V_{in1} = V_{in2}$, and hence

$$CMRR = \frac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \quad (1\text{-}9)$$

$$\approx \frac{g_m}{\Delta g_m}(1+2g_m R_{SS}) \quad (1\text{-}10)$$

where g_m denote the mean value of g_{m1} and g_{m2}.

From the equation of (1-10), it is a valid argument that the value of CMRR decrease as the mismatches between the two transistors get worse, which means that the differential amplifier has worse tolerance with signal's fluctuation. Therefore, it is obvious that the study of the matching behavior of MOS (Metal-Oxide-Silison) transistors remains important because the performance of analog MOS integrated circuits depends heavily upon the element of matching accuracy [y1].

1-2. Mismatch on MOSFETs and LTPS TFTs

It is generally agreed that the mismatching variations in IC design are further extended as wafer-to-wafer, batch-to-batch and lot-to-lot variation. The mismatch issue is examined with respect to the mutual device distance. In the application using MOSFETs (Metal-Oxide-Silicon Field Effect Transistors) with high sensitivity to the mismatch variations such as differential amplifiers, the statistical mismatching analysis would be a very important verification step. In the scope of this thesis, since the LTPS TFTs (Low Temperature Poly-Si, Thin Film Transistors) may be used to make advanced circuitry and the perspective of System-On-Glass (SOG), the mismatch and uniformity issue would become more essential.

There is no disagreement that LTPS TFTs have different process from IC industry owing to the different substrate and low process temperature, which could be the source of the device's mismatching behavior. Besides, compared with MOSFETs, the LTPS TFTs contains a larger number of defects in the poly-silicon film as shown in Fig. 1-2, which distributes randomly and hardly controlled by manufacturing process[2-4]. Therefore, it may farely be assumed that the mismatching effect on LTPS TFTs could be more essential and complicated than that on MOSFETs[5].

1-3. Mismatch Source of LTPS TFTs

LTPS TFTs are found to suffer serious behaviors of mismatching variations even from predominant process conditions. Though the device structure is similar to MOSFETs, the mismatching behaviors of TFTs are much worse than those of MOSFETs. Since the mismatch of device behavior may directly affect the circuit performance and reliability prediction, it would be very essential to have a clear understanding of what the mismatch property comes from.

Mismatch sources of LTPS TFTs can be divided as local variations characterized by short correlation distances and global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performance[6]. If this distance is lower than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g. a charge trapped in the gate oxide layer). For the global variation, which is characterized by process disturbances with longer correlation distances (e.g. the gate oxide thickness across the wafer surface), affects all the devices within a defined region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other.

In this work, the sources of mismatch are classified as macro variation and micro variation. Macro variation comes from the issue of process control, such as gate insulator thickness, LDD (Lightly Doped Drain) length fluctuation and ion implantation uniformity. This non-uniformity of process control will result in the common shift of device parameters. On the other hand, micro variation comes from the differences of the defect site, defect density in the active region and the activation efficiency. Since these conditions vary from device to device, micro variation will lead to the random distribution of device parameter. In chapter 2, the mismatch issue

of LTPS TFTs will be discussed with the distribution of device parameters.

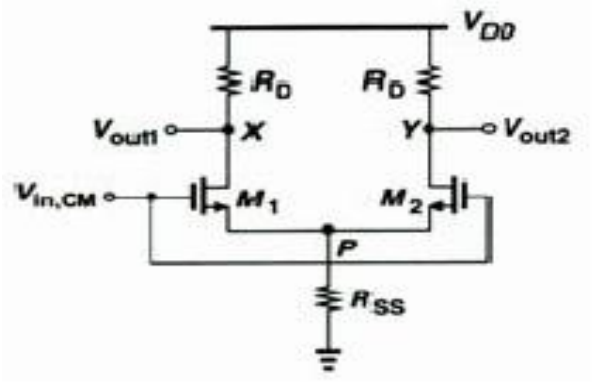
1-4. Motivation

Up to now, very few researches have been made on the mismatch issue of LTPS TFTs. Most researches about LTPS TFTs aim at the improvement of the device performance. However, before LTPS TFTs can be widely-applied in mass production, the study of mismatch would be crucial and necessary. In this thesis, we focus on the mismatch effect on LTPS TFTs and various interdigitated method to improve the performance on device behavior and circuit.

In chapter 2, we start from examining the mismatch behavior of LTPS TFTs on different size and dimensions. In order to evaluate the mismatch properties with statistical method, a new device layout is proposed, e.g. the crosstie layout. By utilizing this layout, various kinds of interdigitated could be performed to eliminate the mismatch effect. As shown in chapter 3, interdigitated methods with different number of fingers, distances and configurations are demonstrated. In addition, a model is also proposed to predict the performance of the interdigitated method. In chapter 4, we further examine the mismatch property via C-V measurements.

1-5. Thesis Outline

1. Introduction
    1.1 Mismatch in IC design
    1.2 Characteristics of Poly-Si TFTs
    1.3 Manufacture of devices
    1.4 Motivation
    1.5 Thesis outline
2. I-V Mismatch Analysis



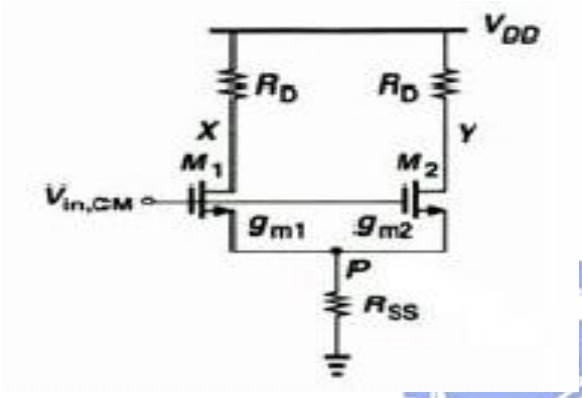


Fig. 1-1 Common-mode response in the presence of transistor mismatch (a) Differential pair sensing CM input (b) equivalent circuit of (a)

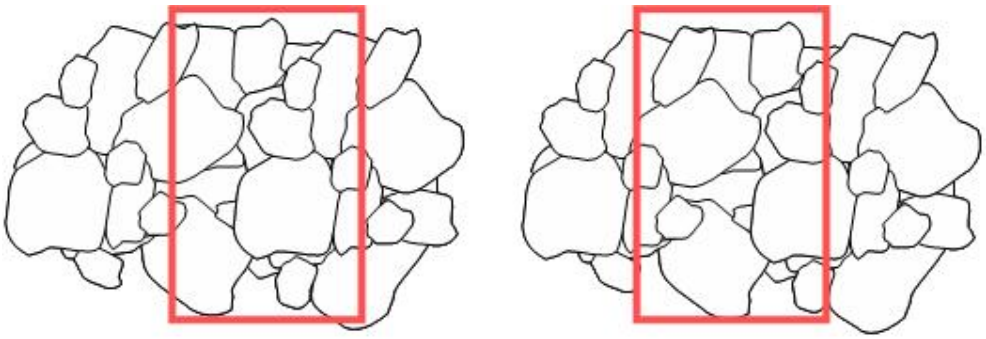


Fig. 1-2 The initial characteristics of LTPS TFTs are different from one another due to various distributions of grain boundaries

Chapter 2

I-V Mismatch Analysis

2-1. Size Effect and Interdigitated Method

2-1-1. Device Fabrication

Since the uniformity of polycrystalline TFT's is expected to be worse than that of MOS transistors qualitatively [8], the mismatching behaviors that can be observed between the electrical characteristics of equally designed devices are further analyzed by means of equally designed devices with various dimensions.

The p-channel LTPS TFTs were fabricated by the following sequence of processes and the cross section view of device is illustrated in Fig. 2-1. Firstly, a 3000Å-thick buffer oxide and 500Å-thick a-Si thin film was deposited on glass substrate. Then, the amorphous Si thin film was crystallized by KrF excimer laser annealing at room temperature. After defining the active layer, a 1000Å-thick gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400°C. A 3000Å-thick MoW thin film was then deposited at 200°C by sputtering for gate electrode. Then, the MoW thin film and gate oxide were etched to form gate electrodes. A self-aligned implantation was carried out to form the source and drain regions. Next, a 4000Å-thick oxide was deposited by PECVD as interlayer. Finally, p-channel LTPS TFTs were formed after contact-hole formation and metallization. All the devices are unhydrogenated.

In order to realize the matching properties of LTPS TFTs, the p-type differential pair devices were fabricated, shown in Fig. 2-2(a). Fig. 2-2(b) shows the layout

method corresponding to excimer laser scanning direction.

The I-V curves of the TFTs were measured using an HP 4156 semiconductor parameter analyzer. The maximum field-effect mobility was extracted from the transconductance in the linear region at Vds= -0.1V. The minimum subthreshold swing were measured at Vds = -0.1 V and the threshold voltage was defined as the gate voltage required to achieve a normalized drain current of Ids = (W/L)*10^{-8} A at Vds = -0.1 V.

2-1-2. Parameter Extraction

The purpose of this section is to introduce the definition of estimating the key parameters threshold voltage (V_{th}), field effect mobility (Muo) and subthreshold swing (S.S) from measured data obtained from the I-V characteristics, including the operation on tride and saturation region.

For most of the researches on TFT, the constant current method is widely-used to determine the threshold voltage (V_{th}). The threshold voltage in the thesis is determined from this method, which extracts V_{th} from the gate voltage at the normalized drain current $I_N = I_D/(W_{eff}/L_{eff}) = 10nA$ for V_D=0.1V.

The field effect mobility (Muo) is derived from the transconductance g_m. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si. The MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \qquad (2\text{-}1)$$

Where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If the drain voltage V_D is much smaller compared with $V_G - V_{th}$ (i.e. $V_D << V_G - V_{th}$), then the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \quad (2\text{-}2)$$

And the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D = const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D$$

Therefore, the field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \quad (2\text{-}3)$$

We can get the field-effect mobility by taking the maximum value of the g_m into (2-3) when $V_D = 0.1V$.

The subthreshold swing S.S (V/dec) is a typical parameter to describe the gate control toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. In our thesis, it is defined as the minimum value of the gate voltage required to increase drain current by one order of magnitude for $V_D = 0.1V$.

$$S.S = \left[\frac{\partial (\log I_{ds})}{\partial V_{gs}} \right]^{-1} \quad (2\text{-}4)$$

2-1-3. Size Effect Analysis

In order to realize the matching properties of LTPS TFTs, the p-type differential pair devices were fabricated. Devices with different channel widths and lengths, different layout methods, were characterized. Fig. 2-3(a)-(d) shows the

typical normalized output characteristics (i.e. W/L ratio=1) of non-passivated p-channel matching TFTs with W/L = 2 μm/2 μm, 3 μm/3 μm, 6 μm/6 μm, and 12 μm/12 μm. It is observed that the channel dimension dependence of drain current Ids. In Fig. 2-3(a), the small dimension exhibits larger output current and more serious kink effect. It is reported that the improved grain structure of the TFT's with small channel dimensions may be related to the decrease in the number of grain boundaries in the active channel of the devices [7]. Furthermore, these results reveal that the difference of output decrease with larger device size. Uncontrolled variations tend to become dominant at small device sizes. They require device or circuit designs that improve uniformity.

The electrical characteristic data, such as threshold voltage, field-effect mobility, and subthreshold swing which were further identified in the next section, were taken down and statistically analyzed. The impact of the random grain size variation to the device characteristic variation in different layout method will be discussed.

2-1-4. Interdigitated Layout Method and Analysis

With the parameter extraction of threshold voltage, field-effect mobility, and subthreshold swing identified in the previous section, the impact of the mismatch effect to the device characteristic in different layout method could be observed. Fig. 2-4 shows another layout method of interdigitated arrangement [8]. Devices of different layout methods, with different channel widths and lengths were measured and characterized. In the electrical characteristic data, each point is calculated from a mean value of five pairs of matching TFTs.

The threshold voltage difference of conventional arrangement and interdigitated arrangement matching TFTs with different channel widths and channel lengths are

plotted in Fig. 2-5(a) and Fig. 2-5(b). The threshold voltage is mainly dependent on the grain boundaries. The grain boundaries cause dangling bonds and traps which lead to high energy barrier for the channel conducting. The threshold voltage difference order is around 0.03V-2V in conventional arrangement and 0.02V-0.15V in interdigitated arrangement. It is clear that threshold voltage difference of interdigitated arrangement smaller than the original arrangement. Furthermore, the small TFTs suffer larger threshold voltage difference than large ones. The large contribution of threshold voltage variations suggests that circuit and device design using small TFTs must be more variation-tolerant.

Concerning field-effect mobility, manufacturers are primarily concerned with higher mobilities at the driver area in order to squeeze in all the required circuitry within the narrow pixel pitch as well as to integrate more circuitry. Field-effect mobility performance is closely tied to the grain size and grain crystallinity. Since the defect traps place a profound influence on electrical characteristics of LTPS TFTs, the mobility difference issue is essential. Fig. 2-6(a)-(b) shows the field-effect mobility difference between matching TFTs with different channel widths and channel lengths. In general, the field-effect mobility difference ranges from $0.04cm^2/V*s$ to $2.4cm^2/V*s$ of the original arrangement and from $0.07cm^2/V*s$ to $2.2cm^2/V*s$ of the interdigitated arrangement.

Fig. 2-7(a)-(b) summarizes the subthreshold swing difference between matching TFTs with different channel widths and channel lengths. The subthreshold swing difference seems to be irrelevant to active region dimensions. In general, the devices with small dimension exhibit small subthreshold swing due to less interface traps density. However, the devices with smaller dimension have a higher chance to encounter many grain boundaries or a few ones leading large subthreshold swing difference. In general, the subthreshold swing difference ranges from 0.5mV/dec to

78.5 mV/dec of the original arrangement and ranges from 5 mV/dec to 52.5 mV/dec of the interdigitated arrangement. In other words, most subthreshold swing difference range from 5 mV/dec to 30 mV/dec. Since the differences are too small to be considered in comparison with the ordinary value of the subthreshold swing, only the threshold voltage and the filed-effect mobility are observed and analyzed in our study.

Fig. 2-8(a)-(b) shows the mismatching factor related to active area. The mismatching factor is defined as the difference between maximum value and minimum value, divided by the average absolute value. From these plots, the worst situation always happened on small active area in different electrical characteristics and layout methods. The worse mismatching factor is around 0.2 (20% mismatch) in device characteristics, and the usual mismatching factor is around 0.05 (5% mismatch) in device characteristics. It is observed that the interdigitated arrangement has better tolerance than the original arrangement in electrical data statistically of matching TFTs. This is because the grain structure after excimer laser irrdiation is polygon-like but not stripe-like. The corresponding grain boundaries with the current flow are randomly located in the channel.

So far it is observed that the mismatching factor decreases rapidly with the increase of the device's area, and the interdigitated arrangement has better performance than the original one. In particular, the mismatching factor seems to be irrelevant while the device's area are larger than 100 cm^2, which means that the size effect are less obvious than small-size device. In current applications, small size TFTs are seldom used. In order to further confirm the mismatching effect for large area TFTs, nominally identical devices with width/length dimension of 20μm / 5μm are fabricated with a special layout and measured.

2-2. Introduction to crosstie TFTs and Statistical Method

2-2-1. Introduction to Crosstie TFTs

Although the size effect on mismatching properties are observed and evaluated by applying the various sizes of differential pairs, it is not proper for statistical analysis. To further investigate the mismatching properties of the interdigitated arrangements, a huge number of devices with the same dimension are necessary. In addition, the variation factors in LTPS TFTs needs to be considered to evaluate the mismatching property more precisely.

In prior studies, it is known that LTPS TFTs suffered from severe device variation even under well-controlled process. Since the device variation is inevitable in LTPS TFTs, it is essential to classify the sources of variation. In MOSFETs (Metal-Oxide-Silicon Field Effect Transistors), the local variations can be characterized by short correlation distances and global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performances. If this distance is lower than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g. a charge trapped in the gate oxide layer). For the global variation, which is characterized by process disturbances with longer correlation distances (e.g. the gate oxide thickness across the wafer surface), affects all the devices within a defined region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other.

In order to investigate the relationship between mismatching issue and device distance, a special layout of the devices adopted in this work is shown in Fig. 2-9. The red, blue and yellow regions respectively represent the polysilicon film, the gate metal and the source/drain metal. The structure of the poly-Si film and the gate metal are in

the order that resembles the crosstie of the railroad and therefore this layout is called the crosstie type layout of LTPS TFTs. The distance of two nearest active regions is equally-spaced 40μm. The global variation may be ignored within this small distance, and the variation of device behavior can therefore be reduced to only local variation. For this reason, we can find out the relationship between the variation behaviors and the distance of mutual devices by adopting the crosstie layout TFTs.

2-2-2. Device fabrication

Top gate LTPS TFTs with width/length dimension of 20μm / 5μm were fabricated using low temperature process. The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates, and then XeCl excimer laser was used to crystallize the a-Si:H film, followed by poly-Si active area definition.

Subsequently, a gate insulator was deposited. Next, the metal gate formation and source/drain doping were performed. A lightly doped drain (LDD) structure was used on the n-type devices, while self-align structure was used on p-type ones. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. The Fig. 2-10 shows the schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain (LDD).

2-2-3. Statistical Method

It is reported that the averages of parameters differences stand for global variation of LTPS TFTs, while the standard deviation of parameter differences shows the local variation in the devices. In prior art [9], the averages of the differences of

these parameters show different behaviors, they still appear in linear form. On the other hand, the effects of variation in a range are still minor than those of the micro variation under short device distance. Since the variation in a long range is not our concern because the distance between two devices will not be too long for the crosstie layout. A good place to start is analyzing the distribution of the differences of these parameters.

Since the crosstie devices queues as a row with narrow distance of 40um, it can be used for statistical method to analyze the mismatch effect. In this study, the crosstie devices are interdigitated with different numbers of fingers. In order to compare the performance of the interdigitated pairs and the original ones, the value of the drain currents within the same pair are summed together and extracted to acquire the two parameters of threshold voltage and mobility. To further confirm the matching properties of the interdigitated pairs, the crosstie devices could be interdigitated not only with different number of fingers, but also with different distance of fingers. By employing various arrangements of the interdigitated pairs, the property of mismatch effect can be further analyzed and evaluated.

2-3. I-V Mismatch Analysis with interdigitated method

2-3-1. Interdigitated Analysis

The purpose of this section is to present the results and the descriptions of statistical methods applied to evaluate the mismatching properties of crosstie TFTs, which are divided into two sets for the p- and the n- channel devices. In order to evaluate the performance of the interdigitated pairs, more than 130 crosstie devices are measured and interdigitated statistically with different pairs as illustrated in Fig. 2-11. According to the device's parameters from the measured data, the distributions

of the two device parameters' differences including threshold voltages and mobilities are observed. The sample means and standard deviations of each distribution for various kinds of interdigitated methods are examined.

Fig. 2-12 (a)-(c) shows the distribution of △Vth in both original and interdigitated of n-type devices. We examined the interdigitated device with different number of fingers, which means the number of device within one interdigitated pair. In Fig. 2-12(a), the threshold voltage's difference of original devices spread out as Gaussian distribution, whose mean value and standard deviation are -0.025mV and 0.020V individually. In the case of interdigitated method, the distributions are still Gaussian with the mean value of 0.05mV and 0.017mV, as shown in Fig. 2-12(b)-(c). However, the standard deviation of one-finger and two-finger interdigitated devices decrease linearly with the value of 0.013V and 0.010V. Observing the decrease of standard deviation, it is not too far to say that the interdigitated method is able to suppress the mismatch effect with the increase of finger numbers.

Since the interdigitated method shows superior properties on △Vth parameter in n-type devices, the performances on △Muo are intended to be examined. The diatribution of △Muo, in each finger group, are shown in Fig. 2-13 (a)-(c). In the three distributions the mean values of -0.0146 $cm^2/V*s$, -0.0037 $cm^2/V*s$, and -0.0126 $cm^2/V*s$, are very close to zero, while the standard deviation shows more apparent difference with the value of 1.929 $cm^2/V*s$, 1.243 $cm^2/V*s$ and 0.857 $cm^2/V*s$. As far as the standard deviation is concerned, the interdigitated method of one-finger has better performance than the original one, and the two-finger are still superior than one-finger.

From the characteristics of n-type devices, it could be observed thatvthe mean values of △Vth and △Muo approach zero very closely and almost have no tendency. Therefore, in the case of p-type device standard deviations of △Vth and △Muo are

especially examined. In Fig. 2-14(a)-(c) and Fig. 2-15(a)-(c), standard deviations of the original and interdigitated devices are 0.062V, 0.047V, 0.039V for △Vth and 2.267 cm^2/V*s, 1.851 cm^2/V*s, 1.438 cm^2/V*s for △Muo, which reveal the similar properties as those of n-type devices.

Up to know, it is not too far to say that the interdigitated method has better tolerance to mismatch effect than the original ones. For both △Vth and △Muo in n-type and p-type devices, standard deviations decrease with as finger number increases. However, the decreasing tendency seems to be gentler when it comes to two fingers. In order to investigate the saturating point, interdigitated methods with more fingers as illustrated in Fig. 2-16, would be necessary.

The distribution of △Vth on both n-type and p-type, in each finger-number group, are shown in Fig. 2-17 (a)-(b). The line across the middle represents zero, and the middle line in each of the diamond is the response group mean. The vertical endpoints of each diamond form the 95% confidence interval for the mean, and the x-axis is divided by group of finger numbers. The figure clearly shows that as the finger number increase, the distribution of △Vth concentrates and the standard deviation decreases both in n-type and p-type devices. There is further indication that as the finger number increases, the mean of the △Vth decreases as well. In addition, the distributions of △Muo shows the same properties in both n-type and p-type devices as shown in Fig. 2-18 (a)-(b). Therefore, this analysis has achieved its goal by showing the influence of finger numbers of interdigitated method on the mismatch effect.

In order to look further into the influence of finger numbers on the interdigitated devices delicately, the standard deviations of △Vth varying with finger number are plotted in Fig. 2-19(a)-(b) for both n-type and p-type. Concerning △Vth in Fig. 2-19 (a), it is obvious that the standard deviation is inversely proportional to

finger number and begins to saturate on eight fingers[10]. The △Vth of p-type devices reveal the similar characteristics as shown in Fig. 2-19(b). Since the standard deviations of △Vth have great properties of inverse proportionality with finger numbers, proposing a model would be desired to predict the performance :

$$y = a \times \exp\left(-\frac{x}{b}\right) + y_0 \qquad (2\text{-}5)$$

the values of certain parameters (a, b, y_0) are disclosed :

	a	**b**	**y_0**	**R^2**
△Vth_N type	0.05775	1.4777	0.0323	0.99964
△Vth_P type	0.02915	1.2446	0.0073	0.99883
△Muo_N type	2.9284	1.2179	0.6468	0.99282
△Muo_P type	2.1063	2.1657	0.9534	0.97796

As shown in Fig. 2-19(a)(b), the values of R^2 are 0.99964 and 0.99883 for n-type and p-type devices, which is evident that the models presented are able to fit the data accurately. However, in the case of △Muo as shown in Fig. 2-20(a)(b), the R^2 values are lower than those of △Vth. In other words, the standard deviations of △Muo are still inversely proportional to finger numbers but not so exactly as the case in △Vth.

However, the predictive models have clearly indicated that there is practical limit to finger numbers as far as the enhancement of matching accuracy is concerned. As shown in Fig. 2-19 and Fig. 2-20, the predictive models for the standard deviation of △Vth and △Muo have nonzero intercept. Concerning the interdigitated devices of few fingers, only minute local process variations, and not global variations, affect

them since they are within the same region. As finger number increases the local variation is uniformly spread and the devices are affected equally, thus the mismatch effect decreases. However, if the finger number increases so much that not only the local variation is involved, but the global variation also comes into play. This additional variation will impede the further decrease of the mismatch. In fact, at some point the mismatch would stop decreasing when the global process variation is in full control of the two devices.

2-3-2. Distance Analysis

Up to now, we have analyzed the mismatch effect on interdigitated devices of different number but same distance. In the section, devices with the same finger number but different distance ranging from 40 um to 8000 um, which means the distance between two different interdigitated pairs as illustrated in Fig. 2-21, are investigated.

In order to analyze the mismatch effect with distance, both the mean value and standard deviation of △Vth and △Muo are examined with distances of 40um, 200um, 2000um, 4000um and 8000um. Fig. 2-22(a)(b) summarize the mean and standard deviation of n-type devices. Concerning these two parameters, the mean value and standard deviation of △Vth slightly increase after 2000um, while those of △Muo decrease after 4000um. However, taking the whole range from 40um to 8000um into consideration, no apparent characteristics could be observed. Besides, in case of p-type devices as plotted in Fig. 2-23(a)(b), the two parameter seems to be irrelevant to the distance.

While analyzing the graphs in Fig. 2-22 and Fig. 2-23, it could not too far to say that there are almost no correlations between the distance and mismatch effect.

The global variation comes into influence when the distance is far enough, but the local variation effect regardless of the distance. When employing the interdigitated method, increasing the finger number would be more effective than distance to suppress the mismatch effect. Nevertheless, it could be inspiring that getting device as close as possible in device layout is not necessary, since the mismatch effect is irrelevant to distance.

2-4. Summary

Size Effect Analysis

- Device with small dimension contains less grain boundaries, which contributes worse mismatch effect.
- Interdigitated arrangement has better tolerance than original ones, especially in larger area.

Interdigitated Effect Analysis

- The interdigitated method are indeed superior than the original in Vth, Muo.
- Most parameters are inversely proportional to the number of fingers, especially the threshold voltage.
- A model is proposed to predict the performance of the interdigitated method.

Distance Effect Analysis

- Almost no correlations between the distance and mismatch effect could be observed.

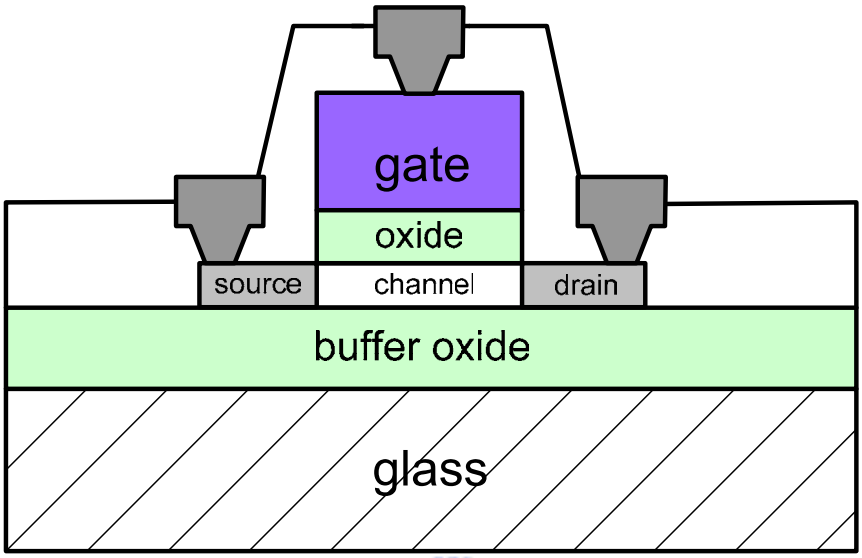
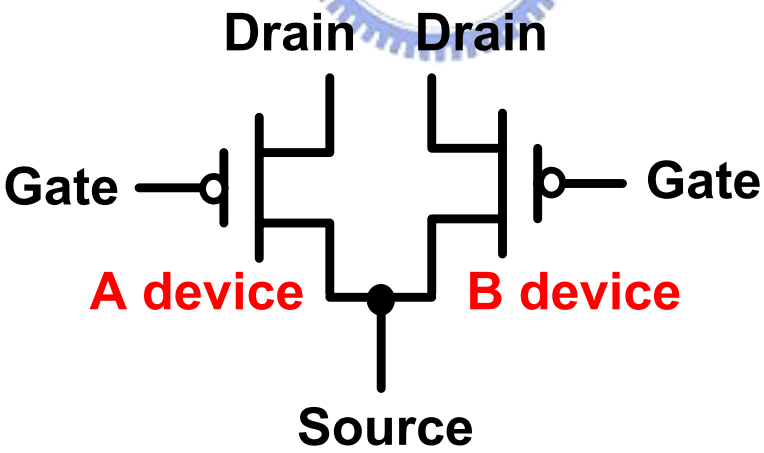


Fig. 2-1. Self-aligned LTPS-TFT's cross section view



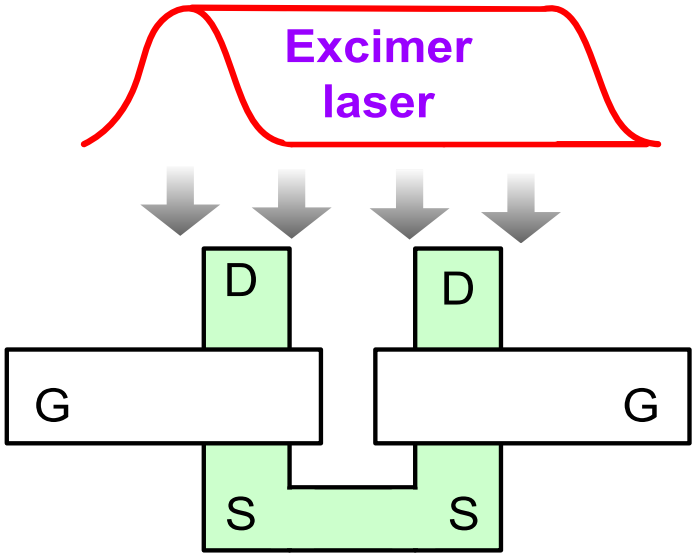
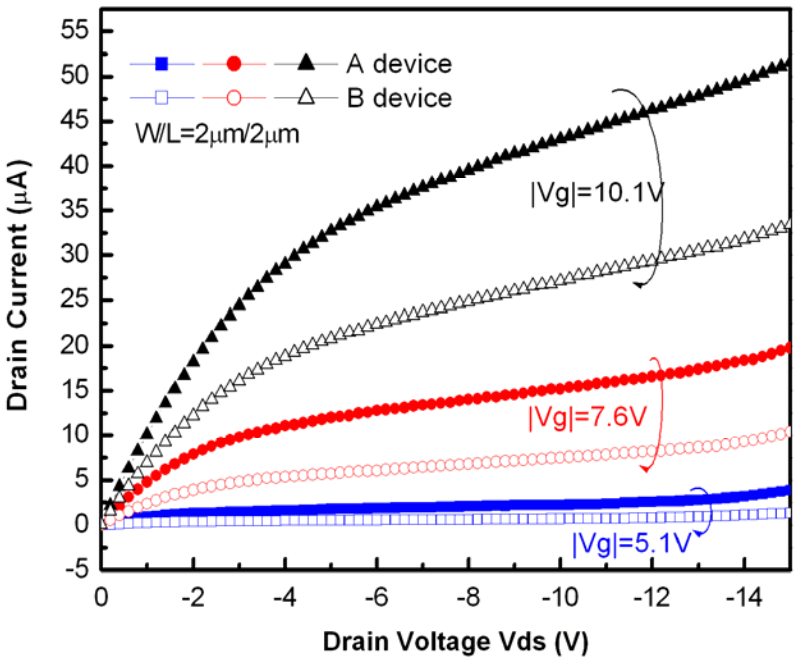
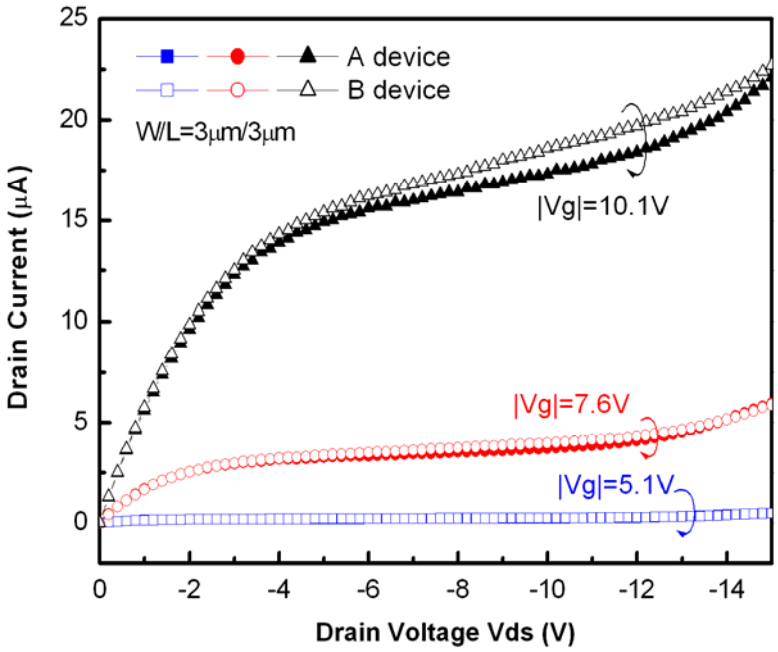
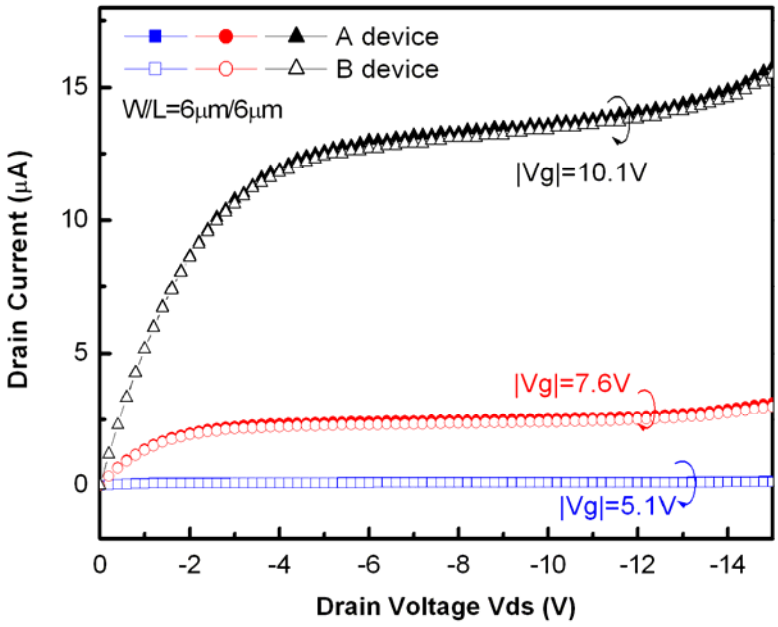


Fig. 2-2. (a) The differential pair circuit, (b) Perpendicular arrangement layout method corresponding to excimer laser scanning direction of matching TFTs




A device
B device
W/L=3μm/3μm
|Vg|=10.1V
|Vg|=7.6V
|Vg|=5.1V
Drain Current (μA)
Drain Voltage Vds (V)
25
20
15
10
5
0
0
-2
-4
-6
-8
-10
-12
-14


A device
B device
W/L=6μm/6μm
|Vg|=10.1V
|Vg|=7.6V
|Vg|=5.1V
Drain Current (μA)
Drain Voltage Vds (V)
15
10
5
0
0
-2
-4
-6
-8
-10
-12
-14

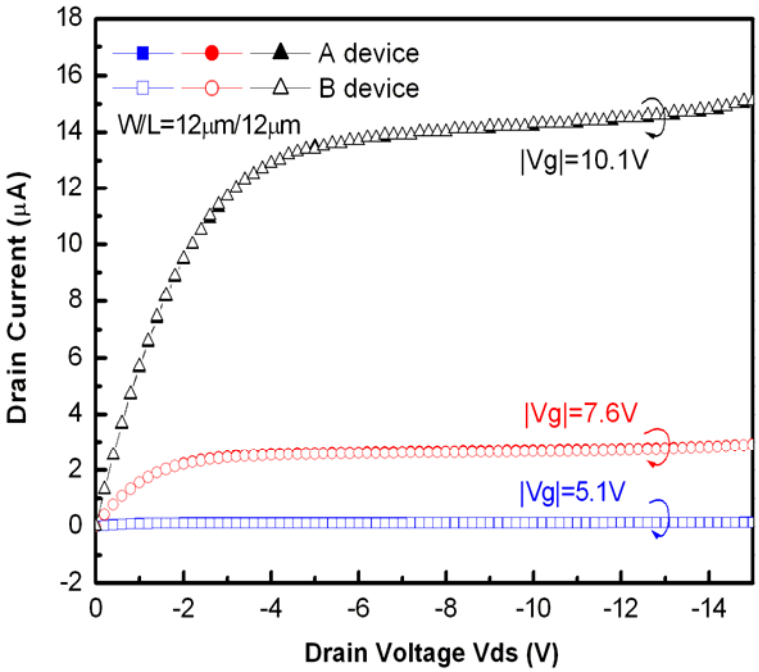


Fig. 2-3. Normalized output characteristics (i.e. W/L ratio=1) for non-passivated p-channel matching TFTs with (a)W/L = 2 μm/2 μm, (b)3 μm/3 μm, (c)6 μm/6 μm, and (d)12 μm/12 μm. The small dimension exhibits larger output current and more serious kink effect.

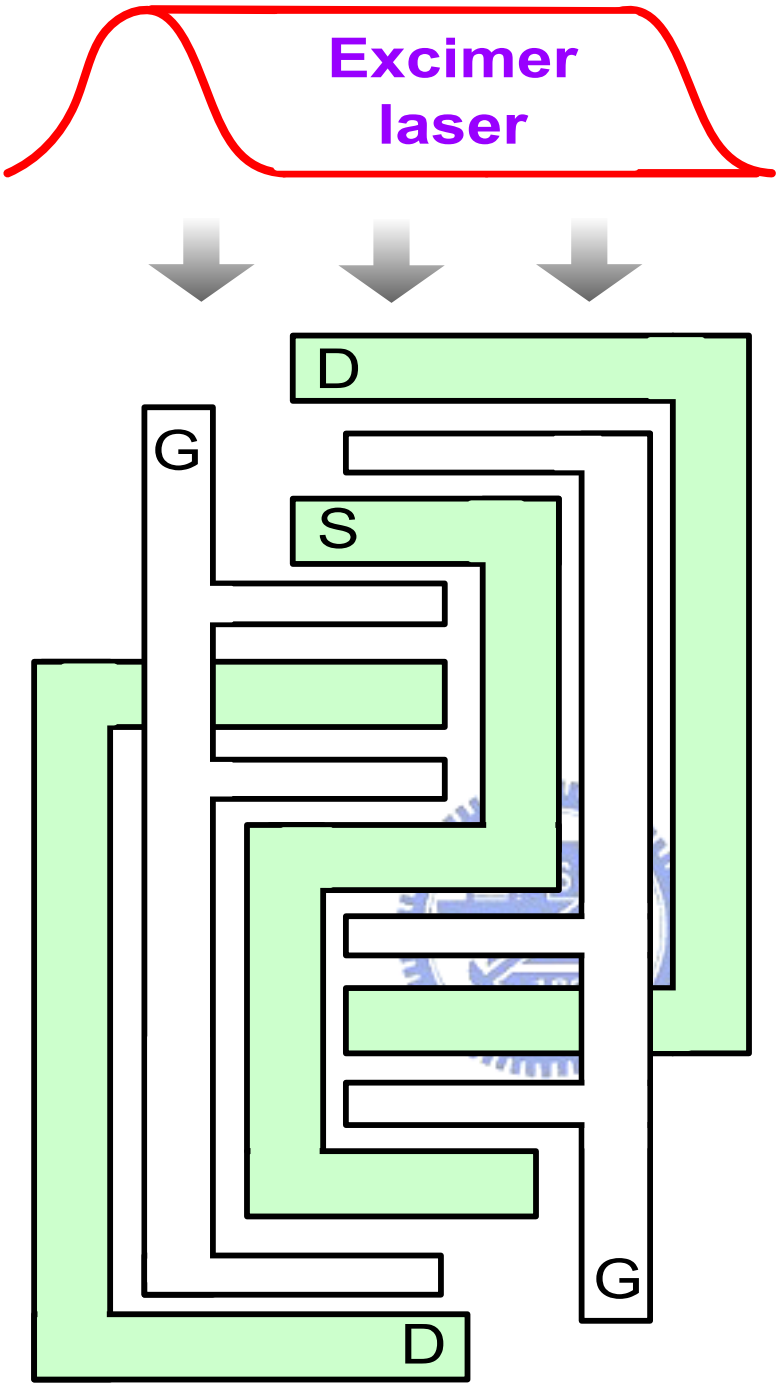


Fig. 2-4. Interdigitated arrangement layout method corresponding to excimer laser scanning direction of matching TFTs

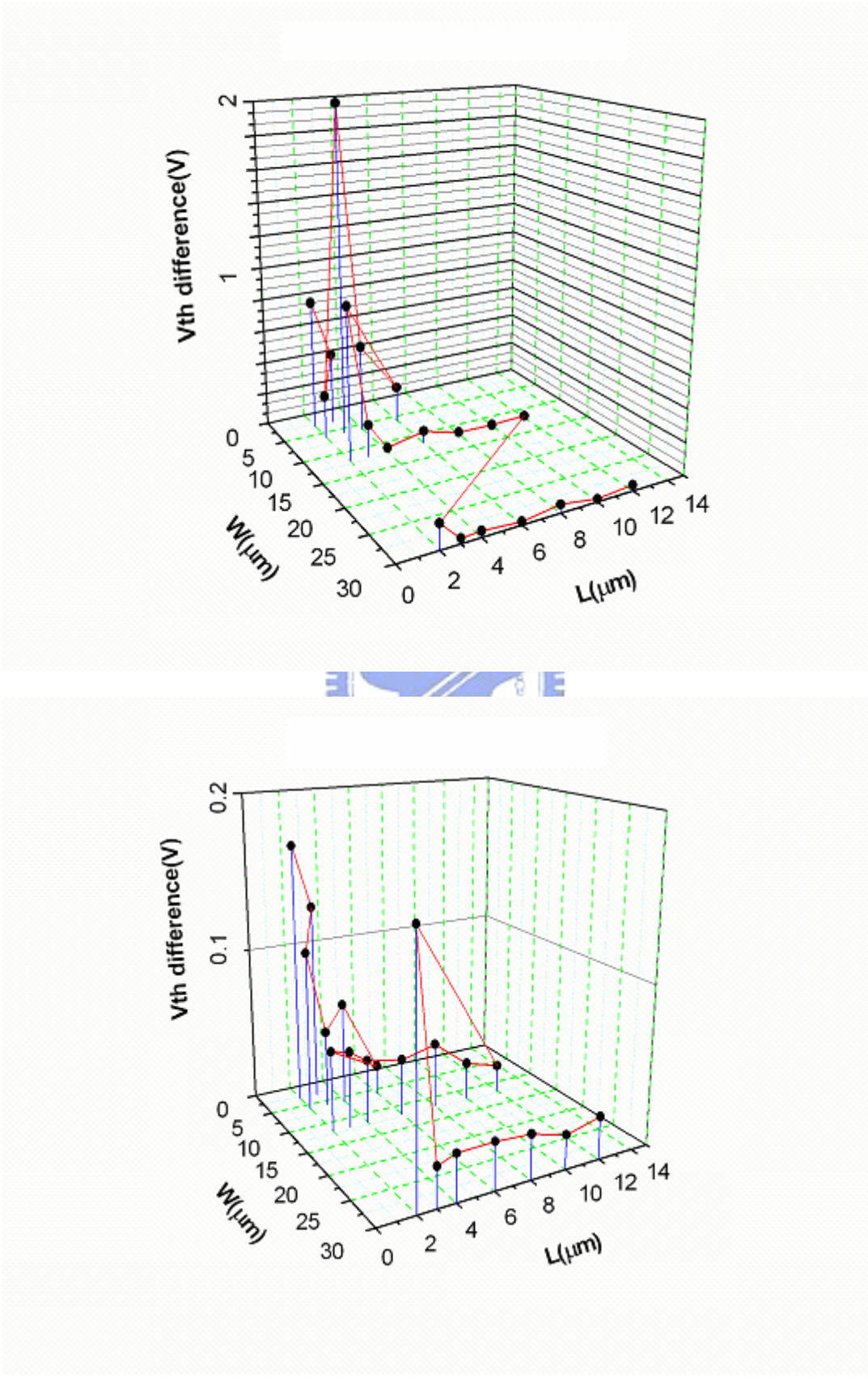
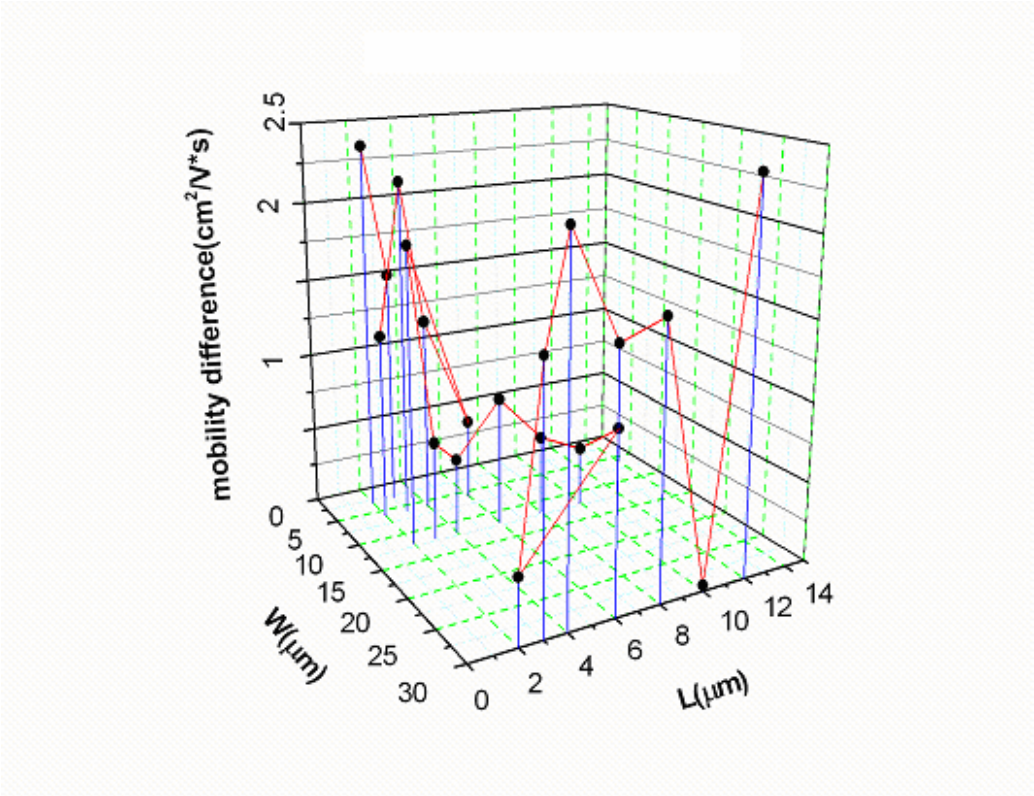


Fig. 2-5. Threshold voltage difference between different layout methods of matching

TFTs with different channel widths and channel lengths (a) original arrangement, (b) interdigitated arrangement



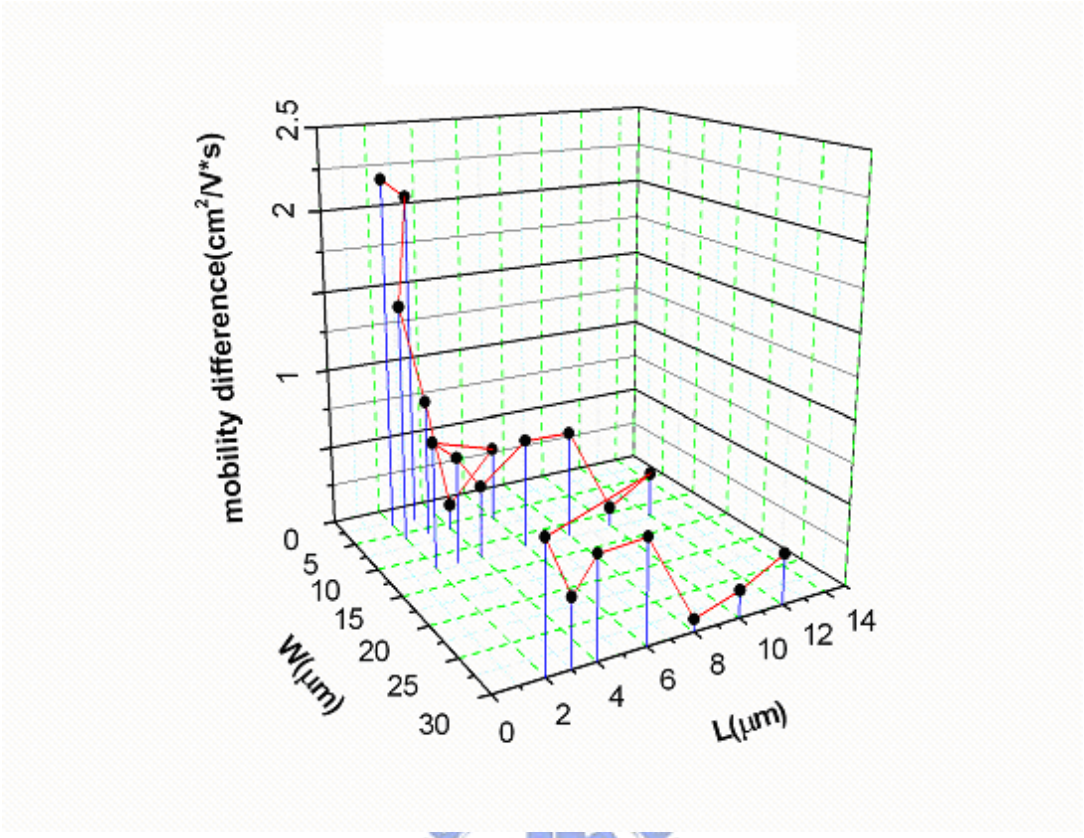


Fig. 2-6. Field-effect mobility difference between different layout methods of matching TFTs with different channel widths and channel lengths (a) original arrangement, (b) interdigitated arrangement

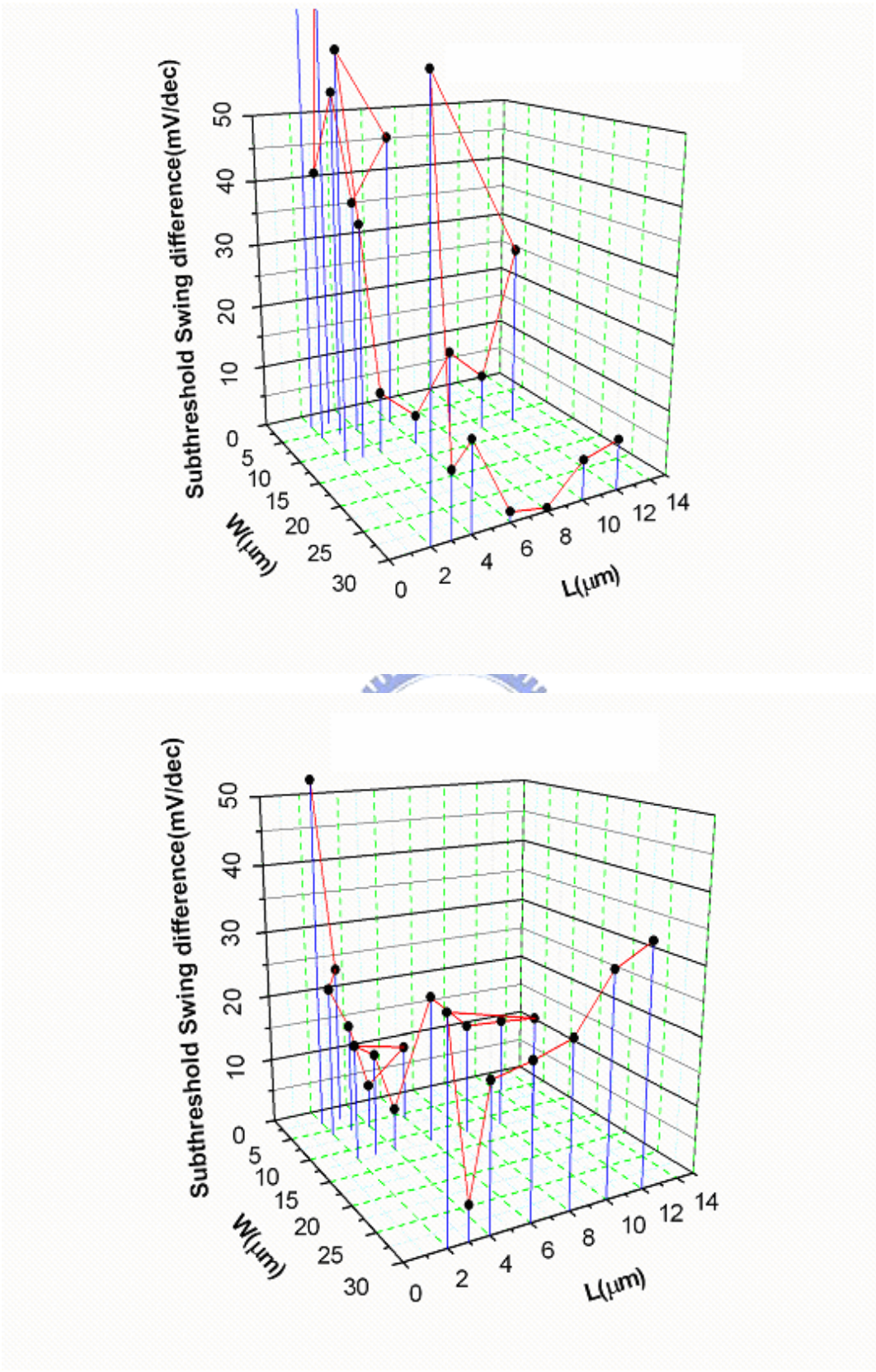


Fig. 2-7. Subthreshold swing difference between different layout methods of matching TFTs with different channel widths and channel lengths (a) original arrangement, (b)

interdigitated arrangement

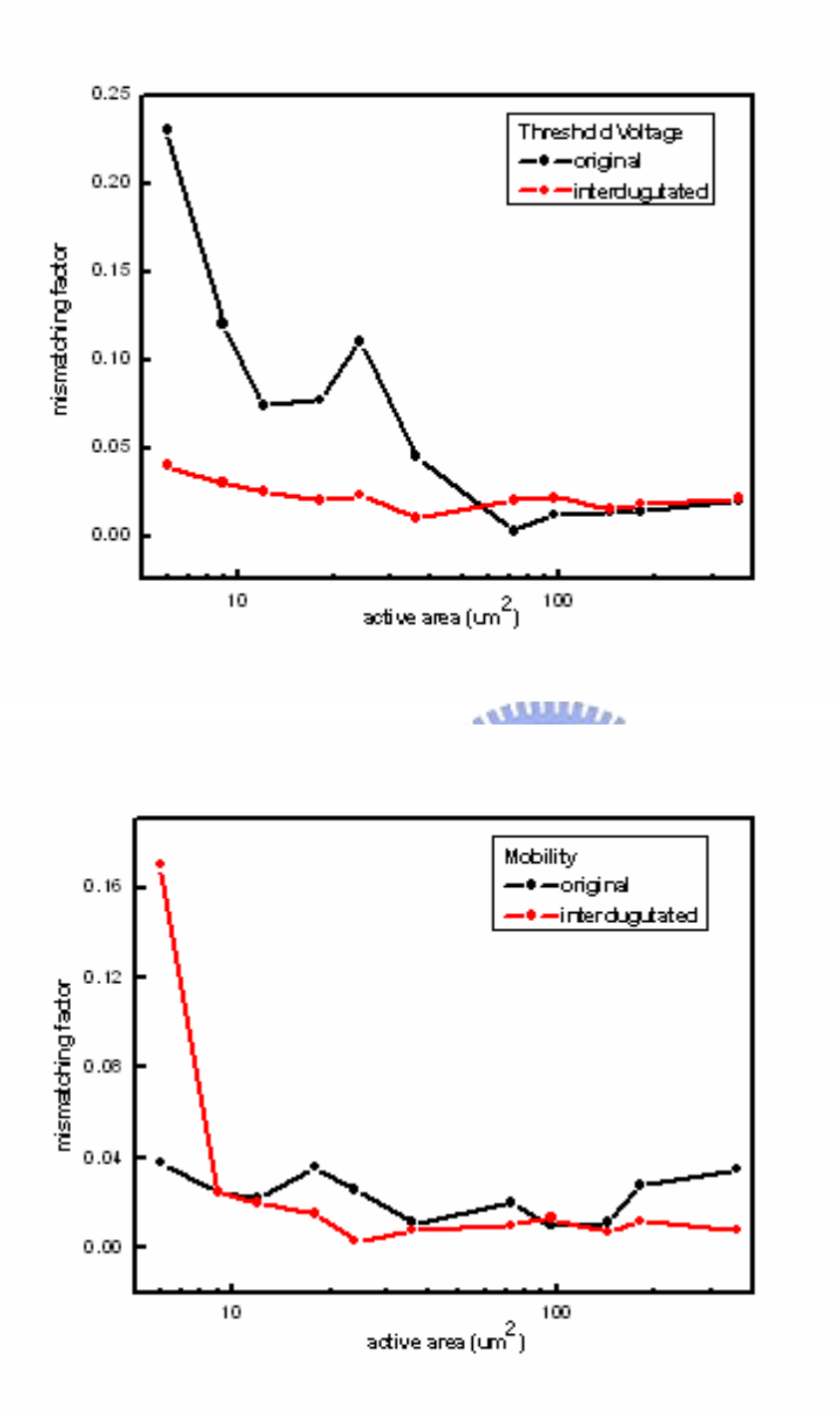


Fig. 2-8. (a) threshold voltage, (b) field-effect mobility, from p-channel LTPS TFTs with different active areas. The worse mismatching factor is around 0.2 (20% mismatch) in device characteristics, and the usual mismatching factor is around 0.05 (5% mismatch) in device characteristics.

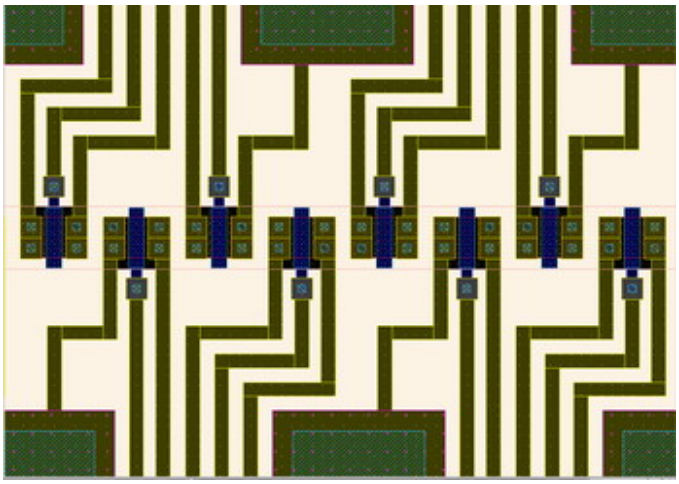


Fig. 2-9. The layout of the crosstie TFTs

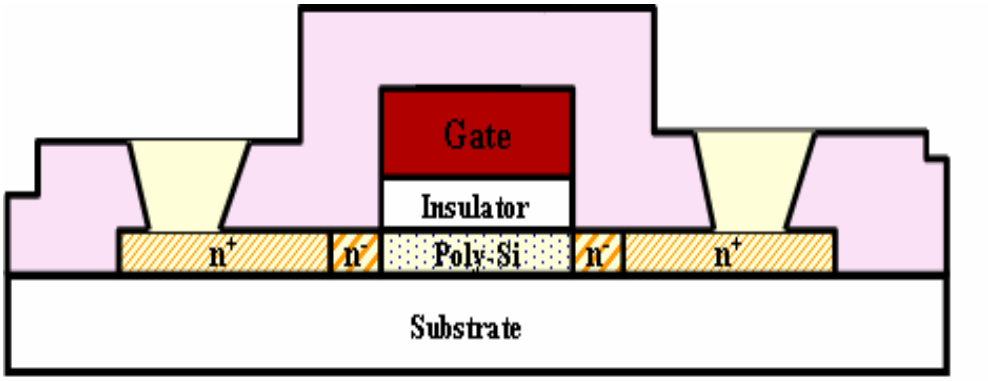


Fig. 2-10. The schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain

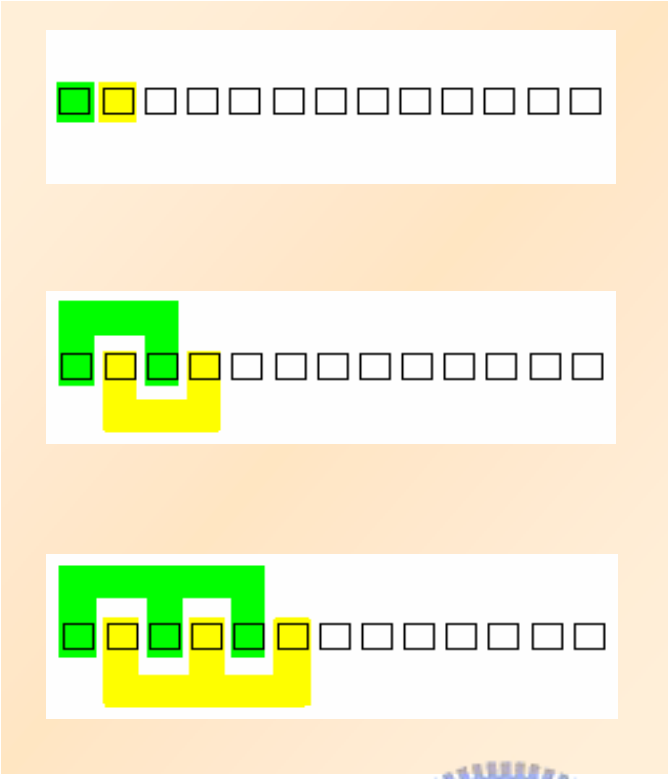
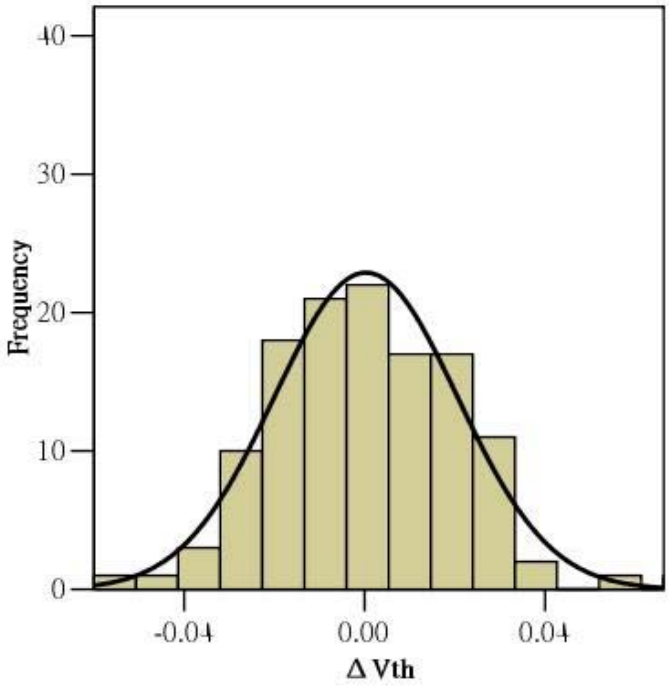


Fig. 2-11. Illustration of the interdigitated method of the crosstie device



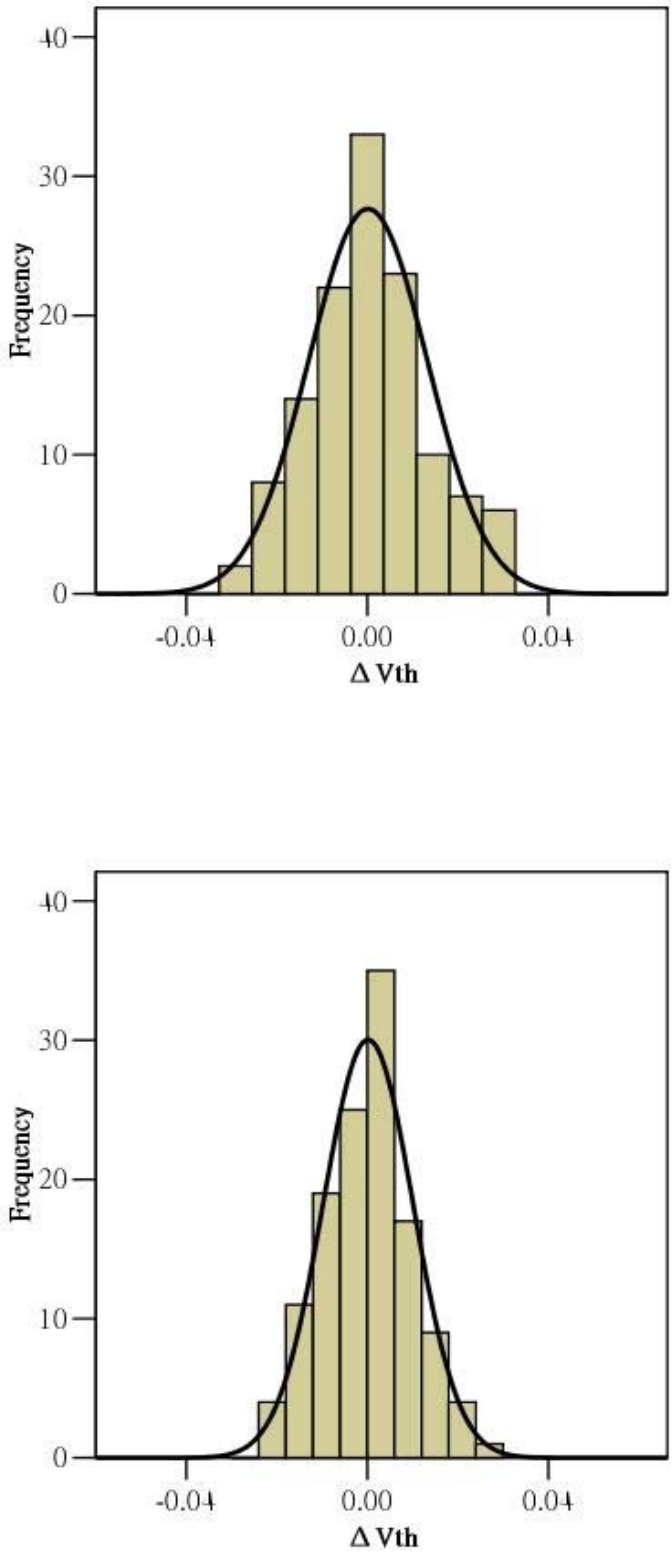
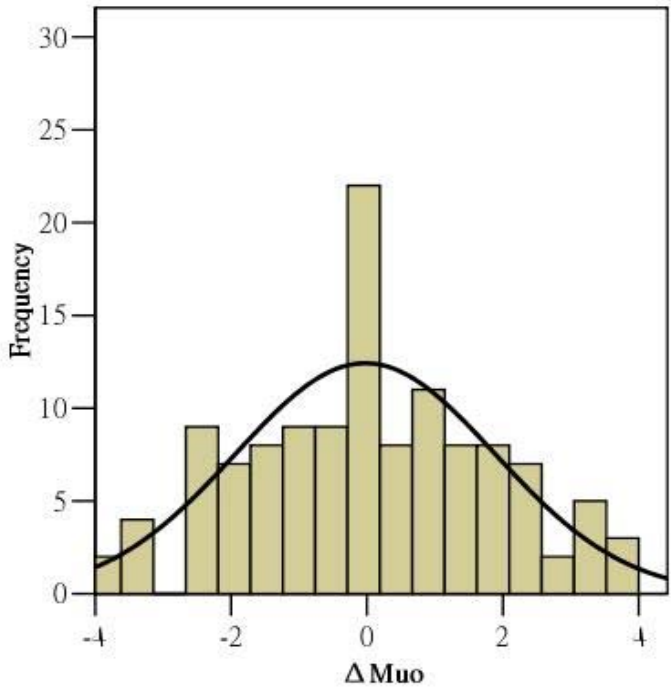
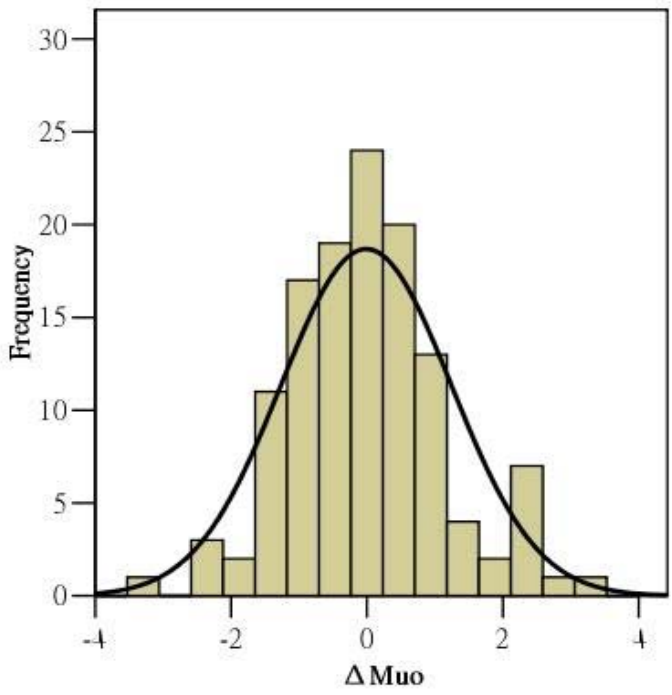


Fig. 2-12 N-type device distributions of threshold voltage difference between original and the interdigitated methods (a) the original devices (b) interdigitated method of

one-finger (c) interdigitated method of two-finger





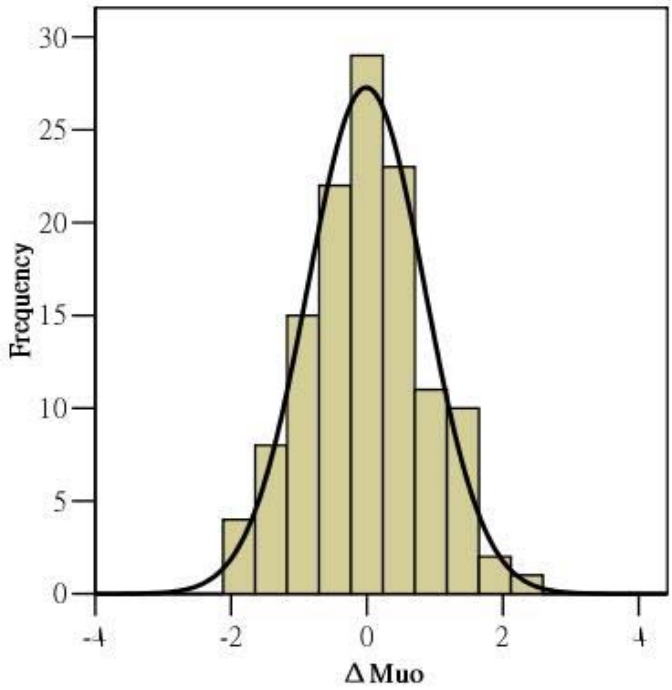
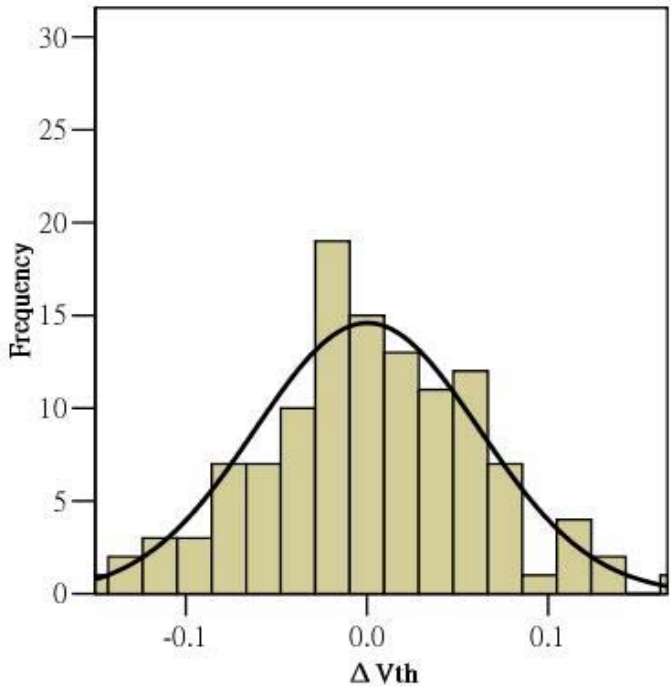
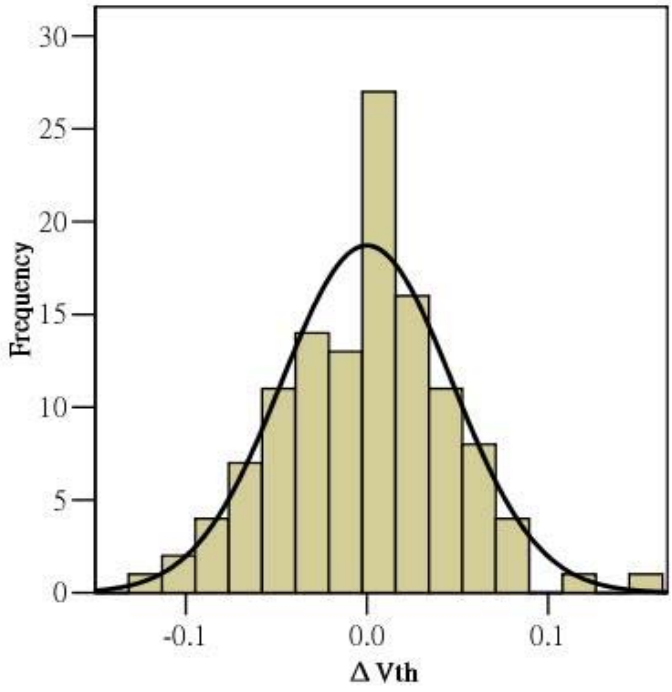


Fig. 2-13 N-type device distributions of mobility difference between original and the interdigitated methods (a) the original devices (b) interdigitated method of one-finger (c) interdigitated method of two-finger


30
25
20
15
10
5
0
Frequency
-0.1
0.0
0.1
Δ Vth


30
25
20
15
10
5
0
Frequency
-0.1
0.0
0.1
Δ Vth

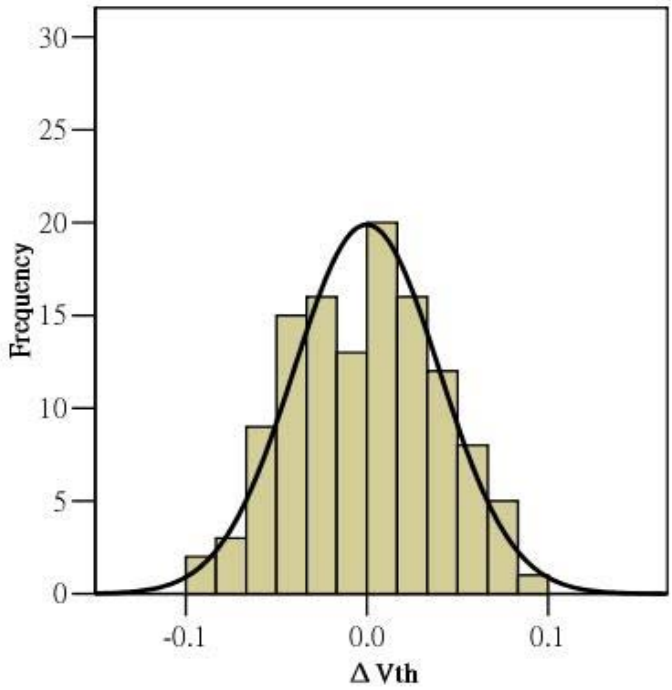
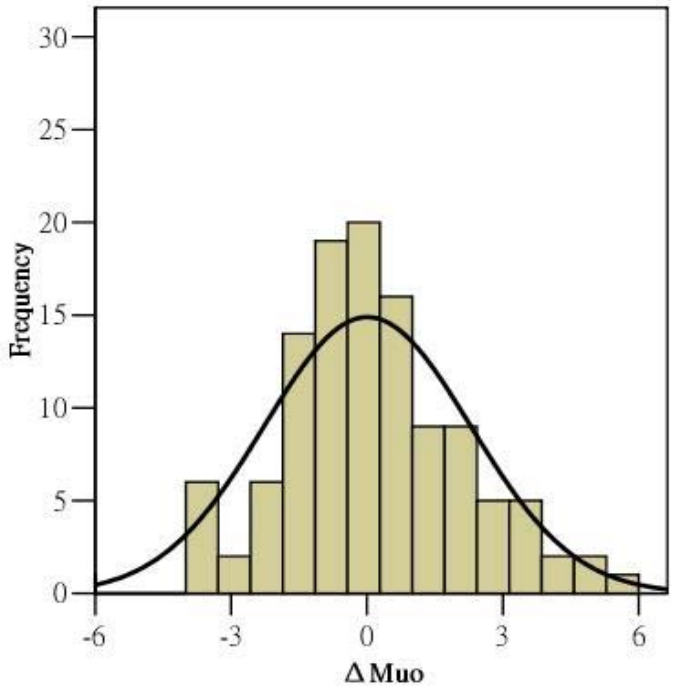
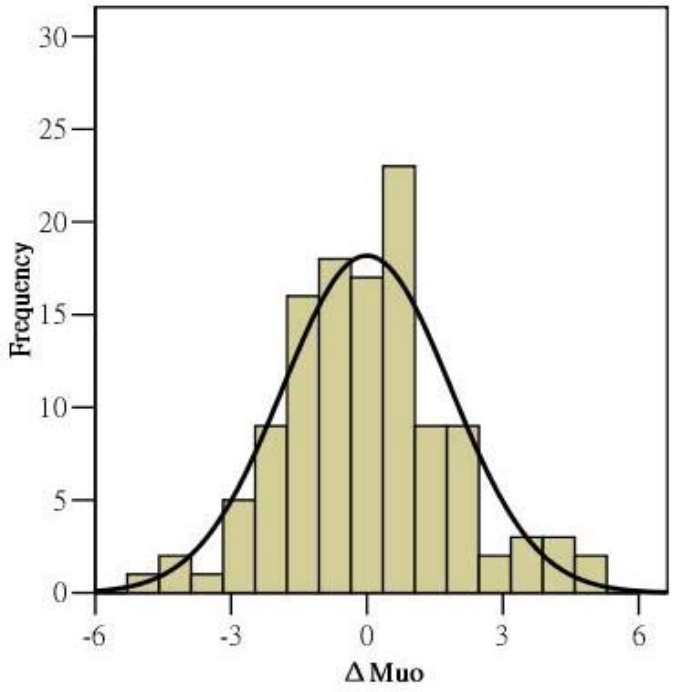


Fig. 2-14 P-type device distributions of threshold voltage difference between original and the interdigitated methods (a) the original devices (b) interdigitated method of one-finger (c) interdigitated method of two-finger


30
25
20
15
10
5
0
Frequency
-6
-3
0
3
6
Δ Muo


30
25
20
15
10
5
0
Frequency
-6
-3
0
3
6
Δ Muo

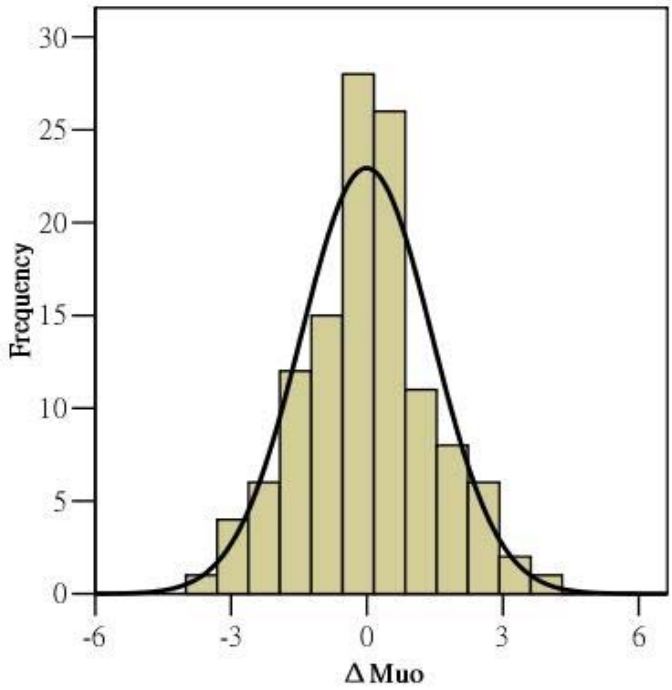


Fig. 2-15 P-type device distributions of mobility difference between original and the interdigitated methods (a) the original devices (b) interdigitated method of one-finger (c) interdigitated method of two-finger

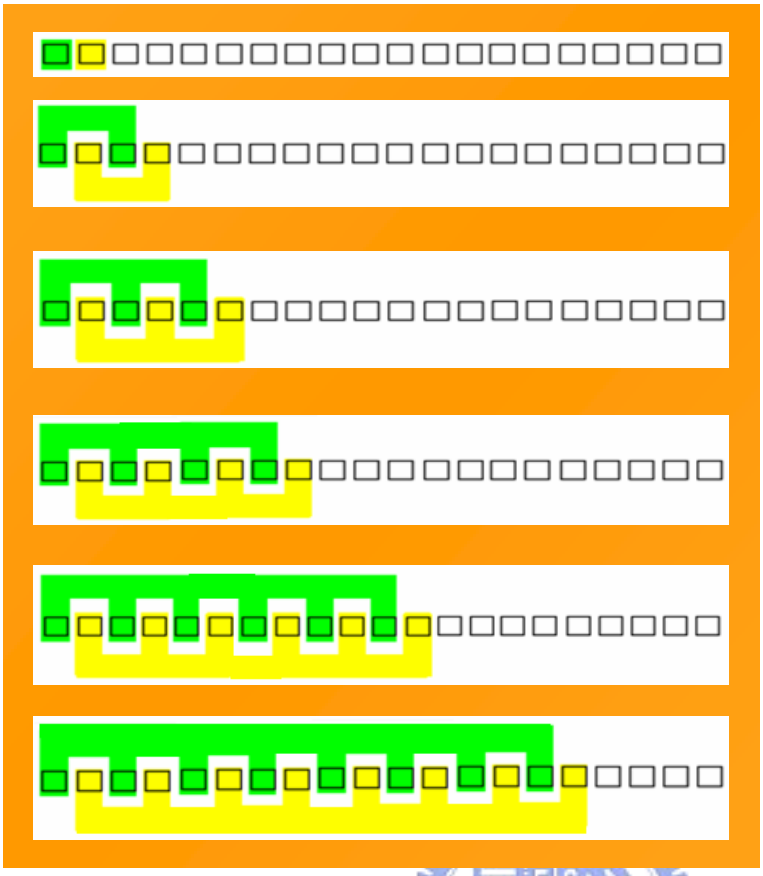
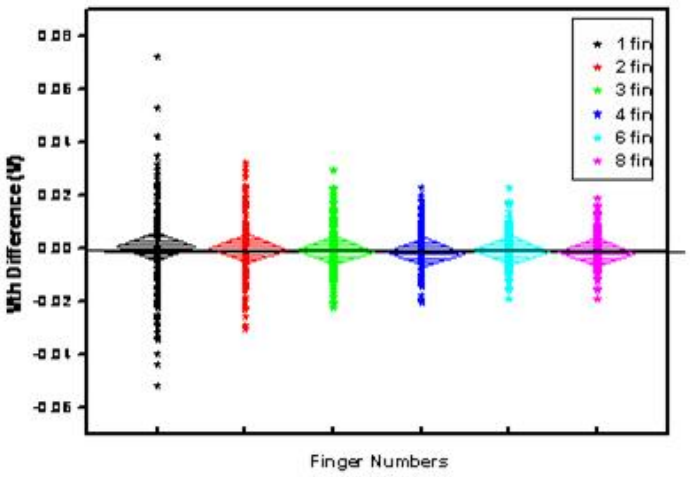


Fig. 2-16 Illustration of the interdigitated method of the crosstie device with more fingers.



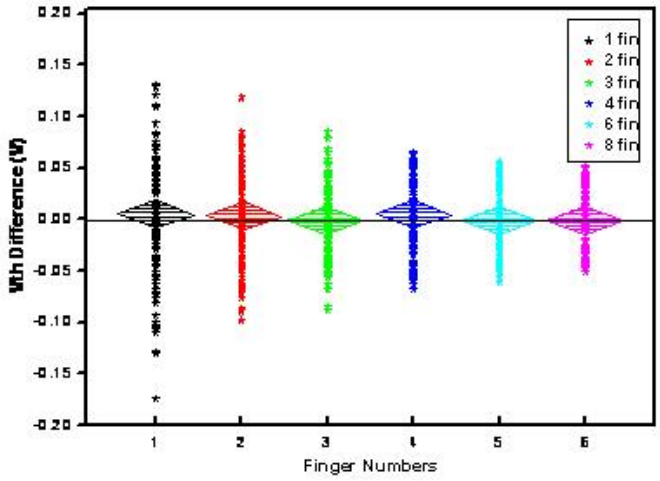
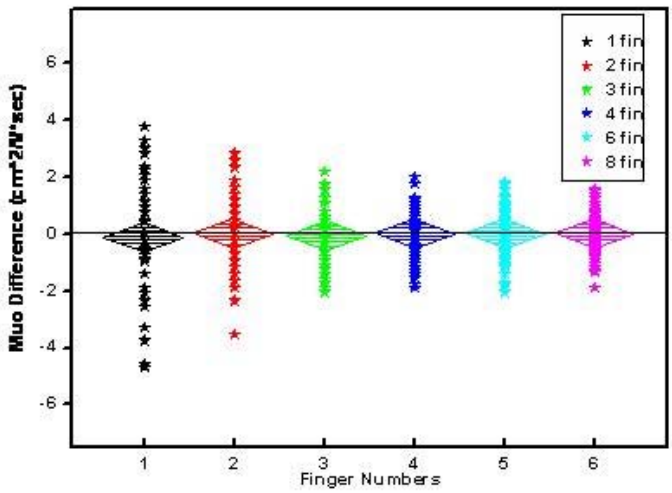


Fig. 2-17　Distribution of △Vth with different number of fingers (a) n-type devices (b) p-type devices



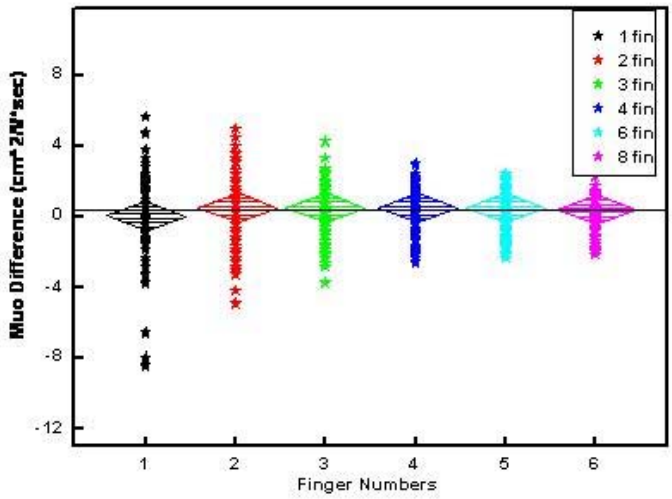
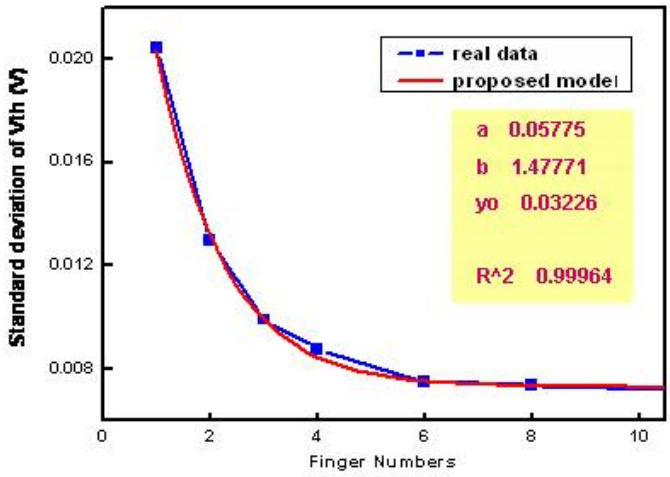


Fig. 2-18 Distribution of △Vth with different number of fingers (a) n-type devices (b) p-type devices



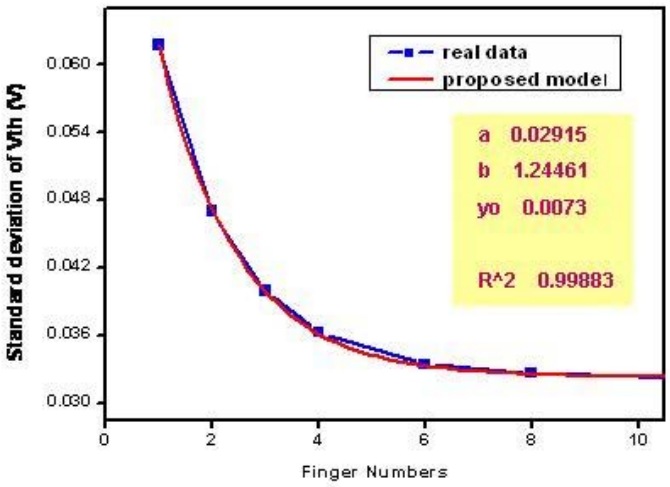
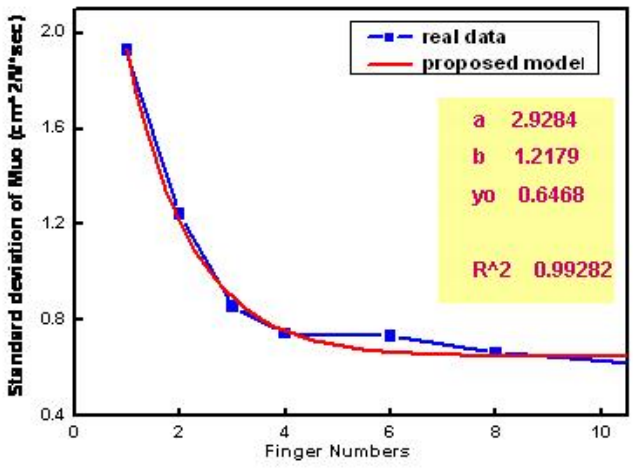


Fig. 2-19 Standard deviation of △Vth with proposed model (a) n-type deives (b) p-type devices



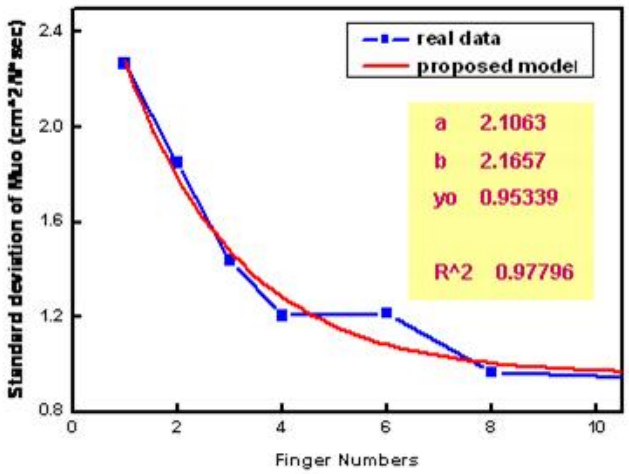


Fig. 2-20 Standard deviation of △Muo with proposed model (a) n-type deives (b) p-type devices

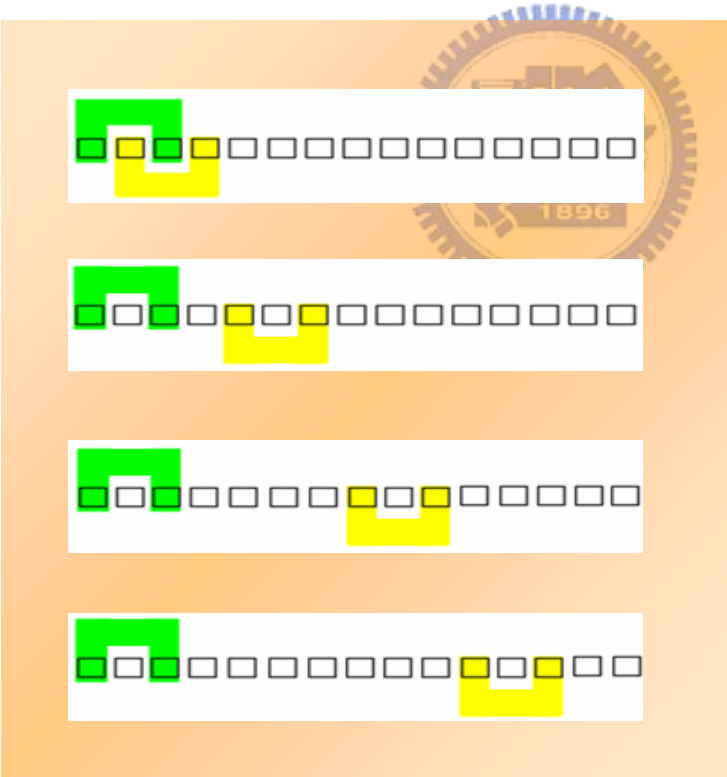


Fig. 2-21 Illustration of the interdigitated method of the crosstie device with different distance between each interfigitated pair.

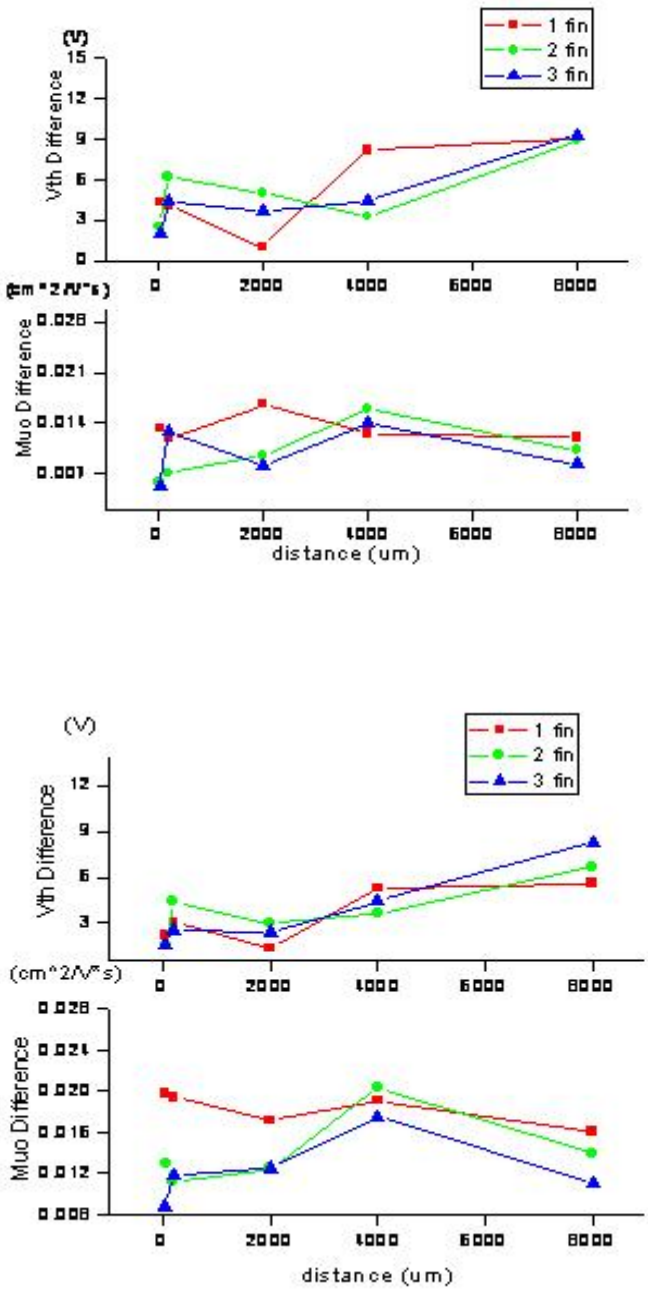


Fig. 2-22 △Vth and △Muo with distance of n-type devices (a) mean value (b) standard deviation

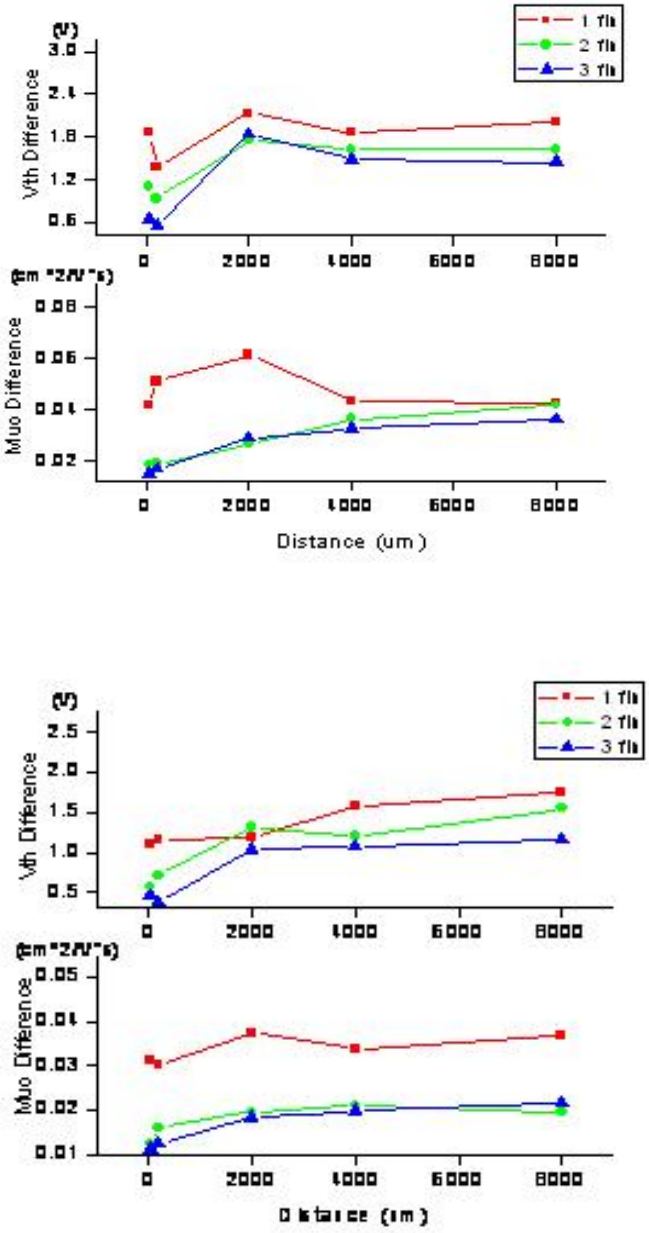


Fig. 2-23 △Vth and △Muo with distance of p-type devices (a) mean value (b) standard deviation

Chapter 3

C-V Mismatch Analysis

3-1. Interdigit Effect Analysis

Up to this chapter, various kinds of interdigitated methods are investigated via I-V measurement. It is demonstrated from previous chapters that by employing interdigitated methods, standard deviations of △Vth and △Muo decrease as finger number increases, while those almost remain the same in spite of finger distance.

It is entirely fair to say that I-V measurements could reveal the whole channel's characteristics which would not afford to provide detailed information about the mechanism of devices. Therefore, C-V measurement would become essential for delicate analysis[11-13]. Generally speaking, the C-V measurement is characterized by its ability of revealing characteristics of gate-to-source and gate-to-drain instead of the whole channel. Besides, it is more sensitive to frequency of applied signal, which plays a important role distinguishing the fixed charge from interface states. Based on the features, it would be inspiring to re-examine the mismatch effect with interdigitated methods by employing C-V measurement[14].

In this section, the gate-to-source capacitance Cgs and gate-to-drain capacitance Cgd of n-type and p-type devices are measured with frequencies of 50kHz and 1MHz. The Cgd curve is measured with a floating source and Cgs curve is measured with a floating drain. Besides, the curves are plotted with normalized value of capacitances, which means the ratio of the measured value to the maximum value of the capacitance. Taking the n-type Cgs curves with 50kHz for example, as shown in Fig. 3-1(a), we could observe that all curves remain unity as the gate voltage is larger than the flat

band voltage V_{FB} and fall to zero sharply around $V_{FB.}$ When the interdigitated method is employed in Fig. 3-1(b), Cgs curves reveal better uniformity especially in the abrupt region around $V_{FB.}$ In addition, Cgs curves of p-type devices are shown in Fig. 3-2(a)(b), which shows similar properties as n-type devices.

Unlike the I-V measurement, parameters such as Vth and Muo could not be extracted from C-V data. In order to analyze practically, we take the derivatives of capacitance versus gate voltage and observe the maximum value and its corresponding voltage. Derivative curves of Cgs in n-type devices are shown in Fig. 3-3(a), and the maximum occurs between 1.1V and 1.5V of gate voltage. After employing the interdigitated method, maximums in Fig. 3-3(b) appear in a narrower range of 1.1V to 1.3V of gate voltage. When it comes to p-type devices, as shown in Fig. 3-4(a) and (b), minimums of derivatives locate between -2.3V to -2.5V in original devices and -2.4V to -2.45V in interdigitated ones.

3-2. Comparison of I-V and C-V Mismatch Analysis

For the purpose of analyzing mismatch effect, graphs of error bar are used to summarize the results of C-V measurements. Fig. 3-5(a) shows the gate voltage Vg_max's distribution where the maximum of derivative occurs. In each condition, for example, Cgd at 1MHz, the straight line represents the standard deviation and the center point represents the mean value.

Comparing Cgd on 1MHz and 50kHz, it could be found that mean values are 1.6V and 1.28V individually. If we set the measurement frequency on 1MHz, careers in certain states could not afford to response on time with such high frequency, which means that the derivative of 1MHz would reach its maximum later. As a consequence, the gate voltage Vg_max where the maximum value occurs of 1MHz would larger than that of 50kHz. In addition, no apparent differences could be observed if we

examine Cgd and Cgs with the same frequency. Comparing with initial condition, devices could more tend to reveal asymmetric properties after stress and degradation.

As far as the mismatch effect is concerned, it would be found that standard deviations with interdigitated method are smaller than those of original devices, while the mean values almost have no changes. In Fig. 3-5(b), maximum values with interdigit are lower in mean value and standard deviation. By employing C-V analysis, it could be further confirmed that interdigitated methods are able to suppress the mismatch effect. In addition, error bar analysis of p-type devices are also shown in Fig. 3-6(a) and (b), which shows smaller deviations than n-type devices.

Since the interdigitated method still has better performance in C-V measurement, it would be desired for further investigation with more fingers of interdigit. In Fig. 3-7, the left side shows a straight line representing standard deviations of Vth difference from I-V measurements, and the right side shows scatters representing those of Vg_max difference from C-V measurements. The four symbols of scatter represent Cgs and Cgd in 50kHz and 1MHz. It could be observed that both the straight line and scatters reveal the characteristic of inverse proportionality with finger numbers. P-type devices in Fig. 3-8 show the similar property, but standard deviations are smaller and closer to zero.

3-3. Summary

In this chapter, the mismatch issues are discussed with C-V measurement. We take the derivatives of capacitance versus gate voltage to observe the maximum value and its corresponding voltage. It is observed that the gate voltage where the maximum value occurs of 1MHz would larger than that of 50kHz, but no apparent differences appear between Cgs and Cgd. As far as the mismatch effect is concerned, it is found that standard deviations with interdigitated method are smaller than those of original

devices, which is consistent with the conclusion of I-V measurement in previous chapter.

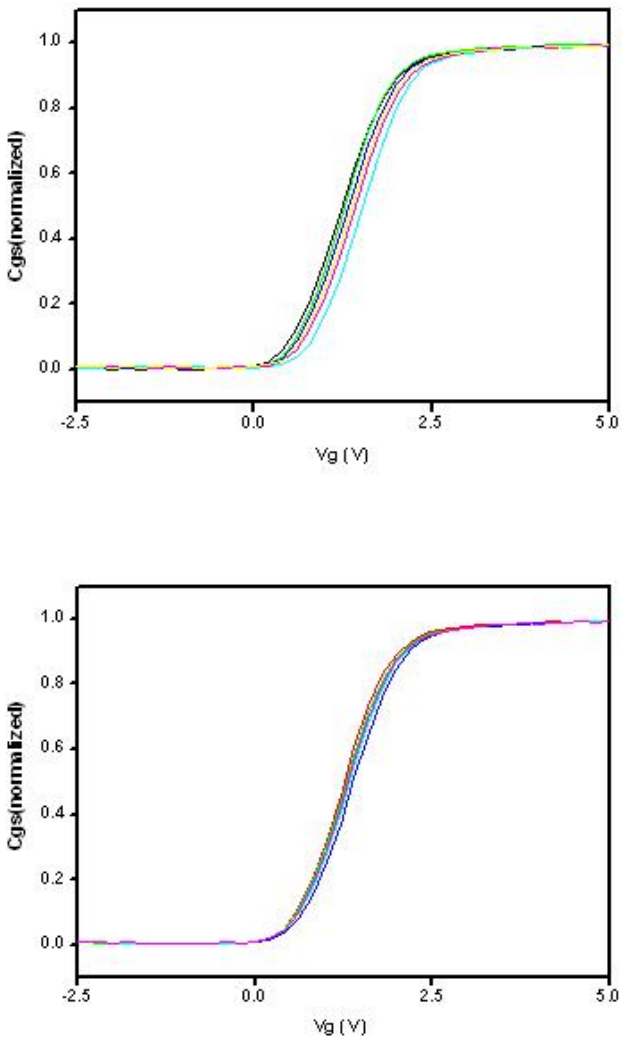


Fig. 3-1 Normalized curves of gate-to-source capacitance with 50kHz in N-type devices (a) original devices (b) interdigitated with one finger

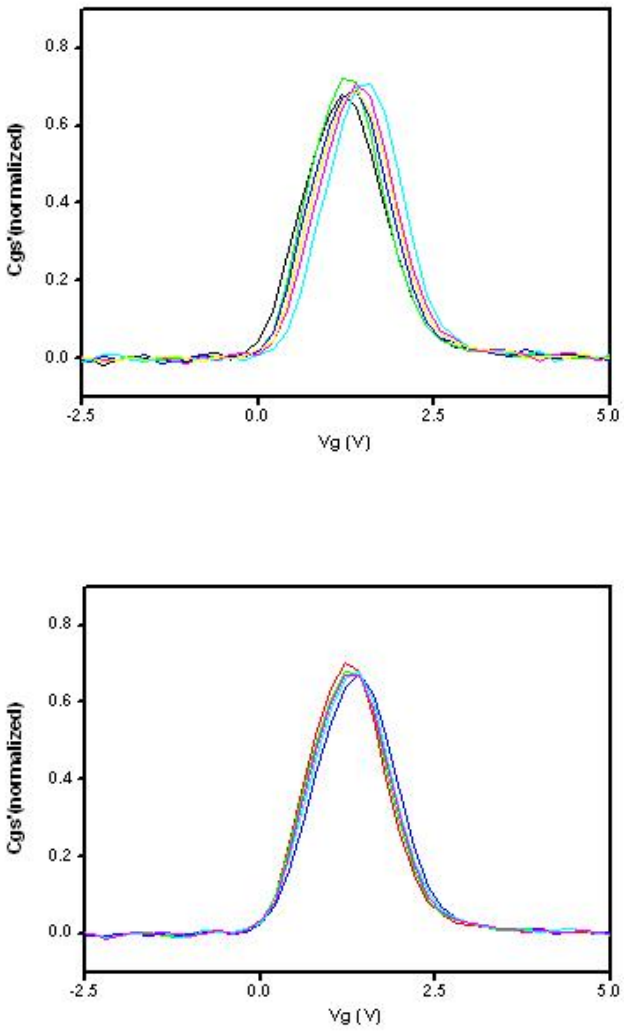


Fig. 3-2 Derivative curves of gate-to-source capacitance with 50kHz in N-type devices (a) original devices (b) interdigitated with one finger

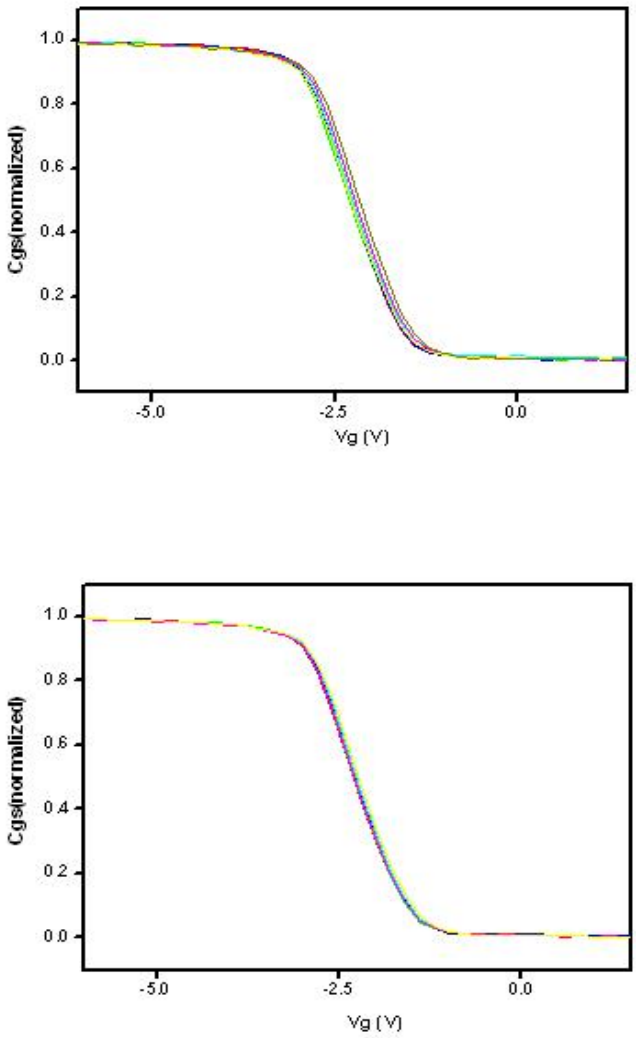


Fig. 3-3 Normalized curves of gate-to-source capacitance with 50kHz in P-type devices (a) original devices (b) interdigitated with one finger

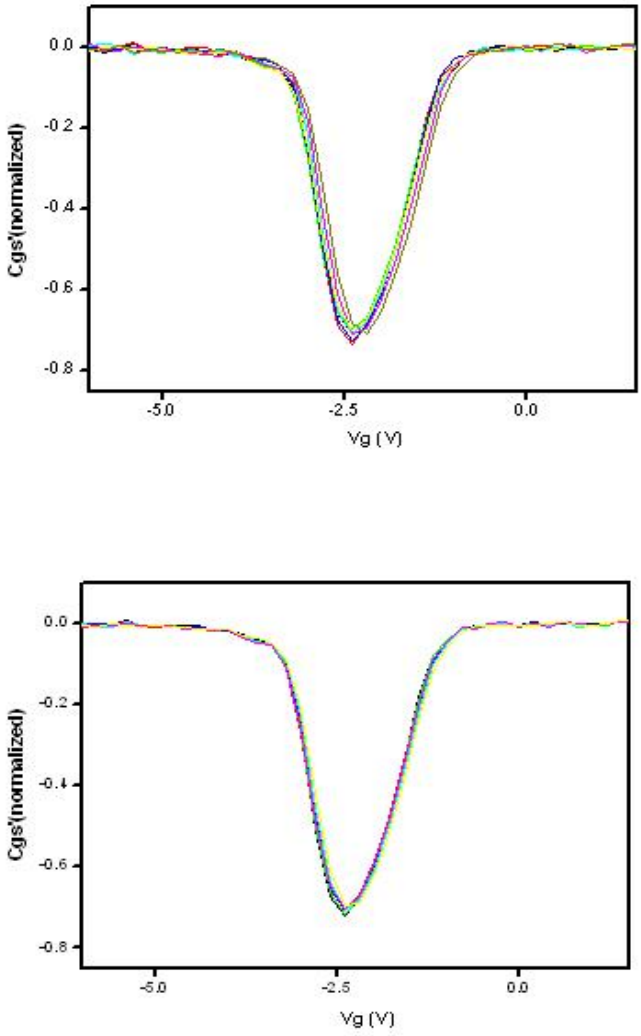


Fig. 3-4 Derivative curves of gate-to-source capacitance with 50kHz in P-type devices (a) original devices (b) interdigitated with one finger

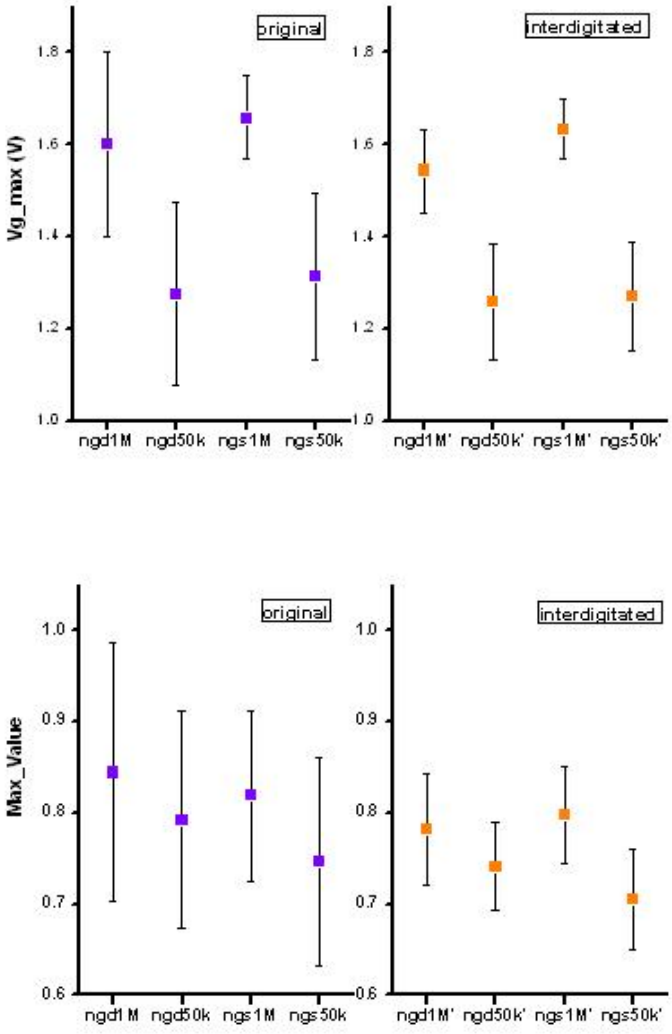


Fig. 3-5 Error bar analysis of derivative curves of capacitance in n-type devices (a) gate voltages Vg_max of derivative's maximum (b) values of derivative's maximum

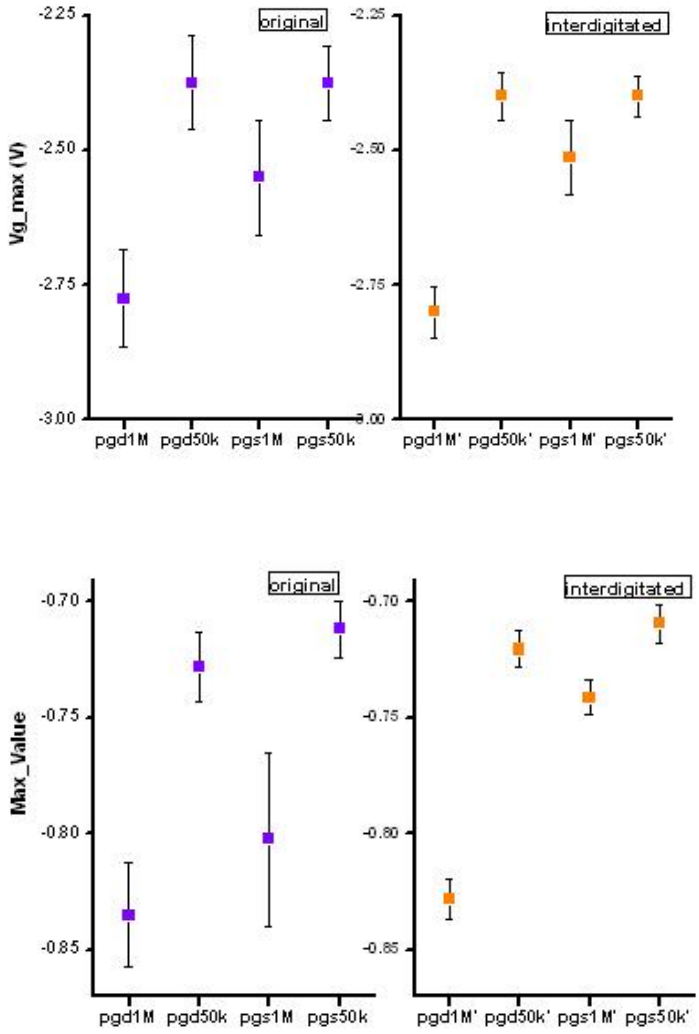


Fig. 3-6 Error bar analysis of derivative curves of capacitance in p-type devices (a) gate voltages Vg_min of derivative's minimum (b) values of derivative's minimum

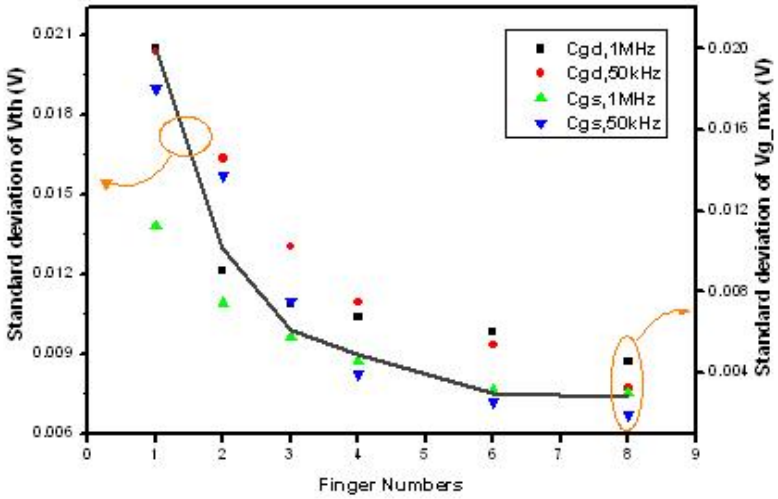


Fig. 3-7 Standard deviations in n-type devices with finger numbers of Vth difference from I-V measurement (left side) and Vg_max difference from C-V measurement (right side)

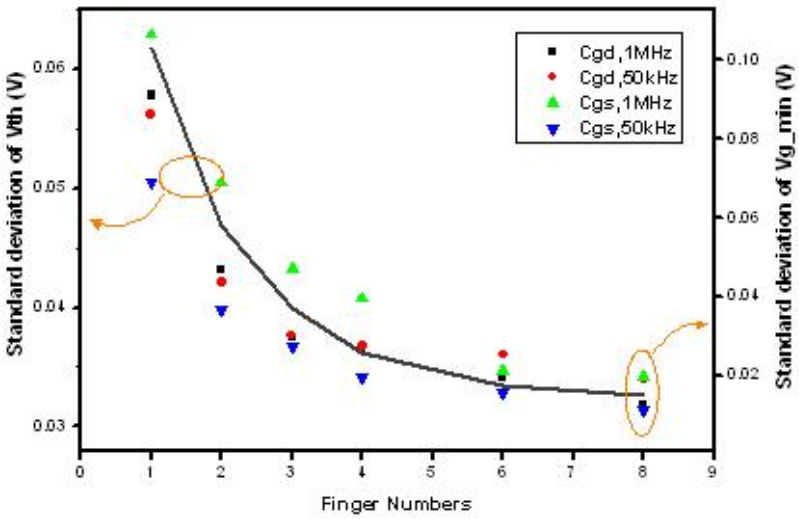


Fig. 3-8 Standard deviations in p-type devices with finger numbers of Vth difference from I-V measurement (left side) and Vg_min difference from C-V measurement (right side)

Chapter 4

Conclusion

In this thesis, we investigate the mismatch issue for LTPS TFTs. Firstly we aim at the size and interdigit effects for small area TFTs. It is observed that the mismatching factor decreases rapidly with the increase of the device's area, and the interdigitated arrangement has better tolerance than the original arrangement in electrical data statistically of matching TFTs. This is because that the device with small dimension contains less grain boundaries, which contributes worse mismatch effect. In particular, the mismatching factor seems to be irrelevant while the device's area are larger than 100 cm^2, which means that the size effect are less obvious than small-size device.

To further investigate the mismatching properties of the interdigitated arrangements, a huge number of devices with the same dimension are utilized. By analyzing standard deviations of parameters' differences, it is found that the interdigitated method is indeed superior than the original. Besides, Vth and Muo are inversely proportional to the number of fingers, especially the threshold voltage. Furthermore, a model is proposed to predict the performance of the interdigitated method, which has high accuracy with the real data. As far as distance analysis is concerned, almost no correlations between the distance and mismatch effect could be observed.

Next, the mismatching properties are examined by C-V measurements. We take the derivatives of capacitance versus gate voltage to observe the maximum value and its corresponding voltage. It is observed that the gate voltage where the maximum value occurs of 1MHz would larger than that of 50kHz, but no apparent differences

appear between Cgs and Cgd. As a consequence, standard deviations with interdigitated method are smaller than those of original devices, which is consistent with the conclusion of I-V measurement.

In order to suppress the mismatch effect, the method of interdigit are concerned since the fabrication process is predetermined. From the viewpoints of statistical analysis, contributions of interdigit are demonstrated by parameter distributions of large amount of devices. In addition, we propose a model to evaluate the inverse proportionality of the interdigitated method, which could be used to predict the mismatch property of devices.

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