Effects of NH_3 Plasma Passivation on N-Channel Polycrystalline Silicon Thin-Film Transistors

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Abstract— **The NH_3-plasma passivation has been performed on polycrystalline silicon (poly-Si) thin-film transistors (TFT's). It is found that the TFT's after the NH_3-plasma passivation achieve better device performance, including the off-current below 0.1 pA/μm and the on/off current ratio higher than 10^8, and also better hot-carrier reliability than the H_2-plasma ones. Based on optical emission spectroscopy (OES) and secondary ion mass spectroscopy (SIMS) analysis, these improvements were attributed to not only the hydrogen passivation of the defect states, but also the nitrogen pile-up at SiO_2/poly-Si interface and the strong Si-N bond formation to terminate the dangling bonds at the grain boundaries of the polysilicon films. Furthermore, the gate-oxide leakage current significantly decreases and the oxide breakdown voltage slightly increases after applying NH_3-plasma treatment. This novel process is of potential use for the fabrication of TFT/LCD's and TFT/SRAM's.**

I. Introduction

POLYCRYSTALLINE SILICON (poly-Si) thin-film transistors (TFT's) are of interest for a number of applications such as ultra-large-scale-integration (ULSI) memories and large-area electronic devices (displays, sensors, etc.) [1], [2]. In these devices, defect states either in the bulk or at grain boundaries play a crucial role [3]. To obtain high-performance poly-Si TFT's, it is necessary to reduce the trap-states of the polysilicon films. It is now well known that hydrogenation tends to tie up the grain-boundary dangling bonds with hydrogen, thereby remarkably improving the characteristics of the poly-Si TFT's [4]. However, it had been observed that the characteristics of the poly-Si TFT's after the hydrogen passivation suffer a low hot-carrier endurance [5], [6]. On the other hand, the O_2 and N_2 plasma passivation are alternative techniques to improve the performance of the TFT's. The effects of the O_2 plasma treatment on poly-Si TFT's have been reported in literature [7]–[9]. Recently, it has been reported that the H_2/N_2 mixture plasma and nitrogen ion implantation significantly improve the electrical characteristics of the poly-Si TFT's [10], [11]. Tsai *et al.* exhibited that the nitrogen-containing hydrogen plasma (H_2/N_2 mixture plasma) treatment could further improve the characteristics of the TFT's as compared with pure H_2 plasma treatment [10]. It is attributed to the passivation effect of the nitrogen radicals themselves and the promotion of the hydrogen plasma generation due to the radical collision. Yang *et al.* showed that the improved characteristics of poly-Si TFT's can be obtained by combining the nitrogen implantation with the H_2-plasma passivation [11]. It is believed that the defect-state passivation and donor effect of nitrogen are responsible for the improved characteristics. It has also been reported that after a pre-oxidation NH_3 annealing (850 °C, 30 min) and an H_2-plasma treatment, the poly-Si TFT's can achieve better characteristics than purely with an H_2-plasma treatment [12]. It is believed that the nitrogen incorporation by a high-temperature NH_3 annealing can form the gate oxynitride and result in better H_2-plasma passivation effect. In this work, a simple low-temperature technique, NH_3-plasma passivation, has been employed to enhance both the electrical properties and hot carrier reliability of the poly-Si TFT's [13], [14]. The mechanism of the defect state passivation and the electrical properties of the gate dielectric after the NH_3-plasma treatment are also discussed.

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II. Experiment

The poly-Si TFT's were fabricated on the thermally oxidized (100) silicon wafers. A 110-nm thick amorphous silicon (α-Si) was initially deposited at 550 °C by low-pressure chemical vapor deposition (LPCVD) using pure SiH_4, and then furnace annealed at 600 °C for 24 h in N_2 ambient to recrystallize such silicon films. After defining the active islands, a 70-nm thick silicon-dioxide was thermally grown by dry oxidation at 1000 °C. Another 300-nm thick polysilicon film was deposited at 620 °C in an LPCVD system and patterned as the gate area. A self-aligned $POCl_3$ doping was performed at 900 °C for 20 min to form the source, drain, and gate electrodes. After the oxide was stripped, the samples were subjected to the NH_3 or H_2 plasma treatment in a parallel-plate plasma reactor at 300 °C with a power density of 0.7 W/cm^2. The plasma exposure time is 30 min if there is no specification in text. The plasma conditions (listed in Table I) for NH_3 and H_2 had been optimized to obtain the optimum device performance, respectively. After a plasma-enhanced CVD (PECVD) SiO_2 with a thickness of about 500 nm was deposited, the contact holes were opened and the Al films were deposited and then defined. The current–voltage (I–V) characteristics of the TFT's and the polyoxides were measured by an HP 4145B semiconductor parameter analyzer. The concentrations of the hydrogen and nitrogen atoms were measured using secondary ion mass spectroscopy (SIMS) with Cs^+ as the primary ion.

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TABLE I
THE OPTIMIZED PLASMA CONDITIONS FOR NH_3- AND H_2-PLASMA PASSIVATION IN THIS WORK

	RF Power (Watt)	Pressure (mTorr)	Flow Rate (sccm)	Temperature (°C)
NH3-plasma	200	300	700	300
H2-plasma	200	100	80	300

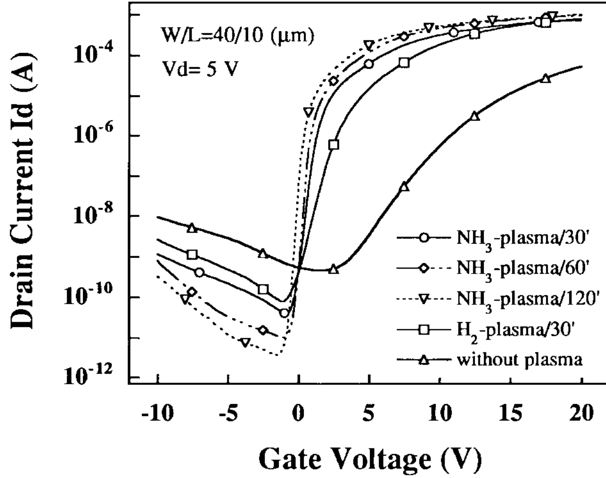

Fig. 1. The transfer characteristics of poly-Si TFT's after applying NH_3-plasma/30 min, 60 min, 120 min, H_2-plasma/30 min, and without plasma treatments.

III. RESULTS AND DISCUSSION

The I_d–V_g characteristics of the n-channel poly-Si TFT's with various NH_3-plasma exposure times from 0 to 120 min are shown in Fig. 1. The transfer curves of the devices with a 30 min H_2-plasma and without plasma treatments are also shown for comparison purposes. It is obvious that the NH_3-plasma and H_2-plasma treatments both can effectively promote the performance of the TFT's. In addition, it seems that the devices treated by NH_3-plasma for 30 min have even better performance than those treated by H_2-plasma. Moreover, as the exposure time of NH_3-plasma increases, the TFT's performance can be enhanced increasingly, such as minimum drain current and inverse subthreshold slope down to 3.54 pA and 200 mV/dec, and field-effect mobility and on/off current ratio increasing to 79.93 cm^2/Vs and 2.23×10^8, respectively, for 120 min NH_3-plasma treated devices, unlike the previous report that the TFT's exposed to H_2-plasma exhibited earlier saturation characteristics [8].

The temperature dependences of the drain current of the NH_3-plasma, the H_2-plasma, and without plasma treated devices were also measured in the temperature range from 30 to 150 °C. Using the linear fitting of the $\ln(I_d)$ versus the 1/kT plot, where k is the Boltzmann constant and T is the absolute temperature, the activation energy E_a of the drain current at different gate biases is deduced as shown in Fig. 2 at $V_d = 0.1$ V. It can be seen that the NH_3-plasma treated devices have lower E_a than the H_2-plasma and without plasma treated ones. The value of the activation energy reflects the carrier transport barrier of the grain boundary within the polysilicon channel.

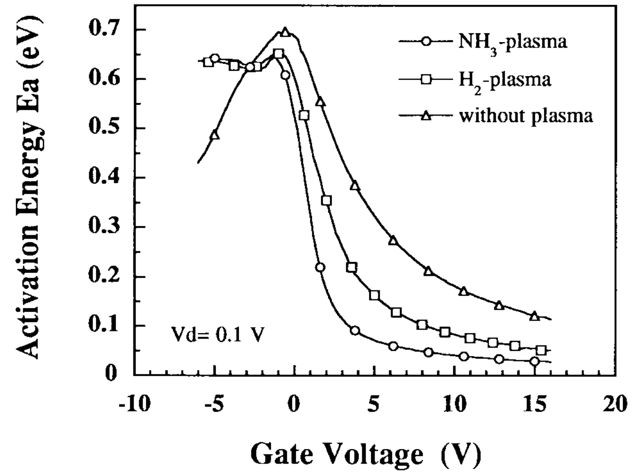

Fig. 2. The activation energies E_a of the drain current of the poly-Si TFT's for different gate biases at $V_d = 0.1$ V with the NH_3-plasma, H_2-plasma, and without plasma treatments.

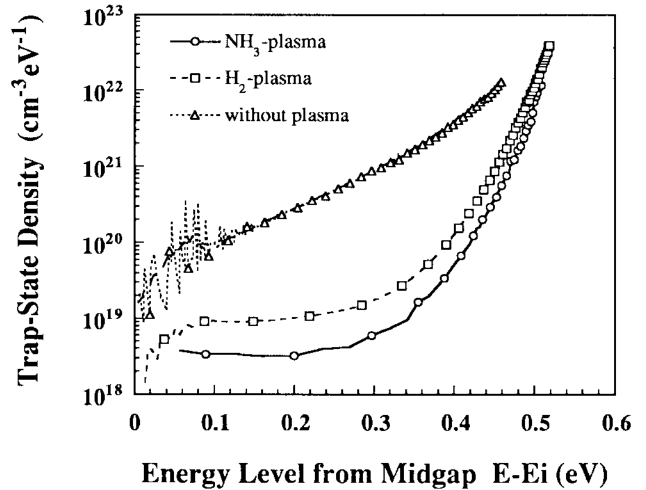

Fig. 3. The trap-state density distribution calculated from field-effect conductance method.

It implies that more trap-states in the channel are passivated by NH_3-plasma than those by H_2-plasma treatment. Hence, the grain boundary barrier potentials are further reduced by NH_3-plasma passivation. Fig. 3 shows the trap-state densities in the energy band gap determined by the field effect conductance method [15]. It is clearly seen that both plasma treatments reduce the trap-state densities significantly, and the NH_3-plasma treated devices have more improvement than those for H_2-plasma treated ones. This result is consistent with the activation energy shown in Fig. 2.

The hot-carrier reliability of the NH_3-plasma treated devices was also investigated. Fig. 4(a) and (b) shows the variations of on current I_{on} and minimum drain current I_{min} for the devices with the NH_3- and H_2-plasma passivation, respectively, after they were stressed at $V_d = 20$ V, $V_g = 10$ V for different stress durations. The starting values of the on/off current are 561 μA/39.5 pA and 333 μA/81.0 pA for NH_3- and H_2-plasma treated devices, respectively, at the stress time $t = 0$. In Fig. 4(a), it is found that I_{on} decreases with increasing hot-carrier stress time. The variations of I_{on} for NH_3-plasma-

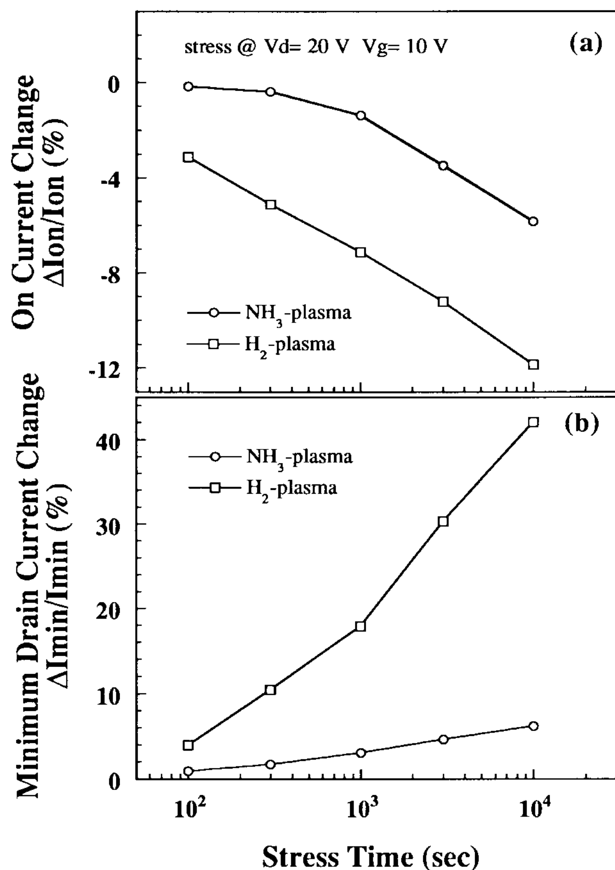

Fig. 4. The variations of (a) the turn on drain current $I_{\rm on}$ and (b) the minimum drain current $I_{\rm min}$ of the poly-Si TFT's with NH_3-plasma and H_2-plasma passivated devices as a function of stress time.

treated devices are less than those for H_2-plasma treated ones. In Fig. 4(b), $I_{\rm min}$ increases with increasing stress time and the degradation rate for the H_2-plasma treated devices is larger than that treated with NH_3-plasma. From the data of Fig. 4(a) and (b), the NH_3-plasma passivated devices have better hot-carrier reliability than the H_2-plasma ones. The performance degradation of both devices induced by the hot carrier stress is ascribed to the generation of poly-Si/SiO_2 acceptor-type interface states and the grain boundary states in the poly-Si channel layer [5], [16]. The hot-carrier endurance of NH_3-plasma passivation is better than that of the H_2-plasma passivation, suggesting that not only hydrogen atoms but also nitrogen atoms are diffusing into the poly-Si films. In order to investigate the causes, the OES and the SIMS analysis were also performed.

The emission spectroscopy is a typical apparatus used for the detection of reactive species in plasma process. Fig. 5 shows the optical emission spectra observed from the NH_3-plasma in the range of 200–900 nm. As indicated in the figure, a strong line spectrum of NH radical emissions at the wavelength of 336 nm and three line spectra of H radical emissions, which correspond with hydrogen atomic lines, H_α 656 nm, H_β 486 nm, and H_γ 434 nm, are found, that can be thought of the sources diffusing into gate dielectric and poly-Si channel to passivate the defect states. In addition, the plasma formation is induced by the radical collisions in the

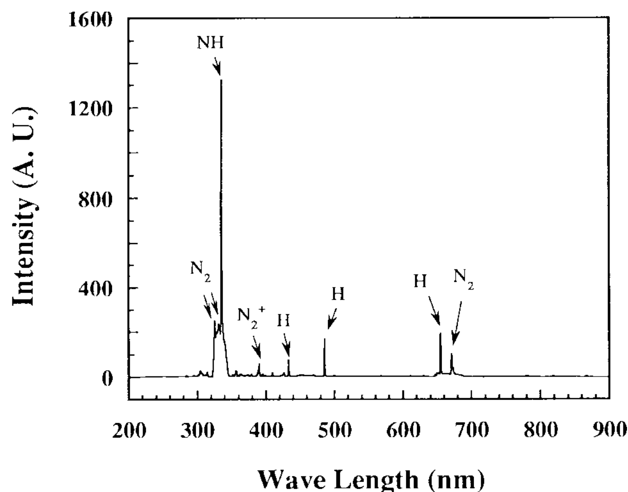

Fig. 5. Emission spectra observed from a PECVD NH_3-plasma process using an optical emission spectroscopy (OES).

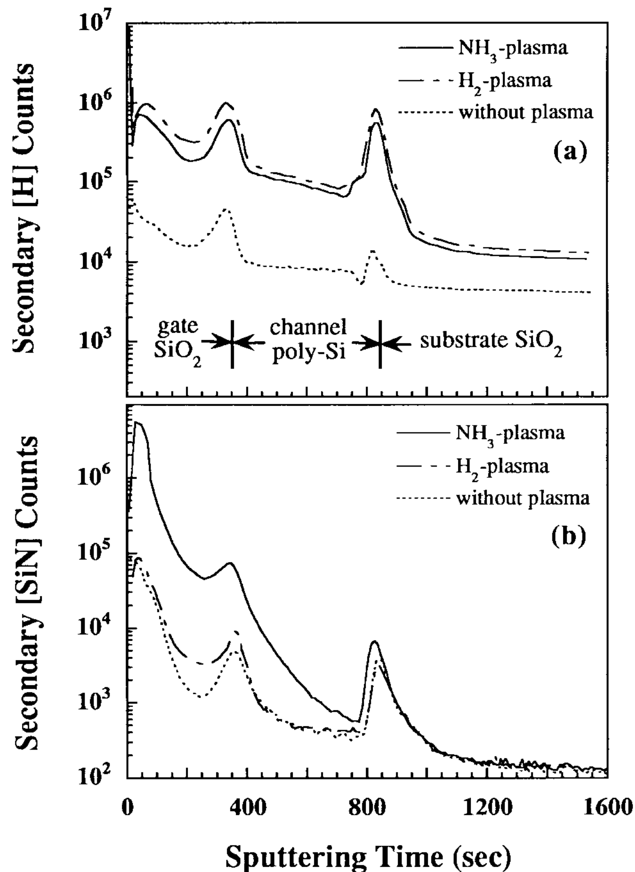

Fig. 6. The SIMS profiles of (a) H and (b) SiN for 70-nm oxide/80-nm poly-Si/field oxide substrate structure with NH_3-plasma, H_2-plasma, and without plasma treatments. The plasma exposure times for NH_3 and H_2 are both 1 hour.

reaction chamber. Although the existing N_2 in the NH_3-plasma provide little contribution to the defect state passivation, the N_2 can urge the other species (such as H and NH) to form radicals by increasing the collision probability, hence promote the hydrogen plasma generation [10]. All of them can enhance the passivation effect of the TFT's in the NH_3-plasma process.

Fig. 6 shows the SIMS results of the specimens exposed to an NH_3- and an H_2-plasma for 1 h, respectively, and the

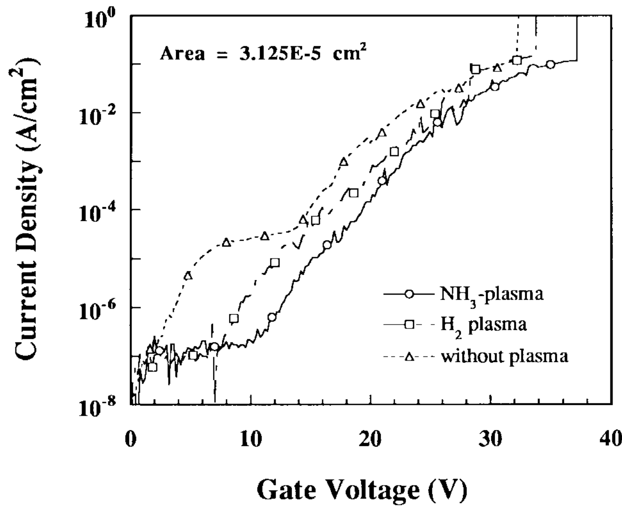

Fig. 7. J_g–V_g characteristics of the gate dielectrics after NH_3-plasma, H_2-plasma, and without plasma treatments.

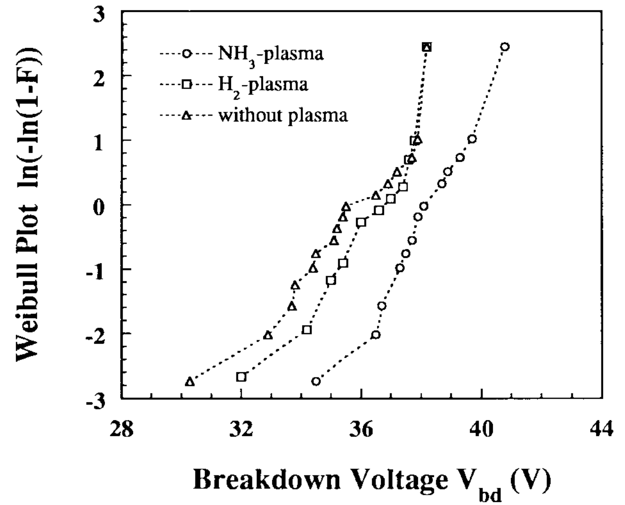

Fig. 8. The cumulative distributions of time-zero-dielectric-breakdown (TZDB) characteristics of the gate dielectrics with NH_3-plasma, H_2-plasma, and without plasma treatments.

control sample (i.e., without plasma treatment) for comparison. As can be seen in Fig. 6(a), the hydrogen concentrations increase significantly both for H_2-plasma and NH_3-plasma treated samples, and the value of the former is slightly higher than that of the latter. However, the performance of the TFT's after NH_3-plasma treatment is even better than that treated with H_2-plasma. Hence, the improvement on electrical properties of the TFT's after NH_3-plasma passivation may come from other reasons. In Fig. 6(b), it is found that the nitrogen atoms can even diffuse throughout the channel poly-Si region for the NH_3-plasma treated samples. From the SIMS analysis, it is suspected that strong Si–N bonds can be formed in the poly-Si channel and at poly-Si/SiO_2 interface besides weak Si–H bonds. In the previous literature, it had been reported that the nitrogen implantation in the poly-Si gate/SiO_2/c-Si substrate MOS structure could obtain a much smaller interface-state generation rate after high-field/current stress [17]. Momose *et al.* also showed that with the low concentration (<1 atom%) nitrogen incorporation in the NH_3 rapid thermal nitrided-oxide, both drivability and hot carrier reliability of MOSFET could be improved [18].

Aforementioned in Fig. 6, the hydrogen and nitrogen radicals can diffuse into and accumulate in gate dielectric, so that the effects of the plasma treatments on the electrical properties of gate dielectrics of the TFT's are worthy to be investigated. The characteristics of leakage current density versus gate voltage (J_g–V_g) for the gate dielectric after NH_3-plasma, H_2-plasma, and without plasma treatments are shown in Fig. 7. It can be seen that the gate dielectrics for NH_3- and H_2-plasma treatments have lower leakage current than those without plasma ones when the gate is positively biased and the source/drain electrodes are commonly grounded. Moreover, it is found that the NH_3-plasma treated devices exhibit lower leakage current than the H_2-plasma treated ones. That is, the qualities of the gate dielectrics for the NH_3-plasma treatments are better than those treated with H_2-plasma. Since these three samples are fabricated by the same processes and thus have almost the same interface morphologies, the improvements of gate dielectrics may be therefore connected with the incorporation of nitrogen and hydrogen.

Fig. 8 shows the cumulative distributions of the time-zero-dielectric-breakdown (TZDB) characteristics of the gate dielectrics with NH_3-plasma, H_2-plasma, and without plasma treatments. The gate dielectric with NH_3-plasma treatments exhibits better TZDB characteristics than the other two cases. The H_2-plasma treated gate dielectrics have slightly higher breakdown voltage value (V_{bd}) and narrower distribution than does those without plasma treated ones. This improved V_{bd} of the gate dielectric is also attributed to the nitrogen and hydrogen participation. Originally, due to the high stress in polyoxide [19], it is expected that there are many strained bonds within the oxide, especially at local regions nearby the grain boundaries. These strained bonds are easy to be broken by high energy electrons to cause trap-state generation when a field is applied to the oxide. After NH_3-plasma treatment, the nitrogen and hydrogen in the oxide may strengthen the strained bonds and passivate the trap-states. Hence, the oxide breakdown strength is improved.

IV. Conclusion

The NH_3-plasma passivation has been used to promote the electrical properties of poly-Si TFT's. It is found that the poly-Si TFT's after NH_3-plasma passivation exhibit significantly superior device characteristics and hot-carrier reliability to those with the conventional H_2-plasma passivation. It is found that the TFT's after the NH_3-plasma passivation can achieve the off-current below 0.1 pA/μm and the on/off current ratio higher than 10^8. By means of OES and SIMS analysis, these improvements were attributed to not only the hydrogen passivation of the defect states, but also the nitrogen pile-up at SiO_2/poly-Si interface and the strong Si–N bond formation to terminate the dangling bonds in the grains and at the grain boundaries in the channel region. Furthermore, the characteristics of the gate dielectrics after the NH_3-plasma treatment has been also improved.

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REFERENCES

[1] W. G. Hawkins, "Polycrystalline-silicon devices technology for large-area electronics," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 477–481, 1986.

[2] P. Migliorato and D. B. Meakin, "Material properties and characteristics of polysilicon transistors for large area electronics," *Appl. Surf. Sci.*, vol. 30, p. 353, 1987.

[3] K. Ono, T. Anoyama, N. Konishi, and K. Miyata, "Analysis of current–voltage characteristics of low-temperature-processed polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 39, pp. 792–802, 1992.

[4] B. A. Khan and R. Pandya, "Activation-energy of source-drain current in hydrogenated and unhydrogenated polysilicon thin-films transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 1727–1734, 1990.

[5] S. Banerjee, R. Sundaresan, H. Schichijo, and S. Malhi, "Hot-carrier degradation of n-channel polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, pp. 152–157, 1988.

[6] M. Hack, A. G. Lewis, and I.-W. Wu, "Physical models for degradation effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 890–897, 1993.

[7] S. Ikeda, S. Hashiba, I. Kuramoto, H. Katoh, S. Ariga, T. Yamanaka, T. Hashimoto, N. Hashimoto, and S. Meguro, "A polysilicon transistor technology for larger capacitance SRAM's," in *IEDM Tech. Dig.*, 1990, pp. 459–463.

[8] H. N. Chern, C. L. Lee, and T. F. Lei, "The effects of H_2–O_2-plasma treatment on the characteristics of polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 2301–2306, 1993.

[9] N. H. Nickel, A. Yin, and S. J. Fonash, "Influence of hydrogen and oxygen plasma treatments on grain-boundary defects in polycrystalline silicon," *Appl. Phys. Lett.*, vol. 65, pp. 3099–3101, 1994.

[10] M. J. Tsai, F. S. Wang, K. L. Cheng, S. Y. Wang, M. S. Feng, and H. C. Cheng, "Characterization of H_2/N_2 plasma passivation process for poly-Si thin-film transistors (TFT's)," *Solid State Electron.*, vol. 38, pp. 1233–1238, 1995.

[11] C. K. Yang, T. F. Lei, and C. L. Lee, "Improved electrical characteristics of thin-film transistors fabricated on nitrogen-implanted polysilicon films," in *IEDM Tech. Dig.*, 1994, pp. 505–508.

[12] ——, "The combined effects of low pressure NH_3-annealing and H_2 plasma hydrogenation on polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 15, pp. 389–390, 1994.

[13] H. C. Ha, S. K. Lee, and C. G. Ko, "Hydrogenation effects on the poly-Si TFT," *J. Korean Inst. Telematics and Electronics*, vol. 30A, pp. 23–30, 1993.

[14] F. S. Wang, M. J. Tsai, and H. C. Cheng, "The effects of NH_3 plasma passivation on polycrystalline silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 16, pp. 503–505, 1995.

[15] G. Fortunato and P. Migliorato, "Determination of gap state density in poly-crystalline silicon by field effect conductance," *Appl. Phys. Lett.*, vol. 49, pp. 1025–1027, 1986.

[16] G. Fortunato, A. Pecora, G. Tallarida, L. Mariucci, C. Reita, and P. Migliorato, "Hot carrier effects in n-channel polycrystalline silicon thin-film transistors: A correlation between off-current and transconductance variations," *IEEE Trans. Electron Devices*, vol. 41, pp. 340–346, 1994.

[17] S. Haddad and M. S. Liang, "Improvement of thin-gate oxide integrity using through-silicon-gate nitrogen ion implantation," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 58–60, 1987.

[18] H. S. Momose, T. Morimoto, Y. Ozawa, K. Yamabe, and H. Iwai, "Electrical characteristics of rapid thermal nitrided-oxide gate n- and p-MOSFET's with less than 1 atom% nitrogen concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 546–552, 1994.

[19] A. Shintani and H. Nakashima, "Anomalous stress in thermal oxide of polycrystalline Si," *Appl. Phys. Lett.*, vol. 36, pp. 983–985, 1980.

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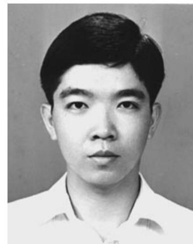

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