# 國 立 交 通 大 學

## 電信工程學系

## 博 士 論 文

多層技術設計之小型化高頻電路

Design of Miniaturized High-frequency Components by Multi-layer Technology

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## 摘 要

隨著材料及製程技術的進步，多層電路的開發配合高速及射頻電路的發展持續進行著，應用多層電路技術，更易於達成高速數位電路及射頻電路的小型化及高整合化。然而，相較於表面黏著元件，當電路元件內埋至多層電路後會產生不同的電氣特性，本篇論文首先探討在射頻電路應用中基本但卻重要的內埋電容及電感，應用多層電路架構及高介電常數材料，內埋電容可提供足夠的電容值範圍，但在內埋電感時，由於製程無法提供夠緊密的繞圈造成大量的磁漏，因此無法在有限的空間產生足夠的電感值。接著討論利用低溫共燒陶瓷製程技術，設計應用於 USB 2.0 產品的共模濾波器，相較於一般以磁性材料為主的繞線式共模濾波器，使用多層電路技術設計的共模濾波器可提供較低的差模訊號損失，此外，應用偏移線路的新架構而非完全重疊的線路來設計差模訊號線路組，可減少33%的零件厚度。為因應高速時脈及高速線路的不斷發展，用於控制訊號、時脈同步的延遲線路需求日益增加，接著討論的題目便是

應用低溫共燒陶瓷製程技術設計多層的延遲線路元件，為了改善在微帶線/帶線型折線式延遲線路波形失真的問題,論文中提出以接地的防護線來設計小型化的三維多層延遲線路元件，比較應用帶線型折線式延遲線路和應用三維架構設計的延遲線路元件，同樣提供 233 ps 的延遲時間，多層架構設計之延遲線路可縮小至 EIA 1206 的尺寸，省下 2.34 倍的電路板面積。論文最後探討上述三種以多層架構設計的元件，提出改進及可能的發展方向。

# Design of Miniaturized High-frequency Components by Multi-layer Technology

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## ABSTRACT

With advances in material and process technologies, developments of multi-layer circuit are enthusiastically pursued by both high-speed and RF communities. Using multi-layered technologies, the miniaturization and, subsequently, increasing level of integration of high speed digital and RF circuits are more easily realized. The embedded components, however, have different electrical characteristics as compared to the surface mount elements. In this dissertation, characterizations of embedded MIM capacitor and solenoid inductor, which are fundamental but important parts in RF systems, are performed first. With multi-layer structure and high dielectric constant material, the designed embedded capacitors can provide sufficient capacitance. But due to significant magnetic flux leakage present in the loosely wound embedded solenoid inductor structure, large inductance cannot be realized in a compact structure. This is followed by the design of a LTCC common-mode filter intended for use with USB 2.0 products. As compared to the wire-wound common-mode choke, the designed multi-layer common-mode filter produces lower insertion loss on differential-mode signal than conventional ferrite-based common-mode filter. Also, by using a novel offset architecture, as opposed to completely overlapped architecture, for the differential transmission pair,

a 33% reduction of thickness is achieved in the design of a miniaturized common-mode filter with multi-layer LTCC technology. In view of increasing need of high-speed clock and data circuits to control their skew problems, a design of LTCC delay line is then conducted. To improve the waveform distortion associated with the microstrip/stripline-type meander delay line, a miniaturized high-frequency 3-D delay line with grounded guard traces is introduced. By means of 3-D structure, the 233 ps delay time, which requires extra board space amounting to a factor of 2.34 by stripline type meander delay line, can be shrunk into an EIA 1206 form factor. Conclusions on the three types of multi-layer component studied here and recommendations concerning potential improvements of these components are discussed, finally.

# 謝 誌

回想大學到交大報到，已經是將近 15 年前的事了，多年的求學生涯在師長、親友的大力支持下，走得辛苦卻也有著滿滿的收穫。要感謝的人有許多許多，首先，最感謝的當然是我的指導教授—吳霖堃老師，他嚴謹的治學態度以及對學生的提攜及照顧，讓我獲益良多且深受感動，在數不清的週末假日裡悉心的指導，使我的論文得以完成，在此致上最深的謝意。

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# CHAPTER 1

# INTRODUCTION

## 1.1 Motivation

As the microelectronic industry continues to advance, demands for aggressive component/system miniaturization, cost reduction, improved performance, and reliability are increasing. Advances in material and process technologies have led to the development of multi-layer circuits. Using multi-layered technologies, the miniaturization and, subsequently, increasing level of integration of high speed digital and RF circuits has become a widespread practice. Several multi-layered substrate technology solutions have shown potential to successfully miniaturizing and integrating modern products.

Miniaturization and integration, especially for RF circuits, has unique requirements due to the high performance requirements and limited available board space. Virtually all of the active functions of existing devices are contained in a few, highly integrated and specialized IC's based on silicon technology or with some specialized IC's built from GaAs for the higher frequency requirements. Passive components, by contrast, show little or no integration with each schematic element realized by the soldered attachment of a single discrete device to an interconnect board.

Passive components are the major factor in determining the overall size, cost and performance of portable products. The drive to further miniaturization and integration of portable electronic devices has recently focused on the task of passive functions [1]-[3]. To increase the component density on the interconnect board, the

EIA (Electronic Industries Association) form factor of discrete resistor, capacitor, and inductor has seen continuous decrease from 0603 (i.e., surface dimension 0.06 in × 0.03 in or 1.6 mm × 0.8 mm) to 0402 (i.e., 1 mm × 0.5 mm) and even 0201 (i.e., 0.6 mm × 0.3 mm). Even with this miniaturization, however, it does not show the entire picture of the board space occupied since the component clearance and mounting pad size to allow for placement accuracy of the pick and place equipment is not considered. With current surface mount technology's (SMT) capability, a 0.25 mm clearance between adjacent components as demonstrated in Fig. 1.1, is required. Beside, using EIA 0402 discrete component as an example, the two rectangular mounting pads are 0.6 mm × 0.4 mm with 0.4 mm spacing. So, the total occupied space of a 0402 discrete component is 1.45 mm × 0.85 mm rather than 1 mm × 0.5 mm. When the component clearance and mounting pads are accounted for, there becomes a substantial waste of the limited available board spaces [4].

## 1.2 Review of Competing Technologies

Around 1980's, the technology of through-hole packaging moved toward SMT. Today the use of integrated and integral passives are gaining popularity. They are defined by National Electronics Manufacturing Initiative (NEMI) in USA as a package containing more than one passive and possibly a few active elements in a single package (integrated) and passives either embedded in or incorporated on the surface of an interconnecting substrate (integral) [5].

Embedded passives which is an emerging technology area provides a method for achieving potentially significant size shrinkage by replacing surface mount components with embedded components in a multi-layer packaging environment. The embedded components, however, have different electrical characteristics as compared to discrete components due to their geometric structure and parasitic effects.

Therefore these effects should be characterized and carefully considered in high frequency applications.

For embedded passive components, several multi-layer technology options can be applied. With each packaging technology, a particular set of attributes exists that make that option a reasonable choice to be adopted. Each of these solutions has advantages, disadvantages, and limitations. The key attributes one would examine in choosing a particular packaging technology for current and future electronic devices are becoming more demanding.

The ideal system-on-chip (SOC) approach, a device containing digital, analog and RF of the entire system's functionality on a single semiconductor chip, is not well suited for integrated passive components because of the high interconnection loss by fine line wiring and the large electromagnetic coupling in the silicon substrate. With micro-electro-mechanical systems (MEMS) technology, by integrating mechanical elements (e.g., movable coil, variable capacitor, capacitive switch with actuation pads, and so on.) on a common silicon substrate through micro-fabrication technology, the performances of passive components (e.g., high-Q suspended inductor) are improved. However, the lack of CAD tools and the increasing pressure of very short time to market combined with a requirement for rapid upgrades of functionality and interface specifications, SOC technology is expected to result in production difficulties as well as financial and investment concerns in setting up wafer fabrication costs.

Instead of SOC technology, the alternative IC-level packaging solution is system-in-package (SIP). This approach allows two or more chips or components to be stacked by microbump bonding in a three-dimensional (3-D) structure. By using SIP technology, the most proper substrate and design rule for each chip to combine high performance with low cost can be realized. However, the key challenge of SIP is the manufacturing repair and the lack of adequate test methods.

The system-on-package (SOP) concept where active and passive components are integrated as part of the packaging has been an attractive option to build miniaturized high-performance modules. In contrast to SOC and SIP technologies, this is a system-level package containing multiple ICs and passives that integrates all the system functions. An SOP is more than a multichip module (MCM), which contains only digital wiring to interconnect ICs. By using multi-layer technology with high-density chip and embedded components, this 3-D technique emerged out of the potential for higher integration and more compact module size.

With apparently low cost and over 30 years of development, polymer technologies can offer sophisticated laminated printed circuit board (PCB). Glass-reinforced epoxy (FR-4), with limited high frequency properties, is the most common PCB substrate material of usage. To meet high-frequency applications and/or increase capacivity, new materials with improved dielectric loss (from 0.03 to 0.003) and low ($\varepsilon_r = 3$) [6] or high ($\varepsilon_r > 1000$) [7] dielectric constant are developed but they are generally more expensive than common polymer materials. High density interconnection (HDI) is an enhanced process to standard FR-4 boards [8]. By sequentially adding thin build-up dielectric layers with laser-drilled or photo-etched microvias (25 to 125μm diameter) [9] and fine line/space (down to 20 μm) resolution on either side of a standard FR-4 core, the circuit density and electric characteristics are improved; also the available space to embedded passive components becomes much larger than standard FR-4 boards. Multi-layer organic (MLO) technology, a cost effective process while offering design flexibility and integration, is getting more attentions in SOP applications [10]. At the Packaging Research Center, Georgia Institute of Technology (PRC-GT), MLO technology is being developed as part of the SOP research.

Low temperature co-fired ceramic (LTCC), using printing process on multiple

ceramic substrates, allows high circuit density for applications up to several tens of GHz. With the ability to fire the entire package at once, rather than sequentially as is done in traditional high temperature co-fire ceramic (HTCC), the layer count is only limited by the ability to have a firing profile that allows the burnout of organic binders for high tape layer count circuit. As a result of low-temperature sinterable ceramic materials (i.e., <900°C) [11], high conductivity conductor (e.g., silver and copper) rather than molybdenum or tungsten applied in HTCC process can be utilized. Since the vias formed by mechanical punching or laser drilling and the conductors printed on ceramic tape can be inspected before lamination, this process can produce a high number of layers with high yield [12]. LTCC, which has been investigated in many published papers [13]-[15] to integrate passive components in multi-layered ceramic, is also one of the most popular SOP technologies. The mentioned high-density packaging solutions are summarized in Fig. 1.2.

## 1.3 Organization of Dissertation

Using 3-D structure provided by multi-layer technology, the same function of passive components could be achieved by more flexible architectures. Inductors and capacitors are elementary and important parts in RF systems. With correct measurement and modeling, embedded capacitor and inductor can be applied as fundamental element in integrated passive circuit design. By MLO technology, these subjects, together with a “T-type” microstrip resonator used for the extraction of high frequency characteristics of different materials, are presented first in Chapter 2.

Common mode filter, which is used to suppress common-mode current for complying with various EMC standards, composed of two mutually coupled inductors is generally constructed by wire-wound configuration. In Chapter 3, design and analysis of a miniaturized common-mode filter using multi-layer LTCC technology is

discussed. In this chapter, an equivalent circuit model of the miniaturized common-mode filter with both overlapped and offset positive and negative traces configuration are designed and compared. Parameters extraction for the equivalent circuit model and measured results with defined specifications are also illustrated.

In high-speed digital system, compensation of fixed skew in clock distribution networks, parallel data buses, or between positive and negative traces of a differential pair is usually achieved by microstrip- or stripline-type meander delay line. These meander lines, 1000's of which can be found in the state-of-the-art PC platform, not only occupy the limited board space but also are dangerously coupled. To have better performance and miniaturized dimension, LTCC multi-layer technology with enhanced design is used to develop this passive component. Chapter 4 describes the design of a miniaturized multi-layer delay line with a delay of 233 ps, which is characterized by distributed parameters, using LTCC technology for high-speed digital applications. To improve the waveform distortion associated with the meander line structure, the designed structure is able to simultaneously contain the electromagnetic coupling among traces while maintaining stable characteristic impedance up to several GHz through the novel use of grounded guard traces.

Finally, conclusions of the topics investigated in this dissertation are discussed in Chapter 5. This is accompanied by recommendations for future work concerning how the performances of these components may be improved further.

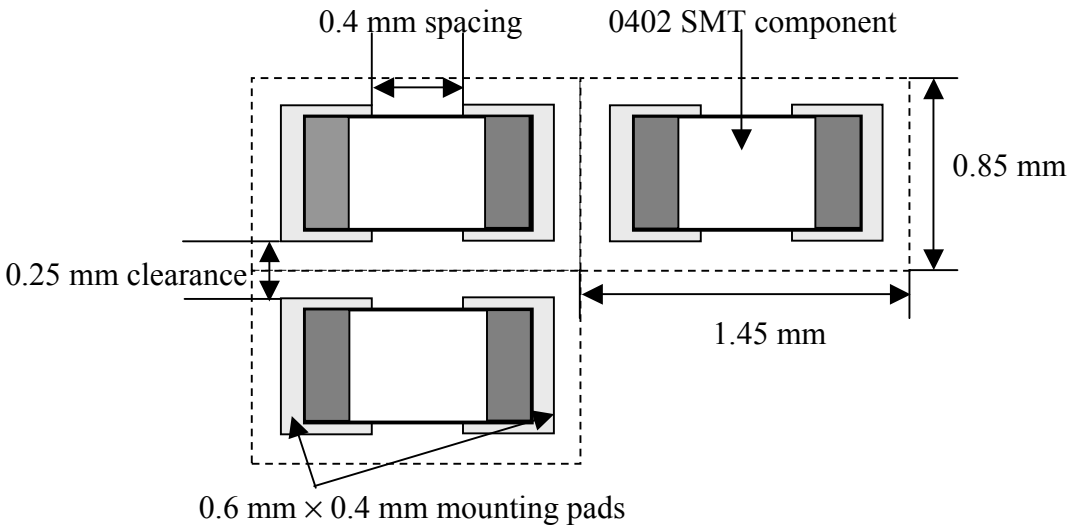



Fig. 1.1 Clearance and mounting pads of 0402 SMT component.

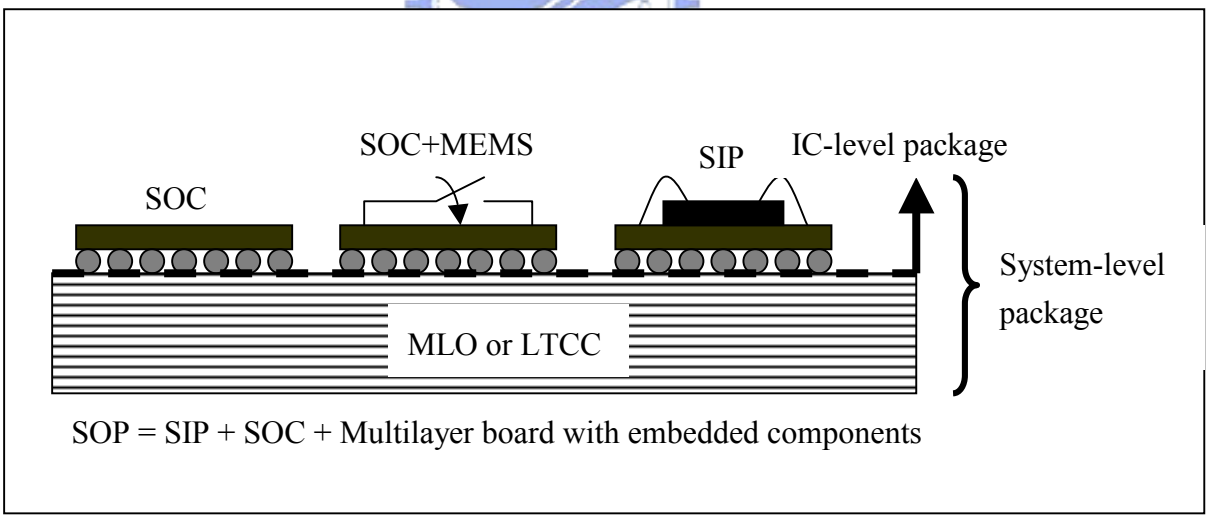



Fig. 1.2 Different level of high density packaging solutions.

# CHAPTER 2

# EMBEDDED CAPACITOR AND INDUCTOR IN MULTI-LAYER PRINTED CIRCUIT BOARD

## 2.1 Introduction

As wireless systems become more popular and applications grow, the advantages of high performance components become more apparent [16-17]. Inductors and capacitors, which are commonly used as stand-alone components or for forming an integral part of filters, matching networks, oscillators, mixers, amplifiers, and other RF circuits, are important parts in RF systems. When unsatisfactory inductors and/or capacitors are applied in RF circuit, the overall RF system performances (e.g., phase noise, power consumption, and so on) are degraded. Although high performance components can be obtained with the use of off-chip discrete components, this approach consumes valuable board space and its performance may be hampered by the introduction of potentially large parasitics due to component mounting pads, vias, and extra traces that exist between the chip and the devices.

The embedded passive component using MLO approach is one solution for new generation RF components and systems. Applications of multi-layer printed-circuit board had been widely prevailing in computer system and other digital circuits. For RF applications, it is possible to utilize the PCB process to embed the required passive components in the inner layers of the substrates and leave only a few components, such as active components and MMICs, on the surface layers of the circuit. This kind of circuit can, at least, in principle, be highly integrated. PCB with embedded inductors and capacitors can save space, reduce cost and improve

performance for modern portable products. Building passive components into laminated substrates has long been discussed, but many technical problems remain to be solved before mass production is feasible [5]. First of all, integrated passives will change the design process and much characterization and modeling must be done to allow designer to easily transition from the use of discrete components to integrated passives [18]. In addition, low cost and high performance materials that allow for tight tolerances, high capacivity and low series inductance are needed.

Due to the performance requirements in today's circuit system, capacitors for decoupling purpose must generally be placed as close to the active device as possible in order to minimize the effect of lead and trace inductances. Therefore, it is increasingly attractive to fabricate the capacitor into the substrate itself in order to place them near active circuitry and to enable chip placement over the integrated capacitors. Also, the form factor of embedded capacitor could be optimized to have minimal effective series inductance (ESL); integrated capacitors are expected to have better performance than discrete capacitors.

The solenoid inductor has the advantage that the main magnetic flux is parallel to the PCB surface, so the interference with the underlying circuit in modules is minimal. Also, this solenoid structure avoids the placement orientation introduced by the magnetic flux direction of the spiral-type, surface-mount, and discrete inductor. The disadvantage of the solenoid inductor is that it will suffer from considerable contact resistance between the repeated via and metal layers.

To further improve the component performance and obtain greater benefits of the embedded passives, multi-dielectric substrates with layer-specific dielectric constant and thickness can be used to design the embedded passives. In this chapter, the characterizations of various embedded passives components using network analyzer and probe station will be discussed first. Subsequently, a "T-type" microstrip

resonator used for the extraction of high frequency characteristics of different materials is presented. With these material characteristics we proceed to the design of various embedded capacitors and inductors in a 6-layer PCB. This is followed by a presentation of the method for converting the *S* parameters, measured by a vector network analyzer and probe station, into the frequency-dependent equivalent circuit model appropriate for each type of components.

## 2.2 Methods of Measurement and Deembedding

Models extracted from appropriate measurement processes can be quite reliable for use with circuit simulation programs. Two measurement techniques are generally applied in characterizing RF components: time-domain reflectometry (TDR)/time-domain transmission (TDT) [18] and frequency-domain network scattering parameter (*S*-parameter) measurement [19]. Although TDR/TDT technique could perform broadband parameter extraction (from DC to several GHz), its performance depends on the quality of the observed signal so the modeling accuracy may be limited. Frequency domain *S*-parameter measurement technique had long been applied in RF/ microwave network analysis. *S*-parameter measurement technique could measure frequency response of a device under test (DUT) accurately. By means of network analysis theory, electrical parameters of DUTs can be solved and explained [20].

To measure the components embedded in a multi-layer substrate, a high frequency probe station Summit 9000 (Cascade Microtech, Beaverton, OR) and a vector network analyzer Agilent 8510C (Agilent, Palo Alto, CA) are utilized. A multi-layer Thru-Reflect-Line (TRL) calibration [21] was performed first to de-embed the on-wafer measurement system and the related part of the test fixture. In order to cover wider frequency band, two calibration standard lines with different lengths of

1000 mils and 500 mils were utilized to cover the frequency band of 0.3-2.45 GHz and 0.6-4.9 GHz in the TRL calibration, respectively. Results shown in Fig. 2.1 and Fig. 2.2 verify the correctness of the multi-layer TRL calibration. In a straightforward manner, the wider measurement frequency band could be obtained with different line lengths.

## 2.3 Material Characterization

Typically, low frequency material characteristics up to approximately 100 MHz, is available based on capacitance measurements by inductance-capacitance-resistance (LCR) meters. Resonators have long been used to characterize the microwave properties of materials. To measure the characteristics of different substrates, a T-type 50-ohm microstrip resonator, as shown in Fig. 2.3, was used as the test pattern for measuring the properties of substrate in high frequency range [22].

With vector network analyzer the transmission response of the T-type resonator was measured and calculated. The resonator is an open-ended transmission line with stub length $l_{stub}$ that resonates at odd-integer multiples of its quarter-wavelength frequency. To determine the effective dielectric constant $\varepsilon_{eff}$, the resonant frequency $f_{res}$ that shows up as the first null of the transmission response is applied in the following equation

$$\varepsilon_{eff} = \left( \frac{c}{4 \times f_{res} \times l_{stub}} \right)^2 \tag{2.1}$$

where $c$ is the speed of light in free space. With the calculated effective dielectric constant $\varepsilon_{eff}$, the dielectric constant can be inverted from [20]

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left( 1 + 12 \frac{h}{w} \right)^{-1/2} \tag{2.2}$$

where $w$ and $h$ are the line width and substrate thickness of the T-type resonator, respectively. Fig. 2.4 is a $S_{21}$ frequency response example of the T-type resonator and shows a first resonant frequency of 1.79 GHz.

With substrate $Q$-factor $Q_d$ measured by a Model-03 split-cavity (Damaskos, Concordville, PA) as shown in Fig. 2.5, the loss tangent of material at each resonant frequency is calculated by the following equation [23]:

$$\tan\delta = \frac{\varepsilon_{eff}(\varepsilon_r - 1)}{Q_d \times \varepsilon_r(\varepsilon_{eff} - 1)} \tag{2.3}$$

where

$\tan\delta$ = loss tangent of the dielectric substrate
$\varepsilon_{eff}$ = effective dielectric constant
$\varepsilon_r$ = dielectric constant
$Q_d$ = $Q$-factor of the dielectric substrate

The dielectric constant and loss tangent of three different substrates measured at 4 different frequencies of interest to current wireless communication applications are summarized in Table 2.1 and Table 2.2. Compared to the vendor-supplied data as listed in Table 2.3, the correspondence is good and the small discrepancy for the loss tangent of BT material may come from material variation.

| Frequency / Material | 0.9 GHz | 1.8 GHz | 2.4 GHz | 5.7 GHz |
|---|---|---|---|---|
| FR-5 | 4.6 | 4.5 | 4.5 | 4.5 |
| BT | 4.4 | 4.4 | 4.4 | 4.5 |
| High Dk | 36.56 | 35.67 | 35.19 | 35.60 |

Table 2.1. Dielectric constant of various substrates at different frequencies.

| Frequency / Material | 0.9 GHz | 1.8 GHz | 2.4 GHz | 5.7 GHz |
|---|---|---|---|---|
| FR-5 | 0.0185 | 0.0185 | 0.0184 | 0.0183 |
| BT | 0.0187 | 0.0187 | 0.0187 | 0.0185 |
| High Dk | 0.043 | 0.046 | 0.0517 | 0.0597 |

Table 2.2. Loss tangent of various substrates at different frequencies.

| | Dielectric constant | | Loss tangent | |
|---|---|---|---|---|
| Frequency / Material | 1 MHz | 1 GHz | 1 MHz | 1 GHz |
| FR-5 | 4.6-4.8 | 4.5 | 0.014-0.015 | 0.0176 |
| BT | 4.7 | 4.4 | 0.006-0.008 | 0.013 |
| High Dk | 40 | N/A | 0.03 | N/A |

Table 2.3. Vendor supplied dielectric constant and loss tangent of various substrates at different frequencies.

## 2.4 Test Pattern Measurements and Models

To meet wireless applications, including GSM (i.e., 900 MHz and 1800 MHz), 2.4/5.8 GHz industrial, scientific and medical (ISM) bands and so on, the range of capacitance and inductance of designed embedded capacitor and inductor are focused on EIA 0402 C0G multi-layer ceramic capacitor (MLCC) and EIA 0402 multi-layer ceramic inductor (MLCI), which cover most of the wireless application requirements and corresponding to capacitance in the range of 0.5 pF to 1000 pF and inductance in the range of 1 nH to 56 nH, respectively.

With the characteristics of various substrates, as listed in Tables 2.1 and 2.2, a series of design exercises were conducted to characterize the embedded MIM (Metal-Insulator-Metal) capacitor with different dimensions and solenoid inductor with various number of turns. The samples have been measured using the vector

network analyzer through a high frequency coplanar waveguide probe ACP40 (Cascade Microtech, Beaverton, OR) with 250 μm pitch size. The multi-layer TRL calibration was performed first to de-embed the on-wafer measurement system. The layer assignment of the 6-layer PCB incorporating three FR-5 substrates and two high dielectric constant (high Dk) substrates of specific thickness is illustrated in Fig. 2.6.

### *2.4.1 Characterization of Embedded Capacitor*

As shown in Fig. 2.7(a), square MIM embedded capacitor of different sizes $W$ were designed and tested. In addition, to increase the effective area for obtaining higher capacitance, a 4-layer vertically inter-digitated capacitor (VIC) topology was also designed. As shown in Fig. 2.7(b), this capacitor can be viewed as being formed by 3 MIM capacitors connected in parallel.

Parasitics associated with the component, which affect the high-frequency behavior of the embedded element, is a fundamental problem in designing embedded passive components. From the structure of the MIM capacitor, a π model [24] was constructed and shown in Fig. 2.8. The lumped model is suitable to cover the entire frequency band of interest here. In this model, series $C$ represents the main capacitor of concern, $L_P$'s are the parasitic series inductances, $C_g$'s are capacitors to ground, and the resistance $R$ represents the equivalent series resistance (ESR).

From the ideal parallel-plate approximation of square MIM capacitor, we know that its capacitance $C_{ideal}$ is directly proportional to the square of its width $W$

$$C_{ideal} = \varepsilon_0 \varepsilon_r \times \frac{W^2}{d} \tag{2.4}$$

where $d$ is the insulator thickness and $\varepsilon_0$ is the permittivity of free space. The fringing capacitance $C_f$, which is caused by the fringing field at the edge of the parallel plate and can be transformed into an excess effective width, is counted as part

of the total effective capacitance $C_{eff}$.

$$C_{eff} = C_{ideal} + C_f \tag{2.5}$$

But as width $W$ increases, the percentage of this fringing capacitance to the total capacitance will decrease [25]. The extracted effective capacitance including fringing capacitance and parasitics of the 2-layer and 4-layer MIM embedded capacitors with different dimensions is demonstrated in Table 2.4 and Table 2.5. As can be seen in these Tables, the effctive capacitance $C_{eff}$ is almost proportional to $W^2$ in our designed structure. Fig. 2.9 illustrates the capacitance *vs*. dimension for the tested capacitors.

| 2-layer MIM (High dielectric substrate) | | | | | |
|---|---|---|---|---|---|
| | W=100 mil | W=200 mil | W=300 mil | W=400 mil | W=500 mil |
| $C_{eff}$ (pF) | 22.95 | 90.87 | 198.23 | 339.88 | 549.81 |

Table 2.4 Extracted capacitance of 2-layer square MIM embedded capacitors with different dimensions.

| 4-layer VIC (Dielectric substrates: 2 layer high dielectric & 1 layer FR-5) | | | | | |
|---|---|---|---|---|---|
| | W=100 mil | W=200 mil | W=300 mil | W=400 mil | W=500 mil |
| $C_{eff}$ (pF) | 40.36 | 174.80 | 392.61 | 707.05 | 1079.65 |

Table 2.5 Extracted capacitance of 4-layer square MIM embedded capacitors with different dimensions.

### *2.4.2 Characterization of Embedded Inductor*

Solenoid inductors with different square cross-sectional dimensions $D$ and turns $N$ as shown in Fig. 2.10 were also designed and tested, where metal trace patterns $M_1$ and $M_2$, both with 6-mil width and 8-mil spacing $S$, are on different layers. By using the equivalent lumped-circuit model represented in Fig. 2.11 [26], the solenoid

inductor can be modeled with good accuracy. In this model, series $L$ represents the main inductor of concern, $C_P$ is the parasitic parallel capacitance of the winding itself, $C_g$'s and $R_g$'s are capacitors and resistors to ground, and the series resistance $R$ represents the ESR.

From Wheeler's approximated equation of single-layer air-core solenoid inductor with circular cross-section, the inductance $L$ is directly proportional to the core area and square of its number of turns $N$ [27].

$$L = \frac{0.394 r^2 N^2}{9r + 10l} \tag{2.6}$$

where $r$ is the coil radius in cm, $l$ is the coil length in cm and $L$ is the inductance in μH. This formula is most accurate when the solenoid traces is tightly wound and its length $l$ is greater than $0.67r$. Due to the large spacing $S$, non-magnetic permeability and insufficient number of turns $N$, considerable interwinding magnetic flux leakage and end fringing are anticipated, thus the effective inductance $L_{eff}$ is not proportional to $N^2$ and $D^2$.

| | D=35 mil, N=1 | D=35 mil, N=2 | D=35 mil, N=3 | D=35 mil, N=4 | D=35 mil, N=5 | D=70 mil, N=1 | D=70 mil, N=2 |
|---|---|---|---|---|---|---|---|
| $L_{eff}$ (nH) | 0.65 | 1.36 | 1.98 | 2.68 | 3.26 | 1.05 | 2.30 |

Table 2.6 Extracted inductance of solenoid inductor with different number of turns and width.

Including all the parasitics shown in Fig. 2.11, the extracted effective inductance $L_{eff}$ of the solenoid inductors with different dimensions and turns are listed in Table

2.6. As can be seen, the effctive inductance $L_{eff}$ is only proportional to $N$, instead of $N^2$, in our designed structure. Fig. 2.12 shows the inductance value *vs.* number of turns for the designed inductors.

## 2.5 Conclusion

The factors driving passive integration technology include higher operating frequencies, which require smaller parasitics than discretes can provide, and overall system miniaturization and/or functionalities (i.e., higher component/packaging density and/or parts count). MLO technology has the potential for achieving denser packaging, more efficient manufacturing processes, better reliability and future replacement of many surface mount devices that will result in savings of volume, weight and cost.

From the above results, the embedded passive components with MLO technology exhibit some limitations in RF applications, which still require further improvements in materials and processes. To cover the inductance range in wireless applications, the designed embedded inductor should be improved. The development of HDI substrate as an enabling technology for improving the circuit density, electric characteristics and integrating passives components is noted. By means of the fine line/spacing resolution and microvias, the interwinding magnetic flux leakage of embedded solenoid inductor could be improved. In addition, high permeability materials with partial filled (i.e., core filled) process to further decrease magnetic leakage, high dielectric constant to increase capacivity and low dielectric loss to improve $Q$-factor are still needed for applications in high frequency system.

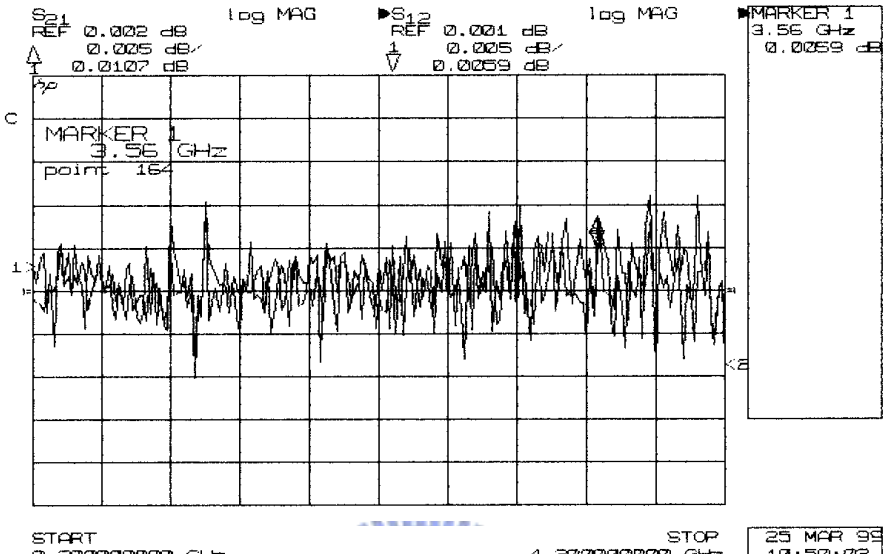



Fig. 2.1 Magnitudes of $S_{12}$ and $S_{21}$ of 500 mils and 1000 mils through lines used in the multi-layer TRL calibration experiment.

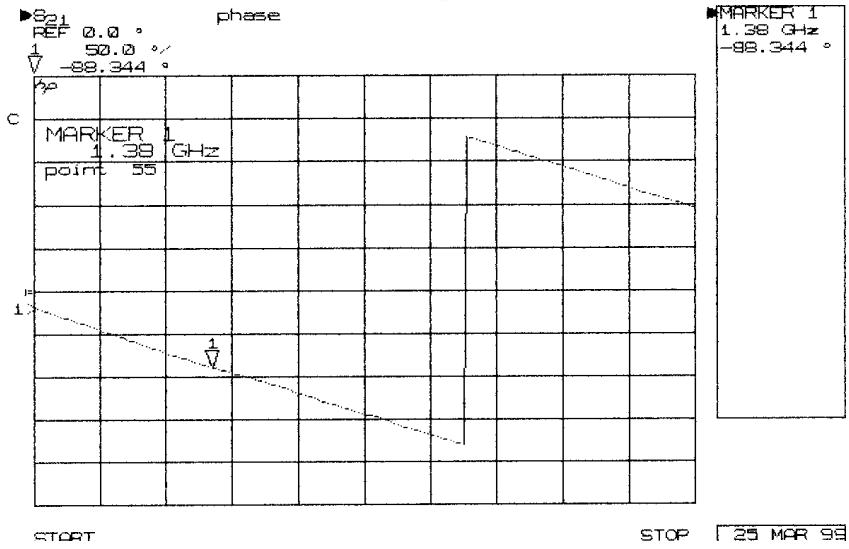



Fig. 2.2 Phase response of 500 mils and 1000 mils through lines used in the multi-layer TRL calibration experiment.

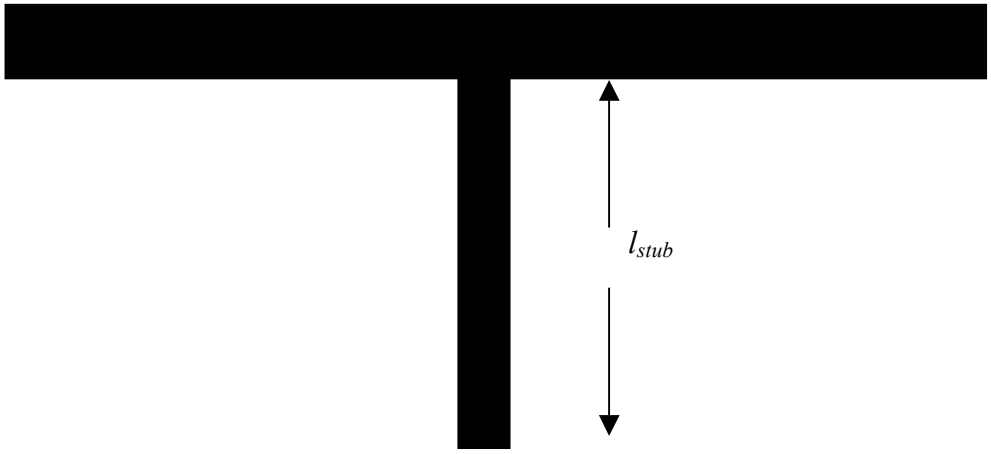



Fig. 2.3 Structure of a T-resonator.

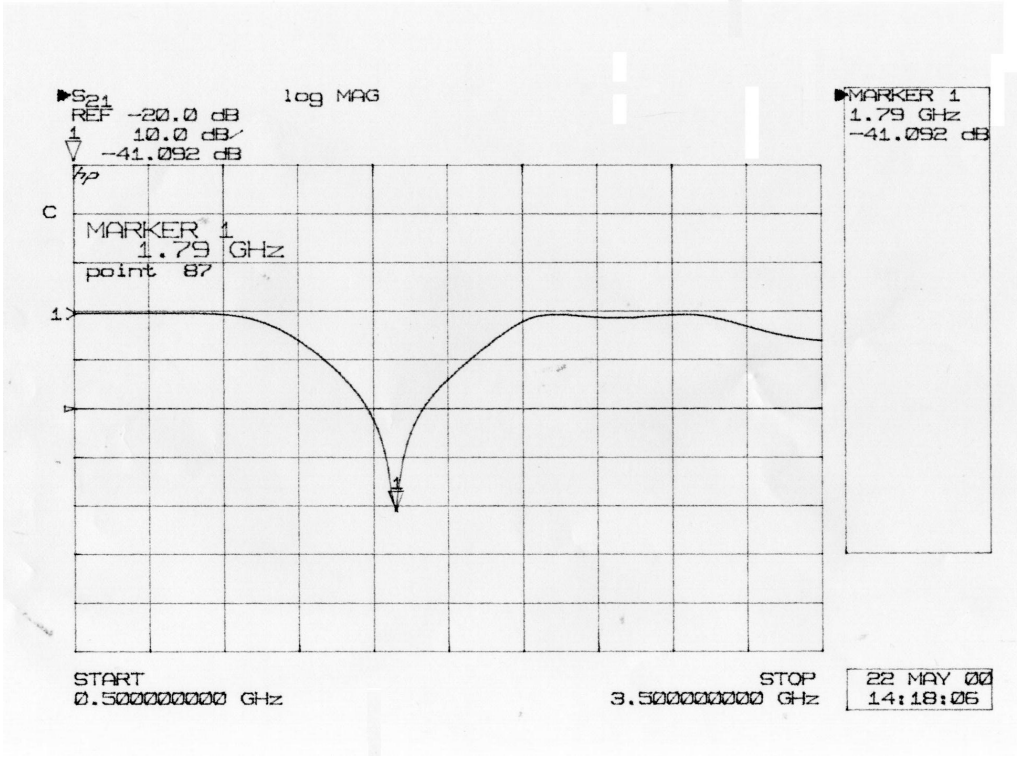



Fig. 2.4 Example frequency response of $S_{21}$ of a T-type resonator.

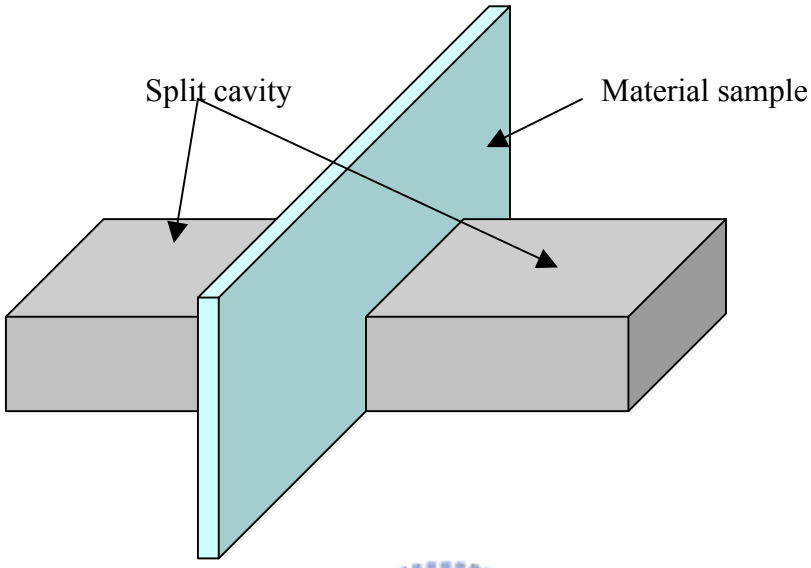



Fig. 2.5 Structure of split-cavity resonator.

Thickness of Cu: 1 oz. Unit: mil

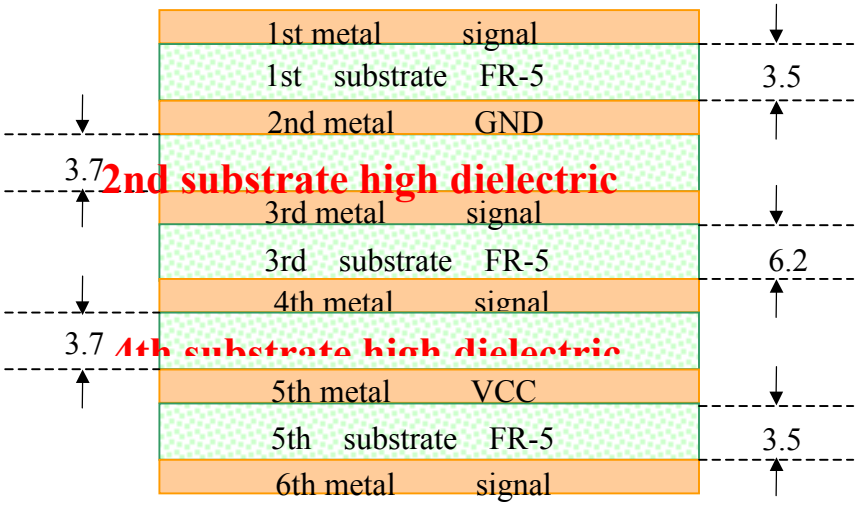



Fig. 2.6 Layer assignment of the 6-layer PCB test board.

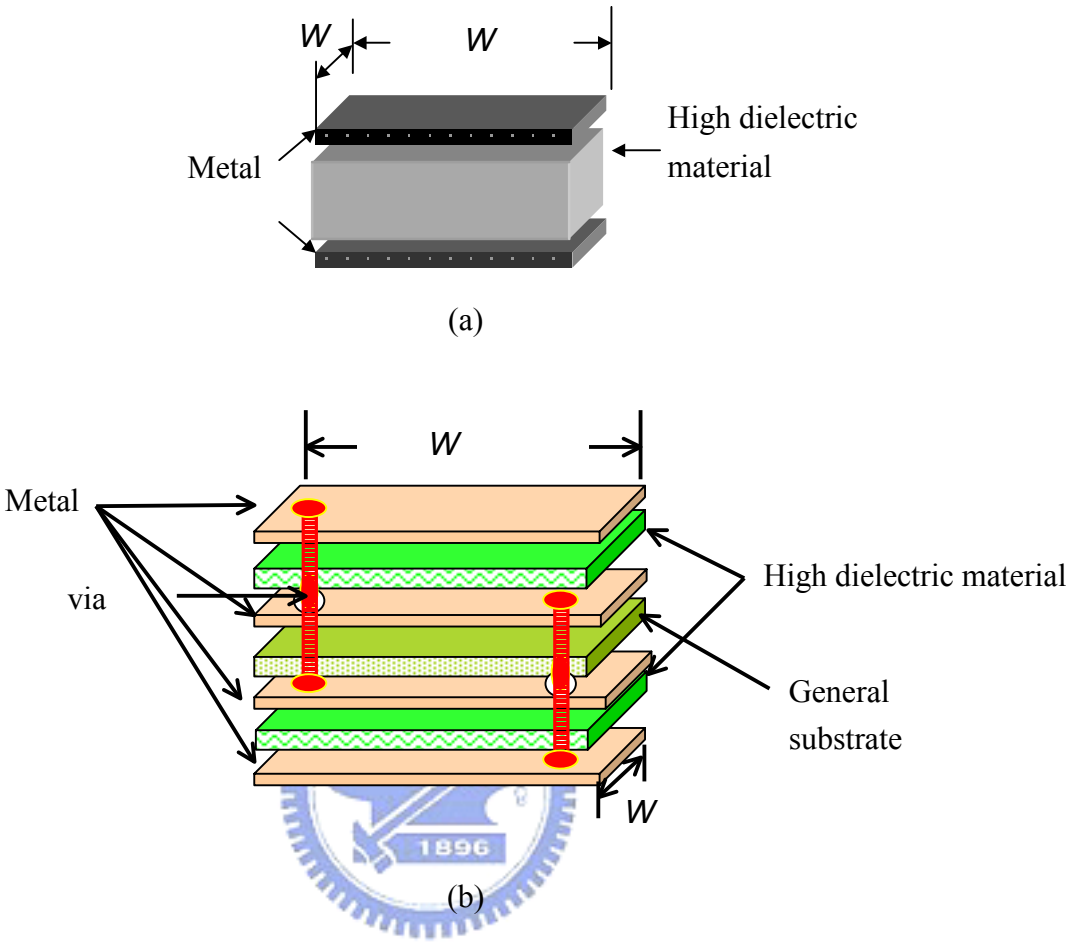



Fig. 2.7 Structures of: (a) 2-layer MIM capacitor and (b) 4-layer MIM capacitor.

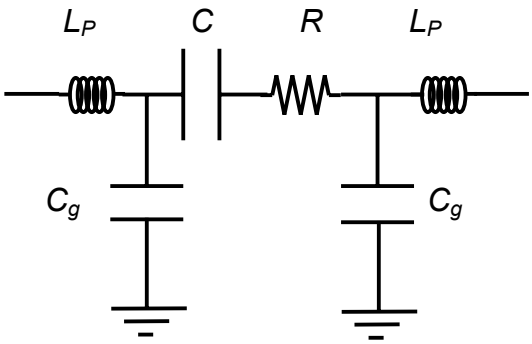



Fig. 2.8 Lumped-element model of a MIM capacitor.

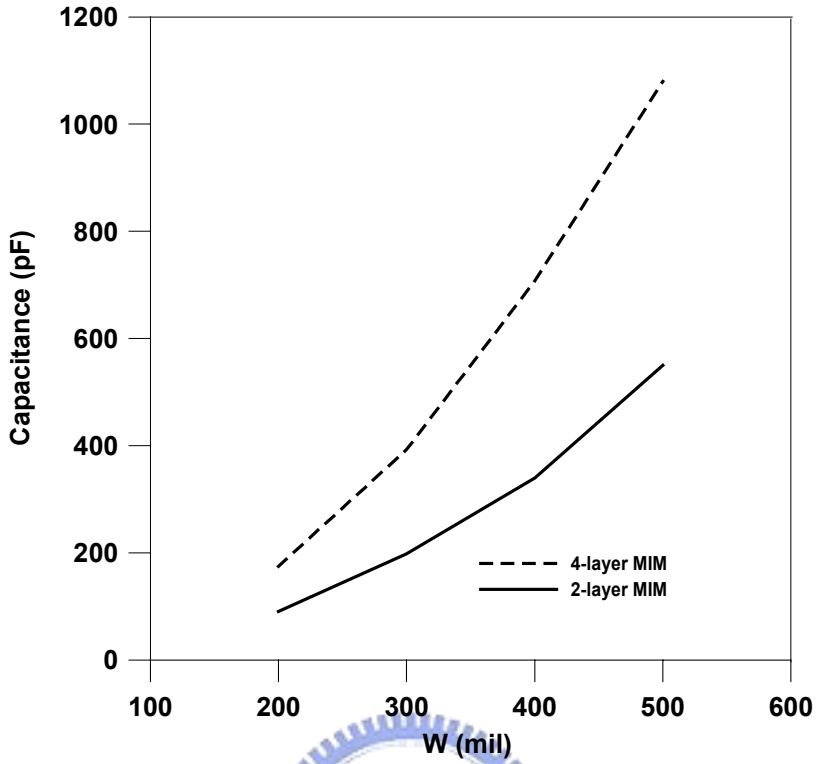



Fig. 2.9 The capacitance *vs*. dimension for the multi-layer MIM capacitors.

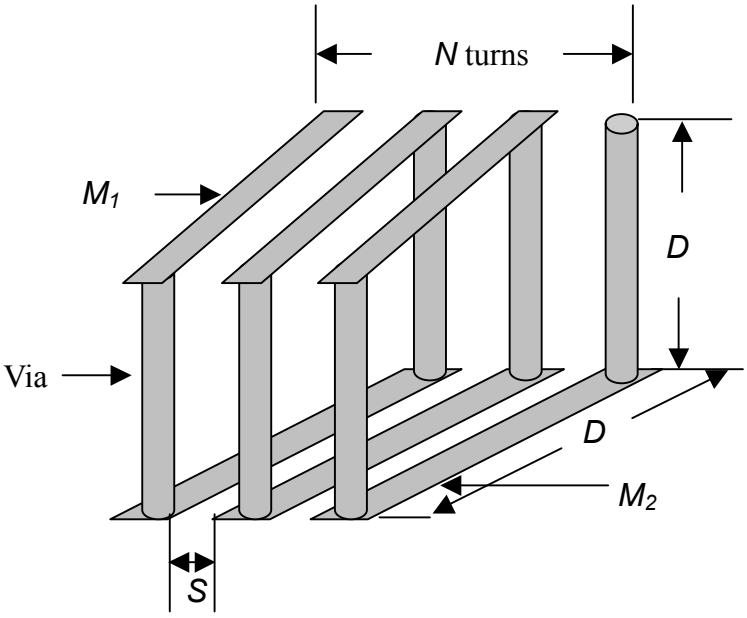



Fig. 2.10 Structure of a *N*-turn solenoid inductor.

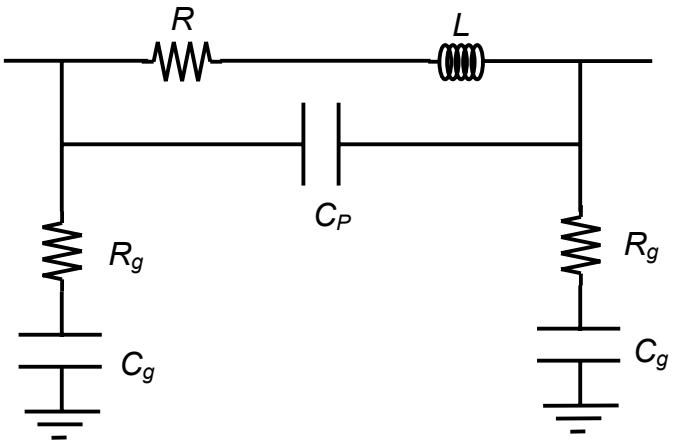



Fig. 2.11 Lumped-element model of a solenoid inductor.

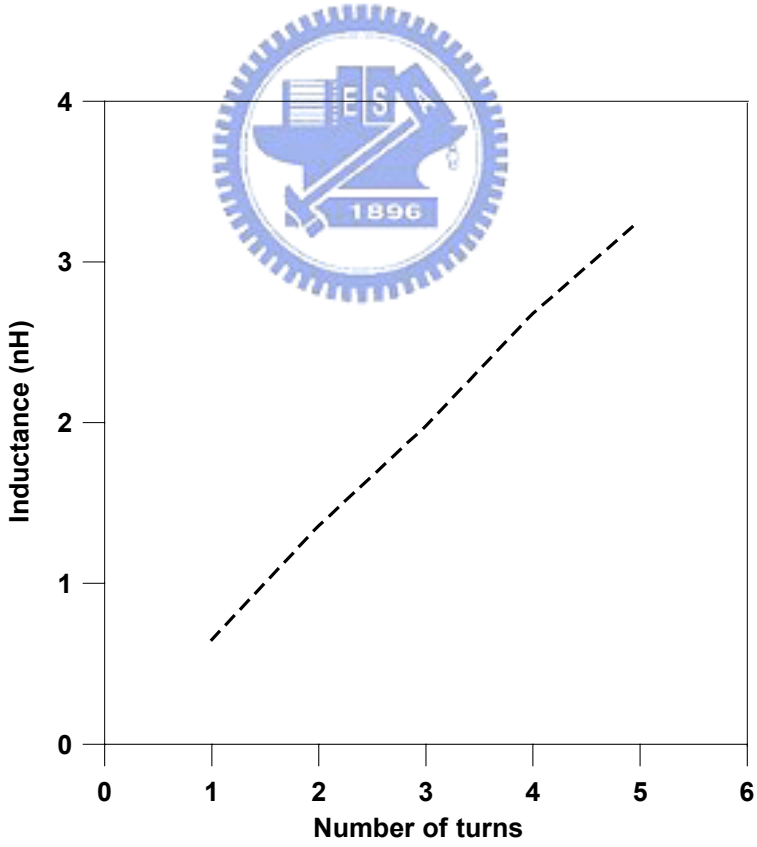



Fig. 2.12 The inductance *vs*. number of turns for the solenoid inductor.

# CHAPTER 3

# DESIGN OF MINIATURIZED COMMON-MODE FILTER BY MULTI-LAYER LOW TEMPERATURE CO-FIRED CERAMIC

## 3.1 Introduction

With increasing demands on system functionality and data storage, higher data rate in electronic devices is requested. In proportion to the higher operating speed and frequency band, more unwanted electromagnetic radiation is introduced. High-speed data transmission together with ever-lower logic threshold voltage makes today's electronic sets extremely vulnerable to the problem of unwanted noise. In high speed transmission, signal integrity of the transferred data is a critical issue, even total system may suffer from malfunction when sufficient radiation noise is picked up by the interface cables or digital devices [24].

In high-speed data communication, differential signaling has found increasing applications (e.g., IEEE 1394, USB 2.0, Gigabit Ethernet, and so on). When two equal-amplitude and 180 degrees out of phase signals are transmitted through a pair of traces, with which a signal on a trace is designed to reference to the signal on another trace, it is operating in a differential signaling scheme. The two traces are known as a differential or balanced pair. In principle, by this electrically symmetrical referencing architecture, common-mode noise picked up by the differential pair will be subtracted. For this reason, differential circuit inherently exhibits better immunity to noise and has been therefore gaining popularity in recent years as data rate demand increases.

Although the ideal differential transmission pair can enhance the immunity capability in noisy environment, discrepancy occurs in delay or path loss between the paired traces, following imbalanced phase and/or amplitude resulted in the source, load, or the circuit path, common-mode current will be introduced [28]. These currents are conducted on the differential pair in the same direction and can act as dominant source of radiated emission at high frequencies. Several published papers [29]-[32] have investigated and analyzed the common-mode current influences. To comply with the various EMC standards, these common-mode currents need to be restricted and suppressed low enough.

Common-mode toroid choke, in the form of 1:1 longitudinal transformer, is one of the most general methods used to reduce common-mode current [33]. Such a choke is actually a 1:1 transformer consisting of a pair of coils wound around a common ferrite toroid. The effectiveness of the common-mode toroid choke relies on the assumption that the high permeability makes the self and mutual inductance equal. In the ideal conditions, the differential-mode current flow through both windings in opposite directions which generate two mutually canceling magnetic fluxes, with their loading effects represented by the subtracting self-inductance and mutual inductance, thus the functional signal can ideally pass the magnetic core smoothly and only be attenuated by ohmic resistances of traces and core material. The common-mode current however, by virtue of additive magnetic fluxes, is effectively “choked” as a result of the complete magnetically coupled high common-mode inductance. The higher permeability ferrite cores can concentrate more flux in the core and reduce any leakage flux. At frequencies on the order of GHz or more, the highly degraded effective permeability and severe material loss of ferrite core might compromise the effectiveness of such ferrite choke. Furthermore, the short wavelength of high frequency signal may become comparable to the

electrical length of the choke coils. Consequently, any small variation in reproducibility of coils and ferrite material may result in significantly degraded performance. Further, the size of the toroid is difficult to reduce, which contribute to effort toward developing alternative multi-layer structures with much improved process tolerance and high-frequency material loss [34], [35].

In this chapter, the design of a common-mode filter using multi-layer LTCC technology for high-data-rate-applications is presented. The design is to achieve sufficient common-mode suppression while introducing minimal pass-band insertion loss and mode conversion to the desired differential-mode signal. This chapter consists of following aspects: in Section 3.2, the designing and equivalent circuit modeling of multi-layer LTCC common-mode filter is presented first, which is followed by the miniaturized offset design. Section 3.3 discusses the extraction of the equivalent circuit model parameters and illustrates some measured results with the specifications defined at USB-IF (http://www.usb.org/). Finally, Section 3.4 gives a summary and some concluding remarks.

## 3.2 Design and Modeling

### *3.2.1 Equivalent Circuit Model of Multi-Layer Common-Mode Filter*

Figure 3.1 shows the structure of multi-layer common-mode filter and its equivalent circuit model, which is represented as a coupled equivalent lumped-circuit, is demonstrated in Fig. 3.2. The multiple equivalent lumped-circuit sections are used to represent the plurality of differential pairs in the designed multi-layer structure. Each section contains a pair of coupled inductances $L_S$ with series resistances $R_S$ accounting for wiring resistance, shunt resistance $R_P$ signifying the dielectric loss, and a parallel capacitance $C_P$ representing capacitive coupling between positive and negative coils in adjacent layers. In addition, series capacitance $C_S$

denotes the parasitic winding capacitance of each coil. The grounded $R$ and shunt $L$-$C$ of each trace account for antenna effect of the distributed solenoid coil and parasitic coupling between coils and the ground plane of the test board. The magnetic coupling between adjacent differential traces is represented by the coupling coefficient $K$. With equal vertical spacing (i.e., layer thickness) $D$ of each differential pair, the coupling coefficient $K$ is assumed to be equal for all sections. The equivalent lumped inductance and resistance $L_S$ and $R_S$ are directly proportional to the length of the coil on each substrate. At higher frequencies, equivalent lumped-circuit representation of a distributed transmission line dictates the use of more than one section per layer. This can be done in a straightforward manner, details of which are therefore skipped here.

The typical single-ended scattering parameters ($S$ parameters) are not sufficient to accurately characterize a differential component operating in differential mode. To have a solid analysis on a differential device, mixed-mode $S$ parameters are introduced [36]. The generalized mixed-mode $S$ parameters can be given as:

$$
\begin{aligned}
b_{dm1} &= s_{dd11}a_{dm1} + s_{dd12}a_{dm2} + s_{dc11}a_{cm1} + s_{dc12}a_{cm2} \\
b_{dm2} &= s_{dd21}a_{dm1} + s_{dd22}a_{dm2} + s_{dc21}a_{cm1} + s_{dc22}a_{cm2} \\
b_{cm1} &= s_{cd11}a_{dm1} + s_{cd12}a_{dm2} + s_{cc11}a_{cm1} + s_{cc12}a_{cm2} \\
b_{cm2} &= s_{cd21}a_{dm1} + s_{cd22}a_{dm2} + s_{cc21}a_{cm1} + s_{cc22}a_{cm2}
\end{aligned} \tag{3.1}
$$

where $a_{dmn}$ and $a_{cmn}$ are the normalized differential- and common-mode incident waves from port $n$, $b_{dmn}$ and $b_{cmn}$ are the corresponding normalized differential- and common-mode reflected waves. With mixed-mode $S$ parameters, a complete characterization of the multi-layer common-mode filter, including the differential-mode, common-mode, and any mode conversion responses, are revealed.

The general 4-port single-ended *S* parameters can be converted to 2-port mixed-mode *S* parameters by using the circuit shown in Fig. 3.3 [37]. To perform the differential-mode conversion and provide the mechanism for the common-mode terms, a center-tapped balun is used. The common-mode conversion occurs at the center tap of the balun where only common-mode signals will appear because of the characteristics of the balun. These common-mode signals are then terminated through a balun into common-mode port. By applying this configuration, differential device represented by general 4-port single-ended *S* parameters are converted to 2-port mixed-mode parameters first. Subsequently, the parameters associated with the equivalent circuit of Fig. 3.2 are extracted and used to fine-tune the structural parameters for the optimization of differential- and common-mode performances and the minimization of component size.

### *3.2.2 Design of Multi-Layer Common-Mode Filter*

Exploring the significant recent advances in the LTCC process techniques for high frequency application, a multi-layer structure using ceramic substrate with relative permeability 1, relative permittivity 4.8, and dielectric loss tangent 0.0016, is designed by employing symmetric structure similar to, but without the drawbacks of, wire-wound common-mode choke. By using longer coupling traces, the lower permeability and the resulting smaller inductance as compared to ferrite material can be compensated. To have long coupling traces, a 3-D multi-layer structure with multi-turn square spiral on each layer is formed. Each substrate is printed with conductive silver coil pattern and via holes. Positive coils and negative coils are formed on alternate substrates. After all the substrates are stacked, each positive coil is then connected in a sequence through the first plurality of via holes. Similarly the negative coils are connected as a sequence through the second plurality

of via holes.

In such design, the dielectric and conductor losses are minimized; so any functional signal deterioration may occur mainly from signal reflection [34]. To achieve negligible effect on the transition edges (i.e., the high-frequency components) of differential digital signal, optimized characteristic impedance matching is needed. With good differential signal matching, the insertion loss incurred on the functional signal, evaluated by $S_{dd21}$ of the mixed-mode $S$ parameters, will be minimal over its intended operating bandwidth such that differential signal passes through the component undisturbed.

To design such optimum differential mode impedance, a full-wave, 3-D finite element method (FEM) simulator HFSS (Ansoft, Pittsburgh, PA) was utilized. As a first example, the spiral patterns in all layers are perfectly aligned. The line width $W$, horizontal trace spacing $S$, vertical spacing between positive and negative coil in each differential pair $D$, and vertical spacing $H$ between adjacent differential pairs, as shown in Fig. 3.1, are parameters used to design an optimized matching. In principle, for the given $W$ and $S$, different $D$ and $H$ combinations can be used to design different characteristic impedances by varying $K$ and $C_P$. For simplicity, $D$ and $H$ are assigned the same value. Using USB 2.0 as an example, the 90 ohms differential characteristic impedance can be obtained with $W = S = 75$ μm and $D = H = 140$ μm. Figure 3.4 depicts the designed filter composed of 4 sets of differential pair and the input/output terminations. To compensate the difference in electrical length of the two differential traces so as to maintain phase balance, one additional layer (i.e., layer M9) for trace length compensation is added.

The simulated results of the designed multi-layer common-mode filter with mixed-mode $S$ parameters are shown in Fig. 3.5. The $S_{dd21}$ curve represents the insertion loss of differential signal, $S_{dd11}$ curve denotes the reflection coefficient of

differential signal, and $S_{cc21}$ is the attenuation of common-mode signal. With both conductor and dielectric losses considered in the simulation, this designed filter provides better than 10 dB common-mode attenuation over the frequency range from 0.273 GHz to 1.74 GHz, very low differential-mode insertion loss of $S_{dd21}$ > - 0.2 dB up to 1.7 GHz, and good differential-mode matching with $S_{dd11}$ < -10 dB up to 2 GHz. To confirm the symmetric property of the multi-layer design, mode conversion *S* parameters $S_{cd21}$ and $S_{dc21}$ are simulated and shown in Fig. 3.6. The small value, less than -20 dB, in the entire frequency band ensures the negligible mode conversion is achieved in the designed filter. So only little input energy is converted from differential signal to common-mode noise (i.e., evaluated by $S_{cd21}$) and only insignificant fraction of input power is transferred from common-mode noise to differential signal (i.e., analyzed by $S_{dc21}$) at the output of the component. Given such performances, the designed common-mode filter appears capable of supporting broadband differential signaling while simultaneously suppressing the unwanted common-mode noise.

The designed filter is fitted in an EIA 1206 form factor (i.e., surface dimension 3.2 mm × 1.6 mm). The total occupied component thickness with 12 μm conductor thickness and the 10 foil substrates is 1.508 mm. It becomes an unusually thick component and a serious problem with which is that, with the width and thickness being almost equal, it is not convenient to differentiate the orientation of component and therefore not suitable for SMT assembly. Novel design to shrink the component thickness is thus required.

### *3.2.3 Miniaturization of Multi-Layer Common-Mode Filter*

In the previous design, the positive traces and negative traces in alternate layers are completely overlapped in vertical direction as depicted in Fig. 3.7(a). The

differential-mode characteristic impedance of the transmission pair is determined mainly by the stray inductance and capacitance of traces. Equation for differential-mode characteristic impedance $Z_{0d}$ can be expressed as follow:

$$Z_{0d} = 2 \times \sqrt{\frac{r_s + jwl_s(1-K)}{1/r_p + jwc_p}} \tag{3.2}$$

$$K = \frac{M}{L} \tag{3.3}$$

where $K$ represents the magnetic coupling coefficient between the two differential traces and $r_s$, $r_p$, $l_s$, and $c_p$ are the per unit length series resistance, parallel resistance, stray inductance, and stray capacitance of the transmission lines, respectively. The self-inductances of each winding are represented by $L$ and the mutual inductance is represented by $M$.

To shrink the thickness of component, a thinner substrate is needed. The thinner the substrate, however, the larger the parasitic capacitance $c_p$ is introduced and lowered $Z_{0d}$ would result if unattended. Solutions used to overcome the large parasitic capacitance include narrowing the overlapping traces and/or using lower dielectric constant material. However, with the general process capability nowadays, forming the narrower traces is difficult to perform. In the other solution, even with the lower dielectric constant material (i.e., $\varepsilon_r$ = 4.3 is the dielectric constant available for the state-of-the-art LTCC process) applied, it was not found to result in significant decrease in the component thickness.

Alternatively, the capacitance associated with thin substrate can be lowered by horizontally displacing the originally overlapping traces, that is, an offset design is applied. As shown in Fig. 3.7(b), for a given layer thickness $D$, when the horizontal offset ($T$) between traces in adjacent layers increases the capacitance between traces

decreases. For a given capacitance, the larger the offset distance, the thinner the substrate foil can be used, which should result in a reduction in the overall thickness of the component.

Figure 3.8 demonstrates the simulated result for the offset structure. A 90 μm foil substrate with a 75 μm offset distance is employed in this design. As can be seen in the figure, $S_{dd11}$ remains lower than -10 dB from DC to 2 GHz. Also, $S_{dd21}$ is better than -0.2 dB at the operation frequency (i.e., 240 MHz) and its higher harmonics. For noise elimination, $S_{cc21}$ is better than 10 dB from 0.239 GHz to 2 GHz. From 0.49 GHz to 1.11 GHz, the attenuation on common-mode noise is even larger than 20 dB. To check its mode conversion performance, $S_{cd21}$ and $S_{dc21}$ are simulated and displayed in Fig. 3.9. Comparing Figs. 3.6 and 3.9, one can see that asymmetry between the displaced traces results in poorer, but yet acceptable (i.e., better than –20 dB), mode conversion performance. Comparing Figs. 3.5 and 3.8, it is concluded that, while offering comparable or even better performance, the filter designed with offset concept has an overall thickness of 1.008 mm, which is 33% less than the original design using completely overlapping traces.

## 3.3 Results and Discussion

### *3.3.1 S-Parameter Measurements and Extractions of Equivalent Circuit Parameters*

According to the two different multi-layer designs mentioned above, samples are fabricated by LTCC process and measured by using an Agilent E5071B ENA series 4-port vector network analyzer. An SOLT (Short-Open-Load-Through) calibration is performed first to de-embed the measurement system and to shift the reference plane to the input/output connectors. To measure the fabricated components, a test board made of FR-4 with 4 feeding traces is applied. By the identical simulated 2-port *S*

parameters of the 4 feeding traces, the effect of the test board is de-embedded. Figure 10 demonstrates the good agreement between the simulated and measured results of the offset design.

Due to the long trace length (about 15 mm) on each layer, a multiple sections equivalent circuit is required to obtain a representative equivalent circuit model at high frequency. To extract the parameters of elements used in the equivalent circuit model, the individual inductor is simulated and characterized first [18]. As depicted in Fig. 3.4, the input pair arranged on the top pair of foils (i.e., M1-M2) has shorter length than the internal pairs (i.e., M3-M4 and M5-M6); this is also the case for the bottom output pair (i.e., M7-M8). For simplicity, the circuit parameters associated with the compensated length on the bottom layer M9 is combined into that of the last pair. With these extracted parameters, $L_S$ and $R_S$ of each inductor, the coupling coefficient $K$, and parasitic capacitances $C_S$ and $C_P$ are then derived by curve fitting. The simulated mixed-mode $S$ parameters $S_{dd21}$ and $S_{cc21}$are simultaneously fitted with the equivalent circuit. Finally, the value of insulation resistance $R_P$ is used to adjust the attenuation depth on the resonance frequency of $S_{cc21}$.

As displayed in all simulated and measured figures, at 1.74 GHz an abrupt change occurs both on $S_{dd21}$ and $S_{cc21}$. By checking the power conservation, it's found to result from an inefficient antenna effect of the long distributed solenoid coil and parasitic coupling between coils and the ground plane of the test board [38]. The grounded $R$ and shunt $L$-$C$ resonator, as shown in Fig. 3.2, is applied to signify these phenomenons, respectively. With 3300-ohm radiation resistance and resonator composed of 820 nH inductance and 0.01 pF capacitance, Fig. 3.11 demonstrates the good agreements of $S_{dd21}$ and $S_{cc21}$ between the equivalent circuit model and the simulated results. By means of 4 cell sections of the equivalent circuit as shown in Fig. 3.2, it can accurately model the electrical behavior of the filter to 2 GHz.

Figure 3.12 compares the simulated results of filters designed with original thick substrates and new offset design with thin substrates. Clearly, very comparable electrical characteristics on common- and differential-mode signals are observed for the two different designs. Table 3.1 summarizes the extracted parameters of the equivalent circuit model with and without offset design. As depicted in the table while $C_p$'s remain nearly unchanged when offset design is applied, the use of the thinner substrate results in larger self-inductance $L_S$'s and magnetic coupling coefficient $K$. Also, as a result of the overlapping between input/output pads and internal traces, as can be seen in Fig. 3.4, the parasitic capacitance $C_{p1}$ is larger than $C_{p2}$ and $C_{p3}$. As for $C_{p4}$, the shorter overlapped traces and larger distance to input/output pads make it smaller than other $C_p$'s. In view of common-mode signal path shown in Fig. 3.2, the frequency of the first null of $S_{cc21}$ appeared in the simulated and measured results can be approximated by the following equation, in which results calculated from parameters shown in Table 3.1 are also given,

$$f_{cm} = \frac{1}{2\pi\sqrt{(\sum L_{Sn})\times(1+K)\times C_S}} = \begin{cases} 745.6 \ \ MHz \ \ (without \ \ offset) \\ 741.1 \ \ MHz \ \ (with \ \ offset) \end{cases} \qquad (3.4)$$

Overall, the agreements found among the theoretically predicted and experimentally measured frequency responses confirm the offset design concept proposed here and the validity of the equivalent circuit model.

Figure 3.13 compares the $S_{dd21}$ measured for a commercially available toroid (TDK ACM2012-900) and LTCC designs with offset. Clearly, the multi-layer design proposed here with ceramic material achieve much better high frequency performance, which is a combined result of a high degree of magnetic coupling, small parasitic capacitances, excellent differential-mode impedance matching, and very low conduction and dielectric loss.

| Parameters | With offset | Without offset |
|---|---|---|
| $K$ | 0.94 | 0.92 |
| $L_{S1}$ (nH) | 20.29 | 17 |
| $R_{S1}$ (Ω) | 0.024 | 0.024 |
| $C_{P1}$ (pF) | 0.58 | 0.59 |
| $L_{S2}$ (nH) | 21.71 | 18.42 |
| $R_{S2}$ (Ω) | 0.026 | 0.026 |
| $C_{P2}$ (pF) | 0.46 | 0.45 |
| $L_{S3}$ (nH) | 21.71 | 18.42 |
| $R_{S3}$ (Ω) | 0.026 | 0.026 |
| $C_{P3}$ (pF) | 0.46 | 0.45 |
| $L_{S4}$ (nH) | 20.29 | 17 |
| $R_{S4}$ (Ω) | 0.024 | 0.024 |
| $C_{P4}$ (pF) | 0.4 | 0.38 |
| $R_P$ (Ω) | 6580 | 3790 |
| $C_S$ (pF) | 0.283 | 0.335 |
| $R$ (Ω) | 3300 | 3300 |
| $L$ (nH) | 820 | 815 |
| $C$ (pF) | 0.01 | 0.01 |

Table 3.1 Summary of the extracted parameters for the common- mode filter with and without offset design

### *3.3.2 Eye Diagram and Radiated Emission Measurements*

To verify the influence on differential signal of the designed common-mode filter, the eye diagram defined in USB 2.0 specifications is measured in system application. Figure 3.14 shows the eye diagram measurement setup and the test plane to examine the influence of common mode filter. Using Tektronix TDS7404 oscilloscope and the TDSUSB2 Universal Serial Bus measurement package, Fig. 3.15(a) and (b) show the measured eye diagram without and with the common-mode filter designed above using offset traces. Due to the small differential-mode insertion loss $S_{dd21}$, there is no significant effect on signal quality when the common-mode filter is

added.

By using an ESCO 94111-1 current probe and a 25 dB amplifier, the spectrum of common-mode current, which is resulted from imbalanced differential signal in the absence of the common-mode filter, is measured and depicted in Fig. 3.16(a). With the balancing effect provided by the common-mode filter, the improved spectrum is shown in Fig. 3.16(b). When comparing these two figures, the fundamental frequency component (i.e., 240 MHz) is effectively suppressed by 5.7 dB and similar noise suppression performance can also be found around the higher harmonics.

As a final check, the radiated emission test conducted in a semi-anechoic chamber for verifying compliance with the CISPR 22 requirements are illustrated in Fig. 3.17(a) and (b). When comparing these two figures, obtained with and without the designed common-mode filter, the fundamental frequency component (i.e., 240 MHz) is suppressed by 7.6 dB and similar performance can also be observed at higher harmonics especially around 900 MHz.

## 3.4 Conclusion

Common-mode noise, which is often the predominant contributor to the overall noise radiated from circuit boards and electronic instrument, must be eliminated or reduced to an acceptable level to comply with the EMC regulations. Components used to solve such problem are not only asked for providing good noise attenuation and negligibly small signal loss but also further dimension shrinkage. In this chapter, a miniaturized common-mode filter with offset traces has been proposed. The procedures for the extraction of equivalent circuit parameters, which are needed for fine-tuning the structural parameters to optimize the electrical performance and to minimize the size of the filter, are described. It's shown that while essentially the same electrical characteristics are retained, a 33% reduction of thickness is achieved

with offset design.

In designing a common-mode filter, 3-D LTCC is advantageous in offering a larger set of structural parameters and more accurate process than wire wound structure. The designed multi-layer common-mode filter made of LTCC with high *Q*-factor ceramic material and silver conductor produces lower insertion loss on differential-mode signal than conventional ferrite-based common-mode filter. This distinguishing feature makes this filter especially suitable for high-speed data communication applications.

As the volume of information transfer grows, data transmission speed in electronic sets will continue to increase. In anticipation of this trend, the noise suppression components need pursue even higher operation frequency by using high frequency material. In high frequency band, the ceramic material has lower loss than conventional ferrite material so the common-mode filter made of ceramic substrate has better performance than wire-wound choke using ferrite material for future application.

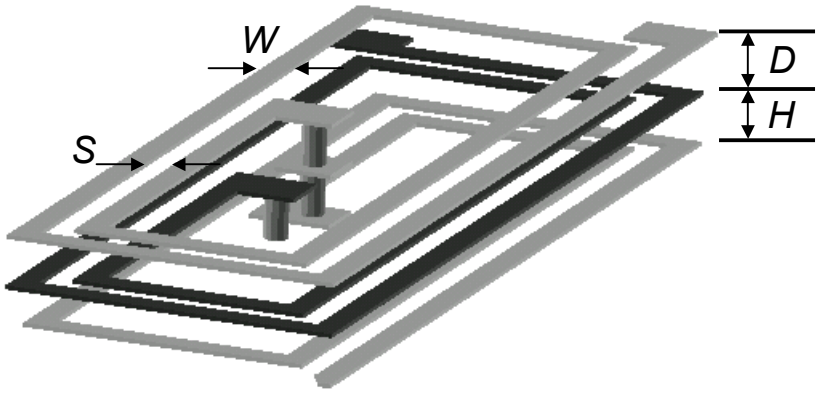



Fig. 3.1 3-D perspective view of multi-layer structure. The gray lines represent positive coil and the black lines represent negative coil.

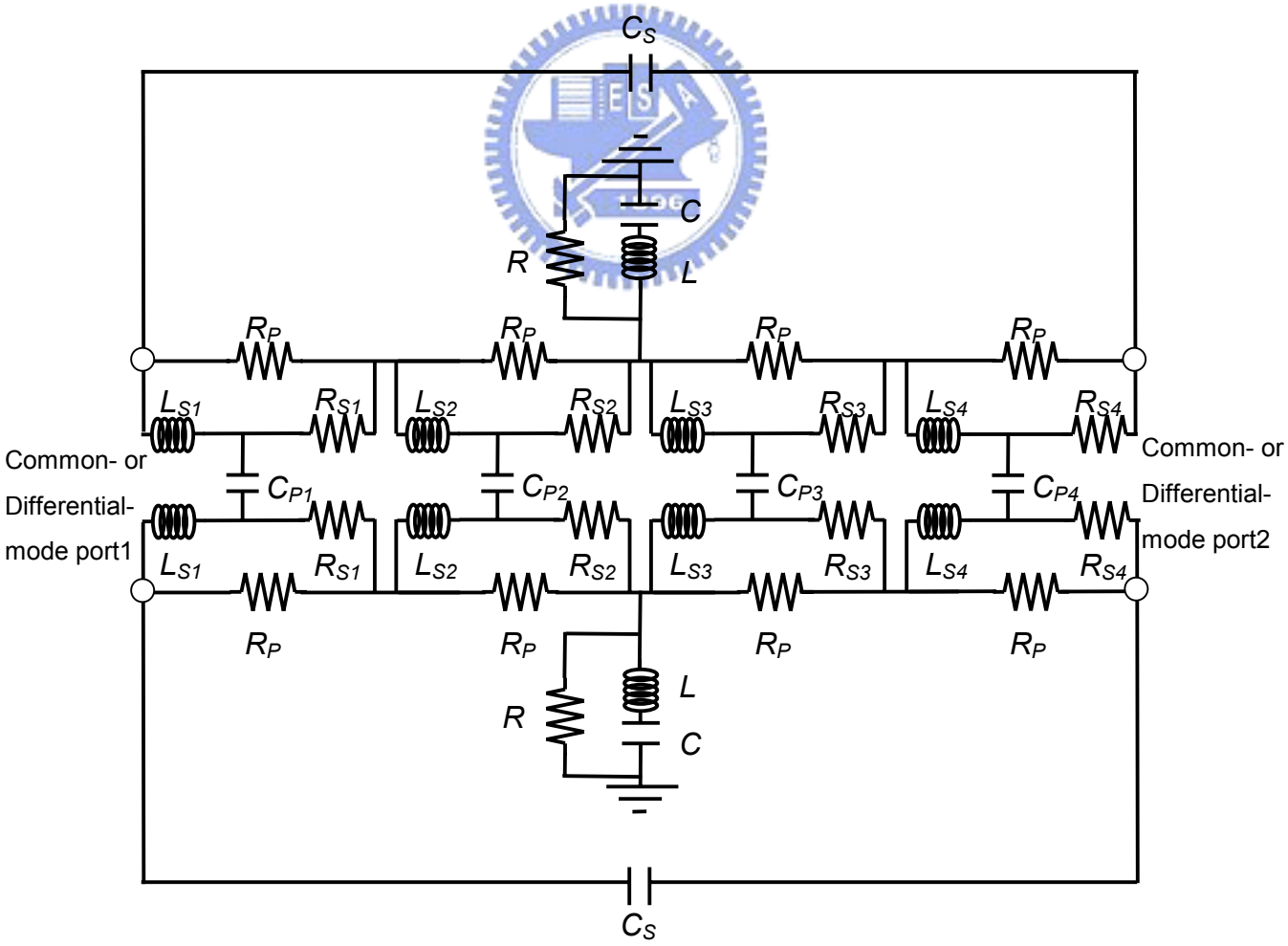



Fig. 3.2 Equivalent lumped-circuit model.

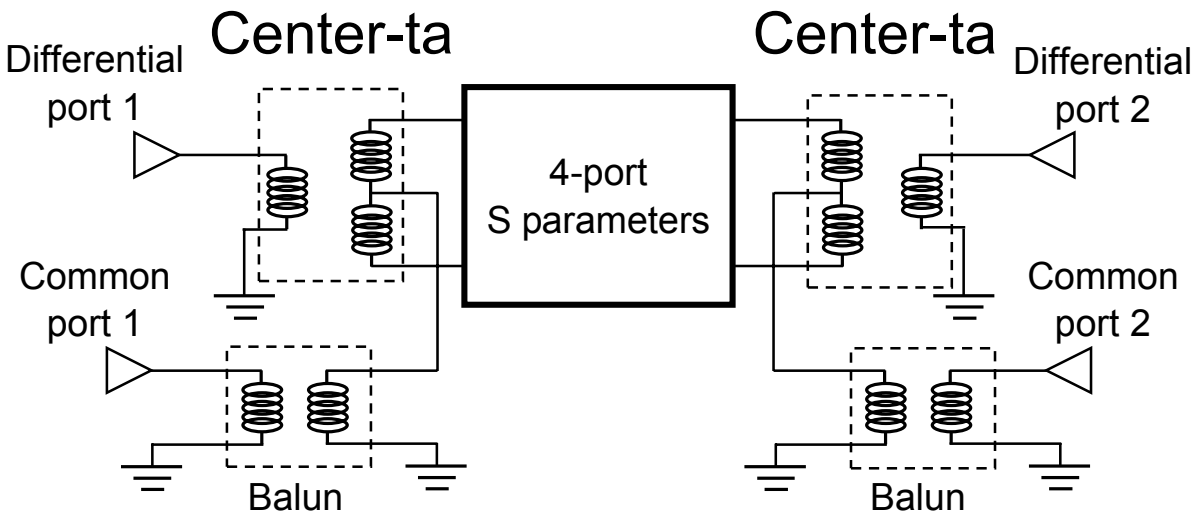



Fig. 3.3 Circuit used to obtain mixed-mode *S* parameters of differential device.

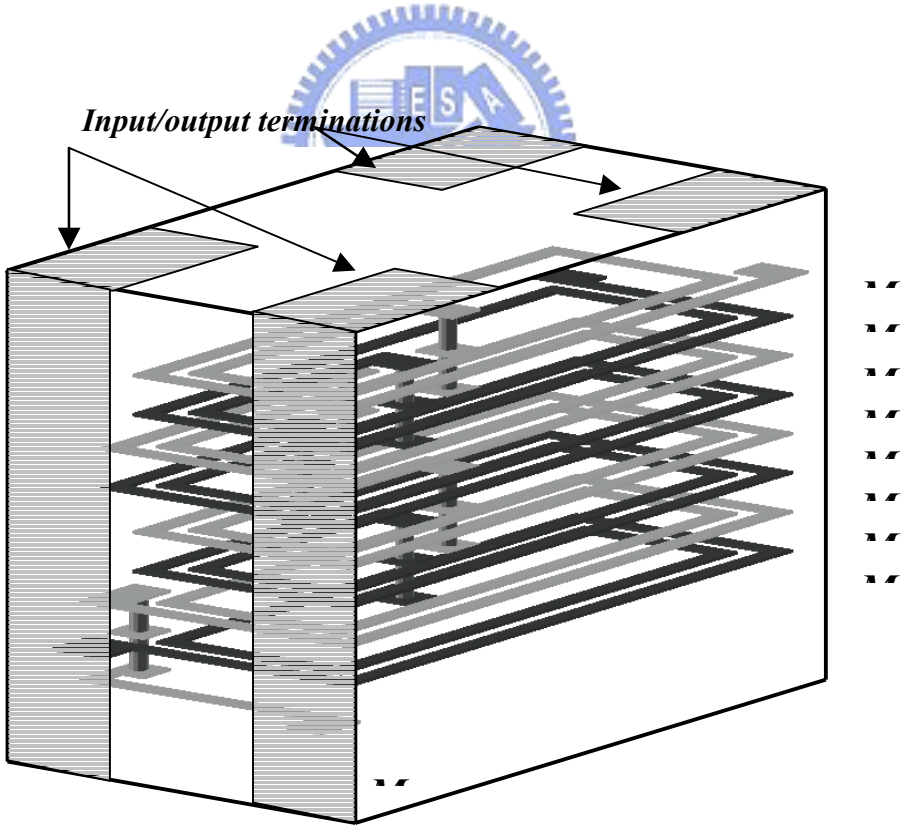



Fig. 3.4 Structure of the designed filter having 4 sets of differential pairs and one added layer for trace length compensation.

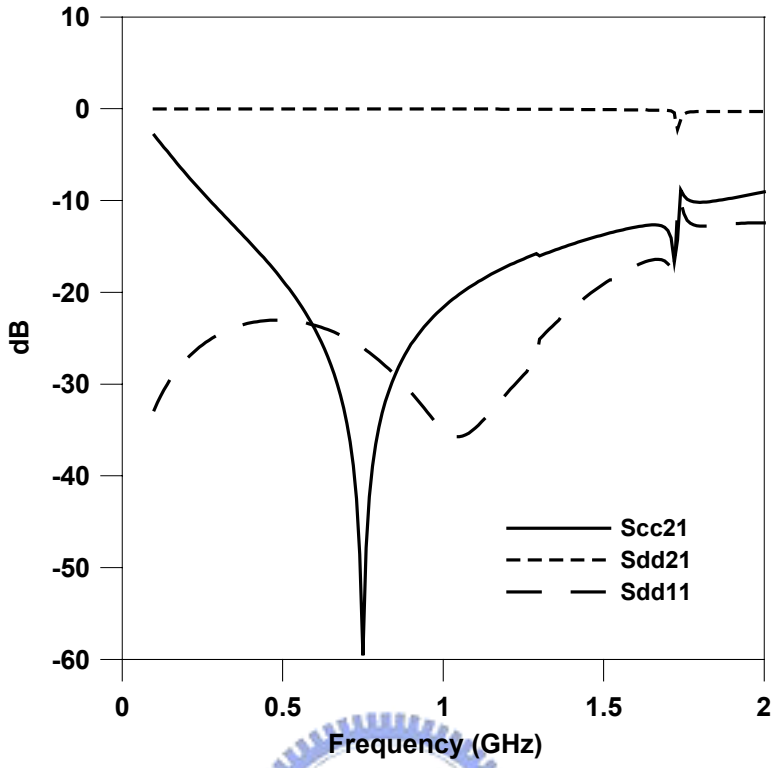



Fig. 3.5 Simulated result of the designed multi-layer common-mode filter.

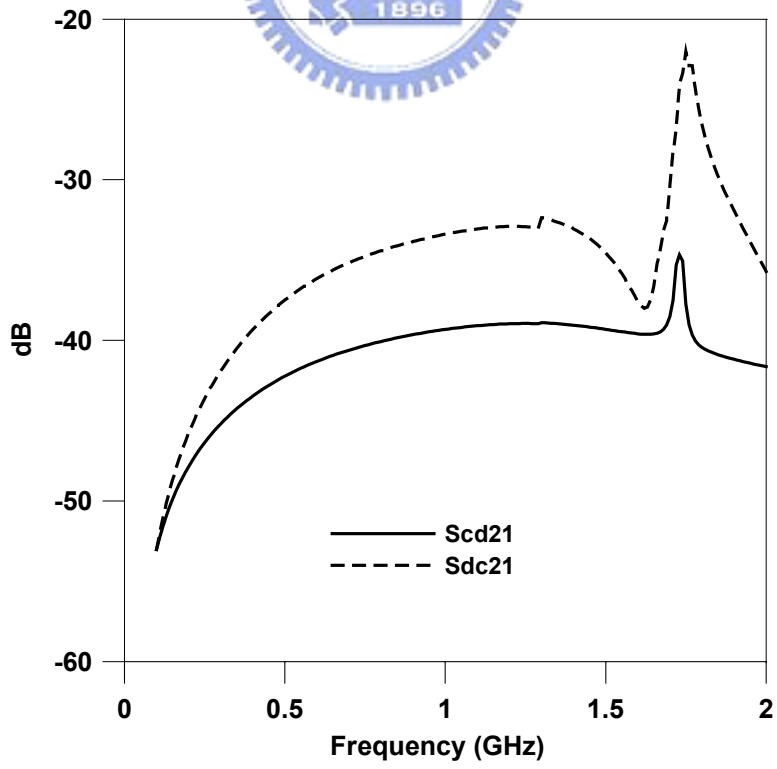



Fig. 3.6 Mode conversion of multi-layer design.

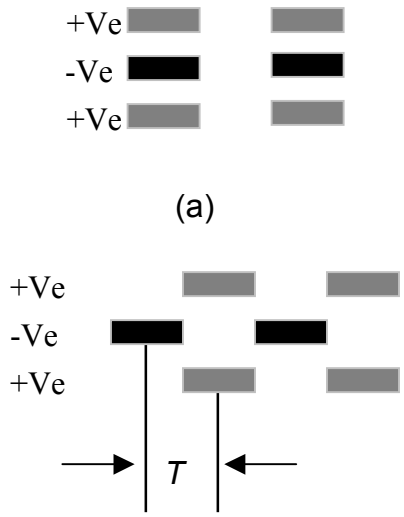



Fig. 3.7 Differential pair with (a) completely overlapped and (b) horizontally offset traces.

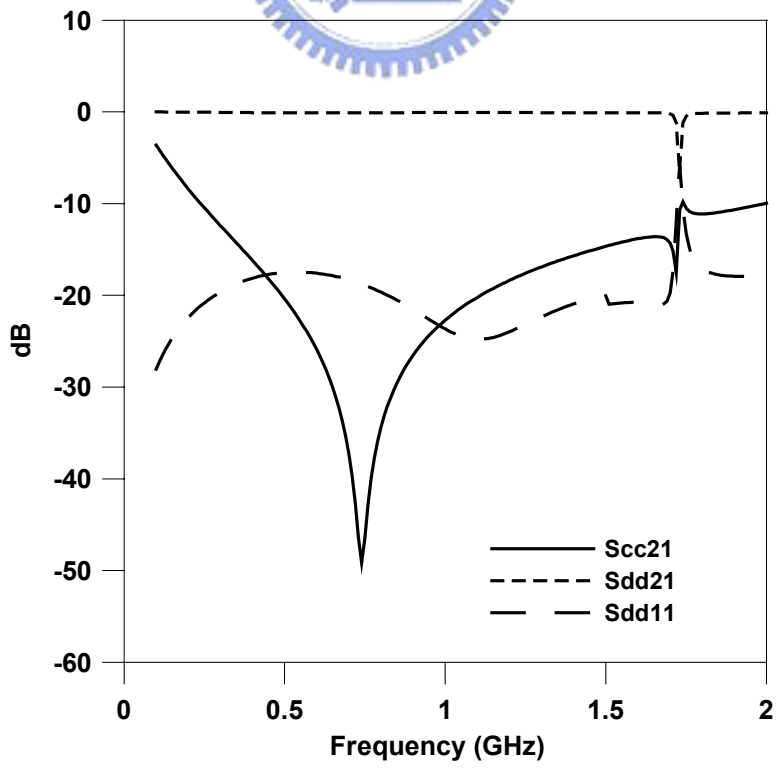



Fig. 3.8 Simulated mixed-mode *S* parameters result with offset design.

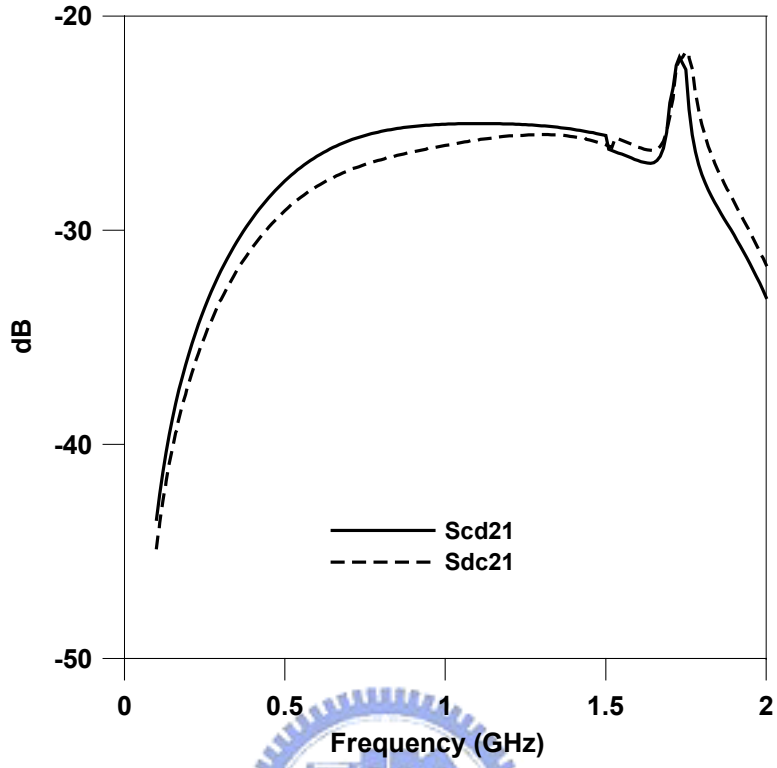



Fig. 3.9 Mode conversion performance of offset multi-layer design.

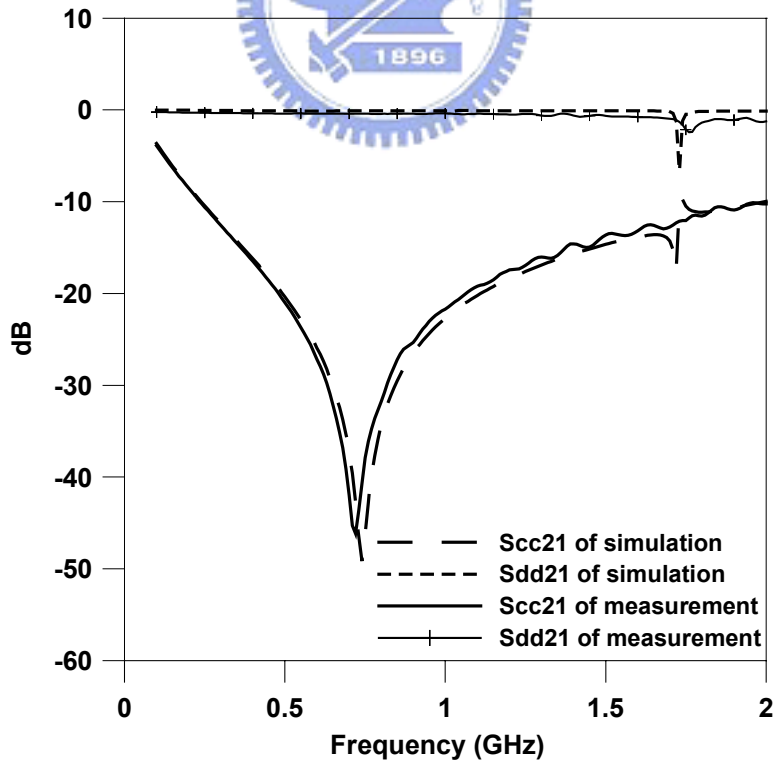



Fig. 3.10 Mixed-mode *S* parameters comparisons between simulated and measured results with offset design.

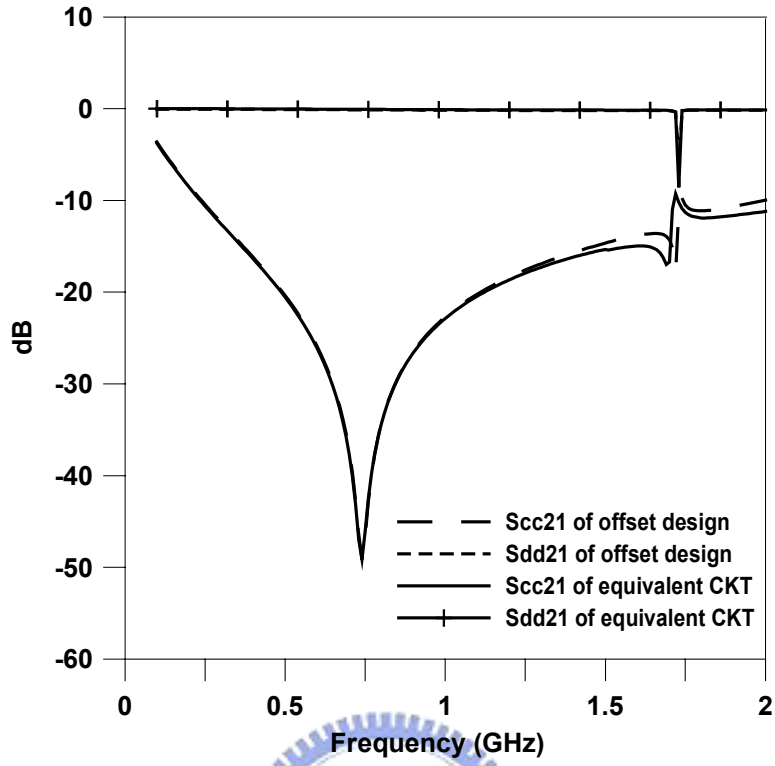



Fig. 3.11 Comparison between simulated and equivalent circuit model results with offset design.

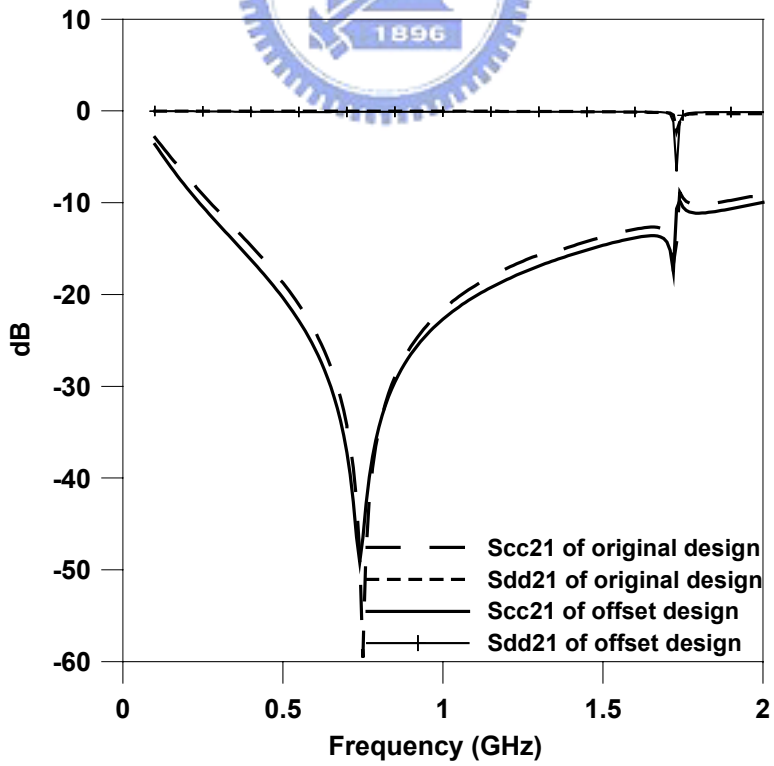



Fig. 3.12 Simulated results of original thick substrates and offset thin substrates design.

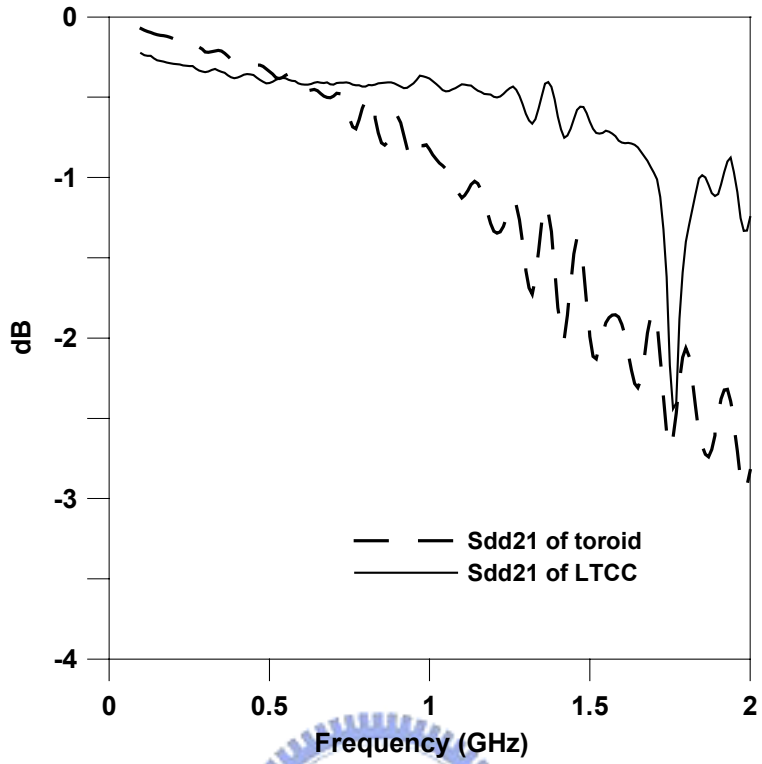



Fig. 3.13 Comparison of $S_{dd21}$ between a commercially-available toroid and the proposed LTCC design.

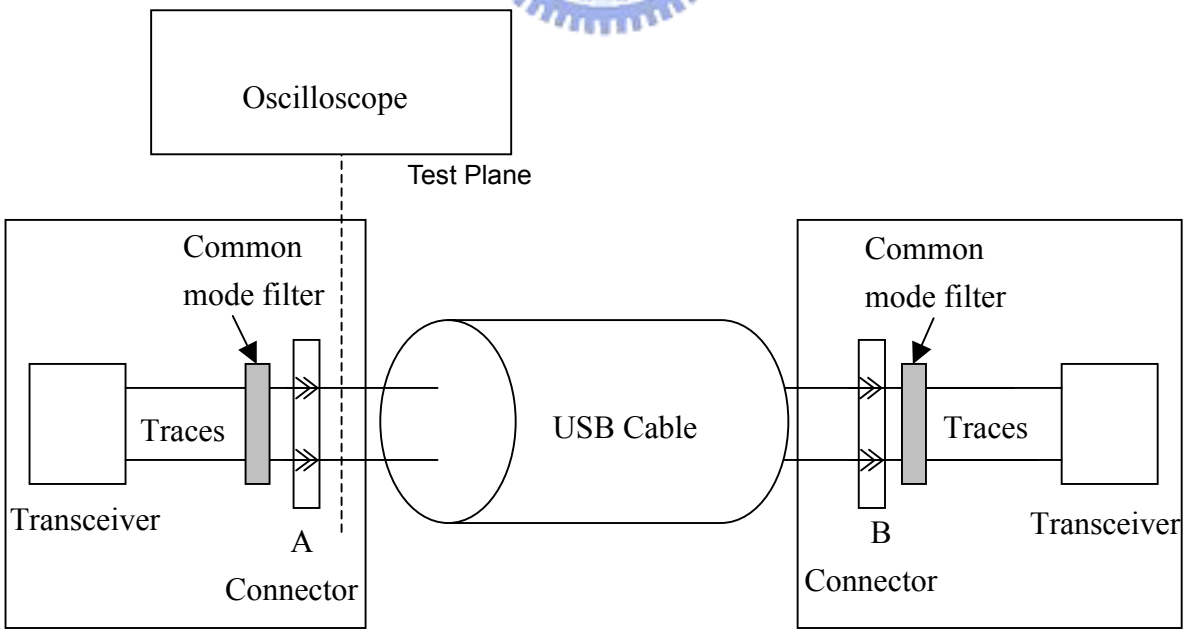
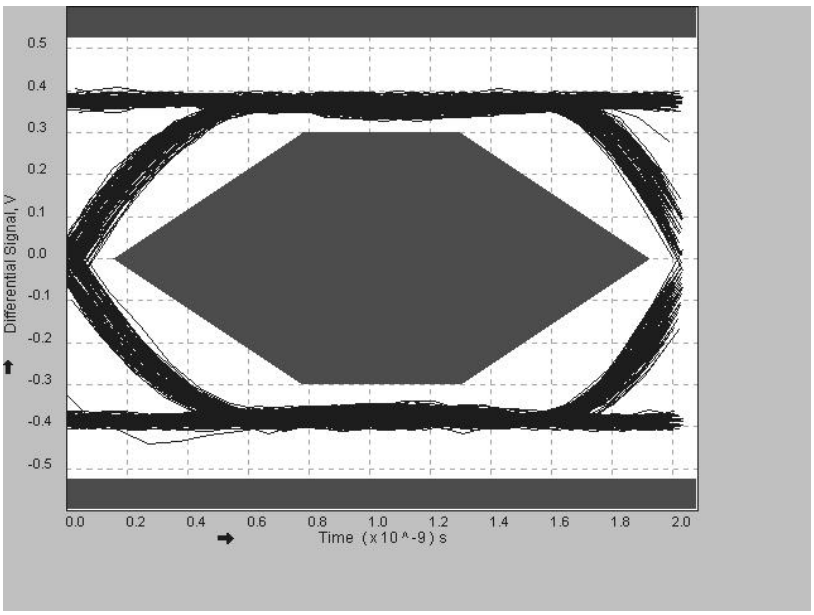
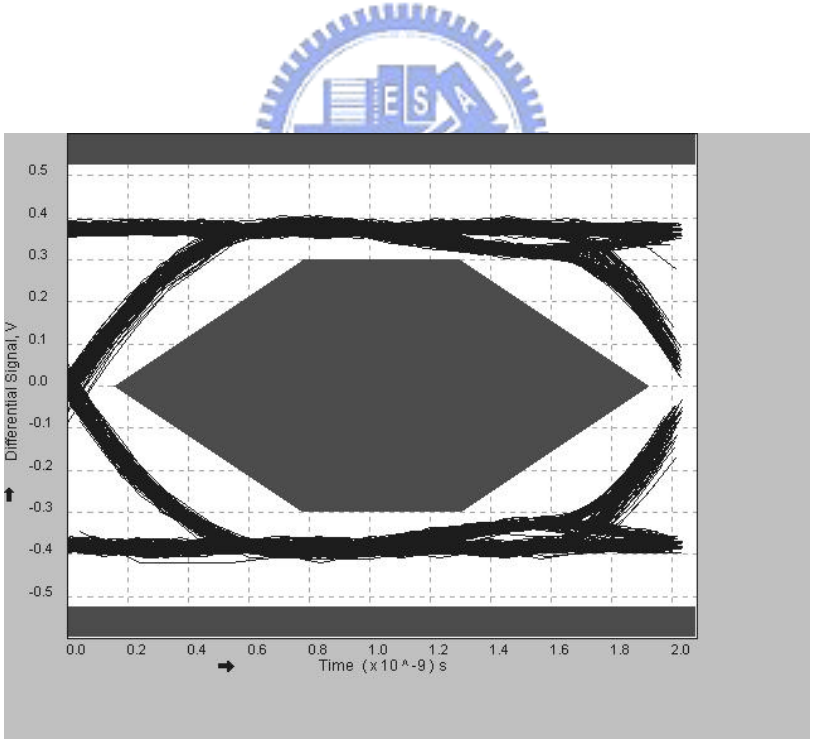



Fig. 3.14 Configuration of eye diagram measurement.

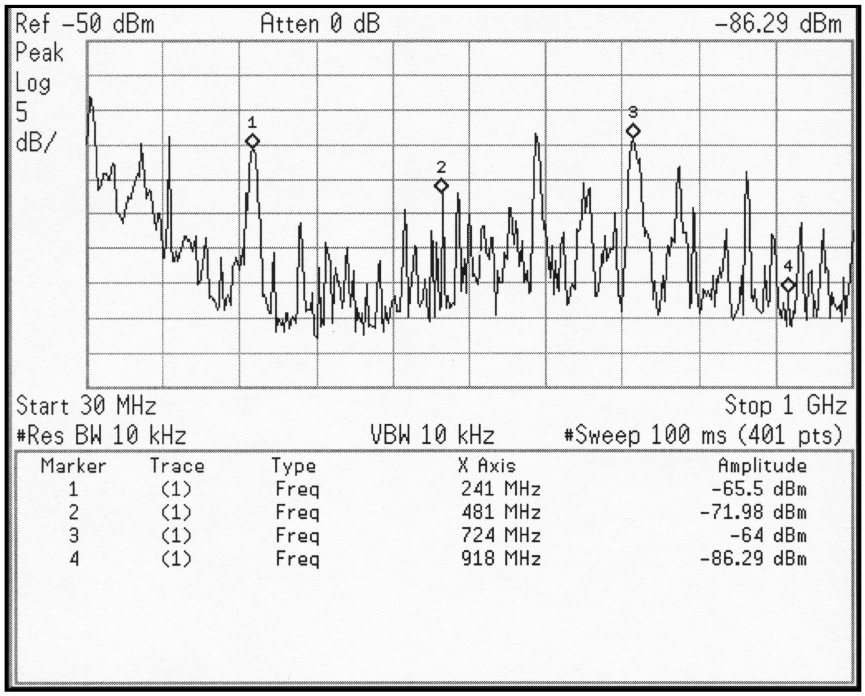



(a)

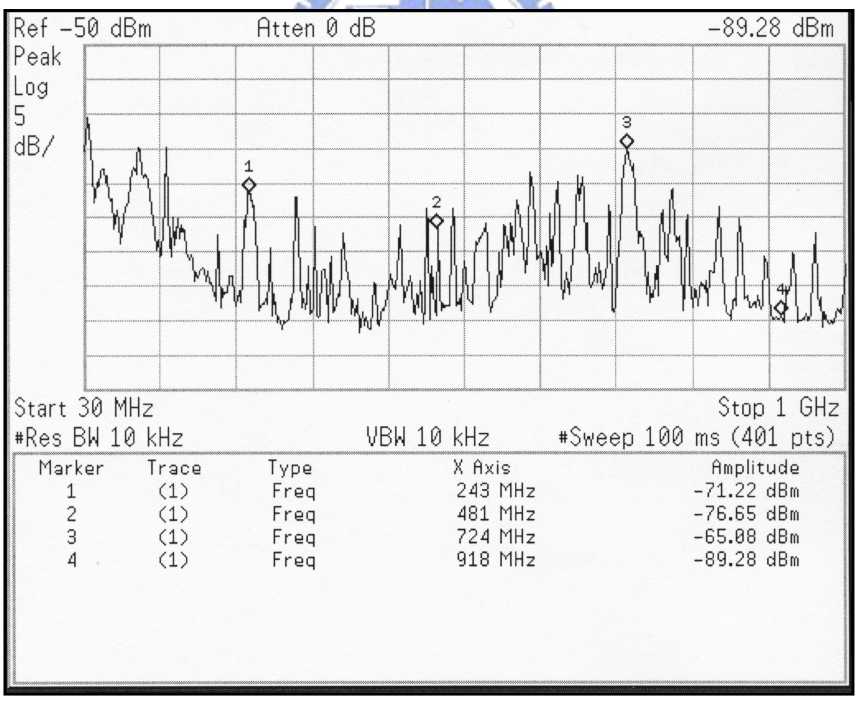



(b)

Fig. 3.15 Eye diagram measurement results: (a) no filter added, and (b) filter added.

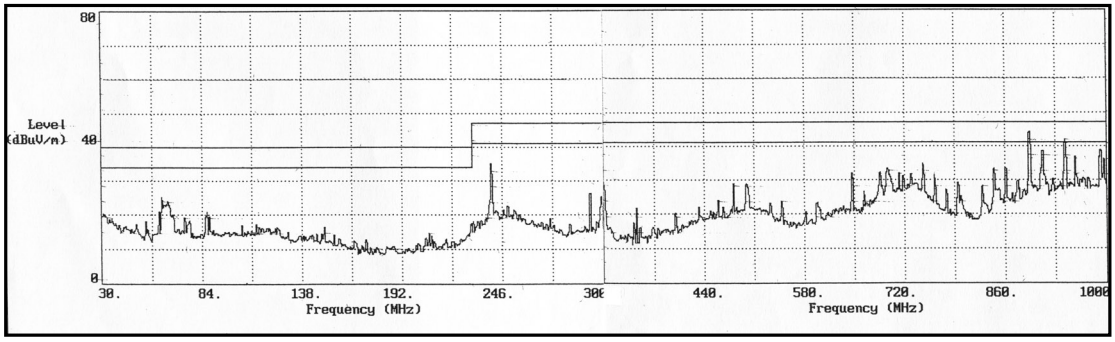



(a)

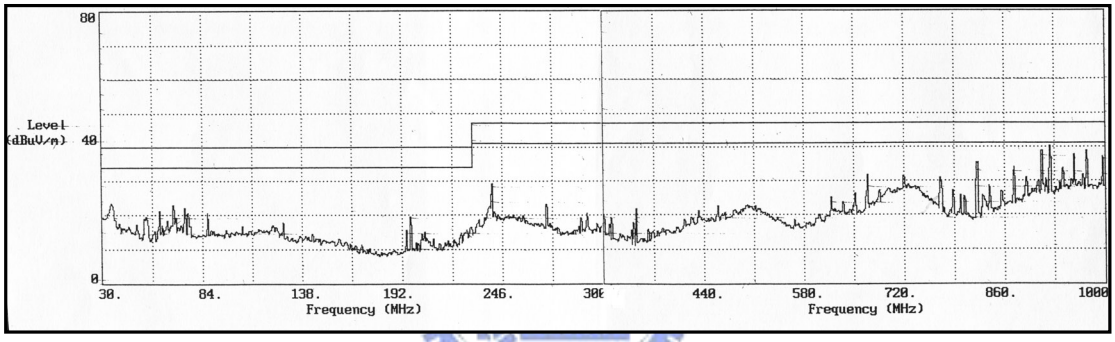



(b)

Fig. 3.16 Spectrum of common-mode current measured: (a) no filter added, and (b) filter added.




(a)




(b)

Fig. 3.17 Spectrum of radiated emission measured in a semi-anechoic chamber: (a) no filter added, and (b) filter added.

# CHAPTER 4

# DESIGN OF MULTI-LAYER DELAY LINE

## 4.1 Introduction

With increasing demands on data storage and system functionality, higher bus speed in electronic system is requested. In proportion to the high clock frequencies, timing and alignment of clock and data signals across a system become much tighter. Not only do signals need to be more closely aligned in high-speed system, but control of duty cycles, pulse-widths, and spurious noise also become serious issues. To avoid false operation of digital logic circuits, it is necessary to constrain clock skew and coupling noise below adequate levels.

To maintain the synchronization in various electronic systems (e.g., TV receiver, super computer, optical link interface, and so on), delay line is encountered. Lumped type delay line can get long delay time easier than distributed one, but it is not applicable in high frequency circuit. As frequency increased, the parasitic effects of lumped type delay line will become apparent then the transmitted signal will be seriously distorted. Another delay line type commonly used in package and board level applications are the microstrip or stripline type meander delay line that consists of a number of transmission line sections closely packed to each other. Intuitively the total time delay will increase proportionally to the total length of the meander line. However, the electromagnetic coupling among the adjacent lines in the meander structure at various time frames is accumulated and appeared as a laddering wave in the receiving waveform [39]. Once the coupling coefficient between adjacent lines grows up to a significant level, the propagation delay of the meander line will turn out to be much shorter than that predicted from conduction

path length and the accumulated crosstalk can also be large enough to distort the waveform to a degree that may cause a false trigger of the logic [40], [41].

Although, microstrip/stripline type delay line has more stable characteristic impedance in high frequency applications, but the crosstalk among meander lines needs to be minimized. However, since the crosstalk is a function of the separation between the adjacent line segments, the only way to minimize the crosstalk would be to increase the line spacing. This unfortunately requires larger circuit board area that can be either expensive or impossible in view of the large number of meander delay lines used in today's high-performance digital system. Several published papers have investigated and analyzed the meander delay line characteristics [42], [43].

There has been a strong incentive to miniaturize the delay line of a distributed-parameter type [44]. This chapter describes a miniaturized multi-layer delay line, which is characterized by the distributed parameters, using LTCC technology for high-speed applications. To improve the waveform distortion that may arise in closely spaced meander delay line, the designed structure utilizes grounded guard traces and square spiral routing structure to suppress coupling among signal traces while maintaining stable characteristic impedance to minimize reflection that may occur at high frequency. This chapter consists of following aspects: in Section 4.2, the design of multi-layer delay line is presented first. Section 4.3 discusses the propagation characteristics of the designed delay line through TDR/TDT and finite difference time domain (FDTD) simulations. Finally, Section 4.4 gives a summary and some concluding remarks.

## 4.2 Multi-Layer Delay Line Design

### *4.2.1 Structure of Multi-Layer Delay Line*

Exploring the significant recent advances in the LTCC process techniques for

high frequency application, a multi-layer delay line using ceramic substrate with relative permeability 1, relative permittivity 4.8, and dielectric loss tangent 0.0016, is designed. Figure 4.1 shows the structure of the proposed multi-layer delay line. As demonstrated by the cross-section view of a portion of the structure shown in Fig. 4.2, with the interlaced arrangement of signal lines and grounded guard traces, the structure is similar to a stripline with finite ground, so the characteristic impedance of the distributed delay line can be kept stable to high frequency band. Also, by the square spiral traces with grounded guard traces, the electromagnetic coupling occurred between closely packed serpentine type delay lines are effectively decreased.

To have long delay time, a 3-D multi-layer structure with square spiral on each layer is formed. Each substrate is printed with conductive silver coil pattern and via holes. After all the substrates are stacked, delay line is then connected in a sequence through a plurality of via holes and the grounded guard traces are connected through the side terminations of the component.

### *4.2.2 Characteristic Impedance of Multi-Layer Delay Line*

Characteristic impedance is an important propagation parameter of any electrically long transmission line element. To achieve negligible effect on the transition edges (i.e., the high-frequency components) of a digital signal, an optimized characteristic impedance matching is needed. With good characteristic impedance matching, the insertion loss incurred on the digital signal, evaluated by $S_{21}$ of the $S$ parameters, will be minimal over its intended operating bandwidth such that signal passes through the component undisturbed.

Since multi-layer structure includes numerous bends and vias, a full-wave, 3-D FEM-based simulator HFSS (Ansoft, Pittsburgh, PA) was utilized to consider the

effects of the discontinuities and electromagnetic coupling when designing the delay line. The signal and ground line width $W$, horizontal spacing $S$, and vertical spacing $D$ between signal and ground trace, as shown in Fig. 4.1, were adjusted to achieve an optimized matching. 50-ohm characteristic impedance, which is usually used in high frequency circuit, is attained by $W$ = 75 μm, $S$ = 112.5 μm, and $D$ = 75 μm. The delay line is designed to fit in an EIA 1206 form factor (i.e., surface dimension 3.2 mm× 1.6 mm). The total occupied component thickness with 12 μm conductor thickness and the 8 foil substrates is 0.6 mm. Figure 4.3 depicts the designed delay line composed of 7 layers and input/output and ground terminations; one of the input/output terminations is shown by dash lines for a better illustration of the designed delay line.

To prevent signal distortion, the 3-dB bandwidth of the delay line must be kept larger than the maximum frequency $f_{max}$ of the propagating signal. The simulated $S$-parameter results of the designed multi-layer delay line are shown in Fig. 4.4. With both conductor and dielectric losses also considered in the simulation, this delay line provides very low insertion loss of $S_{21}$ > -3 dB up to 6.8 GHz, and good matching with $S_{11}$ < -10 dB up to 6.7 GHz. Given these, the $f_{max}$ of the propagating signal is comfortably chosen to be 6 GHz, which corresponds to a minimum rise time $t_{r,min}$ = 0.35/ $f_{max}$ ≅ 58.3 ps, for simulation purpose.

## 4.3 Results and Discussion

For high-speed circuit board designers, one of the important properties of the delay line is propagation delay. The corsstalk among the closely packed traces of the meander type delay line may accumulate significant enough to cause a drastic reduction of the total time delay or to cause a significant waveform distortion to result in an unpredictable delay time. Since delay line is often required to restrict timing

skew to several tens of picosecond in modern high-speed system, a precise time delay estimation of the delay line is essential. To investigate the propagation delay and the received waveform in more details, the transient TDT simulation of ADS (Agilent, Palo Alto, CA) is utilized. With the purpose of performing the time domain analysis, the *S*-parameter of the simulated delay line is transformed into time domain by applying inverse fast Fourier transform (IFFT). Results obtained by TDT simulation including effects due to reflection and material losses and any residual coupling among traces. To carry 6 GHz propagating signal, the rise time of the source is set as $t_r$ = 58.3 ps. With 1V amplitude, 2 ns period and 50 percent duty cycle, the trapezoidal waveforms at the sending and receiving ends are shown in Fig. 4.5. For the multi-layer structure demonstrated in Figs. 4.1 and 4.2, the signal traces and grounded guard traces are broadside coupled. So, the coupling between the adjacent signal traces is effectively reduced. Together with good impedance matching and low insertion loss, a clean, delayed, copy of the input waveform appears at the output port. From the crossing of the input and output simulated waveforms through 0.5V, the delay time is found to be 227 ps.

To further verify the delay time of designed delay line, the FDTD simulator XFDTD (Remcom, State College, PA) is applied. The problem space, as shown in Fig. 4.6, is surrounded by the ground plane modeled with a perfect electric conductor (PEC) boundary and Liao's absorbing boundary condition (ABC) [45] at the rest of the boundaries. The meshing dimensions of the problem space are 101 × 201 × 51 in *x*, *y*, and *z* directions with a 1.5 mil × 1.5 mil × 1.5 mil cell size. In this FDTD simulation, conductor loss is neglected and the metal thickness is assumed to be zero. With the same trapezoidal waveforms used in TDT simulation, Fig. 4.7 shows the waveforms at the sending and receiving ends. From the crossing of the input and output simulated waveforms through 0.5V, the delay time is found to be 251 ps.

After deembedding the propagation through the 111-mil microstrip feed lines, which corresponding to 18 ps, the delay time of designed delay line including the input/output terminations would be 233 ps. Figure 4.8 demonstrates the *S* parameters converted from the FDTD simulation. Comparing Figs. 4.4 and 4.8, good agreement exists between these two simulation methods.

The mutual coupling between the adjacent lines was shown to have the most detrimental effect on the propagation delay associated with the conventional meander lines [40]. In order to demonstrate the improved coupling performance achieved by the designed delay line, the propagation delay difference between a straight line and the designed multi-layer structure is calculated. Using two straight transmission lines of different lengths, the velocity of the straight transmission line in the ceramic material can be simulated and extracted. With the calculated velocity of 1.38E8 m/s, which corresponds to an effective dielectric constant of 4.73, the total delay time for the signal to propagate through the 1161-mil conductive path length of the designed delay line including the input/output terminations would be 218 ps. The delay time difference between TDT/FDTD simulations and calculated one can be attributed to the extra time delay introduced by the via transitions present in the multi-layer structure; coupling between adjacent signal traces is therefore considered insignificant.

To evaluate the potential surface saving efficiency of the proposed multi-layer structure, a symmetric stripline type of meander delay line constructed in a multi-layer PCB is illustrated in Figs. 4.8(a) and (b). With ground plane spacing $H$= 228 μm, dielectric constant $\varepsilon_r$ = 4.3 and half-ounce copper of thickness $t$= 0.69 mil, the 50 ohms characteristic impedance can be obtained with 3-mil line width. To have negligible coupling between the adjacent line segments, the line spacing $P$ is chosen to be wider than 4 times of the line width (i.e., 12-mil) [40]. With meander

structure having the identical EIA 1206 component width of 60-mil, the same 233 ps delay time, which corresponds to an 1349-mil conduction path length, is obtained by the multi-layer structure with length $L$ = 281 mils. As compared to the component length of the designed multi-layer structure, a miniaturization factor 2.34 is attained. Moreover, if longer delay time is required, $L$ will have to be increased proportionally. In contrast, with multi-layer structure, it can be met simply by adding more layers and, therefore, achieving even larger board area saving efficiency.

## 4.4 Conclusions

Tighter timing budget related to the synchronization of the high-speed clock and data signals among the logic gates is required. Synchronization is usually a critical concern in high-speed digital electronic systems. Delay lines are often employed to manage timing skew problem. Significant coupling between closely spaced traces can cause a significant waveform distortion and delay time reduction in the widely used meander structure. In order to attain a high degree of signal integrity and utilize the meander delay line as if it were a straight line in a circuit board, the meander segments are separated at a distance great enough to render an insignificant degree of coupling. It will thus need a large and inefficient use of board space.

To save the limited board space, a miniaturized 3-D delay line was developed in this chapter, which utilized interlaced signal and grounded guard traces to attain simultaneously good impedance control and crosstalk reduction. Results obtained by the TDT and FDTD simulations demonstrate that the proposed structure has excellent transmission performance with minimal insertion loss and coupling effect up to at least 6 GHz and is therefore useful for pulses with a rise time as small as 58.3 ps. The propagation delay and characteristic impedance of the designed delay line have been carefully investigated based on time- and frequency- domain analyses. In

summary, the designed delay line shows two major features: (1) suitability for high frequency/speed applications because of its low material loss, controlled impedance and reduced crosstalk, and (2) small and compact outline as a consequence of multi-layer structure.

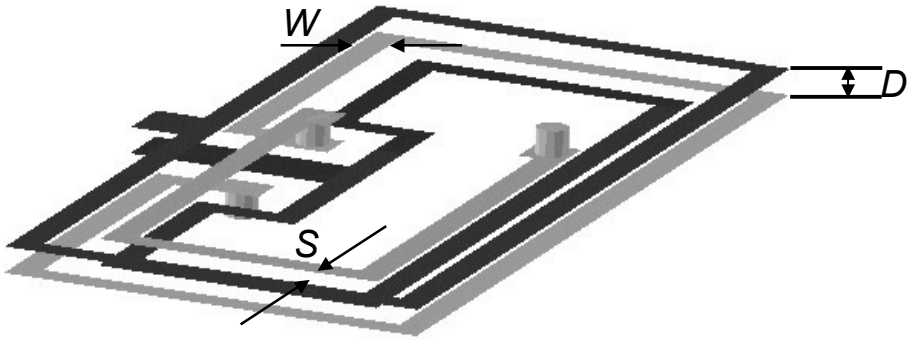



Fig. 4.1 3-D perspective view of multi-layer structure. The gray lines represent signal trace and the black lines represent ground trace.

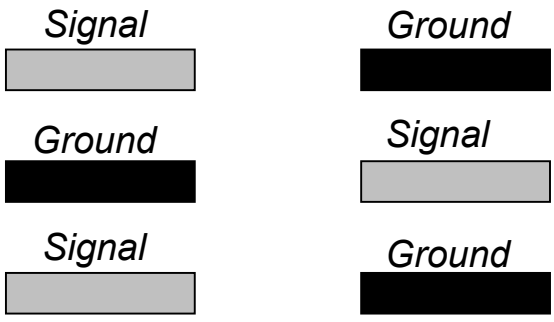



Fig. 4.2 Cross-section view of the interlaced arrangement.

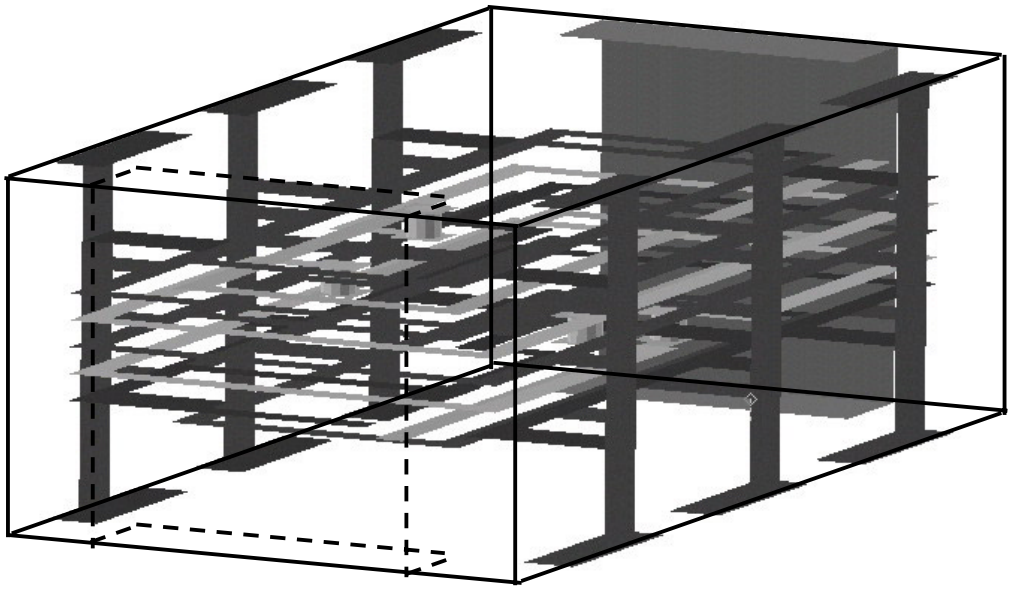


Fig. 4.3 Structure of the multi-layer delay line.

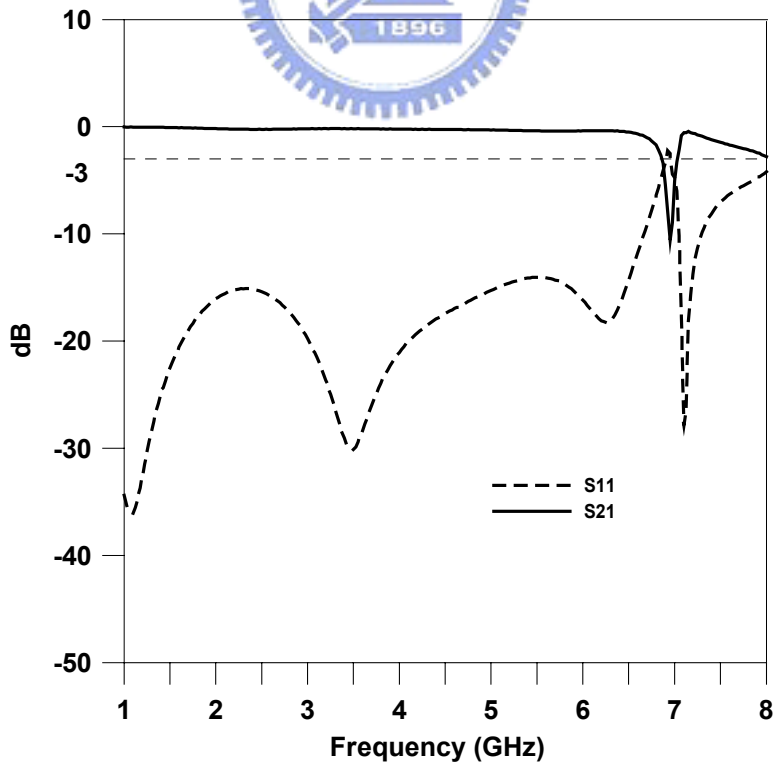



Fig. 4.4 Simulated *S* parameters by FEM simulation.

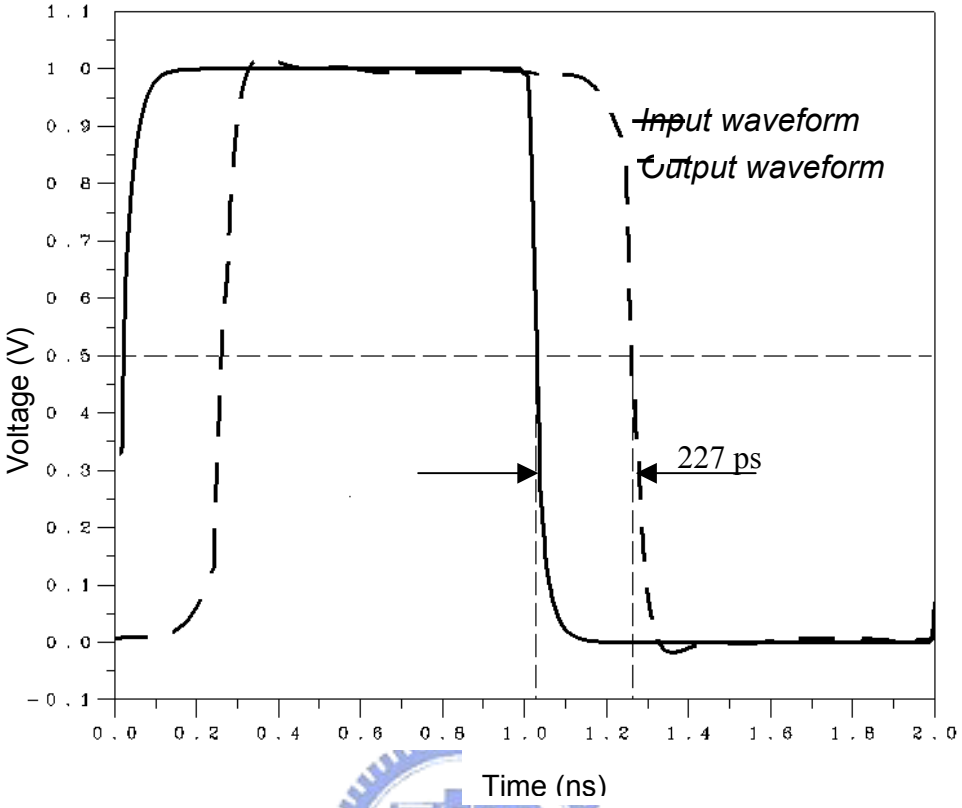



Fig. 4.5 Time domain input and output waveforms by TDT simulation.

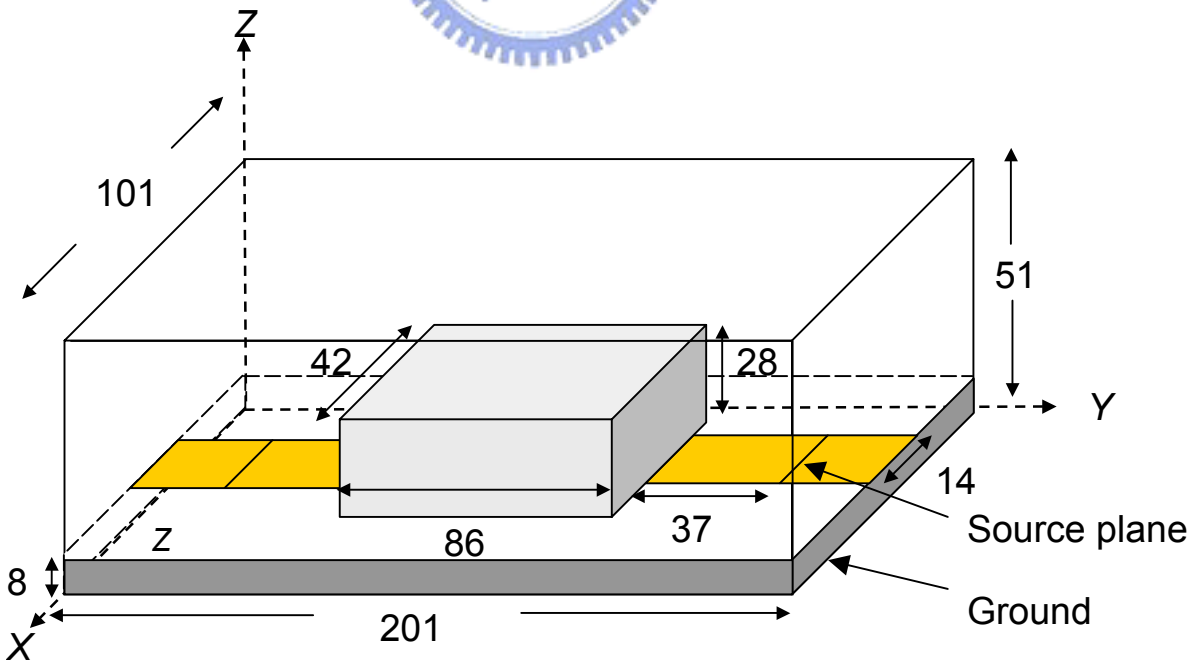



Fig. 4.6 FDTD problem space. Dimensions are given in FDTD cells.

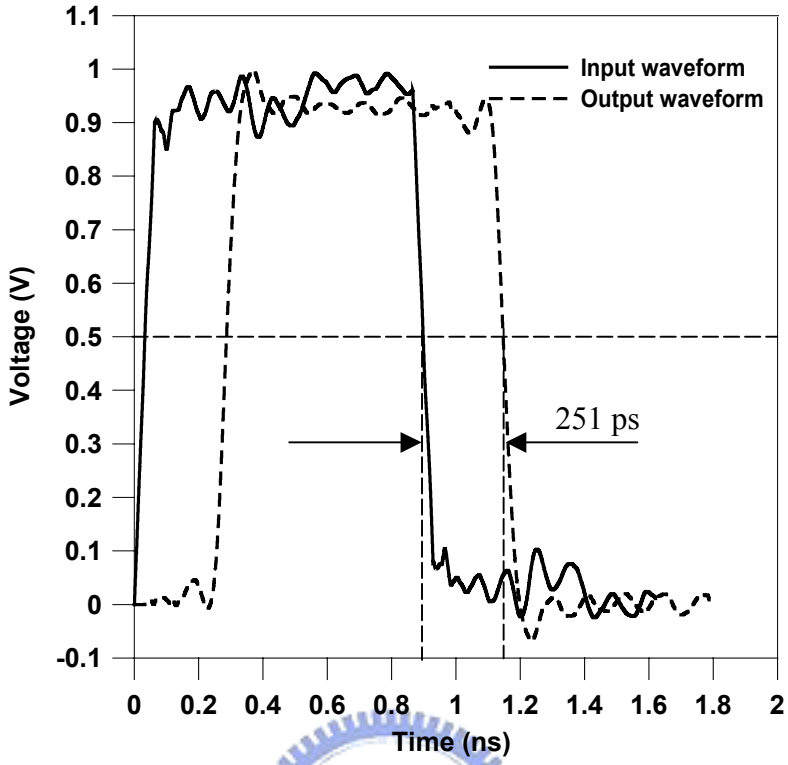



Fig. 4.7 Time domain input and output waveforms by FDTD simulation.

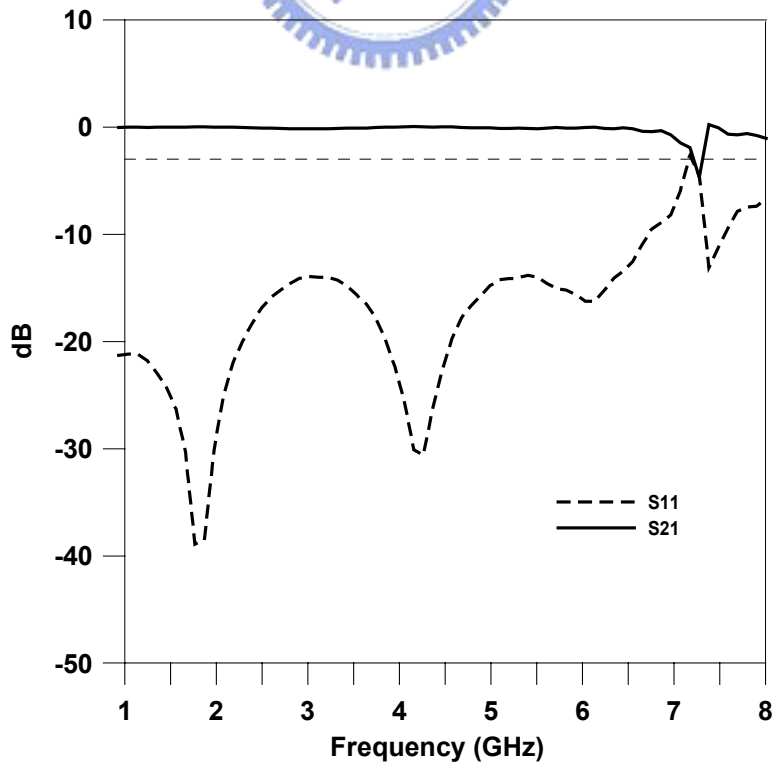
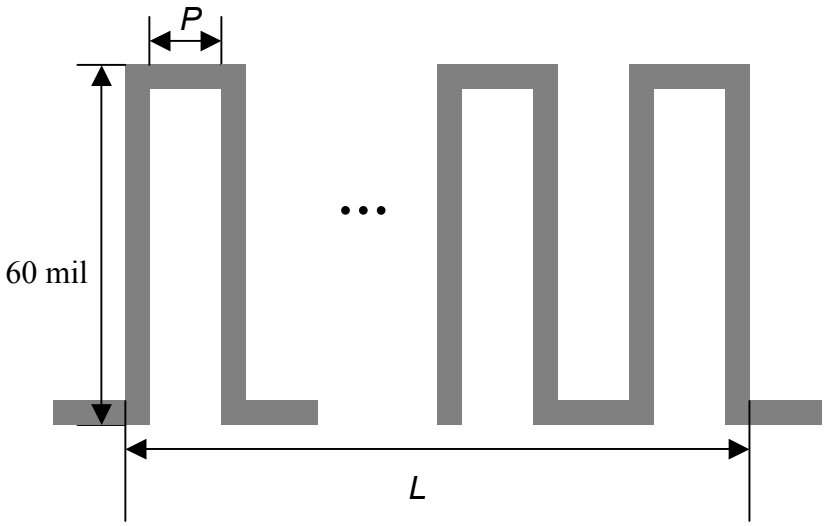
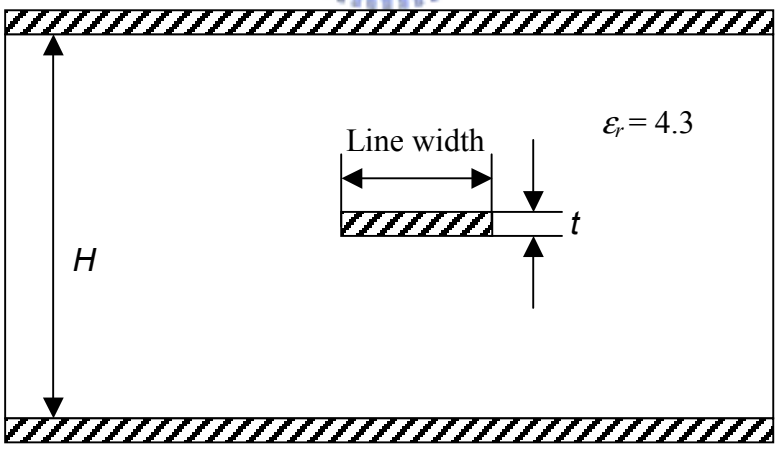



Fig. 4.8 Simulated *S* parameters by FDTD simulation.




(a)




(b)

Fig. 4.9 (a) Top view of the stripline-type meander delay line structure. (b). Cross-section view of the symmetric stripline used in the delay line of (a).

# CHAPTER 5

# CONCLUSIONS AND RECOMMENDATIONS

Generally speaking, the laminated PCB with discrete surface mounted passives and active devices offers the lowest cost infrastructure in system package. However, the potential performance advantage, continuous demand for further product miniaturization and cost saving in both chip- and system board- level are driving the wide acceptance of MLO and LTCC substrates containing embedded passive components. In applying these two SOP approaches, system partitioning has significant impact on performance, size and cost of the final module. The traditional approach of separate active silicon design, packaging design and system board design would have to change to a more coexisting engineering manner to fully realize the benefit of increasing degree of passive integration and miniaturization.

In this dissertation, approaches to characterize high-frequency characteristics of different multi-layer materials used in board-level integration are discussed first. With these material characteristics, various embedded multi-layered capacitors and inductors are designed and tested. As a result of the magnetic flux leakage in the loosely-wound non-magnetic-core structure, the designed embedded inductor cannot cover the high inductance range that may be needed in mainstream wireless communication applications. By way of HDI and partial filled high permeability material processes, the inductance of solenoidal inductor can be increased.

To have a complete analysis of frequency responses of the circuits built with these embedded devices, however, the parasitics in the equivalent lumped-circuit models of MIM capacitor and solenoidal inductor should be extracted and

demonstrated. In addition, to allow designer to easily switch from the use of discrete components to integrated passives, developments of accurate and reliable cell libraries for various embedded components are required. With continuous developments in high permittivity and permeability materials, the embedded capacitor and inductor can be further miniaturized.

Following this, the design of a miniaturized multi-layer common-mode filter for use with USB 2.0 products by LTCC technology are investigated. As compared to the ferrite-based wire-wound common-mode choke, the designed multi-layer common-mode filter produces lower insertion loss on differential-mode signal. Furthermore, by using 3-D multi-layered and offset, instead of completely overlapped, architecture for the differential transmission pair, a 33% thickness reduction is achieved in the design of a miniaturized common-mode filter.

For suppressing higher frequency common-mode noise induced on ever higher speed differential signaling system, the common-mode attenuation characteristics of the designed common-mode filter can easily be tuned to higher frequency bands by simply using shorter trace length, which will also results in a smaller component size. In contrast, to cover lower frequency applications and/or to further reduce the filter, increasing self- and mutual- inductance by a closed ferrite materials loop with partial filled process as shown in Fig. 5.1 is proposed. By this structure, the differential signal will not be degraded due to the use of low-loss ceramic material and high-conductivity conductor. The high permeability material loop will interact with the magnetic flux produced by the common-mode current and, therefore, results in higher common-mode inductance for a given trace length. On the other hand, sufficient common-mode inductance can be obtained with shorter traces and, therefore, smaller component size.

Finally, a miniaturized LTCC delay line is developed. In this design, grounded

guard trace is employed to obtain the desired characteristic impedance and eliminate the undesired coupling effect that may be present in meander delay line. For the 233 ps delay time obtained by our 3-D structure, an extra board space amounting to a factor of 2.34 is required by stripline type meander delay line on FR-4 board; by using higher permittivity material and fine line process, the same delay time can be realized in a more compact multi-layer form factor or larger delay time can be attained by the same form factor component.

While there is no doubt that LTCC approach offers many benefits over other packaging technologies, there are two characteristics that are perceived as limitation of this technology, namely, shrinkage control and thermal conductivity. Despite the simulation tools performance, usually, processes stability is the most critical problem in LTCC technology. Development of new tape systems will bring the cost down while improving performance. Zero shrink tape, better thermal management techniques, lower loss, and lower/higher dielectric constant tapes for high frequency applications will allow LTCC technology to expand into even broader commercial and industrial applications.

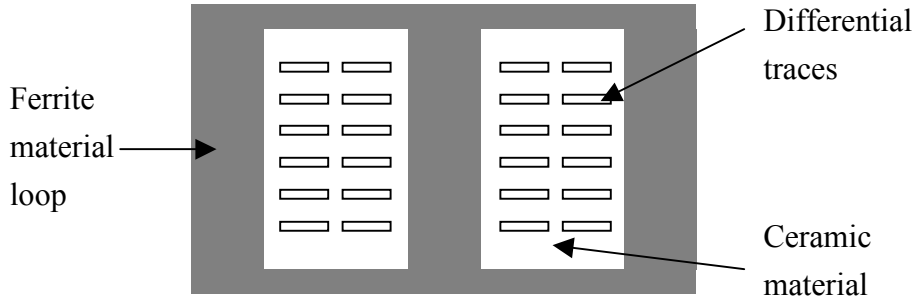



Fig. 5.1 Structure of common-mode filter with ferrite material loop.

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